UCC25800-Q1 Ultra-low EMI Transformer Driver for Isolated Bias Supplies

1 Features

- High-efficiency half-bridge transformer driver
- Ultra-low EMI with low interwinding capacitance
- Smaller and lower-cost transformer
  - Programmable frequency: 0.1 MHz to 1.2 MHz
- Wide input voltage range: 9 V to 34 V
  - 9 W from 34-V input
  - 6 W from 24-V input
  - 4 W from 15-V input
- Automatic dead-time adjustment with maximum dead-time programming
- External clock synchronization for low noise
- Robust protection features
  - Undervoltage lockout (UVLO)
  - Programmable over-current protection (OCP)
  - Input overvoltage protection (OVP)
  - Over temperature protection (TSD)
  - Integrated soft-start to reduce in-rush current
  - External disable function with fault-code output
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 8-Pin DGN package with thermal pad

2 Applications

- Automotive traction inverter & motor control
- Automotive on-board charger (OBC)
- Automotive DC/DC converter
- EV charging station, DC fast charging station
- UPS and solar inverters
- Industrial motors, elevators and escalators
- GaN, IGBT and SiC gate transformer driver bias supply

3 Description

The UCC25800-Q1 ultra-low EMI transformer driver integrates the switching power stage, the control, and the protection circuits to simplify isolated bias supply designs. It allows the design to utilize a transformer with higher leakage inductance, but much smaller parasitic primary-to-secondary capacitance. This low-capacitance transformer design enables an order of magnitude reduction in the common-mode current injection through the bias transformer. This makes the transformer driver an ideal solution for the isolated bias supply in various automotive applications to minimize the EMI noise caused by the high-speed switching devices. The soft-switching feature further reduces the EMI noise.

The transformer driver has a programmable frequency range of 100 kHz to 1.2 MHz. This high switching frequency reduces the transformer size and footprint, as well as the overall cost of the bias supply. The integrated SYNC function allows the system bias supplies to synchronize with an external clock signal, further reducing the system level noise.

The dead-time adjusts automatically to minimize the conduction loss and simplify the design. The programmable maximum dead-time ensures power stage design flexibility.

With the integrated, low-resistance switching power stage, the transformer driver can achieve a 6-W design with 24-V input, and up to 9-W from 34-V input. With a fixed input voltage, the open-loop control also helps the output regulation to remain ±5% when the load is above 10%.

The programmable overcurrent protection (OCP) allows flexibility on the power stage design to minimize the transformer size. The protection features such as adjustable OCP, input OVP, TSD and the protection from pin faults ensure robust operation. A fixed 1.5-ms soft-start period reduces the inrush current during start-up and fault recovery.

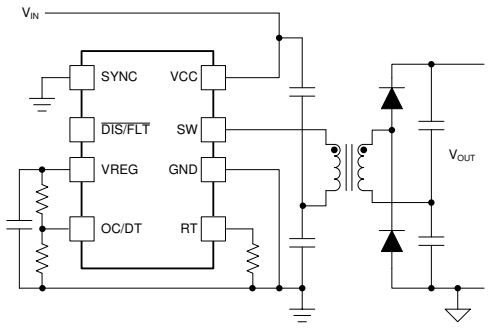
The transformer driver also provides a dedicated multi-function pin for external disabling, and fault code reporting. The fault code reporting sends the fault code once the bias supply is in the protection mode.

The UCC25800-Q1 transformer driver is offered in an 8-pin DGN package with the thermal pad to enhance its thermal handling capability.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCC25800-Q1	HVSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2021) to Revision C (August 2023)	Page
• Initial release of UCC25800B-Q1 device	1
• Updated to include new device UCC25800B-Q1	3
• Updated to include fault mode implications of new device UCC25800B-Q1	24

Changes from Revision A (July 2021) to Revision B (November 2021)	Page
• Updated data sheet status from *Advance Information* to *Production Data*	1

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5 Device Comparison Table

Part Number	OCP1 Protection
UCC25800-Q1	Enable
UCC25800B-Q1	Disable

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6 Pin Configuration and Functions

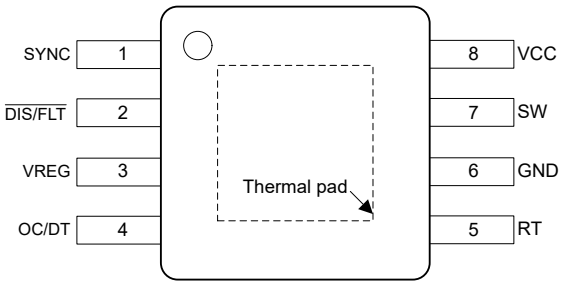

Figure 6-1. DGN Package, 8-Pin PDSO (Top View)

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{\text{DIS/FLT}}$	2	I/O	UCC25800-Q1 disable pin (active low) and fault code output pin.
GND	6	G	The GND pin is the return for all the control and power signals. The layout should separate the power and control signals.
OC/DT	4	I	Voltage on this pin sets the maximum dead-time between the internal switching power devices. The Thevenin resistance on the pin is measured at start-up to set the OCP level.
RT	5	–	Switching frequency setting pin. Connect a resistor from RT pin to GND to set the converter switching frequency. The RT pin can be left open to operate the converter at the default 1.2-MHz switching frequency.
SW	7	–	The switch node of the integrated half-bridge. Connect this pin directly to the transformer.
SYNC	1	I	External clock input for frequency synchronization. The internal MOSFETs are switched synchronized with the rising edge of the SYNC signal, with half of the SYNC pin signal frequency.
VCC	8	I	The input for power and control of UCC25800-Q1. A good high-frequency by-pass capacitor between VCC and GND is needed to ensure high-efficiency, low-EMI design. Use the bypass capacitor layout to minimize the VCC-GND-bypass capacitor loop to reduce the stresses on internal power devices. Referring to Section 11 for layout guidelines.
VREG	3	O	Internal regulated reference. Put a decoupling capacitor right across VREG pin and GND with shortest distance. The VREG pin can also be used as an external supply.
Thermal Pad		–	Connect this pad to GND pin to provide thermal management for the device. Thermal vias are recommended if the design uses multilayer PCB.

(1) I = input, O = output, I/O = input or output, FB = feedback, G = ground, P = power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC		–0.3	40	V
VREG		–0.3	5.5	V
RT		–0.3	5.5	V
$\overline{DIS/FLT}$		–0.3	5.5	V
SYNC		–0.3	5.5	V
OC/DT		–0.3	5.5	V
SW	Pin voltage	–1	VCC + 1	V
	Current transient (100ns)	–7	7	A
	Voltage transient (50ns)	higher of -5V or (VCC-41V)	Lower of (VCC+5V) or 41V	V
I_{Qrms}	MOSFET RMS current		600	mA
T_J	Junction temperature	–40	150	°C
T_{AMB}	Ambient temperature	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (SYNC, OC/DT, RT, and VCC)	±750	V
			Other pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	9		34	V
VREG	VREG current	0		1	mA
C_{VREG}	VREG capacitor	0.1		1	µF
R_{RT}	Switching frequency set pin resistor	10			kΩ
C_{RT}	Capacitor on RT			1000	pF
$\overline{DIS/FLT}$	Disable pin	0		VREG	V
OC/DT	OCP/Dead Time setting pin	1		3.9	V
$R_{OC/DT}$	Thevenin resistance	2.5		22.7	kΩ
$C_{OC/DT}$	Capacitor on OC/DT			1000	pF
SYNC	External sync input voltage	0		VREG	V
$t_{SYNCmin}$	Minimum SYNC pulse width, high	150			ns
	Minimum SYNC pulse width, low	150			ns

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SW	Half bridge output pin	–0.6		VCC + 0.6	V
f_{SW}	Switching frequency range	100		1200	kHz
IQ_{RMS}	Internal MOSFET RMS current rating			500	mA
IQ_{Peak}	Internal MOSFET peak current rating, steady state			1	A

7.4 Thermal Information

THERMAL METRIC(1)		UCC25800-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	47.9	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	59.1	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Unless otherwise stated: V_{VCC} = 15 V, R_{RT} = open, C_{VREG} = 470 nF, and -40 °C <T_J =T_A < 125 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$UVLO_R$	VCC turn on threshold	VCC rising	8	8.6	9	V
$UVLO_F$	VCC turn off threshold	VCC falling	7.5	8	8.5	V
OV_{SD}	VCC overvoltage shutdown threshold	VCC rising	35	37	39	V
OV_{RS}	VCC overvoltage reset	VCC falling	34	36	38	V
OV_{BLNK}	Overvoltage blanking time	V_{VCC} = 40 V	0.75	1.3	2	µs
SUPPLY CURRENT						
$IVCC_{UVLO}$	VCC current during UVLO	V_{VCC} = 7.5 V		200	500	µA
$IVCC_{RUN}$	Input current, not including FET current (3)	f_{SW} = 1.2 MHz, $\overline{DIS/FLT}$ = 1, SW open, I_{VREG} = 0 mA, VCC = 12 V		14	20	mA
$IVCC_{DIS}$	Supply current when disabled	No switching, $\overline{DIS/FLT}$ = 0, I_{VREG} = 0 mA		660	800	µA
VREG OUTPUT						
VREG	Internal regulated reference	I_{VREG} = 0 mA, $\overline{DIS/FLT}$ = 0	4.75	5	5.25	V
$VREG_{LINE}$	Line Regulation	I_{VREG} = 0 mA, 9 V ≤ V_{VCC} ≤ 34 V			10	mV
$VREG_{LOAD}$	Load Regulation	0 mA ≤ I_{VREG} ≤ 1 mA	-100			mV
$VREG_{OK}$	Threshold for VREG GOOD	VREG rising	4.05	4.5	4.95	V
$VREG_{LOW}$	VREG fault threshold	VREG falling	3.6	4	4.4	V
MOSFETs						
RDSON	On Resistance	PMOS I_{SW} = -500 mA		0.45	0.75	Ω
		NMOS I_{SW} = +500 mA		0.3	0.5	Ω
OSCILLATOR						
f_{SW}	SW switching frequency	V_{RT} = 0.25 V	94	100	106	kHz
		V_{RT} = 2.5 V	0.94	1	1.06	MHz
		Default switching frequency, RT open	1.128	1.2	1.272	MHz

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Unless otherwise stated: V_{VCC} = 15 V, R_{RT} = open, C_{VREG} = 470 nF, and -40 °C <T_J =T_A < 125 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWtol}	Tolerance	10 kΩ ≤ R_{RT} ≤ 100 kΩ	94		106	%
Duty	Duty cycle	RT open	49	50	51	%
RT_{SHORT}	Short circuit fault theshold		130	150	170	mV
RT_{OPEN}	Open-circuit default f_{OSC} threshold		2.9	3	3.1	V
SYNC						
$SYNC_{RISNG}$	SYNC rising threshold	V_{SYNC} rising	2.0	2.2	2.4	V
$SYNC_{FALLING}$	SYNC falling threshold	V_{SYNC} falling	1.53	1.7	1.87	V
ADAPTIVE DEAD-TIME						
DT_HS_{TH}	High-side dead-time detection threshold with respect to VCC	SW rising	-1.2	-1	-0.8	V
DT_LS_{TH}	Low-side dead-time detection threshold	SW falling	0.8	1	1.2	V
DT_HS_{DELAY}	High-side turn on delay	From SW crossing DT_HS_{TH} to HS turning on		20	45	ns
DT_LS_{DELAY}	Low-side turn on delay	From SW crossing DT_LS_{TH} to LS turning on		20	45	ns
PROGRAMMABLE MAXIMUM DEAD-TIME						
OC/DT_{SHORT}	short threshold for OC/DT pin		450	500	550	mV
OC/DT_{OPEN}	open threshold for OC/DT pin		4.3	4.5	4.7	V
DT_{MAX}	Programmable maximum dead-time	$V_{OC/DT}$ = 3.9 V	45	50	55	ns
		$V_{OC/DT}$ = 1.9 V	135	150	165	ns
OVER-CURRENT PROTECTION						
$I_{OCP1max}$	First level maximum OCP setting threshold	Low side only	0.9	1	1.1	A
$OCP1_{TO}$	OCP1 time out	Peak current exceeds threshold time out to trigger OCP1 fault	1.9	2.1	2.3	ms
$I_{OCP2max}$	Second level maximum OCP threshold	Low side and high side	4.25	5	5.75	A
$OCP2_{FILTER}$	OCP2 filter time	Continuous over-current to trigger OCP2 fault, low side and high side	80	100	120	ns
OVER-TEMPERATURE PROTECTION						
TSD	Thermal shutdown threshold	$T_J = T_A$ (1)		160		°C
T_{HYST}	Hysteresis	$T_J = T_A$ (1)		20		°C
ENABLE_DISABLE FUNCTION						
EN_{TH}	Enable threshold	$\overline{DIS/FLT}$ rising	2	2.2	2.4	V
DIS_{TH}	Disable threshold	$\overline{DIS/FLT}$ falling	1.53	1.7	1.87	V
I_{pd_DIS}	Internal pull down disable current	$V_{\overline{DIS/FLT}}$ = 5 V	650	750	850	µA
$RESTART_{DEL}$	Restart delay after fault (2)			100		ms

(1) Specified by design. No production tested.
(2) Specified by bench characterization. No production tested.
(3) This current includes the SW pin parasitic capaticor charge and discharge current. When operating with LLC, soft switching removes the capacitor charge and discharge current. Actual current is smaller.

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7.6 Typical Characteristics

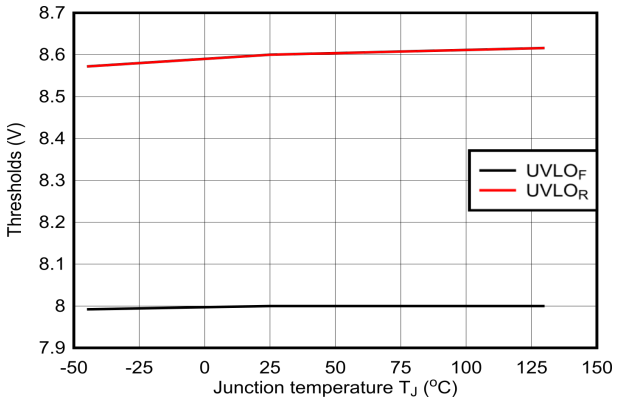


Figure 7-1. UVLO thresholds vs junction temperature

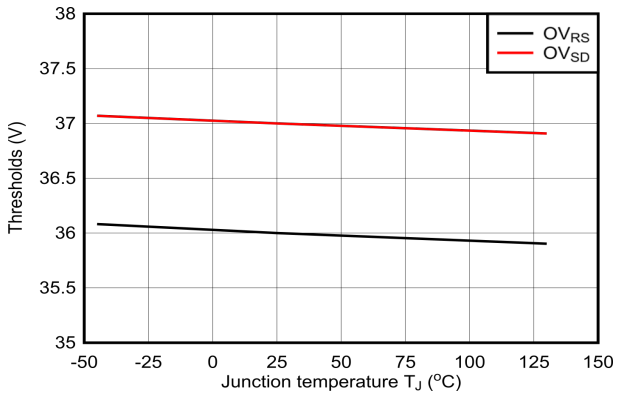
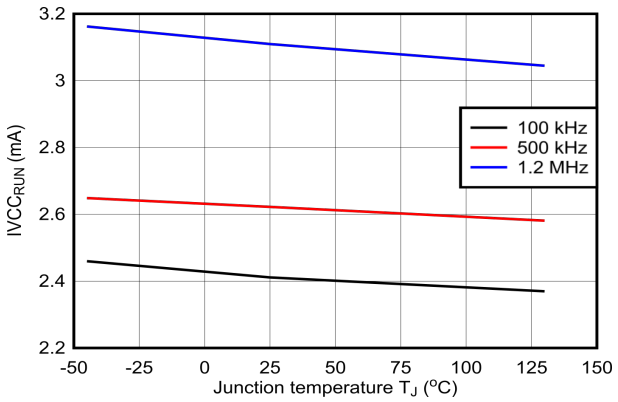
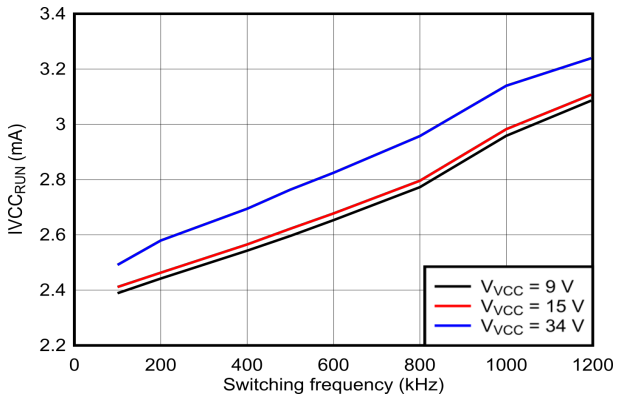


Figure 7-2. OVP thresholds vs junction temperature



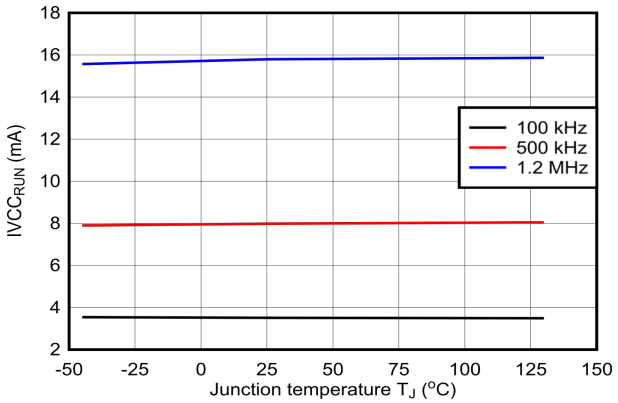
IC is set in test mode. The oscillator is enabled but the internal gate driver and power stage are disabled. V_{VCC} = 15 V

Figure 7-3. VCC current vs junction temperature and switching frequency (Test mode, driver disabled)



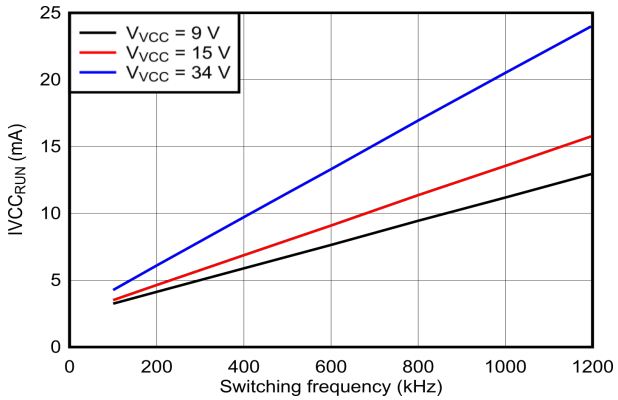
IC is set in test mode. The oscillator is enabled but the internal gate driver and power stage are disabled. T_J = 25 °C

Figure 7-4. VCC current vs switching frequency and VCC voltage (Test mode, driver disabled)



V_{VCC} = 15 V

Figure 7-5. VCC current vs junction temperature and switching frequency



T_J = 25 °C

Figure 7-6. VCC current vs switching frequency and VCC voltage

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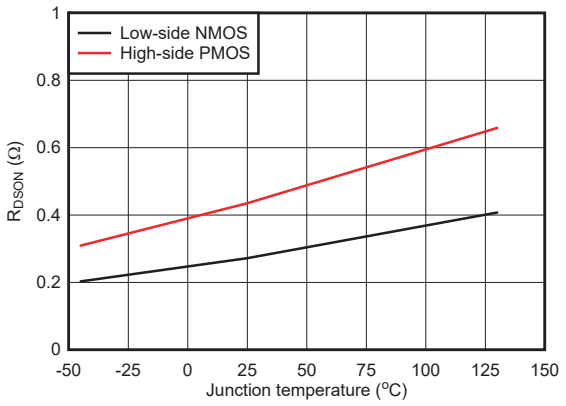
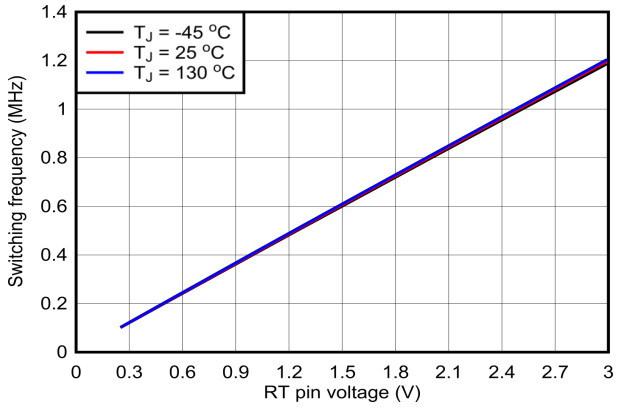
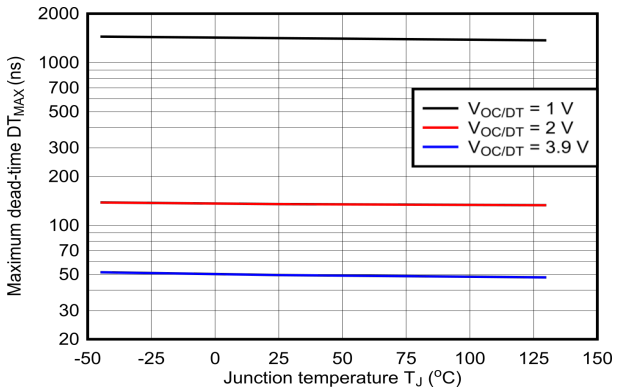


Figure 7-7. R_{DSON} vs junction temperature



V_{VCC} = 15 V

Figure 7-8. Switching frequency vs RT pin voltage and temperature



V_{VCC} = 15 V

Figure 7-9. Programmed maximum dead-time vs junction temperature

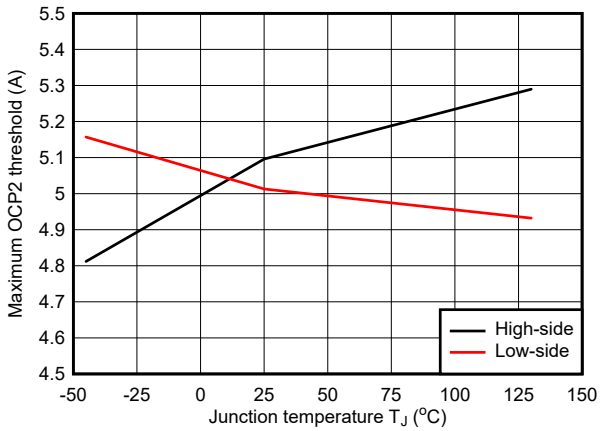


Figure 7-10. Maximum OCP2 thresholds vs junction temperature

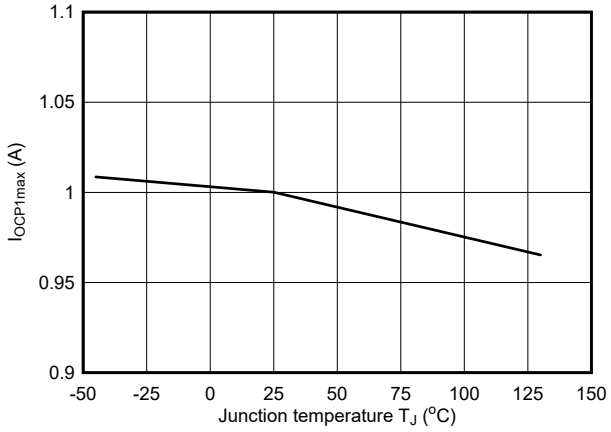


Figure 7-11. Maximum OCP1 threshold vs junction temperature

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8 Detailed Description

8.1 Overview

Modern high-voltage, high-power-inverter, and motor-drive applications require floating bias supply voltages to power at least the high-side totem-pole switches, where source (and gate) voltages move up and down with the inverter switch-node. The traditional way of providing small amounts of isolated bias power has been to use a flyback converter. Often a single flyback converter with multiple outputs can generate the required rails for all the switches. However, issues with reliability, redundancy, shock and vibration testing, noise immunity and particularly EMI and common mode current have led to a trend away from the flyback topology and centralized architecture toward distributed open-loop approaches. The open-loop approaches such as 50% duty cycle push-pull, open-loop half bridge or full bridge without an output inductor are deployed while the flyback converter or *flybuck* (an isolated buck converter) continue to be used by some designs to provide regulated outputs despite the larger common-mode capacitance (transformer primary-side to secondary-side parasitic capacitance). With the adoption of SiC and GaN devices, the inverter power stage switches at a much higher dv/dt. This behavior causes much larger common-mode current injection through the isolated bias transformers and drives the needs for a bias supply design with minimum parasitic capacitance. The need to further reduce the primary-to-secondary capacitance without suffering performance degradation has led some designs to deploy resonant topologies such as the LLC. As the leakage inductance in an LLC is a component of the power train, the topology can enable a higher leakage inductance transformer to be used with an associated reduction in the parasitic primary-secondary capacitance. The UCC25800-Q1 transformer driver is a small, simple controller enabling this topology to be deployed with low component count, integrated protection features, high switching frequency, high parameter tolerance and robust operation. An 8-pin DGN package with thermal pad is used to provide up to 6-W power handling capability with 24-V input.

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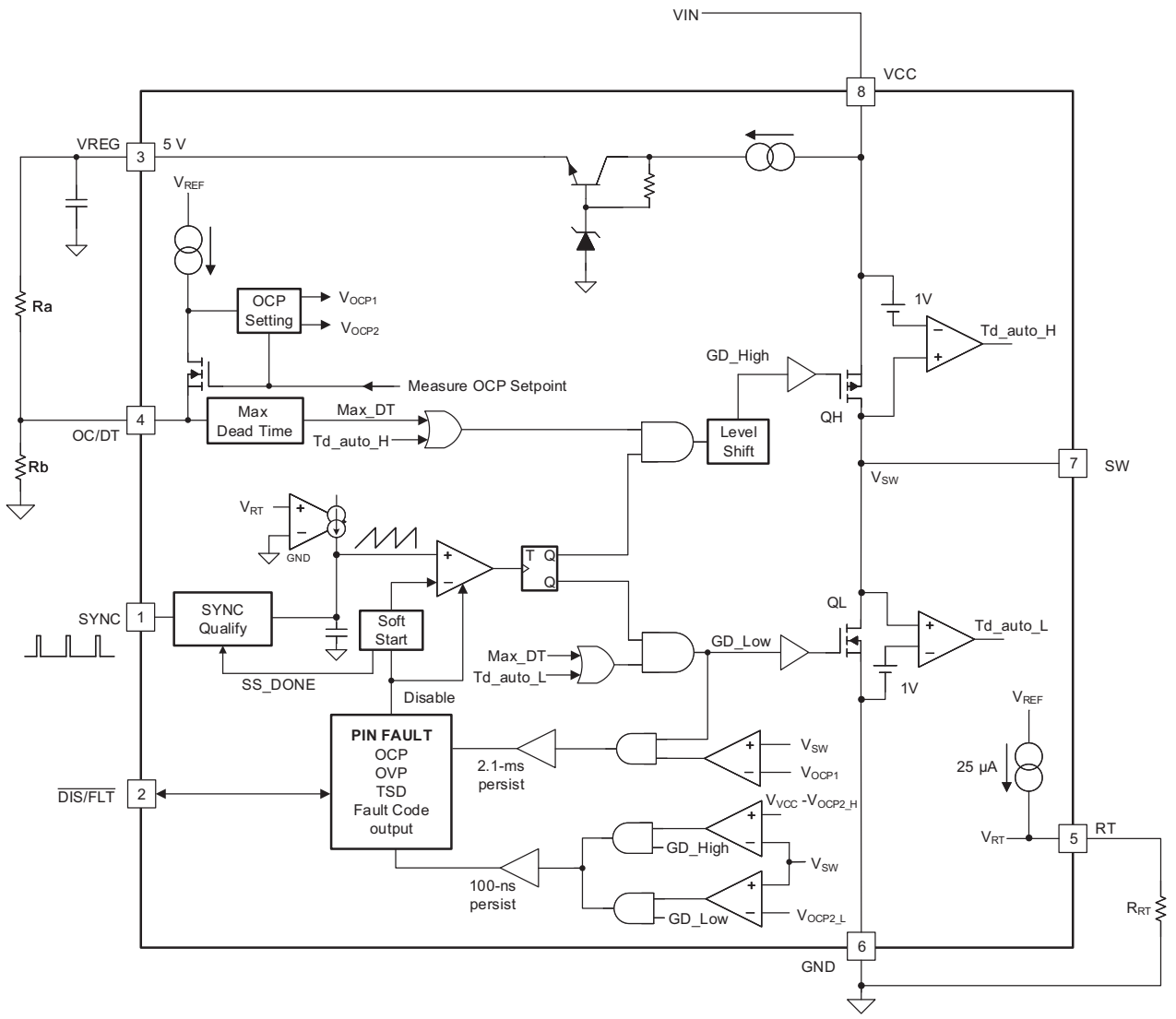
8.2 Functional Block Diagram



8.3 Feature Description

UCC25800-Q1 is an 8-pin open-loop half-bridge transformer driver that integrates all the control and power devices. It converts a fixed input voltage to an isolated voltage source through an isolation transformer. The relationship between the output voltage and input voltage is fixed, which is determined by the transformer turns-ratio and the rectification method. The open-loop control, together with the LLC resonant converter operation, makes the solution more robust, smaller size, higher efficiency, as well as lower EMI and common mode noise. The transformer driver requires a minimum of external components while providing design flexibility and robust protection features. The 1.2-MHz maximum switching frequency reduces the transformer size and cost, making it easier to pass the shock and vibration test in the automotive applications. The fault code output allows the designer to identify the protection mode, during the development stage, as well as during normal operation. This makes the development process much easier. It also enables the system controller to make intelligent decisions when bias supply faults happen.

8.3.1 Power Management

The VCC pin powers the UCC25800-Q1 transformer driver. When the VCC pin voltage is below the UVLO rising threshold ($UVLO_R$), the VREG pin 5-V regulator is disabled (VREG = 0 V). After the VCC pin voltage exceeds

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$UVLO_R$, the 5-V regulator is enabled and VREG pin rises, while the $\overline{DIS/FLT}$ pin is internally pulled low through an internal 750-µA current source, ($\overline{DIS/FLT}$ = 0 V). When the VREG exceeds 4.5 V ($VREG_{OK}$), the $\overline{DIS/FLT}$ pin is released. If the $\overline{DIS/FLT}$ pin is not pulled low externally, it rises to VREG pin voltage level via an internal 100-kΩ pull up resistor. When $\overline{DIS/FLT}$ pin voltage exceeds the rising enable threshold (EN_{TH}), the internal regulators and references are turned on and the transformer driver reads the Thevenin resistance on the OC/DT pin to set the overcurrent protection (OCP) thresholds. After this process completes, the faults are checked and if they are all cleared, the oscillator is enabled and the power stage starts switching. The time to complete this process is approximately 500 µs.

If a fault is detected, the transformer driver activates the internal pull-down current source on the $\overline{DIS/FLT}$ pin, the power stage stops switching, and the device outputs the fault code.

The rise time of the $\overline{DIS/FLT}$ pin depends on the external loading on the pin. An external pull-up can be added to the pin if there is concern over noise immunity. The values are specified in Section 8.3.6.

When the VCC pin voltage is above the $UVLO_R$ threshold and $\overline{DIS/FLT}$ pin is pulled low externally the transformer driver remains disabled with $IVCC_{DIS}$ = 660 µA.

If after a completed power-up sequence, VCC falls below the UVLO falling threshold ($UVLO_F$), the power stage switching is immediately stopped. The VREG pin voltage regulator is disabled making the VREG pin voltage fall.

The VCC pin current is a combination of the IC bias current and the power stage current. It is important to have a low ESL bypass capacitor to minimize the current loop among this capacitor and VCC, GND pins. Refer to Section 11 for details.

8.3.2 Oscillator

The internal oscillator of the UCC25800-Q1 transformer driver sets the switching frequency of the power stage. It operates at a 50% duty cycle. The voltage on the RT pin sets the oscilator frequency. A 25-µA current source flows out of the pin so that the switching frequency can be set by connecting a resistor to GND. Figure 8-1 shows the internal oscillator.

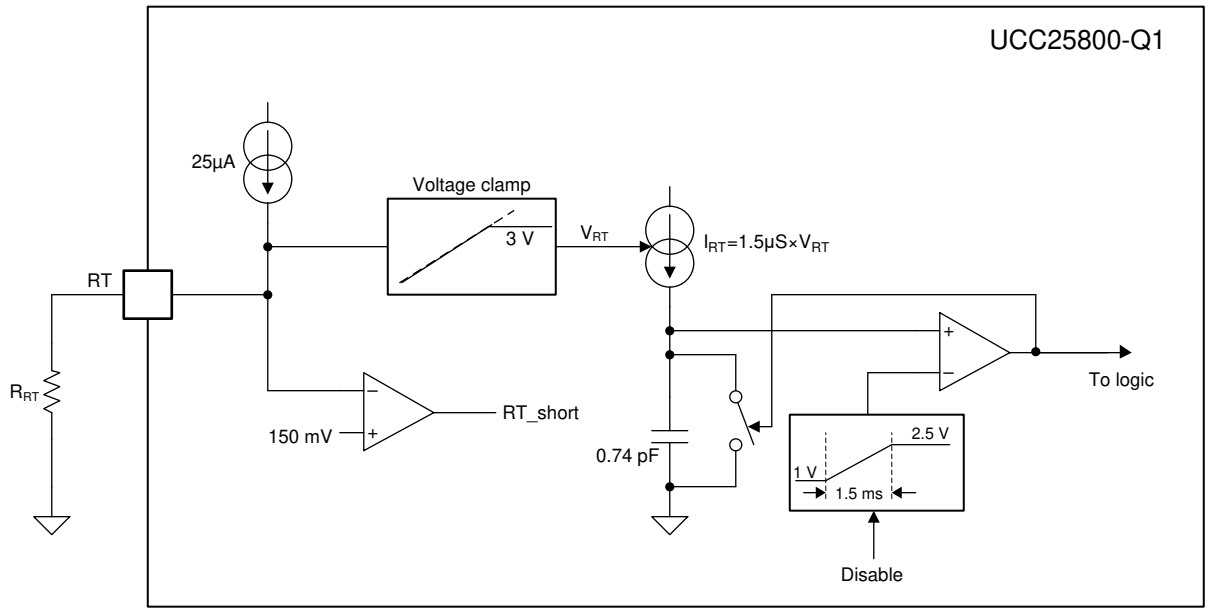

Figure 8-1. Equivalent circuit for internal oscillator

Use Equation 1 to calculate the RT pin resitance for a required switching frequency.

$$f_{SW} = R_{RT} \times 10 \frac{Hz}{\Omega} \quad (1)$$

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If the RT pin is left open, or an RT pin resistor value results in an RT pin voltage at RT_{OPEN} threshold or above, the power stage operates with the default switching frequency of 1.2 MHz. If the RT pin voltage is below 150 mV, the transformer driver considers the RT pin shorted to ground and declares a fault. The programmable voltage range on the RT pin is 250 mV to 2.5 V. The relationship between the power stage switching frequency and the RT-pin voltage is shown in Figure 8-2.

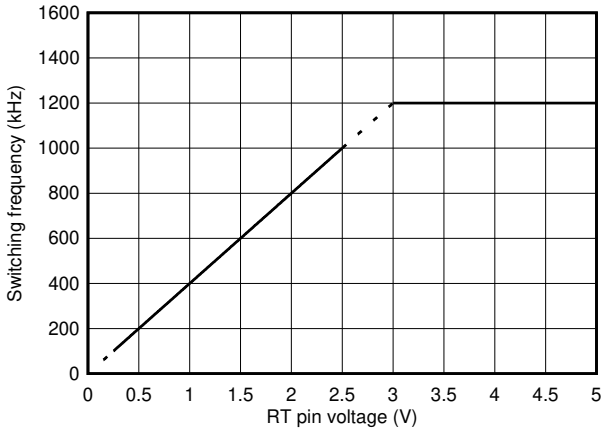

Figure 8-2. Relationship between switching frequency and RT-pin voltage

To avoid the excessive current stress during the start-up process, the transformer driver integrates a soft-start function. The oscillator starts by ramping the oscillator reference from 1 V to 2.5 V, which results in the switching frequency reducing from 2.5 times of the set frequency to the set frequency. Because the current source in the oscillator remains the same while the reference changes, the switching cycle decays linearly. The soft-start time is fixed internally at 1.5 ms. This long soft-start time limits the inrush current when charging large output capacitors. The soft-start is enabled during the start-up and fault recovery process. Figure 8-3 shows the switching frequency variation during the start-up time.

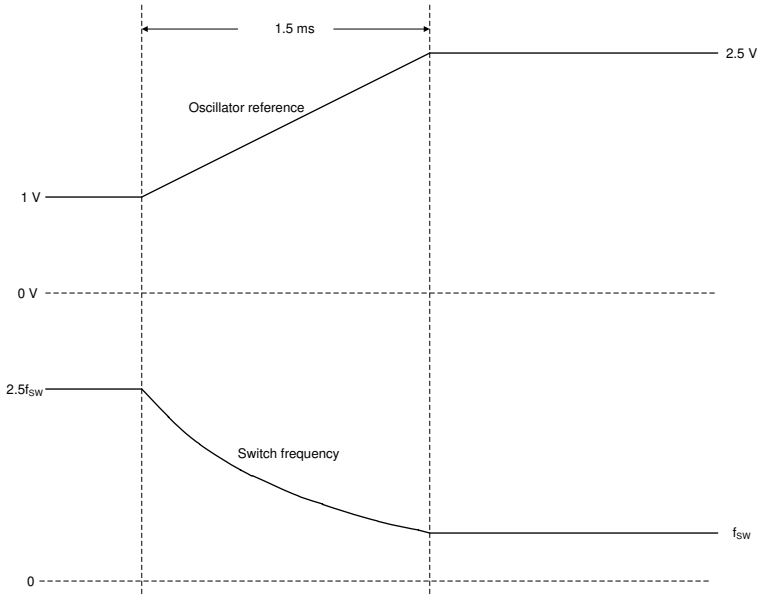

Figure 8-3. Switching frequency during soft start time

During the soft-start sequence, the first pulse from the oscillator is a half of the second pulse width (25% of the period at the starting switching frequency) and followed immediately by 50% duty cycle pulses. This process ensures the LLC transformer magnetizing current is symmetrical from the first pulse to minimize ringing in the system. The high-side switch is always turned on at the first pulse to avoid uncertainty of the circuit operation.

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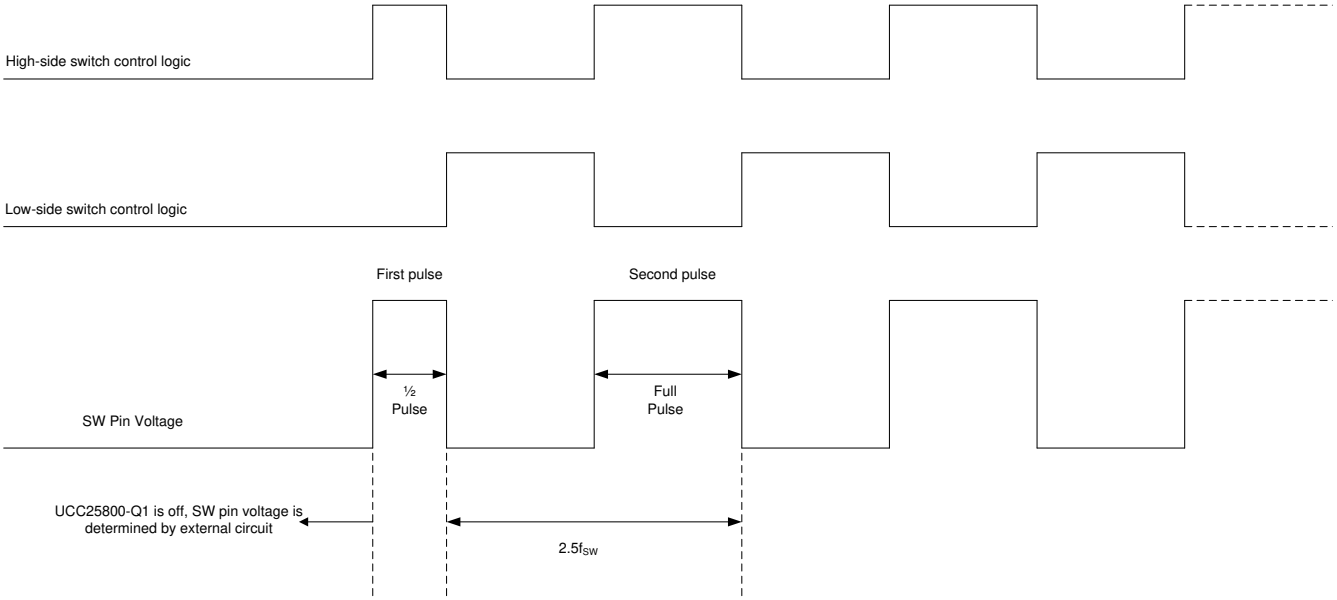

Figure 8-4. SW pin voltage and control logic at the first switching cycle (dead-time is not shown)

8.3.3 External Synchronization

An external signal connected to the SYNC pin synchronizes the switching frequency of the UCC25800-Q1 transformer driver.

In the external synchronization mode, the switching frequency of the SW pin is half of the SYNC pin signal frequency. Given that, to ensure the output voltage remains within the normal operation range, the half of the frequency of external synchronization signal needs to be between 15% and 30% (nominal) above the programmed switching frequency with a tolerance of 5% or less, as described in Equation 2. A minimum high and low pulse width of 150 ns is required. The SYNC pin logic is compatible with TTL and CMOS levels for the design simplicity. It is recommended to use 50% duty cycle signal.

$$1.15 \times f_{SW} < \frac{1}{2} \times f_{SYNC} < 1.3 \times f_{SW} \quad (2)$$

where

- f_{SW} is the RT pin programmed SW-pin switching frequency
- f_{SYNC} is the SYNC pin signal frequency

The transformer driver ignores the external synchronization signal during the 1.5-ms soft-start time. The switching frequency during the soft-start time is based on the RT pin voltage as described in Section 8.3.2. After the soft-start period ends, if an external synchronization signal is present and its frequency and pulse width are within the specified range, the switch node is driven by the SYNC pin signal. The transformer driver also integrates a hand-off algorithm so that when the switching frequency transitions from internal oscillator to the external synchronization signal, the disturbance is minimal and transformer saturation is avoided.

The hand-off algorithm first confirms that the external synchronization signal is within the range. If the frequency is not within the acceptable range, the hand-off doesn't happen. If the frequency is within the acceptable range, the hand-off algorithm begins to search for the optimal transition point and locks the switching frequency with the external SYNC signal. After the frequency is locked, the hand-off algorithm stops monitoring the SYNC pin frequency. It is important to ensure external synchronization source has a stable frequency. There is an internal watchdog timer to prevent the external frequency from falling below the set frequency (the watchdog time does not monitor if the SYNC pin frequency goes above the range). If the SYNC pin frequency drops below the set frequency, the transformer driver loses synchronization and the converter operates with the set frequency determined by RT pin voltage.

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The Figure 8-5 shows an oscilloscope screen capture for the controller transition from internal oscillator to the external synchronization signal. The smooth transition can be observed and the SW pin current sees minimal disturbance.

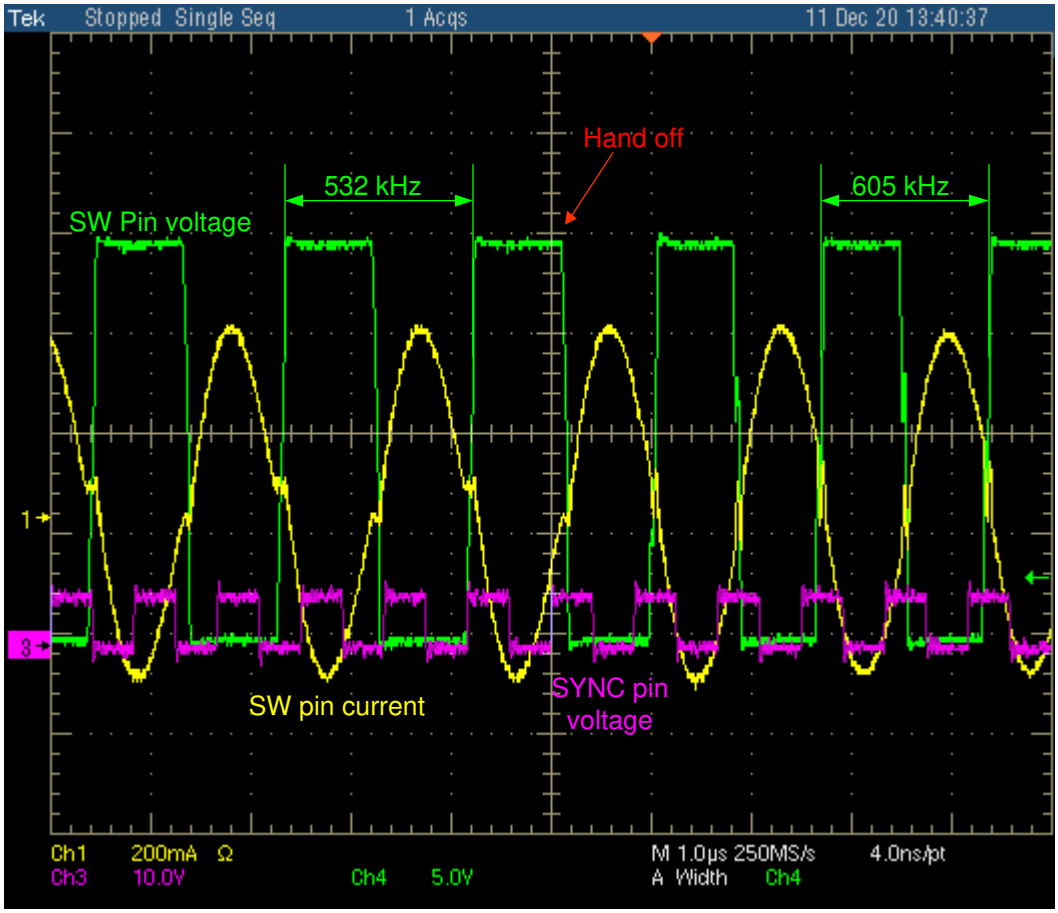

Figure 8-5. Transition from internal oscillator to external synchronization

The internal MOSFET gate drives are toggled on each SYNC pin voltage rising edge, so the switch-node frequency is equal to half of the SYNC pin signal frequency, as shown in Figure 8-6. Due to the internal filter delays, the SW pin switching edge is not aligned with the SYNC pin switching edge. There is a delay of approximately 150 ns.

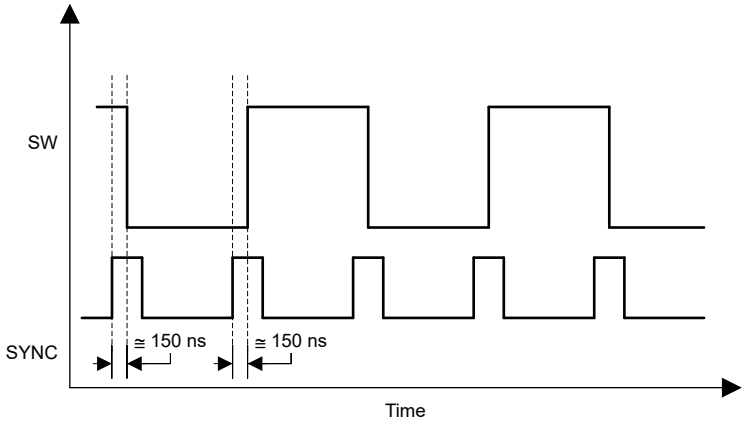

Figure 8-6. External SYNC signal drives switching frequency

8.3.4 Dead-Time

A dead-time is needed between the turn off of one switch and the turn on of the other switch to avoid shoot through. This also allows the switch-node voltage to transition to the opposite rail voltage, which reduces switching loss and EMI noise.

8.3.4.1 Adaptive Dead-time

The UCC25800-Q1 transformer driver automatically detects the dead-time after the switch-node voltage slews to within 1 V of the opposite rail. This slewing of the node is driven by the current flowing through the SW pin into the resonant tank at the end of the each MOSFET on-time. There must be sufficient current flowing through the SW pin at the end of the on-time to drive the SW pin voltage to the opposite rail. the voltage on the OC/DT pin programs the maximum dead-time. Even if the SW pin voltage crossing the threshold is not detected within the maximum programmed dead-time, the internal MOSFET switches on when the maximum programmed dead-time expires. Figure 8-7 and Figure 8-8 demonstrate the two adaptive dead-time operation conditions.

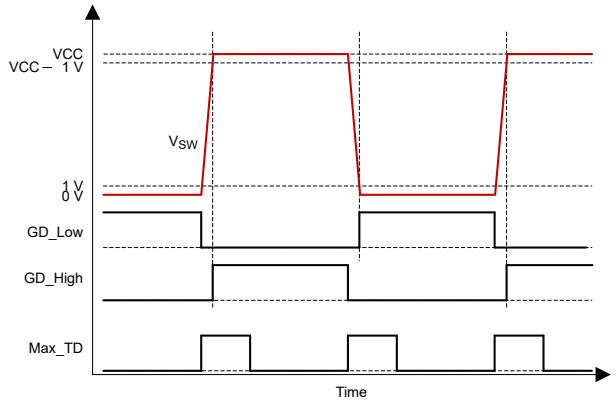

Figure 8-7. Adaptive dead-time operation without triggering maximum dead-time

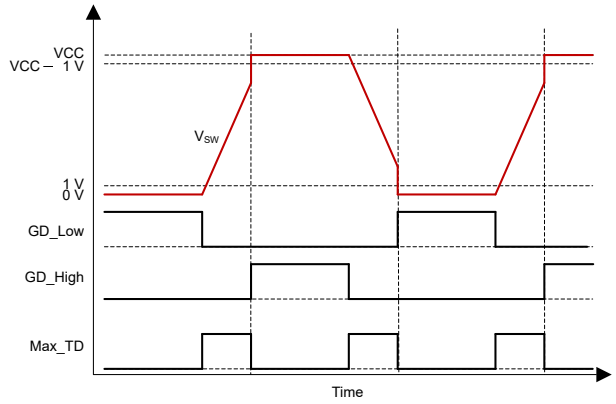

Figure 8-8. Adaptive dead-time operation with maximum dead-time

8.3.4.2 Maximum Programmable Dead-time

During operation, the voltage on the OC/DT pin sets a maximum duration of the dead-time. If the adaptive dead-time has not triggered the turn-on of the internal MOSFET within this time, it switches on when the maximum dead-time expires. The relationship between the OC/DT pin voltage and this maximum programmable dead-time is shown in Figure 8-9 and given by Equation 3. The UCC25800-Q1 transformer driver also limits the maximum dead-time to be 1/8 of the switching cycle. Therefore, the programmed maximum dead-time is the lower value of these two.

$$\mathrm{DT_{MAX}} = \frac{150\ \mathrm{ns} \times 1\ \mathrm{V}}{\mathrm{V_{OC/CT}} - 0.9\ \mathrm{V}} \tag{3}$$

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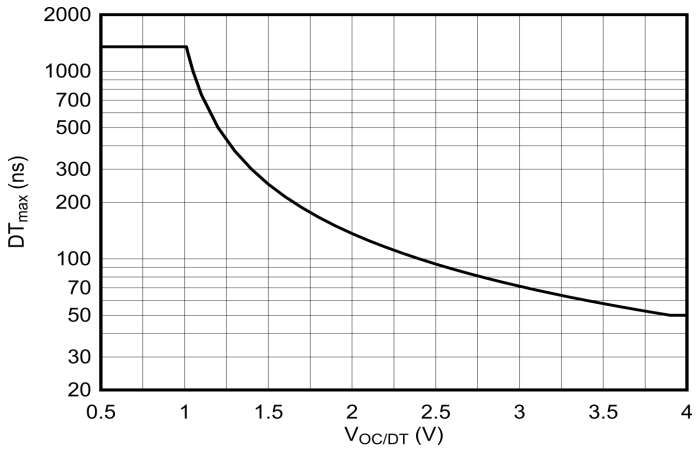

Figure 8-9. Maximum dead time vs. OC/DT pin voltage

When the OC/DT pin voltage falls below 0.5 V, the transformer driver triggers the pin-short protection and it shuts down. When the OC/DT pin voltage is between 0.5 V to 3.95 V, the maximum dead-time is set by Equation 3 with a clamped maximum value of 1.35 µs and a clamped minimum value of 50 ns. When the OC/DT pin voltage is between 3.95 V and 4.5 V, it triggers the DT-out-of-range fault and the transformer driver shuts down. When the OC/DT pin voltage is above 4.5 V, the transformer driver shuts down due to the OC/DT open pin fault protection.

8.3.5 Protections

UCC25800-Q1 transformer driver provides a full set of protection functions to improve the system level reliability, meeting automotive design requirements. The protection functions include programmable two-level over current protection (OCP), input undervoltage protection (UVLO), input over-voltage protection (OVP), and over-temperature protection (TSD). This design considers possible pin fault conditions such as pin open and pin short.. Extra protection mechanisms are also integrated inside the design.

8.3.5.1 Overcurrent Protection

The UCC25800-Q1 transformer driver has two levels of overcurrent protection (OCP).

- The first level (OCP1) triggers if the current through the low-side MOSFET exceeds programmed threshold I_{OCP} during its on-time in each switching cycle for 2.1 ms. Refer to OCP Threshold Setting for OCP1 threshold programming details.
  - OCP1 detection is based on only the low-side MOSFET current, when the SW pin current flows into the SW pin
- The second level (OCP2) triggers if the current in either the high-side or low-side MOSFET exceeds 5 × I_{OCP} for 100 ns.
  - The OCP2 threshold is set significantly above OCP1 threshold to allow the unit to cope with heavy load surges for a short duration, or during the start-up to charge the large output capacitor. If OCP2 is exceeded, it indicates that there is a serious fault in the system. OCP2 tracks OCP1 so that events like output overload can still trip OCP2, even if the current limit is set well below the maximum current limit of the transformer driver.
- During soft-start
  - The OCP1 is disabled
  - The OCP2 threshold is fixed at its maximum value of 5 A
- After soft-start
  - OCP1 is enabled, with the threshold I_{OCP} equal to the programmed value
  - OCP2 threshold becomes 5 times of the programmed I_{OCP} level.
- The OCP1 overcurrent timer is implemented as an up-down counter to ensure that the repetitive short over-current events as well as a sustained 2.1-ms over current trigger the OCP.
  - OCP1 overcurrent timer counts up if the SW current crosses I_{OCP} for longer than 100 ns in each switching cycle

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  - OCP1 overcurrent timer counts down if the SW current does not cross I_{OCP} for longer than 100 ns in the entire switching cycle
  - The internal counter for OCP1 overcurrent timer counts up in 2.1 ms from 0 to the trip threshold and counts down in 180 ms from the trip threshold down to 0.
- OCP2 detection has an analog filter which filters out pulses of less than 100 ns.

The transformer driver imposes a restart time of 100 ms before restarting from overcurrent protection to maintain the RMS current in the transformer driver below its limit. The OCP behaviors are illustrated in Figure 8-10 and Figure 8-11.

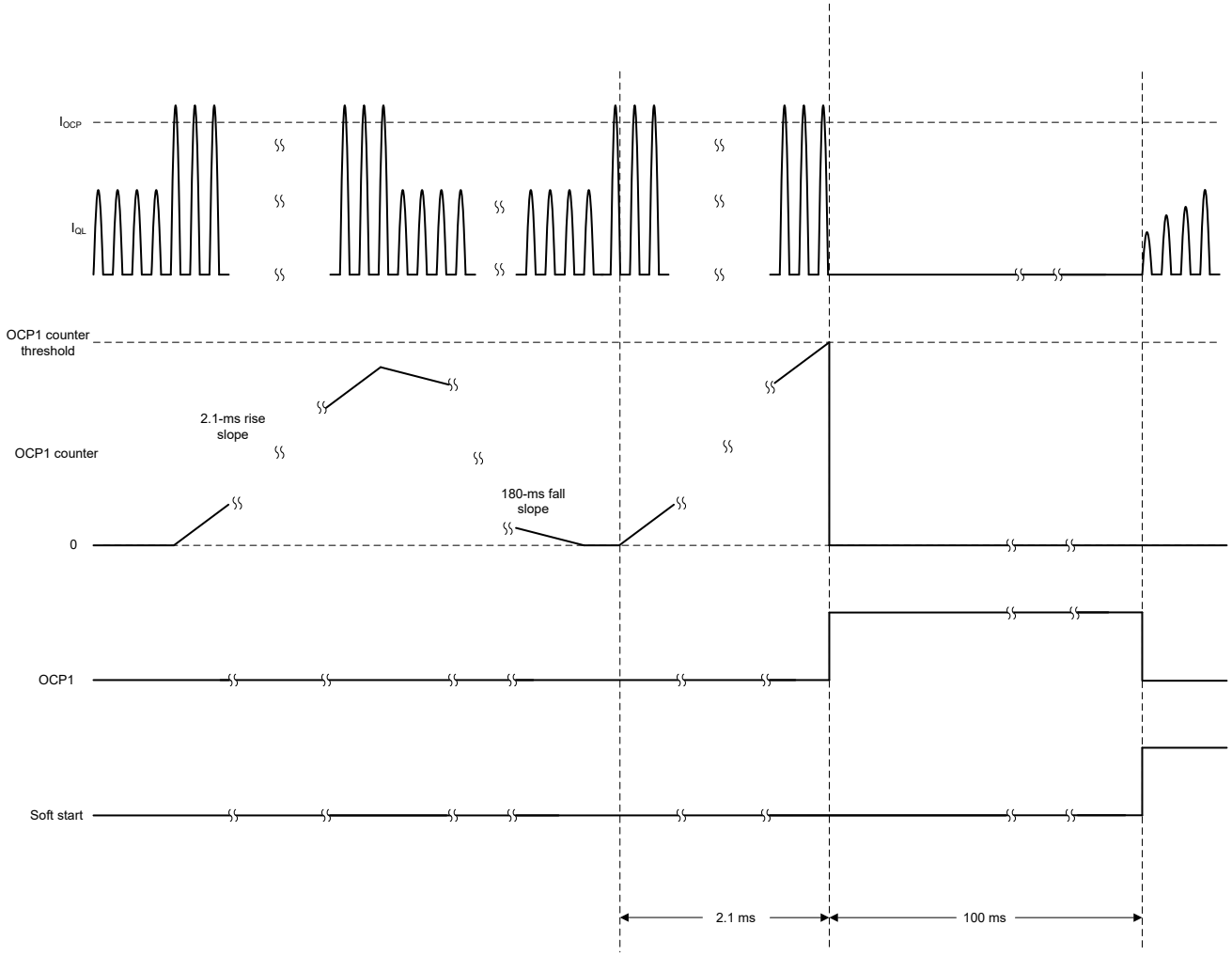

Figure 8-10. OCP1 protection and recovery behavior

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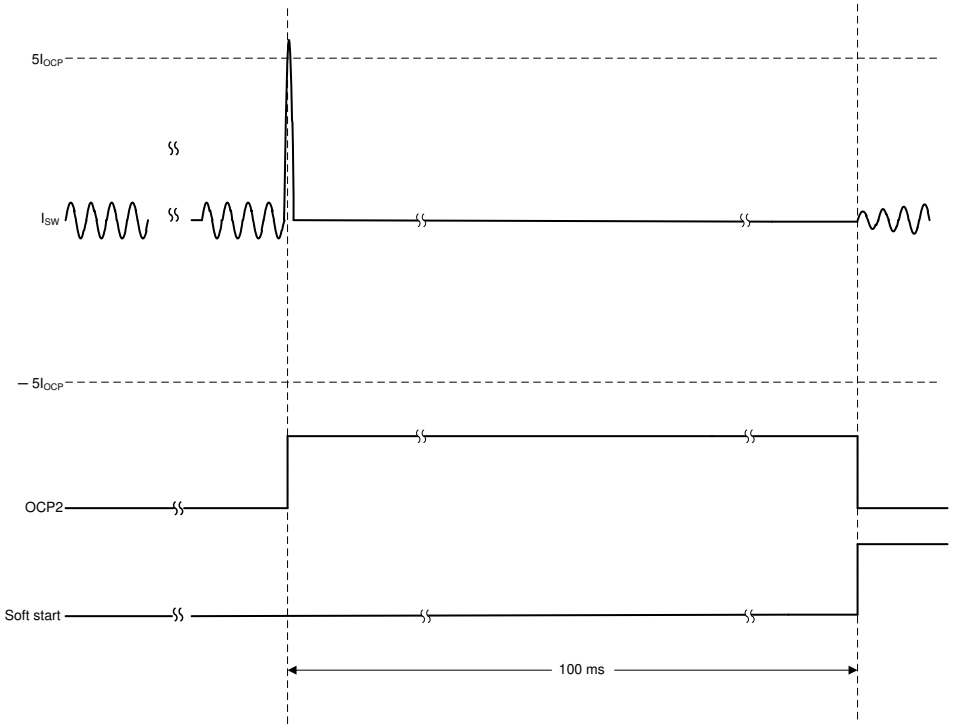

Figure 8-11. OCP2 protection and recovery behavior

8.3.5.1.1 OCP Threshold Setting

The UCC25800-Q1 transformer driver can support 6-W output power with 24-V input. For designs with lower power levels, the overcurrent protection (OCP) threshold can be adjusted accordingly to limit the maximum output power to improve the system reliability.

The OCP threshold setting shares the same pin as the maximum dead-time programming through OC/DT pin. During the transformer driver start-up sequence (after its VREG pin settles down to its final value) an internal 50-µA current source flowing out of OC/DT pin is turned on and off. The voltage on the OC/DT pin is measured at the current source on and off conditions. The measured voltage difference is used to set the OCP threshold. After the OCP setting is determined, the current source is turned off, so that the voltage on the OC/DT pin can be used for the maximum dead-time setting.

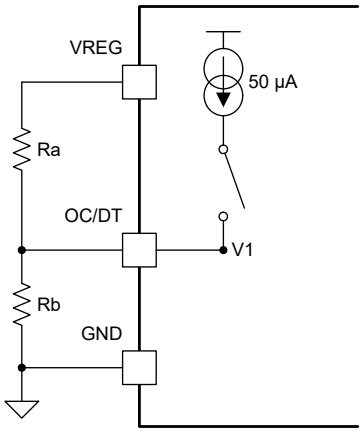

Figure 8-12. Current Source On

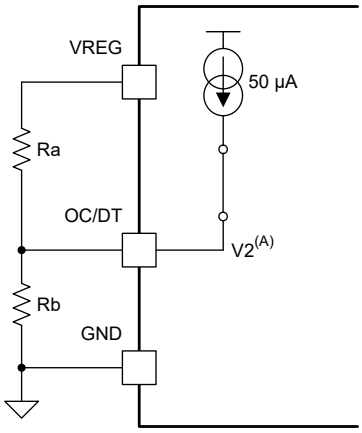

Figure 8-13. Current Source Off

According to the Thevenin theorem, the measured voltage difference is the current source multiplied by the Thevenin resistance on the voltage divider on OC/DT pin. The OCP settings using different Thevenin resistance are summarized in Table 8-1. The Thevenin resistance can be calculated using Equation 5.

$$\mathrm{Rth} = \frac{\mathrm{Ra} \times \mathrm{Rb}}{\mathrm{Ra} + \mathrm{Rb}} \tag{5}$$

Table 8-1. OCP Settings

	OCP1 _1	OCP1_2	OCP1_3	OCP1_4	OCP1_5	OCP1_6
R_{th}	22.25 kΩ ~ 23.15 kΩ	16.4 kΩ ~ 17 kΩ	11.7 kΩ ~ 12.1 kΩ	7.95 kΩ ~ 8.25 kΩ	4.9 kΩ ~ 5.1 kΩ	2.45 kΩ ~ 2.55 kΩ
OCP1 threshold (I_{OCP})	1/6 $I_{OCP1max}$	1/3 $I_{OCP1max}$	1/2 $I_{OCP1max}$	2/3 $I_{OCP1max}$	5/6 $I_{OCP1max}$	$I_{OCP1max}$
OCP2 threshold during soft-start	5 A	5 A	5 A	5 A	5 A	5 A
OCP2 threshold after soft-start	5/6 $I_{OCP1max}$	5/3 $I_{OCP1max}$	5/2 $I_{OCP1max}$	10/3 $I_{OCP1max}$	25/6 $I_{OCP1max}$	5 $I_{OCP1max}$

To ensure accurate reading of the Thevenin resistance, the time constant of Rth and any capacitance connected to the OC/DT pin should not be greater than 20 µs. For this reason, the maximum recommended capacitance on the pin is 1 nF. It is not required to add capacitance to the pin.

The OC/DT pin voltage during start-up is illustrated in Figure 8-14.

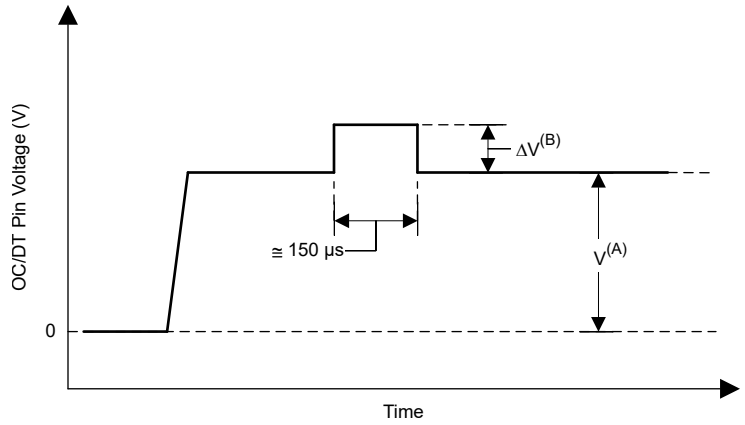

Figure 8-14. OC/DT pin voltage during start-up

A. $$\mathrm{V} = \mathrm{VREG} \times \frac{\mathrm{Rb}}{\mathrm{Ra} + \mathrm{Rb}} \tag{6}$$

B. $$\Delta \mathrm{V} = 50\ \mu\mathrm{A} \times \mathrm{Rth} \tag{7}$$

8.3.5.1.2 Output Power Capability

Figure 8-15 shows the output power capability of the UCC25800-Q1 transformer driver at different input voltages and switching frequencies with its highest OCP set-point (I_{OCP} = $I_{OCP1max}$ = 1 A), based on an input-output efficiency of 90%. There are two limiting factors on the power handling capability of the transformer driver; the OCP1 threshold and the thermal stress.

OCP1 serves as an over-power limit rather than over current protection since it has a 2.1-ms timer. Given its maximum value is 1 A and considering the sinusoidal current shaped, transformer driver limits its maximum output power proportionally to the input voltage. In Figure 8-15, the 100-kHz line is approximately the OCP1 limit.

The thermal limitation is to prevent the junction temperature of the transformer driver from becoming too high. Assuming its loss is only the IC bias consumption and the MOSFET conduction loss, at 125°C ambient temperature and 90% efficiency, the maximum output power creates the loss to make the junction temperature

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reach 150°C. Figure 8-15 shows that with higher the switching frequency, the IC power consumption increases and the maximum power capability decreases.

The power handling capability can be increased by increasing the input voltage or lowering the switching frequency, but it cannot exceed the OCP1 limit.

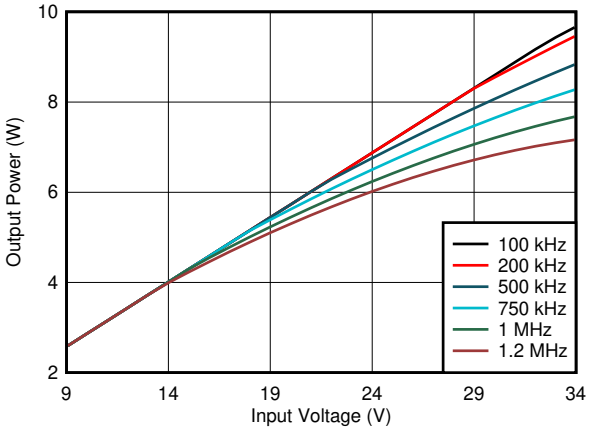

Figure 8-15. Power rating curves

8.3.5.2 Input Overvoltage Protection (OVP)

Due to the lack of feedback, UCC25800-Q1 transformer driver includes input overvoltage protection to prevent the output voltage from becoming too high, in case its input voltage becomes too high. If the VCC pin voltage exceeds the overvoltage set-point of OV_{SD} for overvoltage blanking time (OV_{BLNK}, 1.3 µs typical), the input overvoltage protection is triggered. When the input overvoltage protection is triggered, the fault mode is activated, stops the switching, and discharges the $\overline{DIS/FLT}$ pin and disables the transformer driver. Before restarting from an OVP fault, the input voltage must be below the OVP recovery threshold OV_{RS}. The transformer driver attempts to restart after 100 ms as described in Section 8.4.5.

The overvoltage protection threshold is a fixed value and cannot be programmed.

8.3.5.3 Over-Temperature Protection (TSD)

Over-temperature protection is required, primarily to stop the internal MOSFETs from failing in either high ambient temperature operation conditions or due to self-heating from high switching current. An over-temperature condition occurs when the junction temperature goes above the TSD threshold of 160°C (typical). In this case, the fault mode is activated, the switching stops, discharging the $\overline{DIS/FLT}$ pin and disabling the UCC25800-Q1 transformer driver. Before restarting from a TSD fault, the junction temperature must be below the overtemperature protection recover threshold (TSD-T_{HYST}). Over-temperature protection parameters are specified by design.

8.3.5.4 Pin-Fault Protections

Table 8-2 below shows the UCC25800-Q1 transformer driver response to open and short circuits on the pins. For example, the SYNC function operates on the rising edge of the SYNC pin. Hence if the pin is open or short the only impact is the loss of synchronization functionality. The transformer driver continues to operate as normal at the switching frequency programmed by the RT pin. .

Table 8-2. Pin Open and Short Response

PIN	OPEN	SHORT TO GND
SYNC	Normal operation with the programmed frequency	Normal operation with the programmed frequency
$\overline{DIS/FLT}$	Normal operation	OFF
VREG	OFF (VREG open protection)	OFF
OC/DT	Fault (OC/DT open protection)	Fault (OC/DT short protection)
RT	f_{SW} = 1.2 MHz	Fault (RT short protection)
GND	Unknown	-

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Table 8-2. Pin Open and Short Response (continued)

PIN	OPEN	SHORT TO GND
SW	V_{OUT} = 0	Fault (OCP) / ✖
VCC	OFF	OFF

Table 8-3. Pin-to-Pin Shorts Responses

1 2 3	SYNC	$\overline{\text{DIS/FLT}}$	VREG	OC/DT	VCC	SW	GND	RT
SYNC	–							
$\overline{\text{DIS/FLT}}$	– / OFF	–						
VREG	No SYNC	Always enabled	–					
OC/DT	– / OC/DT Fault	Indeterminate	Fault (OC/ DT_OPEN)	-				
VCC	✖	✖	✖	✖	–			
SW	✖	OCP Fault / ✖	✖	Fault / ✖	Fault / ✖	-		
GND	No SYNC	OFF	OFF	Fault (OC/ DT_SHORT)	IC not biased	Fault (OCP)/ ✖	-	
RT	Indeterminate	Indeterminate	Fault (RT_OPEN)	Indeterminate	✖	✖	Fault (RT_SHORT)	–

1. ✖ indicates that the transformer driver will or may become damaged.
2. – indicates no effect on the circuit operation.
3. *Indeterminate* indicates the IC behavior is unpredictable

8.3.5.5 VREG Pin Protection

The VREG pin is an internal linear regulator output and the bias pin for most of the internal circuits. It is important to ensure a good regulated voltage on VREG pin. A low ESL decoupling capacitor is recommended between VREG to GND. The layout should follow the Layout Guidelines.

VREG pin is equipped with two sets of protection functions to prevent the pin from being left open or over loaded from external circuit.

When VREG pin is left open, since there is no decoupling capacitor, the internal linear regulator becomes unstable. The UCC25800-Q1 transformer driver detects this condition, stops the operation, shuts down the internal linear regulator, and enters the latch-off mode. VCC must be recycled to clear this protection.

To prevent VREG pin from being over-loaded, the VREG pin has its own over-current protection. During start-up, when VREG pin voltage is below 1 V, the VREG pin current is limited to 15-mA, to protect the IC from short or over-load conditions. When the VREG pin voltage rises above 1 V, the VREG pin current limit increases to 40 mA for a fast start-up. When the voltage crosses the $VREG_{OK}$ value, the VREG pin current limit returns to 15 mA. Because the VREG pin provides current for both internal circuit and external circuit, it is recommended to maintain the VREF pin external load to a value less than 1 mA. When the external VREG-pin current is between 1 mA and 15 mA, excessive VREG pin current can cause the VREG pin voltage to drop. During normal operation, if the VREG pin is over loaded and its voltage drops below the $VREG_{low}$ threshold, the transformer driver shuts down the linear regulator and enters latch-off mode. VCC must be recycled to clear this protection.

8.3.6 $\overline{\text{DIS/FLT}}$ Pin operation

The $\overline{\text{DIS/FLT}}$ pin is an input/output pin. It can be

- Externally driven to enable or disable the transformer driver
- Read as a status flag telling whether the transformer driver is in fault mode or not and specifically what fault it is
- Left floating to enable the transformer driver by default

Internally the pin is tied high through a 100-kΩ pullup resistor from VREG. This pullup resistor activates only after the VREG pin is high. If the UCC25800-Q1 transformer driver enters the fault mode, the $\overline{\text{DIS/FLT}}$ pin is pulled low internally via a 750-µA current source. When the pin is low, switching is inhibited.

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The $\overline{\text{DIS/FLT}}$ internal pulldown current source is activated during the power-up sequence once the VCC voltage exceeds the UVLO rising threshold. After the VREG voltage has risen above the VREG_{OK} threshold, the pulldown current source is released and the $\overline{\text{DIS/FLT}}$ pin rises (unless it is externally pulled down). When the $\overline{\text{DIS/FLT}}$ pin voltage exceeds the EN_{TH} threshold, the transformer driver is enabled. When $\overline{\text{DIS/FLT}}$ pin falls below the DIS_{TH} the transformer driver is disabled. When the transformer driver is disabled its power consumption is reduced to IVCC_{DIS}.

If there is concern about noise coupling to the $\overline{\text{DIS/FLT}}$ pin it can be pulled up with an external resistor to an external rail or to VREG. In order to read the pin as a status flag, the external resistor value must be high enough that the 750-µA current source can pull the pin below the threshold level of the device reading the pin. It is recommended that the value for an external pullup resistor to 5 V is 10 kΩ and the value for an external pullup resistor to 3.3 V is 4.7 kΩ in order for the pin to be read as a fault output.

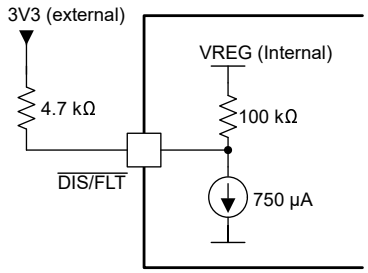

Figure 8-16. External Pullup for 3.3-V Supply

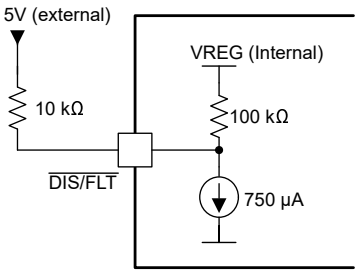

Figure 8-17. External Pullup for 5-V Supply

If the $\overline{\text{DIS/FLT}}$ pin functionality is not required, it can be left floating or tied to VREG to allow the transformer driver to operate normally.

8.3.6.1 FAULT Codes

When the UCC25800-Q1 transformer driver enters fault mode, it outputs a train of pulses to indicate which faults have occurred through the $\overline{\text{DIS/FLT}}$ pin. The pulse train consists of a number 50% duty cycle pulses at 50 kHz, (that is, 10-µs wide pulses), where the number of pulses indicates the fault listed in Table 8-4. The pulse train is created through controlling the internal 750-µA pull-down current source, together with the 100-kΩ pull-up resistor.

Table 8-4. Fault codes

NO. OF PULSES	FAULT
1	OCP1
2	OCP2
3	Input overvoltage protection
4	Over temperature protection
5	DT out of range
6	OC/DT open
7	OC/DT short
8	RT short
9	OTP (one-time-programmable bit) error

The pulse train starts 10 µs after the fault has been asserted. Transmission of the fault code begins with a 100-µs wide high pulse. If more than one fault is detected, the codes are transmitted successively based on the order in Table 8-4, separated by a 100-µs wide high pulse, as shown below in Figure 8-18.

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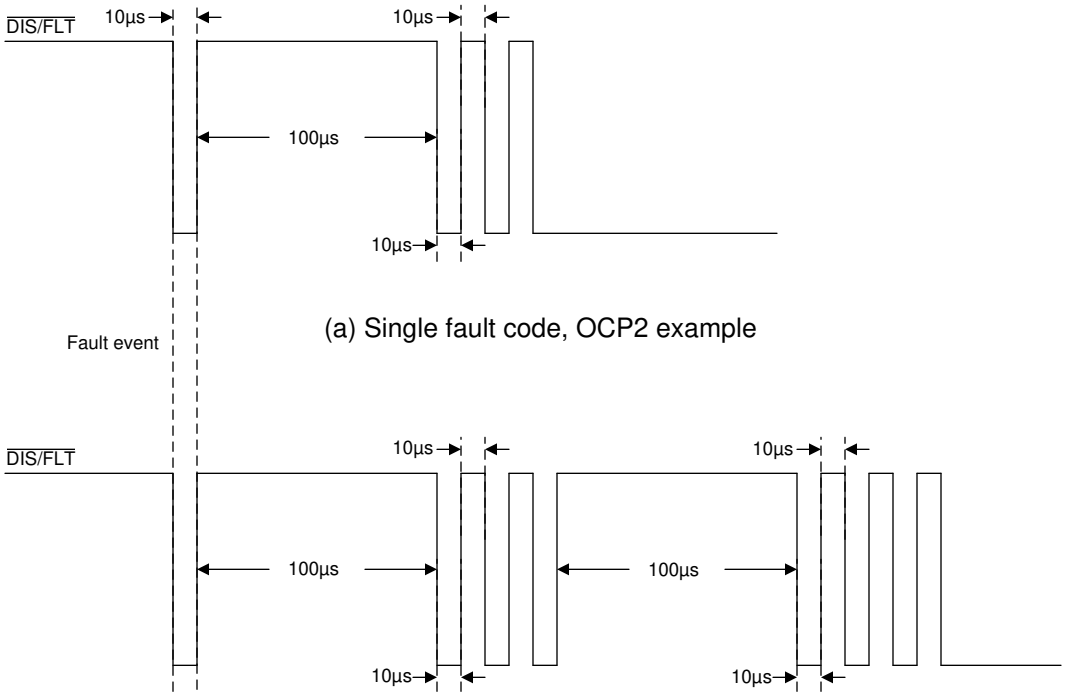

(a) Single fault code, OCP2 example

(b) Multiple fault codes, OCP2 and input over-voltage example

Figure 8-18. Fault code diagram

8.4 Device Functional Modes

Depending on the operating condition, the UCC25800-Q1 transformer driver can operate in different modes, including UVLO, soft-start, normal operation, disabled and the fault modes.

8.4.1 UVLO Mode

When the input voltage on VCC is less than the transformer driver UVLO threshold, the transformer driver is disabled. There is no switching on the SW pin and VREG is off.

8.4.2 Soft-start Mode

After the VCC voltage is above the UVLO threshold, all the faults are cleared, and $\overline{\text{DIS/FLT}}$ is released, the converter operates in the soft-start mode. During the soft-start period, the switching frequency gradually decreases to reduce the current stress. The soft-start period duration is 1.5 ms. The UCC25800-Q1 transformer driver always operates in soft-start mode during startup or after fault recovery. Refer to Section 8.3.2 for more details of soft-start mode.

8.4.3 Normal Operation Mode

Most of the cases, the UCC25800-Q1 transformer driver operates in the normal operation mode. The switching frequency is fixed, determined by eithert he RT pin voltage or external synchronization signal.

8.4.4 Disabled Mode

When the $\overline{\text{DIS/FLT}}$ pin is pulled low externally, the UCC25800-Q1 transformer driver enters disabled mode. In this mode, the VREG pin is regulated while the SW pin remains off. The VCC current consumption reduces to the disable current $IVCC_{DIS}$.

8.4.5 Fault Modes

Occasionally, different fault conditions occur and the UCC25800-Q1 transformer driver protects the system from more severe damage by entering the following fault modes.

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Table 8-5. Fault Mode Summary

FAULT	DESCRIPTION
Overcurrent (OCP1)	OCP1 occurs when the current in the internal low-side MOSFET during the low-side MOSFET on time exceeds I_{OCP} for 2.1 ms. UCC25800B-Q1 disables the OCP1 fault action.
Overcurrent (OCP2)	OCP2 occurs when the current in either MOSFET exceeds five times of the I_{OCP} for more than 100 ns. UCC25800B-Q1 keeps the same OCP2 setting and fault action as UCC25800-Q1.
Over temperature (TSD)	Over temperature protection (TSD) occurs when the junction temperature goes above TSD threshold.
Input overvoltage	Input overvoltage protection occurs when VCC voltage is above the overvoltage shut-down (OV_{SD}) threshold for more than 1.3 µs.
OC/DT open	OC/DT open protection occurs if the OC/DT pin exceeds 4.5 V after the OCP check has been completed.
OC/DT short	OC/DT short protection occurs if the OC/DT pin falls below 500 mV.
OC/DT out of range	OC/DT out-of-range protection occurs when the OC/DT pin voltage is between 3.95 V and 4.5 V during the OCP programming check.
RT short	RT short protection occurs when RT pin is below 150 mV.
OTP error	OTP error fault occurs when, during the OTP reading at start-up, the OTP sanity check fails. In case of OTP error fault, only OTP error fault code is transmitted while all other faults are ignored. The OTP error fault can be cleared only with a power cycle that forces a new OTP reading.

When any fault occurs the switching is immediately (after individual detection delays) stopped. The $\overline{\text{DIS/FLT}}$ pin is internally pulled down. After the fault codes are transmitted, the transformer driver current consumption is reduced to $IVCC_{DIS}$. The VREG regulator remains enabled and the RT pin remains at its programmed level.

When the transformer driver enters fault mode it pulses the pull-down current on the $\overline{\text{DIS/FLT}}$ pin on and off to output a fault code and signal which fault has been triggered as explained in Section 8.3.6.1.

After a delay time of 100 ms, the $\overline{\text{DIS/FLT}}$ pin is released and, if it is not pulled low externally. When it crosses the EN_{TH}, the transformer driver is enabled, the power up sequence occurs and the switching can start again. Before starting switching, the faults are checked again. If the protection that caused the fault condition still presents, or a new protection is triggered, the switching is not started and a new fault condition is asserted; fault codes are transmitted again. And the transformer driver current consumption is reduced to $IVCC_{DIS}$. This fault and power-up sequence is automatically cycled until all the faults are cleared.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The isolated bias supply is required in many applications, such as the gate driver bias for the traction inverters, on board chargers in electrical vehicles. It is also used in other sensing and control circuits in the electrical vehicles to minimize the noise or provide safety isolation. The open-loop LLC converter based on the UCC25800-Q1 transformer driver provides a reliable solution for these applications. It uses the open-loop control to improve the noise immunity. The LLC topology is able to operate at a higher switching frequency with soft switching, achieve high efficiency and low EMI, reducing the transformer size. Furthermore, the LLC topology is able to absorb the transformer leakage inductance as part of the resonant circuit. This absorption allows the transformer to have extremely low primary side to secondary side parasitic capacitance, which reduces the system level common-mode noise. The LLC topology also helps to simplify the transformer construction and reduces the transformer cost.

9.2 Typical Application

In the automotive traction inverters or on-board chargers, a regulated bus voltage is often generated from the 12-V battery and then processed by the isolated bias supplies to provide the gate driver bias power for the inverter switches, as shown in Figure 9-1. The isolated bias supply can be used to bias the high-side drivers or low-side drivers, to provide the isolation for function, safety, or noise immunity.

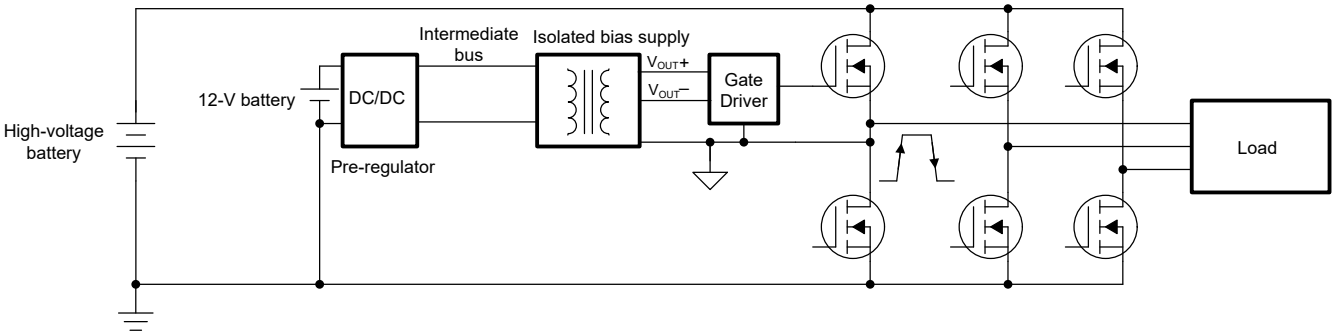

Figure 9-1. Gate driver bias supply example for automotive traction inverter

When the isolated based bias supply used in the inverter applications, especially for the high side switches, the high dv/dt on the inverter switch-node can couple through the bias supply transformer and causes extra EMI noise, as demonstrated in Figure 9-2.

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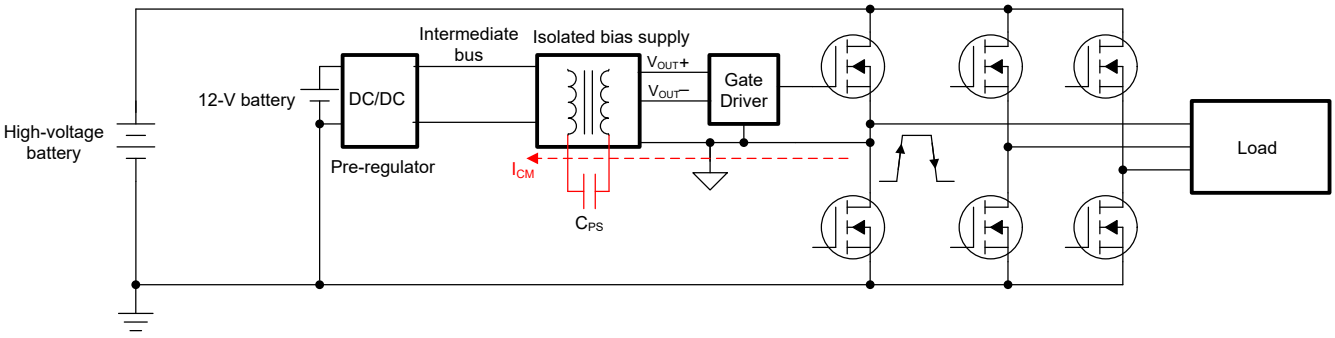

Figure 9-2. Noise coupling path from inverter power stage to isolated bias supply

Given the high dv/dt is caused by the inverter power stage, to minimize this noise coupling, it is desired to minimize the transformer primary side to secondary side parasitic capacitor (inter-winding capacitor) C_{PS}. Popular topologies, such as Flyback or Push-pull, require the minimum leakage inductance to improve the efficiency, reduce the voltage and current stress, as well as minimize the noise created by the converter. In turn, this type of transformers suffer from larger inter-winding capacitance. When they are used in the gate driver bias supply applications, the high dv/dt from the inverter power stage could be coupled through the transformer inter-winding capacitor to the low-voltage side. This creates a much severe EMI noise issue. Instead, the LLC topology utilizes the transformer leakage inductance as its resonant component, allowing the converter to use a transformer with larger leakage inductance but much smaller inter-winding capacitance. This results in less system EMI noise challenges.

9.2.1 LLC Converter Operation Principle

Different than the traditional PWM converters, LLC converters adjust the output voltage through varying the switching frequency. It is often called a PFM (pulse frequency modulation) converter. As shown in Figure 9-3, the LLC converter has three resonant elements, the resonant inductor (L_r), the magnetizing inductor (L_m), and the resonant capacitor (C_r). In the isolated bias supply design, the transformer leakage inductor, and the magnetizing inductor can be used as part of the resonant circuit. In this case, the only external resonant component is the resonant capacitor.

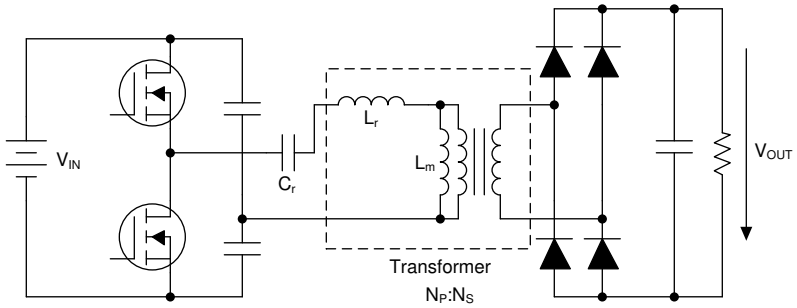

Figure 9-3. LLC Converter

At the resonant switching frequency (series resonant frequency of L_r and C_r), the impedance of the resonant tank (L_r and C_r) is equal to zero. The input and output voltage are virtually connected together through the transformer. Therefore, the gain of the converter is equal to the transformer turns ratio, as shown in Equation 8.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{2}\frac{N_S}{N_P} \tag{8}$$

In this equation, the ½ comes from the half-bridge architecture that the transformer primary side only sees half of the input voltage.

UCC25800-Q1 transformer driver controls the LLC converter to operate at a fixed switching frequency very close to the resonant frequency, to create an output voltage proportional to the input voltage, through a transformer turns-ratio. Depending on the location of the resonant capacitor, the LLC converter can be configured as

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primary-side resonant (as shown in Figure 9-3), or secondary-side resonant (as shown in Figure 9-4). When the resonant capacitor is moved to the secondary side, the magnetizing inductor no longer affects the converter gain. Therefore, the converter is less sensitive to the switching frequency and resonant component tolerances. The secondary-side resonant is more suitable for the open-loop LLC converter and it is a preferred configuration for transformer driver.

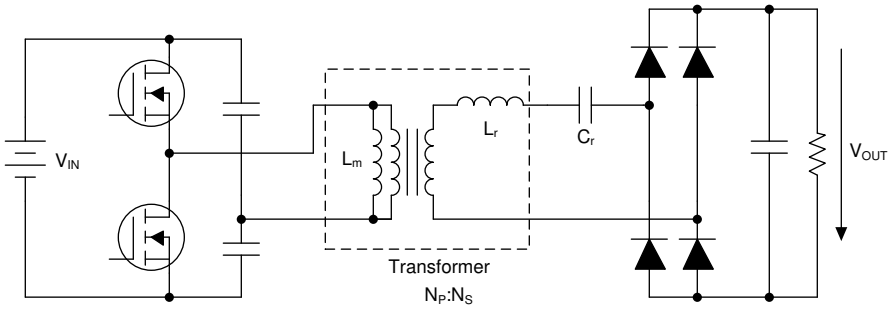

Figure 9-4. Secondary side resonant LLC converter

Furthermore, the secondary-side full-wave rectifier can be replaced with a voltage-doubler rectifier. Together with splitting the resonant capacitor into two, as shown in Figure 9-5, the converter configuration becomes simpler and fewer diodes are used. In this case, the transformer primary side sees half of the input voltage and the transformer secondary side sees half of the output voltage. The converter voltage gain becomes purely the transformer turns-ratio, as shown in Equation 9.

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \tag{9}$$

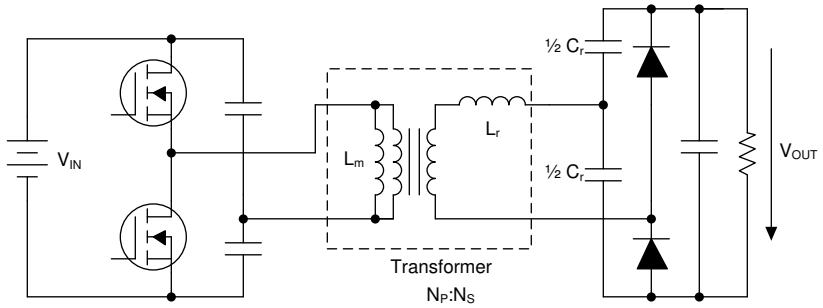

Figure 9-5. Secondary side resonant LLC converter with voltage doubler rectifier

The LLC operation waveforms are shown in Figure 9-6, when switching frequency is equal to the resonant frequency or below the resonant frequency.

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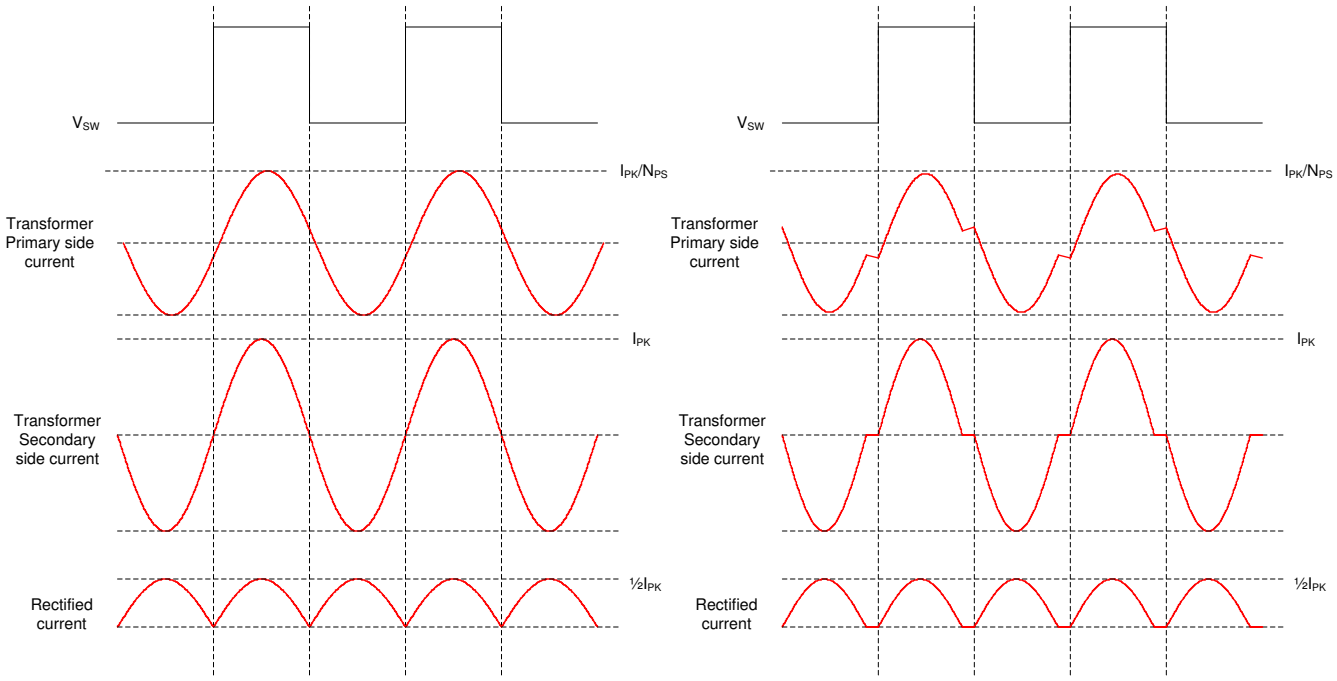

(a) Switching frequency equal to resonant frequency (b) Switching frequency below resonant frequency

Figure 9-6. LLC converter operation waveforms

9.2.2 Design Requirements

A 2-W traction inverter gate driver bias supply design demonstrates the design process based on the UCC25800-Q1 transformer driver.

Table 9-1. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Input Characteristics					
V_{IN}, Input voltage, DC			15		V
Output Characteristics					
V_{OUT1}, set point, DC		17.93	18.10	18.27	V
I_{OUT1}, output current range		0		85	mA
V_{OUT1}, regulation	I_{OUT1} = I_{OUT2}, 0 to full load	–1.0		1.0	%
V_{OUT2}, set point		–5.02	-4.98	-4.94	V
I_{OUT1}, output current range		–85		0	mA
V_{OUT2}, regulation	I_{OUT1} = I_{OUT2}, 0 to full load	-1.0		1.0	%
V_{OUT1}, peak to peak ripple	I_{OUT1} = I_{OUT2}, full load		50		mV
V_{OUT2}, peak to peak ripple	I_{OUT1} = I_{OUT2}, full load		35		mV
System Characteristics					
f_{SW}, switching frequency	Normal operation		500		kHz
I_{OC}, Over current limit			100		mA

9.2.3 Detailed Design Procedure

The design of the isolated bias supply based on the UCC25800-Q1 transformer driver involves both the power-stage design and the controller parameters design.

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The power-stage design involves the selection of the transformer and the resonant capacitors. Traditionally, the LLC transformer design is complicated because the design goal is to optimize the efficiency performance, the input and output voltage ranges, achieving ZVS, as well as minimizing the size of the transformer. It is a lot easier when design the transformer for the isolated bias supply because the design goal is to make it simple and robust. The efficiency is important but not critical since the gate driver power is a tiny portion of the overall system power.

Step 1: Transformer turns-ratio selection

Because this isolated bias supply operates with open-loop control, the voltage accuracy is not able to get down to 1%. The post regulators, such as a linear regulator can be used to achieve 1% regulation accuracy. Therefore, when designing the LLC converter output voltage, the headroom for the post regulator stage needs to be considered.

At the resonant frequency, together with the voltage doubler output, the LLC converter voltage gain is equal to the transformer turns-ratio. Therefore, the transformer turns-ratio can be calculated as:

$$\frac{N_P}{N_S} = N_{PS} = \frac{V_{IN}}{V_{OUT1} + V_{OUT2} + 2V_F + V_{headroom}} = \frac{15V}{18V + 5V + 2 \times 0.5V + 1V} = \frac{15V}{25V} = 0.6 \quad (10)$$

Where:

- V_F is the output diode forward voltage drop
- $V_{headroom}$ is the extra headroom needed for the post regulator

Step 2: Calculate transformer volt-second rating

The transformer volt-second rating on the primary side can be calculated as:

$$VS = \frac{V_{IN}}{2} \times \frac{1}{4f_{SW}} = \frac{15V}{2} \times \frac{1}{4 \times 500kHz} = 3.75V\mu s \quad (11)$$

Step 3: Calculate the transformer currents

The transformer sees highest RMS current right before over current protection. According to Figure 9-6, the output current is equal to the average current of the secondary-side rectified current. When load current is at the over current protection level of 100 mA, the primary side current can be calculated. The transformer primary-side and secondary-side peak and RMS current can be calculated based on Equation 12 through Equation 15.

$$I_{rmsS} = \frac{\pi}{\sqrt{2}} I_{OC} = \frac{\pi}{\sqrt{2}} \times 100mA = 222mA \quad (12)$$

$$I_{pkS} = \sqrt{2} I_{rmsS} = 314mA \quad (13)$$

$$I_{rmsP} = \frac{I_{rmsS}}{N_{PS}} = \frac{222mA}{0.6} = 370mA \quad (14)$$

$$I_{pkP} = \frac{I_{pkS}}{N_{PS}} = \frac{314mA}{0.6} = 523mA \quad (15)$$

From step 1 through 3, the key transformer information can be summarized in Table 9-2. It can be used to share with transformer vender to get the transformer designed and manufactured. It is recommended to leave some design margins (30%~50%) for the current ratings to consider the tolerance of the components.

Table 9-2. Transformer parameter summary

Parameter Name	Value	Unit
Primary side to secondary side turns ratio	0.6	
Primary side volt-second	3.75	Vμs
Primary side peak current	523	mA
Primary side RMS current	370	mA

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Table 9-2. Transformer parameter summary (continued)

Parameter Name	Value	Unit
Secondary side peak current	314	mA
Secondary side RMS current	222	mA

To minimize the transformer inter-winding capacitance, the split chamber bobbin is recommended, as shown in Figure 9-7.

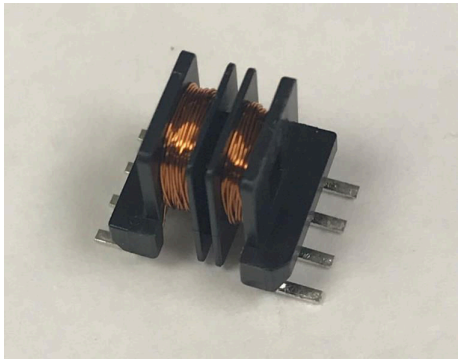

Figure 9-7. Split chamber bobbin

Another key transformer parameter is the magnetizing inductance. In traditional LLC converter design, the magnetizing inductor is used to achieve ZVS and the desired voltage gain to cover the entire input and output voltage range. Given the open-loop LLC operates with fixed input and output voltages, the sole goal of the magnetizing inductor is to achieve ZVS. Based on the ZVS criteria, the design target of the magnetizing inductance can be calculated based on Equation 16. In this equation, L_m is the magnetizing inductor value, t_d is the dead-time, f_{SW} is the switching frequency, and C_{SW} is the SW-pin parasitic capacitance (it has a typical value of 170 pF). With 500-kHz switching frequency and 50-ns of dead-time, the magnetizing inductance can be calculated as 73.5 µH. This inductor value gives an initial design target of the transformer and the final value can be different. If the magnetizing inductance is larger, it does not have enough magnetizing current to achieve full ZVS. With the low input voltage and small parasitic capacitance on the switch node, partial ZVS still brings in the EMI and loss reduction benefit. If the magnetizing inductance is smaller than the target, it'll create more current than needed, which results in extra conduction loss. But the loss increase is limited without causing concerns on the thermal stress or efficiency. Normally, it is recommended to use the core without an air gap, and the transformer magnetizing inductance is more than 20 times higher than the leakage inductance Otherwise, a minimum air gap is recommended without causing extra manufacture cost.

$$L_m = \frac{t_d}{8 C_{SW} f_{SW}} \tag{16}$$

Based on the calculation results, Wurth transformer 750319177 is selected to be the transformer. It has a turns ratio of N_{PS} = 1:1.67, which is 0.6. The magnetizing inductance measured from primary side is 16.5 µH and the leakage inductance measured from primary side is 0.75 µH. Given the secondary-side resonant is used, the leakage inductance should be measured from secondary side, with primary side shorted, at the resonant frequency. The secondary-side leakage inductance is measured as 1.4 µH.

Step 4: Select resonant capacitor

The resonant capacitor selection is based on the resonant frequency. Choose the resonant tank resonant frequency 10~15% above the switching frequency.

$$C_r = \frac{1}{4\pi^2 L_r f_r^2} = \frac{1}{4\pi^2 L_r (1.1 f_{SW})^2} = 60\text{nF} \tag{17}$$

When using the voltage double rectifier, each resonant capacitor value should be half of this value. Therefore, a 22-nF resonant capacitor can be used on each of the resonant capacitor.

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Step 5: Choose output capacitor

The output capacitor selection is based on the output voltage ripple requirement. The output capacitor can be calculated based on Equation 18. Design the capacitor based on half of the ripple amplitude so that there is margin for the voltage ripple caused by the capacitor ESR. Choose the output capacitor needs to consider both the ripple requirement and the gate driver requirement. A 10-µF capacitor can be used in this case. It should be noticed that the ceramic capacitor loses its capacitance when the voltage is applied.

$$C_{OUT} > \frac{0.421 \times I_{OUT}}{4V_{ripple}f_{SW}} = \frac{0.421 \times 85mA}{4 \times 50mV \times 500kHz} = 0.358\mu F \quad (18)$$

Step 6: Choose primary side DC blocking capacitor

The primary-side half-bridge DC blocking capacitors need to be much larger than the resonant capacitor. Given the high-switching frequency design, low ESR X7R capacitors with value between 1 µF and 10 µF are recommended.

Once the power stage is set up, the programming pins of the IC can be set up accordingly. Given the minimum external components, setting up the UCC25800-Q1 is extremely easy.

Step 7: Setting up RT pin resistor

To set the switching frequency to 500 kHz, according to the description in Oscillator, the RT pin resistor can be calculated as:

$$R_{RT} = \frac{f_{SW}}{10\frac{Hz}{\Omega}} = \frac{500kHz}{10\frac{Hz}{\Omega}} = 50k\Omega \quad (19)$$

Given 50 kΩ is not a standard resistor value, choose an R_{RT} value of 49.9 kΩ.

Step 8: Setting up OC/DT pin resistor divider

The OC/DT pin is a multi-function pin. It sets the maximum dead-time for the adaptive dead-time, and sets the OCP levels for over current protection.

For the dead-time setting, generally choose 5 % to 10% of the switching cycle, as the maximum dead-time. This value can be further adjusted according to the measurement result, depending on the soft switching conditions. Equation 3 calculates the voltage on DT/CT pin:

$$V_{OC/DT} = \frac{150ns \times 1V}{DT_{MAX}} + 0.9V = \frac{150ns \times 1V}{\frac{0.05}{500kHz}} + 0.9V = 2.4V \quad (20)$$

The OCP setting is determined by the primary-side peak current. In Equation 15, the primary-side peak current is calculated as 523 mA. Leaving extra 30% margin, the OCP1 level should be roughly 680 mA. OCP1_4 can be used as the OCP1 setting.

According to Table 8-1, the Thevenin resistance should be between 7.95 kΩ and 8.25 kΩ. We can use the value in the middle to set up the resistor and verify the Thevenin resistance after the resistor values are calculated,

The pull-up resistor can be calculated as

$$Ra = \frac{Rth \times V_{REG}}{V_{OC/DT}} = \frac{8.1k\Omega \times 5V}{2.4V} = 16.875k\Omega \cong 16.9k\Omega \quad (21)$$

And the pull-down resistor can be calculated as

$$Rb = \frac{Rth \times V_{REG}}{V_{REG} - V_{OC/DT}} = \frac{8.1k\Omega \times 5V}{5V - 2.4V} = 15.58k\Omega \cong 15.4k\Omega \quad (22)$$

It can be seen, due to the limited standard resistor value, the selected resistor values are different than the calculated resistor values. The Thevenin resistance needs to be checked. In this case, the Thevenin resistance is 8.058 kΩ and it is within the OCP1_4 setting range.

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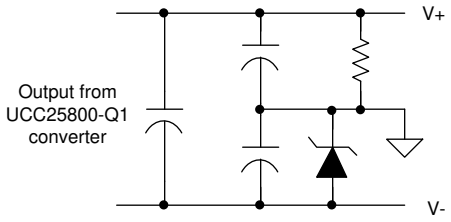
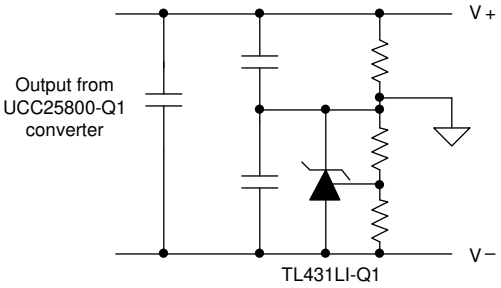
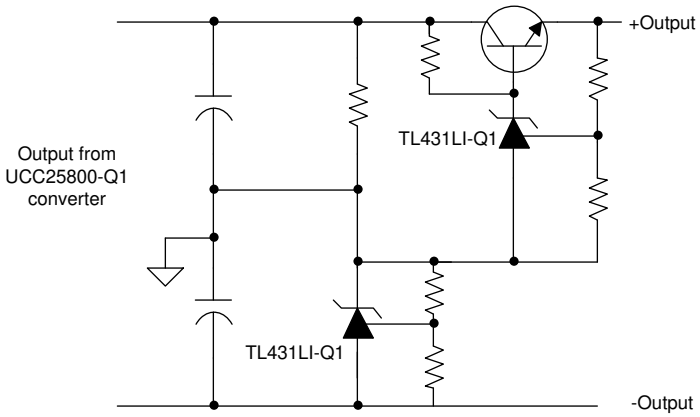
The UCC25800-Q1 based LLC converter can output a single output. It needs some help to split it into the dual outputs needed for the final designs. Depending on the regulation accuracy requirement, the splitting can be done using a simple Zener diode, a shunt-regulator, or even with a linear regulator, as demonstrated in Figure 9-8.



(a) Split the output voltage using Zener diode



(b) Split the output voltage using shunt-regulator



(c) splitting the output voltage using shunt-regulator and linear regulator

Figure 9-8. Different ways of splitting single output voltage to positive and negative outputs

Using the Zener diode, the negative rail voltage is determined by the Zener voltage and the rest of the output voltage becomes the positive rail. Due to the tolerance of the Zener diode, a shunt-regulator can be used to improve the negative rail voltage accuracy. Furthermore, a linear regulator can be added to improve the positive rail voltage accuracy as well. The designer can choose the right solution based on the performance and cost tradeoffs.

In this design, the shunt-regulator and linear-regulator are used to get 1% accuracy required for the positive and negative rail. ATL431-Q1 is used as the shunt-regulator and the voltage reference for the linear regulator. Given the reference voltage of ATL431-Q1 is 2.5 V, to create 5-V shunt-regulator voltage, a 1-kΩ and 1-kΩ voltage divider can be used to set up the 5-V regulation voltage. On the positive rail side, to create 18-V output voltage, 6.34 kΩ and 1 kΩ can be used to set up the output voltage divider ((6.34+1)×2.5V=18.35V).

With all the calculated circuit parameters, the design schematic is shown in Figure 9-9.

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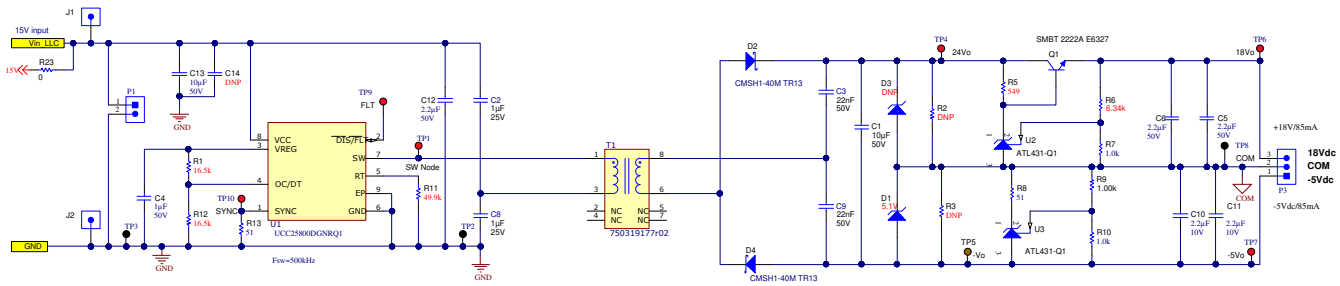

Figure 9-9. Circuit schematic for the designed isolated bias supply

9.2.4 Application Curves

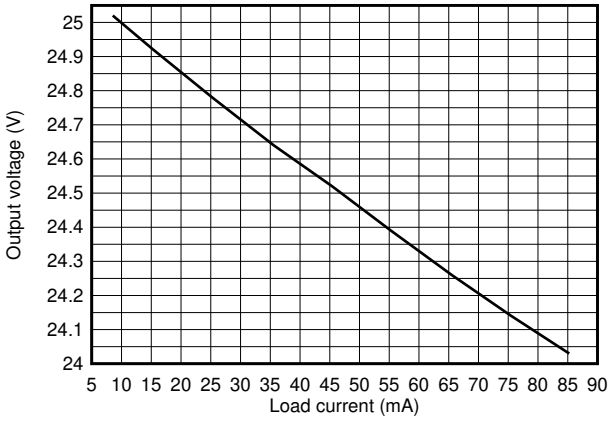

Figure 9-10. LLC output voltage load regulation

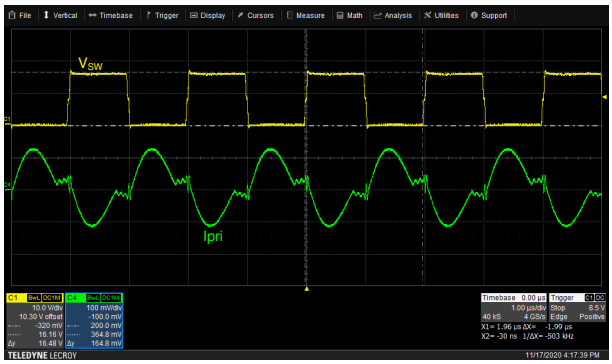

Figure 9-11. Switch-node Voltage (yellow) and Current (Primary side, 0.2V/A) at Full Load

9.3 What to Do and What Not to Do

Do

- Good decoupling between VCC and GND, minimize the loop of VCC-GND and the decoupling capacitor
- Use transformer with split chamber bobbin to minimize the EMI noise coupling from the inverter power stage
- The UCC25800-Q1 transformer driver can be used to drive single higher power transformer or multiple lower power transformer
- Setting the OCP1 level according to the designed load
- Use post regulator if the voltage regulation requirement can't be met
- Add Zener clamp at output if the output load can be completely removed
- If cost is acceptable, use NP0 or C0G type resonant capacitor, or use X7R with much higher voltage rating than needed
- Sufficient copper area for thermal management if the ambient temperature is high or the power level is high

Not to Do

- Long VCC-GND decoupling capacitor trace
- Set up the OCP1 to the highest level for all designs

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10 Power Supply Recommendations

The UCC25800-Q1 transformer driver drives an LLC converter with constant switching frequency to make the LLC converter operate near its resonant frequency. When LLC converter operates at its resonant frequency, the impedance of the resonant tank is equal to zero. The input and output voltages are virtually connected together, through the transformer turns-ratio. Given the LLC converter is a half-bridge converter, the transformer primary side only sees half of the input voltage. If the secondary side uses voltage double rectifier, it also only sees half of the output voltage. The relationship between the input and output voltages is simply the transformer turns-ratio.

Given that, to achieve a fixed output voltage, the input voltage needs to be fixed. Even though the transformer driver is recommended to operate with an input voltage source between 9 V and 34 V, it is meant to be one fixed voltage within this voltage range. Because the relationship between input and output voltages is simply the transformer turns-ratio, the accuracy of the input would impact the accuracy of the output. There is no requirement from the transformer driver, while the input voltage accuracy is demanded by the output voltage requirements.

When the input voltage is very close to 9 V (because it is very close to the UVLO threshold $UVLO_F$) sufficient input bypass capacitor is recommended to ensure the load transient does not cause the VCC voltage drops below UVLO threshold $UVLO_F$.

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11 Layout

Given the minimum external components, transformer driver layout is straightforward. The main considerations are the power loop and the grounding.

11.1 Layout Guidelines

- The most important layout guideline is to minimize the VCC-GND-bypass capacitor loop. Because this loop carries all the switching current, it is important to have a low ESL bypass capacitor between VCC and GND, with the minimum loop. Refer to Layout Example for how to layout the bypass capacitor on VCC to GND.
- Return all control signals to GND pin through a separated plane. Avoid sharing path between the signal ground and the power ground. Use a short trace to connect GND pin to the thermal pad.
- Separate the power stage components and signal component to minimize the coupling between these components
- Short VREG-GND-decoupling capacitor loop is recommended. A low ESL decoupling capacitor between VREG and GND is needed to ensure stable operation of the internal linear regulator.
- Add decoupling capacitors on RT and DT/OC pin to improve the noise immunity if it is needed. Refer to Section 7.3 for recommended maximum capacitor values.
- Short SYNC pin to GND when external synchronization is not used.
- Minimize the current loop with high di/dt and minimize the copper area of the switch-node with high dv/dt.
- Other general power supply design layout guidelines.
- The secondary side of the LLC converter is often connected with the high dv/dt node in the end equipment. In these cases, it is recommended to minimize the secondary-side copper area.

11.2 Layout Example

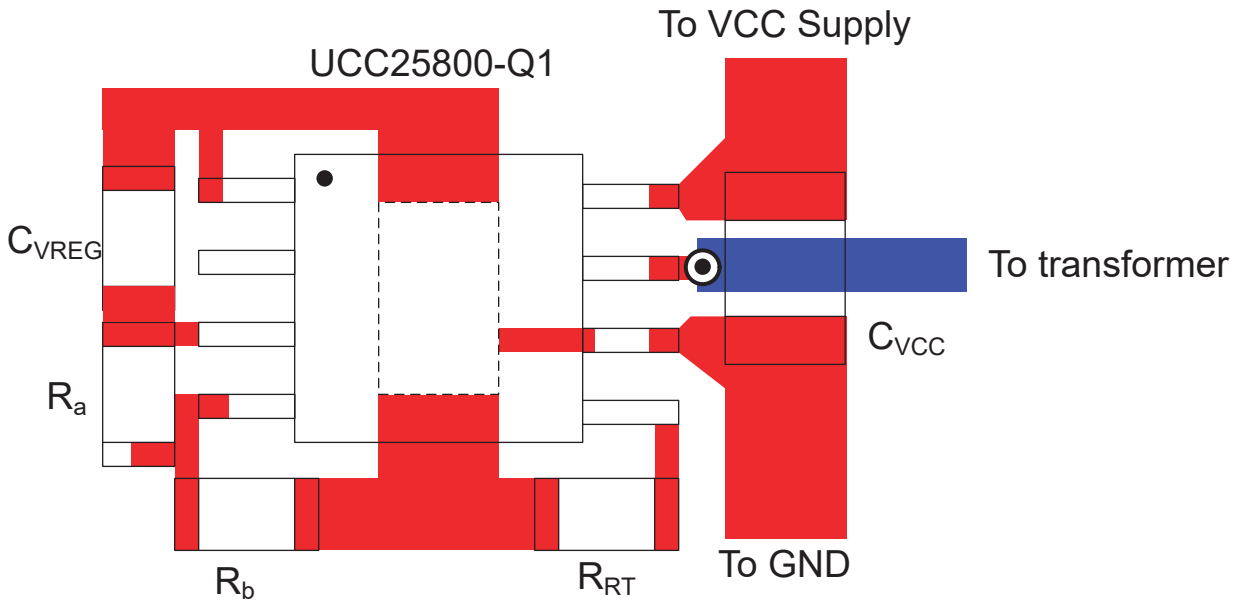

Figure 11-1. Layout example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, UCC25800EVM-1, 2-W LLC converter with 6-V to 26-V DC input and 18-V and 5-V outputs
- Texas Instruments, Reference design PMP22835, Isolated IGBT and SiC driver bias supply reference design for traction-inverter applications
- Texas Instruments, Reference design PMP23061, Pre-regulated isolated driver bias supply reference design for traction-inverter applications
- Texas Instruments, UCC25800-Q1 design Calculator
- Texas Instruments, UCC25800-Q1 SIMPLIS Transient Model
- Texas Instruments, Application note, Bias Supply Design for Isolated Gate Driver Using UCC25800-Q1
- Texas Instruments, Functional-safety information, UCC25800-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA
- Texas, Instruments, White paper, Power Through the Isolation Barrier: The Landscape of Isolated DC/DC Bias Power

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-side navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC25800AQDGNQ1	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	580Q
UCC25800AQDGNQ1.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	580Q
UCC25800AQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	580Q
UCC25800AQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	580Q
UCC25800BQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	80BQ
UCC25800BQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	80BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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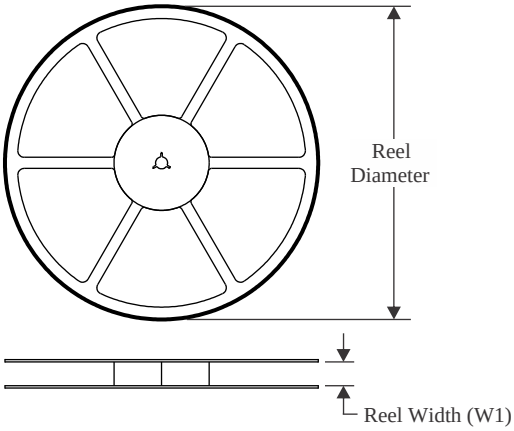
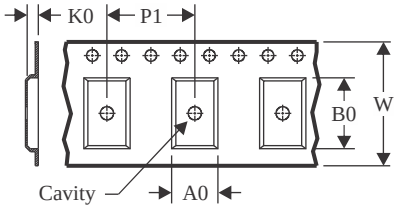
TAPE AND REEL INFORMATION

REEL DIMENSIONS

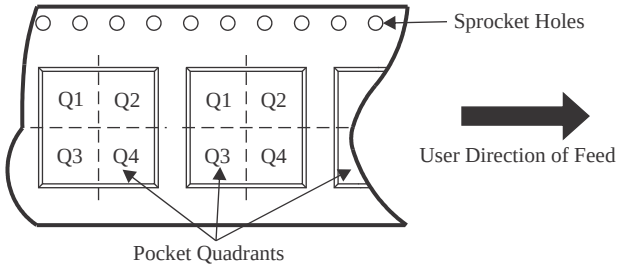


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

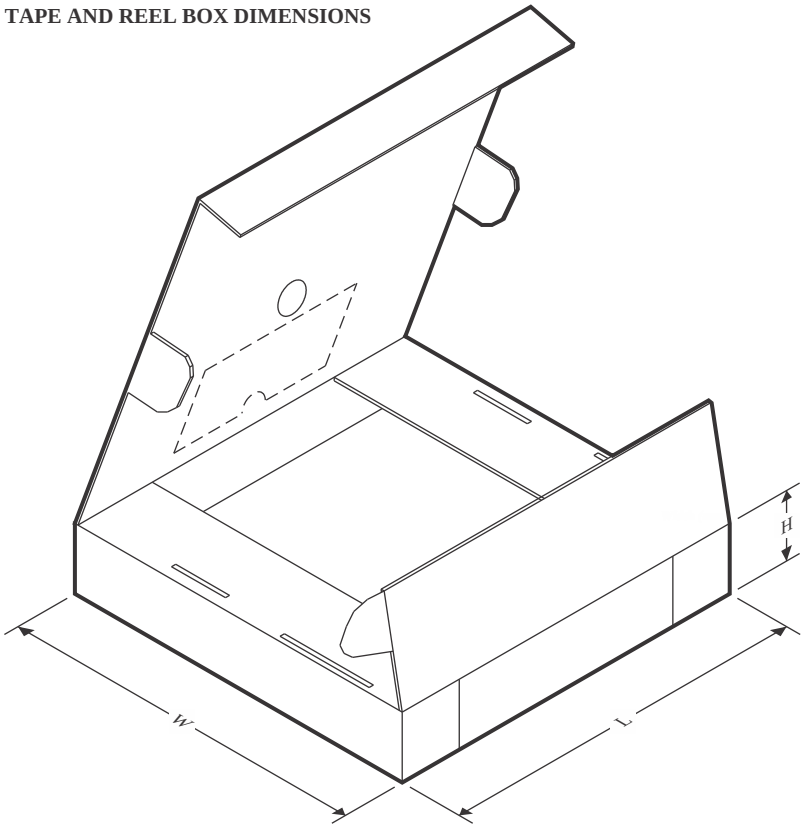
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25800AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC25800BQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

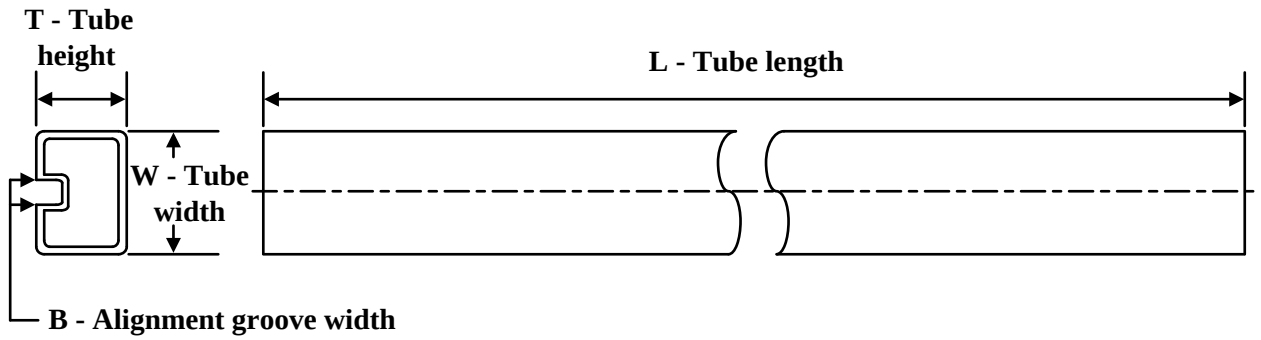
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25800AQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
UCC25800BQDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC25800AQDGNQ1	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC25800AQDGNQ1.A	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

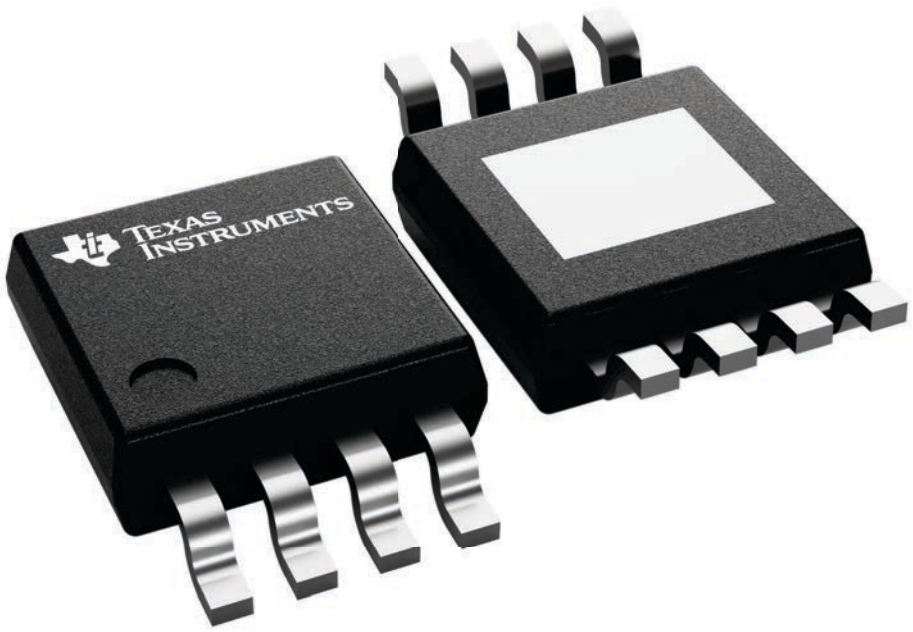
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

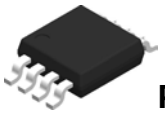
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

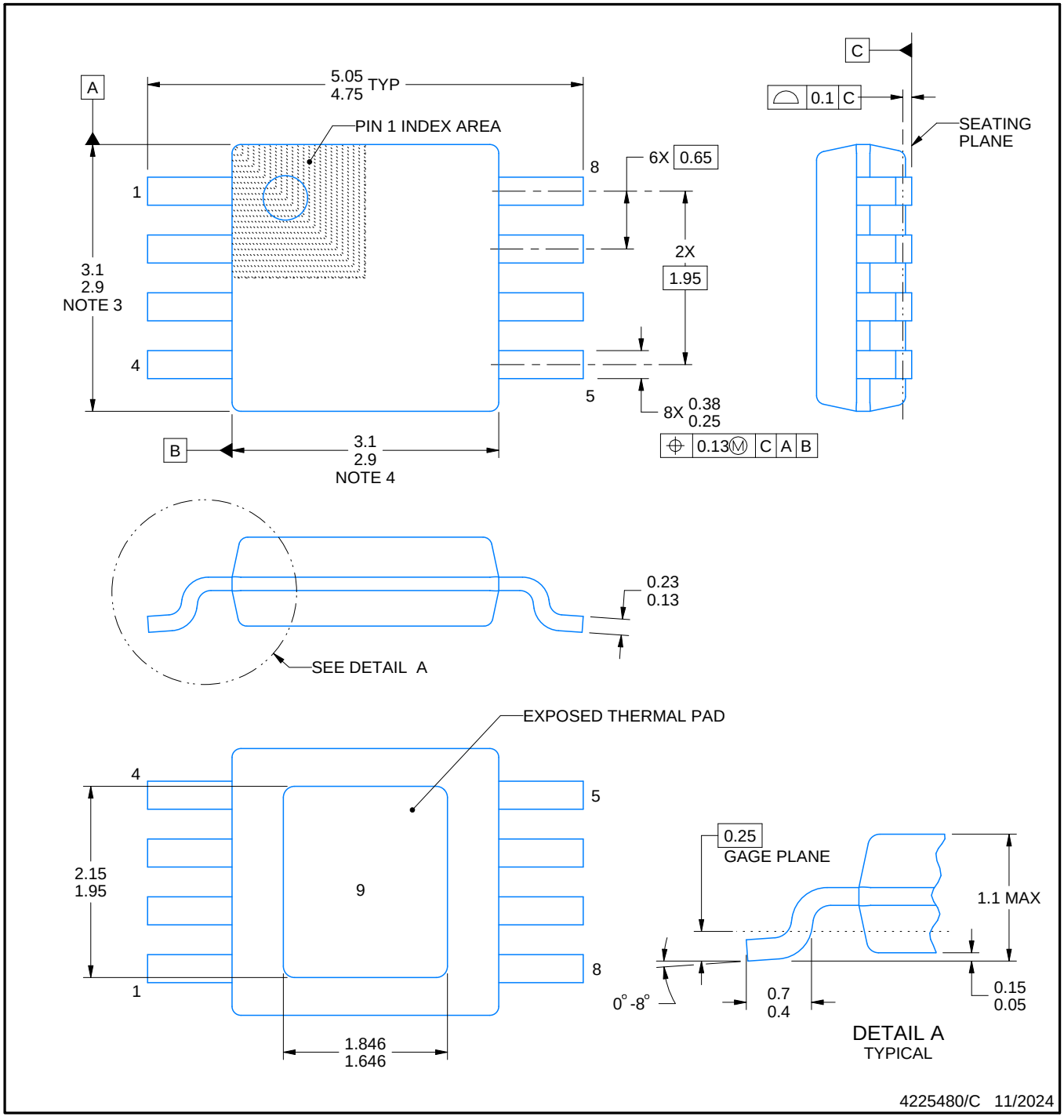
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

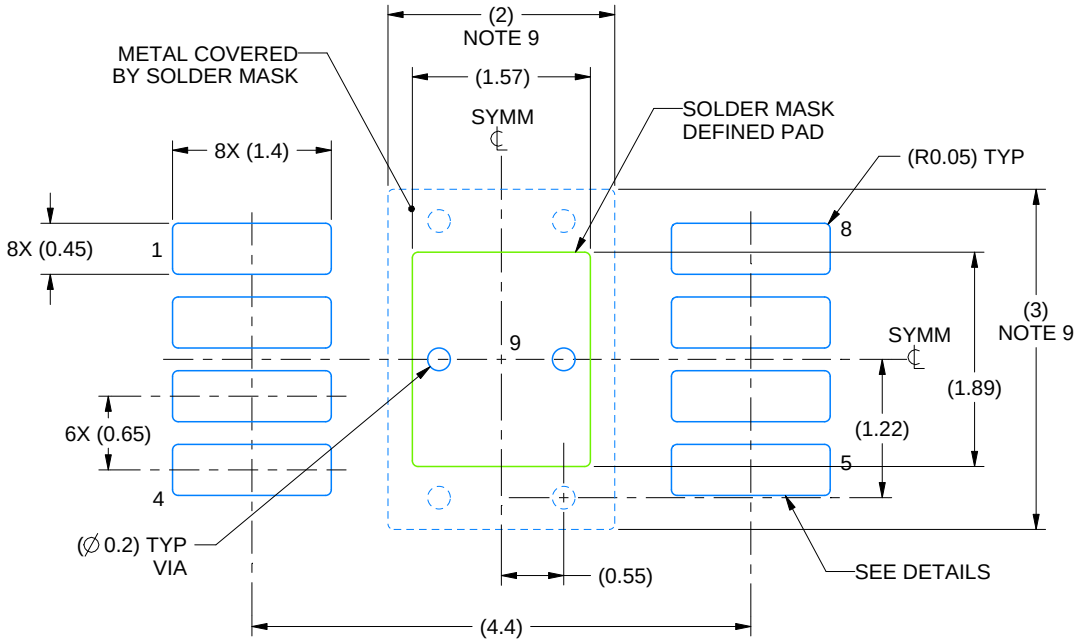
SMALL OUTLINE PACKAGE



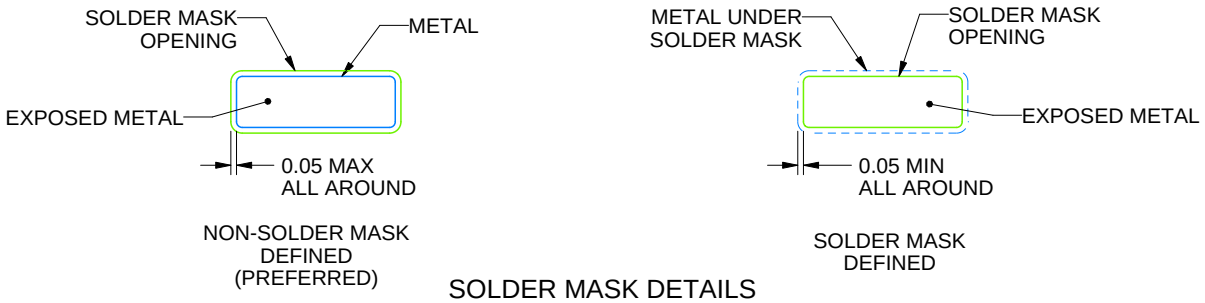
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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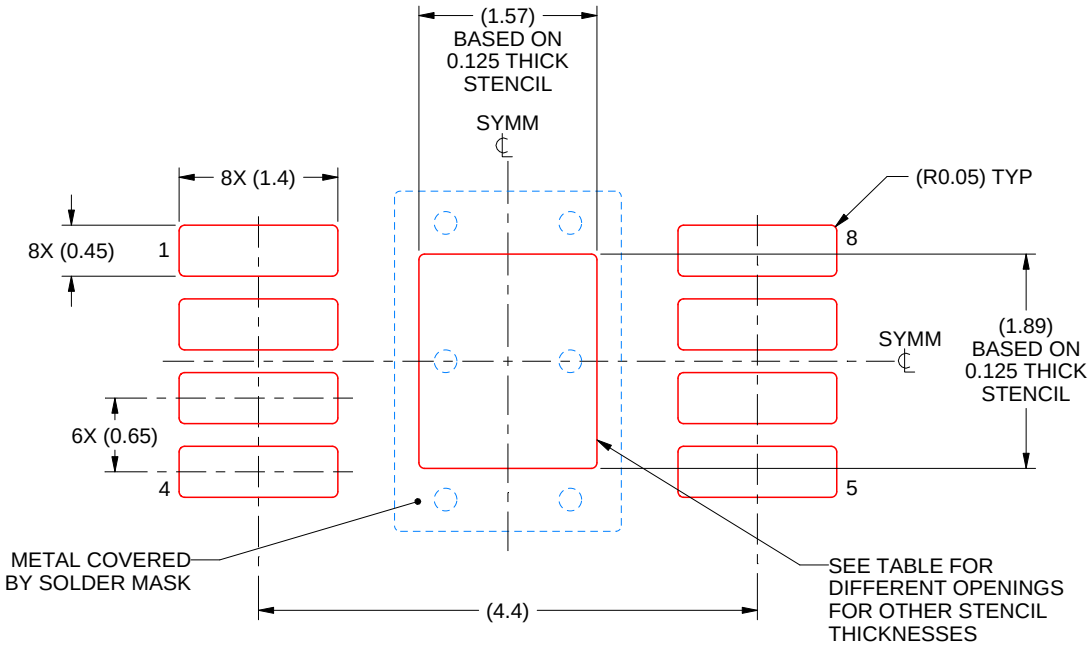
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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