TPS659119-Q1 Automotive Integrated Power-Management Unit

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 3: –40°C to 85°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Embedded Power Controller (EPC) With EEPROM Programmability
- Two Efficient Step-Down DC-DC Converters With Dynamic Voltage Scaling for Processor Cores (VDD1, VDD2)
- One Efficient Step-Down DC-DC Converter for I/O Power (VIO)
- An Interface to Control an External DCDC Converter (EXTCTRL)
- Eight LDO Voltage Regulators and One RTC LDO (Supply for Internal RTC)
- One High-Speed I^2C Interface for General-Purpose Control Commands (CTL-I^2C)
- Two Independent Enable Signals for Controlling Power Resources (EN1, EN2) Which can be Used as a High-Speed I^2C Interface Dedicated for VDD1 and VDD2 Voltage Scaling.
- Thermal Shutdown Protection and Hot-Die Detection
- A Real-Time Clock (RTC) Resource with:
  - Fast Start-Up 16.384-MHz Crystal Oscillator
  - Configurable Clock Source from Crystal Oscillator, External 32-kHz Clock or Internal 32-kHz RC Oscillator
  - Date, Time, and Calendar
  - Alarm Capability
- Nine Configurable GPIOs with Multiplexed Feature Support:
  - Four can be Used as Enable for External Resources, Included into Power-Up Sequence and Controlled by State-Machine
  - As GPI, GPIOs Support Logic-level Detection and Can Generate Maskable Interrupt for Wake-Up
  - Two of the GPIOs Have 10-mA Current Sink Capability for Driving LEDs
  - DCDCs Switching Synchronization Through an External 3-MHz Clock
- Two Reset Inputs for Cold Reset (HDRST) and a Power-Initialization Reset (PWRDN) for Thermal Reset Input
- 32-kHz Clock Output (CLK32KOUT) and System Reset (NRESPWRON) Included in Power Sequence
- Watchdog
- Two ON and OFF LED-Pulse Generators and One PWM Generator

2 Applications

- Automotive
- Infotainment
- ADAs
- Instrument Cluster

3 Description

The TPS659119-Q1 device is an integrated power-management IC dedicated to systems using an applications processor requiring multiple power rails. The device provides three step-down converters, one control for an external converter, eight LDOs, and is designed to be flexible for supporting different processors and applications.

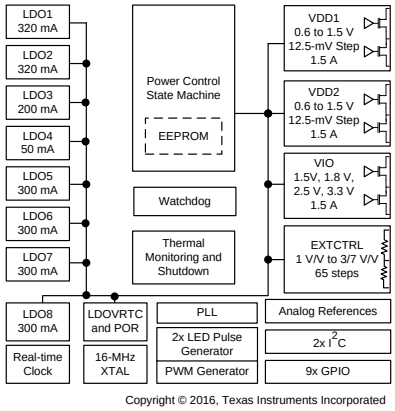
Two of the step-down converters provide power for dual-processor cores and support for dynamic voltage scaling by a dedicated I^2C interface for optimum power savings. The third converter provides power for inputs and outputs (I/Os) and memory in the system. The control for an external converter can sequence and scale the voltage of an external converter for a high-current rail in the system.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS659119-Q1	HTQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2014) to Revision F — **Page**

- Deleted *Top Specification* from title of document ... 1
- Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature to the *Absolute Maximum Ratings* table ... 7
- Added the *Receiving Notification of Documentation Updates* and *Community Resources* sections ... 124

Changes from Revision D (July 2014) to Revision E — **Page**

- Updated the PSKIP rows for the TPS659119KBIPFPRQ1 in the *EEPROM Configuration* table ... 49
- Added column for TPS659119LBIPFP to and removed the TOP-SIDE MARKING row from the *EEPROM CONFIGURATION* table in the *BOOT CONFIGURATION AND SWITCH-ON AND SWITCH-OFF SEQUENCES* section ... 49

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Changes from Revision C (August 2013) to Revision D **Page**

- Changed CDM classification level from C4A to C4B and updated CDM ESD rating to include corner pin values as well as other pin values ... 1
- Updated data sheet format to include new document flow and the following new items: *Device Information* table, *Overview* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section (now contains the glossary), *Mechanical, Packaging, and Orderable Information* section. Also deleted *Appendix A: Functional Registers* and moved the register map and descriptions to the *Detailed Description* section ... 1
- Deleted the *PARAMETER* and *TEST CONDITION* column headings from the *Absolute Maximum Ratings*, *Recommended Operating Conditions*, and *External Component Recommendation* tables ... 7
- Moved storage temperature range and ESD ratings from the *Absolute Maximum Ratings* table into the new *Handling Ratings* table ... 7
- Changed the TYP column to NOM in the *Recommended Operating Conditions* table ... 7
- Replaced *Characteristics* with *Requirements* in all timing table titles ... 7
- Split the DC output parameter for each LDO into output voltage, step size, and output accuracy and removed multiple TYP values ... 7
- Added column for TPS659119KBIPFP (top-side marking) to the *EEPROM CONFIGURATION* table in the *BOOT CONFIGURATION AND SWITCH-ON AND SWITCH-OFF SEQUENCES* section ... 49
- Added pullup resistors to VDDIO on the I^2C pins in the *Application Schematic* image ... 118
- Added T659119KB device marking information to the *PACKAGE OPTION ADDENDUM* and *PACKAGE MATERIALS INFORMATION* pages at the end of the document ... 123

Changes from Revision B (April 2013) to Revision C **Page**

- Added Storage Temperature range to *ABSOLUTE MAXIMUM RATINGS* table ... 7

Changes from Revision A (April 2013) to Revision B **Page**

- Changed 0x20 to 0x22 for TPS659119HAIPFPRQ1 column in EEPROM Configuration table. ... 49

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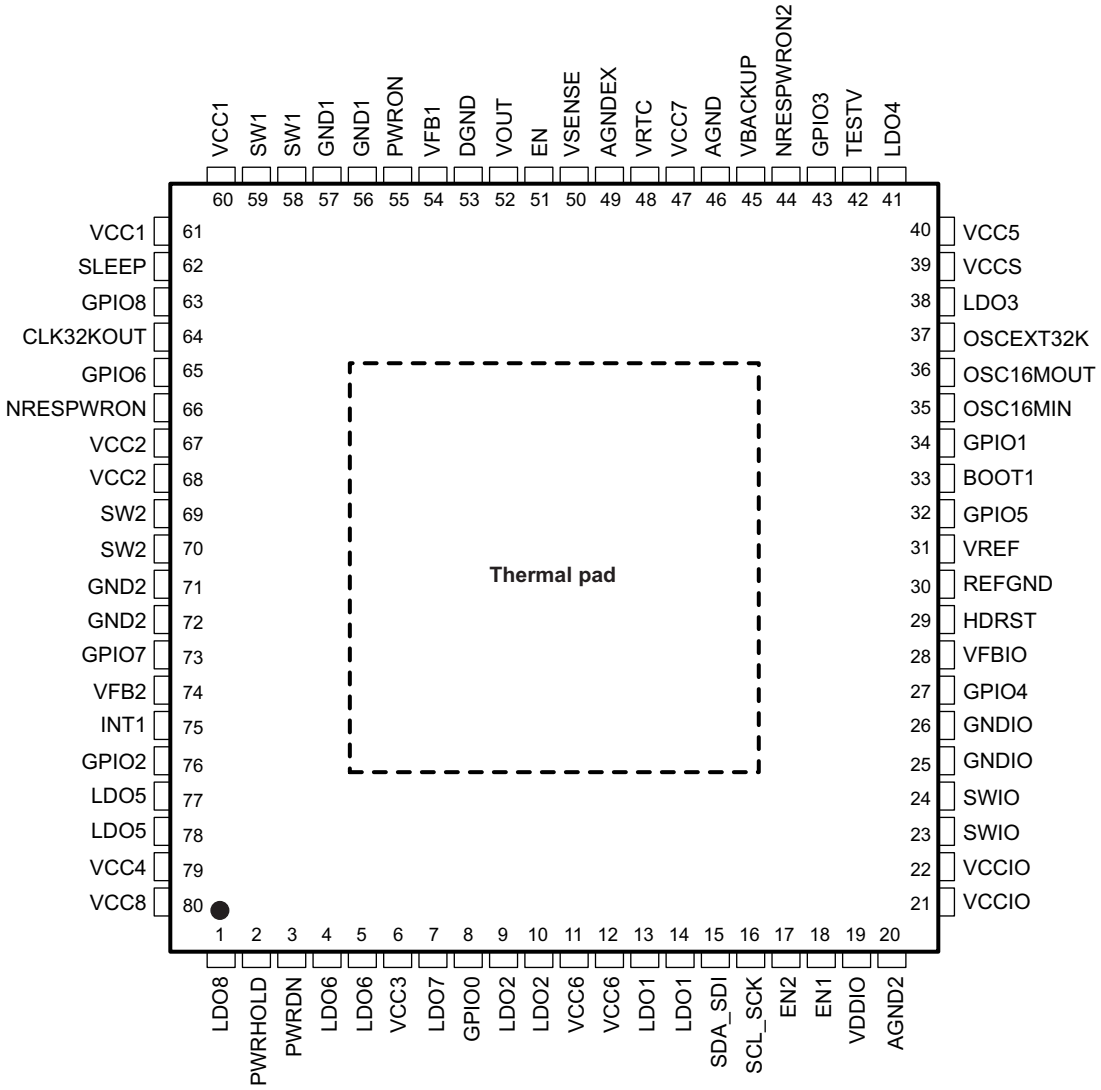
5 Description (continued)

The device also includes eight general-purpose LDOs providing a wide range of voltage and current capabilities. Five of the LDOs support 1 to 3.3 V with 100-mV steps, and three LDOs support 1 to 3.3 V with 50-mV steps. All LDOs are fully controllable by the I^2C interface.

In addition to the power regulators, the device contains nine configurable GPIOs with multiplexing features to support a wide variety of functions. The device also includes an embedded power controller to manage the power sequencing requirements of the system. The power sequencing is programmable by EEPROM.

6 Pin Configuration and Functions

PFP Package, 0.5-mm Pitch
80-Pin HTQFP With Thermal Pad
Top View



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Pin Functions

PIN		TYPE	I/O	DESCRIPTION	SUPPLIES	PU / PD
NAME	NO.					
LDO8	1	Power	O	LDO regulator output	VCC3, REFGND	PD 5 µA
PWRHOLD	2	Digital	I	Switch-on, switch off control signal and GPI	VRTC, DGND	Programmable PD (default active)
PWRDN	3	Analog	I	Reset input, for example, thermal reset	VRTC, DGND	PD
LDO6	4	Power	O	LDO regulator output	VCC3, REFGND	PD 5 µA
	5					
VCC3	6	Power	I	LDO6 and LDO7 power Input	VCC3, AGND2	No
LDO7	7	Power	O	LDO regulator output	VCC3, REFGND	PD 5 µA
GPIO0	8	Digital	I/O	GPIO, push pull and OD as output	VCC7, DGND	OD: external PU
LDO2	9	Power	O	LDO regulator output	VCC6, REFGND	No
	10					
VCC6	11	Power	I	LDO1, LDO2 power Input	VCC6, AGND2	No
	12					
LDO1	13	Power	O	LDO regulator output	VCC6, REFGND	No
	14					
SDA_SDI	15	Digital	I/O	I^2C bidirectional-data signal and serial-peripheral-interface data input (multiplexed)	VDDIO, DGND	External PU
SCL_SCK	16	Digital	I/O	I^2C bidirectional-clock signal and serial-peripheral-interface clock input (multiplexed)	VDDIO, DGND	External PU
EN2	17	Digital	I/O	Enable for supplies and voltage scaling dedicated to I^2C data	VDDIO, DGND	External PU
EN1	18	Digital	I/O	Enable for supplies and voltage scaling dedicated to I^2C clock	VDDIO, DGND	External PU
VDDIO	19	Power	I	Digital I/O supply	VDDIO, DGND	No
AGND2	20	Power	I/O	Analog ground	AGND2	No
VCCIO	21	Power	I	VIO DC-DC power Input	VCCIO, GNDIO	No
	22					
SWIO	23	Power	O	VIO DC-DC switched output	VCCIO, GNDIO	No
	24					
GNDIO	25	Power	I/O	VIO DC-DC power ground	VCCIO, GNDIO	No
	26					
GPIO4	27	Digital	I/O	GPIO	VRTC, DGND	OD: External PU
			OD			
VFBIO	28	Analog	I	VIO feedback voltage	VCC7, DGND	PD 5 µA
HDRST	29	Digital	I	Cold reset	VRTC, DGND	PD
REFGND	30	Analog	I/O	Reference ground	REFGND	No
VREF	31	Analog	O	Bandgap voltage	VCC7, REFGND	No
GPIO5	32	Digital	I/O	GPIO	VRTC, DGND	OD: external PU
			OD			
BOOT1	33	Digital	I	Power-up sequence selection	VRTC, DGND	No
GPIO1	34	Digital	I/O	GPIO and LED1 output	VRTC, DGND	OD: External PU
			OD			
OSC16MIN	35	Analog	I	16.384-MHz crystal oscillator input	VCC7, DGND	External PD if not in use
OSC16MOUT	36	Analog	O	16.384-MHz crystal oscillator output	VCC7, DGND	No
OSCEXT32K	37	Digital	I	External 32-kHz clock input	VRTC, DGND	External PD if not in use
LDO3	38	Power	O	LDO regulator output	VCC5, REFGND	PD 5 µA
VCCS	39	Analog	I/O	VCC7 voltage sense input	VCC7, DGND	No
VCC5	40	Power	I	LDO3 and LDO4 power Input	VCC5, AGND	No
LDO4	41	Power	O	LDO regulator output	VCC5, REFGND	PD 5 µA
TESTV	42	Analog	O	Analog test output (DFT)	VCC7, AGND	No

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Pin Functions (continued)

PIN		TYPE	I/O	DESCRIPTION	SUPPLIES	PU / PD
NAME	NO.					
GPIO3	43	Digital	I/O OD	GPIO and LED2 output	VRTC, DGND	OD: External PU
NRESPWRON2	44	Digital	O OD	Second NRESPWRON output	VRTC, DGND	PD active during device OFF state.External pullup when ACTIVE
VBACKUP	45	Power	I	Tie this pin to AGND	VBACKUP, AGND	No
AGND	46	Power	I/O	Analog ground	AGND	No
VCC7	47	Power	I	VRTC power input and analog references supply	VCC7, REFGND	No
VRTC	48	Power	O	LDO regulator output	VCC7, REFGND	PD 5 µA
AGNDEX	49	Power	I/O	EXTCTRL resistive divider ground	AGNDEX	No
VSENSE	50	Analog	I	EXTCTRL resistive divider output	VOUT, AGNDEX	No
EN	51	Digital	O	EXTCTRL enable signal for external converter	VCC7, DGND	No
VOUT	52	Analog	I	EXTCTRL resistive divider input	VOUT, AGNDEX	No
DGND	53	Power	I/O	Digital ground	DGND	No
VFB1	54	Analog	I	VDD1 feedback voltage	VCC7, DGND	PD 5 µA
PWRON	55	Digital	I	External switch-on control (ON button)	VCC7, DGND	Programmable PU (default active)
GND1	56 57	Power	I/O	VDD1 DC-DC power ground	VCC1, GND1	No
SW1	58 59	Power	O	VDD1 DC-DC switched output	VCC1, GND1	No
VCC1	60 61	Power	I	VDD1 DC-DC power Input	VCC1, GND1	No
SLEEP	62	Digital	I	ACTIVE-SLEEP state transition control signal	VDDIO, DGND	Programmable PD (default active)
GPIO8	63	Digital	I/O, OD	GPIO	VRTC, DGND	OD: External PU
CLK32KOUT	64	Digital	O	32-kHz clock output	VDDIO, DGND	PD, disabled in ACTIVE or SLEEP state
GPIO6	65	Digital	I/O, OD	GPIO	VRTC, DGND	OD: External PU
NRESPWRON	66	Digital	O	Power off reset	VDDIO, DGND	PD active during device OFF state
VCC2	67 68	Power	I	VDD2 DC-DC power input	VCC2, GND2	No
SW2	69 70	Power	O	VDD2 DC-DC switched output	VCC2, GND2	No
GND2	71 72	Power	I/O	VDD2 DC-DC power ground	VCC2, GND2	No
GPIO7	73	Digital	I/O, OD	GPIO	VRTC, DGND	OD: External PU
VFB2	74	Analog	I	VDD2 DC-DC feedback voltage	VCC7, DGND	PD 5 µA
INT1	75	Digital	O	Interrupt flag	VDDIO, DGND	No
GPIO2	76	Digital	I/O, OD	GPIO and DC-DC clock synchronization	VRTC, DGND	OD: External PU
LDO5	77 78	Power	O	LDO regulator output	VCC4, REFGND	PD 5 µA
VCC4	79	Power	I	LDO5 power input	VCC4, AGND2	No
VCC8	80	Power	I	LDO8 power input	VCC8, AGND2	No

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	VCC1, VCC2, VCCIO, VCC3, VCC4, VCC5, VCC7, VCC8		–0.3	7	V
	VCC6, VDDIO		–0.3	3.6	V
	SW1, SW2, SWIO		–0.3	7	V
		10 ns Transient	–2	7	V
	VFB1,VFB2,VFBIO		–0.3	3.6	V
	VOUT, VSENSE		–0.3	7	V
	BOOT1		–0.3	VRTCMAX + 0.3	V
	SDA_SDI, SCL_SCK, EN2, EN1, SLEEP, INT1, CLK32KOUT, NRESPWRON		–0.3	VDDIOMAX + 0.3	V
	PWRON		–0.3	7	V
	PWRHOLD, GPIO0		–0.3	7	V
	OSCEXT32K, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8(2)		–0.3	7	V
	HDRST		–0.3	VRTCMAX + 0.3	V
	OSC16MIN, OSC16MOUT		–0.3	5.7	V
	NRESPWRON2(2)		–0.3	7	V
	PWRDN(3)		–0.3	7	V
	VCCS		–0.3	7	V
Peak output current	All other pins than power resources		–5	5	mA
Functional junction temperature			–45	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VRTC supplies the I/O but the I/O can also be driven from VCC7 or to VCC7 voltage level.
(3) VRTC supplies the input supplied but can also be driven from VCC7 voltage level.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 20, 21, 40, 41, 60, 61, and 80)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)
Note: VCC7 should be connected to highest supply that is connected to device VCCx pin.
Exception: The VCC4, VCC5, VIN, and AVIN inputs can be higher than VCC7. VCCS can be higher than VCC7 if VMBBUF_BYPASS = 0 (buffer is enabled).

		MIN	NOM	MAX	UNIT
Input voltage	VCC5, VCCS	2.7		5.5	V
	VCC3, VCC4, VCC8	1.7		5.5	V
	VCC1, VCC2, VCCIO, VCC7	4	5	5.5	V
	VCC6, VDDIO	1.4	3.3	3.6	V
	VSENSE	–0.1		6.5	V
	PWRON	0	3.8	5.5	V
	SDA_SDI, SCL_SCK, EN2, EN1, SLEEP, INT1, CLK32KOUT	1.65	VDDIO	3.45	V
	PWRHOLD, HDRTS	1.65	VRTC	5.5	V
	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, PWRDN	1.65	VRTC	5.5	V
	VCCS	0		5.5	V
	OSCEXT32K	0		5.5	V

7.4 Thermal Characteristics

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS659119-Q1 PFP (HTQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	9.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 External Component Recommendation

For crystal oscillator components, see the *32-kHz RTC Clock* section. **Note**: The VCC7 supply must have enough capacitance to specify that when the supply is switched off, voltage does not fall at a rate faster than 10 mV/ms. This ensures that RTC domain data is maintained.

			MIN	NOM	MAX	UNIT
POWER REFERENCES						
$C_{O(VREF)}$	VREF filtering capacitor	Connected from VREF to REFGND		100		nF
VDD1 SMPS						
$C_{I(VCC1)}$	Input capacitor	X5R or X7R dielectric		10		µF
$C_{O(VDD1)}$	Output filter capacitor	X5R or X7R dielectric	4	10	12	µF
	C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
$L_{O(VDD1)}$	Inductor			2.2		µH
DCR_L	L_O inductor dc resistor				125	mΩ
VDD2 SMPS						
$C_{I(VCC2)}$	Input capacitor	X5R or X7R dielectric		10		µF
$C_{O(VDD2)}$	Output filter capacitor	X5R or X7R dielectric	4	10	12	µF
	C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
$L_{O(VDD2)}$	Inductor			2.2		µH

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External Component Recommendation (continued)

For crystal oscillator components, see the *32-kHz RTC Clock* section. **Note**: The VCC7 supply must have enough capacitance to specify that when the supply is switched off, voltage does not fall at a rate faster than 10 mV/ms. This ensures that RTC domain data is maintained.

			MIN	NOM	MAX	UNIT
DCR_L	L_O inductor dc resistor				125	mΩ
VIO SMPS						
$C_{I(VCCIO)}$	Input capacitor	X5R or X7R dielectric		10		µF
$C_{O(VIO)}$	Output filter capacitor	X5R or X7R dielectric	4	10	12	µF
	C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
$L_{O(VIO)}$	Inductor			2.2		µH
DCR_L	L_O inductor dc resistor				125	mΩ
LDO1						
$C_{I(VCC6)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(LDO1)}$	Output filtering capacitor		0.8	2.2	2.64	µF
	C_O filtering capacitor ESR		0		500	mΩ
LDO2						
$C_{O(LDO2)}$	Output filtering capacitor		0.8	2.2	2.64	µF
	C_O filtering capacitor ESR		0		500	mΩ
LDO3						
$C_{I(VCC5)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(LDO3)}$	Output filtering capacitor		0.8	2.2	2.64	µF
	C_O filtering capacitor ESR		0		500	mΩ
LDO4						
$C_{O(LDO4)}$	Output filtering capacitor		0.8	2.2	2.64	µF
	C_O filtering capacitor ESR		0		500	mΩ
LDO5						
$C_{I(VCC4)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(LDO5)}$	Output filtering capacitor	V_{OUT}(LDOx) > 1.2 V	0.8	2.2	2.64	µF
		V_{OUT}(LDOx) ≤ 1.2 V	0.8	2	2.2	
	C_O filtering capacitor ESR		0		500	mΩ
LDO6						
$C_{I(VCC3)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(LDO6)}$	Output filtering capacitor	V_{OUT}(LDOx) > 1.2 V	0.8	2.2	2.64	µF
		V_{OUT}(LDOx) ≤ 1.2 V	0.8	2	2.2	
	C_O filtering capacitor ESR		0		500	mΩ
LDO7						
$C_{O(LDO7)}$	Output filtering capacitor	V_{OUT}(LDOx) > 1.2 V	0.8	2.2	2.64	µF
		V_{OUT}(LDOx) ≤ 1.2 V	0.8	2	2.2	
	C_O filtering capacitor ESR		0		500	mΩ
LDO8						
$C_{I(VCC8)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(LDO8)}$	Output filtering capacitor	V_{OUT}(LDOx) > 1.2 V	0.8	2.2	2.64	µF
		V_{OUT}(LDOx) ≤ 1.2 V	0.8	2	2.2	
	C_O filtering capacitor ESR		0		500	mΩ
VRTC LDO						
$C_{I(VCC7)}$	Input capacitor	X5R or X7R dielectric		4.7		µF
$C_{O(VRTC)}$	Output filtering capacitor		0.8	2.2	2.64	µF
	C_O filtering capacitor ESR		0		500	mΩ

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7.6 I/O Pullup and Pulldown Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-8 external pullup resistor	Connected to VDDIO	–20%	120	20%	kΩ
GPIO0-8 programmable pulldown (default active except GPIO0)	at 1.8 V, VRTC = 1.8 V, OFF state	2	4.5	15	µA
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 external pullup resistor	Connected to VDDIO		1.2		kΩ
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 programmable pullup (DFT, default inactive)	Grounded, VDDIO = 1.8 V	–45%	8	45%	kΩ
SLEEP, PWRHOLD, programmable pulldown (default active)	at 1.8 V, VRTC = 1.8 V; T_A = 25°C for PWRHOLD	2	4.5	10	µA
NRESPWRON, NRESPWRON2 pulldown	at 1.8 V, VCC7 = 5.5 V, OFF state	2	4.5	10	µA
32KCLKOUT pulldown (disabled in ACTIVE-SLEEP state)	at 1.8 V, VRTC = 1.8 V, OFF state	2	4.5	10	µA
PWRON programmable pullup (default active)	Grounded, VCC7 = 5.5 V	–43	–31	–15	µA
HDRST programmable pulldown (default active)	at 1.8 V, VRTC = 1.8 V	2	4.5	10	µA

(1) The internal pullups on the CTL-I^2C and SR-I^2C pins are used for test purposes or when the SR-I^2C interface is not used. Discrete pullups to the VIO supply must be mounted on the board in order to use the I^2C interfaces. The internal I^2C pullups must not be used for functional applications

7.7 Digital I/O Voltage Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
RELATED I/O: PWRON						
V_{IL}	Low-level input voltage				0.3 x VBAT	V
V_{IH}	High-level input voltage		0.7 x VBAT			V
RELATED I/O: PWRHOLD, GPIO0-8, PWRDN						
V_{IL}	Low-level input voltage				0.45	V
V_{IH}	High-level input voltage		1.3		VBAT	V
RELATED I/O: BOOT1						
	Low level input – Impedance between BOOT1 and GND				10	kΩ
	High level input – Impedance between BOOT1 and VRTC				10	kΩ
	Hi-Z level input – Impedance between BOOT1 and GND		500			kΩ
RELATED I/O: SLEEP						
V_{IL}	Low-level input voltage				0.35 x VDDIO	V
V_{IH}	High-level input voltage		0.65 x VDDIO			V
RELATED I/O: HDRST						
V_{IL}	Low-level input voltage				0.35 x VRTC	V
V_{IH}	High-level input voltage		0.65 x VRTC			V
RELATED I/O: NRESPWRON, INT1, 32KCLKOUT						
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.2	V
		I_{OL} = 2 mA			0.45	V
V_{OH}	High-level output voltage	I_{OH} = 100 µA	VDDIO – 0.2			V
		I_{OH} = 2 mA	VDDIO – 0.45			V
Related I/O: EN						
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.2	V
		I_{OL} = 2 mA			0.9	V

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Digital I/O Voltage Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 100 µA	VCC7– 0.2			V
		I_{OH} = 2 mA	VCC7 – 0.45			V
RELATED I/O: GPIO0 (PUSH-PULL MODE)						
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.2	V
		I_{OL} = 2 mA			0.45	V
V_{OH}	High-level output voltage	I_{OH} = 100 µA	VCC7 – 0.2			V
		I_{OH} = 2 mA	VCC7 – 0.45			V
RELATED OPEN-DRAIN I/O: GPIO0, GPIO2, GPIO4-8, NRESPWRON2						
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.2	V
		I_{OL} = 2 mA			0.45	V
RELATED OPEN-DRAIN I/O: GPIO1, GPIO3						
V_{OL}	Low-level output voltage	I_{OL} = 100 µA			0.2	V
		I_{OL} = 2 mA			0.4	V
I						
V_{IL}	Low-level input voltage		–0.5		0.3 x VDDIO	V
V_{IH}	High-level input voltage		0.7 x VDDIO			V
	Hysteresis		0.1 x VDDIO			V
V_{OL}	Low-level output voltage at 3 mA (sink current), VDDIO = 1.8 V				0.2 × VDDIO	V
V_{OL}	Low-level output voltage at 3 mA (sink current), VDDIO = 3.3 V				0.4 x VDDIO	V

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7.8 I²C Interface and Control Signals

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS(1) (2)	MIN	TYP	MAX	UNIT
GENERAL REQUIREMENTS							
		INT1 rise and fall times	C_L = 5 to 35 pF	5		10	ns
		NRESPWRON rise and fall times	C_L = 5 to 35 pF	5		10	ns
SLAVE HIGH-SPEED MODE							
		SCL/EN1 and SDA/EN2 rise and fall time	C_L = 10 to 100 pF	10		80	ns
		Data rate				3.4	Mbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		10			ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low		0		70	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low		160			ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		160			ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		160			ns
SLAVE FAST MODE							
		SCL/EN1 and SDA/EN2 rise and fall time	C_L = 10 to 400 pF	20 + 0.1 × C_L		250	ns
		Data rate				400	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		100			ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low		0		0.9	µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low		0.6			µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		0.6			µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		0.6			µs
SLAVE STANDARD MODE							
		SCL/EN1 and SDA/EN2 rise and fall time	C_L = 10 to 400 pF			250	ns
		Data rate				100	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high		250			ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low		0			µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low		4.7			µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low		4			µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high		4			µs

(1) The input timing requirements are given by considering a rising or falling time of: 80 ns in high–speed mode (3.4 Mbps) 300 ns in fast–speed mode (400 kbps) 1000 ns in Standard mode (100 kbps)
(2) SDA is SDA_SDI or EN2 signal, SCL is SCL_SCK or EN1 signal

7.9 Switching Characteristics—I²C Interface and Control Signals

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SLAVE HIGH-SPEED MODE							
I1	$t_{w(SCLL)}$	Pulse duration, SCL low		160			ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high		60			ns
SLAVE FAST MODE							
I1	$t_{w(SCLL)}$	Pulse duration, SCL low		1.3			µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high		0.6			µs
SLAVE STANDARD MODE							
I1	$t_{w(SCLL)}$	Pulse duration, SCL low		4.7			µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high		4			µs

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7.10 Power Consumption

over operating free-air temperature range (unless otherwise noted)

All current consumption measurements are relative to the FULL chip, all VCC inputs set to VBAT voltage, COMP2 is off.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device OFF state	VBAT = 5 V, XTAL oscillator running		2.5		mA
	VBAT = 5 V, Bypass clock used		22		µA
Device SLEEP state	VBAT = 5 V, 3 DCDCs on in PFM mode, 5 LDOs on, no load, XTAL oscillator running		2.8		mA
Device ACTIVE state	VBAT = 5 V, 3 DCDCs on in PWM mode, 5 LDOs on, no load, XTAL oscillator running		26.6		mA

7.11 Power References and Thresholds

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output reference voltage (VREF pin)	Device in active or low-power mode	–1%	0.85	1%	V
Main battery not present falling threshold VBNPR	Measured on pin VCC7, falling (Triggering monitored on pin VRTC)	1.8	2.1	2.3	V
PORXTAL	The POR threshold for rising VCC7 voltages	3.58	3.77	3.96	V
	The POR threshold for falling VCC7 voltages	3.50	3.68	3.87	V
	Difference between rising and falling thresholds	62.55	89.35	200	mV

7.12 Thermal Monitoring and Shutdown

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hot-die temperature rising threshold	THERM_HDSEL[1:0] = 00		117		°C
	THERM_HDSEL[1:0] = 01		121		
	THERM_HDSEL[1:0] = 10	113	125	136	
	THERM_HDSEL[1:0] = 11		130		
Hot-die temperature hysteresis			10		°C
Thermal shutdown temperature rising threshold		150	165	180	°C
Thermal shutdown temperature recovery threshold	THERM_HDSEL[1:0] = 00		107		°C
	THERM_HDSEL[1:0] = 01		111		
	THERM_HDSEL[1:0] = 10		115		
	THERM_HDSEL[1:0] = 11		120		
Ground current	Device in ACTIVE state, Temp = 27°C, VCC7 = 3.8 V		6		µA

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7.13 32-kHz RTC Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CLK32KOUT REQUIREMENTS					
CLK32KOUT rise and fall time	C_L = 35 pF			10	ns
EXTERNAL CLOCK (OSC16MIN GROUNDED, OSC16MOUT FLOATING, AND OSCEXT32K INPUT)					
Input bypass clock frequency	OSCKIN input		32		kHz
Input bypass clock duty cycle	OSCKIN input	40%		60%	
Input bypass clock rise and fall time	10% – 90%, OSCEXT32K input		10	20	ns
CLK32KOUT duty cycle	Logic output signal	40%		60%	
Bypass clock setup time	32KCLKOUT output			1	ms
Ground current	Bypass mode			1.5	µA
CRYSTAL OSCILLATOR (CRYSTAL BETWEEN OSC16MIN AND OSC16MOUT, OSCEXT32K GROUNDED)					
Crystal frequency	at specified load cap value		16.384		MHz
Crystal tolerance	at 27°C	–20	0	20	ppm
Oscillator frequency drift	T_J from –40°C to 125°C, VCC7 from 4 V to 5.5 V; excluding crystal drift	–50		50	ppm
Max crystal series resistor	at fundamental frequency			90	Ω
Oscillator startup time	Power on until first time slot			13.2	ms
Drive level power	Steady state operation		15	120	µW
Ground current			2.5		mA
Overall frequency tolerance	CLK32KOUT output	–1%		1%	
Output frequency	CLK32KOUT output		32.768		kHz
Crystal motional inductance	According to crystal data sheet	23	33	43	µH
Crystal shunt capacitance	According to crystal data sheet	0.5		4	pF
Crystal load capacitance	According to crystal data sheet; including PCB parasitic capacitance	9	10	11	pF
RC OSCILLATOR (OSC16MIN AND OSCEXT32K GROUNDED, OSC16MOUT FLOATING)					
Output frequency	CK32KOUT output		32		kHz
Output frequency accuracy	at 25°C	–15%	0	15%	
Cycle jitter (RMS)	Oscillator contribution			10%	
Output duty cycle		40%	50%	60%	
Settling time				150	µs
Ground current	Active at fundamental frequency		4		µA

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7.14 VRTC LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage V_{IN}	On mode		2.5		5.5	V
	Backup mode		1.9		3	
DC output voltage V_{OUT}	On mode, 3 V < V_{IN} < 5.5 V		1.78	1.83	1.9	V
	Backup mode, 2.3 V ≤ V_{IN} ≤ 2.6 V		1.72	1.78	1.9	
Rated output current I_{OUTmax}	On mode		20			mA
	Backup mode		0.1			
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0				100	mV
	Backup mode, I_{OUT} = I_{OUTmax} to 0				100	
DC line regulation	On mode, V_{IN} = 3 V to V_{INmax} at I_{OUT} = I_{OUTmax}				2.5	mV
	Backup mode, V_{IN} = 2.3 V to 5.5 V at I_{OUT} = I_{OUTmax}				100	
Transient load regulation	On mode, V_{IN} = V_{INmin} + 0.2 V to V_{INmax} I_{OUT} = I_{OUTmax}/2 to I_{OUTmax} in 5 µs and I_{OUT} = I_{OUTmax} to I_{OUTmax} / 2 in 5 µs				50 (1)	mV
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs and V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax} / 2				25 (1)	mV
Turn-on time	I_{OUT} = 0, V_{IN} rising from 0 up to 3.6 V, at V_{OUT} = 0.1 V up to V_{OUTmin}			2.2		ms
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = V_{INmin} + 0.1 V to V_{INmax} at I_{OUT} = I_{OUTmax} / 2	f = 217 Hz		55		dB
		f = 50 kHz		35		
Ground current	Device in ACTIVE state			23		µA
	Device in BACKUP or OFF state			3		

(1) These parameters are not tested. They are used for design specification only.

7.15 VIO SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage (VCCIO and VCC7) V_{IN}	V_{OUT} = 1.5 V, 1.8 V, 2.5 or 3.3 V		4		5.5	V
DC output voltage (V_{OUT})	PWM mode (VIO_PSKIP = 0) I_{OUT} = 0	VSEL = 00	–1.5%	1.5	3%	V
		VSEL = 01	–1.5%	1.8	3%	
		VSEL = 10	–1.5%	2.5	3%	
		VSEL = 11	–1.5%	3.3	3%	
		Power down		0		
Rated output current I_{OUTmax}	TPS659119xAIPFPRQ1		1500			mA
P-channel MOSFET	V_{IN} = V_{INmin}			300		mΩ
On-resistance $R_{DS(ON)_PMOS}$	V_{IN} = 4 V			250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INMAX}, SWIO = 0 V				2	µA
N-channel MOSFET	V_{IN} = V_{MIN}			300		mΩ
On-resistance $R_{DS(ON)_NMOS}$	V_{IN} = 4 V			250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SWIO = V_{INmax}				2	µA
PMOS and NMOS current limit (high side and low side) TPS659119xAIPFPRQ1	V_{IN} = V_{INmin} to V_{INmax} source current load; when ILIM[1:0] = 00		700			mA
	when ILIM[1:0] = 01		1200			mA
	when ILIM[1:0] = 10		1700			mA
	when ILIM[1:0] = 11		> 1700			mA
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}				60	mV/A

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VIO SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} at I_{OUT} = 0				30	mV
Transient load regulation	V_{OUT} = 1.8 V I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs I_{OUT} = 700 to 1200 mA , Max slew = 100 mA/µs			50		mV
t_{on}, off to on	I_{OUT} = 200 mA			350		µs
Overshoot	SMPS turned on			3%		
Power-save mode ripple voltage	PFM (pulse skip mode) mode, I_{OUT} = 1 mA			0.025 × V_{OUT}		V_{PP}
Switching frequency			2.7	3	3.3	MHz
Duty cycle					100%	
Minimum on time $T_{ON(MIN)}$ P-channel MOSFET				35		ns
VFBIO internal resistance			0.5	1		MΩ
Ground current (I_Q)	Off				1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VIO_PSKIP = 0			7500		
	PFM (pulse skipping) mode, no switching, 3-MHz clock on			250		
	Low-power (pulse skipping) mode, no switching	ST[1:0] = 11		63		
Conversion efficiency	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:	I_{OUT} = 10 mA		40%		
		I_{OUT} = 100 mA		83%		
		I_{OUT} = 400 mA		85%		
		I_{OUT} = 600 mA		80%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:	I_{OUT} = 1 mA		68%		
		I_{OUT} = 10 mA		80%		
		I_{OUT} = 400 mA		85%		

7.16 VDD1 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC1 and VCC7) V_{IN}	V_{OUT} ≤ 2.7 V	4		5.5	V
	V_{OUT} > 2.7 V	4		5.5	
DC output voltage (V_{OUT})	I_{OUT} = 0 mA, PWM; V_{IN} = 4 V to 5.5 V; V_{OUT} > 1 V; ON MODE:	–1.5%		3%	V
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}		1500			mA
P-channel MOSFET on-resistance $R_{DS(ON)_PMOS}$	V_{IN} = 4 V		250	400	mΩ
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INmax}, SW1 = 0 V			2	µA
N-channel MOSFET on-resistance $R_{DS(ON)_NMOS}$	V_{IN} = 4 V		250	400	mΩ
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW1 = V_{INmax}			2	µA
PMOS current limit (high side)	V_{IN} = V_{INmin} to V_{INmax}	1700			mA
NMOS current limit (low side)	V_{IN} = V_{INmin} to V_{INmax}, source current load	1700			mA
	V_{IN} = V_{INmin} to V_{INmax}, sink current load	1700			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			60	mV/A

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VDD1 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} at I_{OUT} = 0				30	mV
Transient load regulation	V_{OUT} = 1.2 V I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs I_{OUT} = 700 mA to 1.2 A , Max slew = 100 mA/µs			50		mV
t_{on}, off to on	I_{OUT} = 200 mA			350		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA	TSTEP[2:0] = 001		12.5		mV/µs
		TSTEP[2:0] = 011 (default)		7.5		
		TSTEP[2:0] = 111		2.5		
Overshoot	SMPS turned on			3%		
Power-save mode ripple voltage	PFM (pulse skip mode), I_{OUT} = 1 mA			0.025 × V_{OUT}		V_{PP}
Switching frequency			2.7	3	3.3	MHz
Duty cycle					100%	
Minimum on time $t_{ON(MIN)}$ P-channel MOSFET				35		ns
VFB1 internal resistance			0.5	1		MΩ
Ground current (I_Q)	Off				1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD1_PSKIP = 0			7500		
	Pulse skipping mode, no switching			78		
	Low-power (pulse skipping) mode, no switching	ST[1:0] = 11		63		
Conversion efficiency	PWM mode, DCR_L < 0.1 Ω, V_{OUT} = 1.2 V, V_{IN} = 4 V:	I_{OUT} = 10 mA		35%		
		I_{OUT} = 100 mA		78%		
		I_{OUT} = 400 mA		80%		
		I_{OUT} = 800 mA		74%		
		I_{OUT} = 1500 mA		62%		
	PFM mode, DCR_L < 0.1 Ω, V_{OUT} = 1.2 V, V_{IN} = 4 V:	I_{OUT} = 1 mA		59%		
		I_{OUT} = 10 mA		70%		
		I_{OUT} = 400 mA		80%		

7.17 VDD2 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC2 and VCC7) V_{IN}	V_{OUT} ≤ 2.7 V	4		5.5	V
	V_{OUT} > 2.7 V	4		5.5	
DC output voltage (V_{OUT})	V_{OUT} = 0 mA, PWM; V_{IN} = 4 V to 5.5 V; V_{OUT} > 1 V; ON MODE:	–1.5%		3%	V
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}		1500			mA
P-channel MOSFET on-resistance $R_{DS(ON)_PMOS}$	V_{IN} = 4 V		250	400	mΩ

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VDD2 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P-channel leakage current I_{LK_PMOS}	$V_{IN} = V_{INmax}$, SW2 = 0 V				2	µA
N-channel MOSFET on-resistance $R_{DS(ON)_NMOS}$	V_{IN} = 4 V			250	400	mΩ
N-channel leakage current I_{LK_NMOS}	$V_{IN} = V_{INmax}$, SW2 = V_{INmax}				2	µA
PMOS current limit (high side)	$V_{IN} = V_{INmin}$ to V_{INmax}, source current load		1700			mA
NMOS current limit (low side)	$V_{IN} = V_{INmin}$ to V_{INmax}, source current load		1700			mA
	$V_{IN} = V_{INmin}$ to V_{INmax}, sink current load		1700			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}				60	mV/A
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at I_{OUT} = 0				30	mV
Transient load regulation	V_{OUT} = 1.2 V I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs I_{OUT} = 700 mA to 1.2 A , Max slew = 100 mA/µs			50		mV
t_{on}, Off to on	I_{OUT} = 200 mA			350		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA	TSTEP[2:0] = 001		12.5		mV/µs
		TSTEP[2:0] = 011 (default)		7.5		
		TSTEP[2:0] = 111		2.5		
Overshoot	SMPS turned on			3%		
Power-save mode ripple voltage	PFM (pulse skip mode), I_{OUT} = 1 mA			0.025 × V_{OUT}		V_{PP}
Switching frequency			2.7	3	3.3	MHz
Duty cycle					100%	
Minimum on time				35		ns
P-Channel MOSFET						
VFB2 internal resistance			0.5	1		MΩ
Ground current (I_Q)	Off				1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD2_PSKIP = 0			7500		
	PFM (pulse skipping) mode, no switching			78		
	Low-power (pulse skipping) mode, no switching	ST[1:0] = 11		63		

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VDD2 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Conversion efficiency	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 4 V:	I_{OUT} = 10 mA		35%		
		I_{OUT} = 100 mA		78%		
		I_{OUT} = 400 mA		80%		
		I_{OUT} = 800 mA		74%		
		I_{OUT} = 1200 mA		66%		
		I_{OUT} = 1500 mA		62%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 4 V:	I_{OUT} = 1 mA		59%		
		I_{OUT} = 10 mA		70%		
		I_{OUT} = 400 mA		80%		
	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:	I_{OUT} = 10 mA		39%		
		I_{OUT} = 100 mA		85%		
		I_{OUT} = 400 mA		91%		
		I_{OUT} = 800 mA		90%		
		I_{OUT} = 1200 mA		86%		
		I_{OUT} = 1500 mA		84%		
	PFM mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:	I_{OUT} = 1 mA		80%		
		I_{OUT} = 10 mA		82%		
		I_{OUT} = 400 mA		92%		

7.18 EXTCTRL

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ratio of VSENSE to VOUT (Selectable voltage divider)	SEL[6:0] = 0 (EN signal low)		1		V/V
	SEL[6:0] = 1 to 3		1		
	For SEL[6:0] = 3 to 67				
	Ratio = 48 / (45 + SEL[6:0])				
	SEL[6:0] = 4	–0.7%	48:49	0.7%	
	SEL[6:0] = 5	–0.7%	24:25	0.7%	
	...				
	SEL[6:0] = 35	–0.7%	3:5	0.7%	
	...				
	SEL[6:0] = 66	–0.7%	16:37	0.7%	
	SEL[6:0] = 67 to 127	–0.7%	3:7	0.7%	
Programmable voltage step size (with a 0.8 V reference)			16.7		mV
Output voltage transition rate (with 0.8 V reference)	From V_{OUT} = 0.8 V to 1.87 V and V_{OUT} = 1.87 V to 0.8 V		100 (1)		mV / 20 µs

(1) 100 mV / 20 µs reached with 50 mV / 10 µs steps

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7.19 LDO1 AND LDO2

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL LDO1 AND LDO2 CHARACTERISTICS							
V_{IN}	Input voltage (VCC6)	V_{OUT}(LDO1) = 1.05 V at 320 mA and V_{OUT}(LDO2) = 1.05 V at 160 mA		1.4		3.6	V
		V_{OUT}(LDO1) = 1.2 V / 1.5 V at 100 mA and V_{OUT}(LDO2) = 1.2 V / 1.1 V / 1 V		1.7		3.6	
		V_{OUT}(LDO1) = 1.5 V and V_{OUT} (LDO1, LDO2) = 1.8 V at 200 mA		2.1		3.6	
		V_{OUT}(LDO1) = 1.8 V and V_{OUT}(LDO2) = 1.8 V		2.7		3.6	
		V_{OUT}(LDO1) = 2.7 V		3.2		3.6	
		V_{OUT} (LDO1) = V_{OUT}(LDO2) = 3.3 V		3.5		3.6	
LDO1							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA,		1		3.3	V
		Step size			50		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA,		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		320			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV		330	600	1000	mA
V_{DO}	Dropout voltage	ON mode, $V_{DO} = V_{IN} – V_{OUT}$, V_{IN} = 1.4 V, $I_{OUT} = I_{OUTmax}$				350	mV
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				17	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	ON mode, V_{IN} = 1.5 V, V_{OUT} = 1.05 V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs			20		mV
	Transient line regulation	On mode, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs, and V_{IN} = 2.7 to 2.7 + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}$			5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		50	75	100	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		200	300	420	
	Turn-on inrush current	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA,			300	600	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+}= 1.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO1 internal resistance	LDO off			600		Ω
	Ground current	On mode, I_{OUT} = 0			63	75	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			22	20	
		Off mode (max 85°C)				2.7	
LDO2							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA,		1		3.3	V
		Step size			50		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA,		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		320			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV		330	600	1000	mA

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LDO1 AND LDO2 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	ON mode, $V_{DO} = V_{IN} - V_{OUT}$, V_{IN} = 1.4 V, $I_{OUT} = I_{OUTmax}$				350	mV
	DC load regulation	On mode, I_{OUT} = IOUTmax				17	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	ON mode, V_{IN} = 1.5 V, V_{OUT} = 1.05 V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs			20		mV
	Transient line regulation	On mode, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs, and V_{IN} = 2.7 to 2.7 + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}$			5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		40	75	100	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		200	300	420	
	Turn-on inrush current				300	600	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 1.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO2 internal resistance	LDO off			600		Ω
	Ground current	On mode, I_{OUT} = 0			63	75	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			22	20	
		Off mode (max 85°C)				2.7	

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7.20 LDO3 and LDO4

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL LDO3 AND LDO4 CHARACTERISTICS							
V_{IN}	Input voltage (VCC5)	V_{OUT} (LDO3) = 1.8 V and V_{OUT} (LDO4) = 1.8 V / 1.1 V / 1 V		2.7		5.5	V
		V_{OUT} (LDO3) = 2.6 V and V_{OUT} (LDO4) = 2.5 V		3		5.5	
		V_{OUT} (LDO3) = 2.8 V		3.2		5.5	
LDO3							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} - V_{DO}$, I_{OUT} = 0 mA,		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} - V_{DO}$, I_{OUT} = 0 mA,		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		200			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} - 100$ mV		330	550	650	mA
V_{DO}	Dropout voltage	On mode, V_{OUTtyp} = 3.3 V, $V_{DO} = V_{IN} - V_{OUT}$, V_{IN} = 3.3 V, $I_{OUT} = I_{OUTmax}$			150	270	mV
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				28	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	On mode, V_{IN} = 2.7 V, V_{OUTtyp} = 1.8 V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs			15		mV
	Transient line regulation	On mode, V_{OUTtyp} = 1.8 V, $I_{OUT} = I_{OUTmax}$, $V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs and $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}$			0.5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		25	50	70	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	230	
	Turn-on inrush current				200	450	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 50 kHz		40		
	LDO3 internal resistance	LDO off			500		kΩ
	Ground current	On mode, I_{OUT} = 0			65	76	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			14	22	
		Off mode				1	
LDO4							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} - V_{DO}$, I_{OUT} = 0 mA		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} - V_{DO}$, I_{OUT} = 0 mA,		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		50			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} - 100$ mV		200	400	500	mA
V_{DO}	Dropout voltage	On mode, V_{OUTtyp} = 3.3 V, $V_{DO} = V_{IN} - V_{OUT}$ V_{IN} = 3.3 V, $I_{OUT} = I_{OUTmax}$			100	160	mV
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				6	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV

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LDO3 and LDO4 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Transient load regulation	On mode, V_{IN} = 2.7 V, V_{OUTtyp} = 1.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs			6		mV
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs and V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax} / 2			0.2		mV
Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		25	50	70	µs
	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	230	
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+}= 3.8 V, I_{OUT} = I_{OUTmax} / 2	f = 217 Hz		70		dB
		f = 50 kHz		40		
LDO4 internal resistance	LDO Off			500		kΩ
Ground current	On mode, I_{OUT} = 0			55	65	µA
	On mode, I_{OUT} = I_{OUTmax}				900	
	Low-power mode			14	17	
	Off mode				1	

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7.21 LDO5

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS							
V_{IN}	Input voltage (VCC4)	V_{OUT} (LDO5) ≤ 1.2 V		1.7		1.9	V
		V_{OUT} (LDO5) > 1.2 V (See Dropout Voltage parameter for additional constraints)		1.7		5.5	
		V_{OUT} (LDO5) = 2.5 V		3.2		5.5	
		V_{OUT} (LDO5) = 2.8 V at I_{load} = 200 mA		3.2		5.5	
LDO5							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		300			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV		330	550	650	mA
V_{DO}	Dropout voltage	On mode, $V_{DO} = V_{IN} – V_{OUT}$	V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$			500	mV
			V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
			V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
			V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
			V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
			V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				16	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at I_{OUTmax}				1	mV
	Transient load regulation	On mode, V_{IN} = 3.2 V, V_{OUTtyp} = 2.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs			16		mV
	Transient line regulation	On mode, $V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs and $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}$			4		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		20	50	70	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	250	
	Turn-on inrush current				200	450	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO5 internal resistance	LDO Off			60		Ω
	Ground current	On mode, I_{OUT} = 0			65	76	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			14	22	
		Off mode				1	

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7.22 LDO6 and LDO7

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL LDO6 AND LDO7 CHARACTERISTICS							
V_{IN}	Input voltage (VCC3 for LDO6 & LDO7)	V_{OUT} (LDO6/7) ≤ 1.2 V		1.7		1.9	V
		V_{OUT} (LDO6/7) > 1.2 V (See Dropout Voltage parameter for additional constraints)		1.7		5.5	
		V_{OUT}(LDO7) = 2.8 V		3.2		5.5	
		V_{OUT}(LDO7) = 3.3 V		3.6		5.5	
		V_{OUT}(LDO7) = 2.8 V at 250 mA		3.2		5.5	
		V_{OUT}(LDO7) = 3 V		3.6		5.5	
		V_{OUT}(LDO7) = 3.3 V at 250 mA		3.6		5.5	
LDO6							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		300			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV		330	550	650	mA
V_{DO}	Dropout voltage	On mode, $V_{DO} = V_{IN} – V_{OUT}$,	V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$			500	mV
			V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
			V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
			V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
			V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
			V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
	DC load regulation	On mode, $I_{OUT} = I_{OUTmin}$				16	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	On mode, V_{IN} = 3.2 V, V_{OUTtyp} = 2.8 V I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs			20		mV
	Transient line regulation	On mode, V_{IN} = 2.7 V + 0.5 V to 2.7 V in 30 µs and V_{IN} = 2.7 V to 2.7 V + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}$			5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		20	50	70	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	250	
	Turn-on inrush current				200	450	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO6 internal resistance	LDO off			60		Ω
	Ground current	On mode, I_{OUT} = 0			65	76	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			14	22	
		Off mode				1	
LDO7							
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		–2.5%		3%	

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LDO6 and LDO7 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUTmax}	Rated output current	On mode		300			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} - 100$ mV		330	550	650	mA
V_{DO}	Dropout voltage	On mode, $V_{DO} = V_{IN} - V_{OUT}$,	V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$			500	mV
			V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
			V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
			V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
			V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
			V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				24	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	On mode, V_{IN} = 3.6 V, V_{OUTtyp} = 3.3 V $I_{OUT} = 0.1 \times I_{OUTmax}$ to $0.9 \times I_{OUTmax}$ in 5 µs and $I_{OUT} = 0.9 \times I_{OUTmax}$ to $0.1 \times I_{OUTmax}$ in 5 µs			16		mV
	Transient line regulation	On mode, $I_{OUT} = I_{OUTmax} / 2$, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs and V_{IN} = 2.7 V + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax} / 2$			5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		20	50	70	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	250	
	Turn-on inrush current				200	450	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax} / 2$	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO7 internal resistance	LDO off			60		Ω
	Ground current	On mode, I_{OUT} = 0			65	76	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			14	22	
		Off mode				1	

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7.23 LDO8

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage (VCC8)	V_{OUT}(VLDO8) ≤ 1.2 V		1.7		1.9	V
		V_{OUT}(VLDO8) > 1.2 V (See Dropout Voltage parameter for additional constraints)		1.7		5.5	
V_{OUT}	DC output voltage	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		1		3.3	V
		Step size			100		mV
	DC output voltage accuracy	ON and low-power mode, $V_{OUT} < V_{IN} – V_{DO}$, I_{OUT} = 0 mA		–2.5%		3%	
I_{OUTmax}	Rated output current	On mode		300			mA
		Low-power mode		1			
	Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} – 100$ mV		330	550	650	mA
V_{DO}	Dropout voltage	On mode, $V_{DO} = V_{IN} – V_{OUT}$	V_{IN} = 3.3 V, I_{OUT} = 70 mA			100	mV
			V_{IN} = 3.3 V, I_{OUT} = 10 mA			25	
			V_{IN} = 2.7 V, $I_{OUT} = I_{OUTmax}$			500	
			V_{IN} = 2.7 V, I_{OUT} = 250 mA			400	
			V_{IN} = 2.7 V, I_{OUT} = 200 mA			300	
			V_{IN} = 1.7 V, I_{OUT} = 180 mA			700	
			V_{IN} = 1.7 V, I_{OUT} = 150 mA			500	
			V_{IN} = 1.7 V, I_{OUT} = 100 mA			300	
	DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$				26	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$				1	mV
	Transient load regulation	On mode, V_{IN} = 1.7 V, V_{OUTtyp} = 1.2 V I_{OUT} = 10 mA to 90 mA in 5 µs and I_{OUT} = 90 mA to 10 mA in 5 µs			7		mV
	Transient line regulation	On mode, I_{OUT} = 100 mA, V_{IN} = 2.7 V + 0.2 V to 2.7 V in 30 µs and V_{IN} = 2.7 V to 2.7 V + 0.2 V in 30 µs, I_{OUT} = 100 mA			5		mV
	Turn-on time	I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmin}		20	50	70	µs
		I_{OUT} = 0, at V_{OUT} = 0.1 V up to V_{OUTmax}		120	180	250	
	Turn-on inrush current				200	450	mA
	Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}$ / 2	f = 217 Hz		70		dB
			f = 20 kHz		40		
	LDO8 internal resistance	LDO off			60		Ω
	Ground current	On mode, I_{OUT} = 0			65	76	µA
		On mode, $I_{OUT} = I_{OUTmax}$				2000	
		Low-power mode			14	22	
		Off mode				1	

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7.24 Timing Requirements for Boot Sequence Example

See Figure 1.

PARAMETER		MIN	NOM	MAX	UNIT
t_{dsON1}	PWRHOLD rising edge to VIO, LDO5 enable delay		66 × t_{CK32k} = 2060		µs
t_{dsON2}	VIO to VDD2 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON3}	VDD2 to VDD1 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON4}	VDD1 to LDO4 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON5}	LDO4 to LDO3, LDO8 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON6}	LDO3 to LDO6 enable delay		64 × t_{CK32k} = 2000		µs
t_{dsON7}	LDO6 to CLK32KOUT rising-edge delay		9 × 64 × t_{CK32k} = 18000		µs
t_{dsON8}	CLK32KOUT to NRESPWON, NRESPWON2 rising-edge delay		64 × t_{CK32k} = 2000		µs
t_{dsONT}	Total switch-on delay		32		ms
t_{dsOFF1}	PWRHOLD falling-edge to NRESPWON, NRESPWON2 falling-edge delay		2 × t_{CK32k} = 62.5		µs
$t_{dsOFF1B}$	NRESPWON falling-edge to CLK32KOUT low delay		3 × t_{CK32k} = 92		µs
t_{dsOFF2}	PWRHOLD falling-edge to supplies and reference disable delay		5 × t_{CK32k} = 154		µs

7.25 Power Control Timing Requirements

See Figure 2.

PARAMETER			MIN	NOM	MAX	UNIT
$t_{dbPWRONF}$	PWRON falling-edge debouncing delay			100		µs
$t_{dbPWRONR}$	PWRON rising-edge debouncing delay			3 × t_{CK32k} = 94		µs
$t_{dbPWRHOLD}$	PWRON rising-edge debouncing delay			2 × t_{CK32k} = 63		µs
t_{dOINT1}	INT1 (internal) power-on pulse duration after PWRON low-level (debounced) event			1		s
$t_{dONPWHOLD}$	delay to set high PWRHOLD signal or DEV_ON control bit after NRESPWON released to keep on the supplies			t_{dOINT1} – t_{DSONT} = 970 (1)		ms
$t_{dPWRONLP}$	PWRON long-press delay	PWRON falling-edge to PWRON_LP_IT		4		s
$t_{dPWRONLPTO}$	PWROW long-press interrupt (PWRON_LP_IT) to supplies switch-off	PWRON_LP_IT to NRESPWRON falling-edge		1		s

(1) T_{dSONT} = 30 ms, as in example boot sequence.

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7.26 Device SLEEP State Control Timing Requirements

See Figure 4.

PARAMETER			MIN	NOM	MAX	UNIT
$t_{ACT2SLP}$	SLEEP falling-edge to supply n low-power mode (SLEEP resynchronization delay)		$2 \times t_{CK32k}$ = 62		$3 \times t_{CK32k}$ = 94	µs
$t_{ACT2SLP}$	SLEEP falling-edge to CLK32KOUT low		156	$t_{ACT2SLP} + 3 \times t_{CK32k}$	188	µs
$t_{SLP2ACT}$	SLEEP rising edge to supply in high-power mode		$8 \times t_{CK32k}$ = 250		$9 \times t_{CK32k}$ = 281	µs
$t_{SLP2ACTCK32K}$	SLEEP rising edge to CLK32KOUT running		344	$t_{SLP2ACT} + 3 \times t_{CK32k}$	375	µs
$t_{dSLPON1}$	SLEEP rising edge to time step 1 of the turn-on sequence from SLEEP state		281	$t_{SLP2ACT} + 1 \times t_{CK32k}$	312	µs
$t_{dSLPONST}$	turn-on sequence step duration, from SLEEP state	TSLOT_LENGTH[1:0] = 00		0		µs
		TSLOT_LENGTH[1:0] = 01		200		
		TSLOT_LENGTH[1:0] = 10		500		
		TSLOT_LENGTH[1:0] = 11		2000		
$t_{dSLPONDCDC}$	VDD1, VDD2, or VIO turn-on delay from turn-on sequence time step			$2 \times t_{CK32k}$ = 62		µs

7.27 Supplies State Control Through EN1 and EN2 Timing Characteristics

See Figure 5 and Figure 6

PARAMETER		MIN	NOM	MAX	UNIT
t_{dEN}	NRESPWRON to to supply state change delay, EN1 or EN2 driven		0		ms
t_{dOEN}	EN1 or EN2 edge to supply state change delay		$1 \times t_{CK32k}$ = 31		µs
t_{dVDDEN}	EN1 or EN2 edge to VDD1 or VDD2 DCDC turn on delay		$3 \times t_{CK32k}$ = 63		µs

7.28 VDD1 Supply Voltage Control Through EN1 Timing Requirements

See Figure 7

PARAMETER			MIN	NOM	MAX	UNIT
t_{dDVSEN}	EN1 (or EN2) edge to VDD1 (or VDD2) voltage change delay			$2 \times t_{CK32k}$ = 62		µs
$t_{dDVSENL}$	VDD1 (or VDD2) voltage settling delay	TSTEP[2:0] = 001		32		µs
		TSTEP[2:0] = 011 (default)		0.4 / 7.5 = 53		
		TSTEP[2:0] = 111		160		

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The TPS659119-Q1 device supports one fixed boot sequence and one EEPROM-programmable boot sequence. The *Timing Requirements for Boot Sequence Example* section lists and Figure 1 shows an example boot sequence. See the *Boot Configuration and Switch-On and Switch-Off Sequences* section for additional information on boot-mode selection.

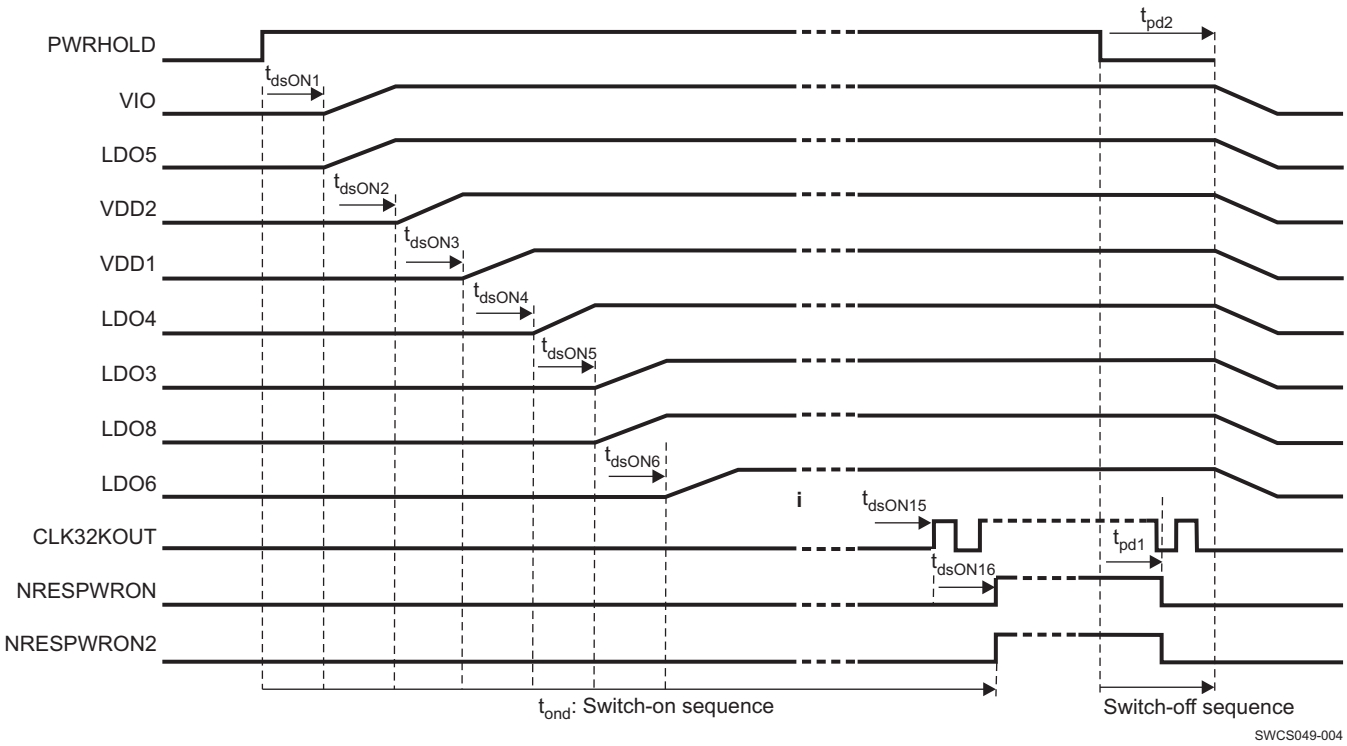

Figure 1. Boot Sequence Example With 2-ms Time Slot and Simultaneous Switch-Off of Resources

Figure 2 shows the device-state control through the PWRON signal (see the *Power Control Timing Requirements* section).

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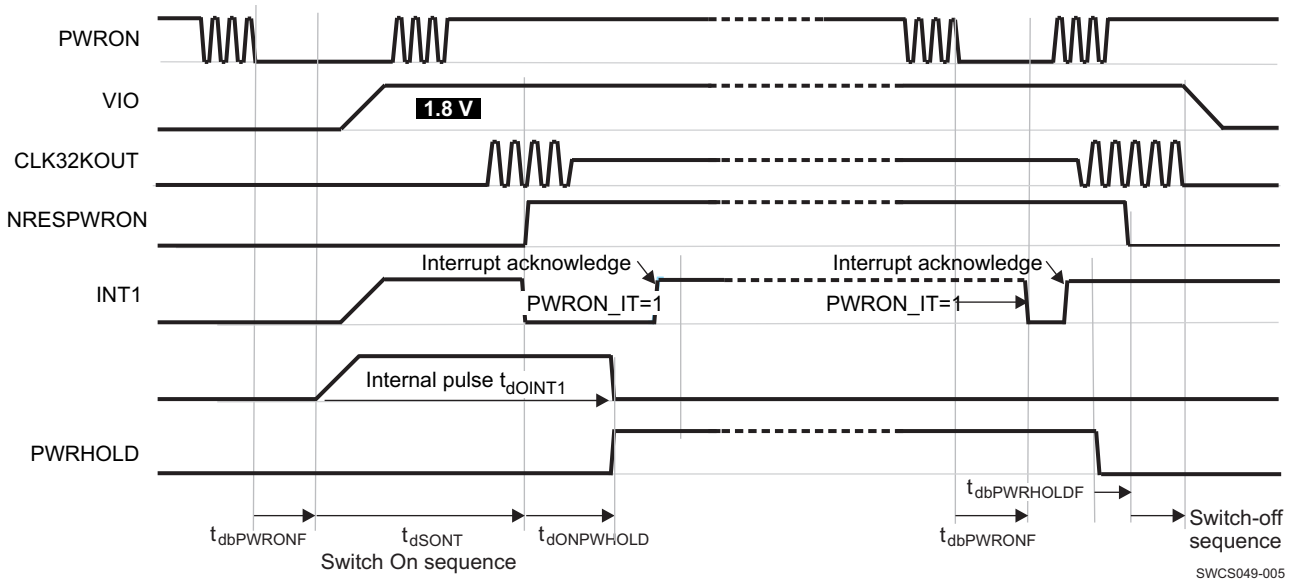


NOTE: DEV_ON or AUTODEV_ON control bits can be used instead of PWRHOLD signal to maintain supplies on after switch-on sequence.

NOTE: Internal POWER ON enable condition pulse T_{dOINT1} keeps device active until PWRHOLD acknowledge.

Figure 2. Device State Control Through PWRON Signal

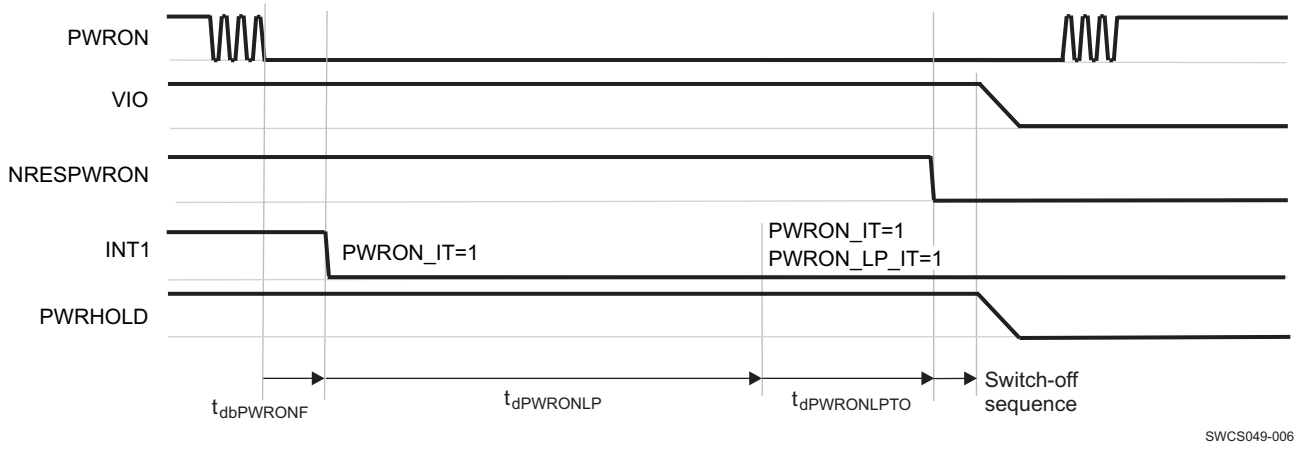
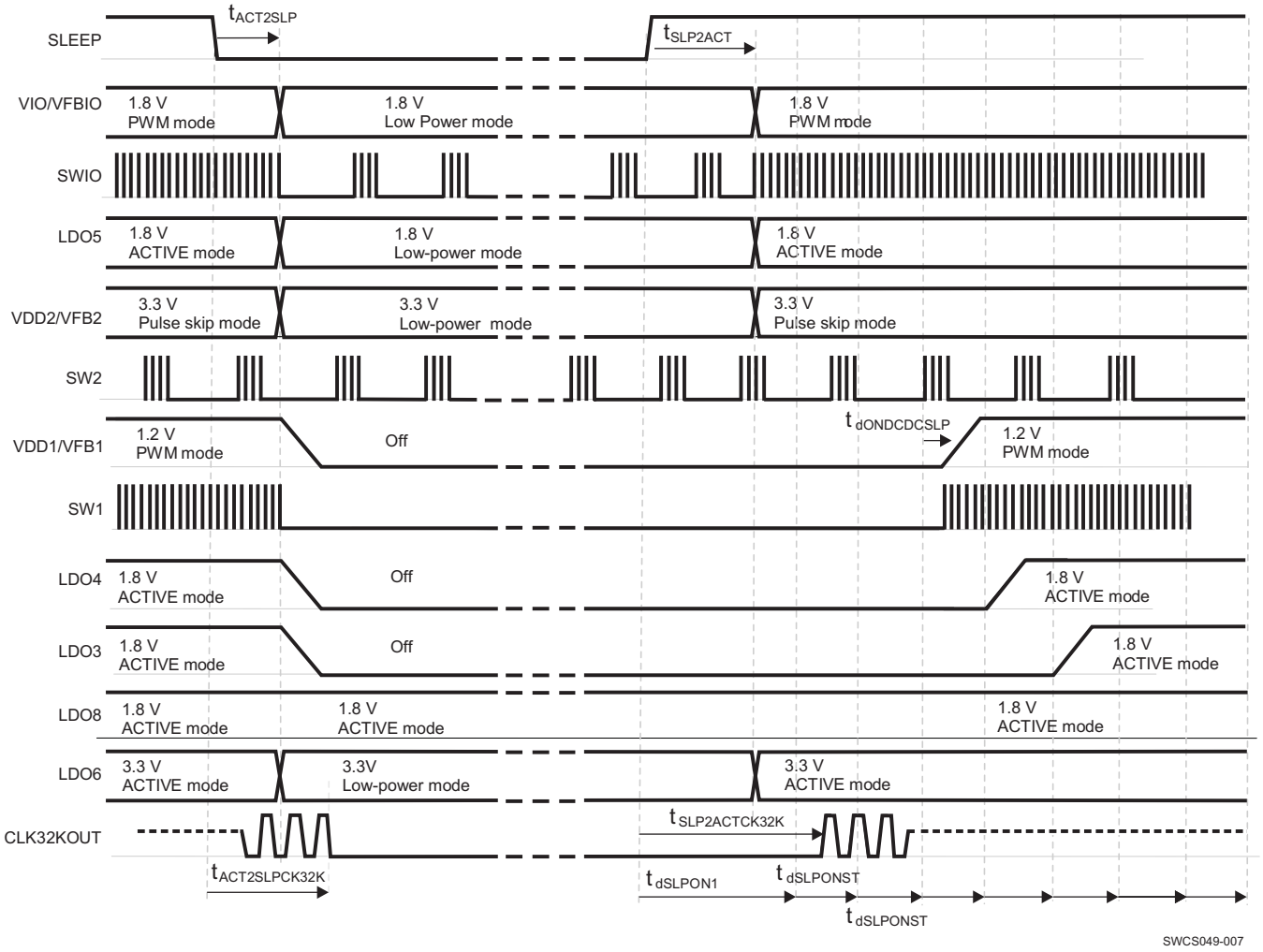


Figure 3. PWRON Long-Press Turn-Off

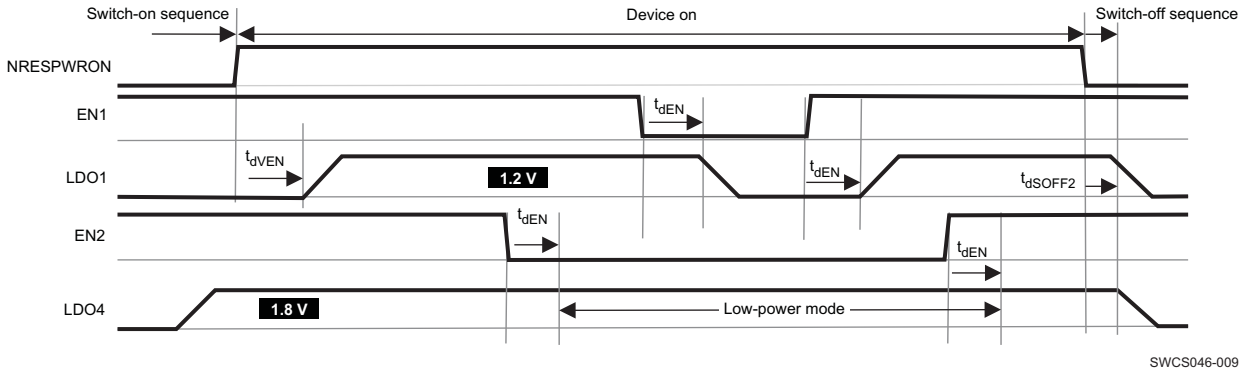
The *Power Control Timing Requirements* Section Lists the Power Control Timing Characteristics



NOTE: Registers programming: VIO_PSKIP = 0, VDD1_PSKIP = 0, VDD1_SETOFF = 1, LDO3_SETOFF = 1, LDO4_SETOFF = 1, LDO8_KEEPON = 1.

Figure 4. Device SLEEP State Control
See the *Device SLEEP State Control Timing Requirements* Section

Figure 5 and Figure 6 show the state control of the power supplies through the EN1 and EN2 signals (see the *Supplies State Control Through EN1 and EN2 Timing Characteristics* section).



NOTE: Register setting: LDO1_EN1 = 1, LDO4_EN2 = 1, and LDO4_KEEPON = 1.

Figure 5. LDO Type Supplies State Control Through EN1 and EN2

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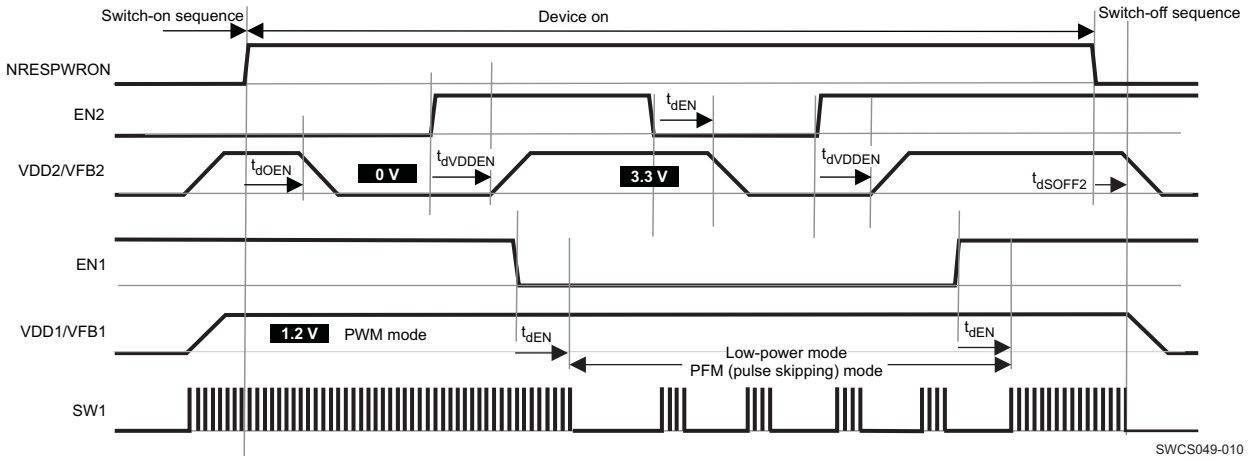
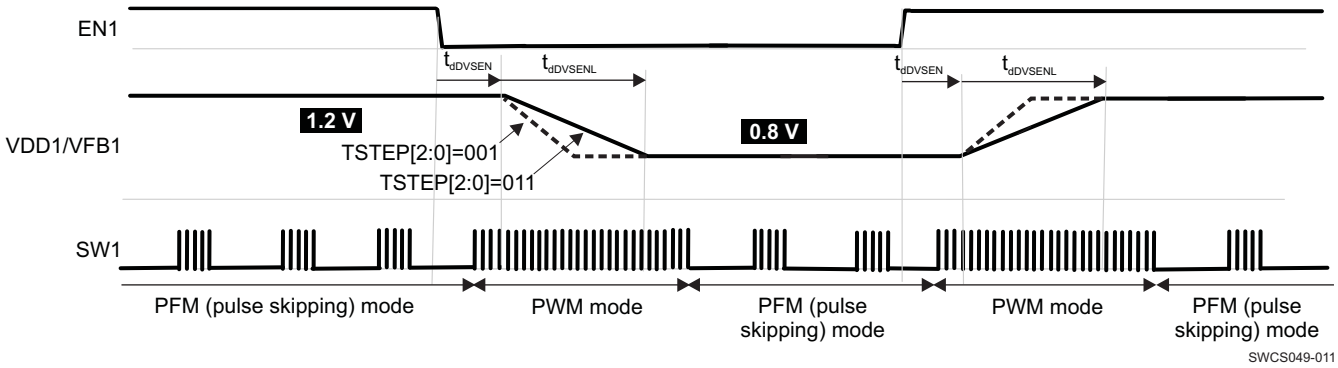


NOTE: Register setting: VDD2_EN2 = 1, VDD1_EN1 = 1, VDD1_KEEPON = 1, VDD1_PSKIP = 0, and SEL[6:0] = hex00 in VDD2_SR_REG.

Figure 6. VDD1 and VDD2 Supplies State Control Through EN1 and EN2



NOTE: Register setting: VDD1_EN1 = 1, SEL[6:0] = hex13 in VDD1_SR_REG

Figure 7. VDD1 Supply Voltage Control Through EN1
See the *VDD1 Supply Voltage Control Through EN1 Timing Requirements* Section

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7.29 Typical Characteristics

7.29.1 VIO SMPS Curves

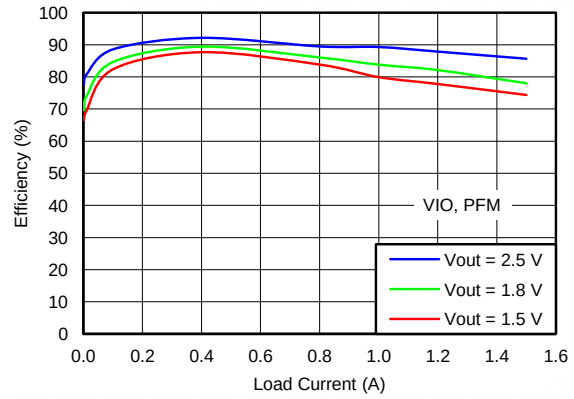

Figure 8. VIO Efficiency vs Load Current, 25°C V_{IN} = 4 V, PFM

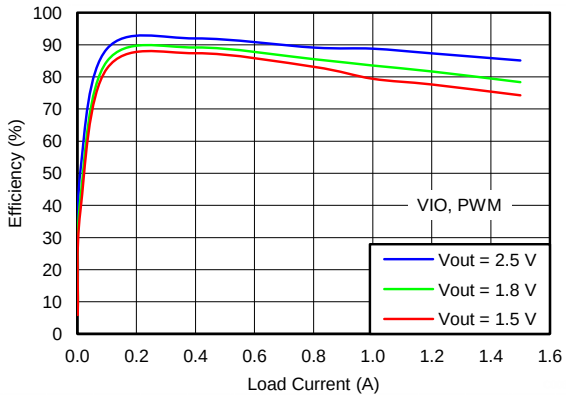

Figure 9. VIO Efficiency vs Load Current, 25°C, V_{OUT} = 2.5 V, V_{IN} = 4 V, PWM

7.29.2 VDD1 SMPS Curves

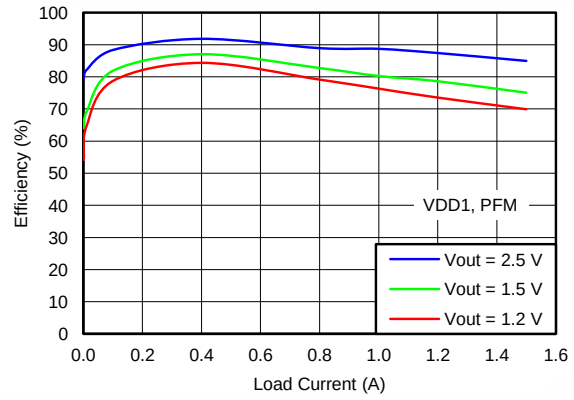

Figure 10. VDD1 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PFM

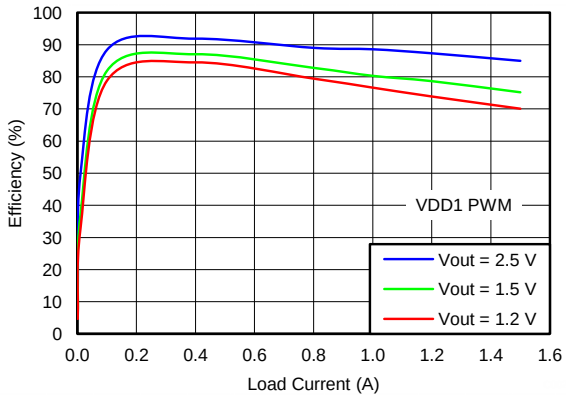

Figure 11. VDD1 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PWM

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7.29.3 VDD2 SMPS Curves

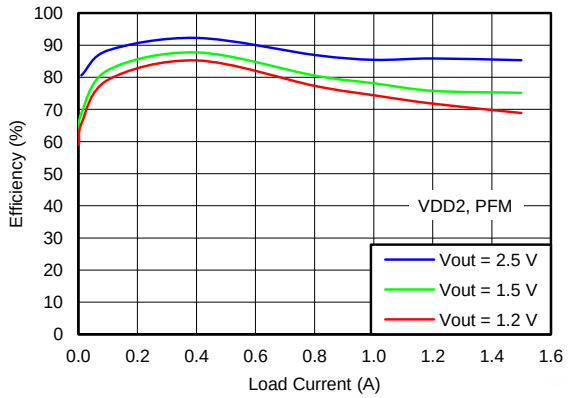

Figure 12. VDD2 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PFM

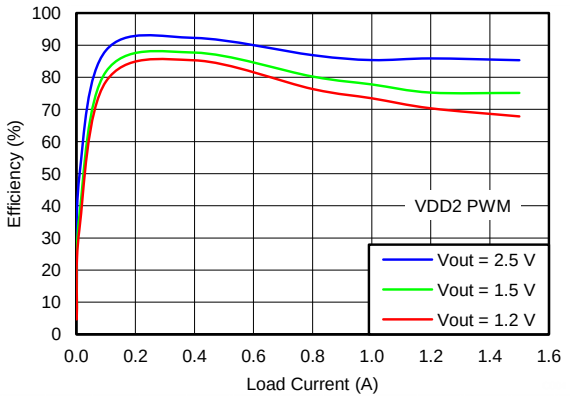

Figure 13. VDD2 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PWM

8 Detailed Description

8.1 Overview

The TPS659119-Q1 device is an integrated power-management integrated-circuit (PMIC) available in an 80-pin, 0,5-mm pitch HTQFP package with thermal pad. This device is designed for automotive applications. The device provides three step-down converters and an interface to control an external converter. The device also provides eight LDOs, nine configurable GPIOs, two LED pulse generators, one PWM generator, and programmability for supporting different processors and applications.

The three step-down converters in this device are high-frequency switch-mode converters with integrated FETs. The converters are capable of synchronizing to an external clock input and support switching frequency between 2.7 MHz and 3.3 MHz. Two of the step-down converters support dynamic voltage scaling by a dedicated I^2C interface for optimum power savings. The third converter can provide power for system I/Os, memory modules, or both which provides four programmable output-voltage settings.

The device includes eight general-purpose LDOs providing a wide range of voltage and current capabilities. Five of the LDOs support 1 to 3.3 V with 100-mV step and three (LDO1, LDO2, LDO4) of the LDOs support 1 to 3.3 V with 50-mV step. All LDOs are fully controllable by the I^2C interface and are supplied from either a system supply or a pre-regulated supply.

The power-up and power-down controller is configurable and programmable through EEPROM. The TPS659119-Q1 devices include a 32-kHz RC oscillator to sequence all resources during power up and power down. In cases where a fast start up is needed, a 16-MHz crystal oscillator is also included to quickly generate a stable 32-kHz for the system. The device also includes an RTC module that provides date, time, calendar, and alarm capability. The RTC module is best used when a 16-MHz crystal or an external and high accuracy 32-kHz clock is present.

The TPS659119-Q1 device also includes nine configurable GPIOs with a multiplexed feature. Four of the GPIOs can be configured and used as enable signals for external resources, which can be included in the power-up and power-down sequence. Two of the GPIOs have a 10-mA current-sink capability for driving external LEDs. The device also includes two on and two off LED-pulse generators and one PWM generator with programmable frequency and duty cycle.

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8.2 Functional Block Diagram

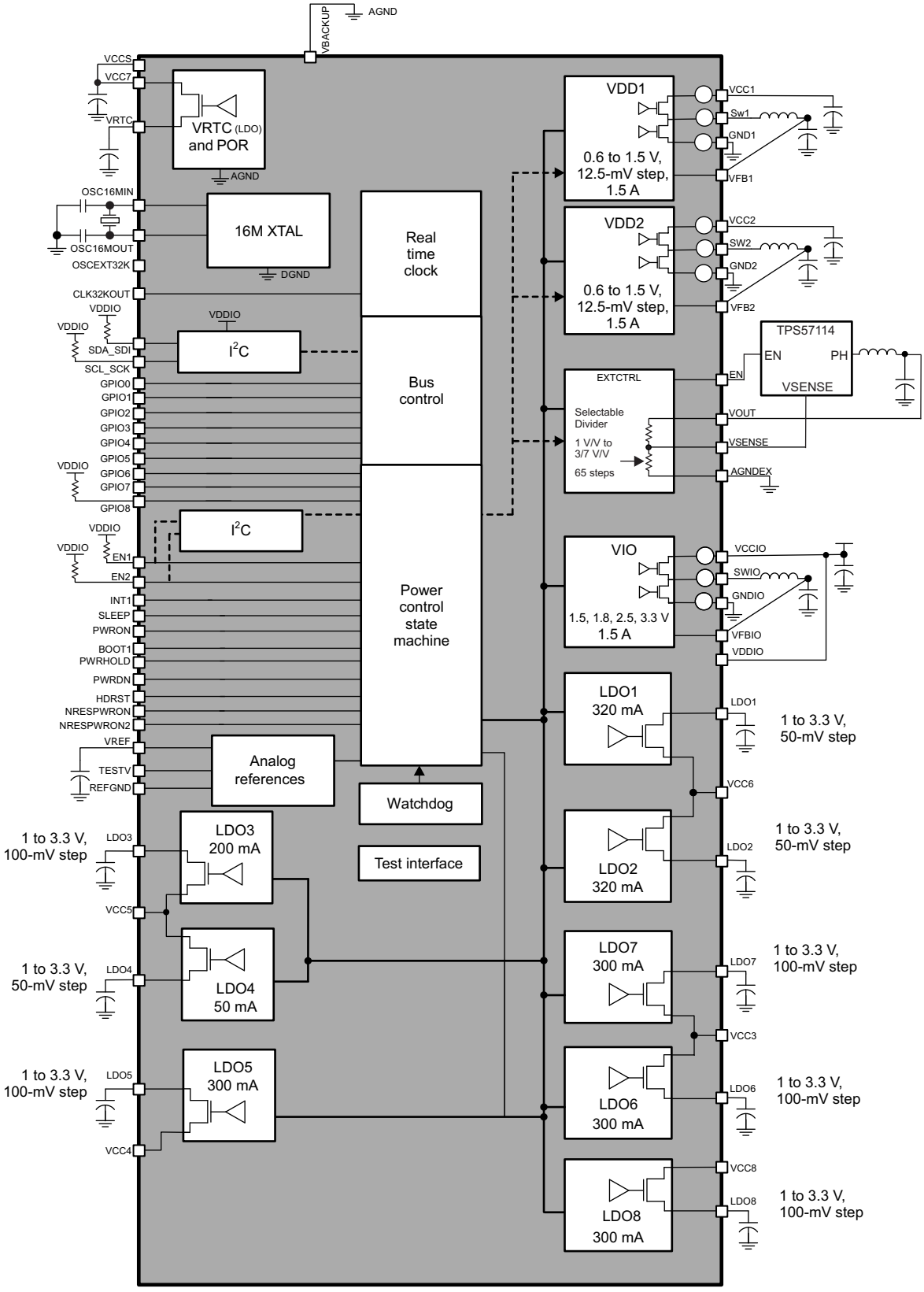

Figure 14. Top-Level Diagram

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8.3 Feature Description

8.3.1 Power Reference

The bandgap voltage reference is filtered by using an external capacitor connected across the VREF output and the analog ground, REFGND (see the *Recommended Operating Conditions* section). The VREF voltage is distributed and buffered inside the device.

8.3.2 Power Resources

The power resources provided by the TPS659119-Q1 device include inductor-based switched-mode power supplies (SMPSs) and linear low-dropout voltage regulators (LDOs). These supply resources provide the required power to the external processor cores and external components, and to modules embedded in the TPS659119-Q1 device.

Two of the integrated SMPSs and the external SMPS controller (EXTCTRL) have voltage scaling capability. These SMPSs provide independent core-voltage domains to the host processor. When changing the output voltage, VDD1 and VDD2 reach the new value through successive steps of 2.5 to 12.5 mV. The size of the voltage step is selected by the TSTEP bit. With a 0.8-V reference, EXTCTRL has a target slew rate of 100 mV / 20 μs. Use Equation 1 to calculate new output values which are reached in successive smaller steps.

$$N \times LSB \quad (1)$$

where

- LSB = 16.7 mV
- N = 1 to 4

A suitable combination of steps is calculated internally based on the current and new target values for the output voltage.

The VIO SMPS provides a supply voltage for the host processor I/Os.

Table 1 lists the power sources provided by the TPS659119-Q1 device.

Table 1. Power Sources

RESOURCE	TYPE	VOLTAGES	POWER
VIO	SMPS	1.5, 1.8, 2.5, and 3.3 V	1500 mA
VDD1	SMPS	0.6 to 1.5 V in 12.5-mV steps Programmable-multiplication factor: x2, x3	1500 mA
VDD2	SMPS	0.6 to 1.5 V in 12.5-mV steps Programmable-multiplication factor: x2, x3	1500 mA
LDO1	LDO	1 to 3.3 V, 0.05-V step	320 mA
LDO2	LDO	1 to 3.3 V, 0.05-V step	320 mA
LDO3	LDO	1 to 3.3 V, 0.1-V step	200 mA
LDO4	LDO	1 to 3.3 V, 0.05-V step	50 mA
LDO5	LDO	1 to 3.3 V, 0.1-V step	300 mA
LDO6	LDO	1 to 3.3 V, 0.1-V step	300 mA
LDO7	LDO	1 to 3.3 V, 0.1-V step	300 mA
LDO8	LDO	1 to 3.3 V, 0.1-V step	300 mA

8.3.3 PWM and LED Generators

The TPS659119-Q1 device has two LED ON and OFF signal generators, LED1 and LED2. The LED1 and LED2 signals have independently controllable periods from 125 ms to 8 s and an ON time from 62.5 to 500 ms. Within the period, one or two ON pulses can be generated (control bit LED1(2)_SEQ). The user must take care to program the period and ON time correctly because no limitation on selected values is imposed. The LED1 and LED2 signals can be routed to GPIO1 and GPO3 open-drain outputs, respectively. These GPIOs have a current-sink capability of 10 mA.

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The PWM generator frequency and duty cycle are set by the PWM_FREQ and PWM_DUTY_CYCLE bits, respectively. The PWM generator signal can be connected to the GPIO3 or GPIO8 output. The PWM generator uses the 3-MHz clock, which is not available in off mode. To enable the PWM in sleep mode, the I2CHS_KEEPON bit must be set to 1.

8.3.4 Dynamic-Voltage Frequency Scaling and Adaptive-Voltage Scaling Operation

Dynamic-voltage frequency scaling (DVFS) operation A supply voltage value corresponding to a targeted frequency of the digital core supplied is programmed in VDD1_OP_REG or VDD2_OP_REG registers. The slew rate of the voltage supply reaching a new VDD1_OP_REG or VDD2_OP_REG programmed value is limited to 12.5 mV/µs, fixed value.

Adaptative-voltage scaling (AVS) operation A supply voltage value corresponding to a supply voltage adjustment is programmed in VDD1_SR_REG or VDD2_SR_REG registers. The supply voltage is then tuned by the digital core supplied, based its performance self-evaluation. The slew rate of VDD1 or VDD2 voltage supply reaching a new programmed value is programmable though the VDD1_REG or VDD2_REG register, respectively.

A serial control interface (optional mode for EN1 and EN2 pins) can be dedicated to voltage scaling applications in order to provide dedicated access to the VDD1_OP_REG, VDD1_SR_REG and VDD2_OP_REG, VDD2_SR_REG registers.

A general-purpose serial-control interface (CTL-I^2C) also gives access to these registers if the SR_CTL_I2C_SEL control bit is set to 1 in the DEVCTRL_REG register (default inactive).

Both control interfaces are compliant with HS-I^2C specification (100 Kbps, 400 Kbps, or 3.4 Mbps).

8.3.5 32-kHz RTC Clock

The TPS659119-Q1 device can provide a 32-kHz clock to the platform through the CLK32KOUT output. Selection of the default RTC clock source is controlled by the EEPROM bit CK32K_CTRL in the DEVCTRL_REG register. This clock must be present for any state of the EPC except the NO SUPPLY state. The following lists the three possible sources for this clock.

Crystal Oscillator To use the crystal oscillator, a 16.384-MHz crystal should be placed between the OSC16MIN and OSC16MOUT pins. The OSCEXT32K pin should be grounded. The 32-kHz clock is produced by dividing the crystal oscillator output by 500. A higher-frequency crystal is used to accelerate the start-up time of the device. Figure 15 shows an essential schematic of the oscillator .

External Clock Source An external 32-kHz clock source may be used by grounding the OSC16MIN pin, floating the OSC16MOUT pin, and applying the clock to the OSCEXT32K pin. When four clock edges are counted on the OSCEXT32K pin, an internal clock-selection MUX selects the external clock source rather than the crystal oscillator. A means of switching between the crystal oscillator and the external clock source is not included in the design. Either one or the other can be used in a given application, but not both.

Internal RC Oscillator Depending on the state of the CK32K_CTRL bit, an internal 32-kHz RC oscillator can also be used as the clock source for the RTC if an accurate time-base is not required.

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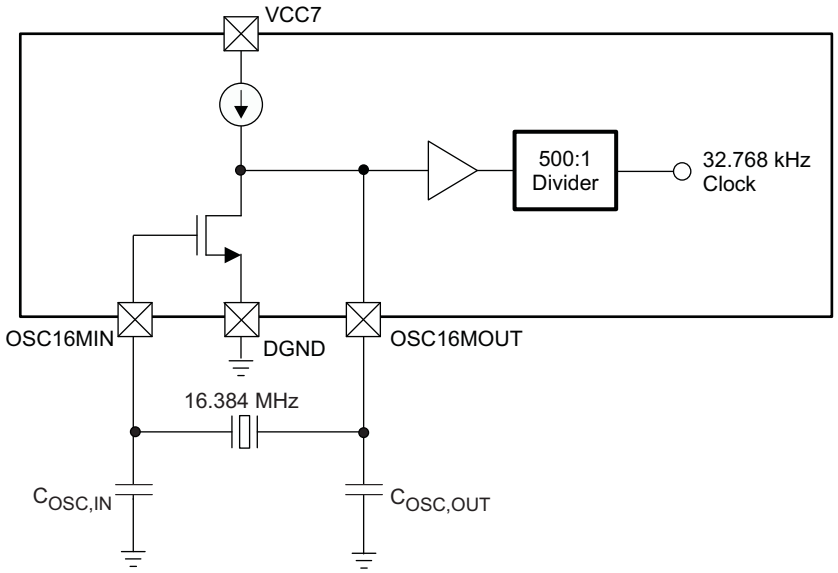

Figure 15. 16-MHz Crystal Oscillator

8.3.6 Real-Time Clock (RTC)

The RTC, which is driven by the 32-kHz clock, provides the alarm and timekeeping functions. The RTC remains supplied when the device is in the OFF or the BACKUP state.

The main functions of the RTC block are:

- Time information (seconds, minutes, and hours) directly in binary-coded decimal (BCD) format
- Calendar information (day, month, year, and day of the week) directly in BCD code up to year 2099
- Programmable interrupts generation
  - The RTC can generate two interrupts: a timer interrupt RTC_PERIOD_IT periodically (1-s, 1-m, 1-h, and 1-d period) and an alarm interrupt RTC_ALARM_IT at a precise time of the day (alarm function). These interrupts are enabled using IT_ALARM and IT_TIMER control bits. Periodically, interrupts can be masked during the SLEEP period to avoid host interruption and are automatically unmasked after SLEEP wakeup (using the IT_SLEEP_MASK_EN control bit).
- Oscillator frequency calibration and time correction

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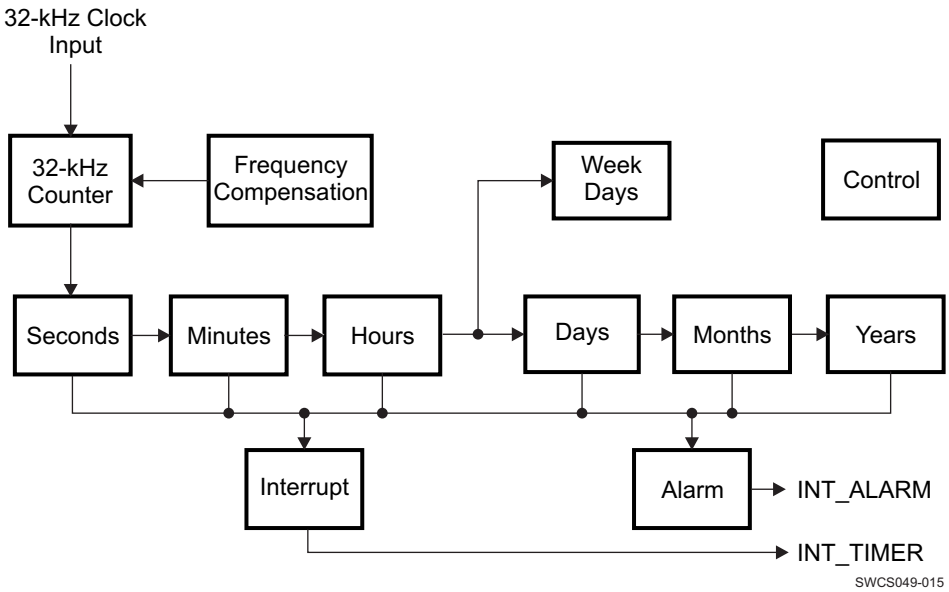

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Figure 16. RTC Digital Section Block Diagram

8.3.7 Thermal Monitoring and Shutdown

A thermal-protection module monitors the junction temperature of the device versus two thresholds:

- Hot-die temperature threshold
- Thermal-shutdown temperature threshold

When the hot-die temperature threshold is reached, an interrupt is sent to software to close the noncritical running tasks.

When the thermal-shutdown temperature threshold is reached, the TPS659119-Q1 device is set under reset and a transition to the OFF state initiates. Then the POWER-ON enable conditions of the device are not considered until the die temperature has decreased below the hot-die threshold. Hysteresis is applied to the hot-die and shutdown thresholds when detecting a falling edge of temperature and both detections are debounced to avoid any parasitic detection.

The TPS659119-Q1 device allows programming of four hot-die temperature thresholds to increase the flexibility of the system.

By default, the thermal protection is enabled in ACTIVE state, but can be disabled through programming the THERM_REG register. The thermal protection can be enabled in the SLEEP state programming the SLEEP_KEEP_RES_ON register. The thermal protection is automatically enabled during an OFF-to-ACTIVE state transition and is kept enabled in the OFF state after a switch-off sequence caused by a thermal shutdown event. A transition to the OFF-state sequence caused by thermal shutdown event is highlighted in Table 67 (the INT_STS_REG status register). Recovery from this OFF state is initiated (switch-on sequence) when the die temperature falls below the hot-die temperature threshold.

Hot-die and thermal shutdown temperature threshold detection states can be monitored or masked by reading or programming the THERM_REG register. Programming the INT_MSK_REG register can mask the hot-die interrupt.

8.3.8 Crystal Oscillator Power-On Reset

The crystal oscillator uses a local independent power-on-reset (POR) circuit. If the crystal oscillator or external clock input are used, then VCC7 must be higher than the rising threshold of this POR circuit (3.96 V max). If VCC7 is not higher than the rising POR threshold, a clock is not delivered to the digital core inside the PMIC and the device does not power up.

8.4 Device Functional Modes

8.4.1 Embedded Power Controller

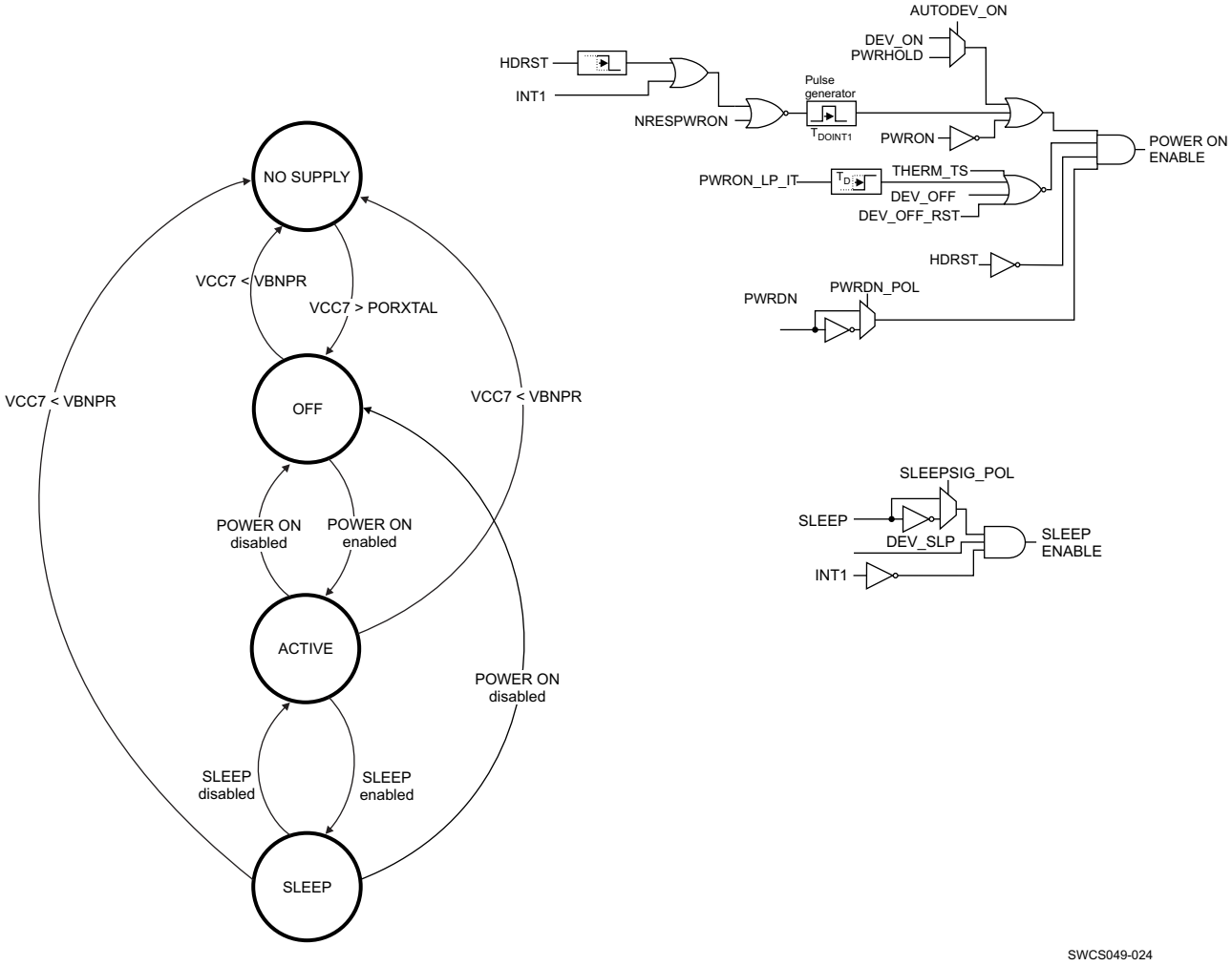
The embedded power controller (EPC) manages the state of the device and controls the power-up sequence.

8.4.1.1 State-Machine

The EPC supports the following states:

- **NO SUPPLY:** The main battery-supply voltage is not high enough to power the VRTC regulator. A global reset is asserted in this case. The device is turned off completely.
- **OFF:** The main battery-supply voltage is high enough to start the power-up sequence but device power-on is not enabled. All power supplies are in the OFF state except VRTC.
- **ACTIVE:** Device POWER-ON enable conditions are met and regulated power supplies are on or can be enabled with full current-capability.
- **SLEEP:** Device SLEEP-enable conditions are met and some selected regulated power supplies are in low-power mode.

Figure 17 shows the transitions for the state-machine.



NOTE: PWRHOLD enables power-on unless the pin is programmed as a GPI pin.

Figure 17. Embedded Power-Control State-Machine

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Device Functional Modes (continued)

8.4.1.1.1 Device POWER-ON Enable Conditions

The enable conditions of device POWER ON include the following:

- None of the device POWER-ON disable conditions are met.
- One of the following is met:
  - PWRON-signal low level
  - PWRHOLD signal high level
  - DEV_ON control bit set to 1 (default inactive)
  - Interrupt flag active (default INT1 low) generates a POWER ON enable condition during a fixed delay (t_{DOINT1} pulse duration defined in). Interrupt sources expected (if enabled), when the device is off:
    - RTC alarm interrupt

The active interrupt flag generates a POWER-ON enable-condition pulse of length t_{DOINT1} only when the device is in the OFF state (when the NRESPWRON signal is low). The POWER-ON enable-condition pulse occurs only if the interrupt status bit is initially low (no previous interrupt pending in the status register). The interrupt status register must first be cleared to allow device power off during the t_{DOINT1} pulse duration.

The GPIO2 signal cannot be used to turn on the device, even if the associated interrupt is not masked. The GPIO0, GPIO1, GPIO3, GPIO4, or GPIO5 signals can be used to turn on the device, if the associated interrupt is not masked.

NOTE

The watchdog interrupt is not a power-on event, but it wakes up the device from sleep mode.

8.4.1.1.2 Device POWER ON Disable Conditions

The disable conditions of device POWER ON include one of the following:

- PWRON signal low level during more than the long-press delay: PWON_LP_DELAY (can be disabled though register programming). The interrupt corresponding to this condition is PWRON_LP_IT in the INT_STS_REG register.
- The die temperature reaches the thermal-shutdown threshold (THERM_TS = 1).
- DEV_OFF or DEV_OFF_RST control bit is set to 1 (the DEV_OFF value is cleared when the device is in the OFF state).

NOTE

If the DEV_ON bit is set to 1, after switch-off, the device switches back on. To keep the device off, DEV_ON must be cleared first.

8.4.1.1.3 Device SLEEP Enable Conditions

The enable conditions of the device SLEEP state include all of the following:

- SLEEP-signal low level (default, or high level depending on the programmed polarity)
- DEV_SLP control bit is set to 1.
- Interrupt flag inactive (default INT1 high): no nonmasked interrupt is pending.

The SLEEP state is controlled by programming DEV_SLP and keeping the SLEEP signal floating. This state is also controlled through the SLEEP signal by setting the DEV_SLP bit to 1 one time after device turn-on.

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Device Functional Modes (continued)

8.4.1.1.4 Device Reset Scenarios

The device has three reset scenarios:

Full reset All digital logic of the device is reset.

Caused by POR (power on reset) when VCC7 < VBNPR

General reset No impact on the RTC, backup registers, or interrupt status.

Caused by one of the follwoing:

- PWON_LP_RST bit set high
- DEV_OFF_RST bit set high
- HDRST input set high

Turnoff Power reinitialization in off or backup mode.

Table 7 lists a mapping of the digital registers to these reset scenarios.

8.4.1.2 Boot Configuration and Switch-On and Switch-Off Sequences

The power sequence is the automated switch-on of the devices resources when an OFF-to-ACTIVE transition occurs. The power-on sequence has 15 sequential time slots to which resources (DCDCs, LDOs, 32-kHz clock, GPIO0, GPIO2, GPIO6, GPIO7) are assigned. The selected length of the time slot is either 0.5 ms or 2 ms. If a resource is not assigned to any time slot, the resource is in OFF mode after the power-on sequence and the voltage level can be changed through the register SEL bits before enabling the resource.

A power-off disables all power resources at the same time by default. By setting the PWR_OFF_SEQ control bit to 1, power-off follows the power-up sequence in reverse order (the first resource powered on is the last resource powered off).

The values of VDD1, VDD2, and EXTCTRL set in the boot sequence can be selected from 16 steps. For the whole range, 100-mV steps are available: 0.6 V and 0.7 to 1.4 V and 1.5 V. From 0.8 to 1.4 V, additional values with 50-mV step resolution can be set: 0.85 V and 1.05 V to 1.35 V.

For LDO1, LDO2, and LDO4 all levels from 1 to 3.3 V are selectable in the boot sequence with 50-mV steps. For other LDOs, the level is selectable with 100-mV steps, from 1 to 3.3 V.

The device supports two boot configurations, which define the power sequence and several device control bits. The boot configuration is selectable by the device BOOT1 pin.

BOOT1	Boot Configuration
0	Fixed boot mode
1	EEPROM boot mode

The BOOT1 input pad is disabled after the boot mode is read at power up, to save power.

Table 2 and Table 3 list the power sequence and general control bits defined in the boot sequence, respectively.

Fixed boot mode is the same in all orderable devices while EEPROM boot mode is different in each. Table 2 lists the boot configuration for power sequence control bits and Table 3 lists the boot configuration for general control bits. Refer to Table 4 for EEPROM boot-mode descriptions for specific orderable devices.

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Table 2. Boot Configuration: Power-Sequence Control Bits

REGISTER	BIT	DESCRIPTION	TPS659119-Q1	
			FIXED BOOT	EEPROM BOOT
VDD1_OP_REG/VDD1_SR_REG		EXTCTRL ratio selection for boot. Levels available: 0.6, 0.7, 0.8, 0.85, 0.9, 0.95 … 1.35, 1.4, and 1.5 V	1.2 V	x
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1	x
EEPROM		VDD1 time slot selection	3	x
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Enable skip	x
VDD2_OP_REG/VDD2_SR_REG		VDD2 voltage level selection for boot. Levels available: 0.6, 0.7, 0.8, 0.85, 0.9 … 0.95 to 1.35, 1.4, and 1.5 V	1.5 V	x
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1	x
EEPROM		VDD2 time slot selection	6	x
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Enable skip	x
VIO_REG	SEL[3:2]	VIO voltage selection	1.8 V	x
EEPROM		VIO time slot selection	4	x
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Enable skip	x
EXTCTRL_OP_REG/EXTCTRL_SR_REG		EXTCTRL voltage level selection for boot. Levels available include: SEL[6:0] = 3, 11, 19, 23, 27, … 59, 63, 67 Where: Ratio = 48 / (45 + SEL[6:0])	Off	x
EEPROM		EXTCTRL time slot selection	Off	x
LDO1_REG	SEL[7:2]	LDO1 voltage selection	1.05 V	x
EEPROM		LDO1 time slot	Off	x
LDO2_REG	SEL[7:2]	LDO2 voltage selection	1.2 V	x
EEPROM		LDO2 time slot	7	x
LDO3_REG	SEL[6:2]	LDO3 voltage selection	LDO3 voltage: 1 V	x
EEPROM		LDO3 time slot	Off	x
LDO4_REG	SEL[7:2]	LDO4 voltage selection	1.2 V	x
EEPROM		LDO4 time slot	2	x
LDO5_REG	SEL[6:2]	LDO5 voltage selection	LDO5 voltage: 1 V	x
EEPROM		LDO5 time slot	Off	x
LDO6_REG	SEL[6:2]	LDO6 voltage selection	LDO6 voltage: 1 V	x
EEPROM		LDO6 time slot	Off	x
LDO7_REG	SEL[6:2]	LDO7 voltage selection	1.2 V	x
EEPROM		LDO7 time slot	5	x
LDO8_REG	SEL[6:2]	LDO8 voltage selection	1 V	x

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Table 2. Boot Configuration: Power-Sequence Control Bits (continued)

REGISTER	BIT	DESCRIPTION	TPS659119-Q1	
			FIXED BOOT	EEPROM BOOT
EEPROM		LDO8 time slot	7	x
CLK32KOUT pin		CLK32KOUT time slot	5	x
NRESPWRON, NRESPWRON2 pin		NRESPWRON time slot	10	x
GPIO0 pin		GPIO0 time slot	1	x
GPIO2 pin		GPIO2 time slot	Off	x
GPIO6 pin		GPIO6 time slot	6	x
GPIO7 pin		GPIO7 time slot	5	x

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Table 3. Boot Configuration: General Control Bits

REGISTER	BIT	DESCRIPTION	TPS659119-Q1	
			FIXED BOOT	EEPROM BOOT
VRTC_REG	VRTC_OFFMASK	0: VRTC LDO is in low-power mode during OFF state. 1: VRTC LDO is in full-power mode during OFF state.	0	x
DEVCTRL_REG	CK32K_CTRL	0: Clock source is crystal / external clock. 1: Clock source is internal RC oscillator.	Crystal	x
DEVCTRL_REG	DEV_ON	0: No impact 1: Maintains device on, in ACTIVE or SLEEP state	0	x
DEVCTRL2_REG	TSLOTD	Boot sequence time slot duration: 0: 0.5 ms 1: 2 ms	2 ms	x
DEVCTRL2_REG	PWON_LP_OFF	0: Turn off device after PWRON long-press not allowed. 1: Turn off device after PWRON long-press.	1	x
DEVCTRL2_REG	PWON_LP_RST	0: No impact 1: Reset digital core when device is off	1	x
DEVCTRL2_REG	IT_POL	0: INT1 signal is active-low. 1: INT1 signal is active-high.	0	x
INT_MSK_REG	VMBHI_IT_MSK	0: Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition 1: Start-up reason required before switch-on	1	x
INT_MSK3_REG	GPIO5_F_IT_MSK	0: GPIO5 falling-edge detection interrupt not masked 1: GPIO5 falling-edge detection interrupt masked	1	x
INT_MSK3_REG	GPIO5_R_IT_MSK	0: GPIO5 rising-edge detection interrupt not masked 1: GPIO5 rising-edge detection interrupt masked	0	x
INT_MSK3_REG	GPIO4_F_IT_MSK	0: GPIO4 falling-edge detection interrupt not masked 1: GPIO4 falling-edge detection interrupt masked	1	x
INT_MSK3_REG	GPIO4_R_IT_MSK	0: GPIO4 rising-edge detection interrupt not masked 1: GPIO4 rising-edge detection interrupt masked	0	x
GPIO0_REG	GPIO_ODEN	0: GPIO0 configured as push-pull output 1: GPIO0 configured as open-drain output	Push-pull	x
WATCHDOG_REG	WATCHDOG_EN	0: Watchdog disabled 1: Watchdog enabled, periodic operation with 100 s	1	x
VMBCH_REG	VMBBUF_BYPASS	0: Enable input buffer for external resistive divider 1: In single-cell system, disable buffer for low lower	Disable buffer	x
BOOTSEQVER_REG	BOOTSEQVER_SEL	EEPROM boot sequence version number	0x20	x

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Table 3. Boot Configuration: General Control Bits (continued)

REGISTER	BIT	DESCRIPTION	TPS659119-Q1	
			FIXED BOOT	EEPROM BOOT
EEPROM	AUTODEV_ON	0: PWRHOLD pin is used as PWRHOLD feature. 1: PWRHOLD pin is GPI. After power on, DEV_ON set high internally, no processor action needed to maintain supplies.	1, PWRHOLD pin is GPI	x
EEPROM	PWRDN_POL	0: PWRDN signal is active-low. 1: PWRDN signal is active-high.	Active-low	x

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Table 4. EEPROM Configuration

BOOTSEQVER:	BOOTSEQVER_REG = 0x24	BOOTSEQVER_REG = 0x26	BOOTSEQVER_REG = 0x30	BOOTSEQVER_REG = 0x20	BOOTSEQVER_REG = 0x28	BOOTSEQVER_REG = 0x2A	BOOTSEQVER_REG = 0x22	BOOTSEQVER_REG = 0x1C	BOOTSEQVER_REG = 0x1A
ORDERABLE DEVICE NUMBER:	**TPS659119AIPFPRQ1**	**TPS659119CAIPFPRQ1**	**TPS659119BAIPFPRQ1**	**TPS659119DAIPFPRQ1**	**TPS659119EAIPFPRQ1**	**TPS659119FAIPFPRQ1**	**TPS659119HAIPFPRQ1**	**TPS659119KBIPFPRQ1**	**TPS659119LBIPFPRQ1**
VDD1_SLOT	Slot 15	Slot 12	Slot 11	OFF	Slot 15	Slot 15	OFF	Slot 15	OFF
VDD2_SLOT	Slot 8	Slot 4	Slot 12	Slot 8	Slot 8	Slot 8	Slot 8	Slot 8	Slot 8
VIO_SLOT	Slot 3	Slot 4	Slot 7	Slot 3	Slot 3	Slot 3	Slot 3	Slot 3	Slot 3
EXTCTRL_SLOT	Slot 1	Slot 3	Slot 10	Slot 1	Slot 1	Slot 1	Slot 1	Slot 1	Slot 1
VDIG1_SLOT (LDO1)	Slot 15	Slot 5	Slot 5	OFF	Slot 15	Slot 15	OFF	Slot 15	OFF
VDIG2_SLOT (LDO2)	Slot 6	Slot 5	Slot 4	Slot 5	Slot 6	Slot 6	Slot 6	Slot 6	Slot 6
VDAC_SLOT (LDO3)	OFF	Slot 2	Slot 6	OFF	OFF	Slot 3	OFF	Slot 3	OFF
VPLL_SLOT (LDO4)	OFF	Slot 5	Slot 4	Slot 1	OFF	Slot 1	Slot 1	Slot 1	Slot 1
VAUX1_SLOT (LDO5)	Slot 11	OFF	Slot 7	Slot 11	Slot 11	Slot 11	Slot 11	Slot 11	Slot 11
VMMC_SLOT (LDO6)	Slot 7	Slot 13	Slot 6	Slot 7	Slot 7	Slot 7	Slot 7	Slot 7	Slot 7
VAUX33_SLOT (LDO7)	Slot 12	Slot 6	Slot 8	Slot 12	Slot 12	Slot 12	Slot 12	Slot 12	Slot 12
VAUX2_SLOT (LDO8)	OFF	Slot 14	Slot 3	OFF	OFF	OFF	OFF	OFF	OFF
GPIO0_SLOT	Slot 5	Slot 1	Slot 9	Slot 6	Slot 5	Slot 5	Slot 5	Slot 5	Slot 5
GPIO2_SLOT	OFF	Slot 4	Slot 7	OFF	OFF	OFF	OFF	OFF	OFF
GPIO6_SLOT	OFF	Slot 10	Slot 12	OFF	OFF	OFF	Slot 15	OFF	Slot 15
GPIO7_SLOT	OFF	OFF	Slot 9	OFF	OFF	OFF	Slot 15	OFF	Slot 15
CLK32KOUT_SLOT	Slot 10	Slot 7	Slot 11	Slot 10	Slot 10	Slot 10	Slot 10	Slot 10	Slot 10
NRESPWRON_SLOT	Slot 14	Slot 10	Slot 14	Slot 14	Slot 14	Slot 14	Slot 14	Slot 14	Slot 14
VDD1_VSEL	1.05 V	1.05 V	1.2 V	1.05 V	1.05 V	1.05 V	1.05 V	1.05 V	1.05 V
VDD2_VSEL	1.5 V	1.5 V	1.2 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V	1.5 V
VIO_VSEL	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
EXTCTRL_VSEL (Ratio)	EXTCTRL Divider Ratio = 2/3	EXTCTRL Divider Ratio = 12/19	EXTCTRL Divider Ratio = 2/3	EXTCTRL Divider Ratio = 1/2	EXTCTRL Divider Ratio = 12/19	EXTCTRL Divider Ratio = 12/19	EXTCTRL Divider Ratio = 12/19	EXTCTRL Divider Ratio = 12/19	EXTCTRL Divider Ratio = 12/19
VDIG1_VSEL (LDO1)	1.05 V	1 V	1.8 V	1.05 V	1.05 V	1.05 V	1.05 V	1.05 V	1.05 V
VDIG2_VSEL (LDO2)	1.2 V	1.2 V	1.8 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V
VDAC_VSEL (LDO3)	1 V	1.2 V	3.3 V	1 V	1 V	1.8 V	1 V	1.8 V	1 V
VPLL_VSEL (LDO4)	0.8 V	1.8 V	1.8 V	1.25 V	0.8 V	1.2 V	1.2 V	1.2 V	1.2 V
VAUX1_VSEL (LDO5)	1 V	3.2 V	3.3 V	1 V	1 V	1 V	1 V	1 V	1 V
VMMC_VSEL (LDO6)	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
VAUX33_VSEL (LDO7)	2.8 V	2.8 V	3.3 V	2.8 V	2.8 V	2.8 V	2.8 V	2.8 V	2.8 V
VAUX2_VSEL (LDO8)	1 V	2.8 V	1.8 V	1 V	1 V	1 V	1 V	1 V	1 V
VDD1_GAINSEL	1×	1×	1×	1×	1×	1×	1×	1×	1×
VDD2_GAINSEL	1×	1×	1×	1×	1×	1×	1×	1×	1×
VDD1_PSKIP	VDD1 PFM mode enabled	VDD1 in PWM mode only	VDD1 in PWM mode only	VDD1 PFM mode enabled	VDD1 PFM mode enabled	VDD1 PFM mode enabled	VDD1 PFM mode enabled	VDD1 PFM mode enabled	VDD1 PFM mode enabled
VDD2_PSKIP	VDD2 PFM mode enabled	VDD2 in PWM mode only	VDD2 in PWM mode only	VDD2 PFM mode enabled	VDD2 PFM mode enabled	VDD2 PFM mode enabled	VDD2 PFM mode enabled	VDD2 PFM mode enabled	VDD2 PFM mode enabled

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Table 4. EEPROM Configuration (continued)

BOOTSEQVER:	BOOTSEQVER_REG = 0x24	BOOTSEQVER_REG = 0x26	BOOTSEQVER_REG = 0x30	BOOTSEQVER_REG = 0x20	BOOTSEQVER_REG = 0x28	BOOTSEQVER_REG = 0x2A	BOOTSEQVER_REG = 0x22	BOOTSEQVER_REG = 0x1C	BOOTSEQVER_REG = 0x1A
ORDERABLE DEVICE NUMBER:	**TPS659119AIPFPRQ1**	**TPS659119CAIPFPRQ1**	**TPS659119BAIPFPRQ1**	**TPS659119DAIPFPRQ1**	**TPS659119EAIPFPRQ1**	**TPS659119FAIPFPRQ1**	**TPS659119HAIPFPRQ1**	**TPS659119KBIPFPRQ1**	**TPS659119LBIPFPRQ1**
VIO_PSKIP	VIO PFM mode enabled	VIO in PWM mode only	VIO in PWM mode only	VIO PFM mode enabled	VIO PFM mode enabled	VIO PFM mode enabled	VIO PFM mode enabled	VIO PFM mode enabled	VIO PFM mode enabled
TSLOTD	0.5 ms	0.5 ms	2 ms	0.5 ms	0.5 ms	0.5 ms	0.5 ms	0.5 ms	0.5 ms
CLK32K_CTRL	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator	CLK32KOUT derived from XTAL oscillator
ITPOL	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low	INT1 output active-low
PWRDN_POL	PWRDN input active-low	PWRDN input active-low	PWRDN input active-high	PWRDN input active-low	PWRDN input active-low	PWRDN input active-low	PWRDN input active-low	PWRDN input active-low	PWRDN input active-low
WATCHDOG	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled	Watchdog disabled
PWRON_LP_RST	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF	Digital core reset when device is OFF
GPIO0_ODEN	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull	GPIO0 is push-pull
GPIO5_R_IT_MSK	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt masked	GPIO5 rising-edge interrupt masked	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt enabled	GPIO5 rising-edge interrupt enabled
GPIO5_F_IT_MSK	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked	GPIO5 falling-edge interrupt masked
GPIO4_R_IT_MSK	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt masked	GPIO4 rising-edge interrupt masked	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt enabled	GPIO4 rising-edge interrupt enabled
GPIO4_F_IT_MSK	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked	GPIO4 falling-edge interrupt masked
VMBHI_IT_MSK	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition	VCCS > VMBHI is NOT a power-on enable condition
VMBBUF_BYPASS	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled	VCCS buffer disabled
AUTO_DEVON	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on	PWRHOLD pin keeps PMIC on
PWRON_LP_OFF	PWRON long-press turnoff ENABLED	PWRON long-press turnoff DISABLED	PWRON long-press turnoff DISABLED	PWRON long-press turnoff ENABLED	PWRON long-press turnoff ENABLED	PWRON long-press turnoff ENABLED	PWRON long-press turnoff ENABLED	PWRON long-press turnoff ENABLED	PWRON long-press turnoff ENABLED
DEV_ON	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default	DEV_ON bit NOT set by default
VRTC_OFFMASK	VRTC in low-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in full-power mode during OFF state	VRTC in low-power mode during OFF state	VRTC in full-power mode during OFF state

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8.4.1.3 Control Signals

8.4.1.3.1 SLEEP

When none of the device SLEEP-disable conditions are met, a falling edge (default or rising edge, depending on the programmed polarity) of this signal causes an ACTIVE-to-SLEEP state transition of the device. A rising edge (default or falling edge, depending on the programmed polarity) causes a transition back to the ACTIVE state. This input signal is level-sensitive and no debouncing is applied.

While the device is in the SLEEP state, predefined resources are automatically set in the low-power mode or off. Resources can be kept in the active mode (full-load capability) by programming the SLEEP_KEEP_LDO_ON and the SLEEP_KEEP_RES_ON registers. These registers contain 1 bit per power resource. If the bit is set to 1, then that resource stays in active mode when the device is in the SLEEP state.

The CLK32KOUT pin is also included in the SLEEP_KEEP_RES_ON register and the 32-kHz clock output is maintained in the SLEEP state if the corresponding mask bit is set.

The status (low or high) of GPO0, GPO6, GPO7, and GPO8 is also controlled by the SLEEP signal, to allow enabling and disabling of external resources during sleep.

8.4.1.3.2 PWRHOLD

The PWRHOLD pin can be used as a PWRHOLD signal input or as a general purpose input (GPI). The mode is selected by the AUTODEV_ON bit, which is part of the boot configuration. When AUTODEV_MODE = 0, the PWRHOLD feature is selected.

Configured as PWRHOLD, when none of the device POWER ON disable conditions are met, a high level of this signal causes an OFF-to-ACTIVE state transition of the device and a low level causes a transition back to the OFF state.

This input signal is level-sensitive and no debouncing is applied. The rising edge, falling edge, or both of PWRHOLD is highlighted through an associated interrupt if interrupt is unmasked.

When AUTODEV_ON = 1, the pin is used as a GPI. As a GPI, this input can generate a maskable interrupt from a rising or falling edge of the input. When AUTODEV_ON = 1, a rising edge of NRESPWRON also automatically sets the DEV_ON bit to 1 to maintain supplies after the switch-on sequence, thus removing the need for the processor to set the PWRHOLD signal or the DEV_ON bit.

8.4.1.3.3 BOOT1

This signal determines with which processor the device is working and, hence, which power-up sequence is needed. For more details, see . There is no debouncing on this input signal.

8.4.1.3.4 NRESPWRON, NRESPWRON2

The NRESPWRON signal is used as the reset to the processor and is in the VDDIO domain. This signal is held low until the ACTIVE state is reached. For more details, see .

The NRESPWRON2 signal is a second reset output. This signal follows the state of NRESPWRON but has an open-drain output with external pullup. The supply for the external pullup must not be activated before the TPS659119-Q1 device is in control of the output state (that is, not earlier than during first power-up sequence slot). In off mode, the NRESPWRON2 output has a weak internal pulldown.

8.4.1.3.5 CLK32KOUT

This signal is the output of the 32-K oscillator, which can be enabled during the power-on sequence, depending on the boot mode. This signal is enabled and disabled by a register bit during the ACTIVE state of the device. The CLK32KOUT output can also be enabled during the SLEEP state of the device depending on the programming of the SLEEPMASK register.

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8.4.1.3.6 PWRON

The PWRON input is connected to an external button. If the device is in the OFF or SLEEP state, a debounced falling edge (PWRON input low for minimum of 100 µs) causes an OFF-to-ACTIVE state or a SLEEP-to-ACTIVE state transition of the device. If the device is in active mode, then a low level on this signal generates an interrupt. If the PWRON signal is low for more than the PWON_TO_OFF_DELAY delay and the corresponding interrupt is not acknowledged by the processor within 1 s, the device enters the OFF state. See Figure 2 and Figure 3 for PWRON behavior.

8.4.1.3.7 INT1

The INT1 signal (default active low) warns the host processor of any event that has occurred on the TPS659119-Q1 device. The host processor can then poll the interrupt from the interrupt status register through I^2C to identify the interrupt source. A low level (default setting) indicates an active interrupt, highlighted in the INT_STS_REG register. The polarity of INT1 can be set programming the IT_POL control bit. INT1 flag active is a POWER ON enable condition during a fixed delay, t_{DOINT1} (only), when the device is in the OFF state (when NRESPWRON is low).

Any of the interrupt sources can be masked programming the INT_MSK_REG register. When an interrupt is masked its corresponding interrupt status bit is still updated, but the INT1 flag is not activated. Interrupt source masking can be used to mask a device switch-on event. Because interrupt flag active is a POWER ON enable condition, during t_{DOINT1} delay, any interrupt not masked must be cleared to allow immediate turn off of the device.

For a description of interrupt sources, see Table 6.

8.4.1.3.8 EN2 and EN1

EN2 and EN1 are the data and clock signals of the serial-control interface dedicated to voltage-scaling applications.

These signals can also be programmed as enable signals of one or several supplies when the device is on (NRESPWRON high). A resource assigned to EN2 or EN1 control automatically disables the serial control interface.

For the EN1_LDO_ASS_REG, EN2_LDO_REG, and SLEEP_KEEP_LDO_ON_REG registers, the EN1 and EN2 signals can be used to control the ACTIVE or SLEEP state of any LDO-type supplies.

For the EN1_SMPS_ASS_REG, EN2_SMPS_ASS_REG, and SLEEP_KEEP_RES_ON registers, the EN1 and EN2 signals can be used to control the ACTIVE or LOW-POWER state (PFM mode) of SMPS-type supplies.

The EN2 and EN1 signals can set the output voltage of the VDD1 and VDD2 SMPS from a roof to a floor value, preprogrammed in the VDD1_OP_REG, VDD2_OP_REG and VDD1_SR_REG, VDD2_SR_REG registers.

When a supply is controlled through the EN1 or EN2 signals, the state of the supply is no longer driven by the device SLEEP state.

8.4.1.3.9 GPIO0–8

GPIO0, GPIO2, and GPIO6–7 can be programmed as part of the power-up sequence and used as enable signals for external resources.

GPIO0 is a configurable I/O in the VCC7 domain. By default, the output of GPIO0 is push-pull, driving low. GPIO0 can also be configured as an open-drain output with an external pullup.

GPIO1 through GPIO8 are configurable open-drain digital I/Os in the VRTC domain. GPIO directivity, debouncing delay, and internal pullup can be programmed. By default, all are inputs with weak internal pulldown because open-drain output an external pullup is required.

GPIO0–1 and GPIO3–5 can turn on the device if the corresponding interrupt is not masked. When configured as an input, GPIO2 cannot be used to turn on the device, even if the associated interrupt is not masked. The GPIO interrupt is level sensitive. When an interrupt is detected, before clearing the interrupt, it should first be disabled by masking it.

GPIO1 and GPIO3 have a current-sink capability of 10 mA, and can also drive LEDs connected to a 5-V supply.

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GPIO2 can be used for synchronizing DCDCs to an external clock. Programming DCDCCKEXT = 1, VDD1, VDD2, and VIO DC-DC switching can be synchronized using a 3-MHz clock set though the GPIO2 pin. VDD1 and VDD2 are in-phase and VIO is phase shifted by 180 degrees.

Not connecting noisy switching signals to GPIO4 and GPIO5 is recommended.

8.4.1.3.10 HDRST Input

HDRST is a cold reset input for the PMIC. A high level at the input forces the TPS659119-Q1 into off mode, causing a general reset of the device to the default settings. The default state is defined by the register reset state and boot configuration. An HDRST high level keeps the device in off mode. When reset is released and HDRST input goes low, the device automatically transitions to active mode. The device is kept in active mode for the period t_{DONIT1}, after which another power-on enable reason is required to keep the device on.

The HDRST input is in the VRTC domain and has a weak internal pulldown which is active by default.

8.4.1.3.11 PWRDN

The PWRDN input is a reset input with selectable polarity (PWRDN_POL). A high level with active-low polarity at the input forces the TPS659119-Q1 device into off mode, causing a power-off reset. Off mode is maintained until PWRDN is released and a start-up reason is detected such as a PWRON button press or DEV_ON = 1. An interrupt is generated to indicate the cause for shutdown. The PWRDN input is in the VRTC domain, but can tolerate a 5-V input.

8.4.1.3.12 Watchdog

The watchdog has two modes of operation.

In periodic operation an interrupt is generated with a regular period defined by the WTCHDG_TIME setting. The IC initiates WTCHDOG shutdown if the interrupt is not cleared within the period. The watchdog interrupt WTCHDOG counter is reinitialized when NRESPWRON is low.

In interrupt mode the IC initiates WTCHDOG counter when an interrupt is pending and is cleared when the interrupt is acknowledged. If the interrupt is not cleared before watchdog expiration within WTCHDG_TIME, the device enters off mode.

By default, periodic watchdog functionality is enabled with the maximum WTCHDG_TIME period.

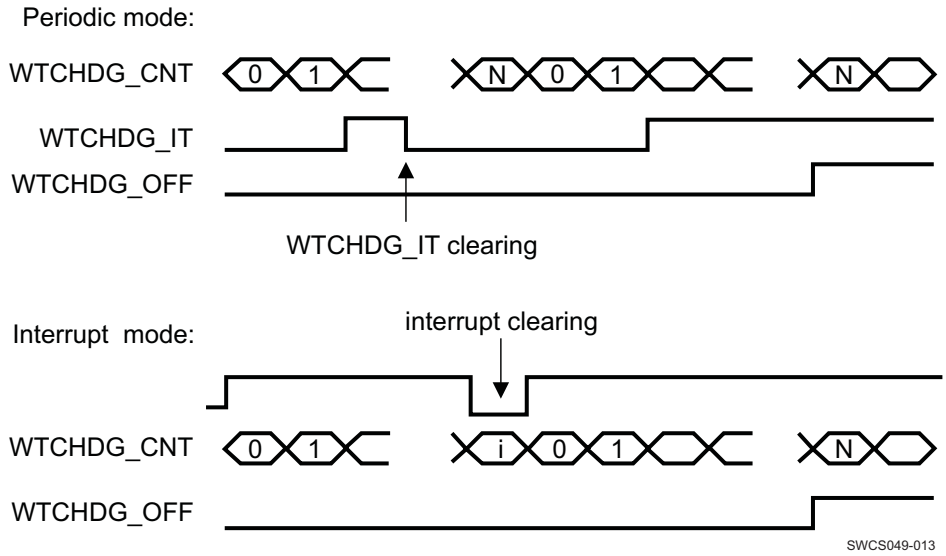

Figure 18. Watchdog Signals

8.4.1.3.13 Tracking LDO

LDO4 has an optional mode where the output level follows that of VDD1, from 0.6 to 1.5 V, when VDD1 is active. When VDD1 is set to off, the LDO4 output is defined by the SEL[7:2] bits in LDO4_REG, and can be set from 0.8 to 1.5 V.

Tracking mode is enabled by setting TRACK = 1 in DCDCCTRL_REG. In initial activation, VDD1 must be enabled and allowed to settle before enabling tracking mode. After initial activation, tracking mode can remain enabled while VDD1 is turned off. The value of TRACK is set to the default (0) after any turnoff event.

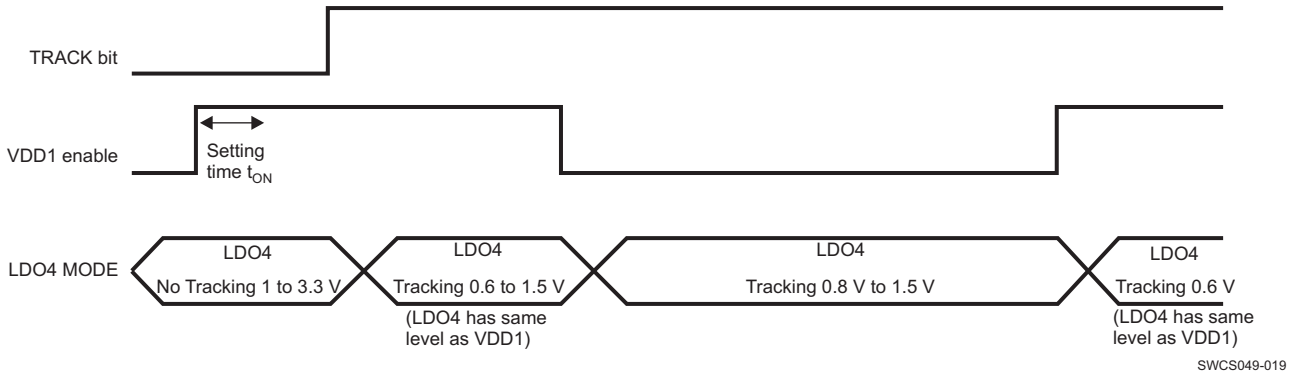

Figure 19. Tracking LDO

8.5 Programming

8.5.1 Time-Calendar Registers

All time and calendar information is available in these dedicated registers, called TC registers. Values of the TC registers are written in BCD format.

1. Year data ranges from 00 to 99
   - Leap year = year divisible by four (2000, 2004, 2008, 2012, and so on)
   - Common year = other years
2. Month data ranges from 1 to 12
3. Day data ranges from the following:
   - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
   - 1 to 30 when months are 4, 6, 9, 11
   - 1 to 29 when month is 2 and year is a leap year
   - 1 to 28 when month is 2 and year is a common year
4. Week data ranges from 0 to 6
5. Hour data ranges from 00 to 23 in 24-hour mode and ranges from 1 to 12 in AM/PM mode
6. Minute data ranges from 0 to 59
7. Second data ranges from 0 to 59

To modify the current time, software writes the new time into TC registers to fix the time-calendar information. The processor can write to the TC registers without stopping the RTC. In addition, software can stop the RTC by clearing the STOP_RTC bit of the control register, checking the RUN bit of the status to ensure that the RTC is frozen, updating the TC values, and restarting the RTC by setting STOP_RTC bit. An example follows.

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Programming (continued)

Table 5 lists the previous register values for the following example:

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5

Table 5. Real-Time Clock Registers Example

REGISTER	VALUE
SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x90
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x08

The user can round to the closest minute by setting the ROUND_30S register bit. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed. Two examples follow:

- If the current time is 10H59M45S, a round operation changes time to 11H00M00S.
- if the current time is 10H59M29S, a round operation changes time to 10H59M00S.

8.5.2 General Registers

Software can access the RTC_STATUS_REG and RTC_CTRL_REG registers at any time. The only exception is that software cannot access the RTC_CTRL_REG[5] bit which must be changed only when the RTC is stopped.

8.5.3 Compensation Registers

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers must be updated before each compensation process. For example, software can load the compensation value into these registers after each hour event during an available access period.

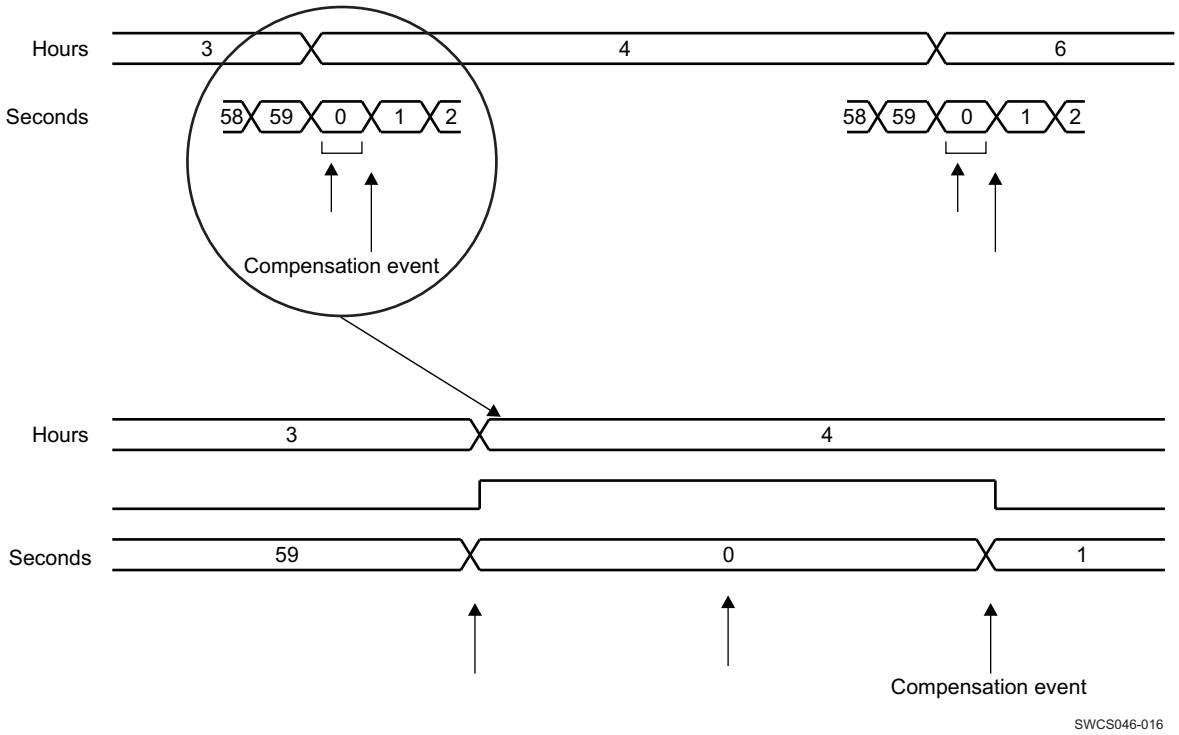

Figure 20. RTC Compensation Scheduling

This drift can be balanced to compensate for any inaccuracy of the 32-kHz oscillator. Software must calibrate the oscillator frequency, calculate the drift compensation versus 1-h time period, and load the compensation registers with the drift compensation value. If the AUTO_COMP_EN bit in the RTC_CTRL_REG is enabled, the value of COMP_REG (in twos-complement) is added to the RTC 32-kHz counter at the first second of each hour. When COMP_REG is added to the RTC 32-kHz counter, the duration of the current second becomes (32768 – COMP_REG) / 32768 s; so, the RTC can be compensated with a 1 / 32768 s/hour time unit accuracy.

NOTE

The compensation is considered when written into the registers.

8.5.4 Backup Registers

As part of the RTC, the device contains five 8-bit registers that can be used for storage by the application firmware when the external host is powered down. These registers retain the content as long as the VRTC is active.

8.5.5 I²C Interface

A general-purpose serial-control interface (CTL-I²C) allows read and write access to the configuration registers of all resources of the system.

A second serial-control interface (optional mode for EN1 and EN2 pins) can be dedicated to DVFS.

Both control interfaces are compliant with the HS-I²C specification.

These interfaces support the standard slave mode (100 Kbps), fast mode (400 Kbps), and high-speed mode (3.4 Mbps). The general-purpose I²C module using one slave hard-coded address (ID1 = 2Dh). The voltage scaling dedicated I²C module uses one slave hardcoded address (ID0 = 12h). The master mode is not supported.

8.5.5.1 Addressing

The device supports seven-bit mode addressing.

It does not support the following features:

- 10-bit addressing
- General call

8.5.5.2 Access Protocols

Access protocols or compatibility, the I²C interfaces in the TPS659119-Q1 device use the same read and write protocol as other TI power ICs, based on an internal register size of 8 bits. Supported transactions are described below.

8.5.5.2.1 Single-Byte Access

A write access is initiated by a first byte including the address of the device (7 MSBs) and a write command (LSB), a second byte provides the address (8 bits) of the internal register, and the third byte represents the data to be written in the internal register (see Figure 21).

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the address (8 bits) of the internal register
- A third byte, including again the device address (7 MSBs) and the read command (LSB)

The device replies by sending a fourth byte which represents the content of the internal register (see Figure 22).

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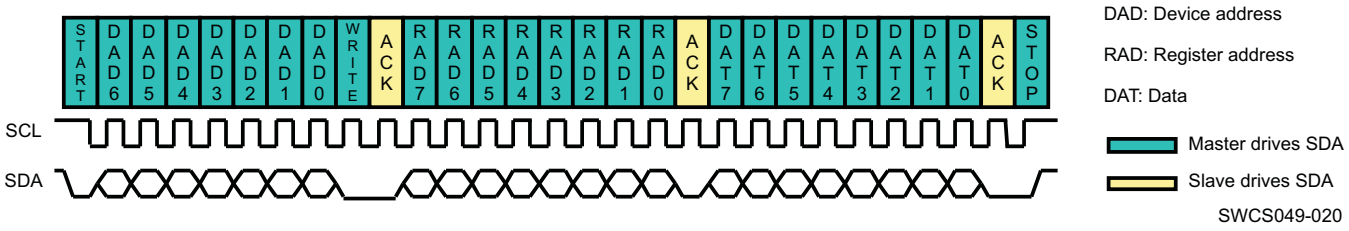

Figure 21. I²C Write-Access Single Byte

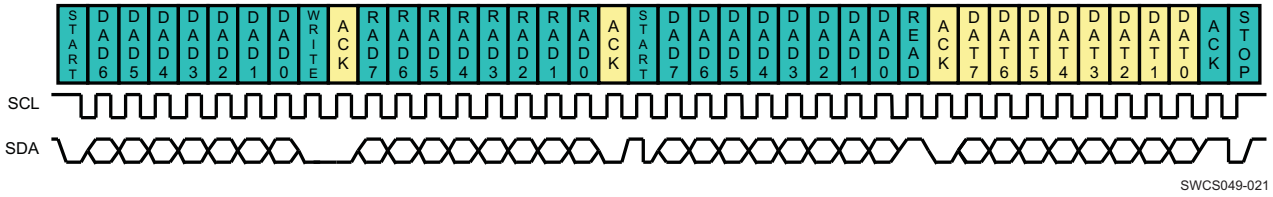

Figure 22. I²C Read-Access Single Byte

8.5.5.2.2 Multiple-Byte Access To Several Adjacent Registers

A write access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal registers

The following N bytes represent the data to be written in the internal register starting at the base address and incremented by one at each data byte (see Figure 23).

A read access is initiated by:

- A first byte, including the address of the device (7 MSBs) and a write command (LSB)
- A second byte, providing the base address (8 bits) of the internal register
- A third byte, including again the device address (7 MSBs) and the read command (LSB)

The device replies by sending a fourth byte, which represents the content of the internal registers, starting at the base address and next consecutive ones (see Figure 24).

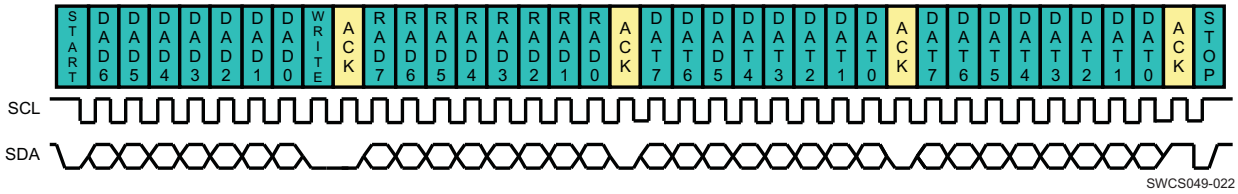

Figure 23. I²C Write-Access Multiple Bytes

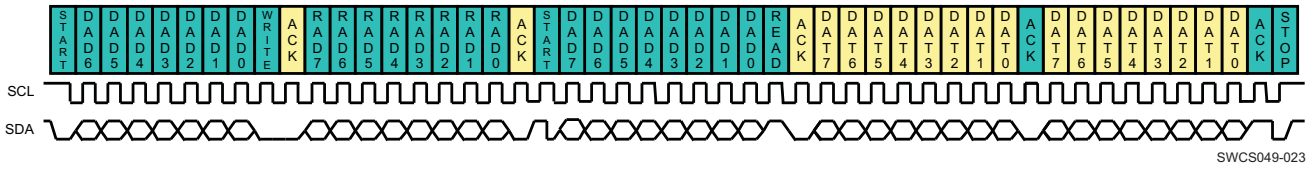

Figure 24. I²C Read-Access Multiple Bytes

8.5.6 Interrupts

Table 6. Interrupt Sources

INTERRUPT	DESCRIPTION
RTC_ALARM_IT	RTC alarm event: Occurs at programmed determinate date and time (running in ACTIVE, OFF, and SLEEP state, default inactive)
RTC_PERIOD_IT	RTC periodic event: Occurs at programmed regular period of time (every second or minute) (running in ACTIVE, OFF, and SLEEP state, default inactive)
HOT_DIE_IT	The embedded thermal monitoring module detects a die temperature above the hot-die detection threshold (running in ACTIVE and SLEEP state). Level sensitive interrupt.
PWRHOLD_R_IT	PWRHOLD signal rising edge
PWRHOLD_F_IT	PWRHOLD signal falling-edge
PWRON_LP_IT	PWRON is low during more than the long-press delay: PWON_TO_OFF_DELAY (can be disable though register programming).
PWRON_IT	PWRON is low while the device is on (running in ACTIVE and SLEEP state). Level-sensitive interrupt.
GPIO0_R_IT	GPIO_CKSYNC rising-edge detection
GPIO0_F_IT	GPIO_CKSYNC falling-edge detection
GPIO1_R_IT	GPIO1 rising-edge detection
GPIO1_F_IT	GPIO1 falling-edge detection
GPIO2_R_IT	GPIO2 rising-edge detection
GPIO2_F_IT	GPIO2 falling-edge detection
GPIO3_R_IT	GPIO3 rising-edge detection
GPIO3_F_IT	GPIO3 falling-edge detection
GPIO4_R_IT	GPIO4 rising-edge detection
GPIO4_F_IT	GPIO4 falling-edge detection
GPIO5_R_IT	GPIO5 rising-edge detection
GPIO5_F_IT	GPIO5 falling-edge detection
WTCHDG_IT	Watchdog interrupt
PWRDN_IT	PWRDN reset interrupt

8.6 Register Maps

8.6.1 Functional Registers

The possible device reset domains are:

- Full reset: All digital of device is reset.
  - Caused by Power On Reset (POR) when VCCS < VBNPR
- General reset: No impact on RTC, backup registers or interrupt status.
  - Caused by PWON_LP_RST bit set high or
  - DEV_OFF_RST bit set high or
  - HDRST input set high
- Turnoff OFF: Power reinitialization in off or backup mode.

In following register description, reset domain for each register is defined at the register table heading.

NOTE

The DCDCCTRL_REG and DEVCTRL2_REG have bits in two reset domains.

The comment, *Default value: See boot configuration*, indicates that the default value of the bit is set in boot configuration and not by register reset value.

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Register Maps (continued)

8.6.2 TPS659119-Q1_FUNC_REG Register Mapping Summary

Table 7. TPS659119-Q1_FUNC_REG Register Summary(1)

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	REGISTER RESET	ADDRESS OFFSET
SECONDS_REG	RW	8	0x00	0x00
MINUTES_REG	RW	8	0x00	0x01
HOURS_REG	RW	8	0x00	0x02
DAYS_REG	RW	8	0x01	0x03
MONTHS_REG	RW	8	0x01	0x04
YEARS_REG	RW	8	0x00	0x05
WEEKS_REG	RW	8	0x00	0x06
ALARM_SECONDS_REG	RW	8	0x00	0x08
ALARM_MINUTES_REG	RW	8	0x00	0x09
ALARM_HOURS_REG	RW	8	0x00	0x0A
ALARM_DAYS_REG	RW	8	0x01	0x0B
ALARM_MONTHS_REG	RW	8	0x01	0x0C
ALARM_YEARS_REG	RW	8	0x00	0x0D
RTC_CTRL_REG	RW	8	0x00	0x10
RTC_STATUS_REG	RW	8	0x80	0x11
RTC_INTERRUPTS_REG	RW	8	0x00	0x12
RTC_COMP_LSB_REG	RW	8	0x00	0x13
RTC_COMP_MSB_REG	RW	8	0x00	0x14
RTC_RES_PROG_REG	RW	8	0x27	0x15
RTC_RESET_STATUS_REG	RW	8	0x00	0x16
BCK1_REG	RW	8	0x00	0x17
BCK2_REG	RW	8	0x00	0x18
BCK3_REG	RW	8	0x00	0x19
BCK4_REG	RW	8	0x00	0x1A
BCK5_REG	RW	8	0x00	0x1B
PUADEN_REG	RW	8	0x1F	0x1C
REF_REG	RO	8	0x01	0x1D
VRTC_REG	RW	8	0x01	0x1E
VIO_REG	RW	8	0x05	0x20
VDD1_REG	RW	8	0x0D	0x21
VDD1_OP_REG	RW	8	0x33	0x22
VDD1_SR_REG	RW	8	0x33	0x23
VDD2_REG	RW	8	0x0D	0x24
VDD2_OP_REG	RW	8	0x4B	0x25
VDD2_SR_REG	RW	8	0x4B	0x26
EXTCTRL_REG	RW	8	0x00	0x27
EXTCTRL_OP_REG	RW	8	0x03	0x28
EXTCTRL_SR_REG	RW	8	0x03	0x29
LDO1_REG	RW	8	0x15	0x30
LDO2_REG	RW	8	0x15	0x31
LDO5_REG	RW	8	0x00	0x32
LDO8_REG	RW	8	0x09	0x33
LDO7_REG	RW	8	0x0D	0x34

(1) Register reset values are for fixed boot mode.

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Register Maps (continued)

Table 7. TPS659119-Q1_FUNC_REG Register Summary(1) (continued)

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	REGISTER RESET	ADDRESS OFFSET
LDO6_REG	RW	8	0x21	0x35
LDO4_REG	RW	8	0x00	0x36
LD03_REG	RW	8	0x00	0x37
THERM_REG	RW	8	0x0D	0x38
BBCH_REG	RW	8	0x00	0x39
DCDCCTRL_REG	RW	8	0x39	0x3E
DEVCTRL_REG	RW	8	0x0000 0014	0x3F
DEVCTRL2_REG	RW	8	0x0000 0036	0x40
SLEEP_KEEP_LDO_ON_REG	RW	8	0x00	0x41
SLEEP_KEEP_RES_ON_REG	RW	8	0x00	0x42
SLEEP_SET_LDO_OFF_REG	RW	8	0x00	0x43
SLEEP_SET_RES_OFF_REG	RW	8	0x00	0x44
EN1_LDO_ASS_REG	RW	8	0x00	0x45
EN1_SMPS_ASS_REG	RW	8	0x00	0x46
EN2_LDO_ASS_REG	RW	8	0x00	0x47
EN2_SMPS_ASS_REG	RW	8	0x00	0x48
INT_STS_REG	RW	8	0x06	0x50
INT_MSK_REG	RW	8	0xFF	0x51
INT_STS2_REG	RW	8	0xA8	0x52
INT_MSK2_REG	RW	8	0xFF	0x53
INT_STS3_REG	RW	8	0x5A	0x54
INT_MSK3_REG	RW	8	0xFF	0x55
GPIO0_REG	RW	8	0x07	0x60
GPIO1_REG	RW	8	0x08	0x61
GPIO2_REG	RW	8	0x08	0x62
GPIO3_REG	RW	8	0x08	0x63
GPIO4_REG	RW	8	0x08	0x64
GPIO5_REG	RW	8	0x08	0x65
GPIO6_REG	RW	8	0x05	0x66
GPIO7_REG	RW	8	0x05	0x67
GPIO8_REG	RW	8	0x08	0x68
WATCHDOG_REG	RW	8	0x07	0x69
BOOTSEQVER_REG	RW	8	0x1E	0x6A
VMBCH2_REG	RW	8	0x00	0x6B
LED_CTRL1_REG	RW	8	0x00	0x6C
LED_CTRL2_REG1	RW	8	0x00	0x6D
PWM_CTRL1_REG	RW	8	0x00	0x6E
PWM_CTRL2_REG	RW	8	0x00	0x6F
SPARE_REG	RW	8	0x00	0x70
VERNUM_REG	RO	8	0x00	0x80

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8.6.3 TPS659119-Q1_FUNC_REG Register Descriptions

Table 8. SECONDS_REG

Address Offset	0x00		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for seconds		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEC1			SEC0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	SEC1	Second digit of seconds (range is 0 up to 5)	RW	0x0
3:0	SEC0	First digit of seconds (range is 0 up to 9)	RW	0x0

Table 9. MINUTES_REG

Address Offset	0x01		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for minutes		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	MIN1	Second digit of minutes (range is 0 up to 5)	RW	0x0
3:0	MIN0	First digit of minutes (range is 0 up to 9)	RW	0x0

Table 10. HOURS_REG

Address Offset	0x02		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for hours		
Type	RW		

7	6	5	4	3	2	1	0
PM_NAM	Reserved	HOUR1		HOUR0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	PM_NAM	Only used in PM_AM mode (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	HOUR1	Second digit of hours(range is 0 up to 2)	RW	0x0
3:0	HOUR0	First digit of hours (range is 0 up to 9)	RW	0x0

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Table 11. DAYS_REG

Address Offset	0x03		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for days		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:4	DAY1	Second digit of days (range is 0 up to 3)	RW	0x0
3:0	DAY0	First digit of days (range is 0 up to 9)	RW	0x1

Table 12. MONTHS_REG

Address Offset	0x04		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for months		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	MONTH1	Second digit of months (range is 0 up to 1)	RW	0
3:0	MONTH0	First digit of months (range is 0 up to 9)	RW	0x1

Table 13. YEARS_REG

Address Offset	0x05		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for day of the week		
Type	RW		

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:4	YEAR1	Second digit of years (range is 0 up to 9)	RW	0x0
3:0	YEAR0	First digit of years (range is 0 up to 9)	RW	0x0

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Table 14. WEEKS_REG

Address Offset	0x06		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for day of the week		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						WEEK	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2:0	WEEK	First digit of day of the week (range is 0 up to 6)	RW	0

Table 15. ALARM_SECONDS_REG

Address Offset	0x08		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming seconds in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1			ALARM_SEC0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_SEC1	Second digit for programming seconds in the alarm setting (range is 0 up to 5)	RW	0x0
3:0	ALARM_SEC0	First digit for programming seconds in the alarm setting (range is 0 up to 9)	RW	0x0

Table 16. ALARM_MINUTES_REG

Address Offset	0x09		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming minutes in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_MIN1			ALARM_MIN0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_MIN1	Second digit for programming minutes in the alarm setting (range is 0 up to 5)	RW	0x0
3:0	ALARM_MIN0	First digit for programming minutes in the alarm setting (range is 0 up to 9)	RW	0x0

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Table 17. ALARM_HOURS_REG

Address Offset	0x0A		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming hours in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_PM_NAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	ALARM_PM_NAM	Only used in PM_AM mode for programming the AM/PM in the alarm setting (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	ALARM_HOUR1	Second digit for programming hours in the alarm setting (range is 0 up to 2)	RW	0x0
3:0	ALARM_HOUR0	First digit for programming hours in the alarm setting (range is 0 up to 9)	RW	0x0

Table 18. ALARM_DAYS_REG

Address Offset	0x0B		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming days in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved	Reserved bit	RO R Special	0x0
5:4	ALARM_DAY1	Second digit for programming days in the alarm setting (range is 0 up to 3)	RW	0x0
3:0	ALARM_DAY0	First digit for programming days in the alarm setting (range is 0 up to 9)	RW	0x1

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Table 19. ALARM_MONTHS_REG

Address Offset	0x0C		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming months in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	ALARM_MONTH1	Second digit for programming months in the alarm setting(range is 0 up to 1)	RW	0
3:0	ALARM_MONTH0	First digit for programming months in the alarm setting(range is 0 up to 9)	RW	0x1

Table 20. ALARM_YEARS_REG

Address Offset	0x0D		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for programming years in the alarm setting		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:4	ALARM_YEAR1	Second digit for programming years in the alarm setting (range is 0 up to 9)	RW	0x0
3:0	ALARM_YEAR0	First digit for programming years in the alarm setting (range is 0 up to 9)	RW	0x0

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Table 21. RTC_CTRL_REG

Address Offset	0x10		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC control register: **Note**: A dummy read of this register is necessary before each I^2C read in order to update the ROUND_30S bit value.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	RTC_V_OPT	RTC date and time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG) 1: Read access to static shadowed registers: (see GET_TIME bit).	RW	0
6	GET_TIME	When writing a 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG and WEEKS_REG) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (In effect: reset it to 0 and then re-write it to 1)	RW	0
5	SET_32_COUNTER	0: No action 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.	RW	0
4	TEST_MODE	0: functional mode 1: test mode (Auto compensation is enable when the 32-kHz counter reaches at the end of the counter)	RW	0
3	MODE_12_24	0: 24-hours mode 1: 12-hours mode (PM-AM mode) Switching between the two modes at any time without disturbing the RTC is possible. Read or write are always performed with the current mode.	RW	0
2	AUTO_COMP	0: No auto compensation 1: Auto compensation enabled	RW	0
1	ROUND_30S	0: No update 1: When a one is written, the time is rounded to the closest minute. This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller reads one until the rounded to the closet.	RW	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	RW	0

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Table 22. RTC_STATUS_REG

Address Offset	0x11		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC status register: **Note**: A dummy read of this register is necessary before each I^2C read in order to update the status register value.		
Type	RW		

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	Reserved

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	POWER_UP	Indicates that a reset occurred (bit cleared to 0 by writing 1). POWER_UP is set by a reset, is cleared by writing one in this bit.	RW	1
6	ALARM	Indicates that an alarm interrupt is generated (bit clear by writing 1). The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS_REG register. The timer interrupt is a low-level pulse (15 µs duration).	RW	0
5	EVENT_1D	One day has occurred	RO	0
4	EVENT_1H	One hour has occurred	RO	0
3	EVENT_1M	One minute has occurred	RO	0
2	EVENT_1S	One second has occurred	RO	0
1	RUN	0: RTC is frozen 1: RTC is running This bit shows the real state of the RTC, because STOP_RTC signal was resynchronized on 32-kHz clock, the action of this bit is delayed.	RO	0
0	Reserved	Reserved bit	RO R returns 0s	0

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Table 23. RTC_INTERRUPTS_REG

Address Offset	0x12		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC interrupt-control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	IT_SLEEP_MASK_EN	1: Mask periodic interrupt while the TPS659119-Q1 device is in SLEEP mode. The interrupt event is back up in a register and occurs as soon as the TPS659119-Q1 device is no longer in SLEEP mode. 0: Normal mode, no interrupt masked	RW	0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers	RW	0
2	IT_TIMER	Enable periodic interrupt 0: interrupt disabled 1: interrupt enabled	RW	0
1:0	EVERY	Interrupt period 00: every second 01: every minute 10: every hour 11: every day	RW	0x0

Table 24. RTC_COMP_LSB_REG

Address Offset	0x13		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC compensation register (LSB) **Note**: This register must be written in twos-complement. Which means that to add one 32-kHz oscillator period every hour, the microcontroller muse write FFFF into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. To remove one 32-kHz oscillator period every hour, the microcontroller needs to write 0001 into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. The 7FFF value is forbidden.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	RTC_COMP_LSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]	RW	0x00

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Table 25. RTC_COMP_MSB_REG

Address Offset	0x14		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC compensation register (MSB) Notes: See RTC_COMP_LSB_REG Notes.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	RTC_COMP_MSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]	RW	0x00

Table 26. RTC_RES_PROG_REG

Address Offset	0x15		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register containing oscillator resistance value		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		SW_RES_PROG					

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:0	SW_RES_PROG	Value of the oscillator resistance	RW	0x27

Table 27. RTC_RESET_STATUS_REG

Address Offset	0x16		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	RTC register for reset status		
Type	RW		

7	6	5	4	3	2	1	0
Reserved							RESET_STATUS

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:1	Reserved	Reserved bit	RO R returns 0s	0x0
0	RESET_STATUS	This bit can only be set to one and is cleared when a manual reset or a POR (VBAT < 2.1) occur. If this bit is reset the RTC lost its configuration.	RW	0

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Table 28. BCK1_REG

Address Offset	0x17		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers retain content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	BCKUP	Backup bit	RW	0x00

Table 29. BCK2_REG

Address Offset	0x18		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers retain content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	BCKUP	Backup bit	RW	0x00

Table 30. BCK3_REG

Address Offset	0x19		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers retain content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	BCKUP	Backup bit	RW	0x00

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Table 31. BCK4_REG

Address Offset	0x1A		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers retain content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	BCKUP	Backup bit	RW	0x00

Table 32. BCK5_REG

Address Offset	0x1B		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers retain content as long as the VRTC is active.		
Type	RW		

7	6	5	4	3	2	1	0
BCKUP							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	BCKUP	Backup bit	RW	0x00

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Table 33. PUADEN_REG

Address Offset	0x1C		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Pullup and pulldown control register.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	I2CCTLP	I2CSRP	PWRONP	SLEEPP	PWRHOLDP	HDRSTP	NRESPWRON2P

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO	0
6	I2CCTLP	SDACTL and SCLCTL pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	0
5	I2CSRP	SDASR and SCLSR pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	0
4	PWRONP	PWRON-pad pullup control: 1: Pullup is enabled 0: Pullup is disabled	RW	1
3	SLEEPP	SLEEP-pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	PWRHOLDP	PWRHOLD-pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
1	HDRSTP	HDRST-pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
0	NRESPWRON2P	NRESPWRON2 pad control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1

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Table 34. REF_REG

Address Offset	0x1D		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	Reference control register		
Type	RO		

7	6	5	4	3	2	1	0
Reserved						ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	ST	Reference state: ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Reserved ST[1:0] = 11: On low power (SLEEP) (Write access available in test mode only)	RO	0x1

Table 35. VRTC_REG

Address Offset	0x1E		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	VRTC internal regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				VRTC_OFFMASK	Reserved	ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3	VRTC_OFFMASK	VRTC internal regulator off mask signal: When set to 1, the regulator keeps its full-load capability during device OFF state. When set to 0, the regulator enters in low-power mode during device OFF state. Note that VRTC enters low-power mode when the device is on backup even if this bit is set to 1 (Default value: See boot configuration)	RW	0
2	Reserved	Reserved bit	RO R returns 0s	0
1:0	ST	Reference state: ST[1:0] = 00: Reserved ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Reserved ST[1:0] = 11: On low power (SLEEP) (Write access available in test mode only)	RO	0x1

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Table 36. VIO_REG

Address Offset	0x20		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VIO control register		
Type	RW		

7	6	5	4	3	2	1	0
ILIM		Reserved		SEL		ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6 TPS659119xAIPFPRQ1	ILIM	Current-limit threshold selection: ILIM[1:0] = 00: 0.7 A ILIM[1:0] = 01: 1.2 A ILIM[1:0] = 10: 1.7 A ILIM[1:0] = 11: > 1.7 A	RW	0x0
5:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Output voltage selection (EEPROM bits): SEL[1:0] = 00: 1.5 V SEL[1:0] = 01: 1.8 V SEL[1:0] = 10: 2.5 V SEL[1:0] = 11: 3.3 V (Default value: see boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: OFF ST[1:0] = 01: ON high power (ACTIVE) ST[1:0] = 10: OFF ST[1:0] = 11: ON low power (SLEEP)	RW	0x0

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Table 37. VDD1_REG

Address Offset	0x21		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD1 control register		
Type	RW		

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	VGAIN_SEL	Select output voltage multiplication factor: G (EEPROM bits): When set to 00: x1 When set to 01: TBD When set to 10: x2 When set to 11: x3 (Default value: see boot configuration)	RW	0x0
5:4	ILMAX	Select current limit threshold: When set to 0: 1.2 A When set to 1: > 1.7 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5-mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000: step duration is 0, step function is bypassed TSTEP[2:0] = 001: 12.5 mV/µs (sampling 3 MHz) TSTEP[2:0] = 010: 9.4 mV/µs (sampling 3 MHz × 3/4) TSTEP[2:0] = 011: 7.5 mV/µs (sampling 3 MHz × 3/5) (default) TSTEP[2:0] = 100: 6.25 mV/µs(sampling 3 MHz/2) TSTEP[2:0] = 101: 4.7 mV/µs(sampling 3 MHz/3) TSTEP[2:0] = 110: 3.12 mV/µs(sampling 3 MHz/4) TSTEP[2:0] = 111: 2.5 mV/µs(sampling 3 MHz/5)	RW	0x3
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: OFF ST[1:0] = 01: ON, high-power mode ST[1:0] = 10: OFF ST[1:0] = 11: ON, low-power mode	RW	0x0

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Table 38. VDD1_OP_REG

Address Offset	0x22		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD1 voltage selection register. This register can be accessed by both control and voltage-scaling I^2C interfaces depending on the SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
CMD	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	CMD	When set to 0: VDD1_OP_REG voltage is applied When set to 1: VDD1_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (4 EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) **Note**: from SEL[6:0] = 3 to 75 (dec) V_{OUT} = (SEL[6:0] × 12.5 mV + 0.5625 V) × G (Default value: See boot configuration)	RW	0x00

Table 39. VDD1_SR_REG

Address Offset	0x23		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD1 voltage selection register. This register can be accessed by both control and voltage scaling dedicated I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) **Note**: from SEL[6:0] = 3 to 75 (dec) V_{OUT} = (SEL[6:0] × 12.5 mV + 0.5625 V) × G (Default value: See boot configuration)	RW	0x00

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Table 40. VDD2_REG

Address Offset	0x24		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 control register		
Type	RW		

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	VGAIN_SEL	Select output voltage multiplication factor (x1, x3 included in EEPROM bits): G When set to 00: x1 When set to 01: TBD When set to 10: x2 When set to 11: x3	RW	0x0
5:4	ILMAX	Select current limit threshold When set to 0: 1.2 A When set to 1: > 1.7 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5-mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000: step duration is 0, step function is bypassed TSTEP[2:0] = 001: 12.5 mV/µs (sampling 3 MHz) TSTEP[2:0] = 010: 9.4 mV/µs (sampling 3 MHz × 3/4) TSTEP[2:0] = 011: 7.5 mV/µs (sampling 3 MHz × 3/5) (default) TSTEP[2:0] = 100: 6.25 mV/µs(sampling 3 MHz/2) TSTEP[2:0] = 101: 4.7 mV/µs(sampling 3 MHz/3) TSTEP[2:0] = 110: 3.12 mV/µs(sampling 3 MHz/4) TSTEP[2:0] = 111: 2.5 mV/µs(sampling 3 MHz/5)	RW	0x1
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: OFF ST[1:0] = 01: ON, high-power mode ST[1:0] = 10: OFF ST[1:0] = 11: ON, low-power mode	RW	0x0

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Table 41. VDD2_OP_REG

Address Offset	0x25		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 voltage selection register. This register can be accessed by both control-dedicated and voltage-scaling-dedicated I^2C interfaces depending on the SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
CMD	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	CMD	Command: When set to 0: VDD2_OP_REG voltage is applied When set to 1: VDD2_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (4 EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0.0 V) **Note**: from SEL[6:0] = 3 to 75 (dec) V_{OUT} = (SEL[6:0] × 12.5 mV + 0.5625 V) × G	RW	0x00

Table 42. VDD2_SR_REG

Address Offset	0x26		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	VDD2 voltage selection register. This register can be accessed by both control-dedicated and voltage-scaling-dedicated I^2C interfaces depending on the SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35 V ... SEL[6:0] = 0110011: 1.2 V ... SEL[6:0] = 0000001 to 0000011: 0.6 V SEL[6:0] = 0000000: Off (0 V) **Note**: from SEL[6:0] = 3 to 75 (dec) VOUT= (SEL[6:0] × 12.5 mV + 0.5625 V) × G	RW	0x00

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Table 43. EXTCTRL_REG

Address Offset	0x27		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	EXTCTRL, external converter voltage controller		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	ST	Supply state (EEPROM dependent): ST[1:0] = 00: Off ST[1:0] = 01: On ST[1:0] = 10: Off ST[1:0] = 11: On	RW	0x0

Table 44. EXTCTRL_OP_REG

Address Offset	0x28		
Physical Address		**Instance**	(RESET DOMAIN: TURN OFF RESET)
Description	EXTCTRL voltage-selection register. This register can be accessed by both control-dedicated and voltage-scaling-dedicated I^2C interfaces depending on the SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
CMD	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	CMD	Command: When set to 0: EXTCTRL_OP_REG voltage is applied When set to 1: EXTCTRL_SR_REG voltage is applied	RW	0
6:0	SEL	Resistive divider ratio selection (4 EEPROM bits): For SEL[6:0] = 3 to 67, Ratio = 48 / (45 + SEL[6:0]) SEL[6:0] = 67 to 127: 3/7 V/V SEL[6:0] = 66: 16/37 V/V ... SEL[6:0] = 35: 3/5 V/V ... SEL[6:0] = 5: 24/25 V/V SEL[6:0] = 4: 48/49 V/V SEL[6:0] = 1 to 3: 1 V/V SEL[6:0] = 0 (EN signal low)	RW	0x00

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Table 45. EXTCTRL_SR_REG

Address Offset	0x29		
Physical Address		**Instance**	(RESET DOMAIN: TURN OFF RESET)
Description	EXTCTRL voltage selection register. This register can be accessed by both control-dedicated and voltage-scaling-dedicated I^2C interfaces depending on the SR_CTL_I2C_SEL register bit value.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL						

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO	0
6:0	SEL	Resistive divider ratio selection (4 EEPROM bits): For SEL[6:0] = 3 to 67, Ratio = 48 / (45 + SEL[6:0]) SEL[6:0] = 67 to 127: 3/7 V/V SEL[6:0] = 66: 16/37 V/V ... SEL[6:0] = 35: 3/5 V/V ... SEL[6:0] = 5: 24/25 V/V SEL[6:0] = 4: 48/49 V/V SEL[6:0] = 1 to 3: 1 V/V SEL[6:0] = 0 (EN signal low)	RW	0x03

Table 46. LDO1_REG

Address Offset	0x30		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO1 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 000011: 1 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V (Default value: See boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

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Table 47. LDO2_REG

Address Offset	0x31		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO2 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 000011: 1 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V (Default value: See boot configuration)	RW	0x0
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 48. LDO5_REG

Address Offset	0x32		
Physical Address		**Instance**	(RESET DOMAIN: TUROFF RESET)
Description	LDO5 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

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Table 49. LDO8_REG

Address Offset	0x33		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO8 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 50. LDO7_REG

Address Offset	0x34		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO7 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

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Table 51. LDO6_REG

Address Offset	0x35		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO6 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

Table 52. LDO4_REG

Address Offset	0x36		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO4 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
SEL						ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	SEL	Supply voltage (EEPROM bits): SEL[7:2] = 00000: 00000: 0.8 V SEL[7:2] = 00000: 000001: 0.85 V SEL[7:2] = 00000: 000010: 0.9 V SEL[7:2] = 000100: 1 V SEL[7:2] = 000101: 1.05 V ... SEL[7:2] = 110001: 3.25 V SEL[7:2] = 110010: 3.3 V Applicable voltage selection TRACK LDO 0: 1 V to 3.3 V TRACK LDO 1: 0.8 V to 1.5 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

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Table 53. LDO3_REG

Address Offset	0x37		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF OFF RESET)
Description	LDO3 regulator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEL					ST	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:2	SEL	Supply voltage (EEPROM bits): SEL[6:2] = 00000: 1 V SEL[6:2] = 00001: 1 V SEL[6:2] = 00010: 1 V SEL[6:2] = 00011: 1.1 V ... SEL[6:2] = 11000: 3.2 V SEL[6:2] = 11001: 3.3 V (Default value: See boot configuration)	RW	0x00
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

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Table 54. Therm_REG

Address Offset	0x38		
Physical Address		**Instance**	(RESET DOMAIN:
Description	Thermal control register		bits[5:2}: GENERAL RESET
Type	RW		bit[0] TURNOFF OFF RESET)

7	6	5	4	3	2	1	0
Reserved		THERM_HD	THERM_TS	THERM_HDSEL		Reserved	THERM_STATE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5	THERM_HD	Hot die detector output: When set to 0: the hot die threshold is not reached When set to 1: the hot die threshold is reached	RO	0
4	THERM_TS	Thermal shutdown detector output: When set to 0: the thermal shutdown threshold is not reached When set to 1: the thermal shutdown threshold is reached	RO	0
3:2	THERM_HDSEL	Temperature selection for hot-die detector: When set to 00: Low temperature threshold … When set to 11: High temperature threshold	RW	0x3
1	Reserved		RO R returns 0s	0
0	THERM_STATE	Thermal shutdown module enable signal: When set to 0: thermal shutdown module is disable When set to 1: thermal shutdown module is enable	RW	1

Table 55. BBCH_REG

Address Offset	0x39		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Back-up battery charger control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						BBSEL	BBCHEN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2:1	BBSEL	Back up battery charge voltage selection: BBSEL[1:0] = 00: 3 V BBSEL[1:0] = 01: 2.52 V BBSEL[1:0] = 10: 3.15 V BBSEL[1:0] = 11: VBAT	RW	0x0
0	BBCHEN	Back up battery charge enable	RW	0

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Table 56. DCDCCTRL_REG

Address Offset	0x3E		
Physical Address		**Instance**	RESET DOMAIN: bits [7:3]: TURNOFF OFF RESET bits [2:0]: GENERAL RESET
Description	DCDC control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRACK	VDD2_PSKIP	VDD1_PSKIP	VIO_PSKIP	DCDCCKEXT	DCDCCKSYNC	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved	Reserved bit	RO R returns 0s	0
6	TRACK	1: Tracking mode: LDO4 output follows VDD1 setting when VDD1 active. See the *Functional Registers* section for more information. 0: Normal LDO operation without tracking	RW	0
5	VDD2_PSKIP	VDD2 pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
4	VDD1_PSKIP	VDD1 pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
3	VIO_PSKIP	VIO pulse skip mode enable (EEPROM bit) Default value: See boot configuration	RW	1
2	DCDCCKEXT	This signal control the muxing of the GPIO2 pad: When set to 0: this pad is a GPIO When set to 1: this pad is used as input for an external clock used for the synchronization of the DCDCs	RW	0
1:0	DCDCCKSYNC	DC-DC clock configuration: DCDCCKSYNC[1:0] = 00: no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 01: DCDC synchronous clock with phase shift DCDCCKSYNC[1:0] = 10: no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 11: DCDC synchronous clock	RW	0x1

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Table 57. DEVCTRL_REG

Address Offset	0x3F		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Device control register		
Type	RW		

7	6	5	4	3	2	1	0
PWR_OFF_SEQ	RTC_PWDN	CK32K_CTRL	SR_CTL_I2C_SEL	DEV_OFF_RST	DEV_ON	DEV_SLP	DEV_OFF

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	PWR_OFF_SEQ	When set to 1, power-off is sequential, reverse of power-on sequence (first resource to power on is the last to power off). When set to 0, all resources disabled at the same time	RW	0
6	RTC_PWDN	When set to 1, disable the RTC digital domain (clock gating and reset of RTC registers and logic). This register bit is not reset in BACKUP state.	RW	0
5	CK32K_CTRL	Internal 32-kHz clock source control bit (EEPROM bit): When set to 0, either the crystal oscillator or the external clock is used as the internal 32-kHz clock source When set to set to 1, the internal RC oscillator is used as the 32-kHz clock source.	RW	0
4	SR_CTL_I2C_SEL	Voltage scaling registers access control bit: When set to 0: access to registers by voltage scaling I^2C When set to 1: access to registers by control I^2C. The voltage scaling registers are: VDD1_OP_REG, VDD1_SR_REG, VDD2_OP_REG, VDD2_SR_REG, EXTCTRL_OP_REG, and EXTCTRL_SR_REG.	RW	1
3	DEV_OFF_RST	Writing 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF device state transition (switch-off event) and activate reset of the digital core. This bit is cleared in OFF state.	RW	0
2	DEV_ON	Writing 1 maintains the device on (ACTIVE or SLEEP device state) (if DEV_OFF = 0 and DEV_OFF_RST = 0). EEPROM bit (Default value: See boot configuration)	RW	0
1	DEV_SLP	Writing 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0). Writing 0 starts an SLEEP-to-ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state.	RW	0
0	DEV_OFF	Writing 1 starts an ACTIVE-to-OFF or SLEEP-to-OFF device state transition (switch-off event). This bit is cleared in OFF state.	RW	0

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Table 58. DEVCTRL2_REG

Address Offset	0x40		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Device control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	DCDC_SLEEP_LVL	TSLOT_LENGTH		SLEEPSIG_POL	PWON_LP_OFF	PWON_LP_RST	IT_POL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6	DCDC_SLEEP_LVL	When set to 1, DCDC output level in SLEEP mode is VDDx_SR_REG, to be other than 0 V. When set to 0, no effect	RW	0
5:4	TSLOT_LENGTH	Time slot duration programming (EEPROM bit): When set to 00: 0 µs When set to 01: 200 µs When set to 10: 500 µs When set to 11: 2 ms (Default value: See boot configuration)	RW	0x3
3	SLEEPSIG_POL	When set to 1, SLEEP signal active-high When set to 0, SLEEP signal active-low	RW	0
2	PWON_LP_OFF	When set to 1, allows device turn-off after a PWON Long Press (signal low) (EEPROM bits). (Default value: See boot configuration)	RW	1
1	PWON_LP_RST	When set to 1, allows digital core reset when the device is OFF (EEPROM bit). (Default value: See boot configuration)	RW	0
0	IT_POL	INT1 interrupt pad polarity control signal (EEPROM bit): When set to 0, active low When set to 1, active high (Default value: See boot configuration)	RW	0

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Table 59. SLEEP_KEEP_LDO_ON_REG

Address Offset	0x41		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	When corresponding control bit = 0 in EN1_ LDO_ASS register (default setting): Configuration Register keeping the full load capability of LDO regulator (ACTIVE mode) during the SLEEP state of the device. When control bit = 1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When control bit = 0, the LDO regulator is set or stay in low-power mode during device SLEEP state(but then supply state can be overwritten programming ST[1:0]). There is no control bit value effect if the LDO regulator is off. When corresponding control bit = 1 in EN1_ LDO_ASS register: Configuration register setting the LDO regulator state driven by SCLSR_EN1 signal low level (when SCLSR_EN1 is high the regulator is on, full power): - the regulator is set off if the corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register (default) - the regulator is set in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_KEEPON	LDO4_KEEPON	LDO7_KEEPON	LDO8_KEEPON	LDO5_KEEPON	LDO2_KEEPON	LDO1_KEEPON	LDO6_KEEPON

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	LDO3_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
6	LDO4_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
5	LDO7_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
4	LDO8_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
3	LDO5_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
2	LDO2_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
1	LDO1_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0
0	LDO6_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1 is low	RW	0

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Table 60. SLEEP_KEEP_RES_ON_REG

Address Offset	0x42
Physical Address	**Instance**
Description	Configuration Register keeping, during the SLEEP state of the device (but then supply state can be overwritten programming ST[1:0]): - the full load capability of LDO regulator (ACTIVE mode), - The PWM mode of DC-DC converter - 32-kHz clock output - Register access though I^2C interface (keeping the internal high speed clock on) - Die thermal monitoring is on There is no control bit value effect if the resource is off.
Type	RW

7	6	5	4	3	2	1	0
THERM_KEEPON	CLKOUT32K_KEEPON	VRTC_KEEPON	I2CHS_KEEPON	Reserved	VDD2_KEEPON	VDD1_KEEPON	VIO_KEEPON

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	THERM_KEEPON	When set to 1, thermal monitoring is maintained during device SLEEP state. When set to 0, thermal monitoring is turned off during device SLEEP state.	RW	0
6	CLKOUT32K_KEEPON	When set to 1, CLK32KOUT output is maintained during device SLEEP state. When set to 0, CLK32KOUT output is set low during device SLEEP state.	RW	0
5	VRTC_KEEPON	When set to 1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When set to 0, the LDO regulator is set or stays in low-power mode during device SLEEP state.	RW	0
4	I2CHS_KEEPON	When set to 1, high speed internal clock is maintained during device SLEEP state. When set to 0, high speed internal clock is turned off during device SLEEP state.	RW	0
3	Reserved		RO	0
2	VDD2_KEEPON	When set to 1, VDD2 SMPS-PWM mode is maintained during device SLEEP state. No effect if VDD2 working mode is PFM. When set to 0, VDD2 SMPS-PFM mode is set during device SLEEP state.	RW	0
1	VDD1_KEEPON	When set to 1, VDD1 SMPS-PWM mode is maintained during device SLEEP state. No effect if VDD1 working mode is PFM. When set to 0, VDD1 SMPS-PFM mode is set during device SLEEP state.	RW	0
0	VIO_KEEPON	When set to 1, VIO SMPS-PWM mode is maintained during device SLEEP state. No effect if VIO working mode is PFM. When set to 0, VIO SMPS-PFM mode is set during device SLEEP state.	RW	0

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Table 61. SLEEP_SET_LDO_OFF_REG

Address Offset	0x43		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Configuration register turning-off LDO regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON register should be 0 to make this *_SET_OFF control bit effective		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_SETOFF	LDO4_SETOFF	LDO7_SETOFF	LDO8_SETOFF	LDO5_SETOFF	LDO2_SETOFF	LDO1_SETOFF	LDO6_SETOFF

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	LDO3_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
6	LDO4_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
5	LDO7_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
4	LDO8_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
3	LDO5_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
2	LDO2_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
1	LDO1_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0
0	LDO6_SETOFF	When set to 1, LDO regulator is turned off during device SLEEP state. When set to 0, No effect	RW	0

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Table 62. SLEEP_SET_RES_OFF_REG

Address Offset	0x44		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Configuration Register turning-off SMPS regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON2 register should be 0 to make this *_SET_OFF control bit effective. Supplies voltage expected after the wake-up (SLEEP-to-ACTIVE state transition) can also be programmed.		
Type	RW		

7	6	5	4	3	2	1	0
DEFAULT_VOLT	Reserved		SPARE_SETOFF	EXTCTRL_SETOFF	VDD2_SETOFF	VDD1_SETOFF	VIO_SETOFF

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	DEFAULT_VOLT	When set to 1, default voltages (register value after switch-on) are applied to all resources during SLEEP-to-ACTIVE transition. When set to 0, voltages programmed before the ACTIVE-to-SLEEP state transition are used to turned-on supplies during SLEEP-to-ACTIVE state transition.	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	SPARE_SETOFF	Spare bit	RW	0
3	EXTCTRL_SETOFF	When set to 1, SMPS is turned off during device SLEEP state. When set to 0, No effect.	RW	0
2	VDD2_SETOFF	When set to 1, SMPS is turned off during device SLEEP state. When set to 0, No effect.	RW	0
1	VDD1_SETOFF	When set to 1, SMPS is turned off during device SLEEP state. When set to 0, No effect.	RW	0
0	VIO_SETOFF	When set to 1, SMPS is turned off during device SLEEP state. When set to 0, No effect.	RW	0

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Table 63. EN1_LDO_ASS_REG

Address Offset	0x45		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the LDO regulators, driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, LDO regulator state is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SCLSR_EN1 is high the regulator is on, When SCLSR_EN1 is low: - the regulator is off if the corresponding control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low-power mode if the corresponding control bit = 1 **in** SLEEP_KEEP_LDO_ON register When control bit = 0 no effect: LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 disables the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_EN1	LDO4_EN1	LDO7_EN1	LDO8_EN1	LDO5_EN1	LDO2_EN1	LDO1_EN1	LDO6_EN1

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	LDO3_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
6	LDO4_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
5	LDO7_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
4	LDO8_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
3	LDO5_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
2	LDO2_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
1	LDO1_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0
0	LDO6_EN1	Setting supply-state control though the SCLSR_EN1 signal	RW	0

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Table 64. EN1_SMPS_ASS_REG

Address Offset	0x46		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration register setting the SMPS supplies driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, SMPS supply state and voltage is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect: SMPS Supply state is driven though registers programming and the device state. Any control bit of this register set to 1 disables the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			SPARE_EN1	EXTCTRL_EN1	VDD2_EN1	VDD1_EN1	VIO_EN1

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved		RO R returns 0s	0x0
4	SPARE_EN1	Spare bit	RW	0
3	EXTCTRL_EN1	When control bit = 1: When EN1 is high the supply voltage is programmed though EXTCTRL_OP_REG register, and it can also be programmed off. When EN1 is low the supply voltage is programmed though EXTCTRL_SR_REG register, and it can also be programmed off. When control bit = 0: No effect: Supply state is driven though registers programming and the device state	RW	0
2	VDD2_EN1	When control bit = 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off through VDD2_SR_REG register. When control bit = 0 No effect: the supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN1	When 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
0	VIO_EN1	When control bit = 1, the supply state is driven by the SCLSR_EN1 control signal and is also defined though the SLEEP_KEEP_RES_ON register setting: When SCLSR_EN1 is high the supply is on, When SCLSR_EN1 is low: - the supply is off (default) or the SMPS is working in low-power mode if the corresponding control bit = 1 in SLEEP_KEEP_RES_ON register When control bit = 0 No effect: SMPS state is driven though registers programming and the device state	RW	0

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Table 65. EN2_LDO_ASS_REG

Address Offset	0x47		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the LDO regulators, driven by the multiplexed SDASR_EN2 signal. When control bit = 1, LDO regulator state is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SDASR_EN2 is high the regulator is on, When SCLSR_EN2 is low: - the regulator is off if the corresponding control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low-power mode if the corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register When control bit = 0 no effect: LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 disables the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
LDO3_EN2	LDO4_EN2	LDO7_EN2	LDO8_EN2	LDO5_EN2	LDO2_EN2	LDO1_EN2	LDO6_EN2

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	LDO3_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
6	LDO4_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
5	LDO7_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
4	LDO8_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
3	LDO5_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
2	LDO2_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
1	LDO1_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0
0	LDO6_EN2	Setting supply-state control though the SDASR_EN2 signal	RW	0

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Table 66. EN2_SMPS_ASS_REG

Address Offset	0x48		
Physical Address		**Instance**	(RESET DOMAIN: TURNOFF RESET)
Description	Configuration Register setting the SMPS Supplies driven by the multiplexed SDASR_EN2 signal. When control bit = 1, the SMPS Supply state and voltage is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect: the SMPS Supply state is driven though registers programming and the device state Any control bit of this register set to 1 disables the I^2C SR Interface functionality		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			SPARE_EN2	EXTCTRL_EN2	VDD2_EN2	VDD1_EN2	VIO_EN2

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved		RO R returns 0s	0x0
4	SPARE_EN2	Spare bit	RW	0
3	EXTCTRL_EN2	When control bit = 1: When EN2 is high the supply voltage is programmed though EXTCTRL_OP_REG register, and it can also be programmed off.. When EN2 is low the supply voltage is programmed though EXTCTRL_SR_REG register, and it can also be programmed off. When EN2 is low and EXTCTRL_KEEPON = 1 the SMPS is working in low-power mode, if not tuned off though EXTCTRL_SR_REG register. When control bit = 0 no effect: the supply state is driven though registers programming and the device state	RW	0
2	VDD2_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD2_SR_REG register. When control bit = 0 no effect: the supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low-power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: the supply state is driven though registers programming and the device state	RW	0
0	VIO_EN2	When control bit = 1, supply state is driven by the SCLSR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting: When SDASR _EN2 is high the supply is on, When SDASR _EN2 is low : - the supply is off (default) or the SMPS is working in low-power mode if its corresponding control bit = 1 in SLEEP_KEEP_RES_ON register When control bit = 0 no effect: the SMPS state is driven though registers programming and the device state	RW	0

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Table 67. INT_STS_REG

Address Offset	0x50		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. The interrupt-status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_PERIOD_IT	RTC_ALARM_IT	HOTDIE_IT	PWRHOLD_R_IT	PWRON_LP_IT	PWRON_IT	Reserved	PWRHOLD_F_IT

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	RTC_PERIOD_IT	RTC-period-event interrupt status	RW W1 to Clr	0
6	RTC_ALARM_IT	RTC-alarm-event interrupt status	RW W1 to Clr	0
5	HOTDIE_IT	Hot-die-event interrupt status	RW W1 to Clr	0
4	PWRHOLD_R_IT	Rising-PWRHOLD-event interrupt status	RW W1 to Clr	0
3	PWRON_LP_IT	PWRON-long-press event interrupt status	RW W1 to Clr	0
2	PWRON_IT	PWRON-event interrupt status	RW W1 to Clr	0
1	Reserved	Reserved, always clear	RW W1 to Clr	0
0	PWRHOLD_F_IT	Falling-PWRHOLD-event interrupt status	RW W1 to Clr	0

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Table 68. INT_MSK_REG

Address Offset	0x51		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

7	6	5	4	3	2	1	0
RTC_PERIOD_IT_MSK	RTC_ALARM_IT_MSK	HOTDIE_IT_MSK	PWRHOLD_R_IT_MSK	PWRON_LP_IT_MSK	PWRON_IT_MSK	Reserved	PWRHOLD_F_IT_MSK

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	RTC_PERIOD_IT_MSK	RTC-period-event interrupt mask	RW	1
6	RTC_ALARM_IT_MSK	RTC-alarm-event interrupt mask	RW	1
5	HOTDIE_IT_MSK	Hot-die-event interrupt mask	RW	1
4	PWRHOLD_R_IT_MSK	PWRHOLD rising-edge-event interrupt mask	RW	1
3	PWRON_LP_IT_MSK	PWRON long-press-event interrupt mask	RW	1
2	PWRON_IT_MSK	PWRON-event interrupt mask	RW	1
1	Reserved	Reserved, always masks	RW	1
0	PWRHOLD_F_IT_MSK	PWRHOLD falling-edge-event interrupt mask	RW	1

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Table 69. INT_STS2_REG

Address Offset	0x52		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3_F_IT	GPIO3_R_IT	GPIO2_F_IT	GPIO2_R_IT	GPIO1_F_IT	GPIO1_R_IT	GPIO0_F_IT	GPIO0_R_IT

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO3_F_IT	GPIO3 falling-edge-detection interrupt status	RW W1 to Clr	0
6	GPIO3_R_IT	GPIO3 rising-edge-detection interrupt status	RW W1 to Clr	0
5	GPIO2_F_IT	GPIO2 falling-edge-detection interrupt status	RW W1 to Clr	0
4	GPIO2_R_IT	GPIO2 rising-edge-detection interrupt status	RW W1 to Clr	0
3	GPIO1_F_IT	GPIO1 falling-edge-detection interrupt status	RW W1 to Clr	0
2	GPIO1_R_IT	GPIO1 rising-edge-detection interrupt status	RW W1 to Clr	0
1	GPIO0_F_IT	GPIO0 falling-edge-detection interrupt status	RW W1 to Clr	0
0	GPIO0_R_IT	GPIO0 rising-edge-detection interrupt status	RW W1 to Clr	0

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Table 70. INT_MSK2_REG

Address Offset	0x53		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3_F_IT_MSK	GPIO3_R_IT_MSK	GPIO2_F_IT_MSK	GPIO2_R_IT_MSK	GPIO1_F_IT_MSK	GPIO1_R_IT_MSK	GPIO0_F_IT_MSK	GPIO0_R_IT_MSK

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO3_F_IT_MSK	GPIO3 falling-edge-detection interrupt mask	RW	1
6	GPIO3_R_IT_MSK	GPIO3 rising-edge-detection interrupt mask	RW	1
5	GPIO2_F_IT_MSK	GPIO2 falling-edge-detection interrupt mask	RW	1
4	GPIO2_R_IT_MSK	GPIO2 rising-edge-detection interrupt mask	RW	1
3	GPIO1_F_IT_MSK	GPIO1 falling-edge-detection interrupt mask	RW	1
2	GPIO1_R_IT_MSK	GPIO1 rising-edge-detection interrupt mask	RW	1
1	GPIO0_F_IT_MSK	GPIO0 falling-edge-detection interrupt mask	RW	1
0	GPIO0_R_IT _MSK	GPIO0 rising-edge-detection interrupt mask	RW	1

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Table 71. INT_STS3_REG

Address Offset	0x54		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. The interrupt-status bit is cleared by writing 1.		
Type	RW		

7	6	5	4	3	2	1	0
PWRDN_IT	Reserved	Reserved	WTCHDG_IT	GPIO5_F_IT	GPIO5_R_IT	GPIO4_F_IT	GPIO4_R_IT

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	PWRDN_IT	PWRDN reset input high detected	RW W1 to Clr	0
6	Reserved	Always clear	RW W1 to Clr	0
5	Reserved	Always clear	RW W1 to Clr	0
4	WTCHDG_IT	Watchdog interrupt status	RW W1 to Clr	0
3	GPIO5_F_IT	GPIO5 falling-edge-detection interrupt status	RW W1 to Clr	0
2	GPIO5_R_IT	GPIO5 rising-edge-detection interrupt status	RW W1 to Clr	0
1	GPIO4_F_IT	GPIO4 falling-edge-detection interrupt status	RW W1 to Clr	0
0	GPIO4_R_IT	GPIO4 rising-edge-detection interrupt status	RW W1 to Clr	0

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Table 72. INT_MSK3_REG

Address Offset	0x55		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.		
Type	RW		

7	6	5	4	3	2	1	0
PWRDN_IT_MSK	Reserved	Reserved	WTCHDG_IT_MSK	GPIO5_F_IT_MSK	GPIO5_R_IT_MSK	GPIO4_F_IT_MSK	GPIO4_R_IT_MSK

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	PWRDN_IT_MSK	PWRDN interrupt mask	RW	1
6	Reserved	Always clear	RW	1
5	Reserved	Always clear	RW	1
4	WTCHDG_IT_MSK	Watchdog interrupt mask	RW	1
3	GPIO5_F_IT_MSK	GPIO5 falling-edge-detection interrupt mask	RW	1
2	GPIO5_R_IT_MSK	GPIO5 rising-edge-detection interrupt mask	RW	1
1	GPIO4_F_IT_MSK	GPIO4 falling-edge-detection interrupt mask	RW	1
0	GPIO4_R_IT_MSK	GPIO4 rising-edge-detection interrupt mask	RW	1

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Table 73. GPIO0_REG

Address Offset	0x60		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO0 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO_SLEEP	1: as GPO, force low 0: No impact, keep as in active mode	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5	GPIO_ODEN	Selection of output mode, EEPROM bit 0: Push-pull output 1: Open-drain output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit is set to 1 by a TURNOFF reset	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	0
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output (Default value: See boot configuration)	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit is in TURNOFF reset	RW	0

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Table 74. GPIO1_REG

Address Offset	0x61		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO1 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		GPIO_SEL	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 0: GPIO_SET 1: LED1 out	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

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Table 75. GPIO2_REG

Address Offset	0x62		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO2 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit is set to 0 by a TURNOFF reset	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit is set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit is in TURNOFF reset	RW	0

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Table 76. GPIO3_REG

Address Offset	0x63		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO3 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	GPIO_SEL		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RO R returns 0s	0
6:5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 00: GPIO_SET 01: LED2 out 10: PWM out	RW	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 77. GPIO4_REG

Address Offset	0x64		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO4 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

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Table 78. GPIO5_REG

Address Offset	0x65		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO5 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

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Table 79. GPIO6_REG

Address Offset	0x66		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO6 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit is set to 0 by a TURNOFF reset	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit is set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit is in TURNOFF reset	RW	0

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Table 80. GPIO7_REG

Address Offset	0x67		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO7 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
GPIO_SLEEP	Reserved		GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	GPIO_SLEEP	1: as GPO, force low 0: no impact, keep as is in active mode	RW	0
6:5	Reserved		RO R returns 0s	0x0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown-control: 1: Pulldown is enabled 0: Pulldown is disabled GPIO assigned to power-up sequence, this bit is set to 0 by a TURNOFF reset	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output (Default value: See boot configuration) GPIO assigned to power-up sequence, this bit is set to 1 by a TURNOFF reset	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	The value set on the GPIO output when configured in output mode GPIO assigned to power-up sequence, this bit is in TURNOFF reset	RW	0

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Table 81. GPIO8_REG

Address Offset	0x68		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	GPIO8 configuration register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		GPIO_SEL	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5	GPIO_SEL	Select signal to be available at GPIO when configured as output: 0: GPIO_SET 1: LED1 out	RW	0
4	GPIO_DEB	GPIO input debouncing time configuration: When set to 0, the debouncing is 91.5 µs using a 30.5-µs clock rate When set to 1, the debouncing is 150 ms using a 50-ms clock rate	RW	0
3	GPIO_PDEN	GPIO pad pulldown control: 1: Pulldown is enabled 0: Pulldown is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO pad direction: When set to 0, the pad is configured as an input When set to 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

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Table 82. WATCHDOG_REG

Address Offset	0x69		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Watchdog		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				WTCHDG_MODE	WTCHDG_TIME		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:4	Reserved		RO R returns 0s	0x0
3	WTCHDG_MODE	0: Periodic operation: A periodical interrupt is generated based on WTCHDG_TIME setting. The IC generates WTCHDOG shutdown if an interrupt is not cleared during the period. 1: Interrupt mode: The IC generates WTCHDOG shutdown if an interrupt is pending (no cleared) more than WTCHDG_TIME s.	RW	0
2:0	WTCHDG_TIME	000: Watchdog disabled 001: 5 seconds 010: 10 seconds 011: 20 Seconds 100: 40 seconds 101: 60 seconds 110: 80 seconds 111: 100 seconds (EEPROM bit) (Default value: See boot configuration)	RW	0x0

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Table 83. BOOTSEQVER_REG

Address Offset	0x6A		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Comparator control register		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		BOOTSEQVER_SEL					Reserved

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5:1	BOOTSEQVER_SEL	EEPROM boot-sequence version	RW	0x00
0	Reserved		RO R returns 0s	0

Table 84. RESERVED

Address Offset	0x6B		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	Reserved		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		Reserved					VMBDCH2_DEB

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5:1	Reserved		RW	0x00
0	Reserved		RW	0

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Table 85. LED_CTRL1_REG

Address Offset	0x6C		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	LED ON and OFF control register.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		LED2_PERIOD			LED1_PERIOD		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5:3	LED2_PERIOD	Period of LED2 signal: 000: LED2 OFF 001: 0.125 s 010: 0.25 s ... 110: 4 s 111: 8 s	RW	0x0
2:0	LED1_PERIOD	Period of LED1 signal: 000: LED1 OFF 001: 0.125 s 010: 0.25 s ... 10: 2 s 110: 4 s 111: 8 s	RW	0x0

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Table 86. LED_CTRL2_REG1

Address Offset	0x6D		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	LED ON and OFF control register.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		LED2_SEQ	LED1_SEQ	LED2_ON_TIME		LED1_ON_TIME	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:6	Reserved		RO R returns 0s	0x0
5	LED2_SEQ	When set to 1, LED2 repeats two pulse sequences: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period When set to 0, LED2 generates one pulse: ON (ON_TIME) - OFF (ON TIME))	RW	0
4	LED1_SEQ	When set to 1, LED1 repeats two pulse sequence: ON (ON_TIME) - OFF (ON TIME) - ON (ON TIME) - OFF remainder of the period. When set to 0, LED1 generates one pulse: ON (ON_TIME) - OFF (ON TIME))	RW	0
3:2	LED2_ON_TIME	LED2 ON time: 00: 62.5 ms 01: 125 ms 10: 250 ms 11: 500 ms	RW	0x0
1:0	LED1_ON_TIME	LED1 ON time: 00: 62.5 ms 01: 125 ms 10: 250 ms 11: 500 ms	RW	0x0

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Table 87. PWM_CTRL1_REG

Address Offset	0x6E		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	PWM frequency		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						PWM_FREQ	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:2	Reserved	Reserved bit	RO R returns 0s	0x00
1:0	PWM_FREQ	Frequency of PWM: 00: 500 Hz 01: 250 Hz 10: 125 Hz 11: 62.5 Hz	RW	0x0

Table 88. PWM_CTRL2_REG

Address Offset	0x6F		
Physical Address		**Instance**	(RESET DOMAIN: GENERAL RESET)
Description	PWM duty cycle.		
Type	RW		

7	6	5	4	3	2	1	0
FREQ_DUTY_CYCLE							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	FREQ_DUTY_CYCLE	Duty cycle of PWM: 00000000: 0/256 ... 11111111: 255/256	RW	0x00

Table 89. SPARE_REG

Address Offset	0x70		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Spare functional register		
Type	RW		

7	6	5	4	3	2	1	0
SPARE							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:0	SPARE	Spare bits	RW	0x00

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Table 90. VERNUM_REG

Address Offset	0x80		
Physical Address		**Instance**	(RESET DOMAIN: FULL RESET)
Description	Silicon version number		
Type	RW		

7	6	5	4	3	2	1	0
READ_BOOT	Reserved			VERNUM			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	READ_BOOT	This bit enables the read of the BOOT mode in order to enter JTAG mode. 0: Disabled 1: Enabled	RW	0
6:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:0	VERNUM	Value depending on silicon version number 0000 - Revision 1.0	RO	0x0

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS659119-Q1 device is an integrated power-management integrated circuit (PMIC) that comes in an 80-pin, 0.5-mm pitch, LQFP package with thermal pad. This device was designed specifically for automotive applications and is dedicated to designs powered from a 5-V input supply that require multiple power rails. The device provides three step-down converters along with an interface to control an external converter and eight LDO regulators. The device can support a variety of different processors and applications. Two of the step-down converters support dynamic voltage scaling through a dedicated I^2C interface to provide optimum power savings. The third converter provides power for the I/Os and memory in the system.

In addition to the power resources, the device contains an embedded power controller (EPC) to manage the power sequencing requirements of systems. The power sequencing is programmable through EEPROM. The device also contains nine configurable GPIOs, a real-time clock module, an internal watchdog circuit, and two LED ON and OFF signal generators.

Details on how to use this device in automotive applications are described throughout this device specification. The following sections provide the typical application use-case with the recommended external components and layout guidelines.

9.2 Typical Application

Following the typical application schematic (see Figure 25) and the list of recommended external components will allow the TPS659119-Q1 device to achieve accurate and stable regulation with the step-down converters and LDO regulators. These devices are internally compensated and have been designed to operate most effectively with the component values listed in Table 91. Deviating from these values is possible but is not recommended.

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Typical Application (continued)

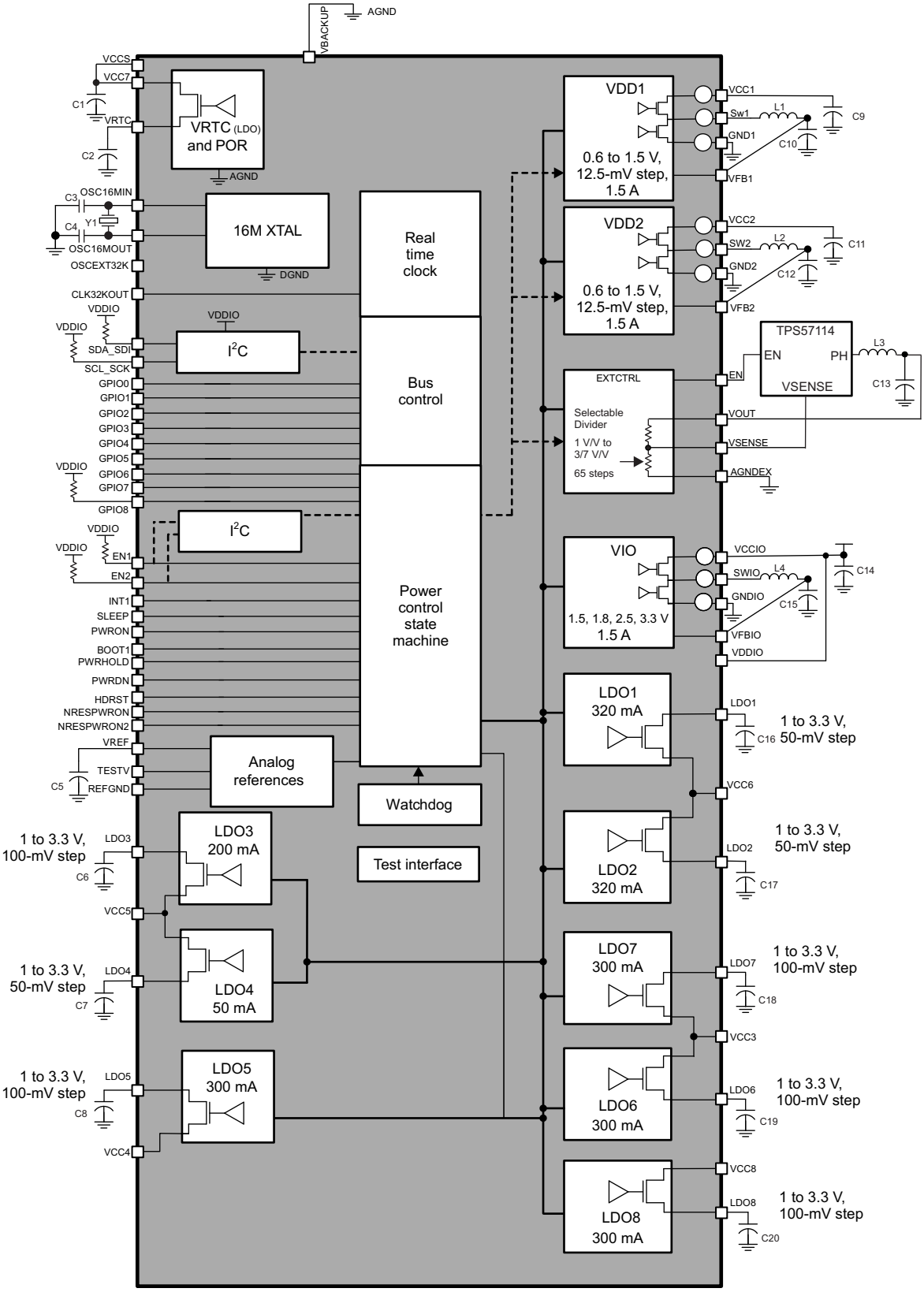

Figure 25. Application Schematic

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Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 91.

Table 91. Design Parameters

REFERENCE DESIGNATOR	COMPONENT FUNCTION	VALUE(1)
C1	Input-supply decoupling capacitor	4.7 µF, 10 V
C2	VRTC output capacitor	2.2 µF, 6.3 V
C3	Crystal load capacitors	10 pF, 50 V
C4		
C5	VREF filtering capacitor	100 nF
C6	LDO output capacitors	2.2 µF, 6.3 V
C7		
C8		
C16		
C17		
C18		
C19		
C20		
C9	Step-down converter input capacitors	10 µF, 10 V
C11		
C14		
C10	Step-down converter output capacitors	10 µF, 10 V
C12		
C15		
C13	External-converter output capacitor	22 µF, 10 V (×2)
L1	Step-down converter inductors	2.2 µH, 2.6 A
L2		
L3		
L4		
Y1	Crystal	16.384 MHz

(1) Component minimum, maximum, or typical values are specified in the electrical-parameter section of each IP (see the *External Component Recommendation* section).

9.2.2 Detailed Design Procedure

9.2.2.1 Step-down Converter Input Capacitors

All step-down converter inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 10-V, 10-µF capacitor for each step-down converter input is recommended. Depending on the input voltage of the step-down converter, a 6.3-V or 10-V capacitor can be used.

For optimal performance, the input capacitors should be placed as close to the step-down converter-input pins as possible. See the *Layout Guidelines* section for more information about component placement.

9.2.2.2 Step-down Converter Output Capacitors

All step-down converter outputs require an output capacitor to hold up the output voltage during a load step or a change to the input voltage. To ensure stability across the entire switching frequency range, the TPS659119-Q1 device requires an output capacitance value between 4 µF and 12 µF. To meet this requirement across temperature and DC bias voltage, using a 10-µF capacitor for each step-down converter is recommended.

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9.2.2.3 Step-down Converter Inductors

Again, to ensure stability across the entire switching frequency range, TI recommends to use a 2.2-µH inductor on each step-down converter. Because the maximum DC current for each step-down converter is 1.5-A, selecting an inductor with a saturation current of at least 2.3-A is important.

9.2.2.4 LDO Input Capacitors

All LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 10-V, 4.7-µF capacitor on each LDO input voltage supply (VCC3, VCC4, VCC5, and VCC6) is recommended. Depending on the input voltage of the LDO, a 6.3-V or 10-V capacitor can be used.

For optimal performance, the LDO input capacitors should be placed as close as possible to the LDO input pins. See the *Layout Guidelines* section for more information about component placement.

9.2.2.5 LDO Output Capacitors

All LDO outputs require an output capacitor to hold up the voltage during a load step or changes to the input voltage. Using a 6-V, 2.2-µF capacitor is recommended for each LDO.

9.2.2.6 VCC7

The VCC7 pin is the input supply for VRTC as well as the analog references of the device. This pin requires a 4.7-µF decoupling capacitor.

9.2.3 Application Curves

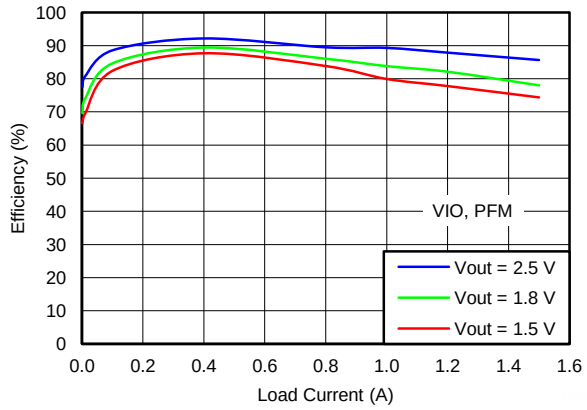

Figure 26. VIO Efficiency vs Load Current, 25°C V_{IN} = 4 V, PFM

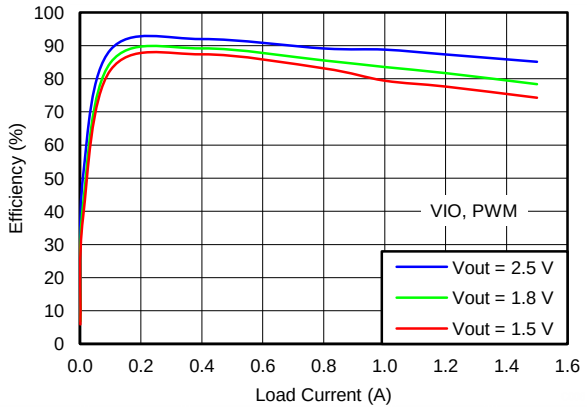

Figure 27. VIO Efficiency vs Load Current, 25°C, V_{OUT} = 2.5 V, V_{IN} = 4 V, PWM

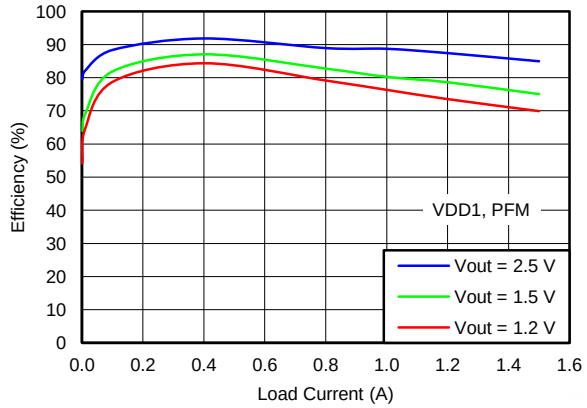

Figure 28. VDD1 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PFM

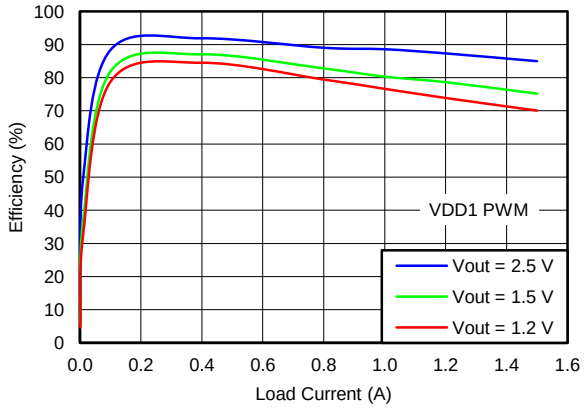

Figure 29. VDD1 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PWM

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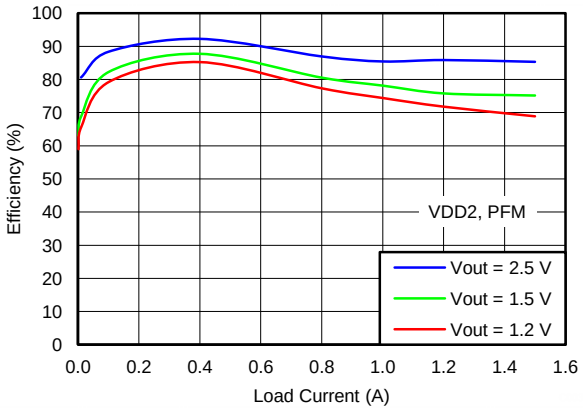

Figure 30. VDD2 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PFM

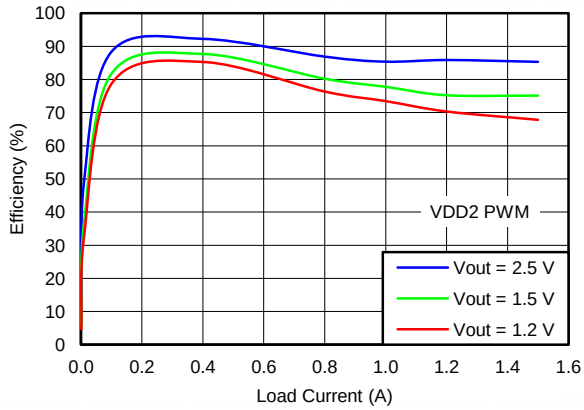

Figure 31. VDD2 Efficiency vs Load Current, 25°C, V_{IN} = 4 V, PWM

10 Power Supply Recommendations

The TPS659119-Q1 device is designed to work with an analog supply voltage range of 4-V to 5.5-V. Typically, a stable 5-V supply is provided to the VCC7 pin as well as the step-down converter and LDO input pins with the appropriate bypass capacitors. If the input supply is located more than a few inches from the TPS659119-Q1 device, additional capacitance may be required in addition to the recommended input capacitors at the VCC7 pin and the step-down converter and LDO input pins.

11 Layout

11.1 Layout Guidelines

As in every switch-mode-supply design, general layout rules apply.

- Use a solid ground plane for power ground (PGND).
- Use an independent ground for logic, LDOs, and analog (AGND).
- Connect those grounds at a star point ideally underneath the IC.
- Place the input capacitors as close as possible to the input pins of the IC.

NOTE

This guideline is the most important and is more important than the output loop.

- Place the inductor and output capacitor as close as possible to the phase node (or switch node) of the IC
- Keep the loop area formed by the phase node, inductor, output capacitor, and PGND as small as possible.
- For traces and vias on power lines, keep inductance and resistance as low as possible by using wide traces and plane shapes. Avoid switching layers, but if needed, use plenty of vias.

The goal of the previously listed guidelines is a layout that minimizes emissions, maximizes EMI immunity, and maintains a safe operating area of the IC.

To minimize the spiking at the phase node for both the high-side (VIN – SWx) as well as the low-side (SWx – PGND), the decoupling of VIN is critical. Appropriate decoupling and thorough layout practices should ensure that the spikes never exceed the absolute maximum rating of the respective pin.

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11.2 Layout Example

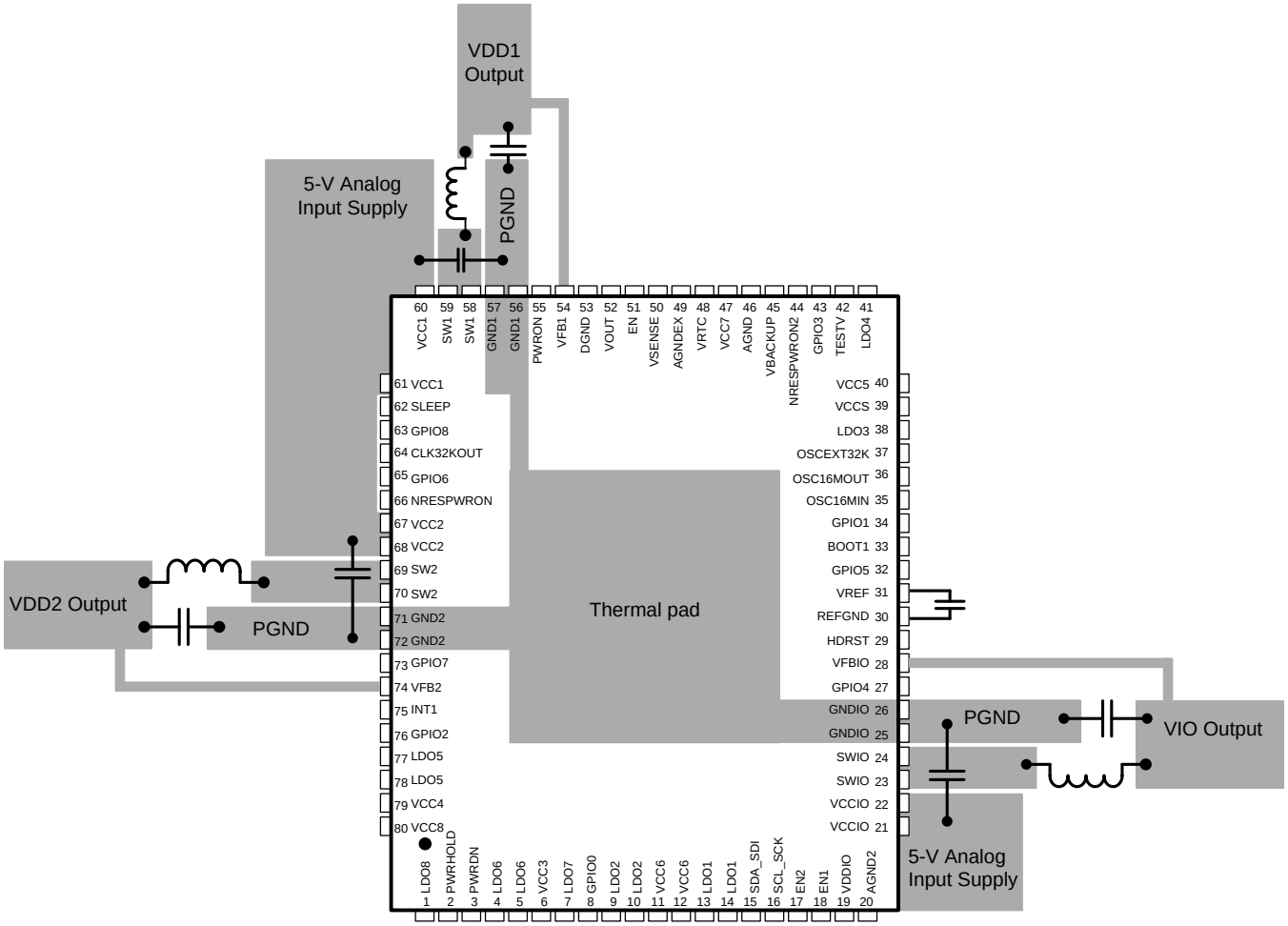

Figure 32. TPS659119-Q1 Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 92. Acronyms, Abbreviations, and Definitions

ACRONYM	DEFINITION
DDR	Dual-Data Rate (memory)
ES	Engineering Sample
ESD	Electrostatic Discharge
FET	Field Effect Transistor
EPC	Embedded Power Controller
FSM	Finite State Machine
GND	Ground
GPIO	General-Purpose I/O
HBM	Human Body Model
HD	Hot-Die
HS-I^2C	High-Speed I^2C
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ID	Identification
IDDQ	Quiescent Supply Current
IEEE	Institute of Electrical and Electronics Engineers
IR	Instruction Register
I/O	Input/Output
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LBC7	Lin Bi-CMOS 7 (360 nm)
LDO	Low Drop Output Voltage Linear Regulator
LP	Low-Power Application Mode
LSB	Least Significant Bit
MMC	Multimedia Card
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NVM	Nonvolatile Memory
OD	Open Drain
OMAP™	Open Multimedia Application Platform™
RTC	Real-Time Clock
SMPS	Switched Mode Power Supply
SPI	Serial Peripheral Interface
POR	Power-On Reset

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

OMAP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS659119AIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119A1
TPS659119AIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119A1
TPS659119BAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119BA
TPS659119BAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119BA
TPS659119CAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119CA
TPS659119CAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119CA
TPS659119DAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119DA
TPS659119DAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119DA
TPS659119EAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119EA
TPS659119EAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119EA
TPS659119FAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119FA
TPS659119FAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119FA
TPS659119HAIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119HA
TPS659119HAIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119HA
TPS659119KBIPFPRQ1	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	T659119KB
TPS659119KBIPFPRQ1.B	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	T659119KB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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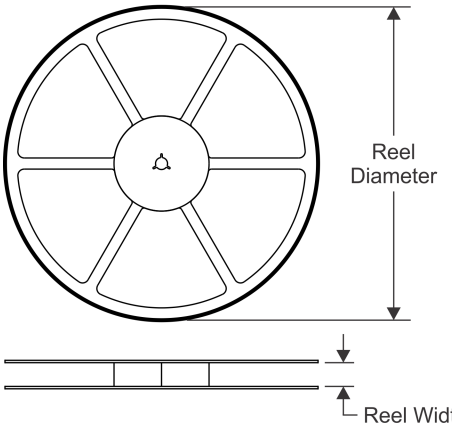
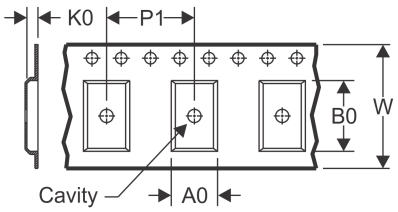
TAPE AND REEL INFORMATION

REEL DIMENSIONS

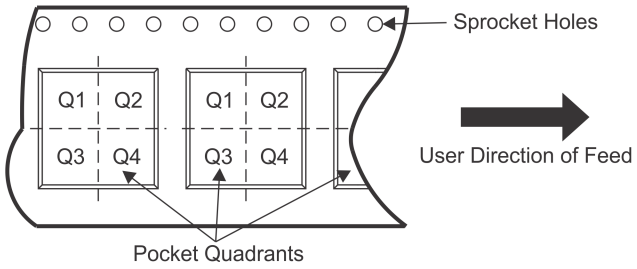


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

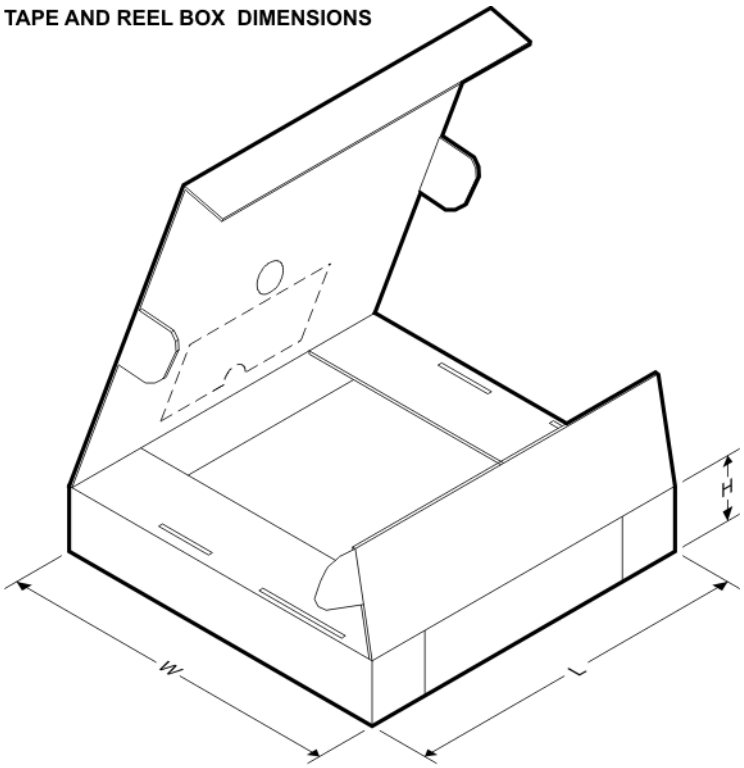
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS659119AIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119BAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119CAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119DAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119EAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119FAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119HAIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TPS659119KBIPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

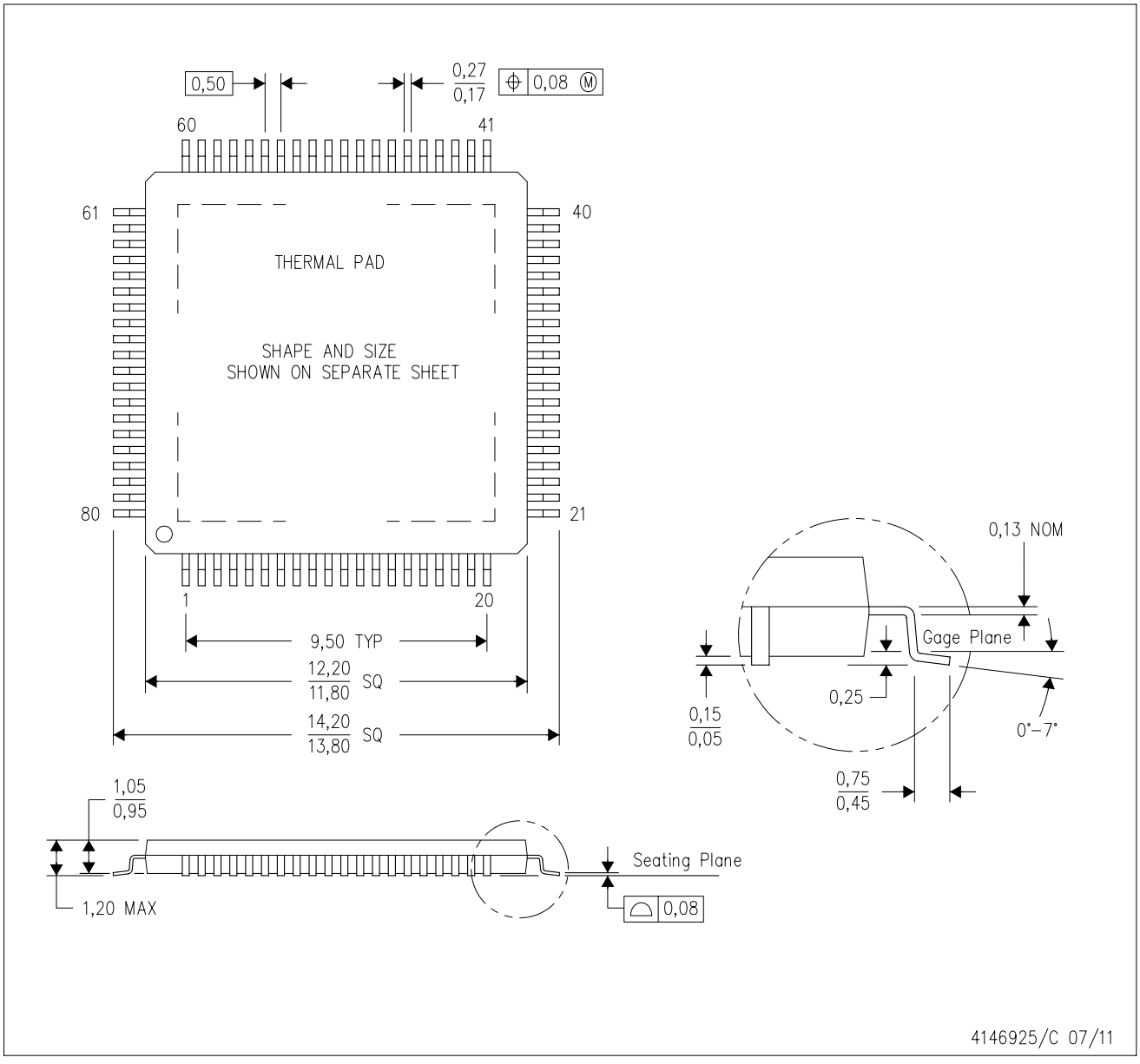
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS659119AIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119BAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119CAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119DAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119EAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119FAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119HAIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0
TPS659119KBIPFPRQ1	HTQFP	PFP	80	1000	367.0	367.0	55.0

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

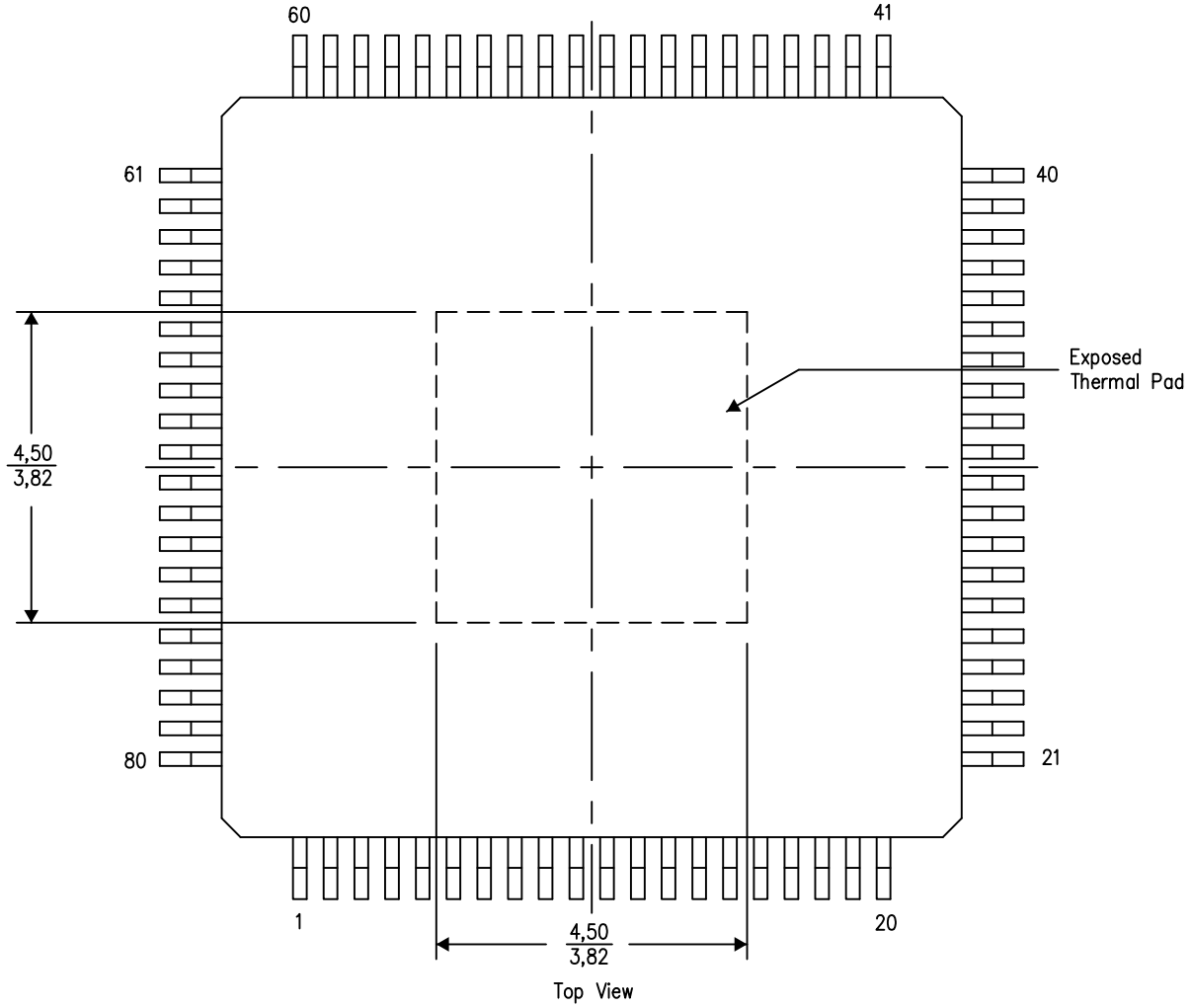
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



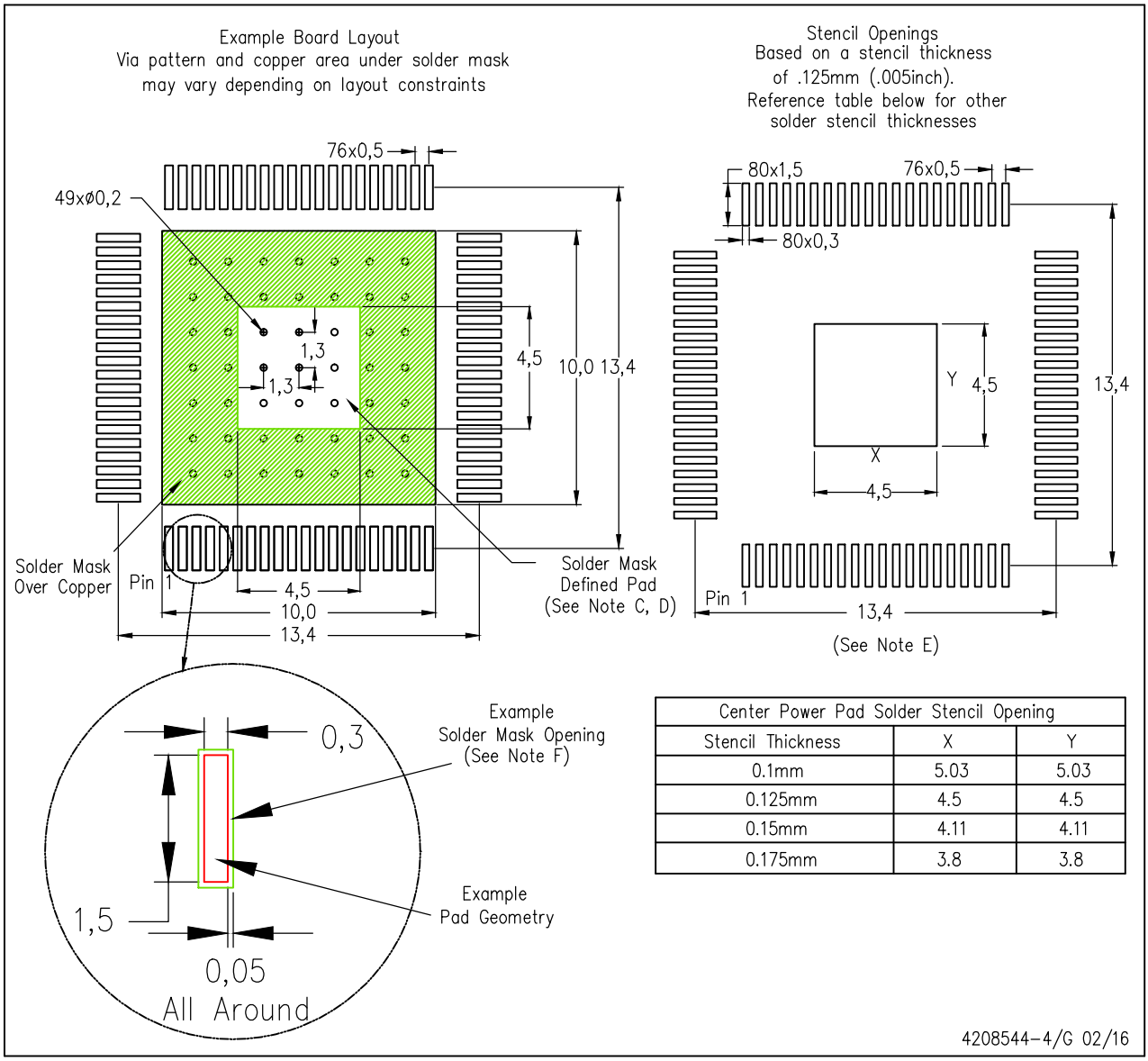
Exposed Thermal Pad Dimensions

4206327–15/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.03	5.03
0.125mm	4.5	4.5
0.15mm	4.11	4.11
0.175mm	3.8	3.8

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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