THE DATASHEET OF

TPS51200DRCR

www.win-source.net 0086-755-83957316

TPS51200 Sink and Source DDR Termination Regulator

1 Features

- Input Voltage: Supports 2.5-V Rail and 3.3-V Rail
- VLDOIN Voltage Range: 1.1 V to 3.5 V
- Sink and Source Termination Regulator Includes Droop Compensation
- Requires Minimum Output Capacitance of 20-µF (Typically 3 × 10-µF MLCCs) for Memory Termination Applications (DDR)
- PGOOD to Monitor Output Regulation
- EN Input
- REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (VOSNS)
- ±10-mA Buffered Reference (REFOUT)
- Built-in Soft Start, UVLO, and OCL
- Thermal Shutdown
- Supports DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT Applications
- 10-Pin VSON Package With Thermal Pad

2 Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Telecom and Datacom
- Base Stations
- LCD-TVs and PDP-TVs
- Copiers and Printers
- Set-Top Boxes

3 Description

The TPS51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The TPS51200 maintains a fast transient response and requires a minimum output capacitance of only 20 µF. The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.

In addition, the TPS51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

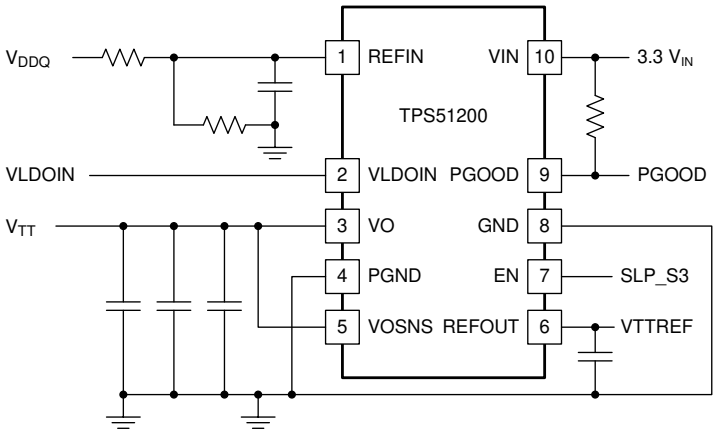
The TPS51200 is available in the thermally efficient 10-pin VSON thermal pad package, and is rated both Green and Pb-free. It is specified from –40°C to +85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51200	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified DDR Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2016) to Revision D — **Page**

- Added "keep total REFOUT capacitance below 0.47 μF" in Pin Functions table ... 4

Changes from Revision B (September 2016) to Revision C — **Page**

- Added references to DDR3L DRAM technology throughout ... 1
- Added DDR3L test conditions to *Output DC voltage, VO* and *REFOUT* specification ... 6
- Added Figure 4 ... 8
- Added Figure 9 ... 9
- Updated Figure 16 to include DDR3L data ... 10

Changes from Revision A (September 2015) to Revision B — **Page**

- Changed " –10 mA < I_{REFOUT} < 10 mA" to "–1 mA < I_{REFOUT} < 1 mA" in all test conditions for the *REFOUT voltage tolerance to V_{REFIN}* specification ... 7
- Changed all MIN and MAX values from "15" to "12" for all test conditions for the *REFOUT voltage tolerance to V_{REFIN}* specification ... 7
- Updated Figure 19 ... 12
- Added *REFOUT (V_{REF}) Consideration for DDR2 Applications* section ... 16
- Updated Figure 28 and Table 3 ... 21
- Added clarity to *Layout Guidelines* section. ... 27

Changes from Original (February 2008) to Revision A — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed “PowerPAD” references to “thermal pad” throughout ... 4

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- Deleted *Dissipation Ratings* table 5

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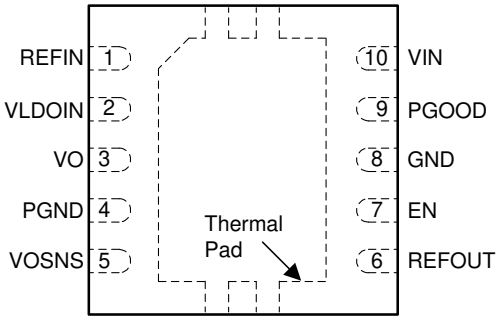
5 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	7	I	For DDR VTT application, connect EN to SLP_S3. For any other application, use the EN pin as the ON/OFF function.
GND	8	G	Signal ground.
PGND(2)	4	G	Power ground for the LDO.
PGOOD	9	O	Open-drain, power-good indicator.
REFIN	1	I	Reference input.
REFOUT	6	O	Reference output. Connect to GND through 0.1-μF ceramic capacitor. If there is a REFOUT capacitors at DDR side, keep total capacitance on REFOUT pin below 0.47 μF. The REFOUT pin can not be open.
VIN	10	I	2.5-V or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1-μF and 4.7-μF is required.
VLDOIN	2	I	Supply voltage for the LDO.
VO	3	O	Power output for the LDO.
VOSNS	5	I	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or the load.

(1) I = Input, O = Output , G = Ground
(2) Thermal pad connection. See Figure 35 in the *Thermal Design Considerations* section for additional information.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	REFIN, VIN, VLDOIN, VOSNS	–0.3	3.6	V
	EN	–0.3	6.5	
	PGND to GND	–0.3	0.3	
Output voltage (2)	REFOUT, VO	–0.3	3.6	V
	PGOOD	–0.3	6.5	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltages	VIN	2.375		3.500	V
Voltage	EN, VLDOIN, VOSNS	–0.1		3.5	V
	REFIN	0.5		1.8	
	PGOOD, VO	–0.1		3.5	
	REFOUT	–0.1		1.8	
	PGND	–0.1		0.1	
Operating free-air temperature, T_A		–40		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS51200 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over recommended free-air temperature range, V_{VIN} = 3.3 V, V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in Figure 24. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	Supply current	T_A = 25 °C, V_{EN} = 3.3 V, No Load		0.7	1	mA
$I_{IN(SDN)}$	Shutdown current	T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} = 0, No Load		65	80	µA
		T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} > 0.4 V, No Load		200	400	
I_{LDOIN}	Supply current of VLDOIN	T_A = 25 °C, V_{EN} = 3.3 V, No Load		1	50	µA
$I_{LDOIN(SDN)}$	Shutdown current of VLDOIN	T_A = 25 °C, V_{EN} = 0 V, No Load		0.1	50	µA
INPUT CURRENT						
I_{REFIN}	Input current, REFIN	V_{EN} = 3.3 V			1	µA
VO OUTPUT						
V_{VOSNS}	Output DC voltage, VO	V_{REFOUT} = 1.25 V (DDR1), I_O = 0 A		1.25		V
			–15		15	mV
		V_{REFOUT} = 0.9 V (DDR2), I_O = 0 A		0.9		V
			–15		15	mV
		V_{REFOUT} = 0.75 V (DDR3), I_O = 0 A		0.75		V
			–15		15	mV
		V_{REFOUT} = 0.675 V (DDR3L), I_O = 0 A		0.675		V
			–15		15	mV
		V_{REFOUT} = 0.6 V (DDR4), I_O = 0 A		0.6		V
			–15		15	mV
V_{VOTOL}	Output voltage tolerance to REFOUT	–2 A < I_{VO} < 2 A	–25		25	mV
I_{VOSRCL}	VO source current Limit	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}	3		4.5	A
I_{VOSNCL}	VO sink current Limit	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}	3.5		5.5	A
I_{DSCHRG}	Discharge current, VO	V_{REFIN} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V, T_A = 25°C		18	25	Ω
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	VO PGOOD threshold	PGOOD window lower threshold with respect to REFOUT	–23.5%	–20%	–17.5%	
		PGOOD window upper threshold with respect to REFOUT	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
$t_{PGSTUPDLY}$	PGOOD start-up delay	Start-up rising edge, VOSNS within 15% of REFOUT		2		ms
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA			0.4	V
$t_{PBADDLY}$	PGOOD bad delay	VOSNS is outside of the ±20% PGOOD window		10		µs
$I_{PGOODLK}$	Leakage current(1)	V_{OSNS} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{VIN} + 0.2 V			1	µA
REFIN AND REFOUT						
V_{REFIN}	REFIN voltage range		0.5		1.8	V
$V_{REFINUVLO}$	REFIN undervoltage lockout	REFIN rising	360	390	420	mV
$V_{REFINUVHYS}$	REFIN undervoltage lockout hysteresis			20		mV
V_{REFOUT}	REFOUT voltage			REFIN		V

(1) Ensured by design. Not production tested.

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Electrical Characteristics (continued)

Over recommended free-air temperature range, V_{VIN} = 3.3 V, V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in Figure 24. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REFOUTTOL}$	REFOUT voltage tolerance to V_{REFIN}	–1 mA < I_{REFOUT} < 1 mA, V_{REFIN} = 1.25 V	–12		12	mV
		–1 mA < I_{REFOUT} < 1 mA, V_{REFIN} = 0.9 V	–12		12	
		–1 mA < I_{REFOUT} < 1 mA, V_{REFIN} = 0.75 V	–12		12	
		–1 mA < I_{REFOUT} < 1 mA, V_{REFIN} = 0.675 V	–12		12	
		–1 mA < I_{REFOUT} < 1 mA, V_{REFIN} = 0.6 V	–12		12	
$I_{REFOUTSRCL}$	REFOUT source current limit	V_{REFOUT} = 0 V	10	40		mA
$I_{REFOUTSNCL}$	REFOUT sink current limit	V_{REFOUT} = 0 V	10	40		mA
UVLO AND EN LOGIC THRESHOLD						
$V_{VINUVVIN}$	UVLO threshold	Wake up, T_A = 25°C	2.2	2.3	2.375	V
		Hysteresis		50		mV
V_{ENIH}	High-level input voltage	Enable	1.7			V
V_{ENIL}	Low-level input voltage	Enable			0.3	
V_{ENYST}	Hysteresis voltage	Enable		0.5		
I_{ENLEAK}	Logic input leakage current	EN, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SON}	Thermal shutdown threshold(1)	Shutdown temperature		150		°C
		Hysteresis		25		

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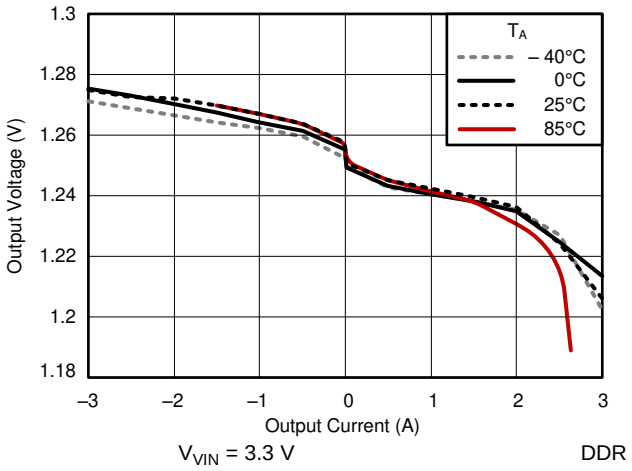
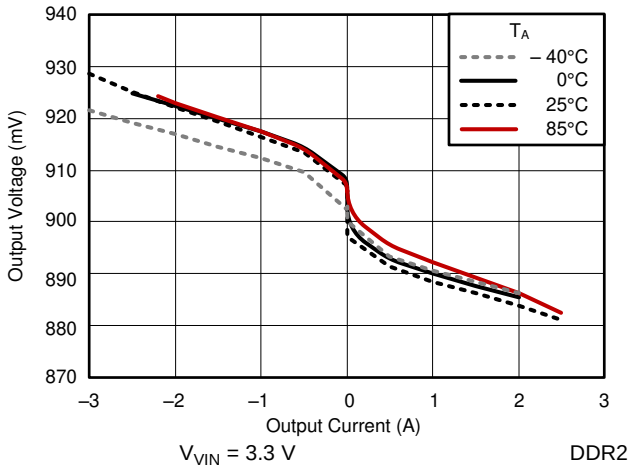
6.6 Typical Characteristics

3 × 10-µF MLCCs (0805) are used on the output



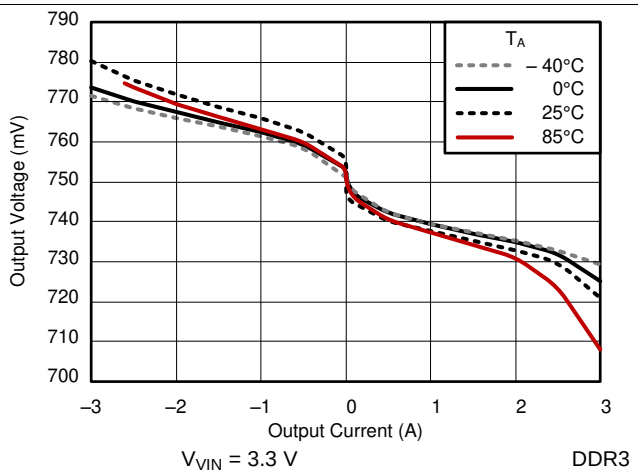
V_{VIN} = 3.3 V DDR

Figure 1. Load Regulation



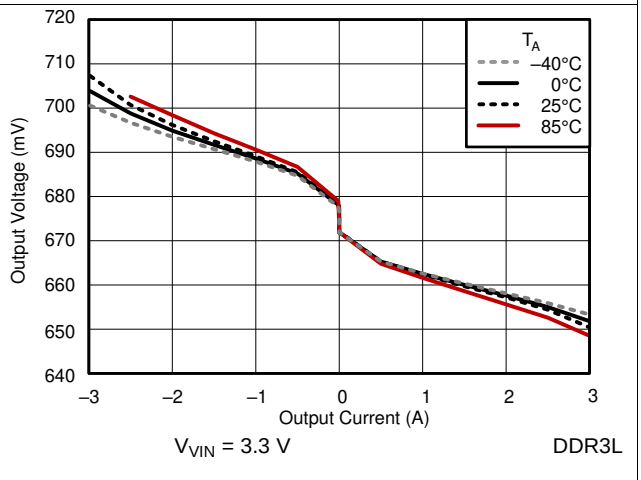
V_{VIN} = 3.3 V DDR2

Figure 2. Load Regulation



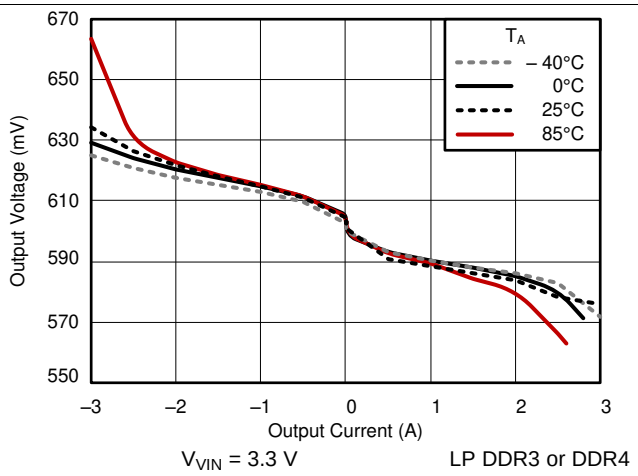
V_{VIN} = 3.3 V DDR3

Figure 3. Load Regulation



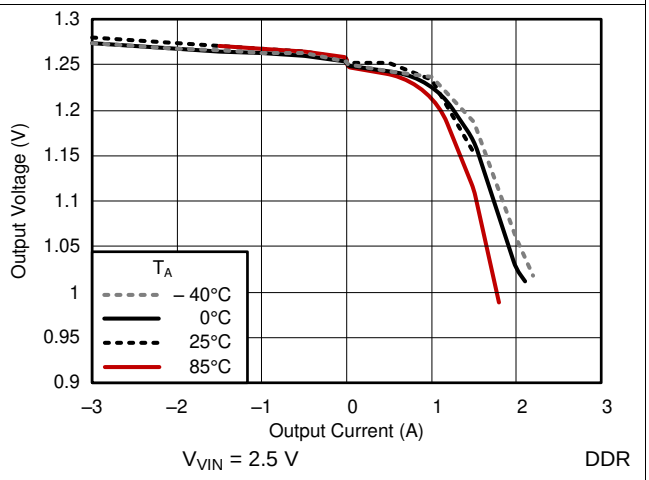
V_{VIN} = 3.3 V DDR3L

Figure 4. Load Regulation



V_{VIN} = 3.3 V LP DDR3 or DDR4

Figure 5. Load Regulation



V_{VIN} = 2.5 V DDR

Figure 6. Load Regulation

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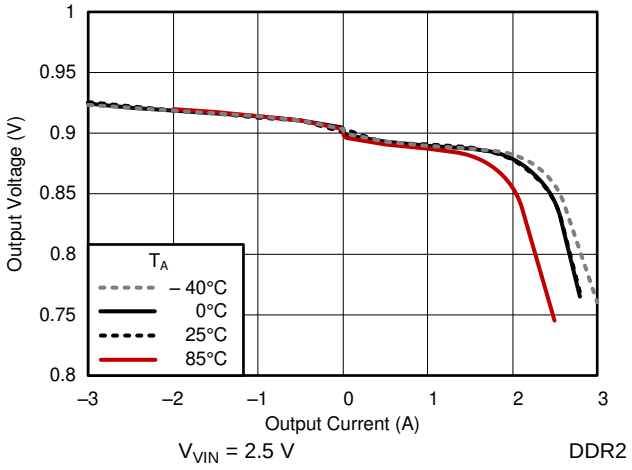
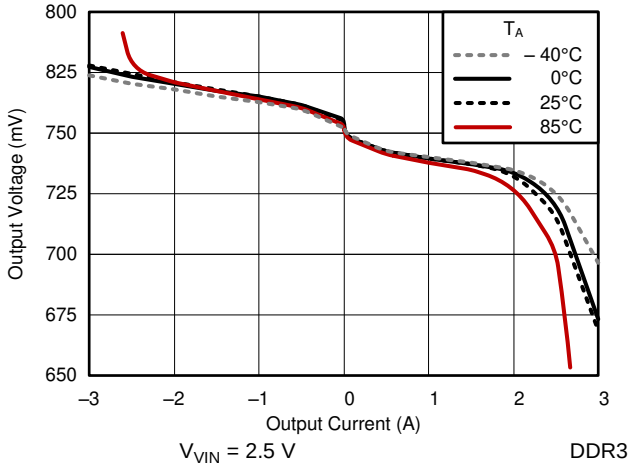
Typical Characteristics (continued)

3 × 10-µF MLCCs (0805) are used on the output



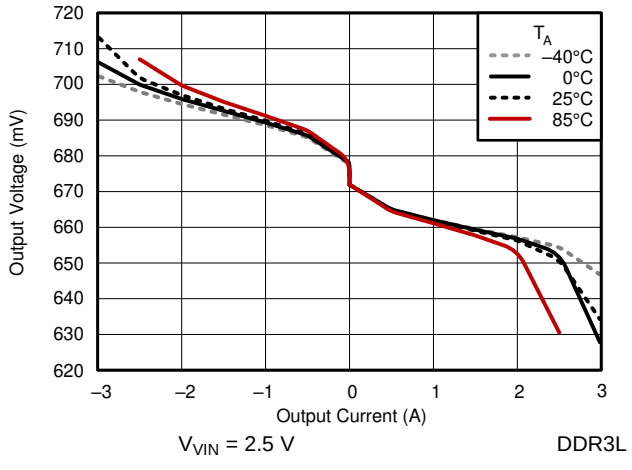
V_{VIN} = 2.5 V DDR2

Figure 7. Load Regulation



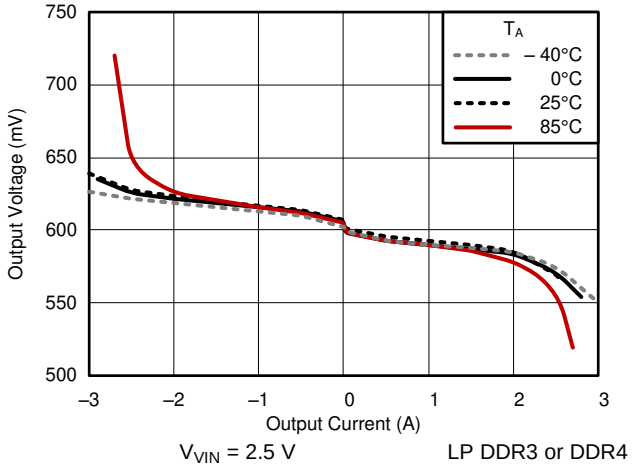
V_{VIN} = 2.5 V DDR3

Figure 8. Load Regulation



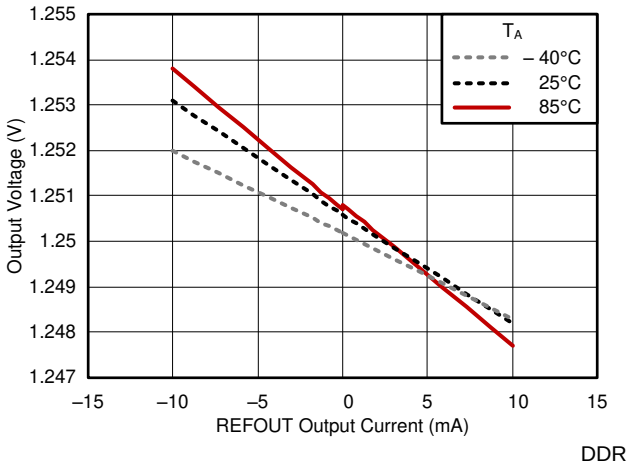
V_{VIN} = 2.5 V DDR3L

Figure 9. Load Regulation



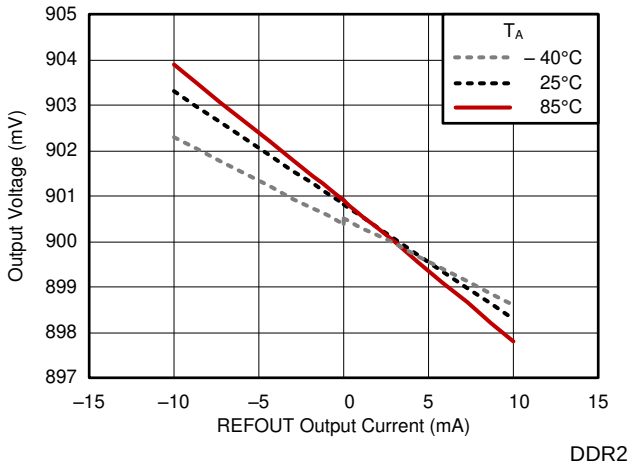
V_{VIN} = 2.5 V LP DDR3 or DDR4

Figure 10. Load Regulation



DDR

Figure 11. REFOUT Load Regulation



DDR2

Figure 12. REFOUT Load Regulation

Typical Characteristics (continued)

3 × 10-µF MLCCs (0805) are used on the output

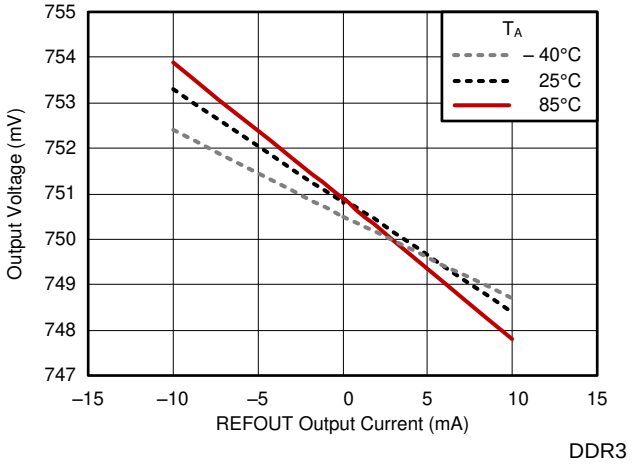


Figure 13. REFOUT Load Regulation

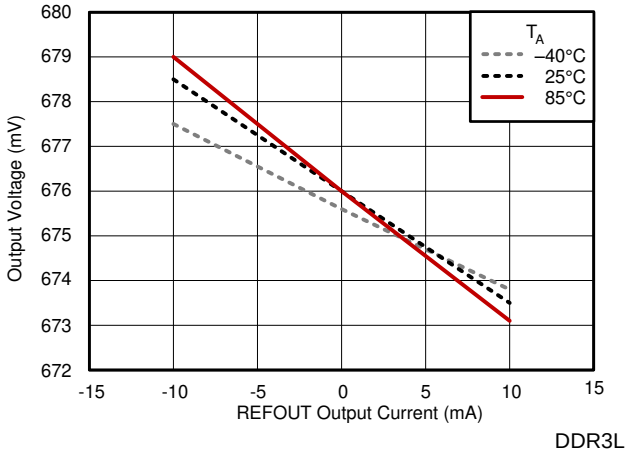


Figure 14. REFOUT Load Regulation

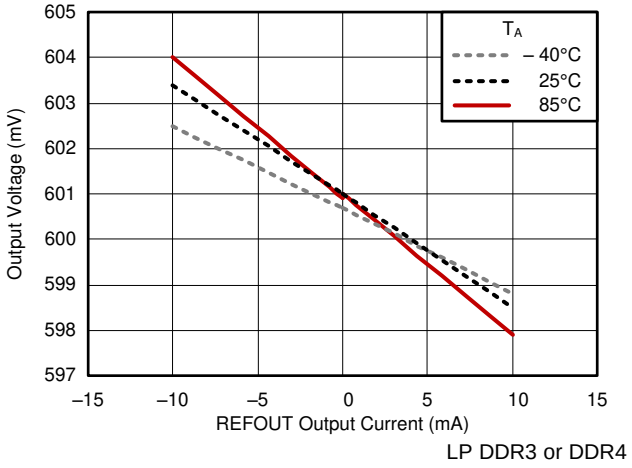


Figure 15. REFOUT Load Regulation

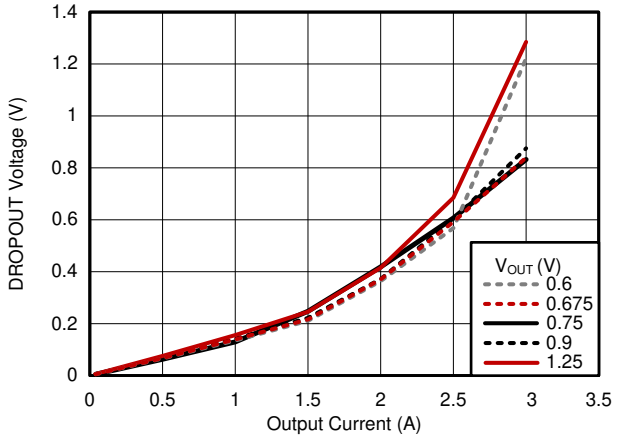


Figure 16. DROPOUT Voltage vs. Output Current

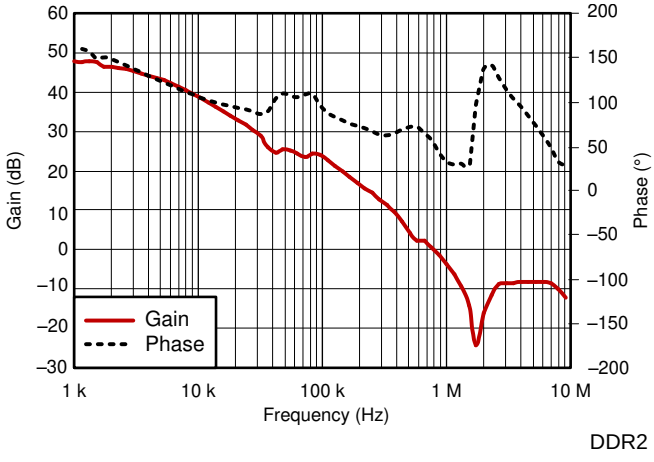


Figure 17. Bode Plot

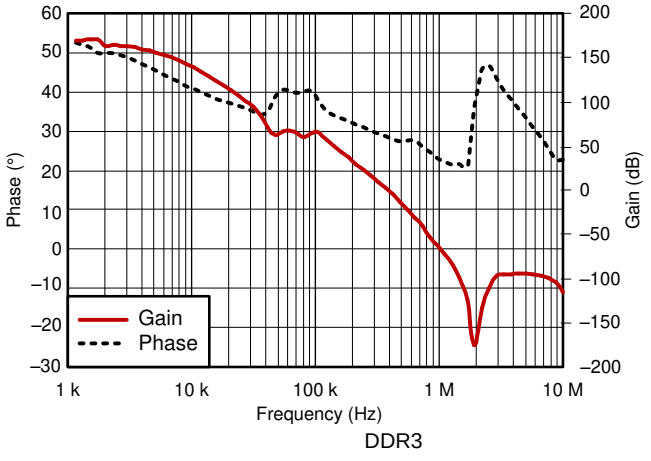


Figure 18. Bode Plot

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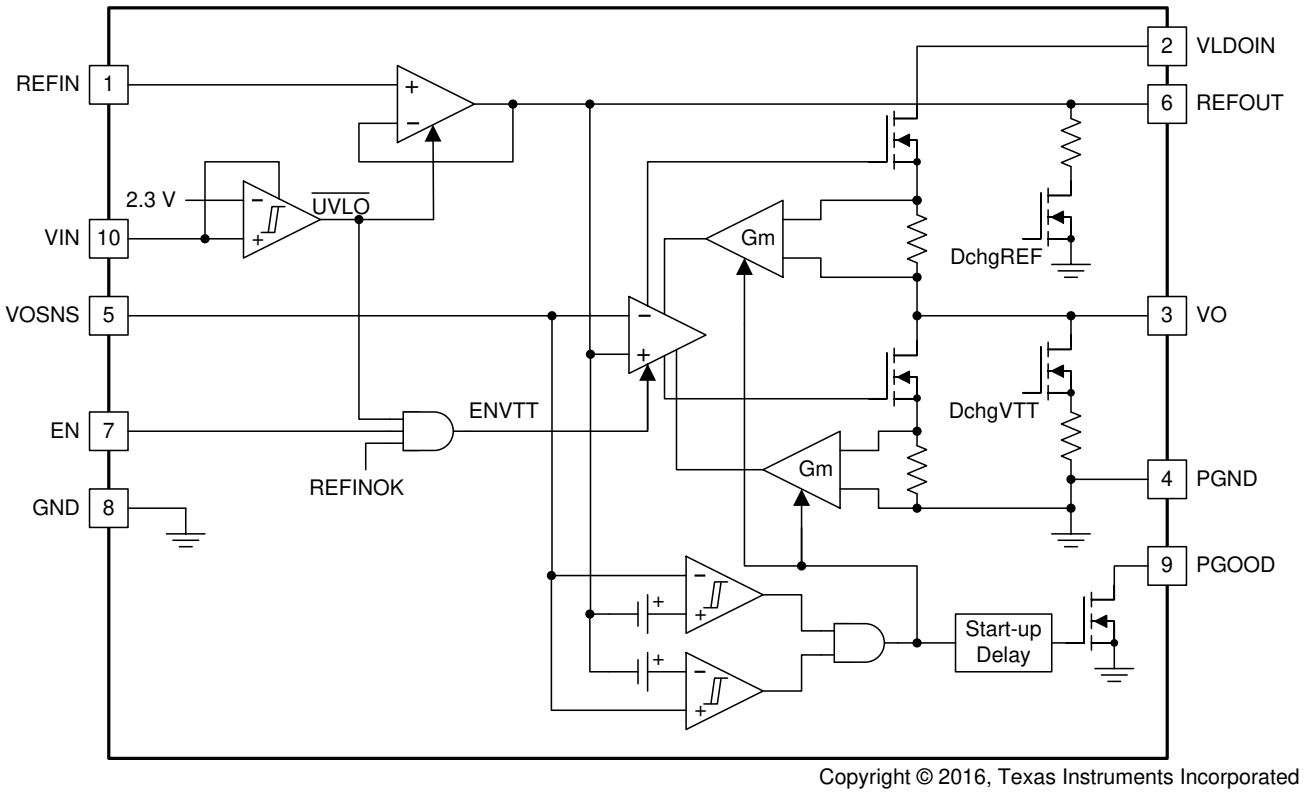
7 Detailed Description

7.1 Overview

The TPS51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The device maintains a fast transient response and only requires a minimum output capacitance of 20 μF. The device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 VTT bus termination.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Sink and Source Regulator (VO Pin)

The TPS51200 is a sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, connect a remote sensing terminal, VOSNS, to the positive terminal of each output capacitor as a separate trace from the high current path from VO.

7.3.2 Reference Input (REFIN Pin)

The output voltage, VO, is regulated to REFOUT. When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The TPS51200 device supports REFIN voltages from 0.5 V to 1.8 V, making it versatile and ideal for many types of low-power LDO applications.

Feature Description (continued)

7.3.3 Reference Output (REFOUT Pin)

When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA. REFOUT becomes active when REFIN voltage rises to 0.390 V and VIN is above the UVLO threshold. When REFOUT is less than 0.375 V, it is disabled and subsequently discharges to GND through an internal 10-kΩ MOSFET. REFOUT is independent of the EN pin state.

7.3.4 Soft-Start Sequencing

A current clamp implements the soft-start function of the VO pin. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When VO is outside of the powergood window, the current clamp level is one-half of the full overcurrent limit (OCL) level. When VO rises or falls within the PGOOD window, the current clamp level switches to the full OCL level. The soft-start function is completely symmetrical and the overcurrent limit works for both directions. The soft-start function works not only from GND to the REFOUT voltage, but also from VLDOIN to the REFOUT voltage.

7.3.5 Enable Control (EN Pin)

When EN is driven high, the VO regulator begins normal operation. When the device drives EN low, VO discharges to GND through an internal 18-Ω MOSFET. REFOUT remains on when the device drives EN low. Ensure that the EN pin voltage remains lower than or equal to V_{VIN} at all times.

7.3.6 Powergood Function (PGOOD Pin)

The TPS51200 device provides an open-drain PGOOD output that goes high when the VO output is within ±20% of REFOUT. PGOOD de-asserts within 10 μs after the output exceeds the size of the powergood window. During initial VO start-up, PGOOD asserts high 2 ms (typ) after the VO enters power good window. Because PGOOD is an open-drain output, a pull-up resistor with a value between 1 kΩ and 100 kΩ, placed between PGOOD and a stable active supply voltage rail is required.

7.3.7 Current Protection (VO Pin)

The LDO has a constant overcurrent limit (OCL). The OCL level reduces by one-half when the output voltage is not within the powergood window. This reduction is a non-latch protection.

7.3.8 UVLO Protection (VIN Pin)

For VIN undervoltage lockout (UVLO) protection, the TPS51200 monitors VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

7.3.9 Thermal Shutdown

The TPS51200 monitors junction temperature. If the device junction temperature exceeds the threshold value, (typically 150°C), the VO and REFOUT regulators both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

7.3.10 Tracking Start-up and Shutdown

The TPS51200 also supports tracking start-up and shutdown when the EN pin is tied directly to the system bus and not used to turn on or turn off the device. During tracking start-up, VO follows REFOUT once REFIN voltage is greater than 0.39 V. REFIN follows the rise of VDDQ rail through a voltage divider. The typical soft-start time (t_{SS}) for the VDDQ rail is approximately 3 ms, however it may vary depending on the system configuration. The soft-start time of the VO output no longer depends on the OCL setting, but it is a function of the soft-start time of the VDDQ rail. PGOOD is asserted 2 ms after V_{VO} is within ±20% of REFOUT. During tracking shutdown, the VO pin voltage falls following REFOUT until REFOUT reaches 0.37 V. When REFOUT falls below 0.37 V, the internal discharge MOSFETs turn on and quickly discharge both REFOUT and VO to GND. PGOOD is deasserted when VO is beyond the ±20% range of REFOUT. Figure 20 shows the typical timing diagram for an application that uses tracking start-up and shutdown.

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Feature Description (continued)

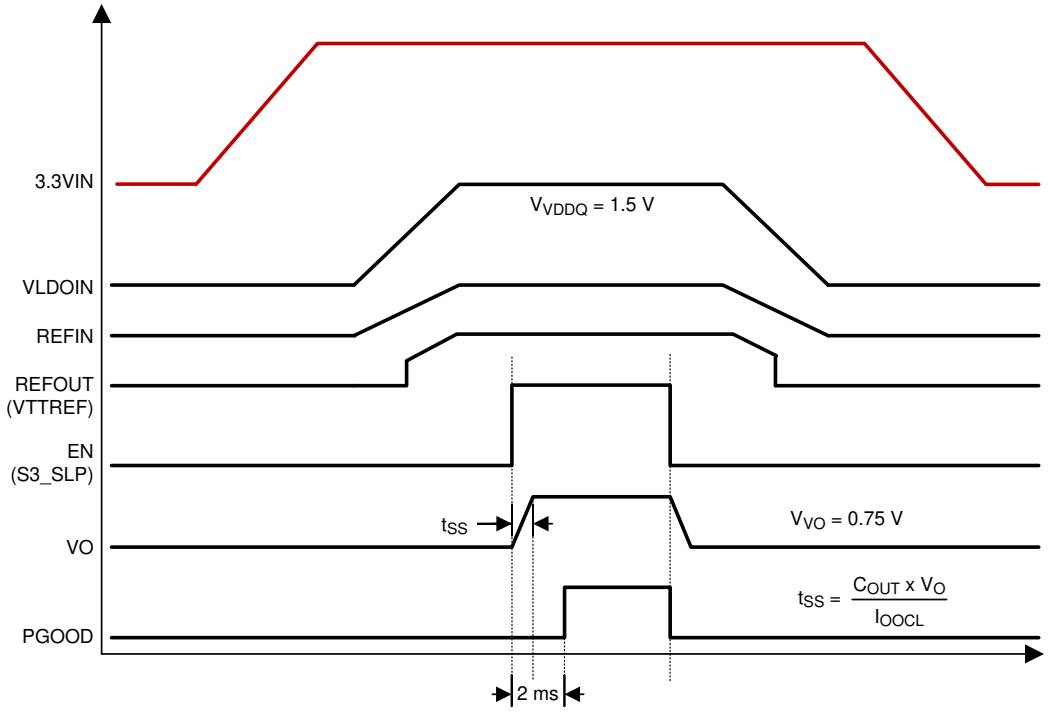

Figure 19. Typical Timing Diagram for S3 and Pseudo-S5 Support

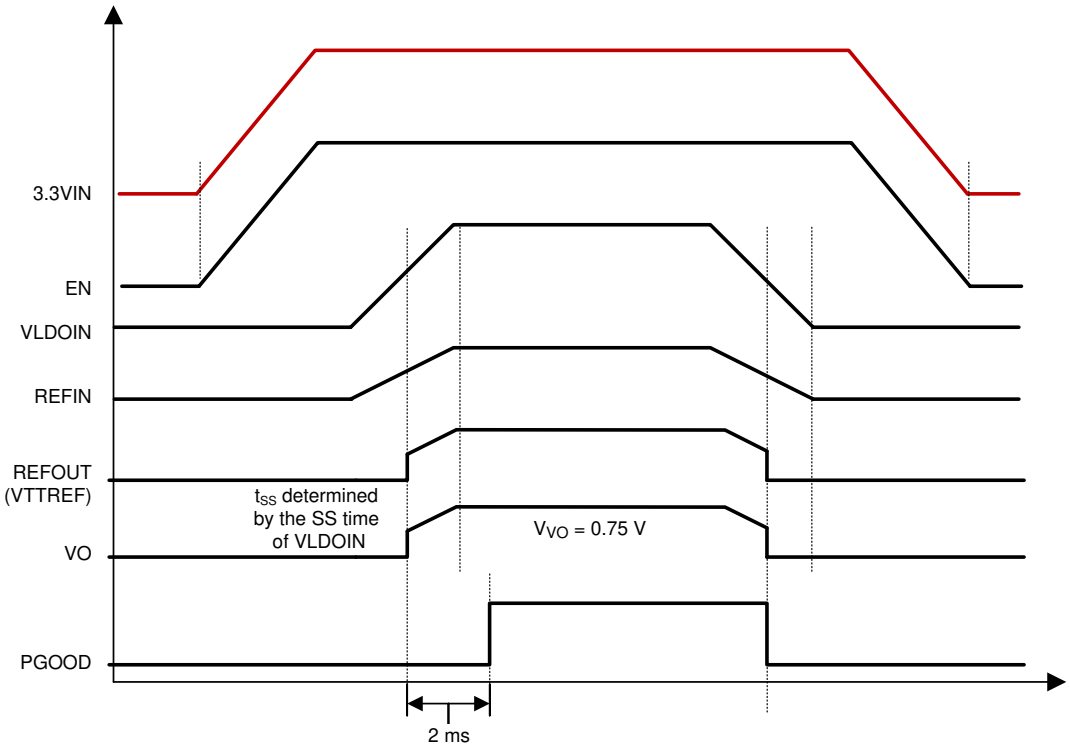

Figure 20. Typical Timing Diagram of Tracking Start-up and Shutdown

Feature Description (continued)

7.3.11 Output Tolerance Consideration for VTT DIMM Applications

The TPS51200 is specifically designed to power up the memory termination rail (as shown in Figure 21). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 22 for typical characteristics for a single memory cell.

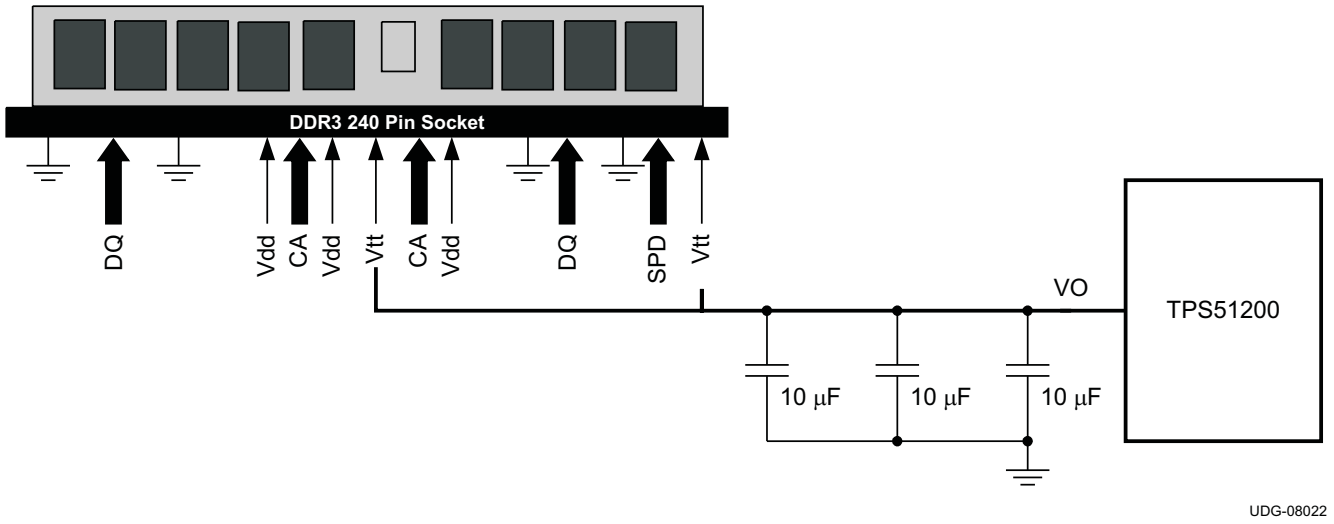

Figure 21. Typical Application Diagram for DDR3 VTT DIMM using TPS51200

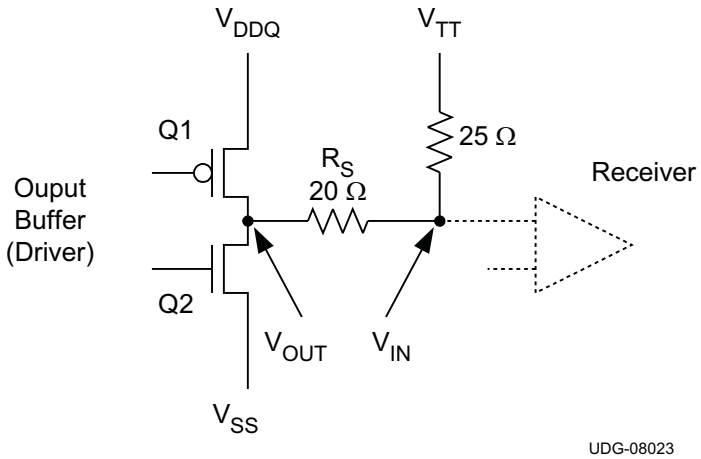

Figure 22. DDR Physical Signal System Bi-Directional SSTL Signaling

In Figure 22, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

In Figure 22, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND
- VTT sources current

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Feature Description (continued)

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Equation 1 applies to both DC and AC conditions and is based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

$$V_{VTTREF} - 40\ mV < V_{VTT} < V_{VTTREF} + 40\ mV \quad (1)$$

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS51200 ensures the regulator output voltage to be as shown in Equation 2, which applies to both DC and AC conditions.

$$V_{VTTREF} - 25\ mV < V_{VTT} < V_{VTTREF} + 25\ mV$$

where

- $-2\ A < I_{VTT} < 2\ A$ (2)

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3, DDR3L, Low Power DDR3, and DDR4 applications (see Table 1 for detailed information). To meet the stability requirement, a minimum output capacitance of 20 µF is needed. Considering the actual tolerance on the MLCC capacitors, three 10-µF ceramic capacitors sufficiently meet the VTT accuracy requirement.

Table 1. DDR, DDR2, DDR3 and LP DDR3 Termination Technology

	DDR	DDR2	DR3	LOW POWER DDR3
FSB Data Rates	200, 266, 333, and 400 MHz	400, 533, 677, and 800 MHz	800, 1066, 1330, and 1600 MHz	
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	
Termination Current Demand	Maximum source/sink transient currents of up to 2.6 A to 2.9 A	Not as demanding	Not as demanding	
		Only 34 signals (address, command, control) tied to VTT	Only 34 signals (address, command, control) tied to VTT	
		ODT handles data signals	ODT handles data signals	
		Less than 1-A of burst current	Less than 1-A of burst current	
Voltage Level	2.5-V Core and I/O 1.25-V VTT	1.8-V Core and I/O 0.9-V VTT	1.5-V Core and I/O 0.75-V VTT	1.2-V Core and I/O 0.6-V VTT

The TPS51200 uses transconductance (g_M) to drive the LDO. The transconductance and output current of the device determine the voltage droop between the reference input and the output regulator. The typical transconductance level is 250 S at 2 A and changes with respect to the load in order to conserve the quiescent current (that is, the transconductance is very low at no load condition). The (g_M) LDO regulator is a single pole system. Only the output capacitance determines the unity gain bandwidth for the voltage loop, as a result of the bandwidth nature of the transconductance (see Equation 3).

$$f_{UGBW} = \frac{g_M}{2 \times \pi \times C_{OUT}}$$

where

- f_{UGBW} is the unity gain bandwidth
- g_M is transconductance
- C_{OUT} is the output capacitance (3)

Consider these two limitations to this type of regulator that come from the output bulk capacitor requirement. In order to maintain stability, the zero location contributed by the ESR of the output capacitors must be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the transconductance (g_M) –3-dB point because of the large ESL, the output capacitor and parasitic inductance of the VO pin voltage trace.

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7.3.12 REFOUT (V_{REF}) Consideration for DDR2 Applications

During TPS51200 tracking start-up, the REFIN voltage follows the rise of the VDDQ rail through a voltage divider, and REFOUT (V_{REF}) follows REFIN once the REFIN voltage is greater than 0.39 V. When the REFIN voltage is lower than 0.39 V, V_{REF} is 0 V.

The JEDEC *DDR2 SDRAM Standard* (JESD79-2E) states that V_{REF} must track VDDQ/2 within ±0.3 V accuracy during the start-up period. To allow the TPS51200

device to meet the JEDEC DDR2 specification, a resistor divider can be used to provide the V_{REF} signal to the DIMM. The resistor divider ratio is 0.5 to ensure that the V_{REF} voltage equals VDDQ/2.

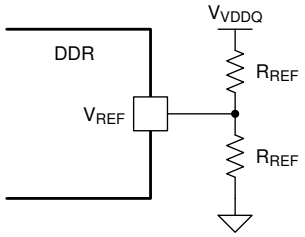

Figure 23. Resistor Divider Circuit

When selecting the resistor value, consider the impact of the leakage current from the DIMM V_{REF} pin on the reference voltage. Use Equation 4 to calculate resistor values.

$$R_{REF} \leq \frac{2 \times \Delta V_{REF}}{I_{REF}} \quad (4)$$

where

- R_{REF} is the resistor value
- ΔV_{REF} is the V_{REF} DC variation requirement
- I_{REF} is the maximum total V_{REF} leakage current from DIMMs

Consider the MT47H64M16 DDR2 SDRAM component from Micron as an example. The MT47H64M16 datasheet shows the maximum V_{REF} leakage current of each DIMM is ±2 µA, and $V_{REF(DC)}$ variation must be within ±1% of VDDQ. In this DDR2 application, the VDDQ voltage is 1.8 V. Assuming one TPS51200 device needs to power 4 DIMMs, the maximum total V_{REF} leakage current is ±8 µA. Based on the calculations, the resistor value should be lower than 4.5 kΩ. To ensure sufficient margin, 100 Ω is the suggested resistor value. With two 100-Ω resistors, the maximum V_{REF} variation is 0.4 mV, and the power loss on each resistor is 8.1 mW.

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7.4 Device Functional Modes

7.4.1 Low Input Voltage Applications

TPS51200 can be used in an application system that offers either a 2.5-V rail or a 3.3-V rail. If only a 5-V rail is available, consider using the TPS51100 device as an alternative. The TPS51200 device has a minimum input voltage requirement of 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

7.4.2 S3 and Pseudo-S5 Support

The TPS51200 provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both REFOUT and VO are on when EN = high (S0 state). REFOUT is maintained while VO is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). When EN = low and the REFIN voltage is less than 0.390 V, TPS51200 enters pseudo-S5 state. Both VO and REFOUT outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4 or S5 state). Figure 19 shows a typical start-up and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

This design example describes a 3.3-V_{IN}, DDR3 configuration.

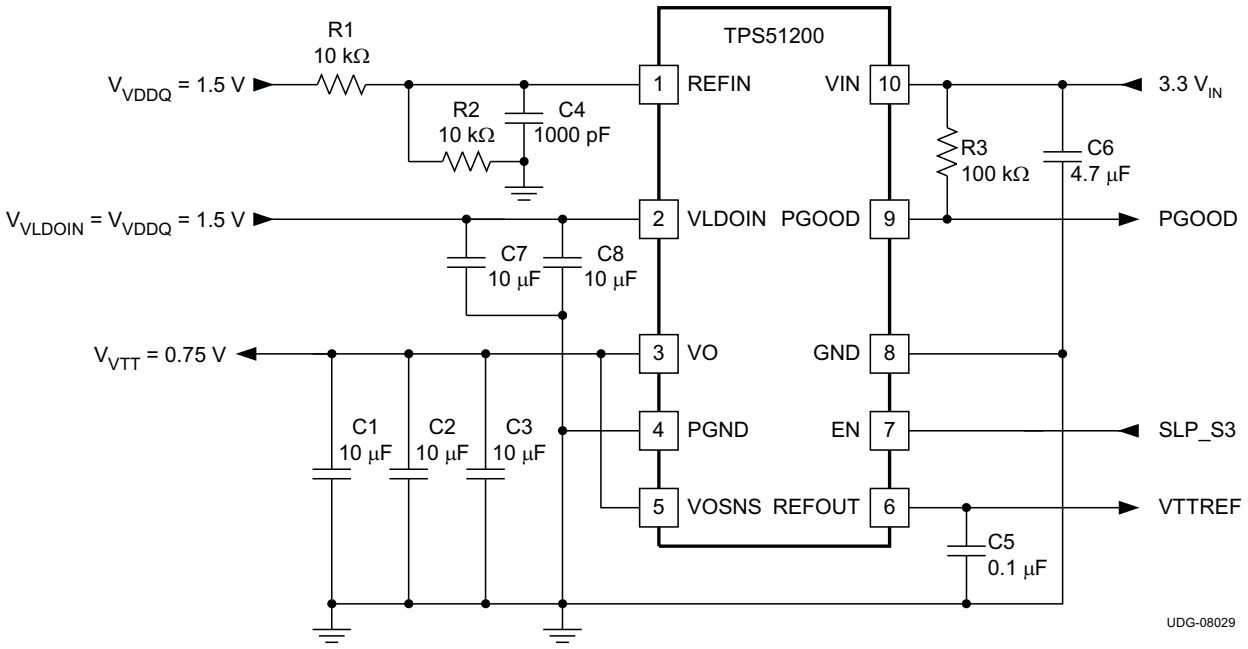

Figure 24. 3.3-V_{IN}, DDR3 Configuration

Table 2. 3.3-V_{IN}, DDR3 Application List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.2.1 Design Requirements

- V_{IN} = 3.3 V
- V_{DDDQ} = 1.5 V
- V_{VLDOIN} = V_{VDDQ} = 1.5 V
- V_{VTT} = 0.75 V

8.2.2 Detailed Design Procedure

8.2.2.1 Input Voltage Capacitor

Add a ceramic capacitor, with a value between 1.0-μF and 4.7-μF, placed close to the VIN pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

8.2.2.2 VLDO Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-μF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at the VO pin. In general, use one-half of the C_{OUT} value for input.

8.2.2.3 Output Capacitor

For stable operation, the total capacitance of the VO output pin must be greater than 20 μF. Attach three, 10-μF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an RC filter between the output and the VOSNS input to achieve loop stability. The RC filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

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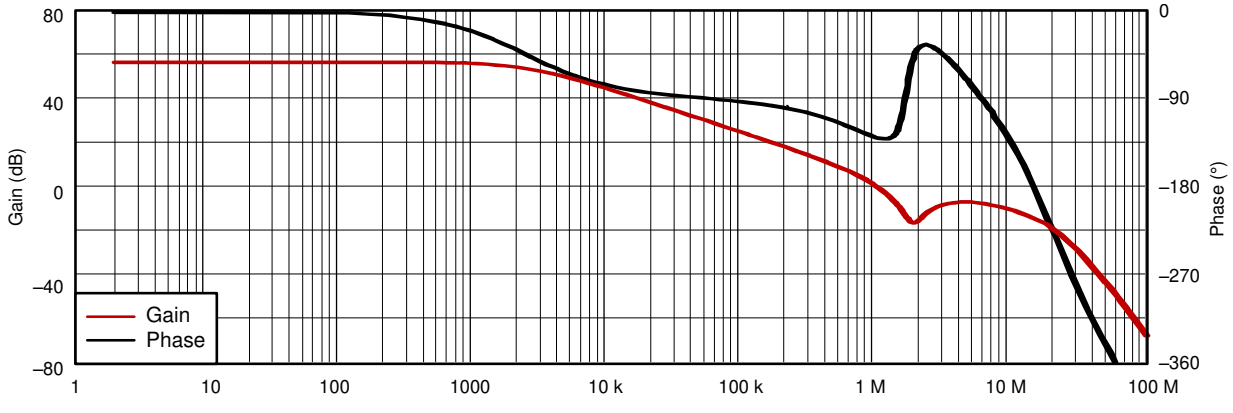
8.2.3 Application Curves

Figure 25 shows the bode plot simulation for this DDR3 design example of the TPS51200 device.

The unity-gain bandwidth is approximately 1 MHz and the phase margin is 52°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking maintains a level well below 0 dB.

Figure 26 shows the load regulation and Figure 27 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to ±1.5-A load step and release, the output voltage measurement shows no difference between the dc and ac conditions.

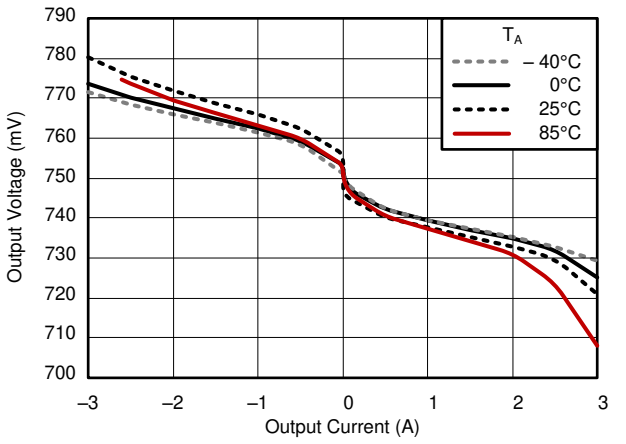


V_{IN} = 3.3 V
I_{IO} = 2 A

V_{VLDOIN} = 1.5 V
3 × 10-µF capacitors

V_{VO} = 0.75 V
ESR = 2.5 mΩ
ESL = 800 pH

Figure 25. DDR3 Design Example Bode Plot



V_{VIN} = 3.3 V

DDR3

Figure 26. Load Regulation

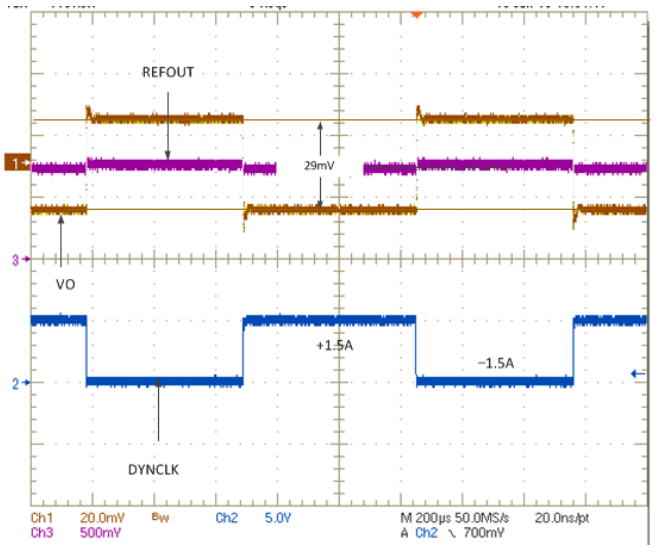


Figure 27. Transient Waveform

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8.3 System Examples

8.3.1 3.3-V_{IN}, DDR2 Configuration

This section describes a 3.3-V_{IN}, DDR2 configuration application.

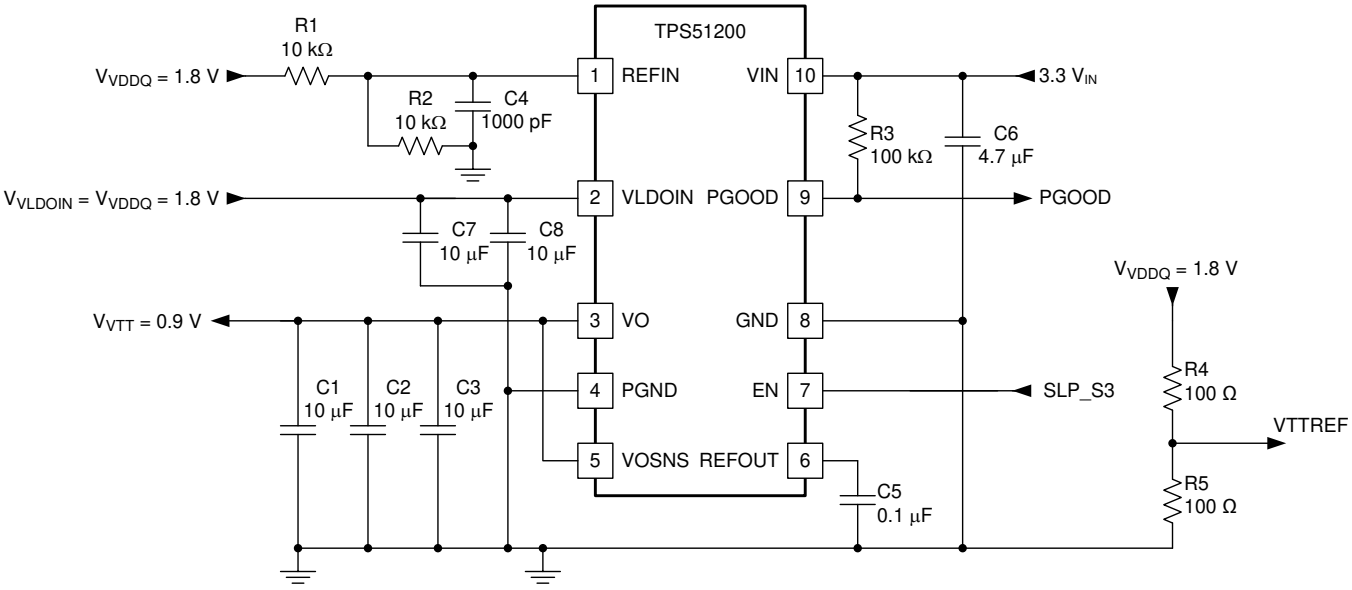

Figure 28. 3.3-V_{IN}, DDR2 Configuration

Table 3. 3.3-V_{IN}, DDR2 Configuration List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
R4, R5		100 Ω		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.3.2 2.5-V_{IN}, DDR3 Configuration

This design example describes a 2.5-V_{IN}, DDR3 configuration application.

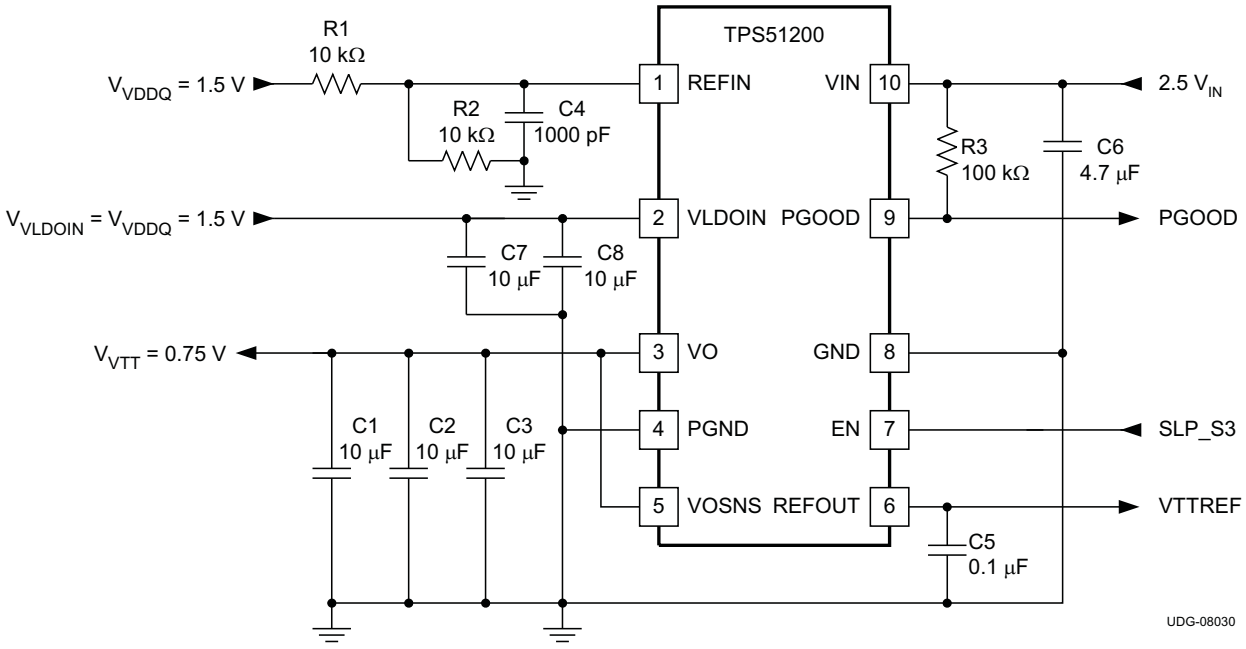

Figure 29. 2.5-V_{IN}, DDR3 Configuration

Table 4. 2.5-V_{IN}, DDR3 Configuration List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.3.3 3.3-V_{IN}, LP DDR3 or DDR4 Configuration

This example describes a 3.3-V_{IN}, LP DDR3 or DDR4 configuration application.

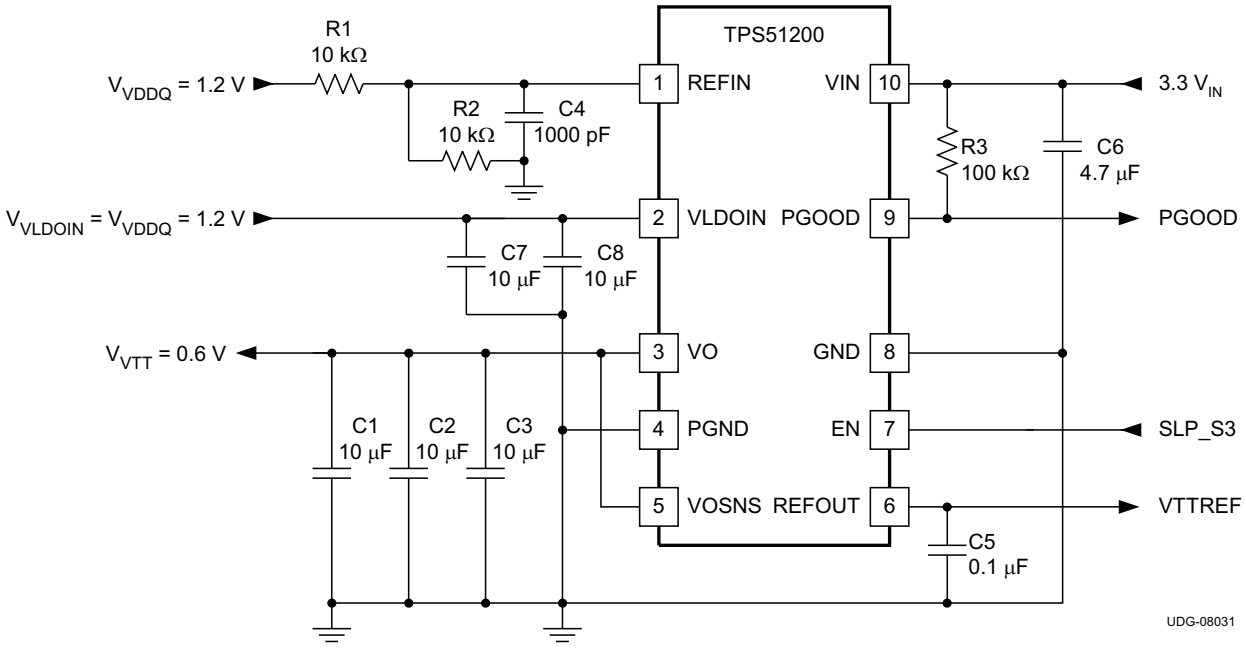

Figure 30. 3.3-V_{IN}, LP DDR3 or DDR4 Configuration

Table 5. 3.3-V_{IN}, LP DDR3 or DDR4 Configuration

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.3.4 3.3-V_{IN}, DDR3 Tracking Configuration

This design example describes a 3.3-V_{IN}, DDR3 tracking configuration application.

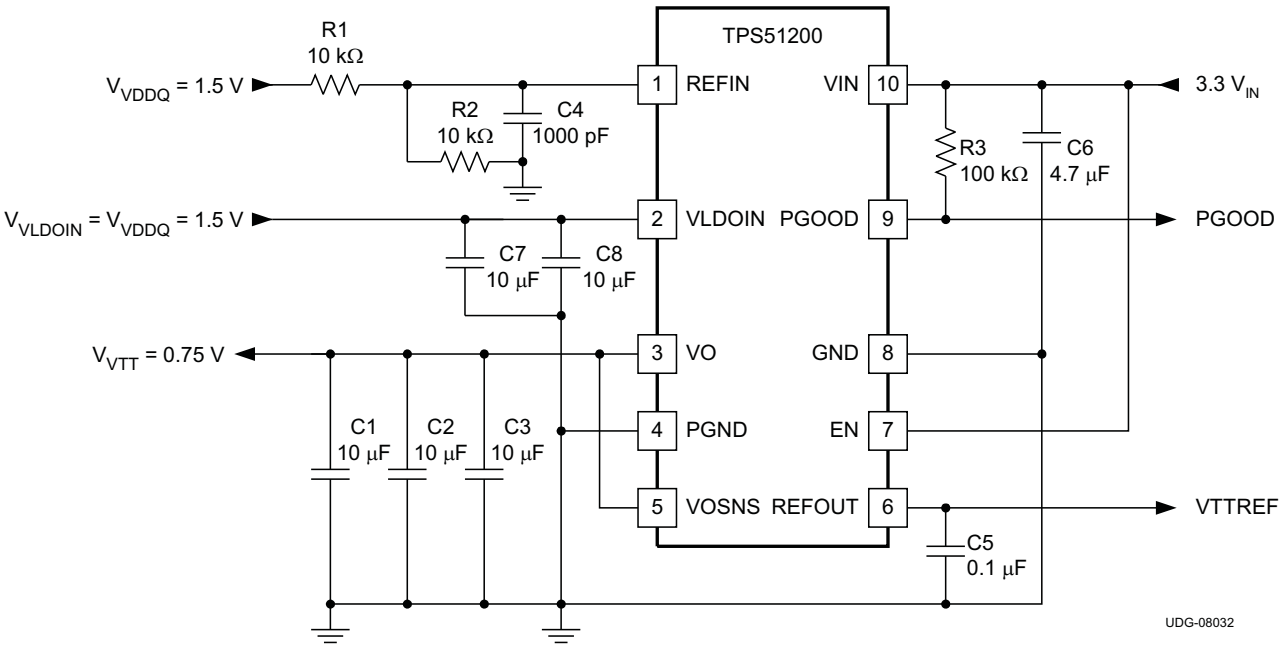

Figure 31. 3.3-V_{IN}, DDR3 Tracking Configuration

Table 6. 3.3-V_{IN}, DDR3 Tracking Configuration List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.3.5 3.3-V_{IN}, LDO Configuration

This example describes a 3.3-V_{IN}, LDO configuration application.

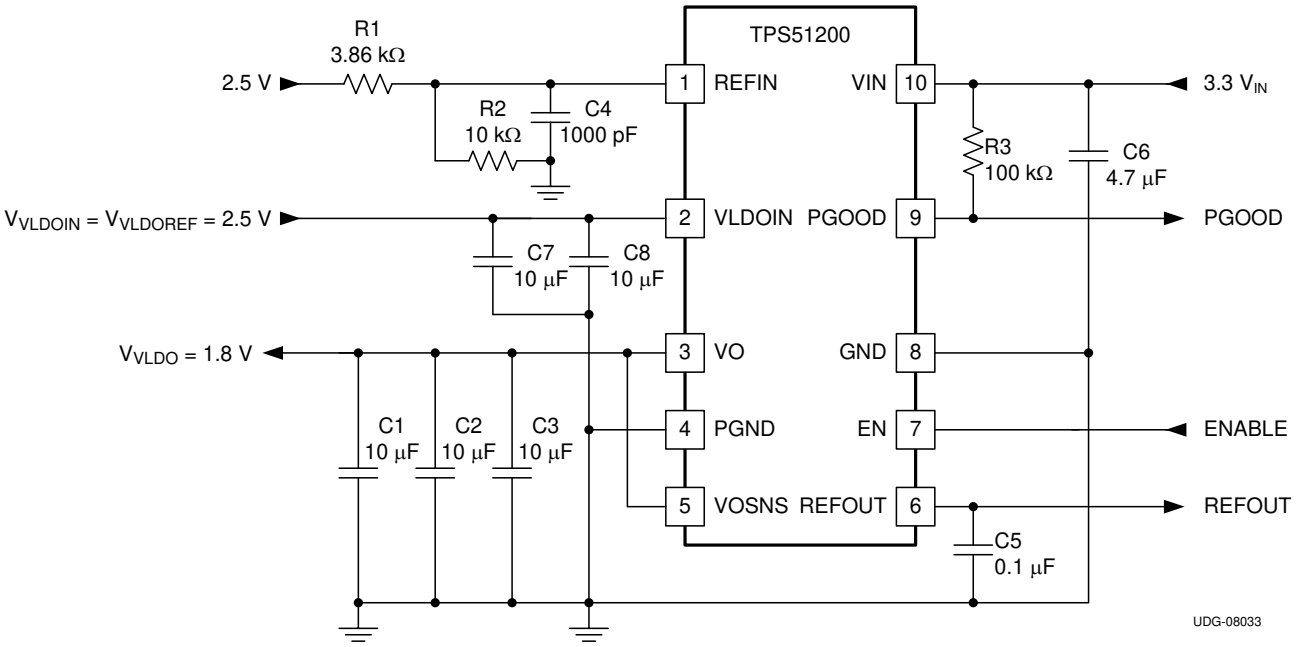

Figure 32. 3.3-V_{IN}, LDO Configuration

Table 7. 3.3-V_{IN}, LDO Configuration List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	3.86 kΩ		
R2		10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

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8.3.6 3.3-V_{IN}, DDR3 Configuration with LFP

This design example describes a 3.3-V_{IN}, DDR3 configuration with LFP application.

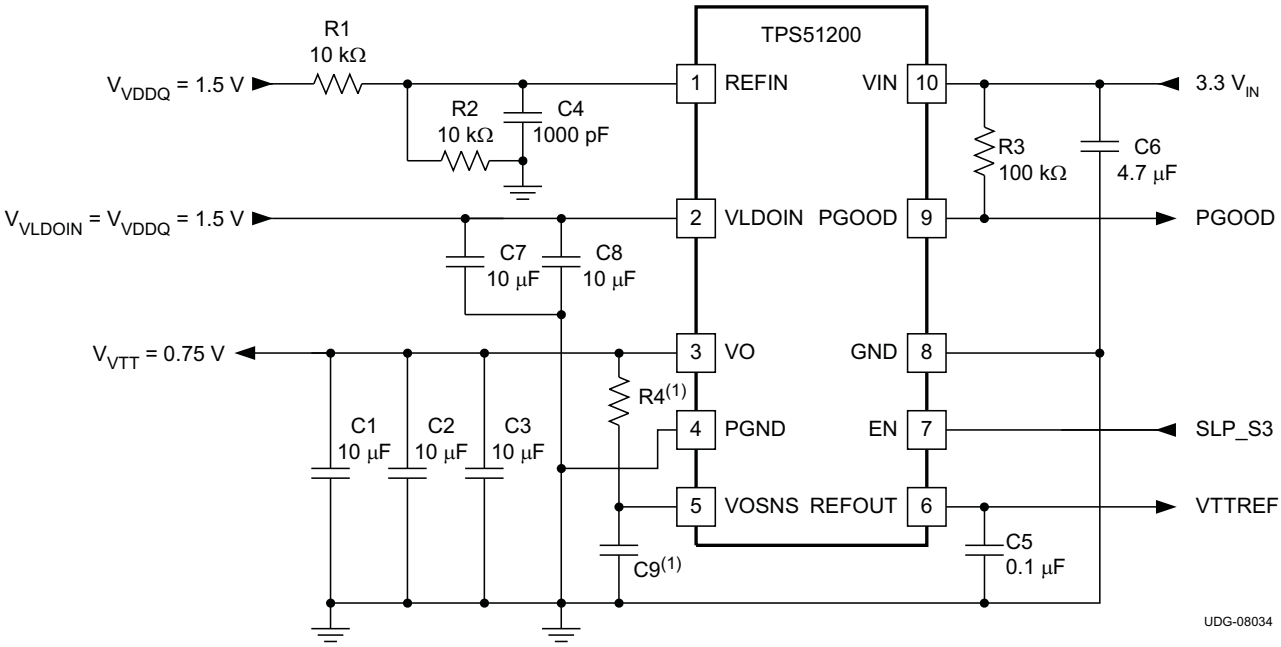

Figure 33. 3.3-V_{IN}, DDR3 Configuration with LFP

Table 8. 3.3-V_{IN}, DDR3 Configuration with LFP List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
R4(1)				
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C9(1)				

(1) Choose values for R4 and C9 to reduce the parasitic effect of the trace (between VO and the output MLCCs) and the output capacitors (ESR and ESL).

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9 Power Supply Recommendations

This device is designed to operate from an input bias voltage from 2.375 V to 3.5 V, with LDO input from 1.1 V to 3.5 V. Refer to Figure 19 and Figure 20 for recommended power-up sequence. Maintain a EN voltage equal or lower than V_{VIN} at all times. VLDOIN can ramp up earlier than VIN if the sequence in Figure 19 and Figure 20 cannot be used. The input supplies should be well regulated. VLDOIN decoupling capacitance of 2 × 10 µF is recommended, and VIN decoupling capacitance of 1 × 4.7 µF is recommended.

10 Layout

10.1 Layout Guidelines

Consider the following points before starting the TPS51200 device layout design.

- Place the input capacitors as close to VDLOIN pin as possible with short and wide connection.
- Place the output capacitor as close to VO pin as possible with short and wide connection. Place a ceramic capacitor with a value of at least 10-µF as close to VO pin if the rest of output capacitors need to be placed on the load side.
- Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VO sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.
- Consider adding low-pass filter at VOSNS if the VO sense trace is very long.
- Connect the GND pin and PGND pin to the thermal pad directly.
- TPS51200 uses its thermal pad to dissipate heat. In order to effectively remove heat fromTPS51200 package, place numerous ground vias on the thermal pad. Use large ground copper plane, especially the copper plane on surface layer, to pour over those vias on thermal pad.
- Consult the TPS51200EVM User's Guide (SLUU323) for detailed layout recommendations.

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10.2 Layout Example

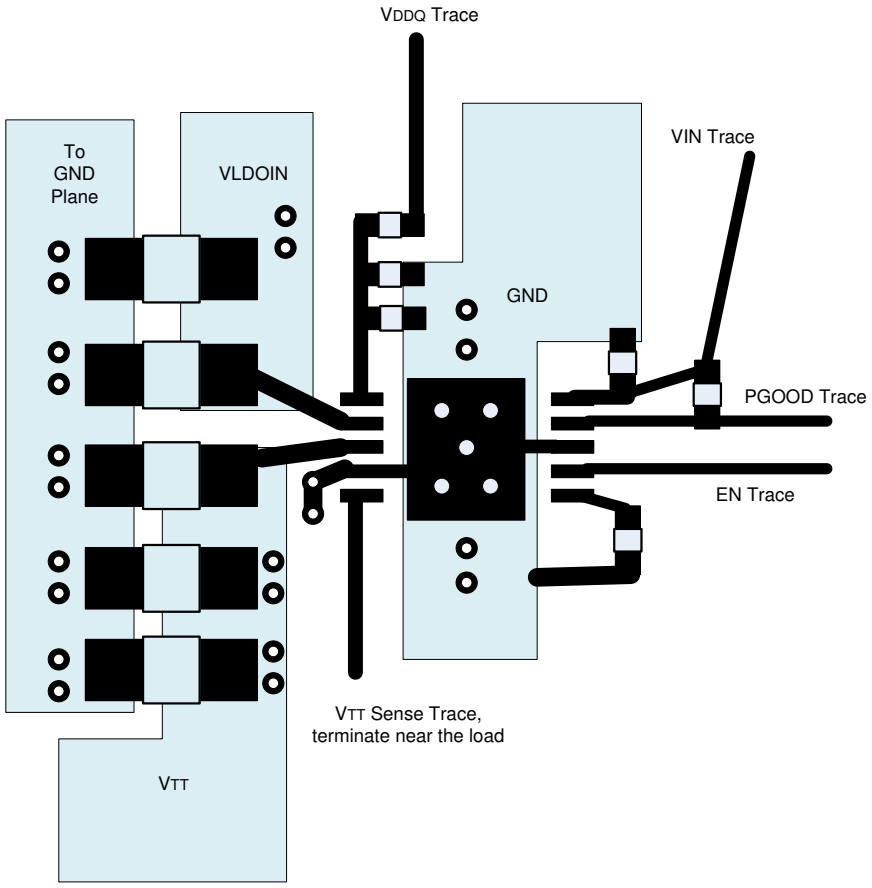

Figure 34. Layout Recommendation

10.3 Thermal Design Considerations

Because the TPS51200 is a linear regulator, the VO current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference shown in Equation 5 calculates the power dissipation.

$$P_{D_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O_SRC} \quad (5)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the V_{DDQ} voltage, overall power loss can be reduced. During the sink phase, the device applies the VO voltage across the internal LDO regulator. Equation 6 calculates he power dissipation, P_{D_SNK} can be calculated by .

$$P_{D_SNK} = V_{VO} \times I_{SNK} \quad (6)$$

Because the device does not sink and source current at the same time and the I/O current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. The current used for the internal current control circuitry from the VIN supply and the VLDOIN supply are other sources of power consumption. This power can be estimated as 5 mW or less during normal operating conditions and must be effectively dissipated from the package.

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Thermal Design Considerations (continued)

Maximum power dissipation allowed by the package is calculated by Equation 7.

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \quad (7)$$

where

- $T_{J(max)}$ is 125°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from junction to ambient

NOTE

Because Equation 7 demonstrates the effects of heat spreading in the ground plane, use it as a guideline only. Do not use Equation 7 to estimate actual thermal performance in real application environments.

In an application where the device is mounted on PCB, TI strongly recommends using ψ_{JT} and ψ_{JB}, as explained in the section pertaining to estimating junction temperature in the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953. Using the thermal metrics ψ_{JT} and ψ_{JB}, as shown in the *Thermal Information* table, estimate the junction temperature with corresponding formulas shown in Equation 8. The older θ_{JC} top parameter specification is listed as well for the convenience of backward compatibility.

$$T_J = T_T + \Psi_{JT} \times P_D \quad (8)$$

$$T_J = T_B + \Psi_{JB} \times P_D \quad (9)$$

where

- P_D is the power dissipation shown in Equation 5 and Equation 6
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1-mm away from the thermal pad package on the PCB surface (see Figure 36).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer). For more information about measuring T_T and T_B, see the application report *Using New Thermal Metrics* (SBVA025).

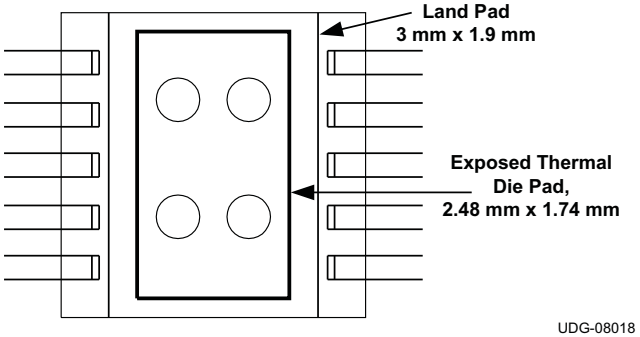

Figure 35. Recommended Land Pad Pattern

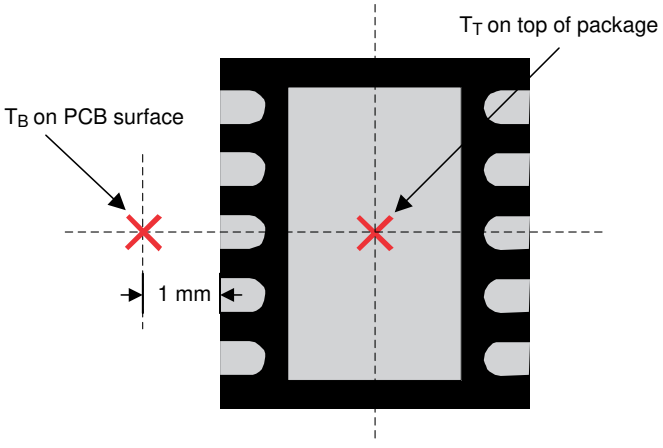

Figure 36. Package Thermal Measurement

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

11.1.2.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS51200 device. The TPS51200EVM evaluation module and related user's guide (SLUU323) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS51200 device is available here.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *Semiconductor and IC Package Thermal Metrics*, SPRA953
- *Using the TPS51200 EVM Sink/Source DDR Termination Regulator*, SLUU323
- For more information on the TPS51100 device, see the product folder on ti.com.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51200DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	Samples
TPS51200DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	Samples
TPS51200DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	Samples
TPS51200DRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1200	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS51200 :

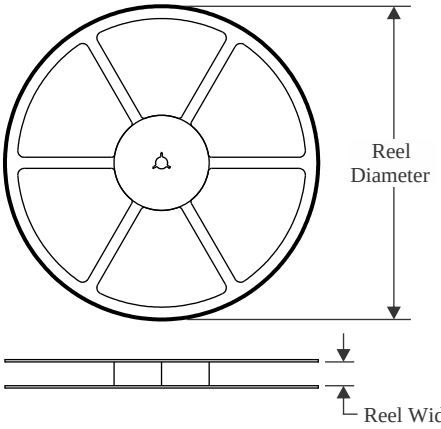
- Automotive: TPS51200-Q1
- Enhanced Product: TPS51200-EP

NOTE: Qualified Version Definitions:

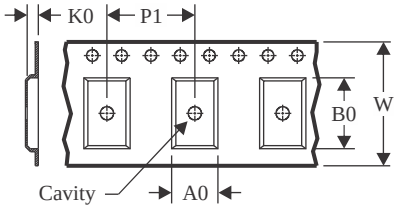
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

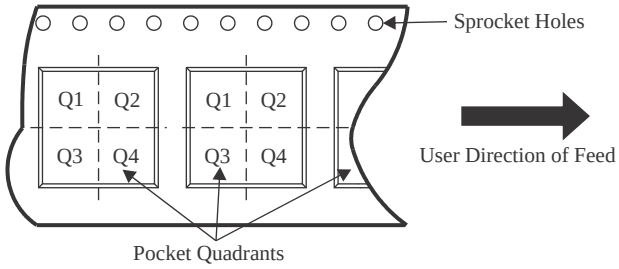


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

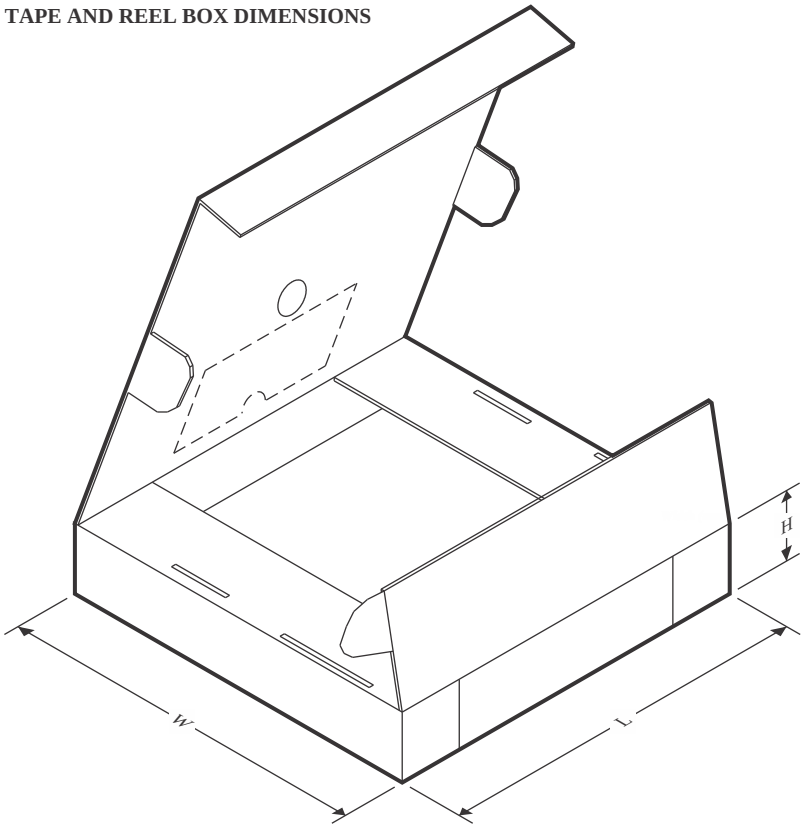
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51200DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51200DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51200DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS51200DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

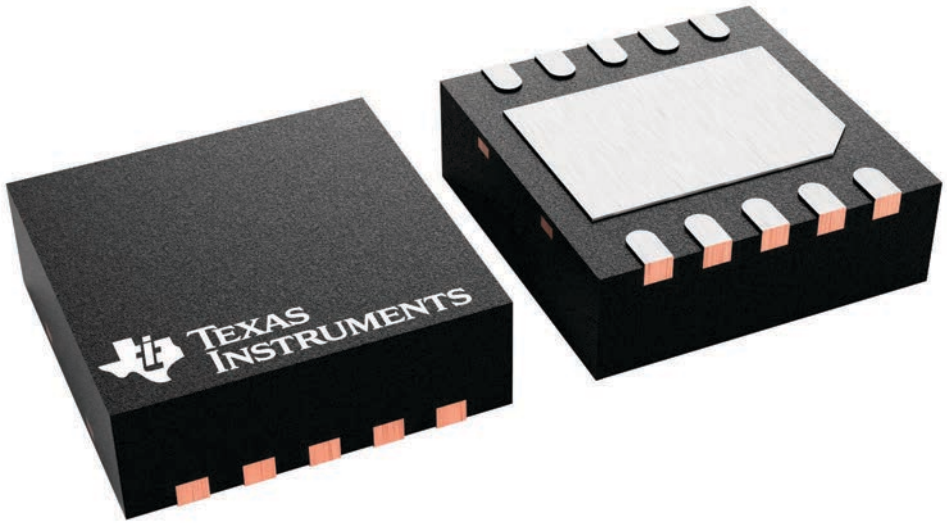
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



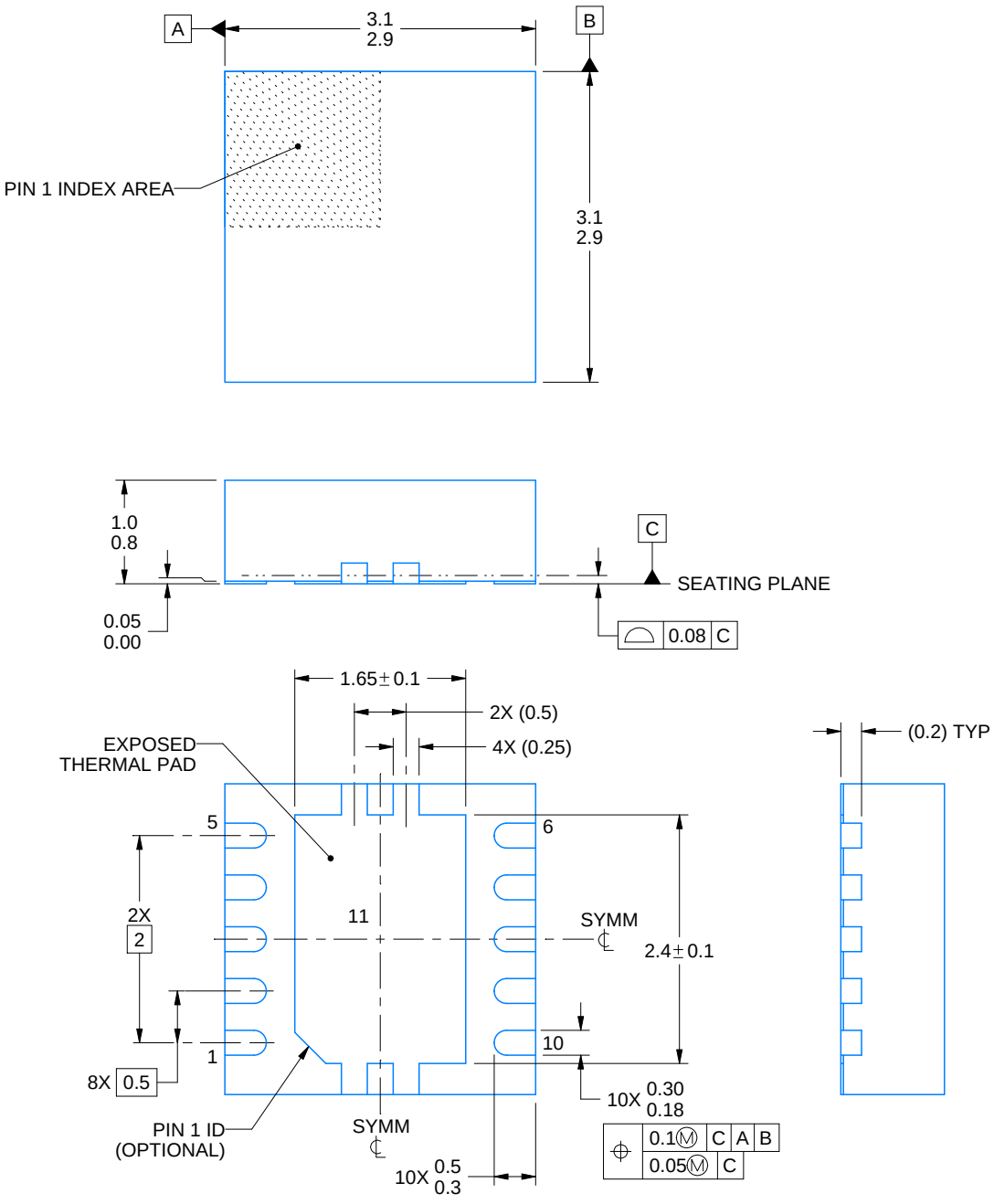
4226193/A

DRC0010J

PACKAGE OUTLINE

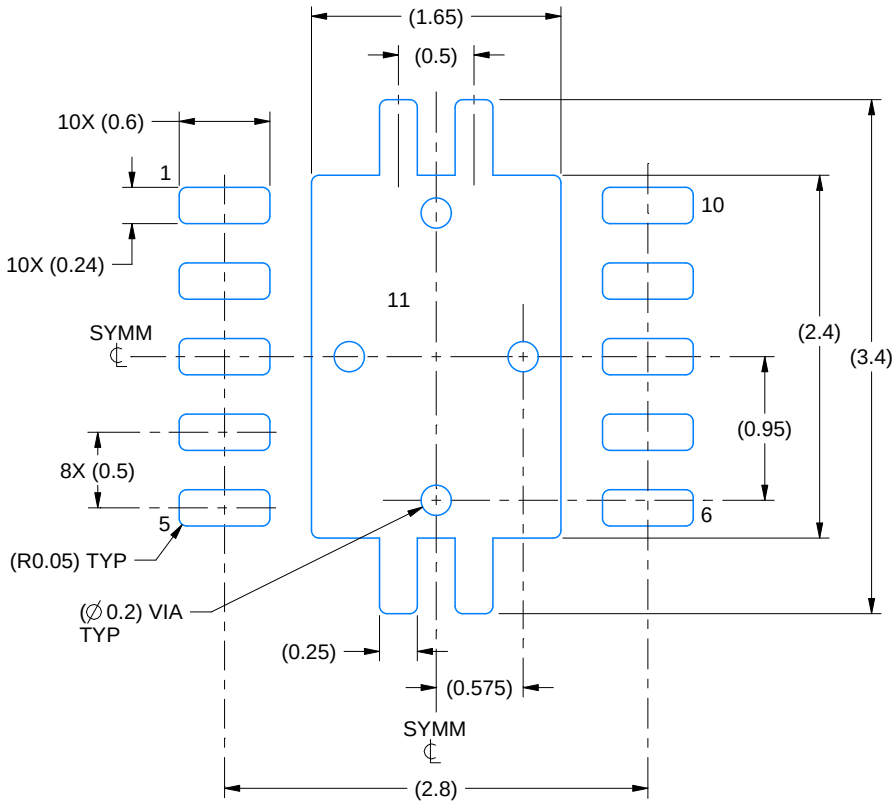
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

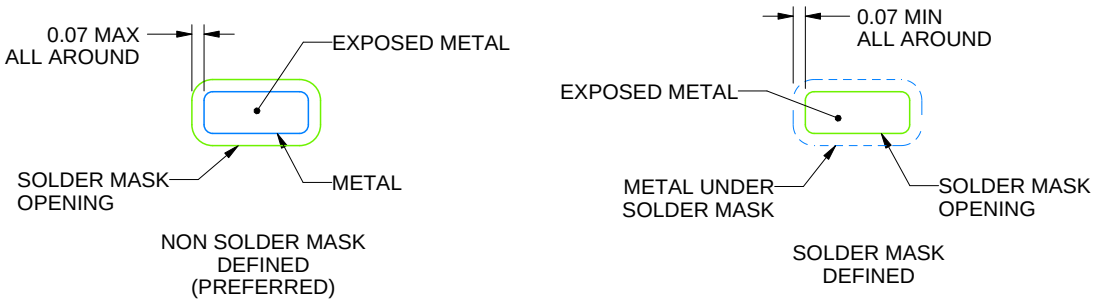


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

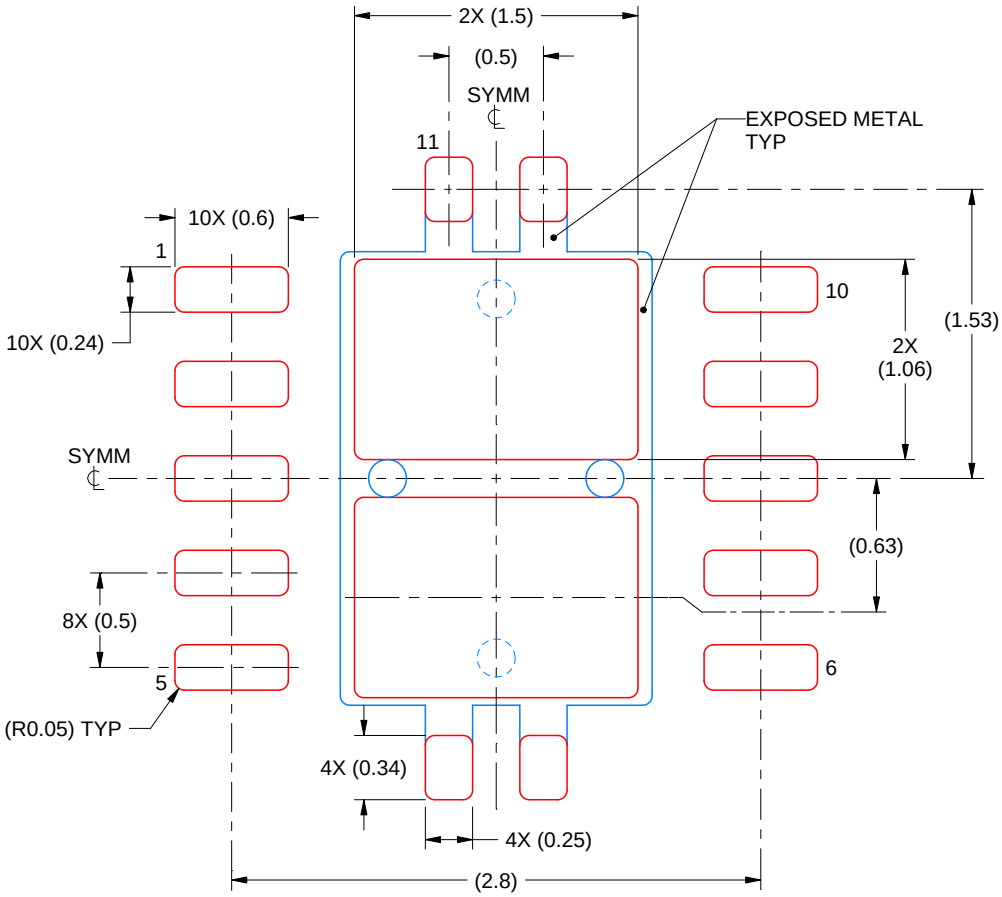
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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