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# TMS320VC5509A Fixed-Point Digital Signal Processor

## Data Manual

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**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**






## REVISION HISTORY

This revision history highlights the technical changes made to SPRS205J to generate SPRS205K.

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| 20 | Table 2−3, Signal Descriptions (Continued):<br>− Updated/changed D[15:0] **FUNCTION** description from "... The data bus keepers are ***disabled*** at reset, ..." to "... The data bus keepers are ***enabled*** at reset, ...". |

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# 1 TMS320VC5509A Features

- High-Performance, Low-Power, Fixed-Point TMS320C55x™ Digital Signal Processor
  - 9.26-, 6.95-, 5-ns Instruction Cycle Time
  - 108-, 144-, 200-MHz Clock Rate
  - One/Two Instruction(s) Executed per Cycle
  - Dual Multipliers [Up to 400 Million Multiply-Accumulates per Second (MMACS)]
  - Two Arithmetic/Logic Units (ALUs)
  - Three Internal Data/Operand Read Buses and Two Internal Data/Operand Write Buses
- 128K x 16-Bit On-Chip RAM, Composed of:
  - 64K Bytes of Dual-Access RAM (DARAM) 8 Blocks of 4K × 16-Bit
  - 192K Bytes of Single-Access RAM (SARAM) 24 Blocks of 4K × 16-Bit
- 64K Bytes of One-Wait-State On-Chip ROM (32K × 16-Bit)
- 8M × 16-Bit Maximum Addressable External Memory Space (Synchronous DRAM)
- 16-Bit External Parallel Bus Memory Supporting Either:
  - External Memory Interface (EMIF) With GPIO Capabilities and Glueless Interface to:
    - Asynchronous Static RAM (SRAM)
    - Asynchronous EPROM
    - Synchronous DRAM (SDRAM)
  - 16-Bit Parallel Enhanced Host-Port Interface (EHPI) With GPIO Capabilities
- Programmable Low-Power Control of Six Device Functional Domains
- On-Chip Scan-Based Emulation Logic
- On-Chip Peripherals
  - Two 20-Bit Timers
  - Watchdog Timer
  - Six-Channel Direct Memory Access (DMA) Controller
  - Three Serial Ports Supporting a Combination of:
    - Up to 3 Multichannel Buffered Serial Ports (McBSPs)
    - Up to 2 MultiMedia/Secure Digital Card Interfaces
  - Programmable Phase-Locked Loop Clock Generator
  - Seven (LQFP) or Eight (BGA) General-Purpose I/O (GPIO) Pins and a General-Purpose Output Pin (XF)
  - USB Full-Speed (12 Mbps) Slave Port Supporting Bulk, Interrupt and Isochronous Transfers
  - Inter-Integrated Circuit ($I^2C$) Multi-Master and Slave Interface
  - Real-Time Clock (RTC) With Crystal Input, Separate Clock Domain, Separate Power Supply
  - 4-Channel (BGA) or 2-Channel (LQFP) 10-Bit Successive Approximation A/D
- IEEE Std 1149.1† (JTAG) Boundary Scan Logic
- Packages:
  - 144-Terminal Low-Profile Quad Flatpack (LQFP) (PGE Suffix)
  - 179-Terminal MicroStar BGA™ (Ball Grid Array) (GHH Suffix)
  - 179-Terminal Lead-Free MicroStar BGA™ (Ball Grid Array) (ZHH Suffix)
- 1.2-V Core (108 MHz), 2.7-V – 3.6-V I/Os
- 1.35-V Core (144 MHz), 2.7-V – 3.6-V I/Os
- 1.6-V Core (200 MHz), 2.7-V – 3.6-V I/Os

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

# 2 Introduction

This section describes the main features of the TMS320VC5509A, lists the pin assignments, and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

**NOTE:** This data manual is designed to be used in conjunction with the*TMS320C55x™ DSP Functional Overview* (literature number SPRU312), the *TMS320C55x DSP CPU Reference Guide* (literature number SPRU371), and the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317).

## 2.1 Description

The TMS320VC5509A fixed-point digital signal processor (DSP) is based on the TMS320C55x DSP generation CPU processor core. The C55x™ DSP architecture achieves high performance and low power through increased parallelism and total focus on reduction in power dissipation. The CPU supports an internal bus structure that is composed of one program bus, three data read buses, two data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to three data reads and two data writes in a single cycle. In parallel, the DMA controller can perform up to two data transfers per cycle independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions.

The general-purpose input and output functions and the10-bit A/D provide sufficient pins for status, interrupts, and bit I/O for LCDs, keyboards, and media interfaces. The parallel interface operates in two modes, either as a slave to a microcontroller using the HPI port or as a parallel media interface using the asynchronous EMIF. Serial media is supported through two MultiMedia Card/Secure Digital (MMC/SD) peripherals and three McBSPs.

The 5509A peripheral set includes an external memory interface (EMIF) that provides glueless access to asynchronous memories like EPROM and SRAM, as well as to high-speed, high-density memories such as synchronous DRAM. Additional peripherals include Universal Serial Bus (USB), real-time clock, watchdog timer, $I^2C$ multi-master and slave interface. Three full-duplex multichannel buffered serial ports (McBSPs) provide glueless interface to a variety of industry-standard serial devices, and multichannel communication with up to 128 separately enabled channels. The enhanced host-port interface (HPI) is a 16-bit parallel interface used to provide host processor access to 32K bytes of internal memory on the 5509A. The HPI can be configured in either multiplexed or non-multiplexed mode to provide glueless interface to a wide variety of host processors. The DMA controller provides data movement for six independent channel contexts without CPU intervention, providing DMA throughput of up to two 16-bit words per cycle. Two general-purpose timers, up to eight dedicated general-purpose I/O (GPIO) pins, and digital phase-locked loop (DPLL) clock generation are also included.

The 5509A is supported by the industry's award-winning eXpressDSP™, Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS™, Texas Instruments' algorithm standard, and the industry's largest third-party network. The Code Composer Studio IDE features code generation tools including a C Compiler and Visual Linker, simulator, RTDX™, XDS510™ emulation device drivers, and evaluation modules. The 5509A is also supported by the C55x DSP Library which features more than 50 foundational software kernels (FIR filters, IIR filters, FFTs, and various math functions) as well as chip and board support libraries.

C55x, eXpressDSP, Code Composer Studio, DSP/BIOS, RTDX, and XDS510 are trademarks of Texas Instruments.

The TMS320C55x DSP core was created with an open architecture that allows the addition of application-specific hardware to boost performance on specific algorithms. The hardware extensions on the 5509A strike the perfect balance of fixed function performance with programmable flexibility, while achieving low-power consumption, and cost that traditionally has been difficult to find in the video-processor market. The extensions allow the 5509A to deliver exceptional video codec performance with more than half its bandwidth available for performing additional functions such as color space conversion, user-interface operations, security, TCP/IP, voice recognition, and text-to-speech conversion. As a result, a single 5509A DSP can power most portable digital video applications with processing headroom to spare. For more information, see the *TMS320C55x Hardware Extensions for Image/Video Applications Programmer's Reference* (literature number SPRU098). For more information on using the the DSP Image Processing Library, see the *TMS320C55x Image/Video Processing Library Programmer's Reference* (literature number SPRU037).

## 2.2 Pin Assignments

Figure 2−1 illustrates the ball locations for the 179-pin ball grid array (BGA) package and is used in conjunction with Table 2−1 to locate signal names and ball grid numbers.

$DV_{DD}$ is the power supply for the I/O pins while $CV_{DD}$ is the power supply for the core. $V_{SS}$ is the ground for both the I/O pins and the core. $RCV_{DD}$ and $RDV_{DD}$ are RTC module core and I/O supply, respectively. $USBV_{DD}$ is the USB module I/O (DP, DN, and PU) supply. $ADV_{DD}$ is the power supply for the digital portion of the ADC. $AV_{DD}$ is the power supply for the analog part of the ADC. $ADV_{SS}$ is the ground pin for the digital portion of the ADC. $AV_{SS}$ is the ground pin for the analog part of the ADC. $USBPLLV_{DD}$ and $USBPLLV_{SS}$ are the dedicated supply and ground pins for the USB PLL, respectively.

### *2.2.1 Terminal Assignments for the GHH and ZHH Packages*

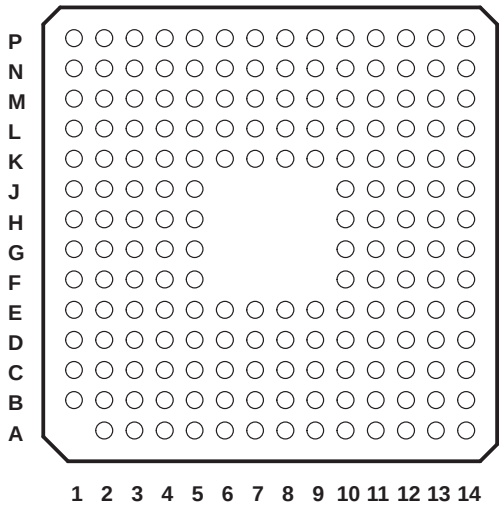



**Figure 2−1. 179-Terminal GHH and ZHH Ball Grid Array (Bottom View)**

**Table 2−1. Pin Assignments for the GHH and ZHH Packages**

| BALL # | SIGNAL NAME | BALL # | SIGNAL NAME | BALL # | SIGNAL NAME | BALL # | SIGNAL NAME |
|---|---|---|---|---|---|---|---|
| A2 | $V_{SS}$ | D5 | GPIO5 | H2 | $DV_{DD}$ | L13 | D15 |
| A3 | GPIO4 | D6 | DR0 | H3 | A19 | L14 | $CV_{DD}$ |
| A4 | $DV_{DD}$ | D7 | S10 | H4 | C4 | M1 | C10 |
| A5 | FSR0 | D8 | S11 | H5 | C5 | M2 | C13 |
| A6 | $CV_{DD}$ | D9 | $DV_{DD}$ | H10 | $DV_{DD}$ | M3 | $V_{SS}$ |
| A7 | S12 | D10 | S25 | H11 | A'[0] | M4 | $CV_{DD}$ |
| A8 | $DV_{DD}$ | D11 | $V_{SS}$ | H12 | $\overline{\text{RESET}}$ | M5 | $V_{SS}$ |
| A9 | S20 | D12 | AIN2 | H13 | SDA | M6 | A5 |
| A10 | S21 | D13 | AIN1 | H14 | SCL | M7 | A1 |
| A11 | S23 | D14 | AIN0 | J1 | C6 | M8 | A15 |
| A12 | RTCINX1 | E1 | GPIO1 | J2 | $DV_{DD}$ | M9 | D3 |
| A13 | $RDV_{DD}$ | E2 | GPIO2 | J3 | C7 | M10 | D6 |
| A14 | $RDV_{DD}$ | E3 | $DV_{DD}$ | J4 | C8 | M11 | $CV_{DD}$ |
| B1 | $V_{SS}$ | E4 | $V_{SS}$ | J5 | $CV_{DD}$ | M12 | $DV_{DD}$ |
| B2 | $CV_{DD}$ | E5 | $V_{SS}$ | J10 | $CV_{DD}$ | M13 | $V_{SS}$ |
| B3 | GPIO3 | E6 | $DV_{DD}$ | J11 | $CV_{DD}$ | M14 | D12 |
| B4 | TIN/TOUT0 | E7 | DX0 | J12 | $\overline{\text{TRST}}$ | N1 | $V_{SS}$ |
| B5 | CLKR0 | E8 | S15 | J13 | TCK | N2 | $V_{SS}$ |
| B6 | FSX0 | E9 | S13 | J14 | TMS | N3 | A13 |
| B7 | $CV_{DD}$ | E10 | NC | K1 | A18 | N4 | A10 |
| B8 | $CV_{DD}$ | E11 | AIN3 | K2 | C9 | N5 | A7 |
| B9 | $V_{SS}$ | E12 | $ADV_{SS}$ | K3 | C11 | N6 | $DV_{DD}$ |
| B10 | S24 | E13 | $V_{SS}$ | K4 | $V_{SS}$ | N7 | $CV_{DD}$ |
| B11 | $V_{SS}$ | E14 | XF | K5 | $V_{SS}$ | N8 | $CV_{DD}$ |
| B12 | RTCINX2 | F1 | X1 | K6 | A3 | N9 | $V_{SS}$ |
| B13 | $RDV_{DD}$ | F2 | X2/CLKIN | K7 | A2 | N10 | $V_{SS}$ |
| B14 | $AV_{SS}$ | F3 | GPIO0 | K8 | D1 | N11 | D8 |
| C1 | PU | F4 | $V_{SS}$ | K9 | A14 | N12 | D11 |
| C2 | $V_{SS}$ | F5 | CLKOUT | K10 | $DV_{DD}$ | N13 | $DV_{DD}$ |
| C3 | NC | F10 | $ADV_{DD}$ | K11 | EMU0 | N14 | $V_{SS}$ |
| C4 | GPIO6 | F11 | $V_{SS}$ | K12 | EMU1/$\overline{\text{OFF}}$ | P1 | $V_{SS}$ |
| C5 | $V_{SS}$ | F12 | $\overline{\text{INT4}}$ | K13 | TDO | P2 | $V_{SS}$ |
| C6 | CLKX0 | F13 | $DV_{DD}$ | K14 | TDI | P3 | A12 |
| C7 | $V_{SS}$ | F14 | $\overline{\text{INT3}}$ | L1 | $CV_{DD}$ | P4 | A9 |
| C8 | S14 | G1 | $CV_{DD}$ | L2 | C14 | P5 | A17 |
| C9 | S22 | G2 | C1 | L3 | C12 | P6 | A4 |
| C10 | $CV_{DD}$ | G3 | A20 | L4 | A11 | P7 | A16 |
| C11 | $V_{SS}$ | G4 | C2 | L5 | A8 | P8 | $DV_{DD}$ |
| C12 | $RCV_{DD}$ | G5 | C0 | L6 | A6 | P9 | D2 |
| C13 | $AV_{SS}$ | G10 | $\overline{\text{INT2}}$ | L7 | A0 | P10 | D5 |
| C14 | $AV_{DD}$ | G11 | $USBPLLV_{DD}$ | L8 | D0 | P11 | D7 |
| D1 | GPIO7 | G12 | $USBPLLV_{SS}$ | L9 | D4 | P12 | D10 |
| D2 | $USBV_{DD}$ | G13 | $\overline{\text{INT1}}$ | L10 | D9 | P13 | $DV_{DD}$ |
| D3 | DN | G14 | $\overline{\text{INT0}}$ | L11 | D13 | P14 | $DV_{DD}$ |
| D4 | DP | H1 | C3 | L12 | D14 | | |

### 2.2.2 Pin Assignments for the PGE Package

The TMS320VC5509APGE 144-pin low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2−2 and is used in conjunction with Table 2−2 to locate signal names and pin numbers.

$DV_{DD}$ is the power supply for the I/O pins while $CV_{DD}$ is the power supply for the core. $V_{SS}$ is the ground for both the I/O pins and the core. $RCV_{DD}$ and $RDV_{DD}$ are RTC module core and I/O supply, respectively. $USBV_{DD}$ is the USB module I/O (DP, DN, and PU) supply. $ADV_{DD}$ is the power supply for the digital portion of the ADC. $AV_{DD}$ is the power supply for the analog part of the ADC. $ADV_{SS}$ is the ground pin for the digital portion of the ADC. $AV_{SS}$ is the ground pin for the analog part of the ADC. $USBPLLV_{DD}$ and $USBPLLV_{SS}$ are the dedicated supply and ground pins for the USB PLL, respectively.

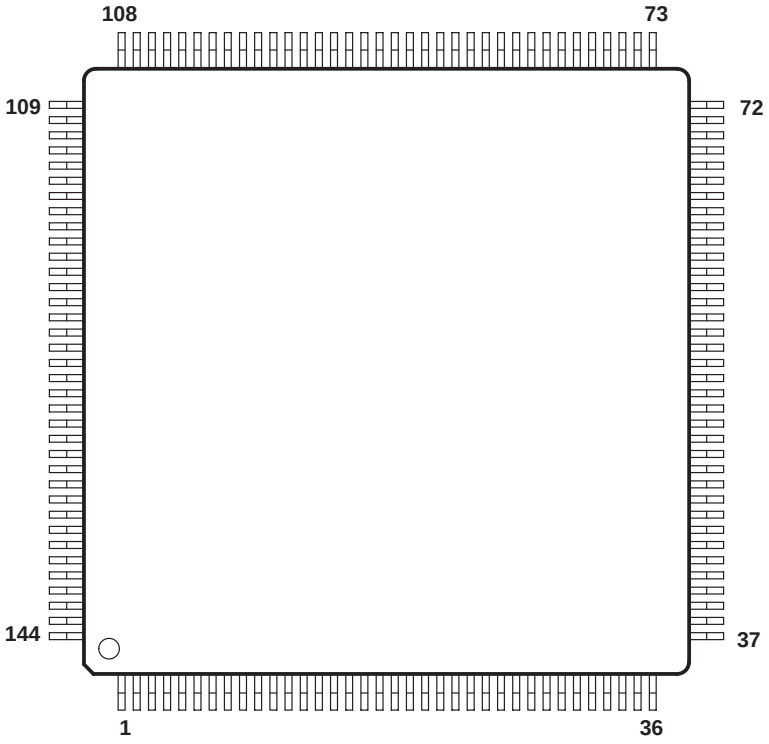



**Figure 2−2. 144-Pin PGE Low-Profile Quad Flatpack (Top View)**

**Table 2−2. Pin Assignments for the PGE Package**

| PIN NO. | SIGNAL NAME | PIN NO. | SIGNAL NAME | PIN NO. | SIGNAL NAME | PIN NO. | SIGNAL NAME |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 37 | $V_{SS}$ | 73 | $V_{SS}$ | 109 | $RDV_{DD}$ |
| 2 | PU | 38 | A13 | 74 | D12 | 110 | $RCV_{DD}$ |
| 3 | DP | 39 | A12 | 75 | D13 | 111 | RTCINX2 |
| 4 | DN | 40 | A11 | 76 | D14 | 112 | RTCINX1 |
| 5 | $USBV_{DD}$ | 41 | $CV_{DD}$ | 77 | D15 | 113 | $V_{SS}$ |
| 6 | GPIO7 | 42 | A10 | 78 | $CV_{DD}$ | 114 | $V_{SS}$ |
| 7 | $V_{SS}$ | 43 | A9 | 79 | EMU0 | 115 | $V_{SS}$ |
| 8 | $DV_{DD}$ | 44 | A8 | 80 | EMU1/$\overline{OFF}$ | 116 | S23 |
| 9 | GPIO2 | 45 | $V_{SS}$ | 81 | TDO | 117 | S25 |
| 10 | GPIO1 | 46 | A7 | 82 | TDI | 118 | $CV_{DD}$ |
| 11 | $V_{SS}$ | 47 | A6 | 83 | $CV_{DD}$ | 119 | S24 |
| 12 | GPIO0 | 48 | A5 | 84 | $\overline{TRST}$ | 120 | S21 |
| 13 | X2/CLKIN | 49 | $DV_{DD}$ | 85 | TCK | 121 | S22 |
| 14 | X1 | 50 | A4 | 86 | TMS | 122 | $V_{SS}$ |
| 15 | CLKOUT | 51 | A3 | 87 | $CV_{DD}$ | 123 | S20 |
| 16 | C0 | 52 | A2 | 88 | $DV_{DD}$ | 124 | S13 |
| 17 | C1 | 53 | $CV_{DD}$ | 89 | SDA | 125 | S15 |
| 18 | $CV_{DD}$ | 54 | A1 | 90 | SCL | 126 | $DV_{DD}$ |
| 19 | C2 | 55 | A0 | 91 | $\overline{RESET}$ | 127 | S14 |
| 20 | C3 | 56 | $DV_{DD}$ | 92 | $USBPLLV_{SS}$ | 128 | S11 |
| 21 | C4 | 57 | D0 | 93 | $\overline{INT0}$ | 129 | S12 |
| 22 | C5 | 58 | D1 | 94 | $\overline{INT1}$ | 130 | S10 |
| 23 | C6 | 59 | D2 | 95 | $USBPLLV_{DD}$ | 131 | DX0 |
| 24 | $DV_{DD}$ | 60 | $V_{SS}$ | 96 | $\overline{INT2}$ | 132 | $CV_{DD}$ |
| 25 | C7 | 61 | D3 | 97 | $\overline{INT3}$ | 133 | FSX0 |
| 26 | C8 | 62 | D4 | 98 | $DV_{DD}$ | 134 | CLKX0 |
| 27 | C9 | 63 | D5 | 99 | $\overline{INT4}$ | 135 | DR0 |
| 28 | C11 | 64 | $V_{SS}$ | 100 | $V_{SS}$ | 136 | FSR0 |
| 29 | $CV_{DD}$ | 65 | D6 | 101 | XF | 137 | CLKR0 |
| 30 | $CV_{DD}$ | 66 | D7 | 102 | $V_{SS}$ | 138 | $V_{SS}$ |
| 31 | C14 | 67 | D8 | 103 | $ADV_{SS}$ | 139 | $DV_{DD}$ |
| 32 | C12 | 68 | $CV_{DD}$ | 104 | $ADV_{DD}$ | 140 | TIN/TOUT0 |
| 33 | $V_{SS}$ | 69 | D9 | 105 | AIN0 | 141 | GPIO6 |
| 34 | C10 | 70 | D10 | 106 | AIN1 | 142 | GPIO4 |
| 35 | C13 | 71 | D11 | 107 | $AV_{DD}$ | 143 | GPIO3 |
| 36 | $V_{SS}$ | 72 | $DV_{DD}$ | 108 | $AV_{SS}$ | 144 | $V_{SS}$ |

## 2.3 Signal Descriptions

Table 2−3 lists each signal, function, and operating mode(s) grouped by function. See Section 2.2 for pin locations based on package type.

**Table 2−3. Signal Descriptions**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS** | | | | | |
| A[13:0] | | I/O/Z | A subset of the parallel address bus A13−A0 of the C55x™ DSP core bonded to external pins. These pins serve in one of three functions: HPI address bus (HPI.HA[13:0]), EMIF address bus (EMIF.A[13:0]), or general-purpose I/O (GPIO.A[13:0]). The initial state of these pins depends on the GPIO0 pin. See Section 3.5.1 for more information.<br>The address bus has a bus holder feature that eliminates passive component requirement and the power dissipation associated with them. The bus holders keep the address bus at the previous logic level when the bus goes into a high-impedance state. | BK | GPIO0 = 1: Output, EMIF.A[13:0]<br>GPIO0 = 0: Input, HPI.HA[13:0] |
| | HPI.HA[13:0] | I | HPI address bus. HPI.HA[13:0] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 10. This setting enables the HPI in non-multiplexed mode.<br>HPI.HA[13:0] provides DSP internal memory access to host. In non-multiplexed mode, these signals are driven by an external host as address lines. | | |
| | EMIF.A[13:0] | O/Z | EMIF address bus. EMIF.A[13:0] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 01. This setting enables the full EMIF mode and the EMIF drives the parallel port address bus. The internal A[14] address is exclusive-ORed with internal A[0] address and the result is routed to the A[0] pin. | | |
| | GPIO.A[13:0] | I/O/Z | General-purpose I/O address bus. GPIO.A[13:0] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 11. This setting enables the HPI in multiplexed mode with the Parallel Port GPIO register controlling the parallel port address bus. GPIO is also selected when the Parallel Port Mode bit field is 00, enabling the Data EMIF mode. | | |
| A′[0] (BGA only) | EMIF.A′[0] | O/Z | EMIF address bus A′[0]. This pin is not multiplexed with EMIF.A[14] and is used as the least significant external address pin on the BGA package. | | Output |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS (CONTINUED)** | | | | | |
| A[15:14] (BGA only) | | I/O/Z | A subset of the parallel address bus A15−A14 of the C55x™ DSP core bonded to external pins. These pins serve in one of two functions: EMIF address bus (EMIF.A[15:14]), or general-purpose I/O (GPIO.A[15:14]). The initial state of these pins depends on the GPIO0 pin. See Section 3.5.1 for more information.<br>The address bus has a bus holder feature that eliminates passive component requirement and the power dissipation associated with them. The bus holders keep the address bus at the previous logic level when the bus goes into a high-impedance state. | BK | GPIO0 = 1: Output, EMIF.A[15:14]<br>GPIO0 = 0: Input, GPIO.A[15:14] |
| | EMIF.A[15:14] | O/Z | EMIF address bus. EMIF.A[15:14] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 01. This setting enables the full EMIF mode and the EMIF drives the parallel port address bus. | | |
| | GPIO.A[15:14] | I/O/Z | General-purpose I/O address bus. GPIO.A[15:14] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 11. This setting enables the HPI in multiplexed mode with the Parallel Port GPIO register controlling the parallel port address bus. GPIO is also selected when the Parallel Port Mode bit field is 00, enabling the Data EMIF mode. | | |
| A[20:16] (BGA only) | EMIF.A[20:16] | O/Z | EMIF address bus. At reset, these address pins are set as output.<br>NOTE: These pins only function as EMIF address pins and they are not multiplexed for any other function. | | Output |
| D[15:0] | | I/O/Z | A subset of the parallel bidirectional data bus D31−D0 of the C55x™ DSP core. These pins serve in one of two functions: EMIF data bus (EMIF.D[15:0]) or HPI data bus (HPI.HD[15:0]). The initial state of these pins depends on the GPIO0 pin. See Section 3.5.1 for more information.<br>The data bus includes bus keepers to reduce the static power dissipation caused by floating, unused pins. This eliminates the need for external bias resistors on unused pins. When the data bus is not being driven by the CPU, the bus keepers keep the pins at the logic level that was most recently driven. (The data bus keepers are enabled at reset, and can be enabled/disabled under software control.) | BK | GPIO0 = 1: Input, EMIF.D[15:0]<br>GPIO0 = 0: Input, HPI.HD[15:0] |
| | EMIF.D[15:0] | I/O/Z | EMIF data bus. EMIF.D[15:0] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 00 or 01. | | |
| | HPI.HD[15:0] | I/O/Z | HPI data bus. HPI.HD[15:0] is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 10 or 11. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS (CONTINUED)** | | | | | |
| C0 | | I/O/Z | EMIF asynchronous memory read enable or general-purpose IO8. This pin serves in one of two functions: EMIF asynchronous memory read enable (EMIF.$\overline{\text{ARE}}$) or general-purpose IO8 (GPIO8). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{ARE}}$<br>GPIO0 = 0: Input, GPIO8 |
| | EMIF.$\overline{\text{ARE}}$ | O/Z | Active-low EMIF asynchronous memory read enable. EMIF.$\overline{\text{ARE}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 00 or 01. | | |
| | GPIO8 | I/O/Z | General-purpose IO8. GPIO8 is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 10 or 11. | | |
| C1 | | O/Z | EMIF asynchronous memory output enable or HPI interrupt output. This pin serves in one of two functions: EMIF asynchronous memory output enable (EMIF.$\overline{\text{AOE}}$) or HPI interrupt output (HPI.$\overline{\text{HINT}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | | GPIO0 = 1: Output, EMIF.$\overline{\text{AOE}}$<br>GPIO0 = 0: Output, HPI.$\overline{\text{HINT}}$ |
| | EMIF.$\overline{\text{AOE}}$ | O/Z | Active-low asynchronous memory output enable. EMIF.$\overline{\text{AOE}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 00 or 01. | | |
| | HPI.$\overline{\text{HINT}}$ | O/Z | Active-low HPI interrupt output. HPI.$\overline{\text{HINT}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 10 or 11. | | |
| C2 | | I/O/Z | EMIF asynchronous memory write enable or HPI read/write. This pin serves in one of two functions: EMIF asynchronous memory write enable (EMIF.$\overline{\text{AWE}}$) or HPI read/write (HPI.HR/$\overline{\text{W}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{AWE}}$<br>GPIO0 = 0: Input, HPI.HR/$\overline{\text{W}}$ |
| | EMIF.$\overline{\text{AWE}}$ | O/Z | Active-low EMIF asynchronous memory write enable. EMIF.$\overline{\text{AWE}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 00 or 01. | | |
| | HPI.HR/$\overline{\text{W}}$ | I | HPI read/write. HPI.HR/$\overline{\text{W}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 10 or 11. HPI.HR/$\overline{\text{W}}$ controls the direction of the HPI transfer. | | |
| C3 | | I/O/Z | EMIF data ready input or HPI ready output. This pin serves in one of two functions: EMIF data ready input (EMIF.ARDY) or HPI ready output (HPI.HRDY). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | H | GPIO0 = 1: Input, EMIF.ARDY<br>GPIO0 = 0: Output, HPI.HRDY |
| | EMIF.ARDY | I | EMIF data ready input. Used to insert wait states for slow memories. EMIF.ARDY is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 00 or 01. When this pin is used as ARDY, an external 2.2 kΩ pull−up resistor is recommended. | | |
| | HPI.HRDY | O | HPI ready output. HPI.HRDY is selected when the Parallel Port Mode bit field of the External Bus Selection Register is 10 or 11. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS (CONTINUED)** | | | | | |
| C4 | | I/O/Z | EMIF chip select for memory space CE0 or general-purpose IO9. This pin serves in one of two functions: EMIF chip select for memory space CE0 (EMIF.$\overline{CE0}$) or general-purpose IO9 (GPIO9). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{CE0}$<br>GPIO0 = 0: Input, GPIO9 |
| | EMIF.$\overline{CE0}$ | O/Z | Active-low EMIF chip select for memory space CE0. EMIF.$\overline{CE0}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | GPIO9 | I/O/Z | General-purpose IO9. GPIO9 is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 10 or 11. | | |
| C5 | | I/O/Z | EMIF chip select for memory space CE1 or general-purpose IO10. This pin serves in one of two functions: EMIF chip-select for memory space CE1 (EMIF.$\overline{CE1}$) or general-purpose IO10 (GPIO10). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{CE1}$<br>GPIO0 = 0: Input, GPIO10 |
| | EMIF.$\overline{CE1}$ | O/Z | Active-low EMIF chip select for memory space CE1. EMIF.$\overline{CE1}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | GPIO10 | I/O/Z | General-purpose IO10. GPIO10 is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 10 or 11. | | |
| C6 | | I/O/Z | EMIF chip select for memory space CE2 or HPI control input 0. This pin serves in one of two functions: EMIF chip-select for memory space CE2 (EMIF.$\overline{CE2}$) or HPI control input 0 (HPI.HCNTL0). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{CE2}$<br>GPIO0 = 0: Input, HPI.HCNTL0 |
| | EMIF.$\overline{CE2}$ | O/Z | Active-low EMIF chip select for memory space CE2. EMIF.$\overline{CE2}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.HCNTL0 | I | HPI control input 0. This pin, in conjunction with HPI.HCNTL1, selects a host access to one of the three HPI registers. HPI.HCNTL0 is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 10 or 11. | | |
| C7 | | I/O/Z | EMIF chip select for memory space CE3, general-purpose IO11, or HPI control input 1. This pin serves in one of three functions: EMIF chip-select for memory space CE3 (EMIF.$\overline{CE3}$), general-purpose IO11 (GPIO11), or HPI control input 1 (HPI.HCNTL1). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{CE3}$<br>GPIO0 = 0: Input, HPI.HCNTL1 |
| | EMIF.$\overline{CE3}$ | O/Z | Active-low EMIF chip select for memory space CE3. EMIF.$\overline{CE3}$ is selected when the Parallel Port Mode bit field is of the External Bus Selection Register set to 00 or 01. | | |
| | GPIO11 | I/O/Z | General-purpose IO11. GPIO11 is selected when the Parallel Port Mode bit field is set to 10. | | |
| | HPI.HCNTL1 | I | HPI control input 1. This pin, in conjunction with HPI.HCNTL0, selects a host access to one of the three HPI registers. The HPI.HCNTL1 mode is selected when the Parallel Port Mode bit field is set to 11. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS (CONTINUED)** | | | | | |
| C8 | | I/O/Z | EMIF byte enable 0 control or HPI byte identification. This pin serves in one of two functions: EMIF byte enable 0 control (EMIF.$\overline{\text{BE0}}$) or HPI byte identification (HPI.$\overline{\text{HBE0}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{BE0}}$<br>GPIO0 = 0: Input, HPI.$\overline{\text{HBE0}}$ |
| | EMIF.$\overline{\text{BE0}}$ | O/Z | Active-low EMIF byte enable 0 control. EMIF.$\overline{\text{BE0}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HBE0}}$ | I | HPI byte identification. This pin, in conjunction with HPI.$\overline{\text{HBE1}}$, identifies the first or second byte of the transfer. HPI.$\overline{\text{HBE0}}$ is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |
| C9 | | I/O/Z | EMIF byte enable 1 control or HPI byte identification. This pin serves in one of two functions: EMIF byte enable 1 control (EMIF.$\overline{\text{BE1}}$) or HPI byte identification (HPI.$\overline{\text{HBE1}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{BE1}}$<br>GPIO0 = 0: Input, HPI.$\overline{\text{HBE1}}$ |
| | EMIF.$\overline{\text{BE1}}$ | O/Z | Active-low EMIF byte enable 1 control. EMIF.$\overline{\text{BE1}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HBE1}}$ | I | HPI byte identification. This pin, in conjunction with HPI.$\overline{\text{HBE0}}$, identifies the first or second byte of the transfer. HPI.$\overline{\text{HBE1}}$ is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |
| C10 | | I/O/Z | EMIF SDRAM row strobe, HPI address strobe, or general-purpose IO12. This pin serves in one of three functions: EMIF SDRAM row strobe (EMIF.$\overline{\text{SDRAS}}$), HPI address strobe (HPI.$\overline{\text{HAS}}$), or general-purpose IO12 (GPIO12). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{SDRAS}}$<br>GPIO0 = 0: Input, HPI.$\overline{\text{HAS}}$ |
| | EMIF.$\overline{\text{SDRAS}}$ | O/Z | Active-low EMIF SDRAM row strobe. EMIF.$\overline{\text{SDRAS}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HAS}}$ | I | Active-low HPI address strobe. This signal latches the address in the HPIA register in the HPI Multiplexed mode. HPI.$\overline{\text{HAS}}$ is selected when the Parallel Port Mode bit field is set to 11. | | |
| | GPIO12 | I/O/Z | General-purpose IO12. GPIO12 is selected when the Parallel Port Mode bit field is set to 10. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **PARALLEL BUS (CONTINUED)** | | | | | |
| C11 | | I/O/Z | EMIF SDRAM column strobe or HPI chip select input. This pin serves in one of two functions: EMIF SDRAM column strobe (EMIF.$\overline{\text{SDCAS}}$) or HPI chip select input (HPI.$\overline{\text{HCS}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{SDCAS}}$<br>GPIO0 = 0: Input, HPI.$\overline{\text{HCS}}$ |
| | EMIF.$\overline{\text{SDCAS}}$ | O/Z | Active-low EMIF SDRAM column strobe. EMIF.$\overline{\text{SDCAS}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HCS}}$ | I | HPI Chip Select Input. HPI.$\overline{\text{HCS}}$ is the select input for the HPI and must be driven low during accesses. HPI.$\overline{\text{HCS}}$ is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |
| C12 | | I/O/Z | EMIF SDRAM write enable or HPI Data Strobe 1 input. This pin serves in one of two functions: EMIF SDRAM write enable (EMIF.$\overline{\text{SDWE}}$) or HPI data strobe 1 (HPI.$\overline{\text{HDS1}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.$\overline{\text{SDWE}}$<br>GPIO0 = 0: Input, HPI.$\overline{\text{HDS1}}$ |
| | EMIF.$\overline{\text{SDWE}}$ | O/Z | EMIF SDRAM write enable. EMIF. $\overline{\text{SDWE}}$ is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HDS1}}$ | I | HPI Data Strobe 1 Input. HPI.$\overline{\text{HDS1}}$ is driven by the host read or write strobes to control the transfer. HPI.$\overline{\text{HDS1}}$ is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |
| C13 | | I/O/Z | SDRAM A10 address line or general-purpose IO13. This pin serves in one of two functions: SDRAM A10 address line (EMIF.SDA10) or general-purpose IO13 (GPIO13). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.SDA10<br>GPIO0 = 0: Input, GPIO13 |
| | EMIF.SDA10 | O/Z | SDRAM A10 address line. Address line/autoprecharge disable for SDRAM memory. Serves as a row address bit (logically equivalent to A12) during ACTV commands and also disables the autoprecharging function of SDRAM during read or write operations. EMIF.SDA10 is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | GPIO13 | I/O/Z | General-purpose IO13. GPIO13 is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |
| C14 | | I/O/Z | Memory interface clock for SDRAM, HPI Data Strobe 2 input, or general-purpose IO14. This pin serves in one of two functions: memory interface clock for SDRAM (EMIF.CLKMEM) or HPI data strobe 2 (HPI.$\overline{\text{HDS2}}$). The initial state of this pin depends on the GPIO0 pin. See Section 3.5.1 for more information. | BK | GPIO0 = 1: Output, EMIF.CLKMEM<br>GPIO0 = 0: Input, HPI.$\overline{\text{HDS2}}$ |
| | EMIF.CLKMEM | O/Z | Memory interface clock for SDRAM. EMIF.CLKMEM is selected when the Parallel Port Mode bit field of the External Bus Selection Register is set to 00 or 01. | | |
| | HPI.$\overline{\text{HDS2}}$ | I | HPI Data Strobe 2 Input. HPI.$\overline{\text{HDS2}}$ is driven by the host read or write strobes to control the transfer. HPI.$\overline{\text{HDS2}}$ is selected when the Parallel Port Mode bit field is set to 10 or 11. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **INTERRUPT AND RESET PINS** | | | | | |
| $\overline{\text{INT}}$[4:0] | | I | Active-low external user interrupt inputs. $\overline{\text{INT}}$[4:0] are maskable and are prioritized by the interrupt enable register (IER) and the interrupt mode bit. | H, FS | Input |
| $\overline{\text{RESET}}$ | | I | Active-low reset. $\overline{\text{RESET}}$ causes the digital signal processor (DSP) to terminate execution and forces the program counter to FF8000h. When $\overline{\text{RESET}}$ is brought to a high level, execution begins at location FF8000h of program memory. $\overline{\text{RESET}}$ affects various registers and status bits. Use an external pullup resistor on this pin. | H, FS | Input |
| **BIT I/O SIGNALS** | | | | | |
| GPIO[7:6,4:0] (LQFP)<br>GPIO[7:0] (BGA) | | I/O/Z | 7-bit (LQFP package) or 8-bit (BGA package) Input/Output lines that can be individually configured as inputs or outputs, and also individually set or reset when configured as outputs. At reset, these pins are configured as inputs. After reset, the on-chip bootloader samples GPIO[3:0] to determine the boot mode selected. | BK (GPIO5 only)<br>H (except GPIO5) | Input |
| | EMIF.CKE (GPIO4) | O/Z | SDRAM CKE signal. The GPIO4 pin can be configured to serve as SDRAM CKE pin by setting the following bits in the External Bus Selection Register: CKE SEL = 1 and CKE EN = 1. In default mode, this pin serves as GPIO4. | | Input (GPIO4) |
| XF | | O/Z | External flag. XF is set high by the BSET XF instruction, set low by BCLR XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. XF goes into the high-impedance state when $\overline{\text{OFF}}$ is low, and is set high following reset. | | Output |
| | EMIF.CKE | O/Z | SDRAM CKE signal. The XF pin can be configured to serve as SDRAM CKE pin by setting the following bits in the External Bus Selection Register: CKE SEL = 0 and CKE EN = 1. In default mode, this pin serves as XF. | | Output (XF) |
| **OSCILLATOR/CLOCK SIGNALS** | | | | | |
| CLKOUT | | O/Z | DSP clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. CLKOUT goes into high-impedance state when $\overline{\text{OFF}}$ is low. | | Output |
| X2/CLKIN | | I/O | System clock/oscillator input. If the internal oscillator is not being used, X2/CLKIN functions as the clock input.<br>NOTE: The USB module requires a 48 MHz clock. Since this input clock is used by both the CPU PLL and the USB module PLL, it must be a factor of 48 MHz in order for the programmable PLL to produce the required 48 MHz USB module clock.<br>In CLKGEN domain idle (OSC IDLE) mode, this pin becomes output and is driven low to stop external crystals (if used) from oscillating or an external clock source from driving the DSP's internal logic. | | Oscillator Input |
| X1 | | O | Output pin from the internal system oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{\text{OFF}}$ is low. | | Oscillator Output |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **TIMER SIGNALS** | | | | | |
| TIN/TOUT0 | | I/O/Z | Timer0 Input/Output. When output, TIN/TOUT0 signals a pulse or a change of state when the on-chip timer counts down past zero. When input, TIN/TOUT0 provides the clock source for the internal timer module. At reset, this pin is configured as an input.<br>NOTE: Only the Timer0 signal is brought out. The Timer1 signal is terminated internally and is not available for external use. | H | Input |
| **REAL-TIME CLOCK** | | | | | |
| RTCINX1 | | I | Real-Time Clock Oscillator input | | Input |
| RTCINX2 | | O | Real-Time Clock Oscillator output | | Output |
| **I2C** | | | | | |
| SDA | | I/O/Z | I2C (bidirectional) data. At reset, this pin is in high-impedance mode. | H | Hi-Z |
| SCL | | I/O/Z | I2C (bidirectional) clock. At reset, this pin is in high-impedance mode. | H | Hi-Z |
| **MULTICHANNEL BUFFERED SERIAL PORTS SIGNALS** | | | | | |
| CLKR0 | | I/O/Z | McBSP0 receive clock. CLKR0 serves as the serial shift clock for the serial port receiver. At reset, this pin is in high-impedance mode. | H | Hi-Z |
| DR0 | | I | McBSP0 receive data | FS | Input |
| FSR0 | | I/O/Z | McBSP0 receive frame synchronization. The FSR0 pulse initiates the data receive process over DR0. At reset, this pin is in high-impedance mode. | | Hi-Z |
| CLKX0 | | I/O/Z | McBSP0 transmit clock. CLKX0 serves as the serial shift clock for the serial port transmitter. The CLKX0 pin is configured as input after reset. | H | Input |
| DX0 | | O/Z | McBSP0 transmit data. DX0 is placed in the high-impedance state when not transmitting, when $\overline{\text{RESET}}$ is asserted, or when $\overline{\text{OFF}}$ is low. | | Hi-Z |
| FSX0 | | I/O/Z | McBSP0 transmit frame synchronization. The FSX0 pulse initiates the data transmit process over DX0. Configured as an input following reset. | | Input |
| S10 | | I/O/Z | McBSP1 receive clock or MultiMedia Card/Secure Digital1 command/response. At reset, this pin is configured as McBSP1.CLKR. | H | Input |
| | McBSP1.CLKR | I/O/Z | McBSP1 receive clock. McBSP1.CLKR serves as the serial shift clock for the serial port receiver. McBSP1.CLKR is selected when the External Bus Selection Register has 00 in the Serial Port1 Mode bit field or following reset. | | |
| | MMC1.CMD SD1.CMD | I/O/Z | MMC1 or SD1 command/response is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode bit field. | | |
| S11 | | I/O/Z | McBSP1 data receive or Secure Digital1 data1. At reset, this pin is configured as McBSP1.DR. | | Input |
| | McBSP1.DR | I/Z | McBSP1 serial data receive. McBSP1.DR is selected when the External Bus Selection Register has 00 in the Serial Port1 Mode bit field or following reset. | | |
| | SD1.DAT1 | I/O/Z | SD1 data1 is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode bit field. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **MULTICHANNEL BUFFERED SERIAL PORTS SIGNALS (CONTINUED)** | | | | | |
| S12 | | I/O/Z | McBSP1 receive frame synchronization or Secure Digital1 data2. At reset, this pin is configured as McBSP1.FSR. | | Input |
| | McBSP1.FSR | I/Z | McBSP1 receive frame synchronization. The McBSP1.FSR pulse initiates the data receive process over McBSP1.DR. | | |
| | SD1.DAT2 | I/O/Z | SD1 data2 is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode bit field. | | |
| S13 | | O/Z | McBSP1 serial data transmit or MultiMedia Card/Secure Digital1 serial clock. At reset, this pin is configured as McBSP1.DX. | BK | Hi-Z |
| | McBSP1.DX | O/Z | McBSP1 serial data transmit. McBSP1.DX is placed in the high-impedance state when not transmitting, when $\overline{\text{RESET}}$ is asserted, or when $\overline{\text{OFF}}$ is low. McBSP1.DX is selected when the External Bus Selection Register has 00 in the Serial Port1 Mode bit field or following reset. | | |
| | MMC1.CLK SD1.CLK | O | MMC1 or SD1 serial clock is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode bit field. | | |
| S14 | | I/O/Z | McBSP1 transmit clock or MultiMedia Card/Secure Digital1 data0. At reset, this pin is configured as McBSP1.CLKX. | H | Input |
| | McBSP1.CLKX | I/O/Z | McBSP1 transmit clock. McBSP1.CLKX serves as the serial shift clock for the serial port transmitter. The McBSP1.CLKX pin is configured as input after reset. McBSP1.CLKX is selected when the External Bus Selection Register has 00 in the Serial Port1 Mode bit field or following reset. | | |
| | MMC1.DAT SD1.DAT0 | I/O/Z | MMC1 or SD1 data0 is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode Bit field. | | |
| S15 | | I/O/Z | McBSP1 transmit frame synchronization or Secure Digital1 data3. At reset, this pin is configured as McBSP1.FSX. | | Input |
| | McBSP1.FSX | I/O/Z | McBSP1 transmit frame synchronization. The McBSP1.FSX pulse initiates the data transmit process over McBSP1.DX. Configured as an input following reset. McBSP1.FSX is selected when the External Bus Selection Register has 00 in the Serial Port1 Mode bit field or following reset. | | |
| | SD1.DAT3 | I/O/Z | SD1 data3 is selected when the External Bus Selection Register has 10 in the Serial Port1 Mode bit field. | | |
| S20 | | I/O/Z | McBSP2 receive clock or MultiMedia Card/Secure Digital2 command/response. At reset, this pin is configured as McBSP2.CLKR. | H | Input |
| | McBSP2.CLKR | I/O/Z | McBSP2 receive clock. McBSP2.CLKR serves as the serial shift clock for the serial port receiver. McBSP2.CLKR is selected when the External Bus Selection Register has 00 in the Serial Port2 Mode bit field or following reset. | | |
| | MMC2.CMD SD2.CMD | I/O/Z | MMC2 or SD2 command/response is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **MULTICHANNEL BUFFERED SERIAL PORTS SIGNALS (CONTINUED)** | | | | | |
| S21 | | I/O/Z | McBSP2 data receive or Secure Digital2 data1. At reset, this pin is configured as McBSP2.DR. | | Input |
| | McBSP2.DR | I | McBSP2 serial data receive. McBSP2.DR is selected when the External Bus Selection Register has 00 in the Serial Port2 Mode bit field or following reset. | | |
| | SD2.DAT1 | I/O/Z | SD2 data1 is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |
| S22 | | I/O/Z | McBSP2 receive frame synchronization or Secure Digital2 data2. At reset, this pin is configured as McBSP2.FSR. | | Input |
| | McBSP2.FSR | I | McBSP2 receive frame synchronization. The McBSP2.FSR pulse initiates the data receive process over McBSP2.DR. | | |
| | SD2.DAT2 | I/O/Z | SD2 data2 is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |
| S23 | | O/Z | McBSP2 data transmit or MultiMedia Card/Secure Digital2 serial clock. At reset, this pin is configured as McBSP2.DX. | BK | Hi-Z |
| | McBSP2.DX | O/Z | McBSP2 serial data transmit. McBSP2.DX is placed in the high-impedance state when not transmitting, when $\overline{\text{RESET}}$ is asserted, or when $\overline{\text{OFF}}$ is low. McBSP2.DX is selected when the External Bus Selection Register has 00 in the Serial Port2 Mode bit field or following reset. | | |
| | MMC2.CLK SD2.CLK | O | MMC2 or SD2 serial clock is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |
| S24 | | I/O/Z | McBSP2 transmit clock or MultiMedia Card/Secure Digital2 data0. At reset, this pin is configured as McBSP2.CLKX. | H | Input |
| | McBSP2.CLKX | I/O/Z | McBSP2 transmit clock. McBSP2.CLKX serves as the serial shift clock for the serial port transmitter. The McBSP2.CLKX pin is configured as input after reset. McBSP2.CLKX is selected when the External Bus Selection Register has 00 in the Serial Port2 Mode bit field or following reset. | | |
| | MMC2.DAT SD2.DAT0 | I/O/Z | MMC2 or SD2 data0 pin is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |
| S25 | | I/O/Z | McBSP2 transmit frame synchronization or Secure Digital2 data3. At reset, this pin is configured as McBSP2.FSX. | | Input |
| | McBSP2.FSX | I/O/Z | McBSP2 frame synchronization. The McBSP2.FSX pulse initiates the data transmit process over McBSP2.DX. McBSP2.FSX is configured as an input following reset. McBSP2.FSX is selected when the External Bus Selection Register has 00 in the Serial Port2 Mode bit field or following reset. | | |
| | SD2.DAT3 | I/O/Z | SD2 data3 is selected when the External Bus Selection Register has 10 in the Serial Port2 Mode bit field. | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **USB** | | | | | |
| DP | | I/O/Z | Differential (positive) receive/transmit. At reset, this pin is configured as input. | | Input |
| DN | | I/O/Z | Differential (negative) receive/transmit. At reset, this pin is configured as input. | | Input |
| PU | | O/Z | Pullup output. This pin is used to pull up the detection resistor required by the USB specification. The pin is internally connected to $USBV_{DD}$ via a software controllable switch (CONN bit of the USBCTL register). | | Hi-Z |
| **A/D** | | | | | |
| AIN0 | | I | Analog Input Channel 0 | | Input |
| AIN1 | | I | Analog Input Channel 1 | | Input |
| AIN2 (BGA only) | | I | Analog Input Channel 2. (BGA package only) | | Input |
| AIN3 (BGA only) | | I | Analog Input Channel 3. (BGA package only) | | Input |
| **TEST/EMULATION PINS** | | | | | |
| TCK | | I | IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. | PU H | Input |
| TDI | | I | IEEE standard 1149.1 test data input. Pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. | PU | Input |
| TDO | | O/Z | IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress. | | Hi-Z |
| TMS | | I | IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK. | PU | Input |
| $\overline{\text{TRST}}$ | | I | IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. This pin has an internal pulldown. | PD FS | Input |
| EMU0 | | I/O/Z | Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as I/O by way of the IEEE standard 1149.1 scan system. | PU | Input |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

**Table 2−3. Signal Descriptions (Continued)**

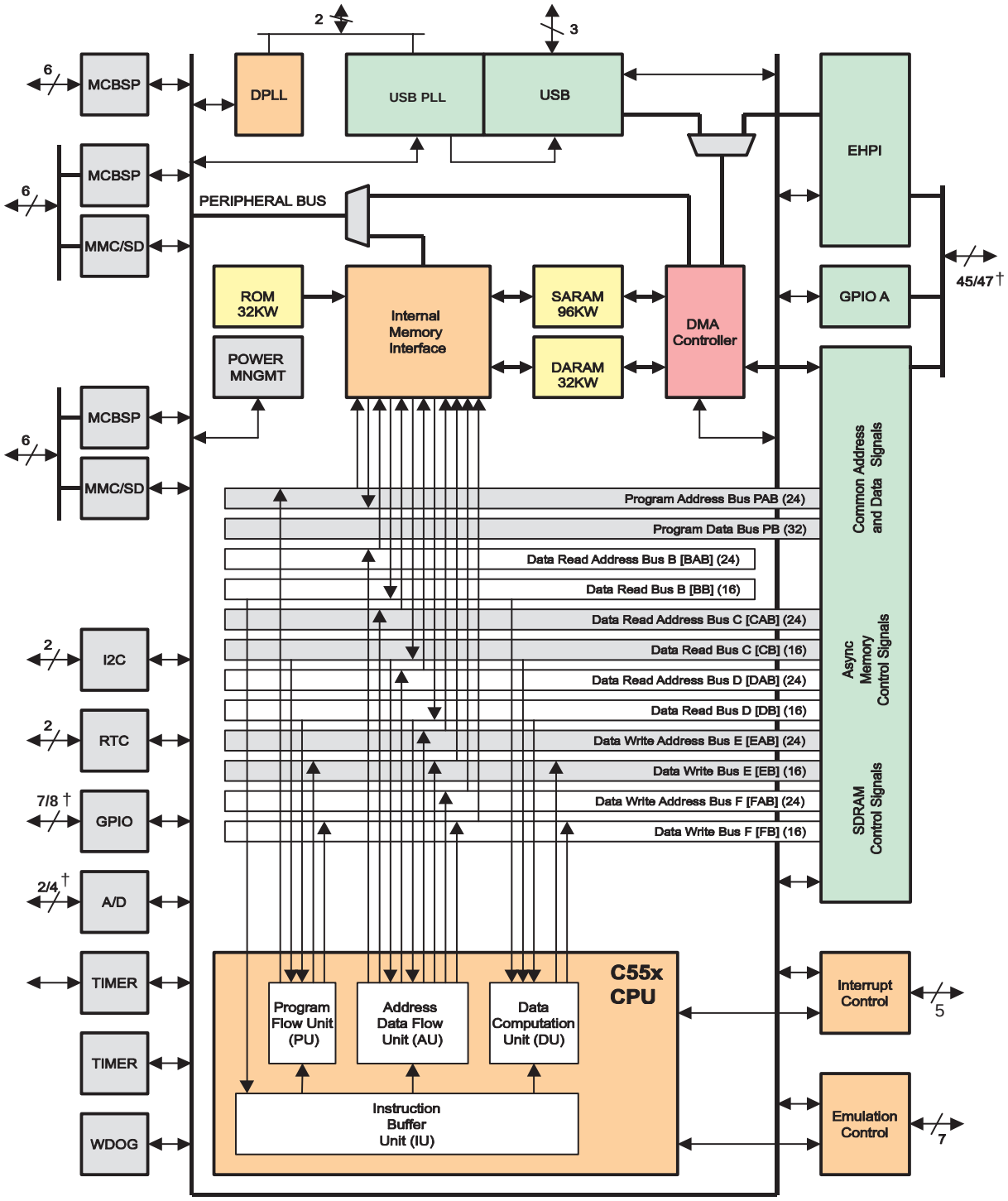
| TERMINAL NAME | MULTIPLEXED SIGNAL NAME | I/O/Z† | FUNCTION | BK‡ | RESET CONDITION |
|---|---|---|---|---|---|
| **TEST/EMULATION PINS (CONTINUED)** | | | | | |
| EMU1/$\overline{OFF}$ | | I/O/Z | Emulator 1 pin/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as I/O by way of IEEE standard 1149.1 scan system. When $\overline{TRST}$ is driven low, EMU1/$\overline{OFF}$ is configured as $\overline{OFF}$. The EMU1/$\overline{OFF}$ signal, when active-low, puts all output drivers into the high-impedance state. Note that $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the $\overline{OFF}$ condition, the following apply: $\overline{TRST}$ = low, EMU0 = high, EMU1/$\overline{OFF}$ = low | PU | Input |
| **SUPPLY PINS** | | | | | |
| $CV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply for the core CPU. | | |
| $DV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply for the I/O pins. | | |
| $USBV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply for the I/O of the USB module (DP, DN , and PU) | | |
| $RDV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply for the I/O pins of the RTC module. | | |
| $RCV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply for the RTC module | | |
| $AV_{DD}$ | | S | Analog Power, + $V_{DD}$. Dedicated power supply for the 10-bit A/D. | | |
| $ADV_{DD}$ | | S | Analog Digital Power, + $V_{DD}$. Dedicated power supply for the digital portion of the 10-bit A/D. | | |
| $USBPLLV_{DD}$ | | S | Digital Power, + $V_{DD}$. Dedicated power supply pin for the USB PLL. | | |
| $V_{SS}$ | | S | Digital Ground. Dedicated ground for the I/O and core pins. | | |
| $AV_{SS}$ | | S | Analog Ground. Dedicated ground for the 10-bit A/D. | | |
| $ADV_{SS}$ | | S | Analog Digital Ground. Dedicated ground for the digital portion of the10-bit A/D. | | |
| $USBPLLV_{SS}$ | | S | Digital Ground. Dedicated ground for the USB PLL. | | |
| **MISCELLANEOUS** | | | | | |
| NC | | | No connection | | |

† I = Input, O = Output, S = Supply, Hi-Z = High-impedance

‡ BK = bus keeper (the bus keeper maintains the previous voltage level during reset or while the output pin is not driven), PU = pullup, PD = pulldown, H = hysteresis input buffer, FS = fail-safe buffer

# 3 Functional Overview

The following functional overview is based on the block diagram in Figure 3−1.




† Number of pins determined by package type.

**Figure 3−1. Block Diagram of the TMS320VC5509A**

## 3.1 Memory

The 5509A supports a unified memory map (program and data accesses are made to the same physical space). The total on-chip memory is 320K bytes (128K 16-bit words of RAM and 32K 16-bit words of ROM).

### *3.1.1 On-Chip Dual-Access RAM (DARAM)*

The DARAM is located in the byte address range 000000h−00FFFFh and is composed of eight blocks of 8K bytes each (see Table 3−1). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). DARAM can be accessed by the internal program, data, or DMA buses. The HPI can only access the first four (32K bytes) DARAM blocks.

**Table 3−1. DARAM Blocks**

| BYTE ADDRESS RANGE | MEMORY BLOCK |
|---|---|
| 000000h − 001FFFh | DARAM 0 (HPI accessible)† |
| 002000h − 003FFFh | DARAM 1 (HPI accessible) |
| 004000h − 005FFFh | DARAM 2 (HPI accessible) |
| 006000h − 007FFFh | DARAM 3 (HPI accessible) |
| 008000h − 009FFFh | DARAM 4 |
| 00A000h − 00BFFFh | DARAM 5 |
| 00C000h − 00DFFFh | DARAM 6 |
| 00E000h − 00FFFFh | DARAM 7 |

† First 192 bytes are reserved for Memory-Mapped Registers (MMRs).

### *3.1.2 On-Chip Single-Access RAM (SARAM)*

The SARAM is located at the byte address range 010000h−03FFFFh and is composed of 24 blocks of 8K bytes each (see Table 3−2). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses.

**Table 3−2. SARAM Blocks**

| BYTE ADDRESS RANGE | MEMORY BLOCK | BYTE ADDRESS RANGE | MEMORY BLOCK |
|---|---|---|---|
| 010000h − 011FFFh | SARAM 0 | 028000h − 029FFFh | SARAM 12 |
| 012000h − 013FFFh | SARAM 1 | 02A000h − 02BFFFh | SARAM 13 |
| 014000h − 015FFFh | SARAM 2 | 02C000h − 02DFFFh | SARAM 14 |
| 016000h − 017FFFh | SARAM 3 | 02E000h − 02FFFFh | SARAM 15 |
| 018000h − 019FFFh | SARAM 4 | 030000h − 031FFFh | SARAM 16 |
| 01A000h − 01BFFFh | SARAM 5 | 032000h − 033FFFh | SARAM 17 |
| 01C000h − 01DFFFh | SARAM 6 | 034000h − 035FFFh | SARAM 18 |
| 01E000h − 01FFFFh | SARAM 7 | 036000h − 037FFFh | SARAM 19 |
| 020000h − 021FFFh | SARAM 8 | 038000h − 039FFFh | SARAM 20 |
| 022000h − 023FFFh | SARAM 9 | 03A000h − 03BFFFh | SARAM 21 |
| 024000h − 025FFFh | SARAM 10 | 03C000h − 03DFFFh | SARAM 22 |
| 026000h − 027FFFh | SARAM 11 | 03E000h − 03FFFFh | SARAM 23 |

### 3.1.3 On-Chip Read-Only Memory (ROM)

The one-wait-state ROM is located at the byte address range FF0000h−FFFFFFh. The ROM is composed of one block of 32K bytes and two 16K-byte blocks, for a total of 64K bytes of ROM. The ROM address space can be mapped by software to the external memory or to the internal ROM.

**NOTE:** Customers can arrange to have the 5509A ROM programmed with contents unique to any particular application. Contact your local Texas Instruments representative for more information on custom ROM programming.

The standard 5509A device includes a bootloader program resident in the ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and byte address range FF0000h−FFFFFFh is directed to external memory space. A hardware reset always clears the MPNMC bit, so it is not possible to disable the ROM at reset. However, the software reset instruction does not affect the MPNMC bit. All three ROM blocks can be accessed by the program, data, or DMA buses. The first 16-bit word access to ROM requires three cycles. Subsequent accesses require two cycles per 16-bit word.

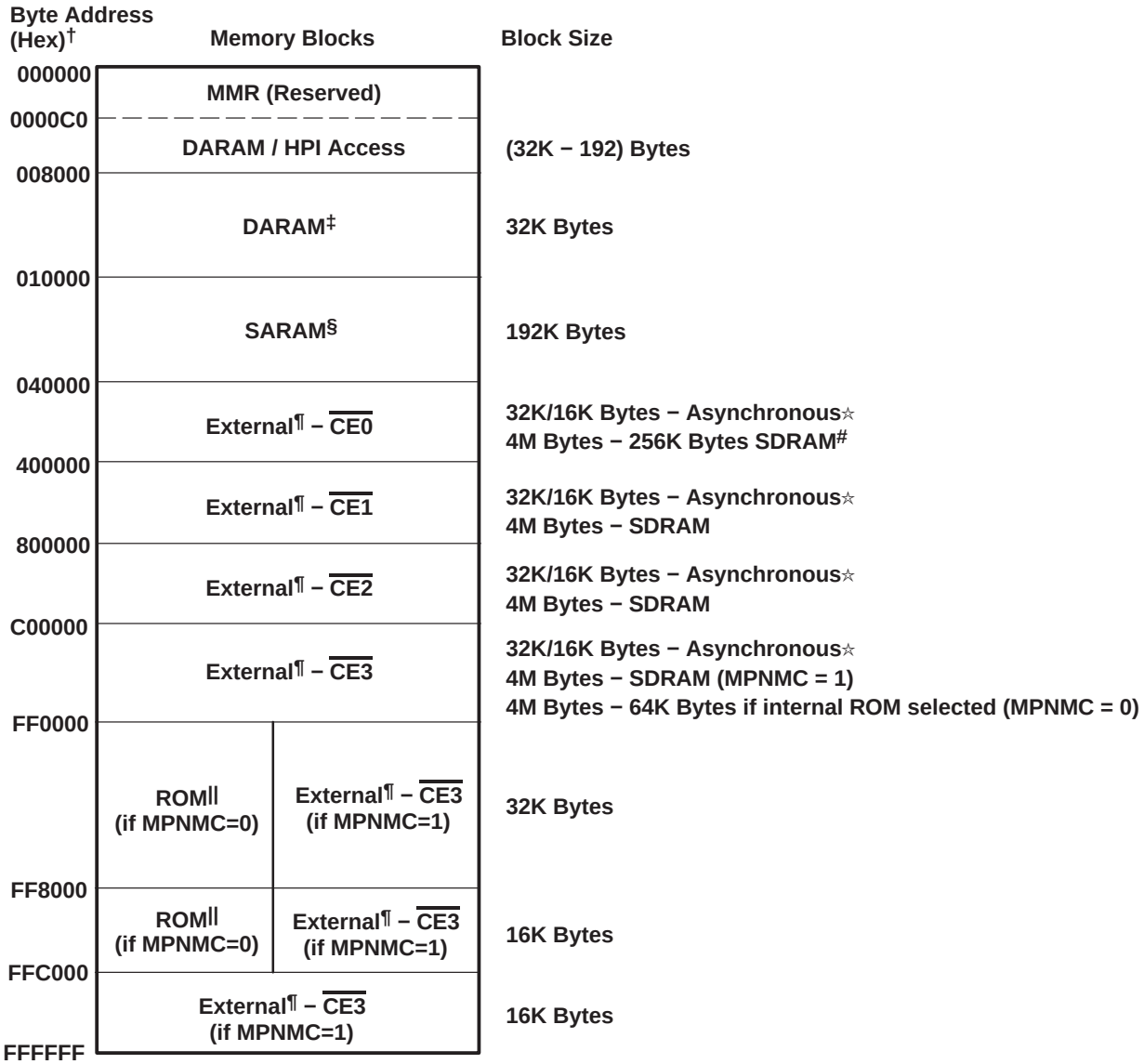
### 3.1.4 Memory Map

The 5509A provides 16M bytes of total memory space composed of on-chip RAM, on-chip ROM, and external memory space supporting a variety of memory types. The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. The 5509A supports 8 blocks of 8K bytes of dual-access RAM. The on-chip, single-access RAM allows one access to a given block per clock cycle. The 5509A supports 24 blocks of 8K byte of single-access RAM.

The remainder of the memory map is external space that is divided into four spaces. Each space has a chip enable decode signal (called CE) that indicates an access to the selected space. The External Memory Interface (EMIF) supports access to asynchronous memories such as SRAM and Flash, and synchronous DRAM.

### 3.1.4.1 PGE Package Memory Map

The PGE package features 14 address bits representing 32K-/16K-byte linear address for asynchronous memories per CE space. Due to address row/column multiplexing, address reach for SDRAM devices is 4M bytes for each CE space. The largest SDRAM device that can be used with the 5509A in a PGE package is 128M-bit SDRAM.

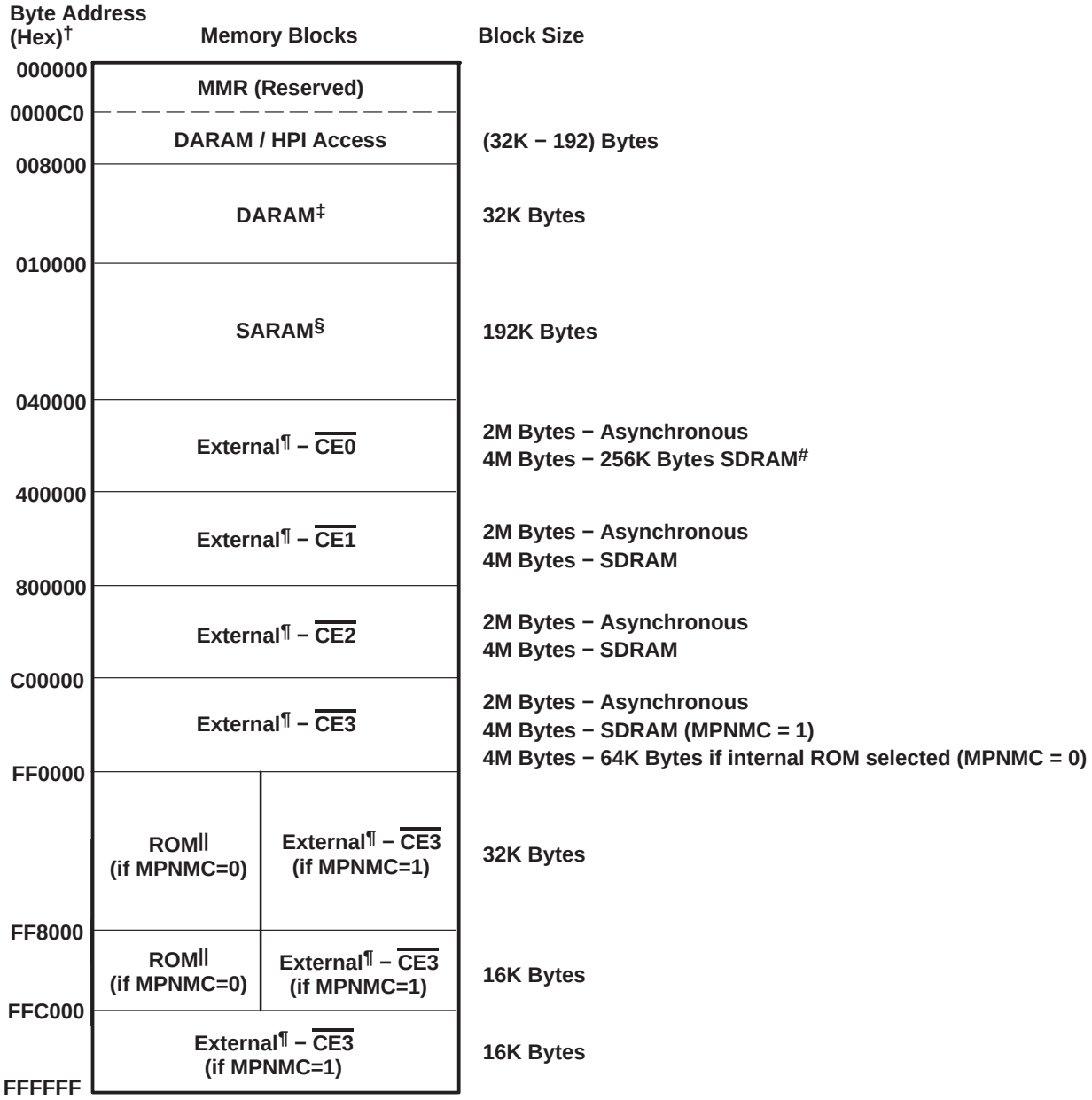



† Address shown represents the first byte address in each block.
‡ Dual-access RAM (DARAM): two accesses per cycle per block, 8 blocks of 8K bytes.
§ Single-access RAM (SARAM): one access per cycle per block, 24 blocks of 8K bytes.
¶ External memory spaces are selected by the chip-enable signal shown ($\overline{CE[0:3]}$). Supported memory types include: asynchronous static RAM (SRAM) and synchronous DRAM (SDRAM).
# The minus 256K bytes consists of 32K-byte DARAM/HPI access, 32K-byte DARAM, and 192K-byte SARAM.
‖ Read-only memory (ROM): one access every two cycles, two blocks of 32K bytes.
☆32K bytes for 16-bit-wide memory. 16K bytes for 8-bit-wide memory.

**Figure 3−2. TMS320VC5509A Memory Map (PGE Package)**

### 3.1.4.2 GHH and ZHH Package Memory Map

The GHH and ZHH packages feature 21 address bits representing 2M-byte linear address for asynchronous memories per CE space. Due to address row/column multiplexing, address reach for SDRAM devices is 4M bytes for each CE space. The largest SDRAM device that can be used with the 5509A in a GHH or ZHH package is 128M-bit SDRAM.




† Address shown represents the first byte address in each block.
‡ Dual-access RAM (DARAM): two accesses per cycle per block, 8 blocks of 8K bytes.
§ Single-access RAM (SARAM): one access per cycle per block, 24 blocks of 8K bytes.
¶ External memory spaces are selected by the chip-enable signal shown ($\overline{CE}$[0:3]). Supported memory types include: asynchronous static RAM (SRAM) and synchronous DRAM (SDRAM).
# The minus 256K bytes consists of 32K-byte DARAM/HPI access, 32K-byte DARAM, and 192K-byte SARAM.
‖ Read-only memory (ROM): one access every two cycles, two blocks of 32K bytes.

**Figure 3−3. TMS320VC5509A Memory Map (GHH and ZHH Packages)**

### 3.1.5 Boot Configuration

The on-chip bootloader provides a method to transfer application code and tables from an external source to the on-chip RAM memory at power up. These options include:

- Enhanced host-port interface (HPI) in multiplexed or nonmultiplexed mode
- External asynchronous memory boot (via the EMIF) from 8-bit-wide or 16-bit-wide memory
- Serial port boot (from McBSP0) with 8-bit or 16-bit data length
- Serial EPROM boot (from McBSP0) supporting EPROMs with 16-bit or 24-bit address
- USB boot
- $I^2C$ EEPROM
- Direct execution from external 16-bit-wide asynchronous memory

External pins select the boot configuration. The values of GPIO[3:0] are sampled, following reset, upon execution of the on-chip bootloader code. It is not possible to disable the bootloader at reset because the 5509A always starts execution from the on-chip ROM following a hardware reset. A summary of boot configurations is shown in Table 3−3. For more information on using the bootloader, see the *Using the TMS320VC5503/VC5507/VC5509/VC5509A Bootloader* Application Report (literature number SPRA375).

**Table 3−3. Boot Configuration Summary**

| GPIO0 | GPIO3 | GPIO2 | GPIO1 | BOOT MODE PROCESS |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reserved |
| 0 | 0 | 0 | 1 | Serial (SPI) EPROM Boot (24-bit address) via McBSP0 |
| 0 | 0 | 1 | 0 | USB |
| 0 | 0 | 1 | 1 | $I^2C$ EEPROM (7-bit address) |
| 0 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 1 | HPI – multiplexed mode |
| 0 | 1 | 1 | 0 | HPI – nonmultiplexed mode |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Execute from 16-bit-wide asynchronous memory (on $\overline{CE1}$ space) |
| 1 | 0 | 0 | 1 | Serial (SPI) EPROM Boot (16-bit address) via McBSP0 |
| 1 | 0 | 1 | 0 | 8-bit asynchronous memory (on $\overline{CE1}$ space) |
| 1 | 0 | 1 | 1 | 16-bit asynchronous memory (on $\overline{CE1}$ space) |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Standard serial boot via McBSP0 (16-bit data) |
| 1 | 1 | 1 | 1 | Standard serial boot via McBSP0 (8-bit data) |

## 3.2 Peripherals

The 5509A supports the following peripherals:

- A Configurable Parallel External Interface supporting either:
  - 16-bit external memory interface (EMIF) for asynchronous memory and/or SDRAM
  - 16-bit enhanced host-port interface (HPI)
- A six-channel direct memory access (DMA) controller
- A programmable phase-locked loop clock generator
- Two 20-bit timers
- Watchdog Timer
- Three serial ports supporting a combination of:
  - up to three multichannel buffered serial ports (McBSPs)
  - up to two MultiMedia/Secure Digital Card Interfaces
- Seven (LQFP) or Eight (BGA) configurable general-purpose I/O pins
- USB full-speed slave interface supporting:
  - Bulk
  - Interrupt
  - Isochronous
- $I^2C$ multi-master and slave interface ($I^2C$ compatible except, no fail-safe I/O buffers)
- Real-time clock with crystal input, separate clock domain and supply pins
- 4-channel (BGA) or 2-channel (LQFP)10-bit Successive Approximation A/D

For detailed information on the C55x™ DSP peripherals, see the following documents:

- *TMS320C55x™ DSP Functional Overview* (literature number SPRU312)
- *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317)

## 3.3 Direct Memory Access (DMA) Controller

The 5509A DMA provides the following features:

- Four standard ports, one for each of the following data resources: DARAM, SARAM, Peripherals and External Memory
- Six channels, which allow the DMA controller to track the context of six independent DMA channels
- Programmable low/high priority for each DMA channel
- One interrupt for each DMA channel
- Event synchronization. DMA transfers in each channel can be dependent on the occurrence of selected events.
- Programmable address modification for source and destination addresses
- Dedicated Idle Domain allows the DMA controller to be placed in a low-power (idle) state under software control.
- Dedicated DMA channel used by the HPI to access internal memory (DARAM)

The 5509A DMA controller allows transfers to be synchronized to selected events. The 5509A supports 19 separate sync events and each channel can be tied to separate sync events independent of the other channels. Sync events are selected by programming the SYNC field in the channel-specific DMA Channel Control Register (DMA_CCR).

### 3.3.1 DMA Channel Control Register (DMA_CCR)

The channel control register (DMA_CCR) bit layouts are shown in Figure 3−4.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DST AMODE | | SRC AMODE | | END PROG | Reserved | REPEAT | AUTO INIT |
| R/W, 00 | | R/W, 00 | | R/W, 0 | R, 0 | R/W, 0 | R/W, 0 |

| 7 | 6 | 5 | 4 | 0 |
|---|---|---|---|---|
| EN | PRIO | FS | SYNC | |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 00000 | |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−4. DMA_CCR Bit Locations**

The SYNC[4:0] bits specify the event that can initiate the DMA transfer for the corresponding DMA channel. The five bits allow several configurations as listed in Table 3−4. The bits are set to zero upon reset. For those synchronization modes with more than one peripheral listed, the Serial Port Mode bit field of the External Bus Selection Register dictates which peripheral event is actually connected to the DMA input.

**Table 3−4. Synchronization Control Function**

| SYNC FIELD IN DMA_CCR | SYNCHRONIZATION MODE |
|---|---|
| 00000b | No event synchronized |
| 00001b | McBSP 0 Receive Event (REVT0) |
| 00010b | McBSP 0 Transmit Event (XEVT0) |
| 00011b | Reserved. These bits should always be written with 0. |
| 00100b | Reserved. These bits should always be written with 0. |
| 00101b | McBSP1/MMC−SD1 Receive Event<br><br>Serial Port 1 Mode:<br>00 = McBSP1 Receive Event (REVT1)<br>01 = MMC/SD1 Receive Event (RMMCEVT1)<br>10 = Reserved<br>11 = Reserved |
| 00110b | McBSP1/MMC−SD1 Transmit Event<br><br>Serial Port 1 Mode:<br>00 = McBSP1 Transmit Event (XEVT1)<br>01 = MMC/SD1 Transmit Event (XMMCEVT1)<br>10 = Reserved<br>11 = reserved |
| 00111b | Reserved. These bits should always be written with 0. |
| 01000b | Reserved. These bits should always be written with 0. |
| 01001b | McBSP2/MMC−SD2 Receive Event<br><br>Serial Port 2 Mode:<br>00 = McBSP2 Receive Event (REVT2)<br>01 = MMC/SD2 Receive Event (RMMCEVT2)<br>10 = Reserved<br>11 = Reserved |

† The $I^2C$ receive event (REVTI2C) and external interrupt 4 (INT4) share a synchronization input to the DMA. When the SYNC field of the DMA_CCR is set to 10011b, the logical OR of these two sources is used for DMA synchronization.

**Table 3−4. Synchronization Control Function (Continued)**

| SYNC FIELD IN DMA_CCR | SYNCHRONIZATION MODE |
|---|---|
| 01010b | McBSP2/MMC−SD2 Transmit Event<br><br>Serial Port 2 Mode:<br>00 = McBSP2 Transmit Event (XEVT2)<br>01 = MMC/SD2 Transmit Event (XMMCEVT2)<br>10 = Reserved<br>11 = Reserved |
| 01011b | Reserved. These bits should always be written with 0. |
| 01100b | Reserved. These bits should always be written with 0. |
| 01101b | Timer 0 Interrupt Event |
| 01110b | Timer 1 Interrupt Event |
| 01111b | External Interrupt 0 |
| 10000b | External Interrupt 1 |
| 10001b | External Interrupt 2 |
| 10010b | External Interrupt 3 |
| 10011b | External Interrupt 4 / $I^2C$ Receive Event (REVTI2C)† |
| 10100b | $I^2C$ Transmit Event (XEVTI2C) |
| Other values | Reserved (Do not use these values) |

† The $I^2C$ receive event (REVTI2C) and external interrupt 4 (INT4) share a synchronization input to the DMA. When the SYNC field of the DMA_CCR is set to 10011b, the logical OR of these two sources is used for DMA synchronization.

## 3.4 $I^2C$ Interface

The TMS320VC5509A includes an $I^2C$ serial port. The $I^2C$ port supports:

- Compatible with Philips $I^2C$ Specification Revision 2.1 (January 2000)
- Operates at 100 Kbps or 400 Kbps
- 7-bit addressing mode
- Master (transmit/receive) and slave (transmit/receive) modes of operation
- Events: DMA, interrupt, or polling

The $I^2C$ module clock *must* be in the range from 7 MHz to 12 MHz. This is necessary for proper operation of the $I^2C$ module. With the $I^2C$ module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The $I^2C$ module clock is derived from the DSP clock divided by a programmable prescaler.

**NOTE:** I/O buffers are *not* fail-safe. The SDA and SCL pins could potentially draw current if the device is powered down and SDA and SCL are driven by other devices connected to the $I^2C$ bus.

## 3.5 Configurable External Buses

The 5509A offers several combinations of configurations for its external parallel port and two serial ports. This allows the system designer to choose the appropriate media interface for its application without the need of a large-pin-count package. The External Bus Selection Register controls the routing of the parallel and serial port signals.

### 3.5.1 External Bus Selection Register (EBSR)

The External Bus Selection Register determines the mapping of the 14 (LQFP) or 21 (BGA) address signals, 16 data signals, and 15 control signals of the external parallel port. It also determines the mapping of the McBSP or MMC/SD ports to Serial Port1 and Serial Port2. The External Bus Selection Register is memory-mapped at port address 0x6C00. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

The reset value of the parallel port mode bit field is determined by the state of the GPIO0 pin at reset. If GPIO0 is high at reset, the full EMIF mode is enabled and the parallel port mode bit field is set to 01. If GPIO0 is low at reset, the HPI multiplexed mode is enabled and the parallel port mode bit field is set to 11. After reset, the parallel port should be selected to function in either EMIF mode or HPI mode. Dynamic switching of the parallel port, once configured, is not recommended.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| **CLKOUT Disable** | **OSC Disable** | **HIDL** | **$\overline{\text{BKE}}$** | **SR STAT** | **HOLD** | **HOLDA** | **CKE SEL** |
| **R/W, 0** | **R/W, 0** | **R/W, 0** | **R/W, 0** | **R/W, 0** | **R/W, 0** | **R/W, 1** | **R/W, 0** |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **CKE EN** | **SR CMD** | **Serial Port2 Mode** | | **Serial Port1 Mode** | | **Parallel Port Mode** | |
| **R/W, 0** | **R/W, 0** | **R/W, 00** | | **R/W, 00** | | **R/W, 01 if GPIO0 = 1<br>11 if GPIO0 = 0** | |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−5. External Bus Selection Register**

**Table 3−5. External Bus Selection Register Bit Field Description**

| BITS | DESCRIPTION |
|---|---|
| 15 | CLKOUT disable.<br><br>CLKOUT disable = 0: CLKOUT enabled<br>CLKOUT disable = 1: CLKOUT disabled |
| 14 | Oscillator disable. Works with IDLE instruction to put the clock generation domain into IDLE mode.<br><br>OSC disable = 0: Oscillator enabled<br>OSC disable = 1: Oscillator disabled |
| 13 | Host mode idle bit. (Applicable **only** if the parallel bus is configured as EHPI.)<br><br>When the parallel bus is set to EHPI mode, the clock domain is not allowed to go to idle, so a host processor can access the DSP internal memory. The HIDL bit works around this restriction and allows the DSP to idle the clock domain and the EHPI. When the clock domain is in idle, a host processor will not be able to access the DSP memory.<br><br>HIDL = 0: Host access to DSP enabled. Idling EHPI and clock domain is not allowed.<br>HIDL = 1: Idles the HPI and the clock domain upon execution of the IDLE instruction when the parallel port mode is set to 10 or 11 selecting HPI mode. In addition, bit 4 of the Idle Control Register must be set to 1 prior to the execution of the IDLE instruction. |
| 12 | Bus keeper enable.†<br><br>$\overline{\text{BKE}}$ = 0: Bus keeper, pullups/pulldowns enabled<br>$\overline{\text{BKE}}$ = 1: Bus keeper, pullups/pulldowns disabled |

† Function available when the port or pins configured as input.

**Table 3−5. External Bus Selection Register Bit Field Description (Continued)**

| BITS | DESCRIPTION |
|---|---|
| 11 | SDRAM self-refresh status bit.<br><br>SR STAT = 0: SDRAM self-refresh signal is not asserted.<br>SR STAT = 1: SDRAM self-refresh signal is asserted |
| 10 | EMIF hold<br><br>HOLD = 0: DSP drives the external memory bus<br>HOLD = 1: Request the external memory bus to be placed in high-impedance so that another device can drive the memory bus |
| 9 | EMIF hold acknowledge.<br><br>HOLDA = 0: DSP indicates that a hold request on the external memory bus has occured, the EMIF completed any pending external bus activity, and placed the external memory bus signals in high-impedance state (address bus, data bus, CE[3:0], AOE, AWE, ARE, SDRAS, SDCAS, SDWE, SDA10, CLKMEM). Once this bit is cleared, an external device can drive the bus.<br>HOLDA = 1: No hold acknowledge |
| 8 | SDRAM CKE pin selection bit.<br><br>CKE SEL = 0: Use XF for SDRAM CKE signal<br>CKE SEL = 1: Use GPIO.4 for SDRAM CKE signal |
| 7 | SDRAM CKE enable bit.<br><br>CKE EN = 0: XF or GPIO.4 operates in normal mode<br>CKE EN = 1: Based on the CKE SEL bit, either XF or GPIO.4 drives the SDRAM CKE pin |
| 6 | SDRAM self-refresh command.<br><br>SR CMD = 0: EMIF will not issue a SDRAM self-refresh command<br>SR CMD = 1: EMIF will issue a SDRAM self-refresh command |
| 5−4 | Serial port2 mode. McBSP2 or MMC/SD2 Mode. Determines the mode of Serial Port2.<br><br>Serial Port2 Mode = 00: McBSP2 mode. The McBSP2 signals are routed to the six pins of Seral Port2.<br>Serial Port2 Mode = 01: MMC/SD2 mode. The MMC/SD2 signals are routed to the six pins of Seral Port2.<br>Serial Port2 Mode = 10: Reserved<br>Serial Port2 Mode = 11: Reserved. |
| 3−2 | Serial port1 mode. McBSP1 or MMC/SD1 Mode. Determines the mode of Serial Port1.<br><br>Serial Port1 Mode = 00: McBSP1 mode. The McBSP1 signals are routed to the six pins of Seral Port1.<br>Serial Port1 Mode = 01: MMC/SD1 mode. The MMC/SD1 signals are routed to the six pins of Seral Port1.<br>Serial Port1 Mode = 10: Reserved<br>Serial Port1 Mode = 11: Reserved. |
| 1−0 | Parallel port mode. EMIF/HPI/GPIO Mode. Determines the mode of the parallel port.<br><br>Parallel Port Mode = 00: Data EMIF mode. The 16 EMIF data signals and 13 EMIF control signals are routed to the corresponding external parallel bus data and control signals. The 14 (LQFP) or 16 (BGA) address bus signals can be used as general-purpose I/O only.<br>Parallel Port Mode = 01: Full EMIF mode. The 14 (LQFP) or 21 (BGA) address signals, 16 data signals, and 15 control signals are routed to the corresponding external parallel bus address, data, and control signals.<br>Parallel Port Mode = 10: Non-multiplexed HPI mode. The HPI is enabled an its 14 address signals, 16 data signals, and 7 control signals are routed to the corresponding address, data, control signals of the external parallel bus. Moreover, 8 control signals of the external parallel bus are used as general-purpose I/O.<br>Parallel Port Mode = 11: Multiplexed HPI mode. The HPI is enabled and its 16 data signals and 10 control signals are routed to the external parallel bus. In addition, 3 control signals of the external parallel bus are used as general-purpose I/O. The 14 (LQFP) or 16 (BGA) external parallel port address bus signals are used as general-purpose I/O. |

† Function available when the port or pins configured as input.

### 3.5.2 Parallel Port

The parallel port of the 5509A consists of 14 (LQFP) or 21 (BGA) address signals, 16 data signals, and 15 control signals. Its 14 bits for address allow it to access 16K (LQFP) or 2M bytes of external memory when using the asynchronous SRAM interface. On the other hand, the SDRAM interface can access the whole external memory space of 16M bytes. The parallel bus supports four different modes:

- **Full EMIF mode:** the EMIF with its 14 (LQFP) or 21 address signals, 16 data signals, and 15 control signals routed to the corresponding external parallel bus address, data, and control signals.
- **Data EMIF mode:** the EMIF with its 16 data signals, and 15 control signals routed to the corresponding external parallel bus data and control signals. The 14 (LQFP) or 16 (BGA) address bus signals can be used as general-purpose I/O signals only.
- **Non-multiplexed HPI mode:** the HPI is enabled with its 14 address signals, 16 data signals, and 8 control signals routed to the corresponding address, data, and control signals of the external parallel bus. Moreover, 7 control signals of the external parallel bus are used as general-purpose I/O.
- **Multiplexed HPI mode:** the HPI is enabled with its 16 data signals and 10 control signals routed to the external parallel bus. In addition, 5 control signals of the external parallel bus are used as general-purpose I/O. The external parallel port's 14 (LQFP) or 16 (BGA) address signals are used as general-purpose I/O.

**Table 3−6. TMS320VC5509A Parallel Port Signal Routing**

| Pin Signal | Data EMIF (00)† | Full EMIF (01)† | Non-Multiplex HPI (10)† | Multiplex HPI (11)† |
|---|---|---|---|---|
| **Address Bus** | | | | |
| **A'[0]** | N/A | EMIF.A[0] (BGA) | N/A | N/A |
| **A[0]** | GPIO.A[0] (LQFP)<br>GPIO.A[0] (BGA) | EMIF.A[0] (LQFP) | HPI.HA[0] (LQFP)<br>HPI.HA[0] (BGA) | GPIO.A[0] (LQFP)<br>GPIO.A[0] (BGA) |
| **A[13:1]** | GPIO.A[13:1] (LQFP)<br>GPIO.A[13:1] (BGA) | EMIF.A[13:1] (LQFP)<br>EMIF.A[13:1] (BGA) | HPI.HA[13:1] (LQFP)<br>HPI.HA[13:1] (BGA) | GPIO.A[13:1] (LQFP)<br>GPIO.A[13:1] (BGA) |
| **A[15:14]** | GPIO.A[15:14] (BGA) | EMIF.A[15:14] (BGA) | N/A | GPIO.A[15:14] (BGA) |
| **A[20:16]‡** | N/A | EMIF.A[20:16] (BGA) | N/A | N/A |
| **Data Bus** | | | | |
| **D[15:0]** | EMIF.D[15:0] | EMIF.D[15:0] | HPI.HD[15:0] | HPI.HD[15:0] |
| **Control Bus** | | | | |
| **C0** | EMIF.$\overline{\text{ARE}}$ | EMIF.$\overline{\text{ARE}}$ | GPIO8 | GPIO8 |
| **C1** | EMIF.$\overline{\text{AOE}}$ | EMIF.$\overline{\text{AOE}}$ | HPI.$\overline{\text{HINT}}$ | HPI.$\overline{\text{HINT}}$ |
| **C2** | EMIF.$\overline{\text{AWE}}$ | EMIF.$\overline{\text{AWE}}$ | HPI.HR/$\overline{\text{W}}$ | HPI.HR/$\overline{\text{W}}$ |
| **C3** | EMIF.ARDY | EMIF.ARDY | HPI.HRDY | HPI.HRDY |
| **C4** | EMIF.$\overline{\text{CE0}}$ | EMIF.$\overline{\text{CE0}}$ | GPIO9 | GPIO9 |
| **C5** | EMIF.$\overline{\text{CE1}}$ | EMIF.$\overline{\text{CE1}}$ | GPIO10 | GPIO10 |
| **C6** | EMIF.$\overline{\text{CE2}}$ | EMIF.$\overline{\text{CE2}}$ | HPI.HCNTL0 | HPI.HCNTL0 |
| **C7** | EMIF.$\overline{\text{CE3}}$ | EMIF.$\overline{\text{CE3}}$ | GPIO11 | HPI.HCNTL1 |
| **C8** | EMIF.$\overline{\text{BE0}}$ | EMIF.$\overline{\text{BE0}}$ | HPI.$\overline{\text{HBE0}}$ | HPI.$\overline{\text{HBE0}}$ |
| **C9** | EMIF.$\overline{\text{BE1}}$ | EMIF.$\overline{\text{BE1}}$ | HPI.$\overline{\text{HBE1}}$ | HPI.$\overline{\text{HBE1}}$ |
| **C10** | EMIF.$\overline{\text{SDRAS}}$ | EMIF.$\overline{\text{SDRAS}}$ | GPIO12 | HPI.$\overline{\text{HAS}}$ |
| **C11** | EMIF.$\overline{\text{SDCAS}}$ | EMIF.$\overline{\text{SDCAS}}$ | HPI.$\overline{\text{HCS}}$ | HPI.$\overline{\text{HCS}}$ |
| **C12** | EMIF.$\overline{\text{SDWE}}$ | EMIF.$\overline{\text{SDWE}}$ | HPI.$\overline{\text{HDS1}}$ | HPI.$\overline{\text{HDS1}}$ |
| **C13** | EMIF.SDA10 | EMIF.SDA10 | GPIO13 | GPIO13 |
| **C14** | EMIF.CLKMEM | EMIF.CLKMEM | HPI.$\overline{\text{HDS2}}$ | HPI.$\overline{\text{HDS2}}$ |

† Represents the Parallel Port Mode bits of the External Bus Selection Register.
‡ A[20:16] of the BGA package always functions as EMIF address pins and they cannot be reconfigured for any other function.

### 3.5.3 Parallel Port Signal Routing

The 5509A allows access to 16-bit-wide (read and write) or 8-bit-wide (read only) asynchronous memory and 16-bit-wide SDRAM. For 16-bit-wide memories, EMIF.A[0] is kept low and is not used. To provide as many address pins as possible, the 5509A routes the parallel port signals as shown in Figure 3−6.

Figure 3−6 shows the addition of the A′[0] signal in the BGA package. This pin is used for asynchronous memory interface only, while the A[0] pin is used with HPI or GPIO. Figure 3−7 summarizes the use of the parallel port signals for memory interfacing.

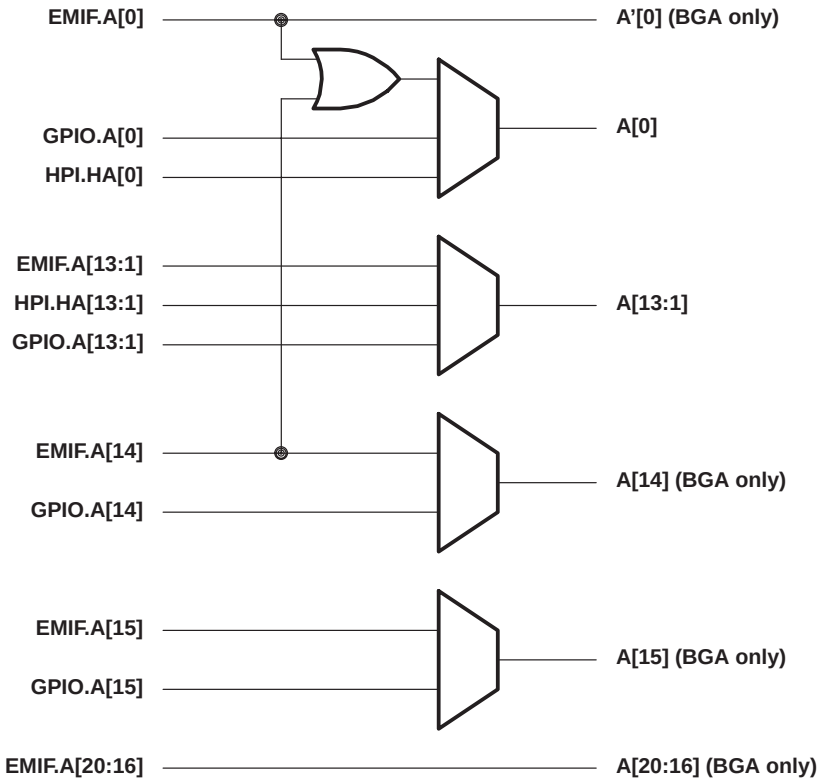
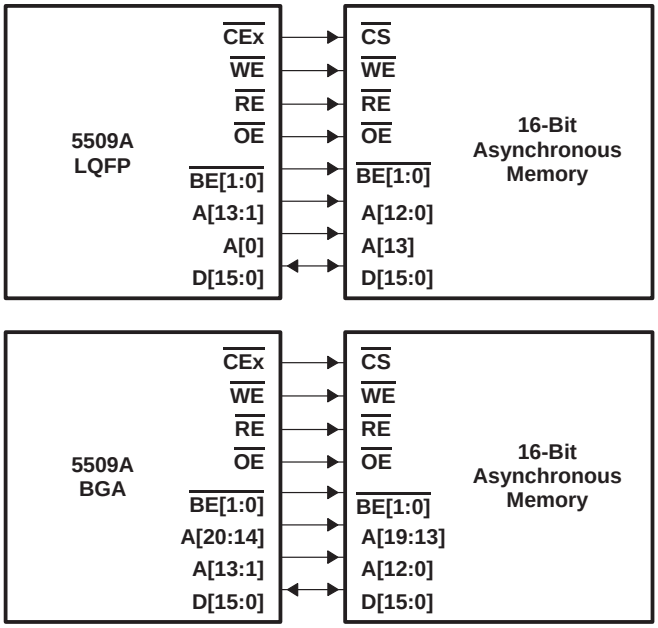
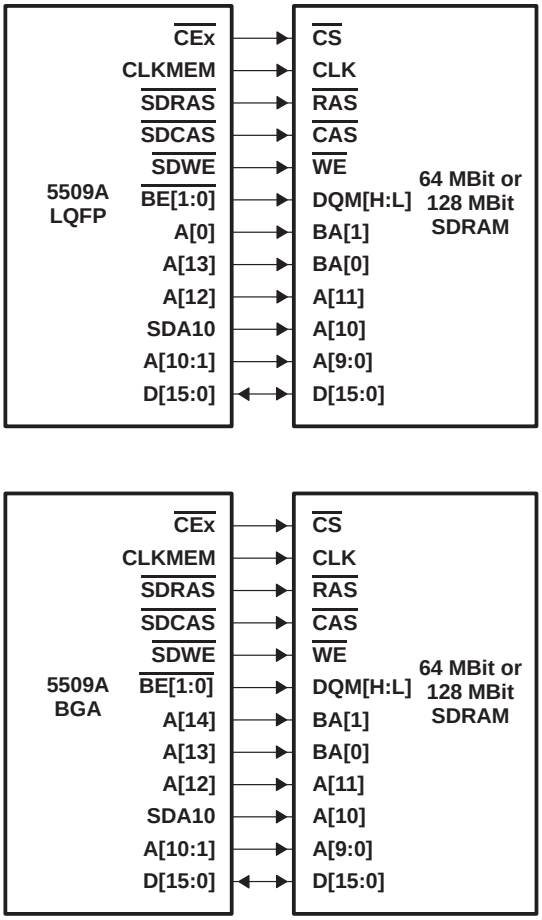



**Figure 3−6. Parallel Port Signal Routing**

**16-Bit-Wide Asynchronous Memory**




**16-Bit-Wide SDRAM**




**8-Bit-Wide Asynchronous Memory**

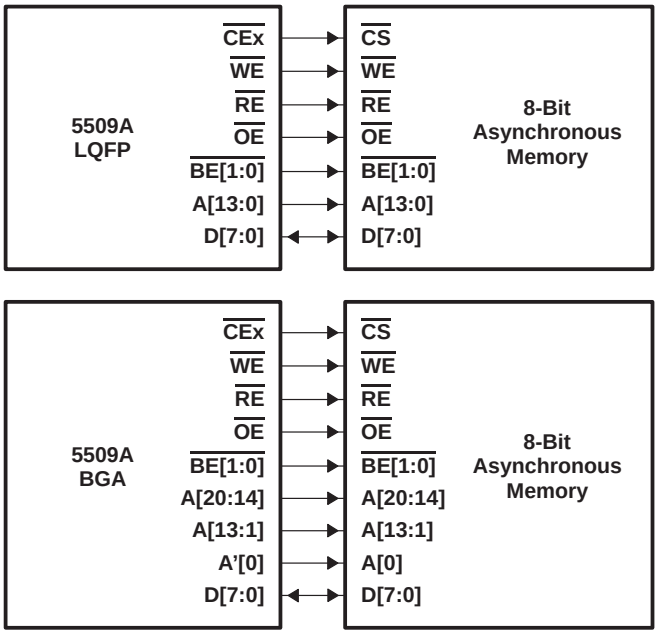



**Figure 3−7. Parallel Port (EMIF) Signal Interface**

### 3.5.4 Serial Ports

The 5509A Serial Port1 and Serial Port2 each consists of six signals that support two different modes:

- **McBSP mode:** all six signals of the McBSP are routed to the six external signals of the serial port.
- **MMC/SD mode:** all six signals of the MultiMedia Card/Secure Digital port are routed to the six external signals of the serial port.

**Table 3−7. TMS320VC5509A Serial Port1 Signal Routing**

| PIN SIGNAL | MCBSP1 (00)† | MMC/SD1 (01)† |
|---|---|---|
| **S10** | McBSP1.CLKR | MMC1.CMD |
| **S11** | McBSP1.DR | MMC1.DAT1 |
| **S12** | McBSP1.FSR | MMC1.DAT2 |
| **S13** | McBSP1.DX | MMC1.CLK |
| **S14** | McBSP1.CLKX | MMC1.DAT0 |
| **S15** | McBSP1.FSX | MMC1.DAT3 |

† Represents the Serial Port1 Mode bits of the External Bus Selection Register.

**Table 3−8. TMS320VC5509A Serial Port2 Signal Routing**

| PIN SIGNAL | MCBSP2 (00)‡ | MMC/SD2 (01)‡ |
|---|---|---|
| **S20** | McBSP2.CLKR | MMC2.CMD |
| **S21** | McBSP2.DR | MMC2.DAT1 |
| **S22** | McBSP2.FSR | MMC2.DAT2 |
| **S23** | McBSP2.DX | MMC2.CLK |
| **S24** | McBSP2.CLKX | MMC2.DAT0 |
| **S25** | McBSP2.FSX | MMC2.DAT3 |

‡ Represents the Serial Port2 Mode bits of the External Bus Selection Register.

## 3.6 General-Purpose Input/Output (GPIO) Ports

### *3.6.1 Dedicated General-Purpose I/O*

The 5509A provides eight dedicated general-purpose input/output pins, GPIO0−GPIO7. Each pin can be indepedently configured as an input or an output using the I/O Direction Register (IODIR). The I/O Data Register (IODATA) is used to monitor the logic state of pins configured as inputs and control the logic state of pins configured as outputs. See Table 3−31 for address information. The description of the IODIR is shown in Figure 3−8 and Table 3−9. The description of IODATA is shown in Figure 3−9 and Table 3−10.

To configure a GPIO pin as an input, clear the direction bit that corresponds to the pin in IODIR to 0. To read the logic state of the input pin, read the corresponding bit in IODATA.

To configure a GPIO pin as an output, set the direction bit that corresponds to the pin in IODIR to 1. To control the logic state of the output pin, write to the corresponding bit in IODATA.

| 15 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Reserved | IO7DIR | IO6DIR | IO5DIR (BGA) | IO4DIR | IO3DIR | IO2DIR | IO1DIR | IO0DIR |
| R−00000000 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−8. I/O Direction Register (IODIR) Bit Layout**

**Table 3−9. I/O Direction Register (IODIR) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−8 | Reserved | 0 | These bits are reserved and are unaffected by writes. |
| 7−0 | IOxDIR† | 0 | **IOx Direction Control Bit.** Controls whether IOx operates as an input or an output.<br>IOxDIR = 0 IOx is configured as an input.<br>IOxDIR = 1 IOx is configured as an output. |

† The GPIO5 pin is available on the BGA package only.

| 15 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Reserved | IO7D | IO6D | IO5D (BGA) | IO4D | IO3D | IO2D | IO1D | IO0D |
| R−00000000 | R/W−pin | R/W−pin | R/W−pin | R/W−pin | R/W−pin | R/W−pin | R/W−pin | R/W−pin |

**LEGEND:** R = Read, W = Write, *pin* = value present on the pin (IO7−IO0 default to inputs after reset)

**Figure 3−9. I/O Data Register (IODATA) Bit Layout**

**Table 3−10. I/O Data Register (IODATA) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−8 | Reserved | 0 | These bits are reserved and are unaffected by writes. |
| 7−0 | IOxD | pin†‡ | **IOx Data Bit.**<br>If IOx is configured as an input (IOxDIR = 0 in IODIR):<br>IOxD = 0 The signal on the IOx pin is low.<br>IOxD = 1 The signal on the IOx pin is high.<br><br>If IOx is configured as an output (IOxDIR = 1 in IODIR):<br>IOxD = 0 Drive the signal on the IOx pin low.<br>IOxD = 1 Drive the signal on the IOx pin high. |

† The GPIO5 pin is available on the BGA package only.
‡ *pin* = value present on the pin (IO7−IO0 default to inputs after reset)

### 3.6.2 Address Bus General-Purpose I/O

The 16 address signals, EMIF.A[15−0], can also be individually enabled as GPIO when the Parallel Port Mode bit field of the External Bus Selection Register is set for Data EMIF (00) or Multiplexed EHPI mode (11). These pins are controlled by three registers: the enable register, AGPIOEN, determines if the pins serve as GPIO or address (Figure 3−10); the direction register, AGPIODIR, determines if the GPIO enabled pin is an input or output (Figure 3−11); and the data register, AGPIODATA, determines the logic states of the pins in general-purpose I/O mode (Figure 3−12). Note that the AGPIOEN bits should be set prior to setting the AGPIODIR bits.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| AIOEN15 (BGA) | AIOEN14 (BGA) | AIOEN13 | AIOEN12 | AIOEN11 | AIOEN10 | AIOEN9 | AIOEN8 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| AIOEN7 | AIOEN6 | AIOEN5 | AIOEN4 | AIOEN3 | AIOEN2 | AIOEN1 | AIOEN0 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−10. Address/GPIO Enable Register (AGPIOEN) Bit Layout**

**Table 3−11. Address/GPIO Enable Register (AGPIOEN) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−0 | AIOENx | 0 | Enable or disable GPIO function of Address Bus of EMIF. AIOEN15 and AIOEN14 are only available in BGA package.<br>AIOENx = 0 GPIO function of Ax line is disabled; i.e., Ax has address function.<br>AIOENx = 1 GPIO function of Ax line is enabled; i.e., Ax has GPIO function. |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| AIODIR15 (BGA) | AIODIR14 (BGA) | AIODIR13 | AIODIR12 | AIODIR11 | AIODIR10 | AIODIR9 | AIODIR8 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AIODIR7 | AIODIR6 | AIODIR5 | AIODIR4 | AIODIR3 | AIODIR2 | AIODIR1 | AIODIR0 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−11. Address/GPIO Direction Register (AGPIODIR) Bit Layout**

**Table 3−12. Address/GPIO Direction Register (AGPIODIR) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−0 | AIODIRx | 0 | Data direction bits that configure the Address Bus configured as I/O pins as either input or output pins. AIODIR15 and AIODIR14 are only available in BGA package.<br>AIODIRx = 0 Configure corresponding pin as an input.<br>AIODIRx = 1 Configure corresponding pin as an output. |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| AIOD15 (BGA) | AIOD14 (BGA) | AIOD13 | AIOD12 | AIOD11 | AIOD10 | AIOD9 | AIOD8 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AIOD7 | AIOD6 | AIOD5 | AIOD4 | AIOD3 | AIOD2 | AIOD1 | AIOD0 |
| R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−12. Address/GPIO Data Register (AGPIODATA) Bit Layout**

**Table 3−13. Address/GPIO Data Register (AGPIODATA) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−0 | AIODx | 0 | Data bits that are used to control the level of the Address Bus configured as I/O output pins, and to monitor the level of the Address Bus configured as I/O input pins. AIOD15 and AIOD14 are only available in BGA package.<br>If AIODIRn = 0, then:<br>AIODx = 0 Corresponding I/O pin is read as a low.<br>AIODx = 1 Corresponding I/O pin is read as a high.<br><br>If AIODIRn = 1, then:<br>AIODx = 0 Set corresponding I/O pin to low.<br>AIODx = 1 Set corresponding I/O pin to high. |

### 3.6.3 EHPI General-Purpose I/O

Six control lines of the External Parallel Bus can also be set as general-purpose I/O when the Parallel Port Mode bit field of the External Bus Selection Register is set to Nonmultiplexed EHPI (10) or Multiplexed EHPI mode (11). These pins are controlled by three registers: the enable register, EHPIGPIOEN, determines if the pins serve as GPIO or address (Figure 3−13); the direction register, EHPIGPIODIR, determines if the GPIO enabled pin is an input or output (Figure 3−14); and the data register, EHPIGPIODATA, determines the logic states of the pins in GPIO mode (Figure 3−15).

| 15 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | GPIOEN13 | GPIOEN12 | GPIOEN11 | GPIOEN10 | GPIOEN9 | GPIOEN8 |
| R, 0000 0000 00 | | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−13. EHPI GPIO Enable Register (EHPIGPIOEN) Bit Layout**

**Table 3−14. EHPI GPIO Enable Register (EHPIGPIOEN) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−6 | Reserved | 0 | Reserved |
| 5−0 | GPIOEN13−GPIOEN8 | 0 | Enable or disable GPIO function of EHPI Control Bus.<br>GPIOENx = 0 GPIO function of GPIOx line is disabled<br>GPIOENx = 1 GPIO function of GPIOx line is enabled |

| 15 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | GPIODIR13 | GPIODIR12 | GPIODIR11 | GPIODIR10 | GPIODIR9 | GPIODIR8 |
| R, 0000 0000 00 | | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−14. EHPI GPIO Direction Register (EHPIGPIODIR) Bit Layout**

**Table 3−15. EHPI GPIO Direction Register (EHPIGPIODIR) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−6 | Reserved | 0 | Reserved |
| 5−0 | GPIODIR13−GPIODIR8 | 0 | Data direction bits that configure the EHPI Control Bus configured as I/O pins as either input or output pins.<br>GPIODIRx = 0 Configure corresponding pin as an input.<br>GPIODIRx = 1 Configure corresponding pin as an output. |

| 15 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| Reserved | GPIOD13 | GPIOD12 | GPIOD11 | GPIOD10 | GPIOD9 | GPIOD8 |
| R, 0000 0000 00 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

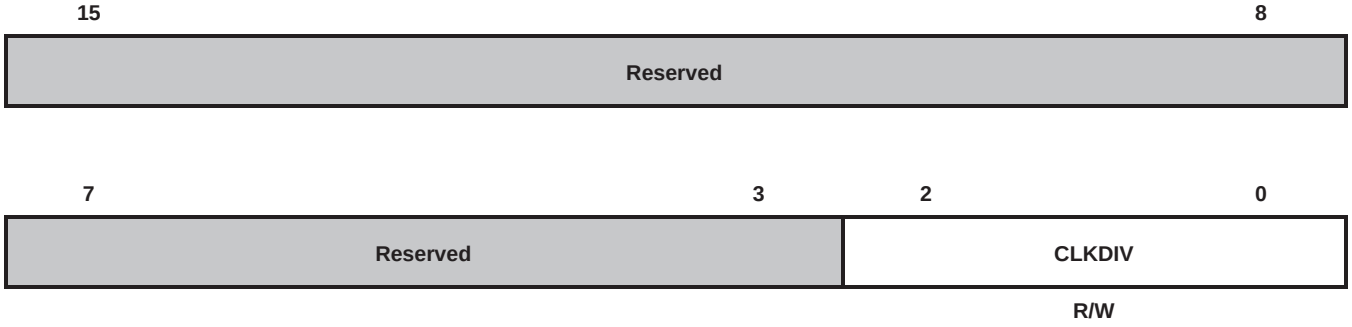
**Figure 3−15. EHPI GPIO Data Register (EHPIGPIODATA) Bit Layout**

**Table 3−16. EHPI GPIO Data Register (EHPIGPIODATA) Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−6 | Reserved | 0 | Reserved |
| 5−0 | GPIOD13−GPIOD8 | 0 | Data bits that are used to control the level of the EHPI Control Bus configured as I/O output pins, and to monitor the level of the EHPI Control Bus configured as I/O input pins.<br>If GPIODIRn = 0, then:<br>GPIODx = 0 Corresponding I/O pin is read as a low.<br>GPIODx = 1 Corresponding I/O pin is read as a high.<br><br>If GPIODIRn = 1, then:<br>GPIODx = 0 Set corresponding I/O pin to low.<br>GPIODx = 1 Set corresponding I/O pin to high. |

## 3.7 System Register

The system register (SYSR) provides control over certain device-specific functions. The register is located at port address 07FDh.




**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−16. System Register Bit Locations**

**Table 3−17. System Register Bit Fields**

| BIT | | FUNCTION |
|---|---|---|
| NUMBER | NAME | |
| 15−3 | Reserved | These bits are reserved and are unaffected by writes. |
| 2−0 | CLKDIV | CLKOUT Divide Factor. Allows the clock present on the CLKOUT pin to be a divided-down version of the internal CPU clock. This field does not affect the programming of the PLL.<br><br>CLKDIV 000 = CLKOUT represents the CPU clock divided by 1<br>CLKDIV 001 = CLKOUT represents the CPU clock divided by 2<br>CLKDIV 010 = CLKOUT represents the CPU clock divided by 4<br>CLKDIV 011 = CLKOUT represents the CPU clock divided by 6<br>CLKDIV 100 = CLKOUT represents the CPU clock divided by 8<br>CLKDIV 101 = CLKOUT represents the CPU clock divided by 10<br>CLKDIV 110 = CLKOUT represents the CPU clock divided by 12<br>CLKDIV 111 = CLKOUT represents the CPU clock divided by 14 |

## 3.8 USB Clock Generation

The USB module can be clocked from either an Analog Phase-Locked Loop (APLL) or a Digital Phase-Locked Loop (DPLL). The APLL is the recommended USB clock source due to better noise tolerance and less long-term jitter than the DPLL. To maintain the backward compatibility, the DPLL is the power-up default clock source for the USB module.

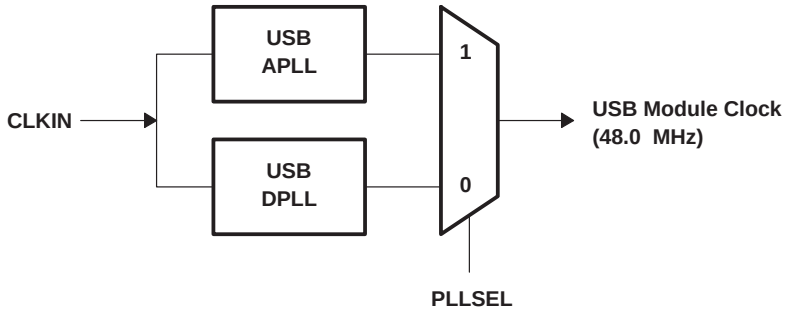



**Figure 3−17. USB Clock Generation**

| 15 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|
| Reserved | | DPLLSTAT | APLLSTAT | PLLSEL |
| R, 0000 0000 0000 0 | | R, 1 | R, 0 | R/W, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−18. USB PLL Selection and Status Register Bit Layout**

**Table 3−18. USB PLL Selection and Status Register Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−3 | Reserved | 0 | Reserved bits. Always write 0. |
| 2 | DPLLSTAT | 1 | Status bit indicating if the DPLL is the source for the USB module clock.<br><br>DPLLSTAT = 0 The DPLL is not the USB module clock source.<br>DPLLSTAT = 1 The DPLL is the USB module clock source. |
| 1 | APLLSTAT | 0 | Status bit indicating if the APLL is the source for the USB module clock.<br><br>APLLSTAT = 0 The APLL is not the USB module clock source.<br>APLLSTAT = 1 The APLL is the USB module clock source. |
| 0 | PLLSEL | 0 | USB module clock source selection bit.<br><br>PLLSEL = 0 DPLL is selected as USB module clock source.<br>PLLSEL = 1 APLL is selected as USB module clock source. |

| 15 | 12 | 11 | 10 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MULT | | DIV | COUNT | | ON | MODE | STAT |
| R/W, 0000 | | R/W, 0 | R, 0000 0000 | | R/W, 0 | R/W, 0 | R, 0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−19. USB APLL Clock Mode Register Bit Layout**

**Table 3−19. USB APLL Clock Mode Register Bit Functions**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 15−12 | MULT | 0 | PLL Multiply Factor K. Multiply Factor K, combined with DIV and MODE, determines the final PLL output clock frequency.<br><br>K = MULT[3:0] + 1 |
| 11 | DIV | 0 | PLL Divide Factor (D) selection bit for PLL multiply mode operation. DIV, combined with K and MODE, determines the final PLL output clock frequency. When the PLL is operating in multiply mode:<br><br>DIV = 0 PLL Divide Factor D = 1<br>DIV = 1 PLL Divide Factor D = 2 if K is odd<br>PLL Divide Factor D = 4 if K is even |
| 10−3 | COUNT | 0 | 8-bit counter for PLL lock timer. When the MODE bit is set to 1, the COUNT field starts decrementing by 1 at the rate of CLKIN/16. When COUNT decrements to 0, the STAT bit is set to 1 and the PLL enabled clock is sourced to the USB module. |

**Table 3−19. USB APLL Clock Mode Register Bit Functions (Continued)**

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---|---|---|---|
| 2 | ON | 0 | PLL Voltage Controlled Oscillator (VCO) enable bit. This bit works in conjunction with MODE to enable or disable the VCO.<br><br>**ON MODE VCO**<br>0 0 OFF<br>1 X ON<br>X 1 ON<br><br>X = Don't care |
| 1 | MODE | 0 | PLL mode selection bit<br><br>MODE = 0 PLL operating in divide mode (VCO bypassed). When the PLL is operating in DIV mode, the PLL Divide Factor (D) is determined by the factor K.<br><br>D = 2 if K = 1 to 15<br>D = 4 if K = 16<br><br>MODE = 1 PLL operating in multiply mode (VCO on). The PLL multiply and divide factors are determined by DIV and K. |
| 0 | STAT | 0 | PLL lock status bit<br><br>STAT = 0 PLL operating in DIV mode (VCO bypassed)<br>STAT = 1 PLL operating in multiply mode (VCO on) |

DIV, combined with MODE and K, defines the final PLL multiplication ratio M/D as indicated below. The USB APLL clock frequency can be simply expressed by:

$$F_{USB\ APLL\ CLK} = F_{CLKIN} \times (M/D)$$

The multiplication factor M and the dividing factor D are defined in Table 3−20.

**Table 3−20. M and D Values Based on MODE, DIV, and K**

| MODE | DIV | K | M | D |
|---|---|---|---|---|
| 0 | X | 1 to 15 | 1 | 2 |
| 0 | X | 16 | 1 | 4 |
| 1 | 0 | 1 to 15 | K | 1 |
| 1 | 0 | 16 | 1 | 1 |
| 1 | 1 | Odd | K | 2 |
| 1 | 1 | Even | K − 1 | 4 |

The USB clock generation and the PLL switching scheme are discussed in detail in the *TMS320VC5507/5509 DSP Universal Serial Bus (USB) Module Reference Guide* (literature number SPRU596) and in the *Using the USB APLL on the TMS320VC5507/5509A* Application Report (literature number SPRA997).

## 3.9 Memory-Mapped Registers

The 5509A has 78 memory-mapped CPU registers that are mapped in data memory space address 0h to 4Fh. Table 3−21 provides a list of the CPU memory-mapped registers (MMRs) available. The corresponding TMS320C54x™ (C54x™) CPU registers are also indicated where applicable.

**Table 3−21. CPU Memory-Mapped Registers**

| C55x REGISTER | C54x REGISTER | WORD ADDRESS (HEX) | DESCRIPTION | BIT FIELD |
|---|---|---|---|---|
| IER0 | IMR | 00 | Interrupt Enable Register 0 | [15−0] |
| IFR0 | IFR | 01 | Interrupt Flag Register 0 | [15−0] |
| ST0_55 | − | 02 | Status Register 0 for C55x | [15−0] |
| ST1_55 | − | 03 | Status Register 1 for C55x | [15−0] |
| ST3_55 | − | 04 | Status Register 3 for C55x | [15−0] |
| − | − | 05 | Reserved | [15−0] |
| ST0 | ST0 | 06 | Status Register ST0 | [15−0] |
| ST1 | ST1 | 07 | Status Register ST1 | [15−0] |
| AC0L | AL | 08 | Accumulator 0 | [15−0] |
| AC0H | AH | 09 | | [31−16] |
| AC0G | AG | 0A | | [39−32] |
| AC1L | BL | OB | Accumulator 1 | [15−0] |
| AC1H | BH | 0C | | [31−16] |
| AC1G | BG | 0D | | [39−32] |
| T3 | TREG | 0E | Temporary Register | [15−0] |
| TRN0 | TRN | 0F | Transition Register | [15−0] |
| AR0 | AR0 | 10 | Auxiliary Register 0 | [15−0] |
| AR1 | AR1 | 11 | Auxiliary Register 1 | [15−0] |
| AR2 | AR2 | 12 | Auxiliary Register 2 | [15−0] |
| AR3 | AR3 | 13 | Auxiliary Register 3 | [15−0] |
| AR4 | AR4 | 14 | Auxiliary Register 4 | [15−0] |
| AR5 | AR5 | 15 | Auxiliary Register 5 | [15−0] |
| AR6 | AR6 | 16 | Auxiliary Register 6 | [15−0] |
| AR7 | AR7 | 17 | Auxiliary Register 7 | [15−0] |
| SP | SP | 18 | Stack Pointer Register | [15−0] |
| BK03 | BK | 19 | Circular Buffer Size Register | [15−0] |
| BRC0 | BRC | 1A | Block Repeat Counter | [15−0] |
| RSA0L | RSA | 1B | Block Repeat Start Address | [15−0] |
| REA0L | REA | 1C | Block Repeat End Address | [15−0] |
| PMST | PMST | 1D | Processor Mode Status Register | [15−0] |
| XPC | XPC | 1E | Program Counter Extension Register | [7−0] |
| − | − | 1F | Reserved | [15−0] |
| T0 | − | 20 | Temporary Data Register 0 | [15−0] |
| T1 | − | 21 | Temporary Data Register 1 | [15−0] |
| T2 | − | 22 | Temporary Data Register 2 | [15−0] |
| T3 | − | 23 | Temporary Data Register 3 | [15−0] |
| AC2L | − | 24 | Accumulator 2 | [15−0] |
| AC2H | − | 25 | | [31−16] |
| AC2G | − | 26 | | [39−32] |

TMS320C54x and C54x are trademarks of Texas Instruments.

**Table 3−21. CPU Memory-Mapped Registers (Continued)**

| C55x REGISTER | C54x REGISTER | WORD ADDRESS (HEX) | DESCRIPTION | BIT FIELD |
|---|---|---|---|---|
| CDP | − | 27 | Coefficient Data Pointer | [15−0] |
| AC3L | − | 28 | Accumulator 3 | [15−0] |
| AC3H | − | 29 | | [31−16] |
| AC3G | − | 2A | | [39−32] |
| DPH | − | 2B | Extended Data Page Pointer | [6−0] |
| MDP05 | − | 2C | Reserved | [6−0] |
| MDP67 | − | 2D | Reserved | [6−0] |
| DP | − | 2E | Memory Data Page Start Address | [15−0] |
| PDP | − | 2F | Peripheral Data Page Start Address | [8−0] |
| BK47 | − | 30 | Circular Buffer Size Register for AR[4−7] | [15−0] |
| BKC | − | 31 | Circular Buffer Size Register for CDP | [15−0] |
| BSA01 | − | 32 | Circular Buffer Start Address Register for AR[0−1] | [15−0] |
| BSA23 | − | 33 | Circular Buffer Start Address Register for AR[2−3] | [15−0] |
| BSA45 | − | 34 | Circular Buffer Start Address Register for AR[4−5] | [15−0] |
| BSA67 | − | 35 | Circular Buffer Start Address Register for AR[6−7] | [15−0] |
| BSAC | − | 36 | Circular Buffer Coefficient Start Address Register | [15−0] |
| BIOS | − | 37 | Data Page Pointer Storage Location for 128-word Data Table | [15−0] |
| TRN1 | − | 38 | Transition Register 1 | [15−0] |
| BRC1 | − | 39 | Block Repeat Counter 1 | [15−0] |
| BRS1 | − | 3A | Block Repeat Save 1 | [15−0] |
| CSR | − | 3B | Computed Single Repeat | [15−0] |
| RSA0H | − | 3C | Repeat Start Address 0 | [23−16] |
| RSA0L | − | 3D | | [15−0] |
| REA0H | − | 3E | Repeat End Address 0 | [23−16] |
| REA0L | − | 3F | | [15−0] |
| RSA1H | − | 40 | Repeat Start Address 1 | [23−16] |
| RSA1L | − | 41 | | [15−0] |
| REA1H | − | 42 | Repeat End Address 1 | [23−16] |
| REA1L | − | 43 | | [15−0] |
| RPTC | − | 44 | Repeat Counter | [15−0] |
| IER1 | − | 45 | Interrupt Enable Register 1 | [15−0] |
| IFR1 | − | 46 | Interrupt Flag Register 1 | [15−0] |
| DBIER0 | − | 47 | Debug IER0 | [15−0] |
| DBIER1 | − | 48 | Debug IER1 | [15−0] |
| IVPD | − | 49 | Interrupt Vector Pointer DSP | [15−0] |
| IVPH | − | 4A | Interrupt Vector Pointer HOST | [15−0] |
| ST2_55 | − | 4B | Status Register 2 for C55x | [15−0] |
| SSP | − | 4C | System Stack Pointer | [15−0] |
| SP | − | 4D | User Stack Pointer | [15−0] |
| SPH | − | 4E | Extended Data Page Pointer for the SP and the SSP | [6−0] |
| CDPH | − | 4F | Main Data Page Pointer for the CDP | [6−0] |

## 3.10 Peripheral Register Description

Each 5509A device has a set of memory-mapped registers associated with peripherals as listed in Table 3−22 through Table 3−39. Some registers use less than 16 bits. When reading these registers, unused bits are always read as 0.

**NOTE:** The CPU access latency to the peripheral memory-mapped registers is 6 CPU cycles. Following peripheral register update(s), the CPU must wait at least 6 CPU cycles before attempting to use that peripheral. When more than one peripheral register is updated in a sequence, the CPU only needs to wait following the final register write. For example, if the EMIF is being reconfigured, the CPU must wait until the very last EMIF register update takes effect before trying to access the external memory. The users should consult the respective peripheral user's guide to determine if a peripheral requires additional time to initialize itself to the new configuration after the register updates take effect.

Before reading or writing to the USB register, the USB module has to be brought out of reset by setting bit 2 of the USB Idle Control and Status Register. Likewise, the MMC/SD must be selected by programming the External Bus Selection Register before reading or writing the MMC/SD module registers.

**Table 3−22. Idle Control, Status, and System Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x0001 | ICR[7:0] | Idle Control Register | xxxx xxxx 0000 0000 |
| 0x0002 | ISTR[7:0] | Idle Status Register | xxxx xxxx 0000 0000 |
| 0x07FD | SYSR[15:0] | System Register | 0000 0000 0000 0000 |

† Hardware reset; x denotes a "don't care."

**Table 3−23. External Memory Interface Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x0800 | EGCR[15:0] | EMIF Global Control Register | xxxx xxxx 0010 xx00 |
| 0x0801 | EMI_RST | EMIF Global Reset Register | xxxx xxxx xxxx xxxx |
| 0x0802 | EMI_BE[13:0] | EMIF Bus Error Status Register | xx00 0000 0000 0000 |
| 0x0803 | CE0_1[14:0] | EMIF CE0 Space Control Register 1 | x010 1111 1111 1111 |
| 0x0804 | CE0_2[15:0] | EMIF CE0 Space Control Register 2 | 0100 1111 1111 1111 |
| 0x0805 | CE0_3[7:0] | EMIF CE0 Space Control Register 3 | xxxx xxxx 0000 0000 |
| 0x0806 | CE1_1[14:0] | EMIF CE1 Space Control Register 1 | x010 1111 1111 1111 |
| 0x0807 | CE1_2[15:0] | EMIF CE1 Space Control Register 2 | 0100 1111 1111 1111 |
| 0x0808 | CE1_3[7:0] | EMIF CE1 Space Control Register 3 | xxxx xxxx 0000 0000 |
| 0x0809 | CE2_1[14:0] | EMIF CE2 Space Control Register 1 | x010 1111 1111 1111 |
| 0x080A | CE2_2[15:0] | EMIF CE2 Space Control Register 2 | 0101 1111 1111 1111 |
| 0x080B | CE2_3[7:0] | EMIF CE2 Space Control Register 3 | xxxx xxxx 0000 0000 |
| 0x080C | CE3_1[14:0] | EMIF CE3 Space Control Register 1 | x010 1111 1111 1111 |
| 0x080D | CE3_2[15:0] | EMIF CE3 Space Control Register 2 | 0101 1111 1111 1111 |
| 0x080E | CE3_3[7:0] | EMIF CE3 Space Control Register 3 | xxxx xxxx 0000 0000 |
| 0x080F | SDC1[15:0] | EMIF SDRAM Control Register 1 | 1111 1001 0100 1000 |
| 0x0810 | SDPER[11:0] | EMIF SDRAM Period Register | xxxx 0000 1000 0000 |
| 0x0811 | SDCNT[11:0] | EMIF SDRAM Counter Register | xxxx 0000 1000 0000 |
| 0x0812 | INIT | EMIF SDRAM Init Register | xxxx xxxx xxxx xxxx |
| 0x0813 | SDC2[9:0] | EMIF SDRAM Control Register 2 | xxxx xx11 1111 1111 |
| 0x0814 | SDC3 | EMIF SDRAM Control Register 3 | 0000 0000 0000 0111 |

† Hardware reset; x denotes a "don't care."

**Table 3−24. DMA Configuration Registers**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **GLOBAL REGISTER** | | | |
| 0x0E00 | DMA_GCR[2:0] | DMA Global Control Register | xxxx xxxx xxxx x000 |
| 0x0E02 | DMA_GSCR | DMA Software Compatibility Register | |
| 0x0E03 | DMA_GTCR | DMA Timeout Control Register | |
| **CHANNEL #0 REGISTERS** | | | |
| 0x0C00 | DMA_CSDP0 | DMA Channel 0 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0C01 | DMA_CCR0[15:0] | DMA Channel 0 Control Register | 0000 0000 0000 0000 |
| 0x0C02 | DMA_CICR0[5:0] | DMA Channel 0 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0C03 | DMA_CSR0[6:0] | DMA Channel 0 Status Register | xxxx xxxx xx00 0000 |
| 0x0C04 | DMA_CSSA_L0 | DMA Channel 0 Source Start Address Register (lower bits) | Undefined |
| 0x0C05 | DMA_CSSA_U0 | DMA Channel 0 Source Start Address Register (upper bits) | Undefined |
| 0x0C06 | DMA_CDSA_L0 | DMA Channel 0 Source Destination Address Register (lower bits) | Undefined |
| 0x0C07 | DMA_CDSA_U0 | DMA Channel 0 Source Destination Address Register (upper bits) | Undefined |
| 0x0C08 | DMA_CEN0 | DMA Channel 0 Element Number Register | Undefined |
| 0x0C09 | DMA_CFN0 | DMA Channel 0 Frame Number Register | Undefined |
| 0x0C0A | DMA_CFI0/ DMA_CSFI0‡ | DMA Channel 0 Frame Index Register/ DMA Channel 0 Source Frame Index Register‡ | Undefined |
| 0x0C0B | DMA_CEI0/ DMA_CSEI0§ | DMA Channel 0 Element Index Register/ DMA Channel 0 Source Element Index Register§ | Undefined |
| 0x0C0C | DMA_CSAC0 | DMA Channel 0 Source Address Counter | Undefined |
| 0x0C0D | DMA_CDAC0 | DMA Channel 0 Destination Address Counter | Undefined |
| 0x0C0E | DMA_CDEI0 | DMA Channel 0 Destination Element Index Register | Undefined |
| 0x0C0F | DMA_CDFI0 | DMA Channel 0 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−24. DMA Configuration Registers (Continued)**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CHANNEL #1 REGISTERS** | | | |
| 0x0C20 | DMA_CSDP1 | DMA Channel 1 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0C21 | DMA_CCR1[15:0] | DMA Channel 1 Control Register | 0000 0000 0000 0000 |
| 0x0C22 | DMA_CICR1[5:0] | DMA Channel 1 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0C23 | DMA_CSR1[6:0] | DMA Channel 1 Status Register | xxxx xxxx xx00 0000 |
| 0x0C24 | DMA_CSSA_L1 | DMA Channel 1 Source Start Address Register (lower bits) | Undefined |
| 0x0C25 | DMA_CSSA_U1 | DMA Channel 1 Source Start Address Register (upper bits) | Undefined |
| 0x0C26 | DMA_CDSA_L1 | DMA Channel 1 Source Destination Address Register (lower bits) | Undefined |
| 0x0C27 | DMA_CDSA_U1 | DMA Channel 1 Source Destination Address Register (upper bits) | Undefined |
| 0x0C28 | DMA_CEN1 | DMA Channel 1 Element Number Register | Undefined |
| 0x0C29 | DMA_CFN1 | DMA Channel 1 Frame Number Register | Undefined |
| 0x0C2A | DMA_CFI1/ DMA_CSFI1‡ | DMA Channel 1 Frame Index Register/ DMA Channel 1 Source Frame Index Register‡ | Undefined |
| 0x0C2B | DMA_CEI1/ DMA_CSEI1§ | DMA Channel 1 Element Index Register/ DMA Channel 1 Source Element Index Register§ | Undefined |
| 0x0C2C | DMA_CSAC1 | DMA Channel 1 Source Address Counter | Undefined |
| 0x0C2D | DMA_CDAC1 | DMA Channel 1 Destination Address Counter | Undefined |
| 0x0C2E | DMA_CDEI1 | DMA Channel 1 Destination Element Index Register | Undefined |
| 0x0C2F | DMA_CDFI1 | DMA Channel 1 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−24. DMA Configuration Registers (Continued)**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CHANNEL #2 REGISTERS** | | | |
| 0x0C40 | DMA_CSDP2 | DMA Channel 2 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0C41 | DMA_CCR2[15:0] | DMA Channel 2 Control Register | 0000 0000 0000 0000 |
| 0x0C42 | DMA_CICR2[5:0] | DMA Channel 2 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0C43 | DMA_CSR2[6:0] | DMA Channel 2 Status Register | xxxx xxxx xx00 0000 |
| 0x0C44 | DMA_CSSA_L2 | DMA Channel 2 Source Start Address Register (lower bits) | Undefined |
| 0x0C45 | DMA_CSSA_U2 | DMA Channel 2 Source Start Address Register (upper bits) | Undefined |
| 0x0C46 | DMA_CDSA_L2 | DMA Channel 2 Source Destination Address Register (lower bits) | Undefined |
| 0x0C47 | DMA_CDSA_U2 | DMA Channel 2 Source Destination Address Register (upper bits) | Undefined |
| 0x0C48 | DMA_CEN2 | DMA Channel 2 Element Number Register | Undefined |
| 0x0C49 | DMA_CFN2 | DMA Channel 2 Frame Number Register | Undefined |
| 0x0C4A | DMA_CFI2/ DMA_CSFI2‡ | DMA Channel 2 Frame Index Register/ DMA Channel 2 Source Frame Index Register‡ | Undefined |
| 0x0C4B | DMA_CEI2/ DMA_CSEI2§ | DMA Channel 2 Element Index Register/ DMA Channel 2 Source Element Index Register§ | Undefined |
| 0x0C4C | DMA_CSAC2 | DMA Channel 2 Source Address Counter | Undefined |
| 0x0C4D | DMA_CDAC2 | DMA Channel 2 Destination Address Counter | Undefined |
| 0x0C4E | DMA_CDEI2 | DMA Channel 2 Destination Element Index Register | Undefined |
| 0x0C4F | DMA_CDFI2 | DMA Channel 2 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−24. DMA Configuration Registers (Continued)**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CHANNEL #3 REGISTERS** | | | |
| 0x0C60 | DMA_CSDP3 | DMA Channel 3 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0C61 | DMA_CCR3[15:0] | DMA Channel 3 Control Register | 0000 0000 0000 0000 |
| 0x0C62 | DMA_CICR3[5:0] | DMA Channel 3 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0C63 | DMA_CSR3[6:0] | DMA Channel 3 Status Register | xxxx xxxx xx00 0000 |
| 0x0C64 | DMA_CSSA_L3 | DMA Channel 3 Source Start Address Register (lower bits) | Undefined |
| 0x0C65 | DMA_CSSA_U3 | DMA Channel 3 Source Start Address Register (upper bits) | Undefined |
| 0x0C66 | DMA_CDSA_L3 | DMA Channel 3 Source Destination Address Register (lower bits) | Undefined |
| 0x0C67 | DMA_CDSA_U3 | DMA Channel 3 Source Destination Address Register (upper bits) | Undefined |
| 0x0C68 | DMA_CEN3 | DMA Channel 3 Element Number Register | Undefined |
| 0x0C69 | DMA_CFN3 | DMA Channel 3 Frame Number Register | Undefined |
| 0x0C6A | DMA_CFI3/ DMA_CSFI3‡ | DMA Channel 3 Frame Index Register/ DMA Channel 3 Source Frame Index Register‡ | Undefined |
| 0x0C6B | DMA_CEI3/ DMA_CSEI3§ | DMA Channel 3 Element Index Register/ DMA Channel 3 Source Element Index Register§ | Undefined |
| 0x0C6C | DMA_CSAC3 | DMA Channel 3 Source Address Counter | Undefined |
| 0x0C6D | DMA_CDAC3 | DMA Channel 3 Destination Address Counter | Undefined |
| 0x0C6E | DMA_CDEI3 | DMA Channel 3 Destination Element Index Register | Undefined |
| 0x0C6F | DMA_CDFI3 | DMA Channel 3 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−24. DMA Configuration Registers (Continued)**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CHANNEL #4 REGISTERS** | | | |
| 0x0C80 | DMA_CSDP4 | DMA Channel 4 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0C81 | DMA_CCR4[15:0] | DMA Channel 4 Control Register | 0000 0000 0000 0000 |
| 0x0C82 | DMA_CICR4[5:0] | DMA Channel 4 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0C83 | DMA_CSR4[6:0] | DMA Channel 4 Status Register | xxxx xxxx xx00 0000 |
| 0x0C84 | DMA_CSSA_L4 | DMA Channel 4 Source Start Address Register (lower bits) | Undefined |
| 0x0C85 | DMA_CSSA_U4 | DMA Channel 4 Source Start Address Register (upper bits) | Undefined |
| 0x0C86 | DMA_CDSA_L4 | DMA Channel 4 Source Destination Address Register (lower bits) | Undefined |
| 0x0C87 | DMA_CDSA_U4 | DMA Channel 4 Source Destination Address Register (upper bits) | Undefined |
| 0x0C88 | DMA_CEN4 | DMA Channel 4 Element Number Register | Undefined |
| 0x0C89 | DMA_CFN4 | DMA Channel 4 Frame Number Register | Undefined |
| 0x0C8A | DMA_CFI4/ DMA_CSFI4‡ | DMA Channel 4 Frame Index Register/ DMA Channel 4 Source Frame Index Register‡ | Undefined |
| 0x0C8B | DMA_CEI4/ DMA_CSEI4§ | DMA Channel 4 Element Index Register/ DMA Channel 4 Source Element Index Register§ | Undefined |
| 0x0C8C | DMA_CSAC4 | DMA Channel 4 Source Address Counter | Undefined |
| 0x0C8D | DMA_CDAC4 | DMA Channel 4 Destination Address Counter | Undefined |
| 0x0C8E | DMA_CDEI4 | DMA Channel 4 Destination Element Index Register | Undefined |
| 0x0C8F | DMA_CDFI4 | DMA Channel 4 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−24. DMA Configuration Registers (Continued)**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CHANNEL #5 REGISTERS** | | | |
| 0x0CA0 | DMA_CSDP5 | DMA Channel 5 Source Destination Parameters Register | 0000 0000 0000 0000 |
| 0x0CA1 | DMA_CCR5[15:0] | DMA Channel 5 Control Register | 0000 0000 0000 0000 |
| 0x0CA2 | DMA_CICR5[5:0] | DMA Channel 5 Interrupt Control Register | xxxx xxxx xx00 0011 |
| 0x0CA3 | DMA_CSR5[6:0] | DMA Channel 5 Status Register | xxxx xxxx xx00 0000 |
| 0x0CA4 | DMA_CSSA_L5 | DMA Channel 5 Source Start Address Register (lower bits) | Undefined |
| 0x0CA5 | DMA_CSSA_U5 | DMA Channel 5 Source Start Address Register (upper bits) | Undefined |
| 0x0CA6 | DMA_CDSA_L5 | DMA Channel 5 Source Destination Address Register (lower bits) | Undefined |
| 0x0CA7 | DMA_CDSA_U5 | DMA Channel 5 Source Destination Address Register (upper bits) | Undefined |
| 0x0CA8 | DMA_CEN5 | DMA Channel 5 Element Number Register | Undefined |
| 0x0CA9 | DMA_CFN5 | DMA Channel 5 Frame Number Register | Undefined |
| 0x0CAA | DMA_CFI5/ DMA_CSFI5‡ | DMA Channel 5 Frame Index Register/ DMA Channel 5 Source Frame Index Register‡ | Undefined |
| 0x0CAB | DMA_CEI5/ DMA_CSEI5§ | DMA Channel 5 Element Index Register/ DMA Channel 5 Source Element Index Register§ | Undefined |
| 0x0CAC | DMA_CSAC5 | DMA Channel 5 Source Address Counter | Undefined |
| 0x0CAD | DMA_CDAC5 | DMA Channel 5 Destination Address Counter | Undefined |
| 0x0CAE | DMA_CDEI5 | DMA Channel 5 Destination Element Index Register | Undefined |
| 0x0CAF | DMA_CDFI5 | DMA Channel 5 Destination Frame Index Register | Undefined |

† Hardware reset: x denotes a “don’t care.”

‡ On the TMS320VC5509, the channel frame index applies to both source and destination and this register behaves as DMA_CFIn. On the TMS320VC5509A, DMA_CSFIn and DMA_CDFIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

§ On the TMS320VC5509, the channel element index applies to both source and destination and this register behaves as DMA_CEIn. On the TMS320VC5509A, DMA_CSEIn and DMA_CDEIn provide separate source and destination frame indexing. The 5509A can be programmed for software compatibility with the 5509 through the Software Compatibility Register (DMA_GSCR).

**Table 3−25. Real-Time Clock Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x1800 | RTCSEC | Seconds Register | 0000 0000 0000 0000 |
| 0x1801 | RTCSECA | Seconds Alarm Register | 0000 0000 0000 0000 |
| 0x1802 | RTCMIN | Minutes Register | 0000 0000 0000 0000 |
| 0x1803 | RTCMINA | Minutes Alarm Register | 0000 0000 0000 0000 |
| 0x1804 | RTCHOUR | Hours Register | 0000 0000 0000 0000 |
| 0x1805 | RTCHOURA | Hours Alarm Register | 0000 0000 0000 0000 |
| 0x1806 | RTCDAYW | Day of the Week Register | 0000 0000 0000 0000 |
| 0x1807 | RTCDAYM | Day of the Month (date) Register | 0000 0000 0000 0000 |
| 0x1808 | RTCMONTH | Month Register | 0000 0000 0000 0000 |
| 0x1809 | RTCYEAR | Year Register | 0000 0000 0000 0000 |
| 0x180A | RTCPINTR | Periodic Interrupt Selection Register | 0000 0000 0000 0000 |
| 0x180B | RTCINTEN | Interrupt Enable Register | 0000 0000 1000 0000 |
| 0x180C | RTCINTFL | Interrupt Flag Register | 0000 0000 0000 0000 |
| 0x180D−0x1BFF | | Reserved | |

† Hardware reset; x denotes a “don’t care.”

**Table 3−26. Clock Generator**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x1C00 | CLKMD[14:0] | Clock Mode Register | 0010 0000 0000 0010 DIV1 mode |
| 0x1E00 | USBDPLL[14:0]‡ | USB DPLL Control Register | If non-USB boot mode:<br>0010 0000 0000 0110 DIV2 mode |
| | | | If USB boot mode:<br>0010 0010 0001 0011 PLL MULT4 mode |
| 0x1E80 | USBPLLSEL[2:0] | USB PLL Selection Register | 0000 0000 0000 0100 |
| 0x1F00 | USBAPLL[15:0] | USB APLL Control Register | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”
‡ DPLL is the power-up default USB clock source.

**Table 3−27. Timers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x1000 | TIM0[15:0] | Timer Count Register, Timer #0 | 1111 1111 1111 1111 |
| 0x1001 | PRD0[15:0] | Period Register, Timer #0 | 1111 1111 1111 1111 |
| 0x1002 | TCR0[15:0] | Timer Control Register, Timer #0 | 0000 0000 0001 0000 |
| 0x1003 | PRSC0[15:0] | Timer Prescaler Register, Timer #0 | xxxx 0000 xxxx 0000 |
| 0x2400 | TIM1[15:0] | Timer Count Register, Timer #1 | 1111 1111 1111 1111 |
| 0x2401 | PRD1[15:0] | Period Register, Timer #1 | 1111 1111 1111 1111 |
| 0x2402 | TCR1[15:0] | Timer Control Register, Timer #1 | 0000 0000 0001 0000 |
| 0x2403 | PRSC1[15:0] | Timer Prescaler Register, Timer #1 | xxxx 0000 xxxx 0000 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−28. Multichannel Serial Port #0**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x2800 | DRR2_0[15:0] | Data Receive Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x2801 | DRR1_0[15:0] | Data Receive Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x2802 | DXR2_0[15:0] | Data Transmit Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x2803 | DXR1_0[15:0] | Data Transmit Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x2804 | SPCR2_0[15:0] | Serial Port Control Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x2805 | SPCR1_0[15:0] | Serial Port Control Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x2806 | RCR2_0[15:0] | Receive Control Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x2807 | RCR1_0[15:0] | Receive Control Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x2808 | XCR2_0[15:0] | Transmit Control Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x2809 | XCR1_0[15:0] | Transmit Control Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x280A | SRGR2_0[15:0] | Sample Rate Generator Register 2, McBSP #0 | 0020 0000 0000 0000 |
| 0x280B | SRGR1_0[15:0] | Sample Rate Generator Register 1, McBSP #0 | 0000 0000 0000 0001 |
| 0x280C | MCR2_0[15:0] | Multichannel Control Register 2, McBSP #0 | 0000 0000 0000 0000 |
| 0x280D | MCR1_0[15:0] | Multichannel Control Register 1, McBSP #0 | 0000 0000 0000 0000 |
| 0x280E | RCERA_0[15:0] | Receive Channel Enable Register Partition A, McBSP #0 | 0000 0000 0000 0000 |
| 0x280F | RCERB_0[15:0] | Receive Channel Enable Register Partition B, McBSP #0 | 0000 0000 0000 0000 |
| 0x2810 | XCERA_0[15:0] | Transmit Channel Enable Register Partition A, McBSP #0 | 0000 0000 0000 0000 |
| 0x2811 | XCERB_0[15:0] | Transmit Channel Enable Register Partition B, McBSP #0 | 0000 0000 0000 0000 |
| 0x2812 | PCR0[15:0] | Pin Control Register, McBSP #0 | 0000 0000 0000 0000 |
| 0x2813 | RCERC_0[15:0] | Receive Channel Enable Register Partition C, McBSP #0 | 0000 0000 0000 0000 |
| 0x2814 | RCERD_0[15:0] | Receive Channel Enable Register Partition D, McBSP #0 | 0000 0000 0000 0000 |
| 0x2815 | XCERC_0[15:0] | Transmit Channel Enable Register Partition C, McBSP #0 | 0000 0000 0000 0000 |
| 0x2816 | XCERD_0[15:0] | Transmit Channel Enable Register Partition D, McBSP #0 | 0000 0000 0000 0000 |
| 0x2817 | RCERE_0[15:0] | Receive Channel Enable Register Partition E, McBSP #0 | 0000 0000 0000 0000 |
| 0x2818 | RCERF_0[15:0] | Receive Channel Enable Register Partition F, McBSP #0 | 0000 0000 0000 0000 |
| 0x2819 | XCERE_0[15:0] | Transmit Channel Enable Register Partition E, McBSP #0 | 0000 0000 0000 0000 |
| 0x281A | XCERF_0[15:0] | Transmit Channel Enable Register Partition F, McBSP #0 | 0000 0000 0000 0000 |
| 0x281B | RCERG_0[15:0] | Receive Channel Enable Register Partition G, McBSP #0 | 0000 0000 0000 0000 |
| 0x281C | RCERH_0[15:0] | Receive Channel Enable Register Partition H, McBSP #0 | 0000 0000 0000 0000 |
| 0x281D | XCERG_0[15:0] | Transmit Channel Enable Register Partition G, McBSP #0 | 0000 0000 0000 0000 |
| 0x281E | XCERH_0[15:0] | Transmit Channel Enable Register Partition H, McBSP #0 | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−29. Multichannel Serial Port #1**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x2C00 | DRR2_1[15:0] | Data Receive Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C01 | DRR1_1[15:0] | Data Receive Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C02 | DXR2_1[15:0] | Data Transmit Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C03 | DXR1_1[15:0] | Data Transmit Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C04 | SPCR2_1[15:0] | Serial Port Control Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C05 | SPCR1_1[15:0] | Serial Port Control Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C06 | RCR2_1[15:0] | Receive Control Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C07 | RCR1_1[15:0] | Receive Control Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C08 | XCR2_1[15:0] | Transmit Control Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C09 | XCR1_1[15:0] | Transmit Control Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C0A | SRGR2_1[15:0] | Sample Rate Generator Register 2, McBSP #1 | 0020 0000 0000 0000 |
| 0x2C0B | SRGR1_1[15:0] | Sample Rate Generator Register 1, McBSP #1 | 0000 0000 0000 0001 |
| 0x2C0C | MCR2_1[15:0] | Multichannel Control Register 2, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C0D | MCR1_1[15:0] | Multichannel Control Register 1, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C0E | RCERA_1[15:0] | Receive Channel Enable Register Partition A, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C0F | RCERB_1[15:0] | Receive Channel Enable Register Partition B, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C10 | XCERA_1[15:0] | Transmit Channel Enable Register Partition A, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C11 | XCERB_1[15:0] | Transmit Channel Enable Register Partition B, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C12 | PCR1[15:0] | Pin Control Register, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C13 | RCERC_1[15:0] | Receive Channel Enable Register Partition C, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C14 | RCERD_1[15:0] | Receive Channel Enable Register Partition D, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C15 | XCERC_1[15:0] | Transmit Channel Enable Register Partition C, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C16 | XCERD_1[15:0] | Transmit Channel Enable Register Partition D, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C17 | RCERE_1[15:0] | Receive Channel Enable Register Partition E, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C18 | RCERF_1[15:0] | Receive Channel Enable Register Partition F, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C19 | XCERE_1[15:0] | Transmit Channel Enable Register Partition E, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C1A | XCERF_1[15:0] | Transmit Channel Enable Register Partition F, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C1B | RCERG_1[15:0] | Receive Channel Enable Register Partition G, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C1C | RCERH_1[15:0] | Receive Channel Enable Register Partition H, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C1D | XCERG_1[15:0] | Transmit Channel Enable Register Partition G, McBSP #1 | 0000 0000 0000 0000 |
| 0x2C1E | XCERH_1[15:0] | Transmit Channel Enable Register Partition H, McBSP #1 | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−30. Multichannel Serial Port #2**

| PORT ADDRESS (WORD) | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x3000 | DRR2_2[15:0] | Data Receive Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x3001 | DRR1_2[15:0] | Data Receive Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x3002 | DXR2_2[15:0] | Data Transmit Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x3003 | DXR1_2[15:0] | Data Transmit Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x3004 | SPCR2_2[15:0] | Serial Port Control Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x3005 | SPCR1_2[15:0] | Serial Port Control Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x3006 | RCR2_2[15:0] | Receive Control Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x3007 | RCR1_2[15:0] | Receive Control Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x3008 | XCR2_2[15:0] | Transmit Control Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x3009 | XCR1_2[15:0] | Transmit Control Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x300A | SRGR2_2[15:0] | Sample Rate Generator Register 2, McBSP #2 | 0020 0000 0000 0000 |
| 0x300B | SRGR1_2[15:0] | Sample Rate Generator Register 1, McBSP #2 | 0000 0000 0000 0001 |
| 0x300C | MCR2_2[15:0] | Multichannel Control Register 2, McBSP #2 | 0000 0000 0000 0000 |
| 0x300D | MCR1_2[15:0] | Multichannel Control Register 1, McBSP #2 | 0000 0000 0000 0000 |
| 0x300E | RCERA_2[15:0] | Receive Channel Enable Register Partition A, McBSP #2 | 0000 0000 0000 0000 |
| 0x300F | RCERB_2[15:0] | Receive Channel Enable Register Partition B, McBSP #2 | 0000 0000 0000 0000 |
| 0x3010 | XCERA_2[15:0] | Transmit Channel Enable Register Partition A, McBSP #2 | 0000 0000 0000 0000 |
| 0x3011 | XCERB_2[15:0] | Transmit Channel Enable Register Partition B, McBSP #2 | 0000 0000 0000 0000 |
| 0x3012 | PCR2[15:0] | Pin Control Register, McBSP #2 | 0000 0000 0000 0000 |
| 0x3013 | RCERC_2[15:0] | Receive Channel Enable Register Partition C, McBSP #2 | 0000 0000 0000 0000 |
| 0x3014 | RCERD_2[15:0] | Receive Channel Enable Register Partition D, McBSP #2 | 0000 0000 0000 0000 |
| 0x3015 | XCERC_2[15:0] | Transmit Channel Enable Register Partition C, McBSP #2 | 0000 0000 0000 0000 |
| 0x3016 | XCERD_2[15:0] | Transmit Channel Enable Register Partition D, McBSP #2 | 0000 0000 0000 0000 |
| 0x3017 | RCERE_2[15:0] | Receive Channel Enable Register Partition E, McBSP #2 | 0000 0000 0000 0000 |
| 0x3018 | RCERF_2[15:0] | Receive Channel Enable Register Partition F, McBSP #2 | 0000 0000 0000 0000 |
| 0x3019 | XCERE_2[15:0] | Transmit Channel Enable Register Partition E, McBSP #2 | 0000 0000 0000 0000 |
| 0x301A | XCERF_2[15:0] | Transmit Channel Enable Register Partition F, McBSP #2 | 0000 0000 0000 0000 |
| 0x301B | RCERG_2[15:0] | Receive Channel Enable Register Partition G, McBSP #2 | 0000 0000 0000 0000 |
| 0x301C | RCERH_2[15:0] | Receive Channel Enable Register Partition H, McBSP #2 | 0000 0000 0000 0000 |
| 0x301D | XCERG_2[15:0] | Transmit Channel Enable Register Partition G, McBSP #2 | 0000 0000 0000 0000 |
| 0x301E | XCERH_2[15:0] | Transmit Channel Enable Register Partition H, McBSP #2 | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−31. GPIO**

| WORD ADDRESS | REGISTER NAME | PIN | DESCRIPTION | RESET VALUE† |
|---|---|---|---|---|
| 0x3400 | IODIR[7:0] | GPIO[7:0] | General-purpose I/O Direction Register | 0000 0000 0000 0000 |
| 0x3401 | IODATA[7:0] | GPIO[7:0] | General-purpose I/O Data Register | 0000 0000 xxxx xxxx |
| 0x4400 | AGPIOEN[15:0] | A[15:0] | Address/GPIO Enable Register | 0000 0000 0000 0000 |
| 0x4401 | AGPIODIR[15:0] | A[15:0] | Address/GPIO Direction Register | 0000 0000 0000 0000 |
| 0x4402 | AGPIODATA[15:0] | A[15:0] | Address/GPIO Data Register | xxxx xxxx xxxx xxxx |
| 0x4403 | EHPIGPIOEN[5:0] | GPIO[13:8] | EHPI/GPIO Enable Register | 0000 0000 0000 0000 |
| 0x4404 | EHPIGPIODIR[5:0] | GPIO[13:8] | EHPI/GPIO Direction Register | 0000 0000 0000 0000 |
| 0x4405 | EHPIGPIODATA[5:0] | GPIO[13:8] | EHPI/GPIO Data Register | 0000 0000 00xx xxxx |

† Hardware reset; x denotes a “don’t care.”

**Table 3−32. Device Revision ID**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | VALUE‡ |
|---|---|---|---|
| 0x3803 | Rev ID[4:1] | Silicon Revision Identification | Rev. 1.0: xxxx xxxx xxx0 000x<br>Rev. 1.1: xxxx xxxx xxx0 001x |

‡ x denotes a “don’t care.”

**Table 3−33. $I^2C$ Module Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x3C00 | I2COAR[9:0]§ | $I^2C$ Own Address Register | 0000 0000 0000 0000 |
| 0x3C01 | I2CIER | $I^2C$ Interrupt Enable Register | 0000 0000 0000 0000 |
| 0x3C02 | I2CSTR | $I^2C$ Status Register | 0000 0001 0000 0000 |
| 0x3C03 | I2CCLKL[15:0] | $I^2C$ Clock Divider Low Register | 0000 0000 0000 0000 |
| 0x3C04 | I2CCLKH[15:0] | $I^2C$ Clock Divider High Register | 0000 0000 0000 0000 |
| 0x3C05 | I2CCNT[15:0] | $I^2C$ Data Count | 0000 0000 0000 0000 |
| 0x3C06 | I2CDRR[7:0] | $I^2C$ Data Receive Register | 0000 0000 0000 0000 |
| 0x3C07 | I2CSAR[9:0] | $I^2C$ Slave Address Register | 0000 0011 1111 1111 |
| 0x3C08 | I2CDXR[7:0] | $I^2C$ Data Transmit Register | 0000 0000 0000 0000 |
| 0x3C09 | I2CMDR[14:0] | $I^2C$ Mode Register | 0000 0000 0000 0000 |
| 0x3C0A | I2CISRC | $I^2C$ Interrupt Source Register | 0000 0000 0000 0000 |
| 0x3C0B | − | Reserved | |
| 0x3C0C | I2CPSC | $I^2C$ Prescaler Register | 0000 0000 0000 0000 |
| 0x3C0D | − | Reserved | |
| 0x3C0E | − | Reserved | |
| 0x3C0F | I2CMDR2 | $I^2C$ Mode Register 2 | 0000 0000 0000 0000 |
| − | I2CRSR | $I^2C$ Receive Shift Register (not accessible to the CPU) | |
| − | I2CXSR | $I^2C$ Transmit Shift Register (not accessible to the CPU) | |

† Hardware reset; x denotes a “don’t care.”

§ Specifies a unique 5509A $I^2C$ address. This register must be set by the programmer. When this device is used in conjunction with another $I^2C$ master device, the register must be programmed to the $I^2C$ slave address (01011xx) allocated by Philips Semiconductor for the 5509A. The two LSBs are programmable address bits.

NOTE: $I^2C$ protocol compatible, no fail-safe buffer.

**Table 3−34. Watchdog Timer Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x4000 | WDTIM[15:0] | WD Timer Counter Register | 1111 1111 1111 1111 |
| 0x4001 | WDPRD[15:0] | WD Timer Period Register | 1111 1111 1111 1111 |
| 0x4002 | WDTCR[13:0] | WD Timer Control Register | 0000 0011 1100 1111 |
| 0x4003 | WDTCR2[15:0] | WD Timer Control Register 2 | 0001 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−35. MMC/SD1 Module Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x4800 | MMCFCLK[8:0] | MMC Function Clock Control Register | 0000 0000 0000 0111 |
| 0x4801 | MMCCTL[10:0] | MMC Control Register | 0000 0000 0000 0000 |
| 0x4802 | MMCCLK[8:0] | MMC Clock Control Register | 0000 0000 0000 1111 |
| 0x4803 | MMCST0[12:0] | MMC Status Register 0 | 0000 0001 0000 0000 |
| 0x4804 | MMCST1[5:0] | MMC Status Register 1 | 0000 0000 0000 0000 |
| 0x4805 | MMCIE[12:0] | MMC Interrupt Enable Register | 0000 0000 0000 0000 |
| 0x4806 | MMCTOR[7:0] | MMC Response Time-Out Register | 0000 0000 0000 0000 |
| 0x4807 | MMCTOD[15:0] | MMC Data Read Time-Out Register | 0000 0000 0000 0000 |
| 0x4808 | MMCBLEN[11:0] | MMC Block Length Register | 0000 0010 0000 0000 |
| 0x4809 | MMCNBLK[15:0] | MMC Number of Blocks Register | 0000 0000 0000 0000 |
| 0x480A | MMCNBLC[15:0] | MMC Number of Blocks Counter Register | 0000 0000 0000 0000 |
| 0x480B | MMCDRR[15:0] | MMC Data Receive Register | 0000 0000 0000 0000 |
| 0x480C | MMCDXR[15:0] | MMC Data Transmit Register | 0000 0000 0000 0000 |
| 0x480D | MMCCMD[15:0] | MMC Command Register | 0000 0000 0000 0000 |
| 0x480E | MMCARGL[15:0] | MMC Argument Register − Low | 0000 0000 0000 0000 |
| 0x480F | MMCARGH[15:0] | MMC Argument Register − High | 0000 0000 0000 0000 |
| 0x4810 | MMCRSP0[15:0] | MMC Response Register 0 | 0000 0000 0000 0000 |
| 0x4811 | MMCRSP1[15:0] | MMC Response Register 1 | 0000 0000 0000 0000 |
| 0x4812 | MMCRSP2[15:0] | MMC Response Register 2 | 0000 0000 0000 0000 |
| 0x4813 | MMCRSP3[15:0] | MMC Response Register 3 | 0000 0000 0000 0000 |
| 0x4814 | MMCRSP4[15:0] | MMC Response Register 4 | 0000 0000 0000 0000 |
| 0x4815 | MMCRSP5[15:0] | MMC Response Register 5 | 0000 0000 0000 0000 |
| 0x4816 | MMCRSP6[15:0] | MMC Response Register 6 | 0000 0000 0000 0000 |
| 0x4817 | MMCRSP7[15:0] | MMC Response Register 7 | 0000 0000 0000 0000 |
| 0x4818 | MMCDRSP[7:0] | MMC Data Response Register | 0000 0000 0000 0000 |
| 0x4819 | Reserved | | |
| 0x481A | MMCCIDX[7:0] | MMC Command Index Register | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

NOTE: The MMC/SD module must be selected in the External Bus Selection Register before any MMC/SD module register read or write attempt.

**Table 3−36. MMC/SD2 Module Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x4C00 | MMCFCLK[8:0] | MMC Function Clock Control Register | 0000 0000 0000 0111 |
| 0x4C01 | MMCCTL[10:0] | MMC Control Register | 0000 0000 0000 0000 |
| 0x4C02 | MMCCLK[8:0] | MMC Clock Control Register | 0000 0000 0000 1111 |
| 0x4C03 | MMCST0[12:0] | MMC Status Register 0 | 0000 0001 0000 0000 |
| 0x4C04 | MMCST1[5:0] | MMC Status Register 1 | 0000 0000 0000 0000 |
| 0x4C05 | MMCIE[12:0] | MMC Interrupt Enable Register | 0000 0000 0000 0000 |
| 0x4C06 | MMCTOR[7:0] | MMC Response Time-Out Register | 0000 0000 0000 0000 |
| 0x4C07 | MMCTOD[15:0] | MMC Data Read Time-Out Register | 0000 0000 0000 0000 |
| 0x4C08 | MMCBLEN[11:0] | MMC Block Length Register | 0000 0010 0000 0000 |
| 0x4C09 | MMCNBLK[15:0] | MMC Number of Blocks Register | 0000 0000 0000 0000 |
| 0x4C0A | MMCNBLC[15:0] | MMC Number of Blocks Counter Register | 0000 0000 0000 0000 |
| 0x4C0B | MMCDRR[15:0] | MMC Data Receive Register | 0000 0000 0000 0000 |
| 0x4C0C | MMCDXR[15:0] | MMC Data Transmit Register | 0000 0000 0000 0000 |
| 0x4C0D | MMCCMD[15:0] | MMC Command Register | 0000 0000 0000 0000 |
| 0x4C0E | MMCARGL[15:0] | MMC Argument Register − Low | 0000 0000 0000 0000 |
| 0x4C0F | MMCARGH[15:0] | MMC Argument Register − High | 0000 0000 0000 0000 |
| 0x4C10 | MMCRSP0[15:0] | MMC Response Register 0 | 0000 0000 0000 0000 |
| 0x4C11 | MMCRSP1[15:0] | MMC Response Register 1 | 0000 0000 0000 0000 |
| 0x4C12 | MMCRSP2[15:0] | MMC Response Register 2 | 0000 0000 0000 0000 |
| 0x4C13 | MMCRSP3[15:0] | MMC Response Register 3 | 0000 0000 0000 0000 |
| 0x4C14 | MMCRSP4[15:0] | MMC Response Register 4 | 0000 0000 0000 0000 |
| 0x4C15 | MMCRSP5[15:0] | MMC Response Register 5 | 0000 0000 0000 0000 |
| 0x4C16 | MMCRSP6[15:0] | MMC Response Register 6 | 0000 0000 0000 0000 |
| 0x4C17 | MMCRSP7[15:0] | MMC Response Register 7 | 0000 0000 0000 0000 |
| 0x4C18 | MMCDRSP[7:0] | MMC Data Response Register | 0000 0000 0000 0000 |
| 0x4C19 | Reserved | | |
| 0x4C1A | MMCCIDX[7:0] | MMC Command Index Register | 0000 0000 0000 0000 |

† Hardware reset; x denotes a “don’t care.”

NOTE: The MMC/SD module must be selected in the External Bus Selection Register before any MMC/SD module register read or write attempt.

**Table 3−37. USB Module Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **DMA CONTEXTS** | | | |
| 0x5800 | Reserved | | |
| 0x5808 | DMAC_O1 | Output Endpoint 1 DMA Context Register | Undefined |
| 0x5810 | DMAC_O2 | Output Endpoint 2 DMA Context Register | Undefined |
| 0x5818 | DMAC_O3 | Output Endpoint 3 DMA Context Register | Undefined |
| 0x5820 | DMAC_O4 | Output Endpoint 4 DMA Context Register | Undefined |
| 0x5828 | DMAC_O5 | Output Endpoint 5 DMA Context Register | Undefined |
| 0x5830 | DMAC_O6 | Output Endpoint 6 DMA Context Register | Undefined |
| 0x5838 | DMAC_O7 | Output Endpoint 7 DMA Context Register | Undefined |
| 0x5840 | Reserved | | |
| 0x5848 | DMAC_I1 | Input Endpoint 1 DMA Context Register | Undefined |
| 0x5850 | DMAC_I2 | Input Endpoint 2 DMA Context Register | Undefined |
| 0x5858 | DMAC_I3 | Input Endpoint 3 DMA Context Register | Undefined |
| 0x5860 | DMAC_I4 | Input Endpoint 4 DMA Context Register | Undefined |
| 0x5868 | DMAC_I5 | Input Endpoint 5 DMA Context Register | Undefined |
| 0x5870 | DMAC_I6 | Input Endpoint 6 DMA Context Register | Undefined |
| 0x5878 | DMAC_I7 | Input Endpoint 7 DMA Context Register | Undefined |
| **DATA BUFFER** | | | |
| 0x5880 | Data Buffers | Contains X/Y data buffers for endpoints 1 – 7 | Undefined |
| 0x6680 | OEB_0 | Output Endpoint 0 Buffer | Undefined |
| 0x66C0 | IEB_0 | Input Endpoint 0 Buffer | Undefined |
| 0x6700 | SUP_0 | Setup Packet for Endpoint 0 | Undefined |
| **ENDPOINT DESCRIPTOR BLOCKS** | | | |
| 0x6708 | OEDB_1 | Output Endpoint 1 Descriptor Register Block | Undefined |
| 0x6710 | OEDB_2 | Output Endpoint 2 Descriptor Register Block | Undefined |
| 0x6718 | OEDB_3 | Output Endpoint 3 Descriptor Register Block | Undefined |
| 0x6720 | OEDB_4 | Output Endpoint 4 Descriptor Register Block | Undefined |
| 0x6728 | OEDB_5 | Output Endpoint 5 Descriptor Register Block | Undefined |
| 0x6730 | OEDB_6 | Output Endpoint 6 Descriptor Register Block | Undefined |
| 0x6738 | OEDB_7 | Output Endpoint 7 Descriptor Register Block | Undefined |
| 0x6740 | Reserved | | |
| 0x6748 | IEDB_1 | Input Endpoint 1 Descriptor Register Block | Undefined |
| 0x6750 | IEDB_2 | Input Endpoint 2 Descriptor Register Block | Undefined |
| 0x6758 | IEDB_3 | Input Endpoint 3 Descriptor Register Block | Undefined |
| 0x6760 | IEDB_4 | Input Endpoint 4 Descriptor Register Block | Undefined |
| 0x6768 | IEDB_5 | Input Endpoint 5 Descriptor Register Block | Undefined |
| 0x6770 | IEDB_6 | Input Endpoint 6 Descriptor Register Block | Undefined |
| 0x6778 | IEDB_7 | Input Endpoint 7 Descriptor Register Block | Undefined |

† Hardware reset; x denotes a “don’t care.”

NOTE: The USB module must be brought out of reset by setting bit 2 of the USB Idle Control and Status Register before any USB module register read or write attempt.

**Table 3−37. USB Module Registers (Continued)**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| **CONTROL AND STATUS REGISTERS** | | | |
| 0x6780 | IEPCNF_0 | Input Endpoint 0 Configuration | xxxx xxxx 0000 0000 |
| 0x6781 | IEPBCNT_0 | Input Endpoint 0 Byte Count | xxxx xxxx 1000 0000 |
| 0x6782 | OEPCNF_0 | Output Endpoint 0 Configuration | xxxx xxxx 0000 0000 |
| 0x6783 | OEPBCNT_0 | Output Endpoint 0 Byte Count | xxxx xxxx 0000 0000 |
| 0x6784 − 0x6790 | Reserved | | |
| 0x6791 | GLOBCTL | Global Control Register | xxxx xxxx 0000 0000 |
| 0x6792 | VECINT | Vector Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6793 | IEPINT | Input Endpoint Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6794 | OEPINT | Output Endpoint Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6795 | IDMARINT | Input DMA Reload Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6796 | ODMARINT | Output DMA Reload Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6797 | IDMAGINT | Input DMA Go Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6798 | ODMAGINT | Output DMA Go Interrupt Register | xxxx xxxx 0000 0000 |
| 0x6799 | IDMAMSK | Input DMA Interrupt Mask Register | xxxx xxxx 0000 0000 |
| 0x679A | ODMAMSK | Output DMA Interrupt Mask Register | xxxx xxxx 0000 0000 |
| 0x679B | IEDBMSK | Input EDB Interrupt Mask Register | xxxx xxxx 0000 0000 |
| 0x679C | OEDBMSK | Output EDB Interrupt Mask Register | xxxx xxxx 0000 0000 |
| | | | |
| 0x67F8 | FNUML | Frame Number Low Register | xxxx xxxx 0000 0000 |
| 0x67F9 | FNUMH | Frame Number High | xxxx xxxx xxxx x000 |
| 0x67FA | PSOFTMR | PreSOF Interrupt Timer Register | xxxx xxxx 0000 0000 |
| | | | |
| 0x67FC | USBCTL | USB Control Register | xxxx xxxx 0101 0000 |
| 0x67FD | USBMSK | USB Interrupt Mask Register | xxxx xxxx 0000 0000 |
| 0x67FE | USBSTA | USB Status Register | xxxx xxxx 0000 0000 |
| 0x67FF | FUNADR | Function Address Register | xxxx xxxx x000 0000 |
| 0x7000 | USBIDLECTL | USB Idle Control and Status Register | xxxx xxxx xxxx x000 |

† Hardware reset; x denotes a “don’t care.”

NOTE: The USB module must be brought out of reset by setting bit 2 of the USB Idle Control and Status Register before any USB module register read or write attempt.

**Table 3−38. Analog-to-Digital Controller (ADC) Registers**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x6800 | ADCCTL[15:11] | ADC Control Register | 0111 0000 0000 0000 |
| 0x6801 | ADCDATA[15:0] | ADC Data Register | 0111 0000 0000 0000 |
| 0x6802 | ADCCLKDIV[15:0] | ADC Function Clock Divider Register | 0000 0000 0000 1111 |
| 0x6803 | ADCCLKCTL[8:0] | ADC Clock Control Register | 0000 0000 0000 0111 |

† Hardware reset; x denotes a “don’t care.”

**Table 3−39. External Bus Selection Register**

| WORD ADDRESS | REGISTER NAME | DESCRIPTION | RESET VALUE† |
|---|---|---|---|
| 0x6C00 | EBSR[15:0] | External Bus Selection Register | 0000 0000 0000 0011‡ |

† Hardware reset; x denotes a “don’t care.”
‡ The reset value is 0000 0000 0000 0001 if GPIO0 = 1; the value is 0000 0000 0000 0011 if GPIO0 = 0.

## 3.11 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3−40.

**Table 3−40. Interrupt Table**

| NAME | SOFTWARE (TRAP) EQUIVALENT | RELATIVE LOCATION† (HEX BYTES) | PRIORITY | FUNCTION |
|---|---|---|---|---|
| RESET | SINT0 | 0 | 0 | Reset (hardware and software) |
| NMI‡ | SINT1 | 8 | 1 | Nonmaskable interrupt |
| BERR | SINT24 | C0 | 2 | Bus Error interrupt |
| INT0 | SINT2 | 10 | 3 | External interrupt #0 |
| INT1 | SINT16 | 80 | 4 | External interrupt #1 |
| INT2 | SINT3 | 18 | 5 | External interrupt #2 |
| TINT0 | SINT4 | 20 | 6 | Timer #0 interrupt |
| RINT0 | SINT5 | 28 | 7 | McBSP #0 receive interrupt |
| XINT0 | SINT17 | 88 | 8 | McBSP #0 transmit interrupt |
| RINT1 | SINT6 | 30 | 9 | McBSP #1 receive interrupt |
| XINT1/MMCSD1 | SINT7 | 38 | 10 | McBSP #1 transmit interrupt, MMC/SD #1 interrupt |
| USB | SINT8 | 40 | 11 | USB interrupt |
| DMAC0 | SINT18 | 90 | 12 | DMA Channel #0 interrupt |
| DMAC1 | SINT9 | 48 | 13 | DMA Channel #1 interrupt |
| DSPINT | SINT10 | 50 | 14 | Interrupt from host |
| INT3/WDTINT | SINT11 | 58 | 15 | External interrupt #3 or Watchdog timer interrupt |
| INT4/RTC§ | SINT19 | 98 | 16 | External interrupt #4 or RTC interrupt |
| RINT2 | SINT12 | 60 | 17 | McBSP #2 receive interrupt |
| XINT2/MMCSD2 | SINT13 | 68 | 18 | McBSP #2 transmit interrupt , MMC/SD #2 interrupt |
| DMAC2 | SINT20 | A0 | 19 | DMA Channel #2 interrupt |
| DMAC3 | SINT21 | A8 | 20 | DMA Channel #3 interrupt |
| DMAC4 | SINT14 | 70 | 21 | DMA Channel #4 interrupt |
| DMAC5 | SINT15 | 78 | 22 | DMA Channel #5 interrupt |
| TINT1 | SINT22 | B0 | 23 | Timer #1 interrupt |
| IIC | SINT23 | B8 | 24 | $I^2C$ interrupt |
| DLOG | SINT25 | C8 | 25 | Data Log interrupt |
| RTOS | SINT26 | D0 | 26 | Real-time Operating System interrupt |
| − | SINT27 | D8 | 27 | Software interrupt #27 |
| − | SINT28 | E0 | 28 | Software interrupt #28 |
| − | SINT29 | E8 | 29 | Software interrupt #29 |
| − | SINT30 | F0 | 30 | Software interrupt #30 |
| − | SINT31 | F8 | 31 | Software interrupt #31 |

† Absolute addresses of the interrupt vector locations are determined by the contents of the IVPD and IVPH registers. Interrupt vectors for interrupts 0−15 and 24−31 are relative to IVPD. Interrupt vectors for interrupts 16−23 are relative to IVPH.

‡ The NMI pin is internally tied high. However, NMI interrupt vector can be used for SINT1 and Watchdog Timer Interrupt.

§ It is recommended that either the INT4 or RTC interrupt be used. If both INT4 and RTC interrupts are used, one interrupt event can potentially hold off the other interrupt. For example, if INT4 is asserted first and held low, the RTC interrupt will not be recognized until the INT4 pin is back to high-logic state again. The INT4 pin must be pulled high if only the RTC interrupt is used.

### 3.11.1 IFR and IER Registers

The IFR0 (Interrupt Flag Register 0) and IER0 (Interrupt Enable Register 0) bit layouts are shown in Figure 3−20.

**NOTE:** Some of the interrupts are shared between multiple interrupt sources. All sources for a particular bit are internally combined using a logic OR function so that no additional user configuration is required to select the interrupt source. In the case of the serial port, the shared functions are mutually exclusive so that only one of the interrupt sources will be active at a time in a given system. For example: It is not possible to use McBSP2 and MMC/SD2 simultaneously. However, in the case of INT3/WDTINT it is possible to have active interrupts simultaneously from both the external INT3 source and the watchdog timer. When an interrupt is detected in this bit, the watchdog timer status register should be polled to determine if the watchdog timer is the interrupt source.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DMAC5 | DMAC4 | XINT2/ MMCSD2 | RINT2 | INT3/ WDTINT | DSPINT | DMAC1 | USB |
| R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| XINT1/ MMCSD1 | RINT1 | RINT0 | TINT0 | INT2 | INT0 | Reserved | |
| R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−00 | |

**LEGEND:** R = Read, W = Write, *n* = value after reset

**Figure 3−20. IFR0 and IER0 Bit Locations**

**Table 3−41. IFR0 and IER0 Register Bit Fields**

| BIT | | FUNCTION |
|---|---|---|
| NUMBER | NAME | |
| 15 | DMAC5 | DMA channel 5 interrupt flag/mask bit |
| 14 | DMAC4 | DMA channel 4 interrupt flag/mask bit |
| 13 | XINT2/MMCSD2 | This bit is used as either the McBSP2 transmit interrupt flag/mask bit, the MMC/SD2 interrupt flag/mask bit. |
| 12 | RINT2 | McBSP2 receive interrupt flag/mask bit. |
| 11 | INT3/WDTINT | This bit is used as either the external user interrupt 3 flag/mask bit, or the watchdog timer interrupt flag/mask bit. |
| 10 | DSPINT | HPI host-to-DSP interrupt flag/mask. |
| 9 | DMAC1 | DMA channel 1 interrupt flag/mask bit |
| 8 | USB | USB interrupt flag/mask bit. |
| 7 | XINT1/MMCSD1 | This bit is used as either the McBSP1 transmit interrupt flag/mask bit, the MMC/SD1 interrupt flag/mask bit. |
| 6 | RINT1 | McBSP1 receive interrupt flag/mask bit. |
| 5 | RINT0 | McBSP0 receive interrupt flag bit |
| 4 | TINT0 | Timer 0 interrupt flag bit |
| 3 | INT2 | External interrupt 2 flag bit |
| 2 | INT0 | External interrupt 0 flag bit |
| 1−0 | − | Reserved for future expansion. These bits should always be written with 0. |

The IFR1 (Interrupt Flag Register 1) and IER1 (Interrupt Enable Register 1) bit layouts are shown in Figure 3−21.

**NOTE:** It is possible to have active interrupts simultaneously from both the external interrupt 4 (INT4) and the real-time clock (RTC). When an interrupt is detected in this bit, the real-time clock status register should be polled to determine if the real-time clock is the source of the interrupt.

| 15 | | | | | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | RTOS | DLOG | BERR |
| R/W−00000† | | | | | | R/W−0 | R/W−0 | R/W−0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| I2C | TINT1 | DMAC3 | DMAC2 | INT4/RTC | DMAC0 | XINT0 | INT1 |
| R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 | R/W−0 |

**LEGEND:** R = Read, W = Write, *n* = value after reset
† Always write zeros.

**Figure 3−21. IFR1 and IER1 Bit Locations**

**Table 3−42. IFR1 and IER1 Register Bit Fields**

| BIT | | FUNCTION |
|---|---|---|
| NUMBER | NAME | |
| 15−11 | – | Reserved for future expansion. These bits should always be written with 0. |
| 10 | RTOS | Real-time operating system interrupt flag/mask bit |
| 9 | DLOG | Data log interrupt flag/mask bit |
| 8 | BERR | Bus error interrupt flag/mask bit |
| 7 | I2C | I2C interrupt flag/mask bit |
| 6 | TINT1 | Timer 1 interrupt flag/mask bit |
| 5 | DMAC3 | DMA channel 3 interrupt flag/mask bit |
| 4 | DMAC2 | DMA channel 2 interrupt flag/mask bit |
| 3 | INT4/RTC | This bit can be used as either the external user interrupt 4 flag/mask bit, or the real-time clock interrupt flag/mask bit. |
| 2 | DMAC0 | DMA channel 0 interrupt flag/mask bit |
| 1 | XINT0 | McBSP transmit 0 interrupt flag/mask bit |
| 0 | INT1 | External user interrupt 1 flag/mask bit |

### 3.11.2 Interrupt Timing

The external interrupts ($\overline{\text{INT}}$[4:0]) are synchronized to the CPU by way of a two-flip-flop synchronizer. The interrupt inputs are sampled on falling edges of the CPU clock. A sequence of 1-1-0-0-0 on consecutive cycles on the interrupt pin is required for an interrupt to be detected. Therefore, the minimum low pulse duration on the external interrupts on the 5509A is three CPU clock periods.

### 3.11.3 Waking Up From IDLE Condition

One of the following four events can wake up the CPU from IDLE:

- Hardware Reset
- External Interrupt
- RTC Interrupt
- USB Event (Reset or Resume)

#### 3.11.3.1 Waking Up From IDLE With Oscillator Disabled

With an external interrupt, a RTC interrupt, or an USB resume/reset, the clock generation circuit wakes up the oscillator and enables the USB PLL to determine the oscillator stable time. In the case of the interrupt being disabled by clearing the associated bit in the Interrupt Enable Register (IERx), the CPU is not “woken up”. If the interrupt due to the wake-up event is enabled, the interrupt is sent to the CPU only after the oscillator is stabilized and the USB PLL is locked. If the external interrupt serves as the wake-up event, the interrupt line must stay low for a minimum of 3 CPU cycles after the oscillator is stabilized to wake up the CPU. Otherwise, only the clock domain will wake up and another external interrupt will be needed to wake up the CPU.

Once out of IDLE, any system not using the USB should put the USB module in idle mode to reduce power consumption.

For more details on the TMS320VC5509A oscillator-disable process, see the *Disabling the Internal Oscillator on the TMS320VC5507/5509/5509A DSP* Application Report (literature number SPRA078).

### 3.11.4 Idling Clock Domain When External Parallel Bus Operating in EHPI Mode

The clock domain cannot be idled when the External Parallel Bus is operating in EHPI mode to ensure host access to the DSP memory. To work around this restriction, use the HIDL bit of the External Bus Selection Register (EBSR) with the CLKGENI bit of the Idle Control Register (ICR) to idle the clock domain.

# 4 Support

## 4.1 Notices Concerning JTAG (IEEE 1149.1) Boundary Scan Test Capability

### *4.1.1 Initialization Requirements for Boundary Scan Test*

The TMS320VC5509A uses the JTAG port for boundary scan tests, emulation capability and factory test purposes. To use boundary scan test, the EMU0 and EMU1/$\overline{\text{OFF}}$ pins must be held LOW through a rising edge of the $\overline{\text{TRST}}$ signal prior to the first scan. This operation selects the appropriate TAP control for boundary scan. If at any time during a boundary scan test a rising edge of $\overline{\text{TRST}}$ occurs when EMU0 or EMU1/$\overline{\text{OFF}}$ are not low, a factory test mode may be selected preventing boundary scan test from being completed. For this reason, it is recommended that EMU0 and EMU1/$\overline{\text{OFF}}$ be pulled or driven low at all times during boundary scan test.

### *4.1.2 Boundary Scan Description Language (BSDL) Model*

BSDL models are available on the web in the TMS320VC5509A product folder under the “simulation models” section.

## 4.2 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the TMS320C5000™ platform of DSPs:

- *TMS320C55x™ DSP Functional Overview* (literature number SPRU312)
- Device-specific data sheets and data manuals
- Complete user’s guides
- Development support tools
- Hardware and software application reports

TMS320C55x reference documentation includes, but is not limited to, the following:

- *TMS320C55x DSP CPU Reference Guide* (literature number SPRU371)
- *TMS320C55x DSP Mnemonic Instruction Set Reference Guide* (literature number SPRU374)
- *TMS320C55x DSP Algebraic Instruction Set Reference Guide* (literature number SPRU375)
- *TMS320C55x DSP Programmer’s Guide* (literature number SPRU376)
- *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317)
- *TMS320C55x Optimizing C/C++ Compiler User’s Guide* (literature number SPRU281)
- *TMS320C55x Assembly Language Tools User’s Guide* (literature number SPRU280)
- *TMS320C55x DSP Library Programmer’s Reference* (literature number SPRU422)
- *TMS320VC5507/5509 DSP Universal Serial Bus (USB) Module Reference Guide* (literature number SPRU596)
- *TMS320C55x Hardware Extensions for Image/Video Applications Programmer’s Reference* (literature number SPRU098)
- *TMS320C55x Image/Video Processing Library Programmer’s Reference* (literature number SPRU037)
- *Using the USB APLL on the TMS320VC5507/5509A* Application Report (literature number SPRA997)
- *Disabling the Internal Oscillator on the TMS320VC5507/5509/5509A DSP* Application Report (literature number SPRA078)
- *Using the TMS320VC5503/VC5507/VC5509/VC5509A Bootloader* Application Report (literature number SPRA375)
- *TMS320VC5509A Power Consumption Summary* Application Report (literature number SPRAA04)
- *TMS320VC5509A Digital Signal Processor Silicon Errata* (literature number SPRZ200)

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The reference guides describe in detail the TMS320C55x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Information regarding TI DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

## 4.3 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320VC5509AGHH). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX** Experimental device that is not necessarily representative of the final device's electrical specifications

**TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

**TMS** Fully qualified production device

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development-support product

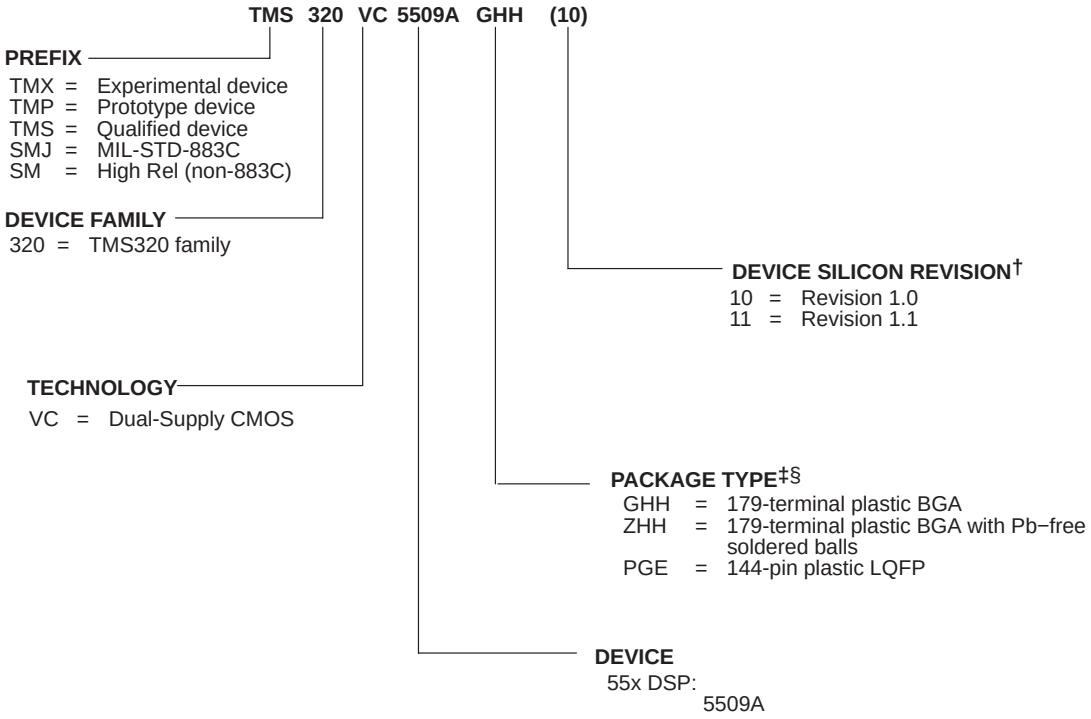
TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

## 4.4 TMS320VC5509A Device Nomenclature




† No silicon revision marked on the package indicates earlier (TMX or TMP) silicon. See the *TMS320VC5509A Digital Signal Processor Silicon Errata* (literature number SPRZ200) to identify TMX or TMP silicon revision.

‡ BGA = Ball Grid Array
LQFP = Low-Profile Quad Flatpack

§ The ZHH package designator represents the version of the GHH with Pb−free soldered balls. The ZHH package devices are supported in the same speed grades as the GHH package devices (*available upon request*).

**Figure 4−1. Device Nomenclature for the TMS320VC5509A**

# 5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320VC5509A DSP.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions unless otherwise specified.

## 5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to $V_{SS}$. Figure 5−1 provides the test load circuit values for a 3.3-V I/O.

Supply voltage I/O range, $DV_{DD}$ . . . . . − 0.3 V to 4.0 V
Supply voltage core range, $CV_{DD}$ . . . . . − 0.3 V to 2.0 V
Input voltage range, $V_I$ . . . . . − 0.3 V to 4.5 V
Output voltage range, $V_O$ . . . . . − 0.3 V to 4.5 V
Operating case temperature range, $T_C$ . . . . . − 40°C to 85°C
Storage temperature range $T_{stg}$ . . . . . − 55°C to 150°C

## 5.2 Recommended Operating Conditions

### 5.2.1 Recommended Operating Conditions for $CV_{DD}$ = 1.2 V (108 MHz)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Core** | | | | | | |
| $CV_{DD}$ | Device supply voltage | | 1.14 | 1.2 | 1.26 | V |
| **Peripherals** | | | | | | |
| $RCV_{DD}$ | RTC module supply voltage, core | | 1.14 | 1.2 | 1.26 | V |
| $RDV_{DD}$ | RTC module supply voltage, I/O (RTCINX1 and RTCINX2) | | 1.14 | 1.2 | 1.26 | V |
| $USBPLLV_{DD}$ | USBPLL supply voltage† | | 1.14 | 1.2 | 1.26 | V |
| $USBV_{DD}$ | USB module supply voltage, I/O (DP, DN, and PU) | | 3 | 3.3 | 3.6 | V |
| $DV_{DD}$ | Device supply voltage, I/O (except DP, DN, PU, SDA, SCL)‡ | | 2.7 | 3.3 | 3.6 | V |
| $ADV_{DD}$ | A/D module digital supply voltage | | 2.7 | 3.3 | 3.6 | V |
| $AV_{DD}$ | A/D module analog supply voltage | | 2.7 | 3.3 | 3.6 | V |
| **Grounds** | | | | | | |
| $V_{SS}$ | Supply voltage, GND, I/O, and core | | | 0 | | V |
| $ADV_{SS}$ | Supply voltage, GND, A/D module, digital | | | 0 | | V |
| $AV_{SS}$ | Supply voltage, GND, A/D module, analog | | | 0 | | V |
| $USBPLLV_{SS}$ | Supply voltage, GND, USBPLL | | | 0 | | V |
| $V_{IH}$ | High-level input voltage, I/O | DN and DP§ | 2.0 | | | V |
| | | SDA & SCL: $V_{DD}$ related input levels‡ | 0.7*$DV_{DD}$ | | $DV_{DD}$(max) +0.5 | |
| | | All other inputs (including hysteresis inputs) | 2.0 | | $DV_{DD}$ + 0.3 | |
| $V_{IL}$ | Low-level input voltage, I/O | DN and DP§ | | | 0.8 | V |
| | | SDA &SCL: $V_{DD}$ related input levels‡ | −0.5 | | 0.3 * $DV_{DD}$ | |
| | | All other inputs (including hysteresis inputs) | −0.3 | | 0.8 | |
| $V_{hys}$ | Hysteresis level | Inputs with hysteresis only | | 0.1*$DV_{DD}$ | | V |
| $I_{OH}$ | High-level output current | DN and DP§ ($V_{OH}$ = 2.45 V) | | | −17.0 | mA |
| | | All other outputs | | | −4 | |
| $I_{OL}$ | Low-level output current | DN and DP§ ($V_{OL}$ = 0.36 V) | 17.0 | | | mA |
| | | SDA and SCL‡ | | | 3 | |
| | | All other outputs | | | 4 | |
| $T_C$ | Operating case temperature | | −40 | | 85 | °C |

† USB PLL is susceptible to power supply ripple. The maximum allowable supply ripple is 1% for 1 Hz to 5 kHz; 1.5% for 5 kHz to 10 MHz; 3% for 10 MHz to 100 MHz, and less than 5% for 100 MHz or greater.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Due to the fact that different voltage devices can be connected to the $I^2C$ bus, the level of logic 0 (low) and logic 1 (high) are not fixed and depends on the associated $V_{DD}$.

§ USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

### 5.2.2 Recommended Operating Conditions for $CV_{DD}$ = 1.35 V (144 MHz)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Core** | | | | | | |
| $CV_{DD}$ | Device supply voltage | | 1.28 | 1.35 | 1.42 | V |
| **Peripherals** | | | | | | |
| $RCV_{DD}$ | RTC module supply voltage, core | | 1.28 | 1.35 | 1.42 | V |
| $RDV_{DD}$ | RTC module supply voltage, I/O (RTCINX1 and RTCINX2) | | 1.28 | 1.35 | 1.42 | V |
| $USBPLLV_{DD}$ | USBPLL supply voltage† | | 1.28 | 1.35 | 1.42 | V |
| $USBV_{DD}$ | USB module supply voltage, I/O (DP, DN, and PU) | | 3 | 3.3 | 3.6 | V |
| $DV_{DD}$ | Device supply voltage, I/O (except DP, DN, PU, SDA, SCL)‡ | | 2.7 | 3.3 | 3.6 | V |
| $ADV_{DD}$ | A/D module digital supply voltage | | 2.7 | 3.3 | 3.6 | V |
| $AV_{DD}$ | A/D module analog supply voltage | | 2.7 | 3.3 | 3.6 | V |
| **Grounds** | | | | | | |
| $V_{SS}$ | Supply voltage, GND, I/O, and core | | | 0 | | V |
| $ADV_{SS}$ | Supply voltage, GND, A/D module, digital | | | 0 | | V |
| $AV_{SS}$ | Supply voltage, GND, A/D module, analog | | | 0 | | V |
| $USBPLLV_{SS}$ | Supply voltage, GND, USBPLL | | | 0 | | V |
| $V_{IH}$ | High-level input voltage, I/O | DN and DP§ | 2.0 | | | V |
| | | SDA & SCL: $V_{DD}$ related input levels‡ | 0.7*$DV_{DD}$ | | $DV_{DD}$(max) +0.5 | |
| | | All other inputs (including hysteresis inputs) | 2.0 | | $DV_{DD}$ + 0.3 | |
| $V_{IL}$ | Low-level input voltage, I/O | DN and DP§ | | | 0.8 | V |
| | | SDA &SCL: $V_{DD}$ related input levels‡ | −0.5 | | 0.3 * $DV_{DD}$ | |
| | | All other inputs (including hysteresis inputs) | −0.3 | | 0.8 | |
| $V_{hys}$ | Hysteresis level | Inputs with hysteresis only | | 0.1*$DV_{DD}$ | | V |
| $I_{OH}$ | High-level output current | DN and DP§ ($V_{OH}$ = 2.45 V) | | | −17.0 | mA |
| | | All other outputs | | | −4 | |
| $I_{OL}$ | Low-level output current | DN and DP§ ($V_{OL}$ = 0.36 V) | 17.0 | | | mA |
| | | SDA and SCL‡ | | | 3 | |
| | | All other outputs | | | 4 | |
| $T_C$ | Operating case temperature | | −40 | | 85 | °C |

† USB PLL is susceptible to power supply ripple. The maximum allowable supply ripple is 1% for 1 Hz to 5 kHz; 1.5% for 5 kHz to 10 MHz; 3% for 10 MHz to 100 MHz, and less than 5% for 100 MHz or greater.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Due to the fact that different voltage devices can be connected to the $I^2C$ bus, the level of logic 0 (low) and logic 1 (high) are not fixed and depends on the associated $V_{DD}$.

§ USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

### 5.2.3 Recommended Operating Conditions for $CV_{DD}$ = 1.6 V (200 MHz)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Core** | | | | | | |
| $CV_{DD}$ | Device supply voltage | | 1.55 | 1.6 | 1.65 | V |
| **Peripherals** | | | | | | |
| $RCV_{DD}$ | RTC module supply voltage, core | | 1.55 | 1.6 | 1.65 | V |
| $RDV_{DD}$ | RTC module supply voltage, I/O (RTCINX1 and RTCINX2) | | 1.55 | 1.6 | 1.65 | V |
| $USBPLLV_{DD}$ | USBPLL supply voltage† | | 1.55 | 1.6 | 1.65 | V |
| $USBV_{DD}$ | USB module supply voltage, I/O (DP, DN, and PU) | | 3 | 3.3 | 3.6 | V |
| $DV_{DD}$ | Device supply voltage, I/O (except DP, DN, PU, SDA, SCL)‡ | | 2.7 | 3.3 | 3.6 | V |
| $ADV_{DD}$ | A/D module digital supply voltage | | 2.7 | 3.3 | 3.6 | V |
| $AV_{DD}$ | A/D module analog supply voltage | | 2.7 | 3.3 | 3.6 | V |
| **Grounds** | | | | | | |
| $V_{SS}$ | Supply voltage, GND, I/O, and core | | | 0 | | V |
| $ADV_{SS}$ | Supply voltage, GND, A/D module, digital | | | 0 | | V |
| $AV_{SS}$ | Supply voltage, GND, A/D module, analog | | | 0 | | V |
| $USBPLLV_{SS}$ | Supply voltage, GND, USBPLL | | | 0 | | V |
| $V_{IH}$ | High-level input voltage, I/O | DN and DP§ | 2.0 | | | V |
| | | SDA & SCL: $V_{DD}$ related input levels‡ | 0.7*$DV_{DD}$ | | $DV_{DD}$(max) +0.5 | |
| | | All other inputs (including hysteresis inputs) | 2.0 | | $DV_{DD}$ + 0.3 | |
| $V_{IL}$ | Low-level input voltage, I/O | DN and DP§ | | | 0.8 | V |
| | | SDA & SCL: $V_{DD}$ related input levels‡ | −0.5 | | 0.3 * $DV_{DD}$ | |
| | | All other inputs (including hysteresis inputs) | −0.3 | | 0.8 | |
| $V_{hys}$ | Hysteresis level | Inputs with hysteresis only | | 0.1*$DV_{DD}$ | | V |
| $I_{OH}$ | High-level output current | DN and DP§ ($V_{OH}$ = 2.45 V) | | | −17.0 | mA |
| | | All other outputs | | | −4 | |
| $I_{OL}$ | Low-level output current | DN and DP§ ($V_{OL}$ = 0.36 V) | 17.0 | | | mA |
| | | SDA and SCL‡ | | | 3 | |
| | | All other outputs | | | 4 | |
| $T_C$ | Operating case temperature | | −40 | | 85 | °C |

† USB PLL is susceptible to power supply ripple. The maximum allowable supply ripple is 1% for 1 Hz to 5 kHz; 1.5% for 5 kHz to 10 MHz; 3% for 10 MHz to 100 MHz, and less than 5% for 100 MHz or greater.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Due to the fact that different voltage devices can be connected to the $I^2C$ bus, the level of logic 0 (low) and logic 1 (high) are not fixed and depends on the associated $V_{DD}$.

§ USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

## 5.3 Electrical Characteristics

### 5.3.1 Electrical Characteristics Over Recommended Operating Case Temperature Range for $CV_{DD}$ = 1.2 V (108 MHz) (Unless Otherwise Noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DN and DP† | $USBV_{DD}$ = 3.0 V–3.6 V, $I_{OH}$ = −300 µA | 2.8 | | $USBV_{DD}$ | V |
| | | PU | $USBV_{DD}$ = 3.0 V–3.6 V, $I_{OH}$ = −300 µA | 0.9 * $USBV_{DD}$ | | $USBV_{DD}$ | |
| | | All other outputs | $DV_{DD}$ = 2.7 V–3.6 V, $I_{OH}$ = MAX | 0.75 * $DV_{DD}$ | | | |
| $V_{OL}$ | Low-level output voltage | SDA & SCL‡ | At 3 mA sink current | 0 | | 0.4 | V |
| | | DN and DP† | $I_{OL}$ = 3.0 mA | | | 0.3 | |
| | | All other outputs | $I_{OL}$ = MAX | | | 0.4 | |
| $I_{IZ}$ | Input current for outputs in high-impedance | Output-only or I/O pins with bus keepers (enabled) | $DV_{DD}$ = MAX, $V_O$ = $V_{SS}$ to $DV_{DD}$ | −300 | | 300 | µA |
| | | All other output-only or I/O pins | $DV_{DD}$ = MAX $V_O$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_I$ | Input current | Input pins with internal pulldown (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | 30 | | 300 | µA |
| | | Input pins with internal pullup (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −300 | | −30 | |
| | | X2/CLKIN | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −50 | | 50 | |
| | | All other input-only pins | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_{DDC}$ | $CV_{DD}$ Supply current, CPU + internal memory access§ | | $CV_{DD}$ = 1.2 V CPU clock = 108 MHz $T_C$ = 25°C | | 0.45 | | mA/ MHz |
| $I_{DDP}$ | $DV_{DD}$ supply current, pins active¶ | | $DV_{DD}$ = 3.3 V CPU clock = 108 MHz $T_C$ = 25°C | | 5.5 | | mA |
| $I_{DDC}$ | $CV_{DD}$ supply current, standby# | Oscillator disabled. All domains in low-power state | $CV_{DD}$ = 1.2 V $T_C$ = 25°C | | 100 | | µA |
| $I_{DDP}$ | $DV_{DD}$ supply current, standby | Oscillator disabled. All domains in low-power state. | $DV_{DD}$ = 3.3 V No I/O activity $T_C$ = 25°C | | 10 | | µA |
| $C_i$ | Input capacitance | | | | 3 | | pF |
| $C_o$ | Output capacitance | | | | 3 | | pF |

† USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

§ CPU executing 75% Dual MAC + 25% ADD with moderate data bus activity (table of sine values). CPU and CLKGEN (DPLL) domain are active. All other domains are idled. See the *TMS320VC5509A Power Consumption Summary* Application Report (literature number SPRAA04).

¶ One word of a table of a 16-bit sine value is written to the EMIF every 250 ns (64 Mbps). Each EMIF output pin is connected to a 10-pF load.

# In CLKGEN domain idle mode, X2/CLKIN becomes output and is driven low to stop external crystals (if used) from oscillating. Standby current will be higher if an external clock source tries to drive the X2/CLKIN pin during this time.

### 5.3.2 Electrical Characteristics Over Recommended Operating Case Temperature Range for $CV_{DD}$ = 1.35 V (144 MHz) (Unless Otherwise Noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DN and DP† | $USBV_{DD}$ = 3.0 V−3.6 V, $I_{OH}$ = −300 µA | 2.8 | | $USBV_{DD}$ | V |
| | | PU | $USBV_{DD}$ = 3.0 V−3.6 V, $I_{OH}$ = −300 µA | 0.9 * $USBV_{DD}$ | | $USBV_{DD}$ | |
| | | All other outputs | $DV_{DD}$ = 2.7 V−3.6 V, $I_{OH}$ = MAX | 0.75 * $DV_{DD}$ | | | |
| $V_{OL}$ | Low-level output voltage | SDA & SCL‡ | At 3 mA sink current | 0 | | 0.4 | V |
| | | DN and DP† | $I_{OL}$ = 3.0 mA | | | 0.3 | |
| | | All other outputs | $I_{OL}$ = MAX | | | 0.4 | |
| $I_{IZ}$ | Input current for outputs in high-impedance | Output-only or I/O pins with bus keepers (enabled) | $DV_{DD}$ = MAX, $V_O$ = $V_{SS}$ to $DV_{DD}$ | −300 | | 300 | µA |
| | | All other output-only or I/O pins | $DV_{DD}$ = MAX $V_O$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_I$ | Input current | Input pins with internal pulldown (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | 30 | | 300 | µA |
| | | Input pins with internal pullup (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −300 | | −30 | |
| | | X2/CLKIN | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −50 | | 50 | |
| | | All other input-only pins | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_{DDC}$ | $CV_{DD}$ Supply current, CPU + internal memory access§ | | $CV_{DD}$ = 1.35 V CPU clock = 144 MHz $T_C$ = 25°C | | 0.51 | | mA/ MHz |
| $I_{DDP}$ | $DV_{DD}$ supply current, pins active¶ | | $DV_{DD}$ = 3.3 V CPU clock = 144 MHz $T_C$ = 25°C | | 5.5 | | mA |
| $I_{DDC}$ | $CV_{DD}$ supply current, standby# | Oscillator disabled. All domains in low-power state | $CV_{DD}$ = 1.35 V $T_C$ = 25°C | | 125 | | µA |
| $I_{DDP}$ | $DV_{DD}$ supply current, standby | Oscillator disabled. All domains in low-power state. | $DV_{DD}$ = 3.3 V No I/O activity $T_C$ = 25°C | | 10 | | µA |
| $C_i$ | Input capacitance | | | | 3 | | pF |
| $C_o$ | Output capacitance | | | | 3 | | pF |

† USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

§ CPU executing 75% Dual MAC + 25% ADD with moderate data bus activity (table of sine values). CPU and CLKGEN (DPLL) domain are active. All other domains are idled. See the *TMS320VC5509A Power Consumption Summary* Application Report (literature number SPRAA04).

¶ One word of a table of a 16-bit sine value is written to the EMIF every 250 ns (64 Mbps). Each EMIF output pin is connected to a 10-pF load.

# In CLKGEN domain idle mode, X2/CLKIN becomes output and is driven low to stop external crystals (if used) from oscillating. Standby current will be higher if an external clock source tries to drive the X2/CLKIN pin during this time.

### 5.3.3 Electrical Characteristics Over Recommended Operating Case Temperature Range for $CV_{DD}$ = 1.6 V (200 MHz) (Unless Otherwise Noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | DN and DP† | $USBV_{DD}$ = 3.0 V–3.6 V, $I_{OH}$ = −300 µA | 2.8 | | $USBV_{DD}$ | V |
| | | PU | $USBV_{DD}$ = 3.0 V–3.6 V, $I_{OH}$ = −300 µA | 0.9 * $USBV_{DD}$ | | $USBV_{DD}$ | |
| | | All other outputs | $DV_{DD}$ = 2.7 V–3.6 V, $I_{OH}$ = MAX | 0.75 * $DV_{DD}$ | | | |
| $V_{OL}$ | Low-level output voltage | SDA & SCL‡ | At 3 mA sink current | 0 | | 0.4 | V |
| | | DN and DP† | $I_{OL}$ = 3.0 mA | | | 0.3 | |
| | | All other outputs | $I_{OL}$ = MAX | | | 0.4 | |
| $I_{IZ}$ | Input current for outputs in high-impedance | Output-only or I/O pins with bus keepers (enabled) | $DV_{DD}$ = MAX, $V_O$ = $V_{SS}$ to $DV_{DD}$ | −300 | | 300 | µA |
| | | All other output-only or I/O pins | $DV_{DD}$ = MAX $V_O$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_I$ | Input current | Input pins with internal pulldown (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | 30 | | 300 | µA |
| | | Input pins with internal pullup (enabled) | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −300 | | −30 | |
| | | X2/CLKIN | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −50 | | 50 | |
| | | All other input-only pins | $DV_{DD}$ = MAX, $V_I$ = $V_{SS}$ to $DV_{DD}$ | −5 | | 5 | |
| $I_{DDC}$ | $CV_{DD}$ Supply current, CPU + internal memory access§ | | $CV_{DD}$ = 1.6 V CPU clock = 200 MHz $T_C$ = 25°C | | 0.60 | | mA/ MHz |
| $I_{DDP}$ | $DV_{DD}$ supply current, pins active¶ | | $DV_{DD}$ = 3.3 V CPU clock = 200 MHz $T_C$ = 25°C | | 5.5 | | mA |
| $I_{DDC}$ | $CV_{DD}$ supply current, standby# | Oscillator disabled. All domains in low-power state | $CV_{DD}$ = 1.6 V $T_C$ = 25°C | | 150 | | µA |
| $I_{DDP}$ | $DV_{DD}$ supply current, standby | Oscillator disabled. All domains in low-power state. | $DV_{DD}$ = 3.3 V No I/O activity $T_C$ = 25°C | | 10 | | µA |
| $C_i$ | Input capacitance | | | | 3 | | pF |
| $C_o$ | Output capacitance | | | | 3 | | pF |

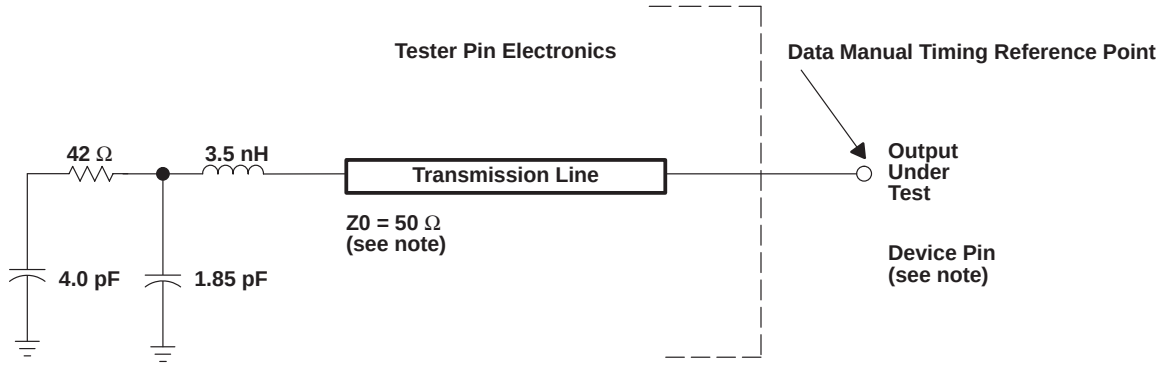
† USB I/O pins DP and DN can tolerate a short circuit at D+ and D− to 0 V or 5 V, as long as the recommended series resistors (see Figure 5−42) are connected between the D+ and DP (package), and the D− and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

‡ The $I^2C$ pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

§ CPU executing 75% Dual MAC + 25% ADD with moderate data bus activity (table of sine values). CPU and CLKGEN (DPLL) domain are active. All other domains are idled. See the *TMS320VC5509A Power Consumption Summary* Application Report (literature number SPRAA04).

¶ One word of a table of a 16-bit sine value is written to the EMIF every 250 ns (64 Mbps). Each EMIF output pin is connected to a 10-pF load.

# In CLKGEN domain idle mode, X2/CLKIN becomes output and is driven low to stop external crystals (if used) from oscillating. Standby current will be higher if an external clock source tries to drive the X2/CLKIN pin during this time.




NOTE: The data manual provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data manual timings.

Input requirements in this data manual are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

**Figure 5−1. 3.3-V Test Load Circuit**

## 5.4 ESD Performance

ESD stress levels were performed in compliance with the following JEDEC standards with the results indicated below:

- Charged Device Model (CDM), based on JEDEC Specification JESD22-C101, passed at ±500 V
- Human Body Model (HBM), based on JEDEC Specification JESD22-A114, passed at ±1500 V

**NOTE:**

According to industry research publications, ESD-CDM testing results show better correlation to manufacturing line and field failure rates than ESD-HBM testing. 500-V CDM is commonly considered as a safe passing level.

## 5.5 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

| | |
|---|---|
| a | access time |
| c | cycle time (period) |
| d | delay time |
| dis | disable time |
| en | enable time |
| f | fall time |
| h | hold time |
| r | rise time |
| su | setup time |
| t | transition time |
| v | valid time |
| w | pulse duration (width) |
| X | Unknown, changing, or don't care level |

Letters and symbols and their meanings:

| | |
|---|---|
| H | High |
| L | Low |
| V | Valid |
| Z | High-impedance |

## 5.6 Clock Options

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of two or four or multiplied by one of several values to generate the internal machine cycle.

### *5.6.1 Internal System Oscillator With External Crystal*

The internal oscillator is always enabled following a device reset. The oscillator requires an external crystal connected across the X1 and X2/CLKIN pins. If the internal oscillator is not used, an external clock source must be applied to the X2/CLKIN pin and the X1 pin should be left unconnected. Since the internal oscillator can be used as a clock source to the PLLs, the crystal oscillation frequency can be multiplied to generate the CPU clock and USB clock, if desired.

The crystal should be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5−1. The connection of the required circuit is shown in Figure 5−2. Under some conditions, all the components shown are not required. The capacitors, $C_1$ and $C_2$, should be chosen such that the equation below is satisfied. $C_L$ in the equation is the load specified for the crystal that is also specified in Table 5−1.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

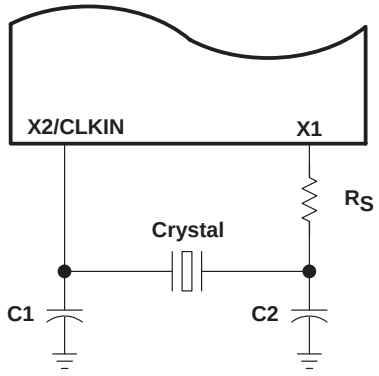



**Figure 5−2. Internal System Oscillator With External Crystal**

**Table 5−1. Recommended Crystal Parameters**

| FREQUENCY RANGE (MHz) | MAX ESR (Ω) | TYP $C_{LOAD}$ (pF) | MAX $C_{SHUNT}$ (pF) | $R_S$ (Ω) |
|---|---|---|---|---|
| 20−15 | 20 | 10 | 7 | 0 |
| 15−12 | 30 | 16 | 7 | 0 |
| 12−10 | 40 | 16 | 7 | 100 |
| 10−8 | 60 | 18 | 7 | 470 |
| 8−6 | 80 | 18 | 7 | 1.5k |
| 6−5 | 80 | 18 | 7 | 2.2k |

Although the recommended ESR presented in Table 5−1 is maximum, theoretically a crystal with a lower maximum ESR might seem to meet the requirement. It is recommended that crystals which meet the maximum ESR specification in Table 5−1 are used.

### 5.6.2 Layout Considerations

Since parasitic capacitance, inductance and resistance can be significant in any circuit, good PC board layout practices should always be observed when planning trace routing to the discrete components used in the oscillator circuit. Specifically, the crystal and the associated discrete components should be located as close to the DSP as physically possible. Also, X1 and X2/CLKIN traces should be separated as soon as possible after routing away from the DSP to minimize parasitic capacitance between them, and a ground trace should be run between these two signal lines. This also helps to minimize stray capacitance between these two signals.

### 5.6.3 Clock Generation in Bypass Mode (DPLL Disabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be divided by a factor of one, two, or four to generate the internal CPU clock cycle. The divide factor (D) is set in the BYPASS_DIV field of the clock mode register. The contents of this field only affect clock generation while the device is in bypass mode. In this mode, the digital phase-locked loop (DPLL) clock synthesis is disabled.

Table 5−2 and Table 5−3 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−3).

**Table 5−2. CLKIN Timing Requirements**

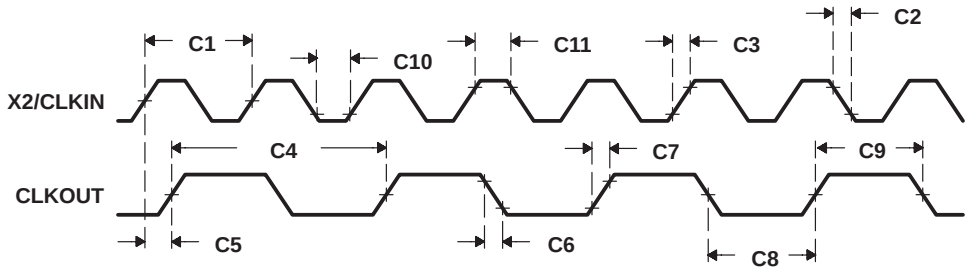
| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V<br>$CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| C1 | $t_{c(CI)}$ | Cycle time, X2/CLKIN | 20 | 400† | ns |
| C2 | $t_{f(CI)}$ | Fall time, X2/CLKIN | | 4 | ns |
| C3 | $t_{r(CI)}$ | Rise time, X2/CLKIN | | 4 | ns |
| C10 | $t_{w(CIL)}$ | Pulse duration, CLKIN low | 6 | | ns |
| C11 | $t_{w(CIH)}$ | Pulse duration, CLKIN high | 6 | | ns |

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. If an external crystal is used, the X2/CLKIN cycle time is limited by the crystal frequency range listed in Table 5−1.

**Table 5−3. CLKOUT Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V<br>$CV_{DD}$ = 1.6 V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| C4 | $t_{c(CO)}$ | Cycle time, CLKOUT | 20‡ | D*$t_{c(CI)}$§ | 1600† | ns |
| C5 | $t_{d(CI-CO)}$ | Delay time, X2/CLKIN high to CLKOUT high/low | 5 | 15 | 25 | ns |
| C6 | $t_{f(CO)}$ | Fall time, CLKOUT | | 1 | | ns |
| C7 | $t_{r(CO)}$ | Rise time, CLKOUT | | 1 | | ns |
| C8 | $t_{w(COL)}$ | Pulse duration, CLKOUT low | H − 1 | | H + 1 | ns |
| C9 | $t_{w(COH)}$ | Pulse duration, CLKOUT high | H − 1 | | H + 1 | ns |

† This device utilizes a fully static design and therefore can operate with $t_{c(CO)}$ approaching ∞. If an external crystal is used, the X2/CLKIN cycle time is limited by the crystal frequency range listed in Table 5−1.
‡ It is recommended that the DPLL synthesised clocking option be used to obtain maximum operating frequency.
§ D = 1/(PLL Bypass Divider)




NOTE A: The relationship of X2/CLKIN to CLKOUT depends on the PLL bypass divide factor chosen for the CLKMD register. The waveform relationship shown in Figure 5−3 is intended to illustrate the timing parameters based on CLKOUT = 1/2(CLKIN) configuration.

**Figure 5−3. Bypass Mode Clock Timings**

### 5.6.4 Clock Generation in Lock Mode (DPLL Synthesis Enabled)

The frequency of the reference clock provided at the X2/CLKIN pin can be multiplied by a synthesis factor of N to generate the internal CPU clock cycle. The synthesis factor is determined by:

$$N = \frac{M}{D_L}$$

where: M = the multiply factor set in the PLL_MULT field of the clock mode register
$D_L$ = the divide factor set in the PLL_DIV field of the clock mode register

Valid values for M are (multiply by) 2 to 31. Valid values for $D_L$ are (divide by) 1, 2, 3, and 4.

For detailed information on clock generation configuration, see the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317).

Table 5−4 and Table 5−5 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−4).

**Table 5−4. Multiply-By-N Clock Option Timing Requirements**

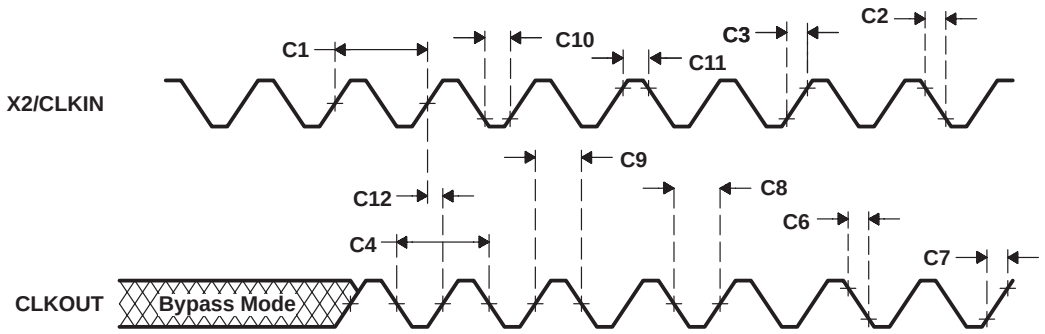
| NO. | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V<br>$CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| C1 | $t_{c(CI)}$ | Cycle time, X2/CLKIN | DPLL synthesis enabled | 20† | 400 | ns |
| C2 | $t_{f(CI)}$ | Fall time, X2/CLKIN | | | 4 | ns |
| C3 | $t_{r(CI)}$ | Rise time, X2/CLKIN | | | 4 | ns |
| C10 | $t_{w(CIL)}$ | Pulse duration, CLKIN low | | 6 | | ns |
| C11 | $t_{w(CIH)}$ | Pulse duration, CLKIN high | | 6 | | ns |

† The clock frequency synthesis factor and minimum X2/CLKIN cycle time should be chosen such that the resulting CLKOUT cycle time is within the specified range ($t_{c(CO)}$). If an external crystal is used, the X2/CLKIN cycle time is limited by the crystal frequency range listed in Table 5−1.

**Table 5−5. Multiply-By-N Clock Option Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V | | | $CV_{DD}$ = 1.35 V | | | $CV_{DD}$ = 1.6 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| C4 | $t_{c(CO)}$ | Cycle time, CLKOUT | 9.26 | $t_{c(CI)}$*N‡ | 1600 | 6.95 | $t_{c(CI)}$*N‡ | 1600 | 5 | $t_{c(CI)}$*N‡ | 1600 | ns |
| C6 | $t_{f(CO)}$ | Fall time, CLKOUT | | 1 | | | 1 | | | 1 | | ns |
| C7 | $t_{r(CO)}$ | Rise time, CLKOUT | | 1 | | | 1 | | | 1 | | ns |
| C8 | $t_{w(COL)}$ | Pulse duration, CLKOUT low | H − 1 | | H + 1 | H − 1 | | H + 1 | H − 1 | | H + 1 | ns |
| C9 | $t_{w(COH)}$ | Pulse duration, CLKOUT high | H − 1 | | H + 1 | H − 1 | | H + 1 | H − 1 | | H + 1 | ns |
| C12 | $t_{d(CI–CO)}$ | Delay time, X2/CLKIN high/low to CLKOUT high/low | 5 | 15 | 25 | 5 | 15 | 25 | 5 | 15 | 25 | ns |

‡ N = Clock frequency synthesis factor




NOTE A: The relationship of X2/CLKIN to CLKOUT depends on the PLL multiply and divide factor chosen for the CLKMD register. The waveform relationship shown in Figure 5−3 is intended to illustrate the timing parameters based on CLKOUT = 1xCLKIN configuration.

**Figure 5−4. External Multiply-by-N Clock Timings**

### 5.6.5 Real-Time Clock Oscillator With External Crystal

The real-time clock module includes an oscillator circuit. The oscillator requires an external 32.768-kHz crystal connected across the RTCINX1 and RTCINX2 pins. The connection of the required circuit, consisting of the crystal and two load capacitors, is shown in Figure 5−5. The load capacitors, $C_1$ and $C_2$, should be chosen such that the equation below is satisfied. $C_L$ in the equation is the load specified for the crystal.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

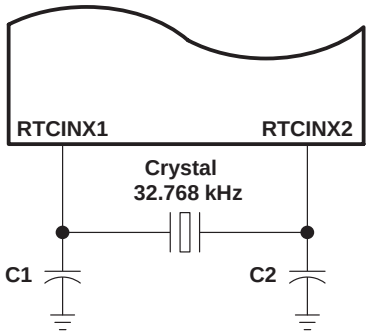



**Figure 5−5. Real-Time Clock Oscillator With External Crystal**

**NOTE:** The RTC can be idled by not supplying its 32-kHz oscillator signal. In order to keep RTC power dissipation to a minimum when the RTC module is not used, it is recommended that the RTC module be powered up, the RTC input pin (RTCINX1) be pulled low, and the RTC output pin (RTCINX2) be left floating.

**Table 5−6. Recommended RTC Crystal Parameters**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_O$ | Frequency of oscillation† | | 32.768 | | kHz |
| ESR | Series resistance† | 30 | | 60 | kΩ |
| $C_L$ | Load capacitance | | 12.5 | | pF |
| DL | Crystal drive level | | | 1 | µW |

† ESR must be 200 kΩ or greater at frequencies other than 32.768kHz. Otherwise, oscillations at overtone frequencies may occur.

## 5.7 Memory Interface Timings

### 5.7.1 Asynchronous Memory Timings

Table 5−7 and Table 5−8 assume testing over recommended operating conditions (see Figure 5−6 and Figure 5−7).

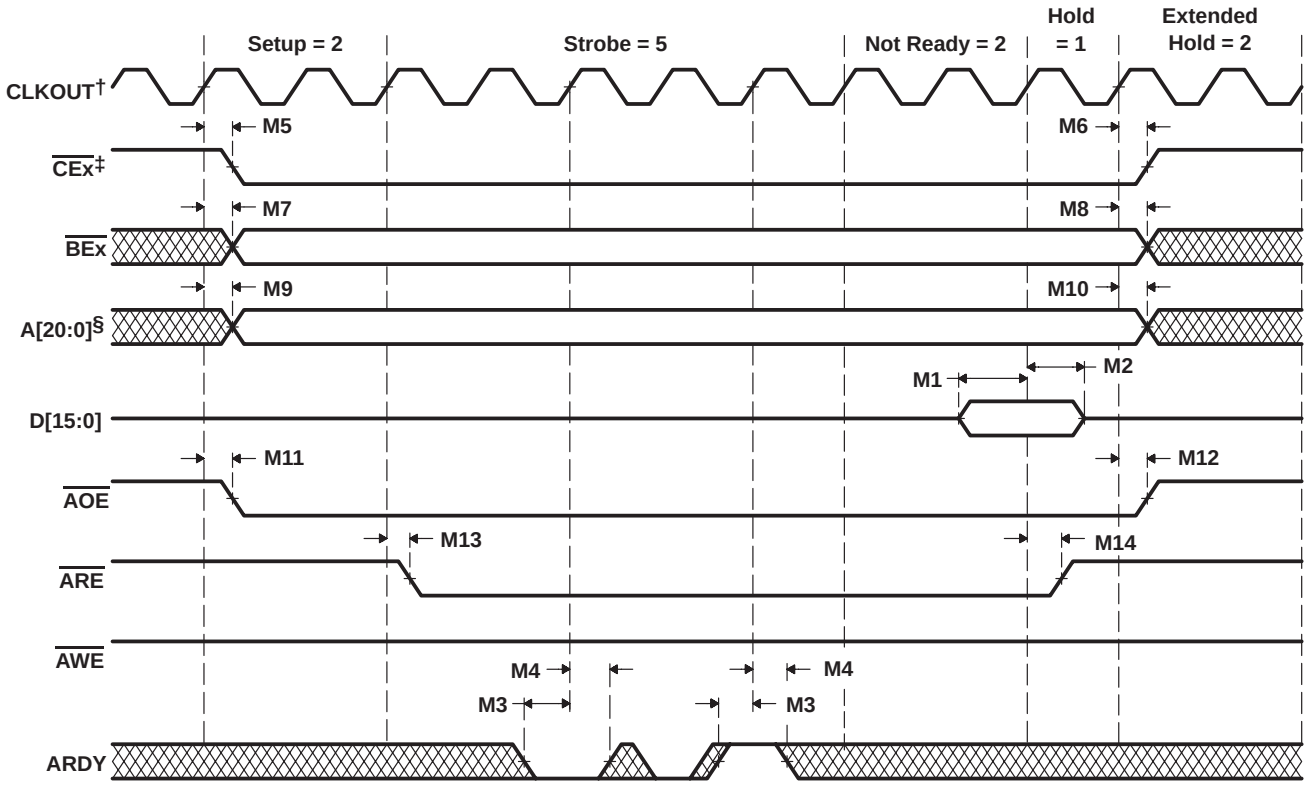
**Table 5−7. Asynchronous Memory Cycle Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| M1 | $t_{su(DV-COH)}$ | Setup time, read data valid before CLKOUT high† | 6 | | 5 | | ns |
| M2 | $t_{h(COH-DV)}$ | Hold time, read data valid after CLKOUT high | 0 | | 0 | | ns |
| M3 | $t_{su(ARDY-COH)}$ | Setup time, ARDY valid before CLKOUT high† | 10 | | 7 | | ns |
| M4 | $t_{h(COH-ARDY)}$ | Hold time, ARDY valid after CLKOUT high | 0 | | 0 | | ns |

† To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

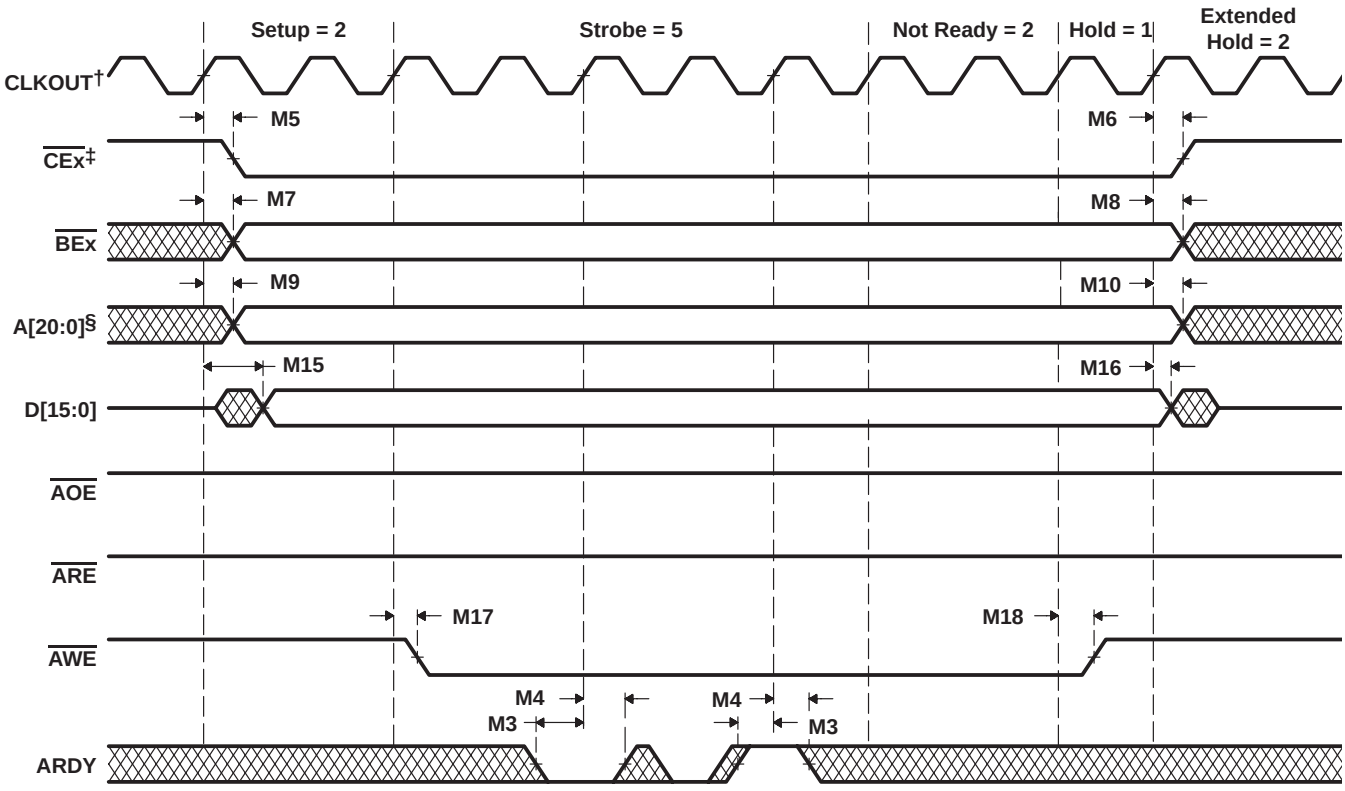
**Table 5−8. Asynchronous Memory Cycle Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| M5 | $t_{d(COH-CEV)}$ | Delay time, CLKOUT high to $\overline{CEx}$ valid | −2 | 4 | −2 | 4 | ns |
| M6 | $t_{d(COH-CEIV)}$ | Delay time, CLKOUT high to $\overline{CEx}$ invalid | −2 | 4 | −2 | 4 | ns |
| M7 | $t_{d(COH-BEV)}$ | Delay time, CLKOUT high to $\overline{BEx}$ valid | | 4 | | 4 | ns |
| M8 | $t_{d(COH-BEIV)}$ | Delay time, CLKOUT high to $\overline{BEx}$ invalid | −2 | | −2 | | ns |
| M9 | $t_{d(COH-AV)}$ | Delay time, CLKOUT high to address valid | | 4 | | 4 | ns |
| M10 | $t_{d(COH-AIV)}$ | Delay time, CLKOUT high to address invalid | −2 | | −2 | | ns |
| M11 | $t_{d(COH-AOEV)}$ | Delay time, CLKOUT high to $\overline{AOE}$ valid | −2 | 4 | −2 | 4 | ns |
| M12 | $t_{d(COH-AOEIV)}$ | Delay time, CLKOUT high to $\overline{AOE}$ invalid | −2 | 4 | −2 | 4 | ns |
| M13 | $t_{d(COH-AREV)}$ | Delay time, CLKOUT high to $\overline{ARE}$ valid | −2 | 4 | −2 | 4 | ns |
| M14 | $t_{d(COH-AREIV)}$ | Delay time, CLKOUT high to $\overline{ARE}$ invalid | −2 | 4 | −2 | 4 | ns |
| M15 | $t_{d(COH-DV)}$ | Delay time, CLKOUT high to data valid | | 4 | | 4 | ns |
| M16 | $t_{d(COH-DIV)}$ | Delay time, CLKOUT high to data invalid | −2 | | −2 | | ns |
| M17 | $t_{d(COH-AWEV)}$ | Delay time, CLKOUT high to $\overline{AWE}$ valid | −2 | 4 | −2 | 4 | ns |
| M18 | $t_{d(COH-AWEIV)}$ | Delay time, CLKOUT high to $\overline{AWE}$ invalid | −2 | 4 | −2 | 4 | ns |




† CLKOUT is equal to CPU clock
‡ $\overline{\text{CEx}}$ becomes active depending on the memory address space being accessed
§ A[13:0] for LQFP

**Figure 5−6. Asynchronous Memory Read Timings**




† CLKOUT is equal to CPU clock
‡ CEx becomes active depending on the memory address space being accessed
§ A[13:0] for LQFP

**Figure 5−7. Asynchronous Memory Write Timings**

## 5.7.2 Synchronous DRAM (SDRAM) Timings

Table 5−9 and Table 5−10 assume testing over recommended operating conditions (see Figure 5−8 through Figure 5−14).

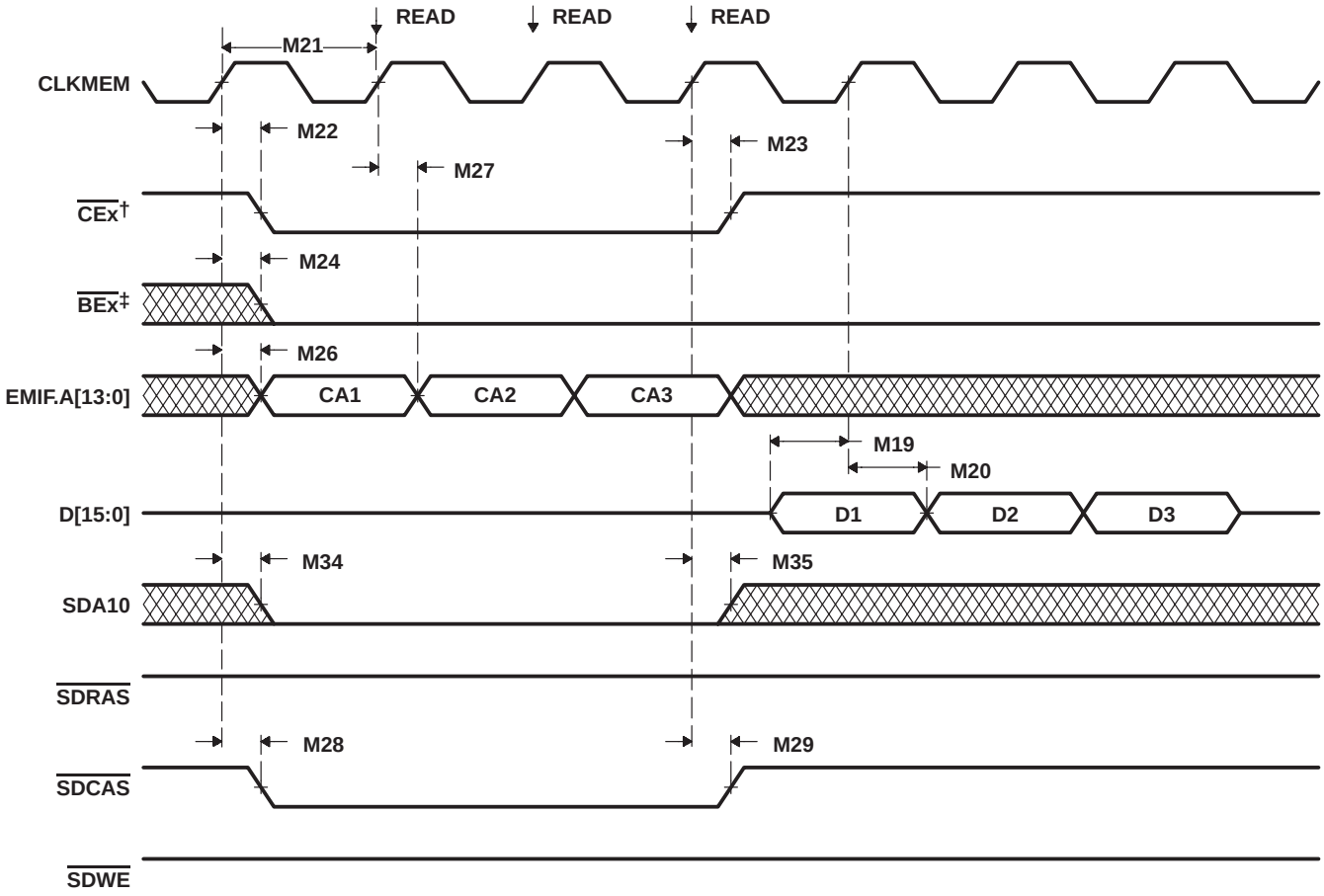
**Table 5−9. Synchronous DRAM Cycle Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| M19 | $t_{su(DV-CLKMEMH)}$ | Setup time, read data valid before CLKMEM high | 3 | | 3 | | ns |
| M20 | $t_{h(CLKMEMH-DV)}$ | Hold time, read data valid after CLKMEM high | 2 | | 2 | | ns |
| M21 | $t_{c(CLKMEM)}$ | Cycle time, CLKMEM | 9.26† | | 7.52‡ | | ns |

† Maximum SDRAM operating frequency = 108 MHz. Actual attainable maximum operating frequency will depend on the quality of the PC board design and the memory chip timing requirement.
‡ Maximum SDRAM operating frequency = 133 MHz. Actual attainable maximum operating frequency will depend on the quality of the PC board design and the memory chip timing requirement.

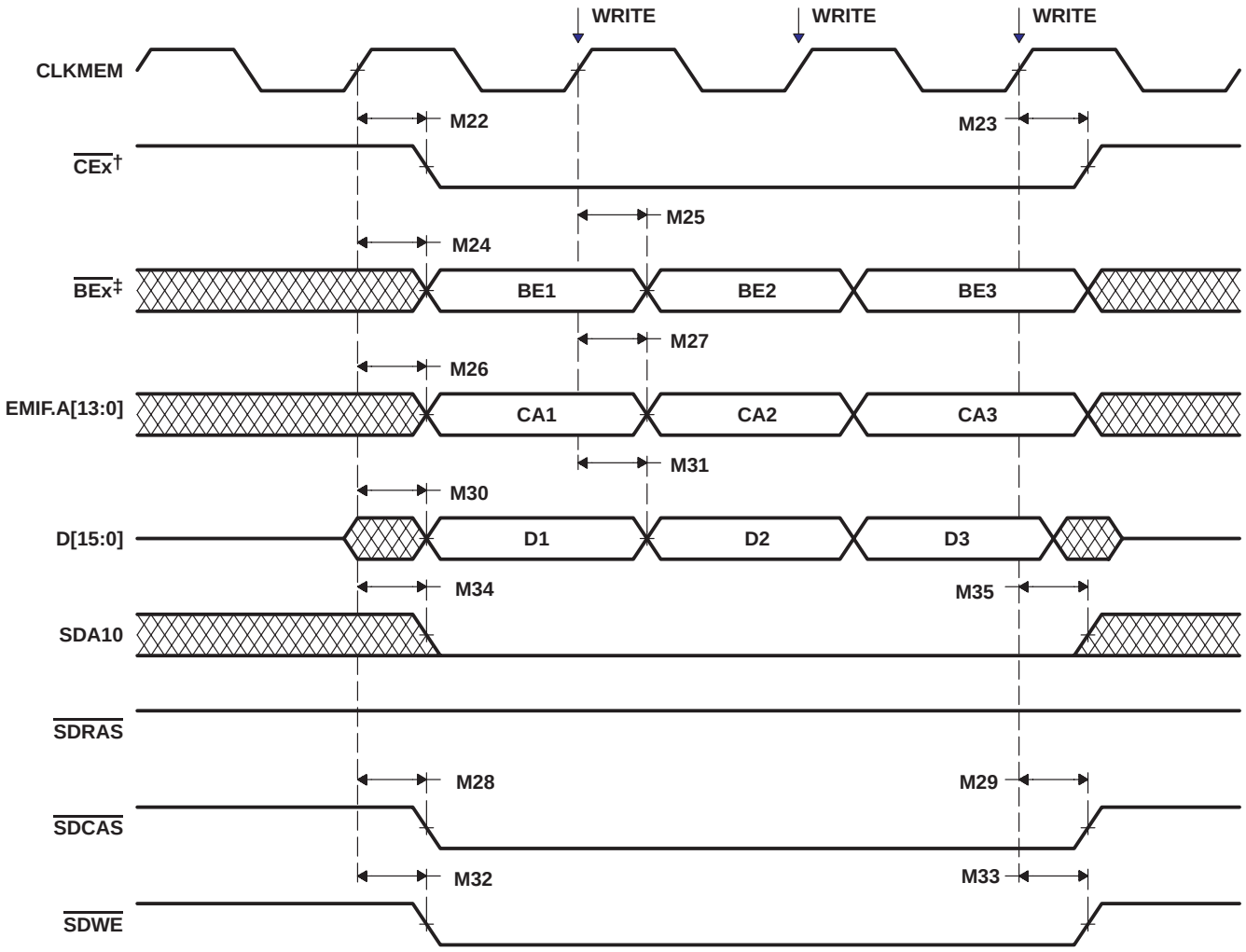
**Table 5−10. Synchronous DRAM Cycle Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| M22 | $t_{d(CLKMEMH-CEL)}$ | Delay time, CLKMEM high to $\overline{CEx}$ low | 1.2 | 7 | 1.2 | 5 | ns |
| M23 | $t_{d(CLKMEMH-CEH)}$ | Delay time, CLKMEM high to $\overline{CEx}$ high | 1.2 | 7 | 1.2 | 5 | ns |
| M24 | $t_{d(CLKMEMH-BEV)}$ | Delay time, CLKMEM high to $\overline{BEx}$ valid | 1.2 | 7 | 1.2 | 5 | ns |
| M25 | $t_{d(CLKMEMH-BEIV)}$ | Delay time, CLKMEM high to $\overline{BEx}$ invalid | 1.2 | 7 | 1.2 | 5 | ns |
| M26 | $t_{d(CLKMEMH-AV)}$ | Delay time, CLKMEM high to address valid | 1.2 | 7 | 1.2 | 5 | ns |
| M27 | $t_{d(CLKMEMH-AIV)}$ | Delay time, CLKMEM high to address invalid | 1.2 | 7 | 1.2 | 5 | ns |
| M28 | $t_{d(CLKMEMH-SDCASL)}$ | Delay time, CLKMEM high to $\overline{SDCAS}$ low | 1.2 | 7 | 1.2 | 5 | ns |
| M29 | $t_{d(CLKMEMH-SDCASH)}$ | Delay time, CLKMEM high to $\overline{SDCAS}$ high | 1.2 | 7 | 1.2 | 5 | ns |
| M30 | $t_{d(CLKMEMH-DV)}$ | Delay time, CLKMEM high to data valid | 1.2 | 7 | 1.2 | 5 | ns |
| M31 | $t_{d(CLKMEMH-DIV)}$ | Delay time, CLKMEM high to data invalid | 1.2 | 7 | 1.2 | 5 | ns |
| M32 | $t_{d(CLKMEMH-SDWEL)}$ | Delay time, CLKMEM high to $\overline{SDWE}$ low | 1.2 | 7 | 1.2 | 5 | ns |
| M33 | $t_{d(CLKMEMH-SDWEH)}$ | Delay time, CLKMEM high to $\overline{SDWE}$ high | 1.2 | 7 | 1.2 | 5 | ns |
| M34 | $t_{d(CLKMEMH-SDA10V)}$ | Delay time, CLKMEM high to SDA10 valid | 1.2 | 7 | 1.2 | 5 | ns |
| M35 | $t_{d(CLKMEMH-SDA10IV)}$ | Delay time, CLKMEM high to SDA10 invalid | 1.2 | 7 | 1.2 | 5 | ns |
| M36 | $t_{d(CLKMEMH-SDRASL)}$ | Delay time, CLKMEM high to $\overline{SDRAS}$ low | 1.2 | 7 | 1.2 | 5 | ns |
| M37 | $t_{d(CLKMEMH-SDRASH)}$ | Delay time, CLKMEM high to $\overline{SDRAS}$ high | 1.2 | 7 | 1.2 | 5 | ns |
| M38 | $t_{d(CLKMEMH–CKEL)}$ | Delay time, CLKMEM high to CKE low | 1.2 | 7 | 1.2 | 5 | ns |
| M39 | $t_{d(CLKMEMH–CKEH)}$ | Delay time, CLKMEM high to CKE high | 1.2 | 7 | 1.2 | 5 | ns |



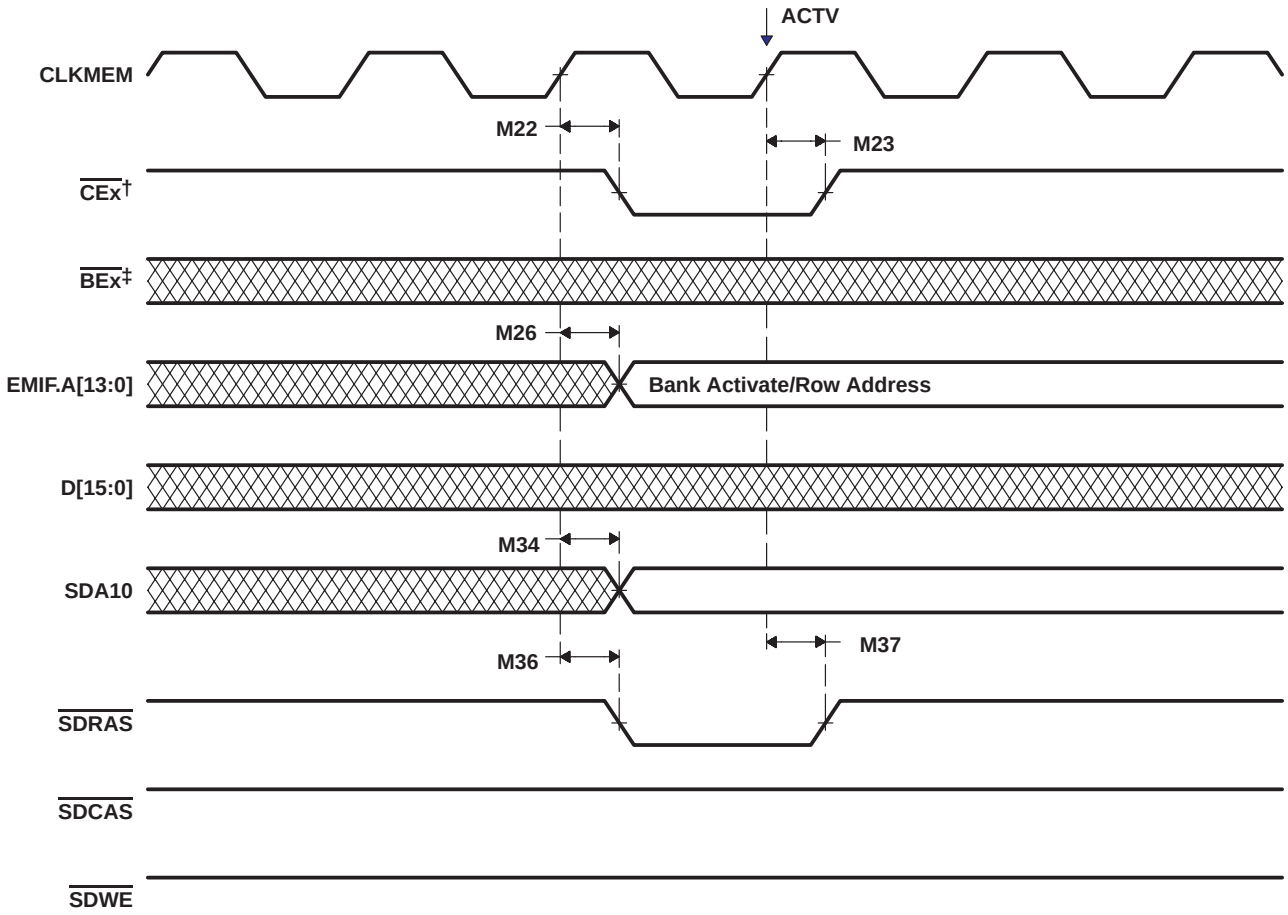

† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.

**Figure 5−8. Three SDRAM Read Commands**



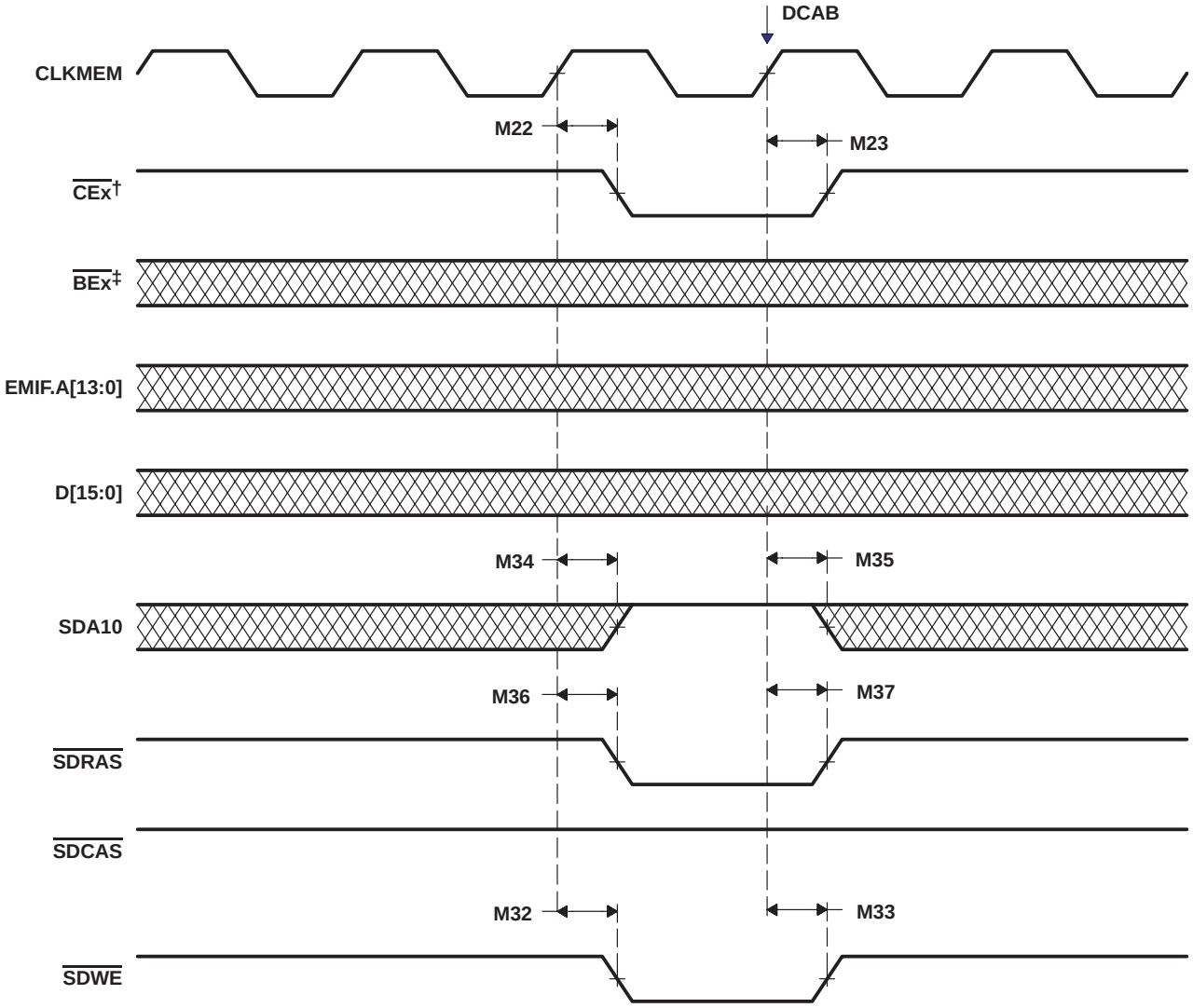

† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.

**Figure 5−9. Three SDRAM WRT Commands**



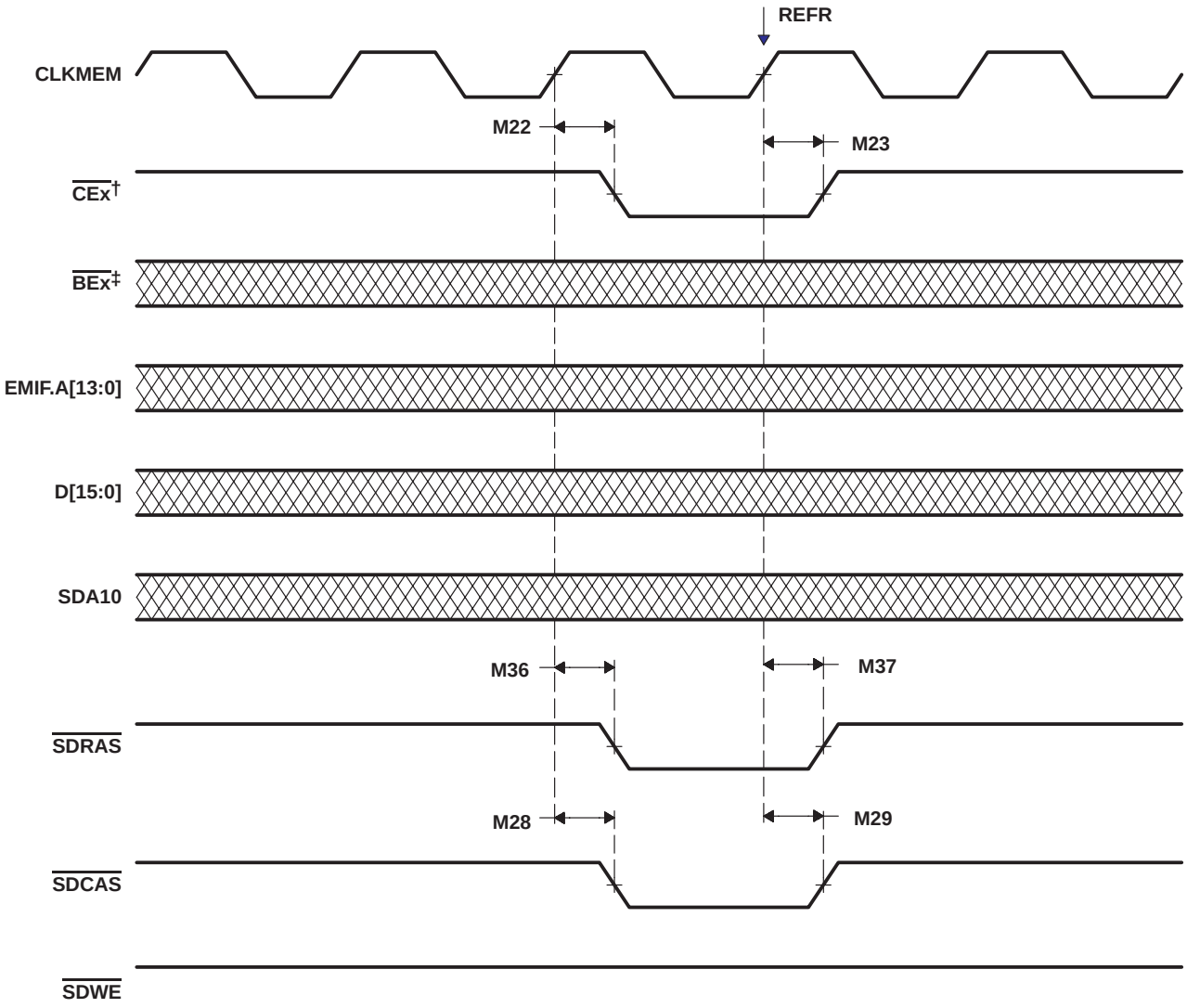

† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.

**Figure 5−10. SDRAM ACTV Command**



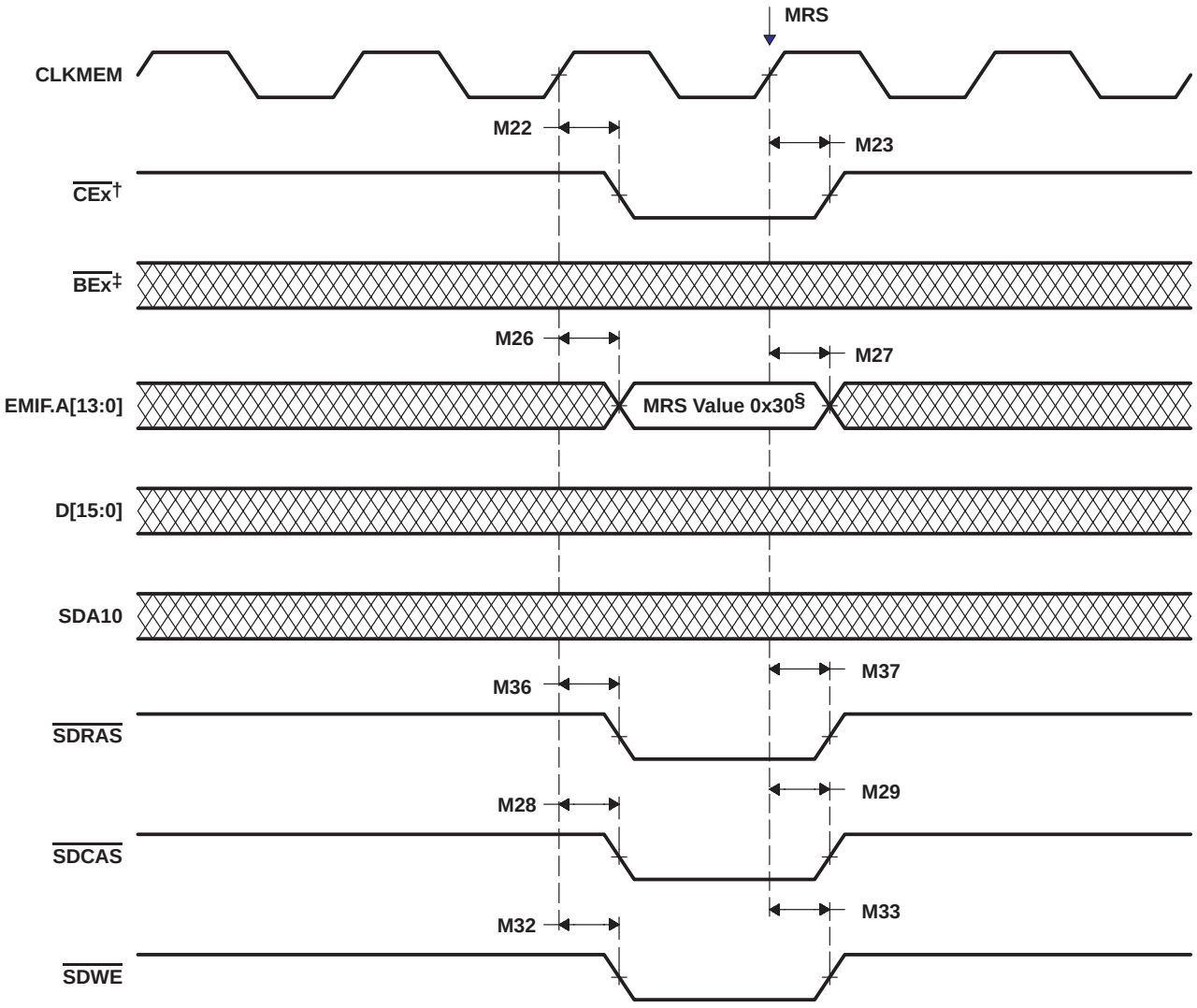

† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.

**Figure 5−11. SDRAM DCAB Command**




† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.

**Figure 5−12. SDRAM REFR Command**




† The chip enable that becomes active depends on the address being accessed.
‡ All BE[1:0] signals are driven low (active) during reads. Byte manipulation of the read data is performed inside the EMIF. These signals remain active until the next access that is not an SDRAM read occurs.
§ Write burst length = 1
Read latency = 3
Burst type = 0 (serial)
Burst length = 1

**Figure 5−13. SDRAM MRS Command**

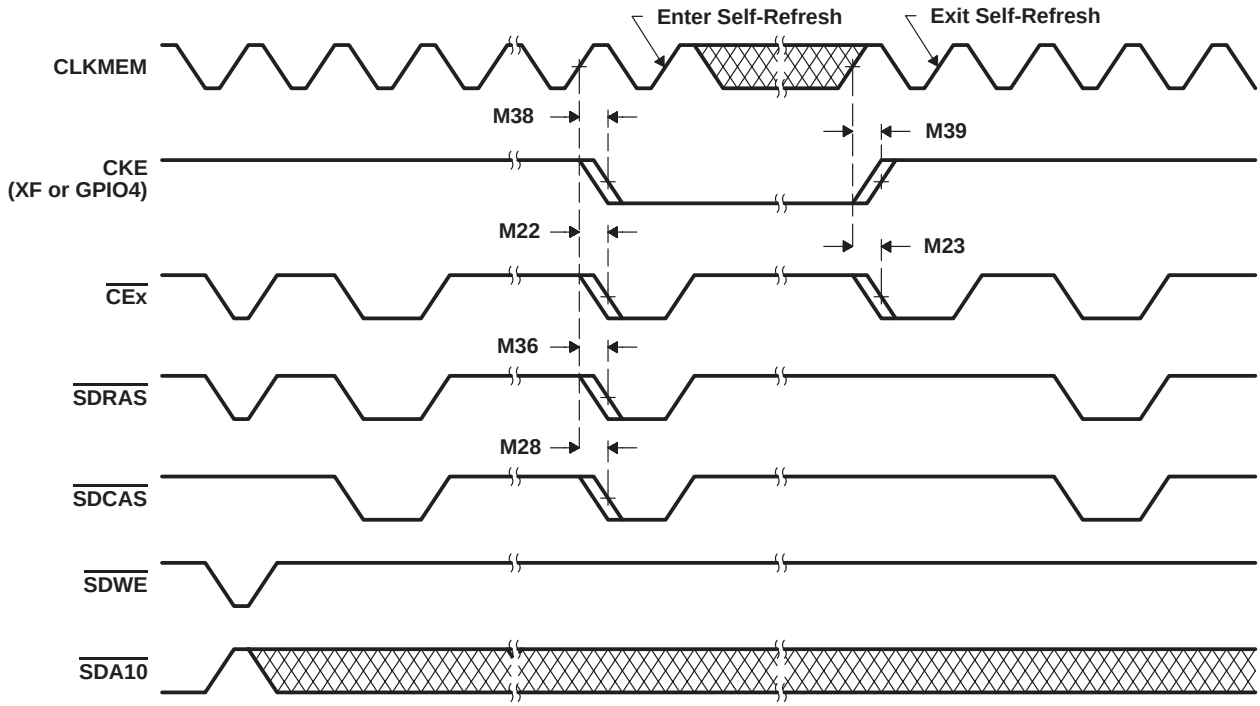



**Figure 5−14. SDRAM Self-Refresh Command**

## 5.8 Reset Timings

### 5.8.1 Power-Up Reset (On-Chip Oscillator Active)

Table 5−11 assumes testing over recommended operating conditions (see Figure 5−15).

**Table 5−11. Power-Up Reset (On-Chip Oscillator Active) Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| R1 | $t_{h(SUPSTBL-RSTL)}$ | Hold time, $\overline{RESET}$ low after oscillator stable† | 3P‡ | | 3P‡ | | ns |

† Oscillator stable time depends on the crystal characteristic (i.e., frequency, ESR, etc.) which varies from one crystal manufacturer to another. Based on the crystal characteristics, the oscillator stable time can be in the range of a few to 10s of ms. A reset circuit with 100 ms or more delay time will ensure the oscillator stabilized before the $\overline{RESET}$ goes high.

‡ P = 1/(input clock frequency) in ns. For example, when input clock is 12 MHz, P = 83.33 ns.

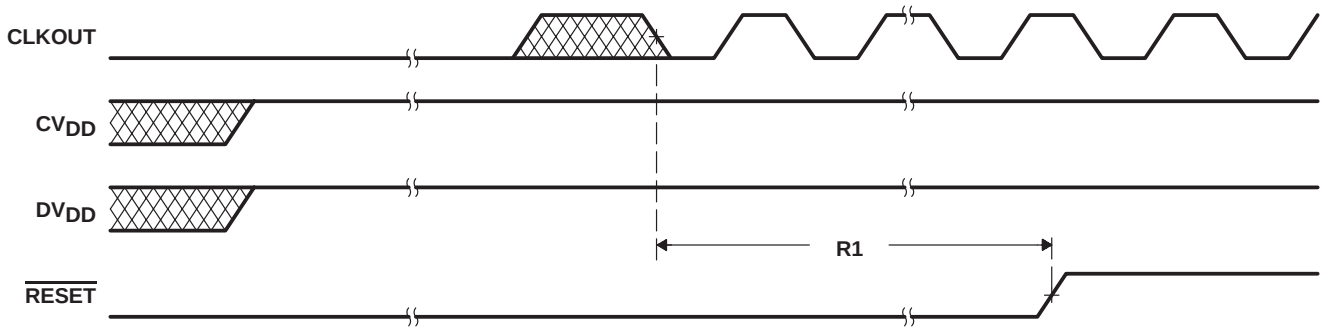



**Figure 5−15. Power-Up Reset (On-Chip Oscillator Active) Timings**

### 5.8.2 Power-Up Reset (On-Chip Oscillator Inactive)

Table 5−12 and Table 5−13 assume testing over recommended operating conditions (see Figure 5−16).

**Table 5−12. Power-Up Reset (On-Chip Oscillator Inactive) Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| R2 | $t_{h(CLKOUTV-RSTL)}$ | Hold time, CLKOUT valid to $\overline{RESET}$ low | 3P‡ | | 3P‡ | | ns |

‡ P = 1/(input clock frequency) in ns. For example, when input clock is 12 MHz, P = 83.33 ns.

**Table 5−13. Power-Up Reset (On-Chip Oscillator Inactive) Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| R3 | $t_{d(CLKINV-CLKOUTV)}$ | Delay time, CLKIN valid to CLKOUT valid | | 30 | | 30 | ns |

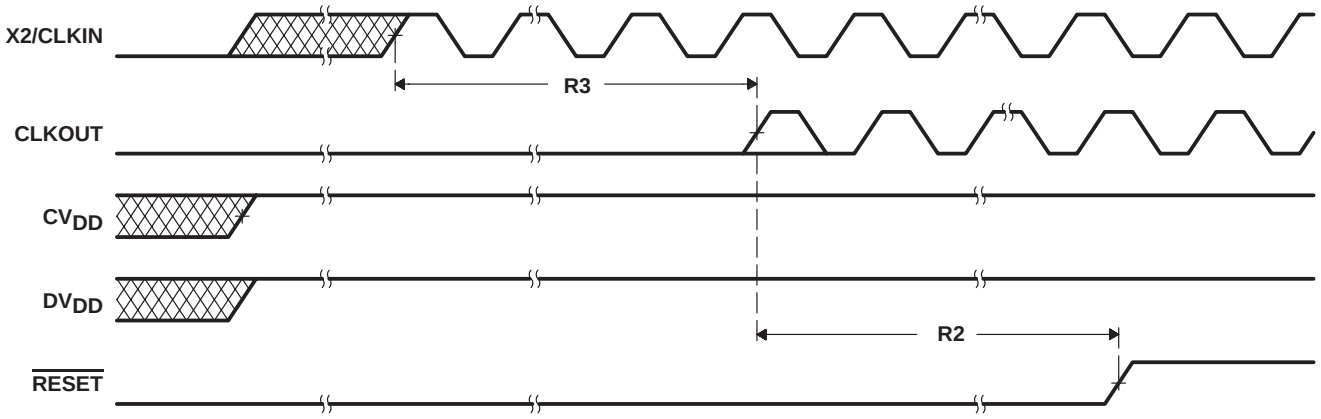



**Figure 5−16. Power-Up Reset (On-Chip Oscillator Inactive) Timings**

### 5.8.3 Warm Reset

Table 5−14 and Table 5−15 assume testing over recommended operating conditions (see Figure 5−17).

**Table 5−14. Reset Timing Requirements**

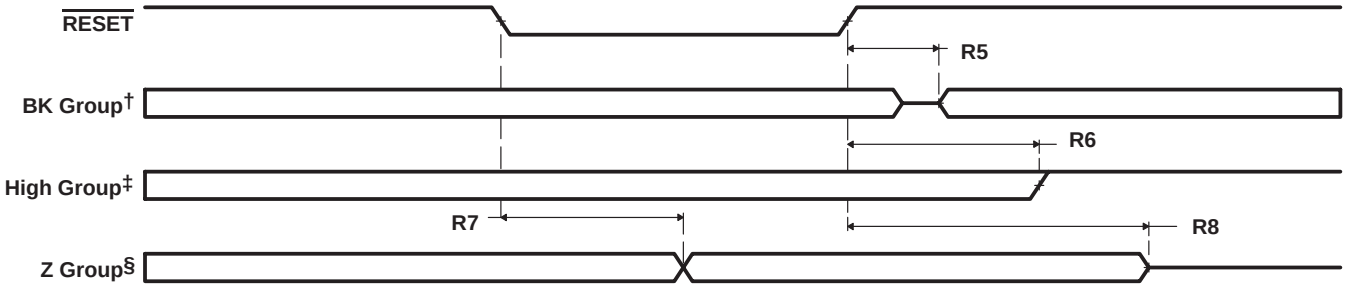
| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| R4 | $t_{w(RSL)}$ | Pulse width, reset low | 3P† | | 3P† | | ns |

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

**Table 5−15. Reset Switching Characteristics†**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| R5 | $t_{d(RSTH-BKV)}$ | Delay time, reset high to BK group valid‡ | | 38P + 15 | | 38P + 15 | ns |
| R6 | $t_{d(RSTH-HIGHV)}$ | Delay time, reset high to High group valid§ | | 38P + 15 | | 38P + 15 | ns |
| R7 | $t_{d(RSTL-ZIV)}$ | Delay time, reset low to Z group invalid¶ | | 1P + 15 | | 1P + 15 | ns |
| R8 | $t_{d(RSTH-ZV)}$ | Delay time, reset high to Z group valid¶ | | 38P + 15 | | 38P + 15 | ns |

† P = 1/CPU clock frequency in ns. For example, when CPU is running at 200 MHz, P = 5 ns.
‡ BK group: Pins with bus keepers, holds previous state during reset. Following low-to-high transition of $\overline{\text{RESET}}$, these pins go to their post-reset logic state.
BK group pins: A'[0], A[15:0], D[15:0], C[14:2], C0, GPIO5, S13, and S23
§ High group: Following low-to-high transition of $\overline{\text{RESET}}$, these pins go to logic-high state.
High group pins: C1[HPI.$\overline{\text{HINT}}$], XF
¶ Z group: Bidirectional pins which become input or output pins. Following low-to-high transition of $\overline{\text{RESET}}$, these pins go to high-impedance state.
Z group pins: C1[EMIF.AOE], GPIO[7:6, 4:0], TIN/TOUT0, SDA, SCL, CLKR0, FSRX0, CLKX0, DX0, FSX0, S[25:24, 22:20, 15:14, 12:10], A[20:16]




† BK group pins: A'[0], A[15:0], D[15:0], C[14:2], C0, GPIO5, S13, and S23
‡ High group pins: C1[HPI.$\overline{\text{HINT}}$], XF
§ Z group pins: C1[EMIF.AOE], GPIO[7:6, 4:0], TIN/TOUT0, SDA, SCL, CLKR0, FSRX0, CLKX0, DX0, FSX0, S[25:24, 22:20, 15:14, 12:10], A[20:16]

**Figure 5−17. Reset Timings**

## 5.9 External Interrupt Timings

Table 5−16 assumes testing over recommended operating conditions (see Figure 5−18).

**Table 5−16. External Interrupt Timing Requirements†**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| I1 | $t_{w(INTH)A}$ | Pulse width, interrupt high, CPU active | 2P | | 2P | | ns |
| I2 | $t_{w(INTL)A}$ | Pulse width, interrupt low, CPU active | 3P | | 3P | | ns |

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

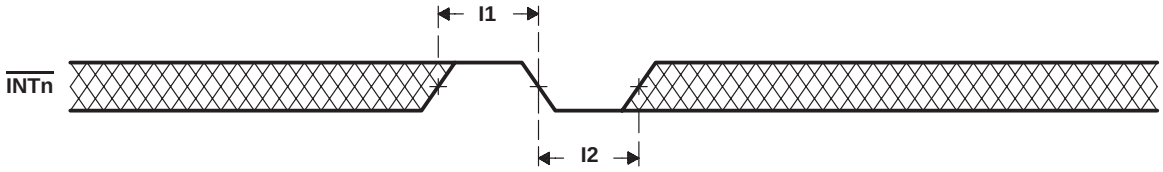



**Figure 5−18. External Interrupt Timings**

## 5.10 Wake-Up From IDLE

Table 5−17 assumes testing over recommended operating conditions (see Figure 5−19).

**Table 5−17. Wake-Up From IDLE Switching Characteristics†**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | $CV_{DD}$ = 1.6 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| ID1 | $t_{d(WKPEVTL-CLKGEN)}$ | Delay time, wake-up event low to clock generation enable (CPU and clock domain idle) | | 1.25‡ | | | 1.25‡ | | ms |
| ID2 | $t_{h(CLKGEN-WKPEVTL)}$ | Hold time, clock generation enable to wake-up event low (CPU and clock domain in idle) | 3P§ | | | 3P§ | | | ns |
| ID3 | $t_{w(WKPEVTL)}$ | Pulse width, wake-up event low (for CPU idle only) | 3P | | | 3P | | | ns |

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

‡ Estimated data based on 12-MHz crystal used with on-chip oscillator at 25°C. This number will vary based on the actual crystal characteristics operating condition and the PC board layout and the parasitics.

§ Following the clock generation domain idle, the $\overline{INTx}$ becomes level-sensitive and stays that way until the low-to-high transition of $\overline{INTx}$ following the CPU wake-up. Holding the $\overline{INTx}$ low longer than minimum requirement will send more than one interrupt to the CPU. The number of interrupts sent to the CPU depends on the $\overline{INTx}$-low time following the CPU wake-up from IDLE.

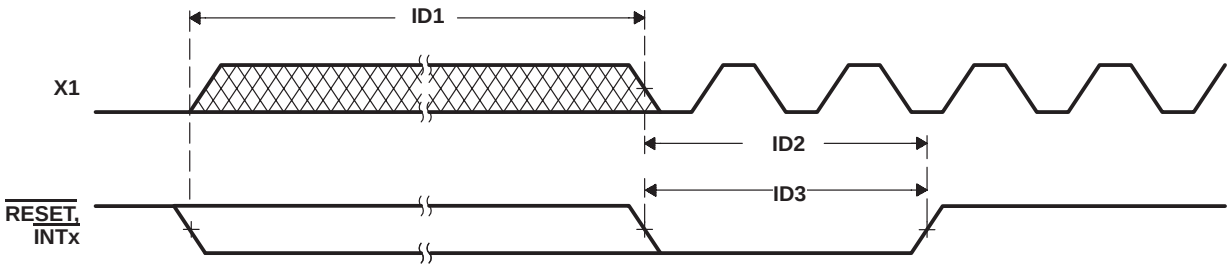


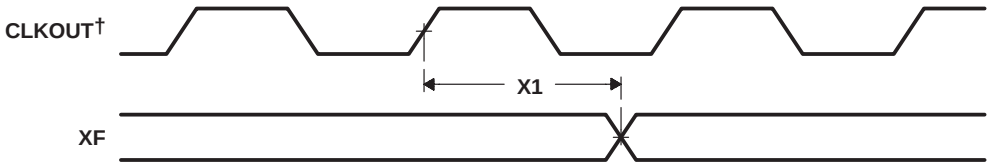

**Figure 5−19. Wake-Up From IDLE Timings**

## 5.11 XF Timings

Table 5−18 assumes testing over recommended operating conditions (see Figure 5−20).

**Table 5−18. XF Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| X1 | $t_{d(XF)}$ | Delay time, CLKOUT high to XF high | −1 | 3 | −1 | 3 | ns |
| | | Delay time, CLKOUT high to XF low | −1 | 3 | −1 | 3 | |




† CLKOUT reflects the CPU clock.

**Figure 5−20. XF Timings**

## 5.12 General-Purpose Input/Output (GPIOx) Timings

Table 5−19 and Table 5−20 assume testing over recommended operating conditions (see Figure 5−21).

**Table 5−19. GPIO Pins Configured as Inputs Timing Requirements**

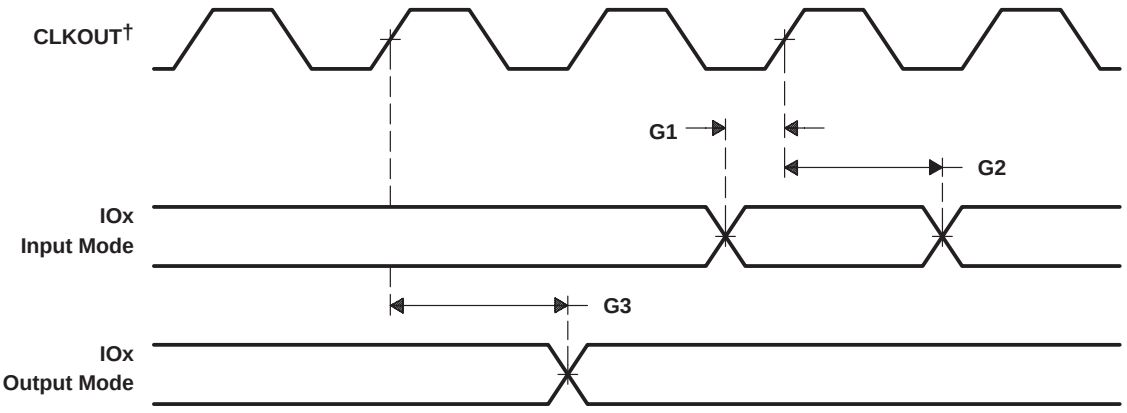
| NO. | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| G1 | $t_{su(GPIO-COH)}$ | Setup time, IOx input valid before CLKOUT high | GPIO | 4 | | 4 | | ns |
| | | | AGPIO† | 8 | | 8 | | |
| | | | EHPIGPIO‡ | 8 | | 8 | | |
| G2 | $t_{h(COH-GPIO)}$ | Hold time, IOx input valid after CLKOUT high | GPIO | 0 | | 0 | | ns |
| | | | AGPIO† | 0 | | 0 | | |
| | | | EHPIGPIO‡ | 0 | | 0 | | |

† AGPIO pins: A[15:0]
‡ EHPIGPIO pins: C13, C10, C7, C5, C4, and C0

**Table 5−20. GPIO Pins Configured as Outputs Switching Characteristics**

| NO. | PARAMETER | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| G3 | $t_{d(COH-GPIO)}$ | Delay time, CLKOUT high to IOx output change | GPIO | 0 | 6 | 0 | 6 | ns |
| | | | AGPIO† | 0 | 11 | 0 | 11 | |
| | | | EHPIGPIO‡ | 0 | 13 | 0 | 13 | |

† AGPIO pins: A[15:0]
‡ EHPIGPIO pins: C13, C10, C7, C5, C4, and C0




† CLKOUT reflects the CPU clock.

**Figure 5−21. General-Purpose Input/Output (IOx) Signal Timings**

## 5.13 TIN/TOUT Timings (Timer0 Only)

Table 5−21 and Table 5−22 assume testing over recommended operating conditions (see Figure 5−22 and Figure 5−23).

**Table 5−21. TIN/TOUT Pins Configured as Inputs Timing Requirements†‡**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| T4 | $t_{w(TIN/TOUTL)}$ | Pulse width, TIN/TOUT low | 2P + 1 | | 2P + 1 | | ns |
| T5 | $t_{w(TIN/TOUTH)}$ | Pulse width, TIN/TOUT high | 2P + 1 | | 2P + 1 | | ns |

† P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns.
‡ Only the Timer0 signal is externally available. The Timer1 signal is internally terminated and is not available for external use.

**Table 5−22. TIN/TOUT Pins Configured as Outputs Switching Characteristics†‡§**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| T1 | $t_{d(COH-TIN/TOUTH)}$ | Delay time, CLKOUT high to TIN/TOUT high | −1 | 3 | −1 | 3 | ns |
| T2 | $t_{d(COH-TIN/TOUTL)}$ | Delay time, CLKOUT high to TIN/TOUT low | −1 | 3 | −1 | 3 | ns |
| T3 | $t_{w(TIN/TOUT)}$ | Pulse duration, TIN/TOUT (output) | P − 1 | | P − 1 | | ns |

† P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns.
‡ Only the Timer0 signal is externally available. The Timer1 signal is internally terminated and is not available for external use.
§ For proper operation of the TIN/TOUT pin configured as an output, the timer period must be configured for at least 4 cycles.

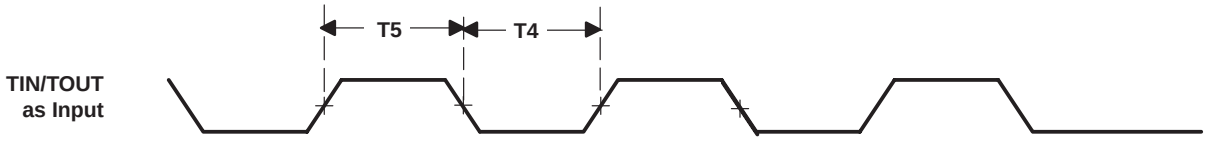



**Figure 5−22. TIN/TOUT Timings When Configured as Inputs**

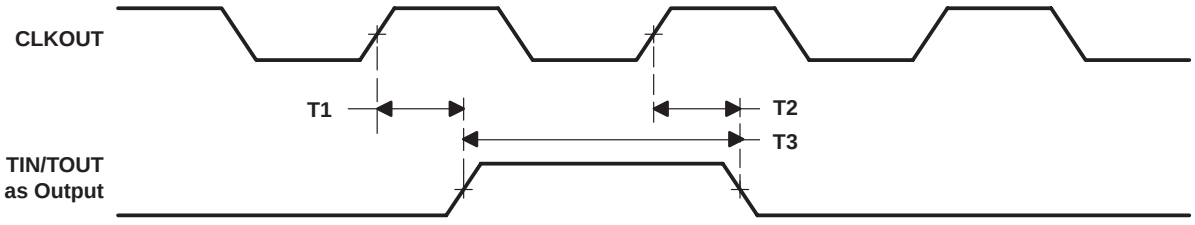



**Figure 5−23. TIN/TOUT Timings When Configured as Outputs**

## 5.14 Multichannel Buffered Serial Port (McBSP) Timings

### *5.14.1 McBSP0 Timings*

Table 5−23 and Table 5−24 assume testing over recommended operating conditions (see Figure 5−24 and Figure 5−25).

**Table 5−23. McBSP0 Timing Requirements†**

| NO. | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| MC1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P‡ | | 2P‡ | | ns |
| MC2 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P–1‡ | | P–1‡ | | ns |
| MC3 | $t_{r(CKRX)}$ | Rise time, CLKR/X | CLKR/X ext | | 6 | | 6 | ns |
| MC4 | $t_{f(CKRX)}$ | Fall time, CLKR/X | CLKR/X ext | | 6 | | 6 | ns |
| MC5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 10 | | 7 | | ns |
| | | | CLKR ext | 2 | | 2 | | |
| MC6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | −3 | | −3 | | ns |
| | | | CLKR ext | 1 | | 1 | | |
| MC7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 10 | | 7 | | ns |
| | | | CLKR ext | 2 | | 2 | | |
| MC8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | −2 | | −2 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| MC9 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 13 | | 8 | | ns |
| | | | CLKX ext | 3 | | 2 | | |
| MC10 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | −3 | | −3 | | ns |
| | | | CLKX ext | 1 | | 1 | | |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

**Table 5−24. McBSP0 Switching Characteristics†‡**

| NO. | PARAMETER | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | MIN | MAX | |
| MC1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | | CLKR/X int | 2P | | 2P | | ns |
| MC3 | $t_{r(CKRX)}$ | Rise time, CLKR/X | | CLKR/X int | | 1 | | 1 | ns |
| MC4 | $t_{f(CKRX)}$ | Fall time, CLKR/X | | CLKR/X int | | 1 | | 1 | ns |
| MC11 | $t_{w(CKRXH)}$ | Pulse duration, CLKR/X high | | CLKR/X int | D−2§ | D+2§ | D−1§ | D+1§ | ns |
| MC12 | $t_{w(CKRXL)}$ | Pulse duration, CLKR/X low | | CLKR/X int | C−2§ | C+2§ | C−1§ | C+1§ | ns |
| MC13 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | | CLKR int | −2 | 1 | −2 | 1 | ns |
| | | | | CLKR ext | 4 | 13 | 4 | 8 | |
| MC14 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | | CLKX int | −2 | 2 | −2 | 2 | ns |
| | | | | CLKX ext | 4 | 15 | 4 | 9 | |
| MC15 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high-impedance from CLKX high following last data bit | | CLKX int | 0 | 5 | −5 | 1 | ns |
| | | | | CLKX ext | 10 | 18 | 3 | 11 | |
| MC16 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted. | | CLKX int | | 5 | | 4 | ns |
| | | | | CLKX ext | | 15 | | 9 | |
| | | Delay time, CLKX high to DX valid¶ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes | DXENA = 0 | CLKX int | | 4 | | 2 | |
| | | | | CLKX ext | | 13 | | 7 | |
| | | | DXENA = 1 | CLKX int | | 2P + 1 | | 2P + 1 | |
| | | | | CLKX ext | | 2P + 4 | | 2P + 3 | |
| MC17 | $t_{en(CKXH-DX)}$ | Enable time, DX driven from CLKX high¶ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY= 01b or 10b) modes | DXENA = 0 | CLKX int | −1 | | −3 | | ns |
| | | | | CLKX ext | 6 | | 3 | | |
| | | | DXENA = 1 | CLKX int | P − 1 | | P − 3 | | |
| | | | | CLKX ext | P + 6 | | P + 3 | | |
| MC18 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid¶ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY= 00b) mode. | DXENA = 0 | FSX int | | 2 | | 2 | ns |
| | | | | FSX ext | | 13 | | 8 | |
| | | | DXENA = 1 | FSX int | | 2P + 1 | | 2P + 1 | |
| | | | | FSX ext | | 2P + 10 | | 2P + 10 | |
| MC19 | $t_{en(FXH-DX)}$ | Enable time, DX driven from FSX high¶ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY= 00b) mode | DXENA = 0 | FSX int | 0 | | 0 | | ns |
| | | | | FSX ext | 8 | | 3 | | |
| | | | DXENA = 1 | FSX int | P − 3 | | P − 3 | | |
| | | | | FSX ext | P + 8 | | P + 4 | | |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

§ T=CLKRX period = (1 + CLKGDV) * P
C=CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D=CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

¶ See the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317) for a description of the DX enable (DXENA) and data delay features of the McBSP.

### 5.14.2 McBSP1 and McBSP2 Timings

Table 5−25 and Table 5−26 assume testing over recommended operating conditions (see Figure 5−24 and Figure 5−25).

**Table 5−25. McBSP1 and McBSP2 Timing Requirements†**

| NO. | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| MC1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P‡ | | 2P‡ | | ns |
| MC2 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P–1‡ | | P–1‡ | | ns |
| MC3 | $t_{r(CKRX)}$ | Rise time, CLKR/X | CLKR/X ext | | 6 | | 6 | ns |
| MC4 | $t_{f(CKRX)}$ | Fall time, CLKR/X | CLKR/X ext | | 6 | | 6 | ns |
| MC5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 11 | | 7 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| MC6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | −3 | | −3 | | ns |
| | | | CLKR ext | 1 | | 1 | | |
| MC7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 11 | | 7 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| MC8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | −2 | | −2 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| MC9 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 14 | | 9 | | ns |
| | | | CLKX ext | 4 | | 3 | | |
| MC10 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | −3 | | −3 | | ns |
| | | | CLKX ext | 1 | | 1 | | |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

**Table 5−26. McBSP1 and McBSP2 Switching Characteristics†‡**

| NO. | PARAMETER | | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | MIN | MAX | |
| MC1 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | | CLKR/X int | 2P | | 2P | | ns |
| MC3 | $t_{r(CKRX)}$ | Rise time, CLKR/X | | CLKR/X int | | 2 | | 2 | ns |
| MC4 | $t_{f(CKRX)}$ | Fall time, CLKR/X | | CLKR/X int | | 2 | | 2 | ns |
| MC11 | $t_{w(CKRXH)}$ | Pulse duration, CLKR/X high | | CLKR/X int | D − 2§ | D + 2§ | D − 2§ | D + 2§ | ns |
| MC12 | $t_{w(CKRXL)}$ | Pulse duration, CLKR/X low | | CLKR/X int | C − 2§ | C + 2§ | C − 2§ | C + 2§ | ns |
| MC13 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | | CLKR int | −3 | 2 | −3 | 2 | ns |
| | | | | CLKR ext | 3 | 14 | 3 | 9 | |
| MC14 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | | CLKX int | −3 | 2 | −3 | 2 | ns |
| | | | | CLKX ext | 4 | 15 | 4 | 9 | |
| MC15 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high-impedance from CLKX high following last data bit | | CLKX int | −3 | 3 | −5 | 1 | ns |
| | | | | CLKX ext | 10 | 19 | 3 | 12 | |
| MC16 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted. | | CLKX int | | 5 | | 3 | ns |
| | | | | CLKX ext | | 15 | | 9 | |
| | | Delay time, CLKX high to DX valid¶ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY= 01b or 10b) modes | DXENA = 0 | CLKX int | | 4 | | 2 | |
| | | | | CLKX ext | | 15 | | 9 | |
| | | | DXENA = 1 | CLKX int | | 2P + 1 | | 2P + 1 | |
| | | | | CLKX ext | | 2P + 5 | | 2P + 3 | |
| MC17 | $t_{en(CKXH-DX)}$ | Enable time, DX driven from CLKX high¶ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY= 01b or 10b) modes | DXENA = 0 | CLKX int | −2 | | −4 | | ns |
| | | | | CLKX ext | 9 | | 4 | | |
| | | | DXENA = 1 | CLKX int | P − 2 | | P − 4 | | |
| | | | | CLKX ext | P + 9 | | P + 4 | | |
| MC18 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid¶ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode. | DXENA = 0 | FSX int | | 3 | | 2 | ns |
| | | | | FSX ext | | 13 | | 8 | |
| | | | DXENA = 1 | FSX int | | 2P + 1 | | 2P + 1 | |
| | | | | FSX ext | | 2P + 12 | | 2P + 7 | |
| MC19 | $t_{en(FXH-DX)}$ | Enable time, DX driven from FSX high¶ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode | DXENA = 0 | FSX int | 1 | | 0 | | ns |
| | | | | FSX ext | 8 | | 4 | | |
| | | | DXENA = 1 | FSX int | P − 1 | | P − 3 | | |
| | | | | FSX ext | P + 8 | | P + 5 | | |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

§ T=CLKRX period = (1 + CLKGDV) * P
C=CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D=CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

¶ See the *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317) for a description of the DX enable (DXENA) and data delay features of the McBSP.

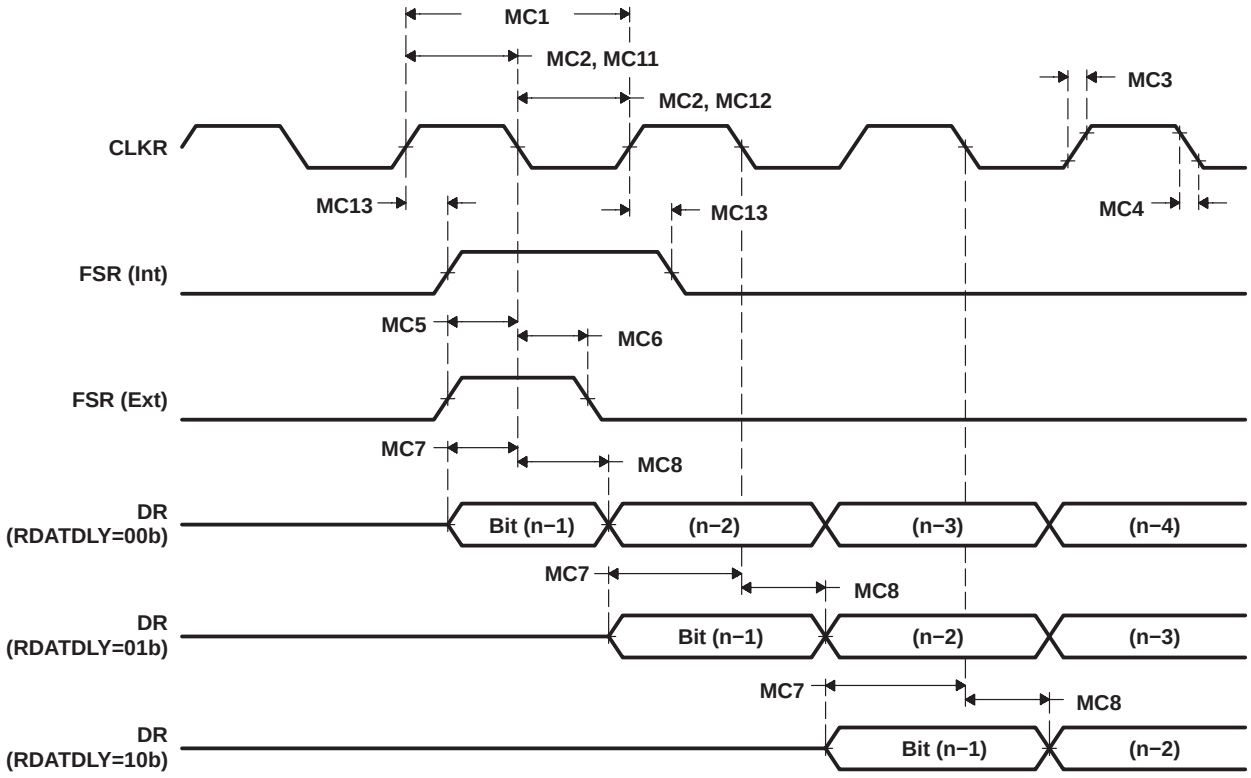



**Figure 5−24. McBSP Receive Timings**

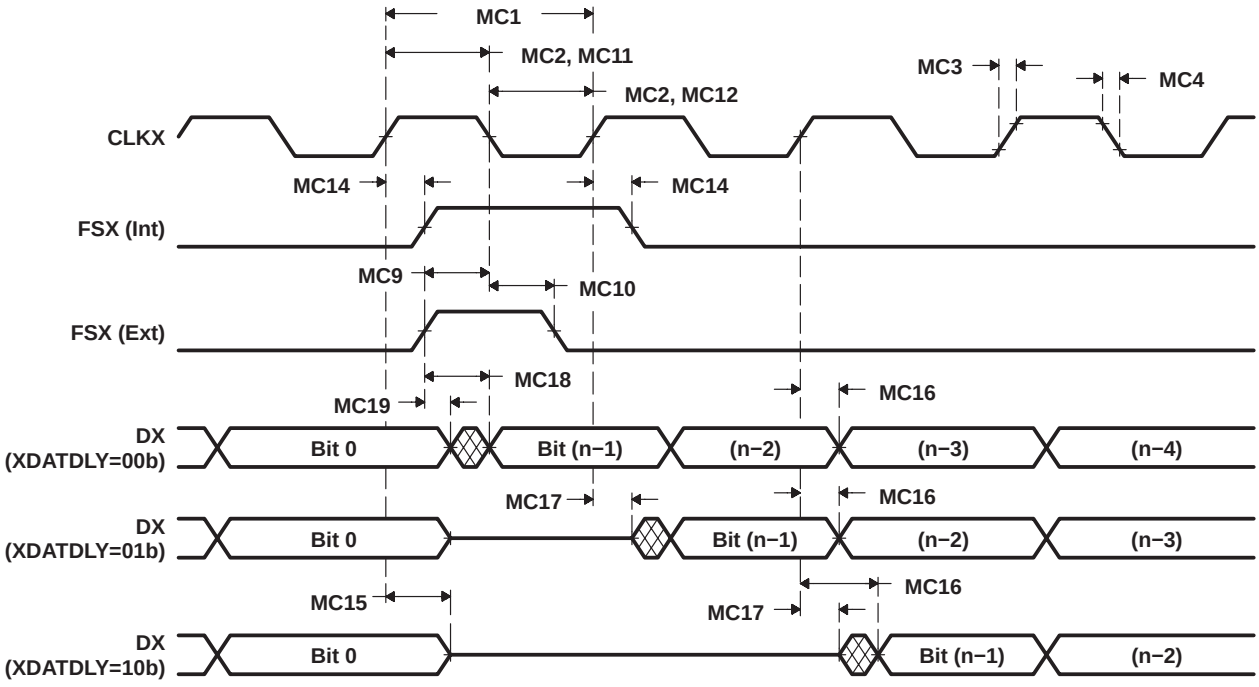



**Figure 5−25. McBSP Transmit Timings**

### 5.14.3 McBSP as SPI Master or Slave Timings

Table 5−27 to Table 5−34 assume testing over recommended operating conditions (see Figure 5−26 through Figure 5−29).

**Table 5−27. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†‡**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER | | SLAVE | | MASTER | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC23 | $t_{su(DRV-CKXL)}$ | Setup time, DR valid before CLKX low | 15 | | 3 − 6P | | 10 | | 3 − 6P | | ns |
| MC24 | $t_{h(CKXL-DRV)}$ | Hold time, DR valid after CLKX low | 0 | | 3 + 6P | | 0 | | 3 + 6P | | ns |
| MC25 | $t_{su(FXL-CKXH)}$ | Setup time, FSX low before CLKX high | | | 5 | | | | 5 | | ns |
| MC26 | $t_{c(CKX)}$ | Cycle time, CLKX | 2P | | 16P | | 2P | | 16P | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

**Table 5−28. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†‡**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER§ | | SLAVE | | MASTER§ | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC27 | $t_{d(CKXL-FXL)}$ | Delay time, CLKX low to FSX low¶ | T − 5 | T + 5 | | | T − 4 | T + 4 | | | ns |
| MC28 | $t_{d(FXL-CKXH)}$ | Delay time, FSX low to CLKX high# | C − 5 | C + 5 | | | C − 4 | C + 4 | | | ns |
| MC29 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | −4 | 6 | 3P + 3 | 5P + 15 | −3 | 3 | 3P + 3 | 5P + 8 | ns |
| MC30 | $t_{dis(CKXL-DXHZ)}$ | Disable time, DX high-impedance following last data bit from CLKX low | C − 4 | C + 4 | | | C − 3 | C + 1 | | | ns |
| MC31 | $t_{dis(FXH-DXHZ)}$ | Disable time, DX high-impedance following last data bit from FSX high | | | 3P+ 4 | 3P + 19 | | | 3P+ 3 | 3P + 11 | ns |
| MC32 | $t_{d(FXL-DXV)}$ | Delay time, FSX low to DX valid | | | 3P + 4 | 3P + 18 | | | 3P + 4 | 3P + 10 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.
§ T = CLKX period = (1 + CLKGDV) * 2P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

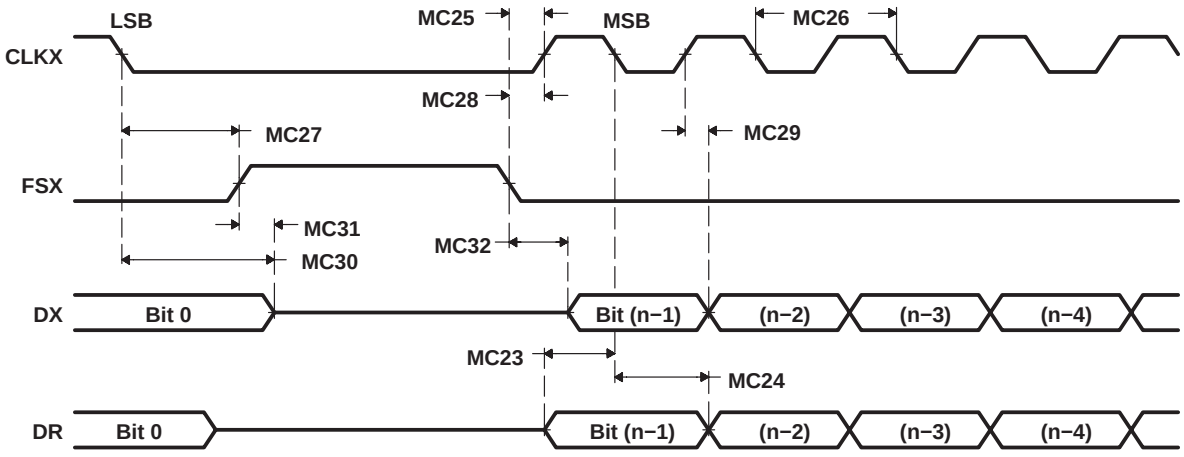



**Figure 5−26. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0**

### Table 5−29. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†‡

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER | | SLAVE | | MASTER | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC33 | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 15 | | 3 − 6P | | 10 | | 3 − 6P | | ns |
| MC34 | $t_{h(CKXH-DRV)}$ | Hold time, DR valid after CLKX high | 0 | | 3 + 6P | | 0 | | 3 + 6P | | ns |
| MC25 | $t_{su(FXL-CKXH)}$ | Setup time, FSX low before CLKX high | | | 5 | | | | 5 | | ns |
| MC26 | $t_{c(CKX)}$ | Cycle time, CLKX | 2P | | 16P | | 2P | | 16P | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

### Table 5−30. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†‡

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER§ | | SLAVE | | MASTER§ | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC27 | $t_{d(CKXL-FXL)}$ | Delay time, CLKX low to FSX low¶ | C − 5 | C + 5 | | | C − 4 | C + 4 | | | ns |
| MC28 | $t_{d(FXL-CKXH)}$ | Delay time, FSX low to CLKX high# | T − 5 | T + 5 | | | T − 4 | T + 4 | | | ns |
| MC35 | $t_{d(CKXL-DXV)}$ | Delay time, CLKX low to DX valid | −4 | 6 | 3P + 3 | 5P + 15 | −3 | 3 | 3P + 3 | 5P + 8 | ns |
| MC30 | $t_{dis(CKXL-DXHZ)}$ | Disable time, DX high-impedance following last data bit from CLKX low | −4 | 4 | 3P + 4 | 3P + 19 | −3 | 1 | 3P + 3 | 3P + 12 | ns |
| MC32 | $t_{d(FXL-DXV)}$ | Delay time, FSX low to DX valid | D − 4 | D + 4 | 3P + 4 | 3P + 18 | D − 3 | D + 3 | 3P + 4 | 3P + 10 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

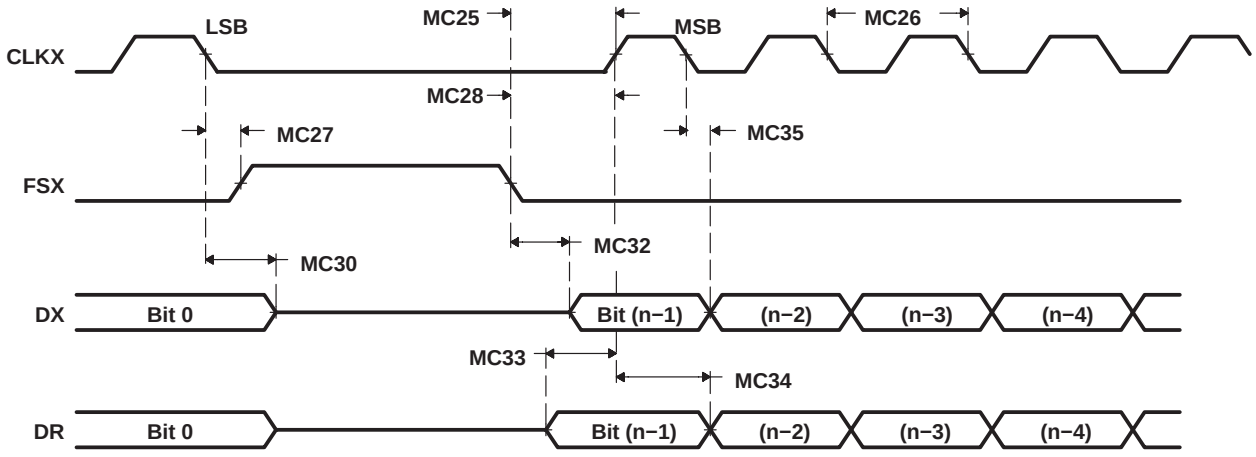



**Figure 5−27. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0**

**Table 5−31. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†‡**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER | | SLAVE | | MASTER | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC33 | $t_{su(DRV-CKXH)}$ | Setup time, DR valid before CLKX high | 15 | | 3 − 6P | | 10 | | 3 − 6P | | ns |
| MC34 | $t_{h(CKXH-DRV)}$ | Hold time, DR valid after CLKX high | 0 | | 3 + 6P | | 0 | | 3 + 6P | | ns |
| MC36 | $t_{su(FXL-CKXL)}$ | Setup time, FSX low before CLKX low | | | 5 | | | | 5 | | ns |
| MC26 | $t_{c(CKX)}$ | Cycle time, CLKX | 2P | | 16P | | 2P | | 16P | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

**Table 5−32. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†‡**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER§ | | SLAVE | | MASTER§ | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC37 | $t_{d(CKXH-FXL)}$ | Delay time, CLKX high to FSX low¶ | T − 5 | T + 5 | | | T − 4 | T + 4 | | | ns |
| MC38 | $t_{d(FXL-CKXL)}$ | Delay time, FSX low to CLKX low# | D − 5 | D + 5 | | | D − 4 | D + 4 | | | ns |
| MC35 | $t_{d(CKXL-DXV)}$ | Delay time, CLKX low to DX valid | −4 | 6 | 3P + 3 | 5P + 15 | −3 | 3 | 3P + 3 | 5P + 8 | ns |
| MC39 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high-impedance following last data bit from CLKX high | D − 4 | D + 4 | | | D − 3 | D + 1 | | | ns |
| MC31 | $t_{dis(FXH-DXHZ)}$ | Disable time, DX high-impedance following last data bit from FSX high | | | 3P + 4 | 3P +19 | | | 3P + 3 | 3P +11 | ns |
| MC32 | $t_{d(FXL-DXV)}$ | Delay time, FSX low to DX valid | | | 3P + 4 | 3P + 18 | | | 3P + 4 | 3P + 10 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

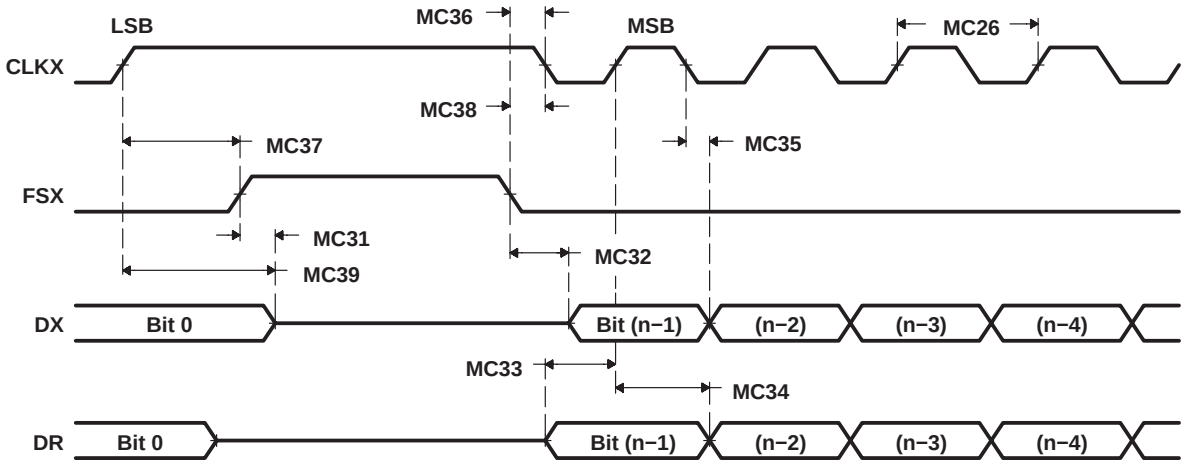



**Figure 5−28. McBSP Timings as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1**

### Table 5−33. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†‡

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER | | SLAVE | | MASTER | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC23 | $t_{su(DRV-CKXL)}$ | Setup time, DR valid before CLKX low | 15 | | 3 − 6P | | 10 | | 3 − 6P | | ns |
| MC24 | $t_{h(CKXL-DRV)}$ | Hold time, DR valid after CLKX low | 0 | | 3 + 6P | | 0 | | 3 + 6P | | ns |
| MC36 | $t_{su(FXL-CKXL)}$ | Setup time, FSX low before CLKX low | | | 5 | | | | 5 | | ns |
| MC26 | $t_{c(CKX)}$ | Cycle time, CLKX | 2P | | 16P | | 2P | | 16P | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.

### Table 5−34. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†‡

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MASTER§ | | SLAVE | | MASTER§ | | SLAVE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| MC37 | $t_{d(CKXH-FXL)}$ | Delay time, CLKX high to FSX low¶ | D − 5 | D + 5 | | | D − 4 | D + 4 | | | ns |
| MC38 | $t_{d(FXL-CKXL)}$ | Delay time, FSX low to CLKX low# | T − 5 | T + 5 | | | T − 4 | T + 4 | | | ns |
| MC29 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | −4 | 6 | 3P + 3 | 5P + 15 | −3 | 3 | 3P + 3 | 5P + 8 | ns |
| MC39 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high-impedance following last data bit from CLKX high | −4 | 4 | 3P + 4 | 3P + 19 | −3 | 1 | 3P + 3 | 3P + 12 | ns |
| MC32 | $t_{d(FXL-DXV)}$ | Delay time, FSX low to DX valid | C − 4 | C + 4 | 3P + 4 | 3P + 18 | C − 3 | C + 3 | 3P + 4 | 3P + 10 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
‡ P = 1/CPU clock frequency. For example, when running parts at 200 MHz, use P = 5 ns. In addition to CPU frequency, the maximum operating frequency of the serial port also depends on meeting the rest of the switching characteristics and timing requirements parameters specified.
§ T = CLKX period = (1 + CLKGDV) * P
C = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

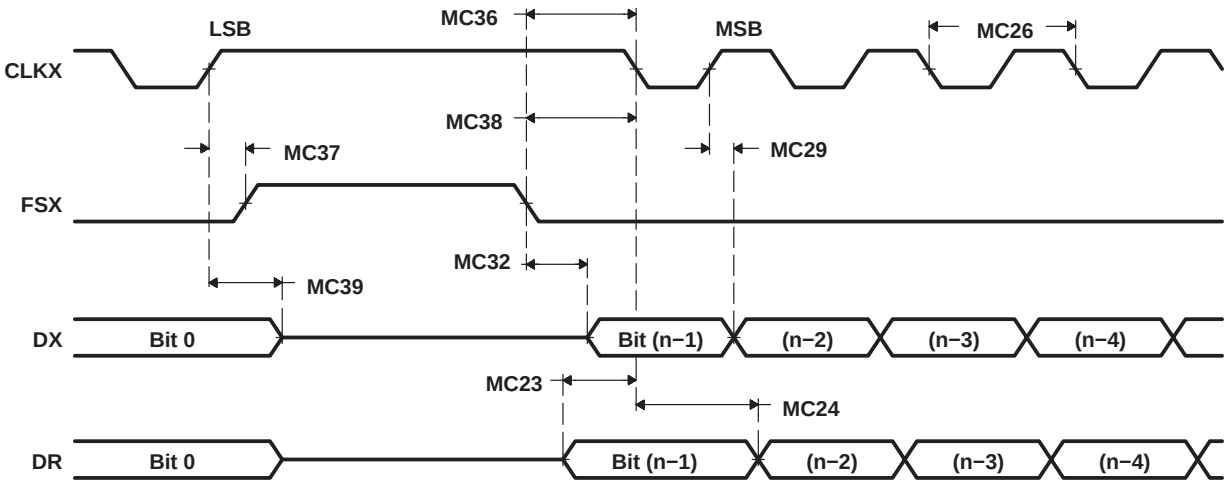



**Figure 5−29. McBSP Timings as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1**

### 5.14.4 McBSP General-Purpose I/O Timings

Table 5−35 and Table 5−36 assume testing over recommended operating conditions (see Figure 5−30).

**Table 5−35. McBSP General-Purpose I/O Timing Requirements**

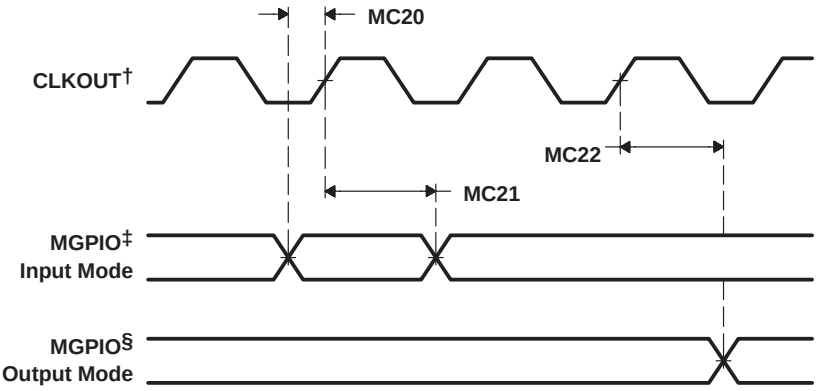
| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MC20 | $t_{su(MGPIO-COH)}$ | Setup time, MGPIOx input mode before CLKOUT high† | 7 | | 7 | | ns |
| MC21 | $t_{h(COH-MGPIO)}$ | Hold time, MGPIOx input mode after CLKOUT high† | 0 | | 0 | | ns |

† MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general-purpose input.

**Table 5−36. McBSP General-Purpose I/O Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MC22 | $t_{d(COH-MGPIO)}$ | Delay time, CLKOUT high to MGPIOx output mode‡ | 0 | 7 | 0 | 7 | ns |

‡ MGPIOx refers to CLKRx, FSRx, CLKXx, FSXx, or DXx when configured as a general-purpose output.




† CLKOUT reflects the CPU clock.
‡ MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general-purpose input.
§ MGPIOx refers to CLKRx, FSRx, CLKXx, FSXx, or DXx when configured as a general-purpose output.

**Figure 5−30. McBSP General-Purpose I/O Timings**

## 5.15 Enhanced Host-Port Interface (EHPI) Timings

Table 5−37 and Table 5−38 assume testing over recommended operating conditions (see Figure 5−31 through Figure 5−36).

**Table 5−37. EHPI Timing Requirements**

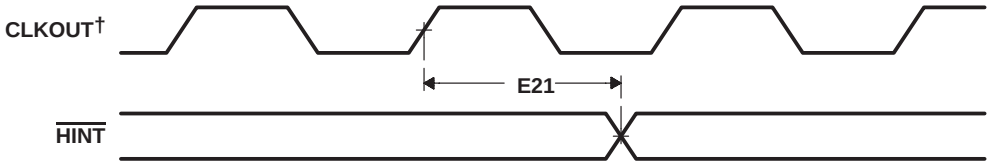
| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| E11 | $t_{su(HASL-HDSL)}$ | Setup time, $\overline{HAS}$ low before $\overline{HDS}$ low | 4 | | 4 | | ns |
| E12 | $t_{h(HDSL-HASL)}$ | Hold time, $\overline{HAS}$ low after $\overline{HDS}$ low | 3 | | 3 | | ns |
| E13 | $t_{su(HCNTLV-HDSL)}$ | Setup time, (HR/$\overline{W}$, HA[13:0], $\overline{HBE[1:0]}$, HCNTL[1:0]) valid before $\overline{HDS}$ low | 2 | | 2 | | ns |
| E14 | $t_{h(HDSL-HCNTLIV)}$ | Hold time, (HR/$\overline{W}$, HA[13:0], $\overline{HBE[1:0]}$, HCNTL[1:0]) invalid after $\overline{HDS}$ low | 4 | | 4 | | ns |
| E15 | $t_{w(HDSL)}$ | Pulse duration, $\overline{HDS}$ low | 4P† | | 4P† | | ns |
| E16 | $t_{w(HDSH)}$ | Pulse duration, $\overline{HDS}$ high | 4P† | | 4P† | | ns |
| E17 | $t_{su(HDV-HDSH)}$ | Setup time, HD bus write data valid before $\overline{HDS}$ high | 3 | | 3 | | ns |
| E18 | $t_{h(HDSH-HDIV)}$ | Hold time, HD bus write data invalid after $\overline{HDS}$ high | 4 | | 4 | | ns |
| E19 | $t_{su(HCNTLV-HASL)}$ | Setup time, (HR/$\overline{W}$, $\overline{HBE[1:0]}$, HCNTL[1:0]) valid before $\overline{HAS}$ low | 3 | | 3 | | ns |
| E20 | $t_{h(HASL-HCNTLIV)}$ | Hold time, (HR/$\overline{W}$, $\overline{HBE[1:0]}$, HCNTL[1:0]) valid after $\overline{HAS}$ low | 4 | | 4 | | ns |

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

**Table 5−38. EHPI Switching Characteristics**

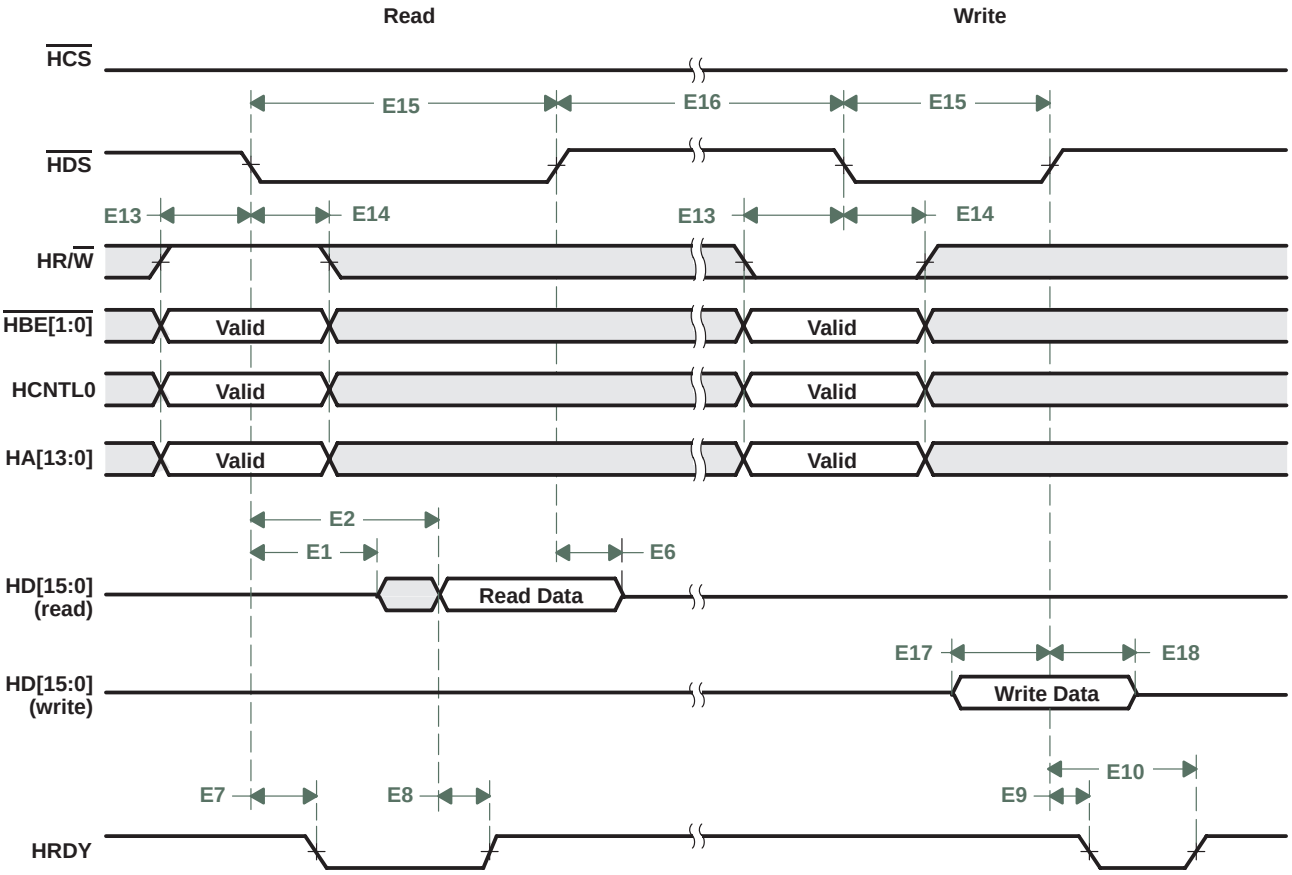
| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| E1 | $t_{en(HDSL-HDD)M}$ | Enable time, $\overline{HDS}$ low to HD bus enabled (memory access) | 6 | 26 | 6 | 19 | ns |
| E2 | $t_{d(HDSL-HDV)M}$ | Delay time, $\overline{HDS}$ low to HD bus read data valid (memory access) | 14P†‡ | | 14P†‡ | | ns |
| E4 | $t_{en(HDSL-HDD)R}$ | Enable time, $\overline{HDS}$ low to HD enabled (register access) | 6 | 26 | 6 | 19 | ns |
| E5 | $t_{d(HDSL-HDV)R}$ | Delay time, $\overline{HDS}$ low to HD bus read data valid (register access) | | 26 | | 19 | ns |
| E6 | $t_{dis(HDSH-HDIV)}$ | Disable time, $\overline{HDS}$ high to HD bus read data invalid | 6 | 26 | 6 | 19 | ns |
| E7 | $t_{d(HDSL-HRDYL)}$ | Delay time, $\overline{HDS}$ low to HRDY low (during reads) | | 18 | | 15 | ns |
| E8 | $t_{d(HDV-HRDYH)}$ | Delay time, HD bus valid to HRDY high (during reads) | 2 | | 2 | | ns |
| E9 | $t_{d(HDSH-HRDYL)}$ | Delay time, $\overline{HDS}$ high to HRDY low (during writes) | | 18 | | 15 | ns |
| E10 | $t_{d(HDSH-HRDYH)}$ | Delay time, $\overline{HDS}$ high to HRDY high (during writes) | 14P†‡ | | 14P†‡ | | ns |
| E21 | $t_{d(COH-HINT)}$ | Delay time, CLKOUT high to $\overline{HINT}$ high/low | 0 | 11 | 0 | 8 | ns |

† P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
‡ EHPI latency is dependent on the number of DMA channels active, their priorities and their source/destination ports. The latency shown assumes no competing CPU or DMA activity to the memory resource being accessed by the EHPI.




† CLKOUT reflects the CPU clock.

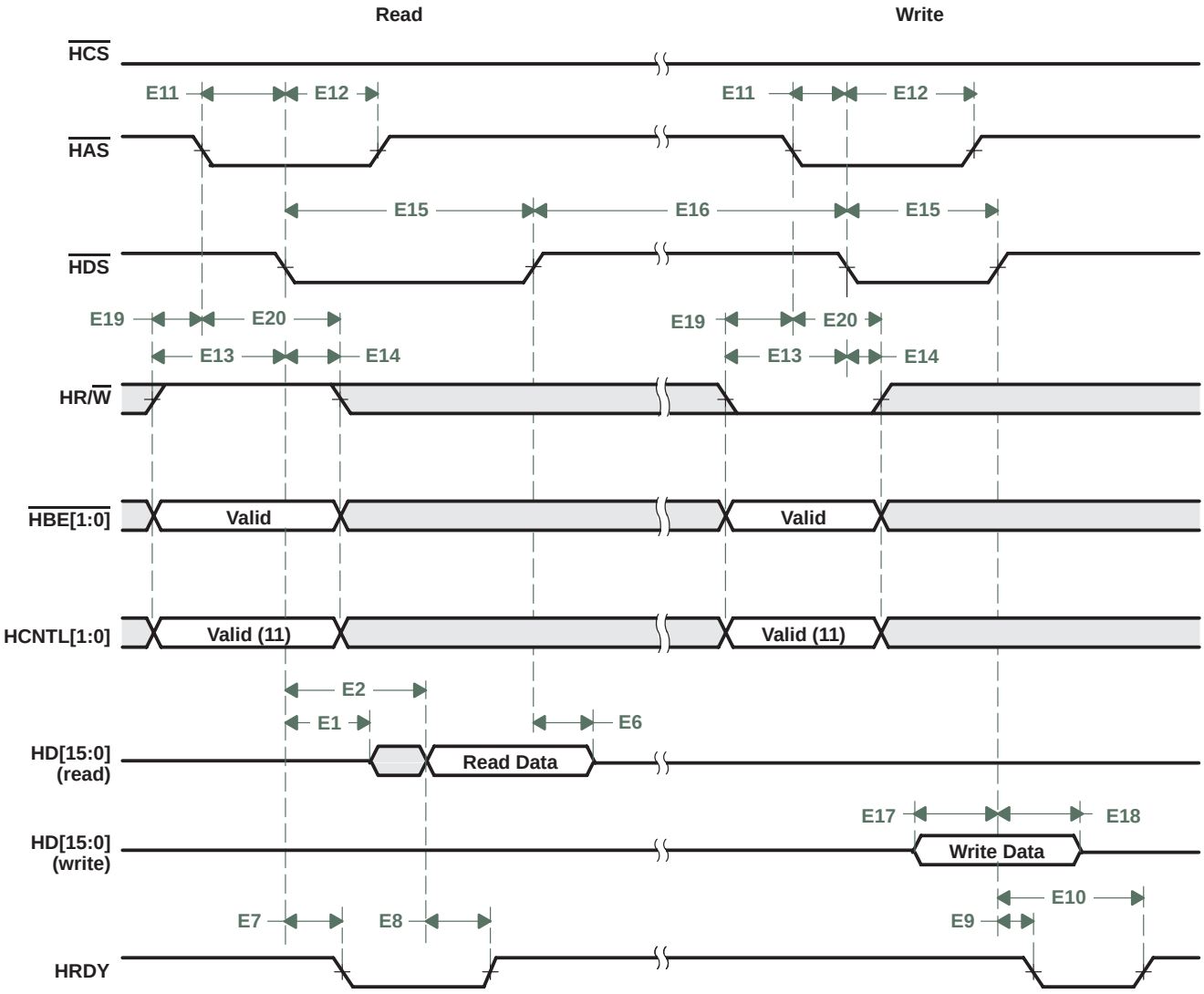
**Figure 5−31. HINT Timings**




NOTES: A. Any non-multiplexed access with HCNTL0 low will result in HPIC register access. For data read or write, HCNTL0 must stay high during the EHPI access.

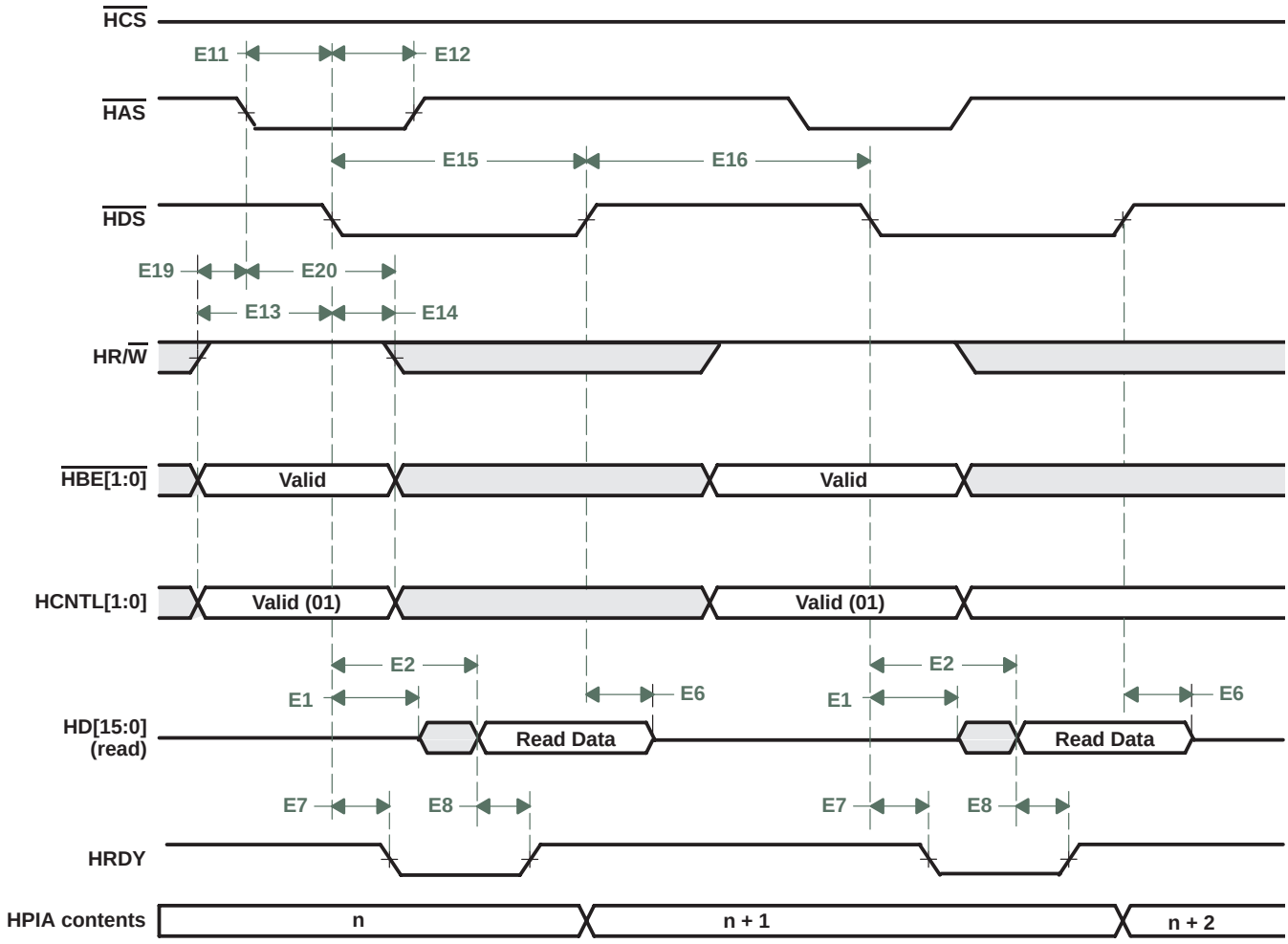
B. The falling edge of HCS must occur concurrent with or before the falling edge of HDS. The rising edge of HCS must occur concurrent with or after the rising edge of HDS. If HDS1 and/or HDS2 are tied permanently active and HCS is used as a strobe, the timing requirements shown for HDS apply to HCS. HRDY is always driven to the same value as its internal state.

**Figure 5−32. EHPI Nonmultiplexed Read/Write Timings**




NOTE: The falling edge of HCS must occur concurrent with or before the falling edge of HDS. The rising edge of HCS must occur concurrent with or after the rising edge of HDS. If HDS1 and/or HDS2 are tied permanently active and HCS is used as a strobe, the timing requirements shown for HDS apply to HCS. HRDY is always driven to the same value as its internal state.

**Figure 5−33. EHPI Multiplexed Memory (HPID) Read/Write Timings Without Autoincrement**

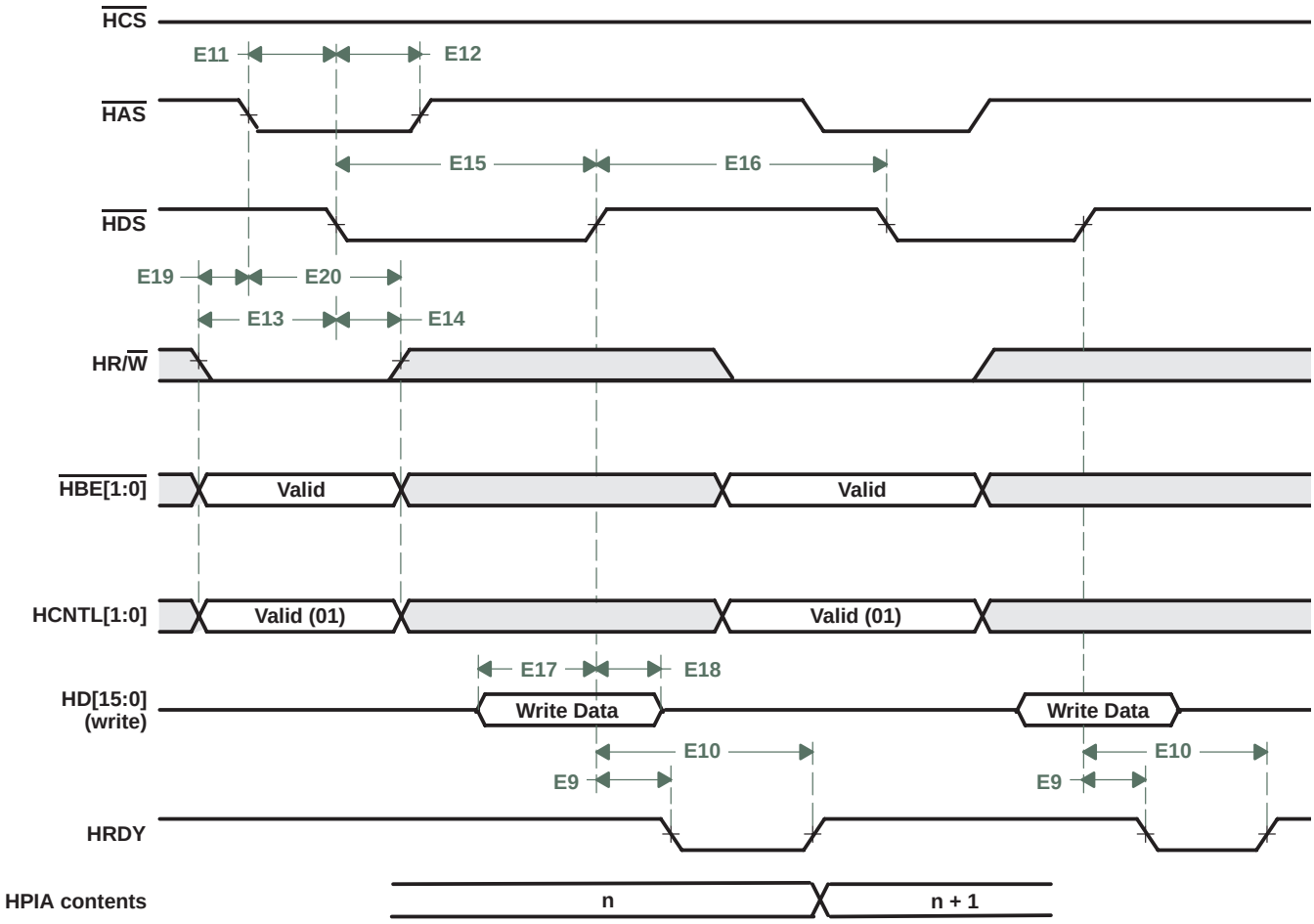



NOTES: A. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

B. In autoincrement mode, if HBE[1:0] are used to access the data as 8-bit-wide units, the HPIA increments only following each high byte (HBE1 low) access.

C. The falling edge of HCS must occur concurrent with or before the falling edge of HDS. The rising edge of HCS must occur concurrent with or after the rising edge of HDS. If HDS1 and/or HDS2 are tied permanently active and HCS is used as a strobe, the timing requirements shown for HDS apply to HCS. HRDY is always driven to the same value as its internal state.

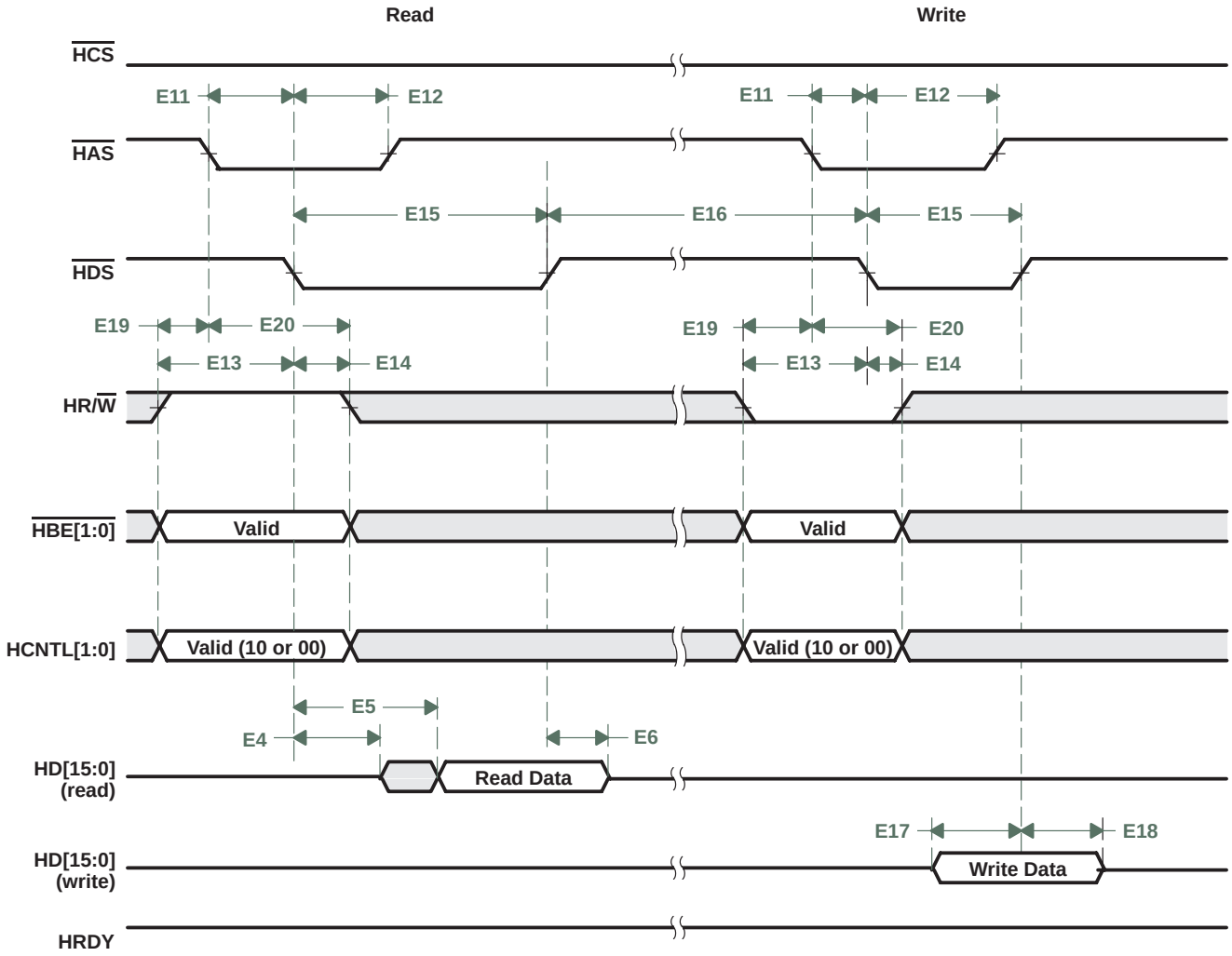
**Figure 5−34. EHPI Multiplexed Memory (HPID) Read Timings With Autoincrement**




NOTES: A. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

B. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied permanently active and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. HRDY is always driven to the same value as its internal state.

**Figure 5−35. EHPI Multiplexed Memory (HPID) Write Timings With Autoincrement**




NOTES: A. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.

B. The falling edge of HCS must occur concurrent with or before the falling edge of HDS. The rising edge of HCS must occur concurrent with or after the rising edge of HDS. If HDS1 and/or HDS2 are tied permanently active and HCS is used as a strobe, the timing requirements shown for HDS apply to HCS. HRDY is always driven to the same value as its internal state.

**Figure 5−36. EHPI Multiplexed Register Read/Write Timings**

## 5.16 I²C Timings

Table 5−39 and Table 5−40 assume testing over recommended operating conditions (see Figure 5−37 and Figure 5−38).

**Table 5−39. I²C Signals (SDA and SCL) Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| IC1 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | 10 | | 2.5 | | µs |
| IC2 | $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low for a repeated START condition | 4.7 | | 0.6 | | 4.7 | | 0.6 | | µs |
| IC3 | $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low for a START and a repeated START condition | 4 | | 0.6 | | 4 | | 0.6 | | µs |
| IC4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | 4.7 | | 1.3 | | µs |
| IC5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | 4 | | 0.6 | | µs |
| IC6 | $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100† | | 250 | | 100† | | ns |
| IC7 | $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low | 0‡ | | 0‡ | 0.9§ | 0‡ | | 0‡ | 0.9§ | µs |
| IC8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | 4.7 | | 1.3 | | µs |
| IC9 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | 20 + 0.1$C_b$¶ | 300 | | 1000 | 20 + 0.1$C_b$¶ | 300 | ns |
| IC10 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | 20 + 0.1$C_b$¶ | 300 | | 1000 | 20 + 0.1$C_b$¶ | 300 | ns |
| IC11 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | 20 + 0.1$C_b$¶ | 300 | | 300 | 20 + 0.1$C_b$¶ | 300 | ns |
| IC12 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | 20 + 0.1$C_b$¶ | 300 | | 300 | 20 + 0.1$C_b$¶ | 300 | ns |
| IC13 | $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4.0 | | 0.6 | | 4.0 | | 0.6 | | µs |
| IC14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | | | 0 | 50 | ns |
| IC15 | $C_b$¶ | Capacitive load for each bus line | | 400 | | 400 | | 400 | | 400 | pF |

† A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.

‡ A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

§ The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period [$t_{w(SCLL)}$] of the SCL signal.

¶ $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

I²C Bus is a trademark of Koninklijke Philips Electronics N.V.

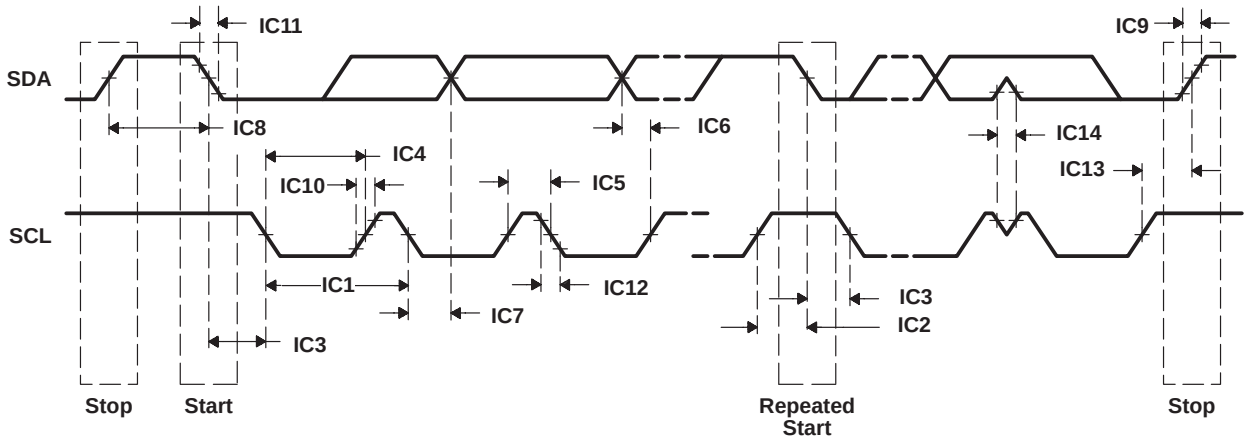



**Figure 5−37. $I^2C$ Receive Timings**

**Table 5−40. I²C Signals (SDA and SCL) Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | | $CV_{DD}$ = 1.6 V | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | STANDARD MODE | | FAST MODE | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| IC16 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | 10 | | 2.5 | | µs |
| IC17 | $t_{d(SCLH-SDAL)}$ | Delay time, SCL high to SDA low for a repeated START condition | 4.7 | | 0.6 | | 4.7 | | 0.6 | | µs |
| IC18 | $t_{d(SDAL-SCLL)}$ | Delay time, SDA low to SCL low for a START and a repeated START condition | 4 | | 0.6 | | 4 | | 0.6 | | µs |
| IC19 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | 4.7 | | 1.3 | | µs |
| IC20 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | 4 | | 0.6 | | µs |
| IC21 | $t_{d(SDA-SCLH)}$ | Delay time, SDA valid to SCL high | 250 | | 100 | | 250 | | 100 | | ns |
| IC22 | $t_{v(SCLL-SDAV)}$ | Valid time, SDA valid after SCL low | 0 | | 0 | 0.9 | 0 | | 0 | 0.9 | µs |
| IC23 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | 4.7 | | 1.3 | | µs |
| IC24 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | $20 + 0.1C_b$† | 300 | | 1000 | $20 + 0.1C_b$† | 300 | ns |
| IC25 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | $20 + 0.1C_b$† | 300 | | 1000 | $20 + 0.1C_b$† | 300 | ns |
| IC26 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | $20 + 0.1C_b$† | 300 | | 300 | $20 + 0.1C_b$† | 300 | ns |
| IC27 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | $20 + 0.1C_b$† | 300 | | 300 | $20 + 0.1C_b$† | 300 | ns |
| IC28 | $t_{d(SCLH-SDAH)}$ | Delay time, SCL high to SDA high for a STOP condition | 4 | | 0.6 | | 4 | | 0.6 | | µs |
| IC29 | $C_p$ | Capacitance for each I²C pin | | 10 | | 10 | | 10 | | 10 | pF |

† $C_b$ = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

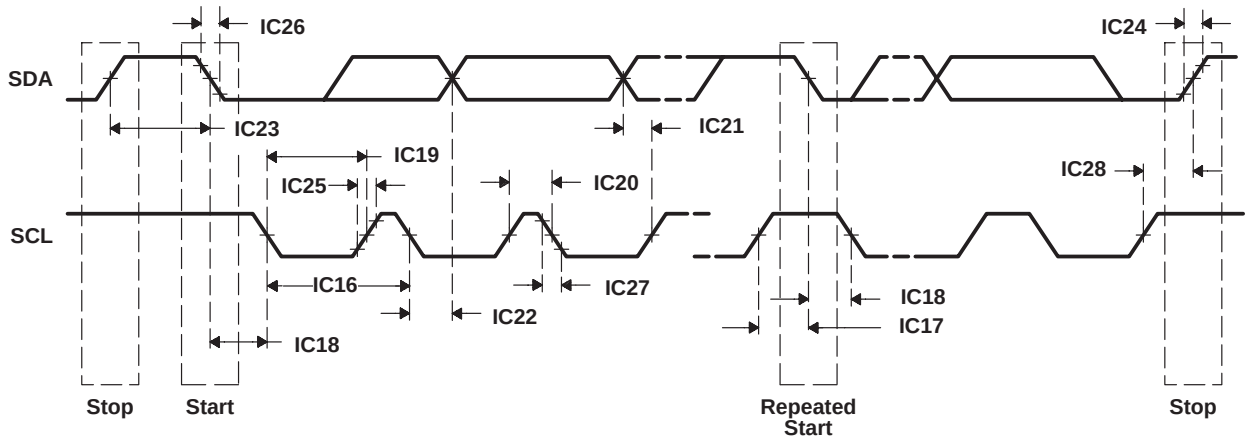



**Figure 5−38. I²C Transmit Timings**

## 5.17 MultiMedia Card (MMC) Timings

Table 5−41 and Table 5−42 assume testing over recommended operating conditions (see Figure 5−39).

**Table 5−41. MultiMedia Card (MMC) Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MMC7 | $t_{su(DV-CLKH)}$ | Setup time, data valid before clock high | 9 | | 6 | | ns |
| MMC8 | $t_{h(CLKH-DV)}$ | Hold time, data valid after clock high | 0 | | 0 | | ns |

**Table 5−42. MultiMedia Card (MMC) Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| MMC1 | $f_{(PP)}$ | Clock frequency data transfer mode (PP) ($C_L$ = 100 pF) | | 17.2† | | 19.2† | MHz |
| MMC2 | $f_{(OD)}$ | Clock frequency identification mode (OD) | | 400 | | 400 | kHz |
| MMC3 | $t_{w(CLKL)}$ | Clock low time ($C_L$ = 100 pF) | 10 | | 10 | | ns |
| MMC4 | $t_{w(CLKH)}$ | Clock high time ($C_L$ = 100 pF) | 10 | | 10 | | ns |
| MMC5 | $t_{r(CLK)}$ | Clock rise time ($C_L$ = 100 pF) | | 10 | | 10 | ns |
| MMC6 | $t_{f(CLK)}$ | Clock fall time ($C_L$ = 100 pF) | | 10 | | 10 | ns |
| MMC9 | $t_{d(CLKL-DV)}$ | Delay time, MMC.CLK low to data valid | −1 | 5 | −1 | 5 | ns |

† Maximum clock frequency specified in MMC Specification version 3.2 is 20 MHz. The 5509A can support clock frequency as high as 19.2 MHz.

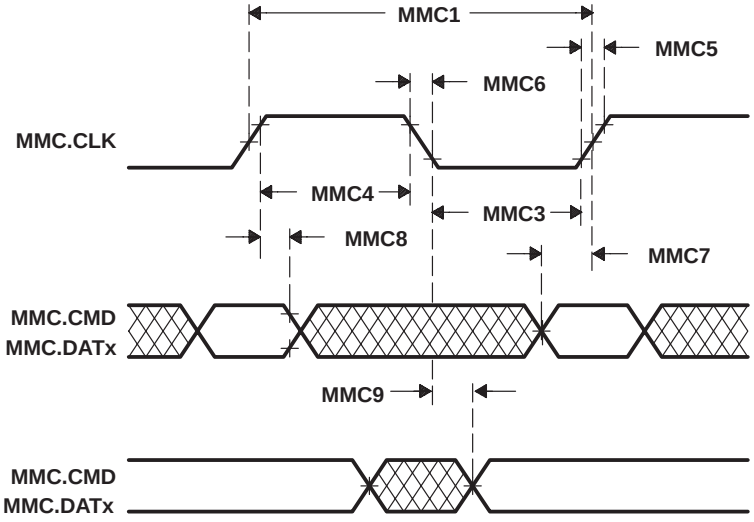



**Figure 5−39. MultiMedia Card (MMC) Timings**

## 5.18 Secure Digital (SD) Card Timings

Table 5−43 and Table 5−44 assume testing over recommended operating conditions (see Figure 5−40).

**Table 5−43. Secure Digital (SD) Card Timing Requirements**

| NO. | | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SD7 | $t_{su(DV-CLKH)}$ | Setup time, data valid before clock high | 9 | | 6 | | ns |
| SD8 | $t_{h(CLKH-DV)}$ | Hold time, data valid after clock high | 0 | | 0 | | ns |

**Table 5−44. Secure Digital (SD) Card Switching Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SD1 | $f_{(PP)}$ | Clock frequency data transfer mode (PP) ($C_L$ = 100 pF) | | 21† | | 25† | MHz |
| SD2 | $f_{(OD)}$ | Clock frequency identification mode (OD) | | 400 | | 400 | kHz |
| SD3 | $t_{w(CLKL)}$ | Clock low time ($C_L$ = 100 pF) | 10 | | 10 | | ns |
| SD4 | $t_{w(CLKH)}$ | Clock high time ($C_L$ = 100 pF) | 10 | | 10 | | ns |
| SD5 | $t_{r(CLK)}$ | Clock rise time ($C_L$ = 100 pF) | | 10 | | 10 | ns |
| SD6 | $t_{f(CLK)}$ | Clock fall time ($C_L$ = 100 pF) | | 10 | | 10 | ns |
| SD9 | $t_{d(CLKL-DV)}$ | Delay time, SD.CLK low to data valid | −1 | 5 | −1 | 5 | ns |

† Maximum clock frequency specified in the SD Specification is 25 MHz. The 5509A can support clock frequency as high as 21.0 MHz at core voltage = 1.2 V.

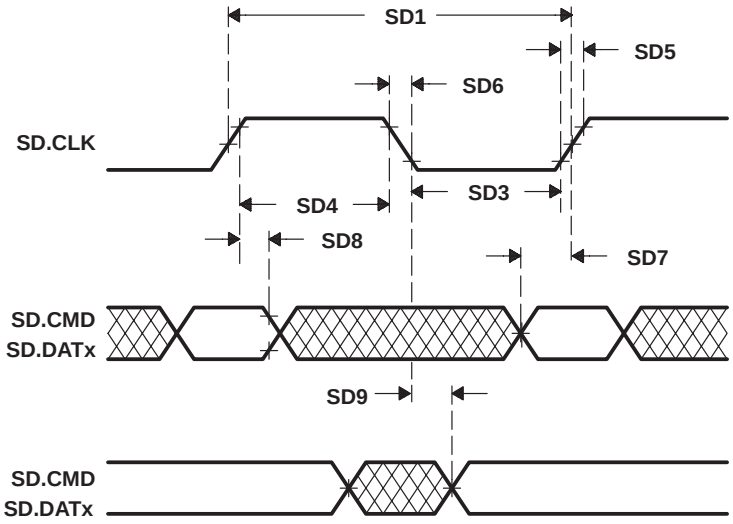



**Figure 5−40. Secure Digital (SD) Timings**

## 5.19 Universal Serial Bus (USB) Timings

Table 5−45 assumes testing over recommended operating conditions (see Figure 5−41 and Figure 5−42).

**Table 5−45. Universal Serial Bus (USB) Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | | $CV_{DD}$ = 1.6 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | FULL SPEED 12Mbps | | | FULL SPEED 12Mbps | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| U1 | $t_r$ | Rise time of DP and DN signals† | 4 | | 20 | 4 | | 20 | ns |
| U2 | $t_f$ | Fall time of DP and DN signals† | 4 | | 20 | 4 | | 20 | ns |
| | $t_{RFM}$ | Rise/Fall time matching‡ | 90 | | 111.11 | 90 | | 111.11 | % |
| | $V_{CRS}$ | Output signal cross-over voltage† | 1.3 | | 2.0 | 1.3 | | 2.0 | V |
| | $t_{jr}$ | Differential propagation jitter§¶ | −2 | | 2 | −2 | | 2 | ns |
| | $f_{op}$ | Operating frequency (Full speed mode) | | 12 | | | 12 | | Mb/s |
| U3 | $R_{S(DP)}$ | Series resistor | | 24 | | | 24 | | Ω |
| U4 | $R_{S(DN)}$ | Series resistor | | 24 | | | 24 | | Ω |
| U5 | $C_{edge(DP)}$ | Edge rate control capacitor | | 22 | | | 22 | | pF |
| U6 | $C_{edge(DN)}$ | Edge rate control capacitor | | 22 | | | 22 | | pF |

† $C_L$ = 50 pF
‡ $(t_r/t_f)$ x 100
§ $t_{px(1)} - t_{px(0)}$
¶ USB PLL is susceptible to power supply ripple, refer to recommend operating conditions for allowable supply ripple to meet the USB peak-to-peak jitter specification.

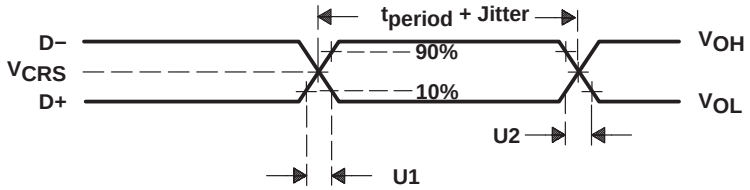
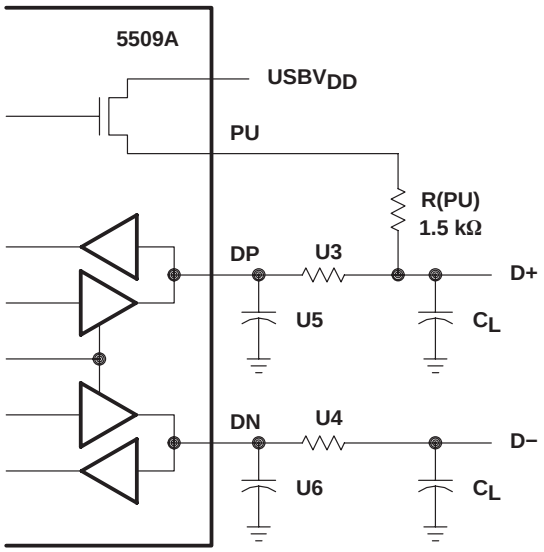



**Figure 5−41. USB Timings**




NOTES: A. A full-speed buffer is measured with the load shown.
B. $C_L$ = 50 pF

**Figure 5−42. Full-Speed Loads**

## 5.20 ADC Timings

Table 5−46 assumes testing over recommended operating conditions.

**Table 5−46. ADC Characteristics**

| NO. | PARAMETER | | $CV_{DD}$ = 1.2 V<br>$CV_{DD}$ = 1.35 V | | $CV_{DD}$ = 1.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| A1 | $t_{c(SCLC)}$ | Cycle time, ADC internal conversion clock | 500 | | 500 | | ns |
| A2 | $t_{d(AQ)}$ | Delay time, ADC sample and hold acquisition time | | 40 | | 40 | µs |
| A3 | $t_{d(CONV)}$ | Delay time, ADC conversion time | | 13 * $t_{c(SCLC)}$ | | 13 * $t_{c(SCLC)}$ | ns |
| A4 | $S_{DNL}$ | Static differential non-linearity error | | 2 | | 2 | LSB |
| | | Static integral non-linearity error | | 3 | | 3 | LSB |
| A5 | $Z_{set}$ | Zero-scale offset error | | 9 | | 9 | LSB |
| A6 | $F_{set}$ | Full-scale offset error | | 9 | | 9 | LSB |
| A7 | | Analog input impedance | 1 | | 1 | | MΩ |

# 6 Mechanical Data

## 6.1 Package Thermal Resistance Characteristics

Table 6−1 and Table 6−2 provide the estimated thermal resistance characteristics for the TMS320VC5509A DSP package types.

**Table 6−1. Thermal Resistance Characteristics (Ambient)**

| PACKAGE | $R_{\Theta JA}$ (°C/W) | BOARD TYPE† | AIRFLOW (LFM) |
|---|---|---|---|
| GHH, ZHH | 37.1 | High-K | 0 |
| | 35.1 | High-K | 150 |
| | 33.7 | High-K | 250 |
| | 32.2 | High-K | 500 |
| | 70.3 | Low-K | 0 |
| | 61.6 | Low-K | 150 |
| | 56.5 | Low-K | 250 |
| | 49.3 | Low-K | 500 |
| PGE | 71.2 | High-K | 0 |
| | 61.8 | High-K | 150 |
| | 58.9 | High-K | 250 |
| | 54.8 | High-K | 500 |
| | 103.6 | Low-K | 0 |
| | 84.2 | Low-K | 150 |
| | 77.8 | Low-K | 250 |
| | 69.4 | Low-K | 500 |

†Board types are as defined by JEDEC. Reference JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements.

**Table 6−2. Thermal Resistance Characteristics (Case)**

| PACKAGE | $R_{\Theta JC}$ (°C/W) | BOARD TYPE† |
|---|---|---|
| GHH, ZHH | 13.8 | 2s JEDEC Test Card |
| PGE | 13.8 | 2s JEDEC Test Card |

† Board types are as defined by JEDEC. Reference JEDEC Standard JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements.

## 6.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMS320VC5509AGBB | Active | Production | NFBGA (GBB) \| 179 | 160 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -40 to 85 | TMS320 VC5509AGBB |
| TMS320VC5509AGBB.A | Active | Production | NFBGA (GBB) \| 179 | 160 \| JEDEC TRAY (5+1) | No | SNPB | Level-3-220C-168 HR | -40 to 85 | TMS320 VC5509AGBB |
| TMS320VC5509AGBBR | Active | Production | NFBGA (GBB) \| 179 | 1000 \| LARGE T&R | No | SNPB | Level-3-220C-168 HR | -40 to 85 | TMS320 VC5509AGBB |
| TMS320VC5509AGBBR.A | Active | Production | NFBGA (GBB) \| 179 | 1000 \| LARGE T&R | No | SNPB | Level-3-220C-168 HR | -40 to 85 | TMS320 VC5509AGBB |
| TMS320VC5509APGE | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-4-260C-72 HR | -40 to 85 | VC5509APGE TMS320 |
| TMS320VC5509APGE.A | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-4-260C-72 HR | -40 to 85 | VC5509APGE TMS320 |
| TMS320VC5509APGEG4 | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-4-260C-72 HR | -40 to 85 | VC5509APGE TMS320 |
| TMS320VC5509APGEG4.A | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-4-260C-72 HR | -40 to 85 | VC5509APGE TMS320 |
| TMS320VC5509AZAY | Active | Production | NFBGA (ZAY) \| 179 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | TMS320 VC5509AZAY |
| TMS320VC5509AZAY.A | Active | Production | NFBGA (ZAY) \| 179 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | TMS320 VC5509AZAY |
| TMS320VC5509AZAYR | Active | Production | NFBGA (ZAY) \| 179 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | TMS320 VC5509AZAY |
| TMS320VC5509AZAYR.A | Active | Production | NFBGA (ZAY) \| 179 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | TMS320 VC5509AZAY |
| VC55GPSPGE | Active | Production | LQFP (PGE) \| 144 | 60 \| JEDEC TRAY (5+1) | Yes | NIPDAU | Level-4-260C-72 HR | -40 to 85 | VC5509APGE TMS320 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

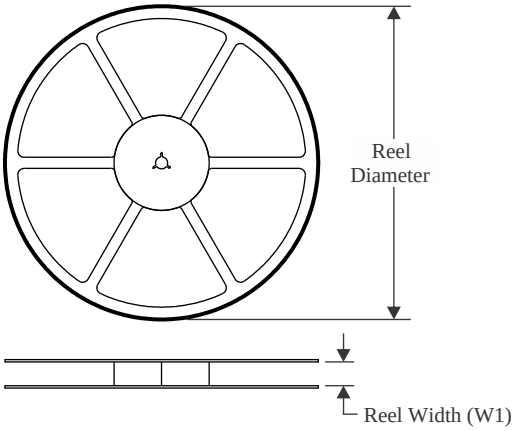
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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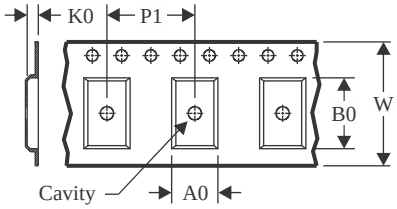
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

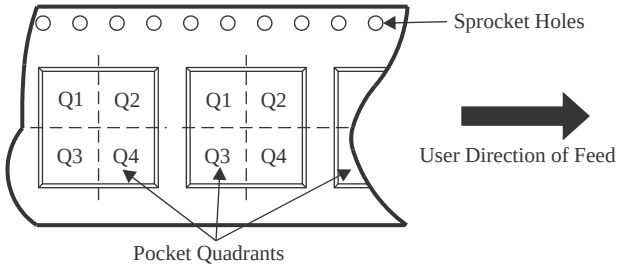



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

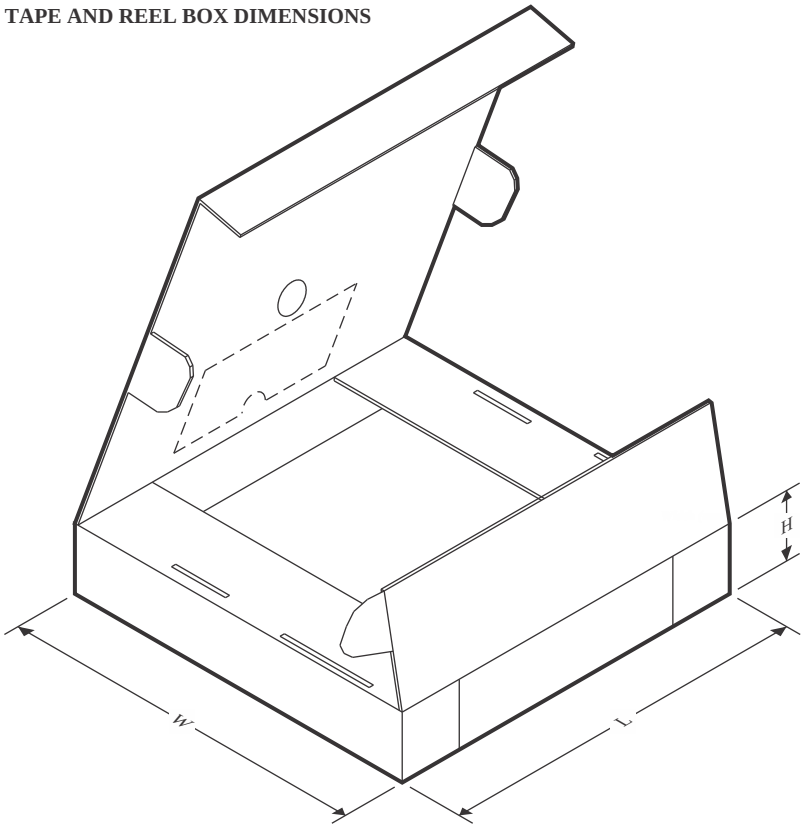
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320VC5509AGBBR | NFBGA | GBB | 179 | 1000 | 330.0 | 24.4 | 12.35 | 12.35 | 2.3 | 16.0 | 24.0 | Q1 |
| TMS320VC5509AZAYR | NFBGA | ZAY | 179 | 1000 | 330.0 | 24.4 | 12.35 | 12.35 | 2.3 | 16.0 | 24.0 | Q1 |

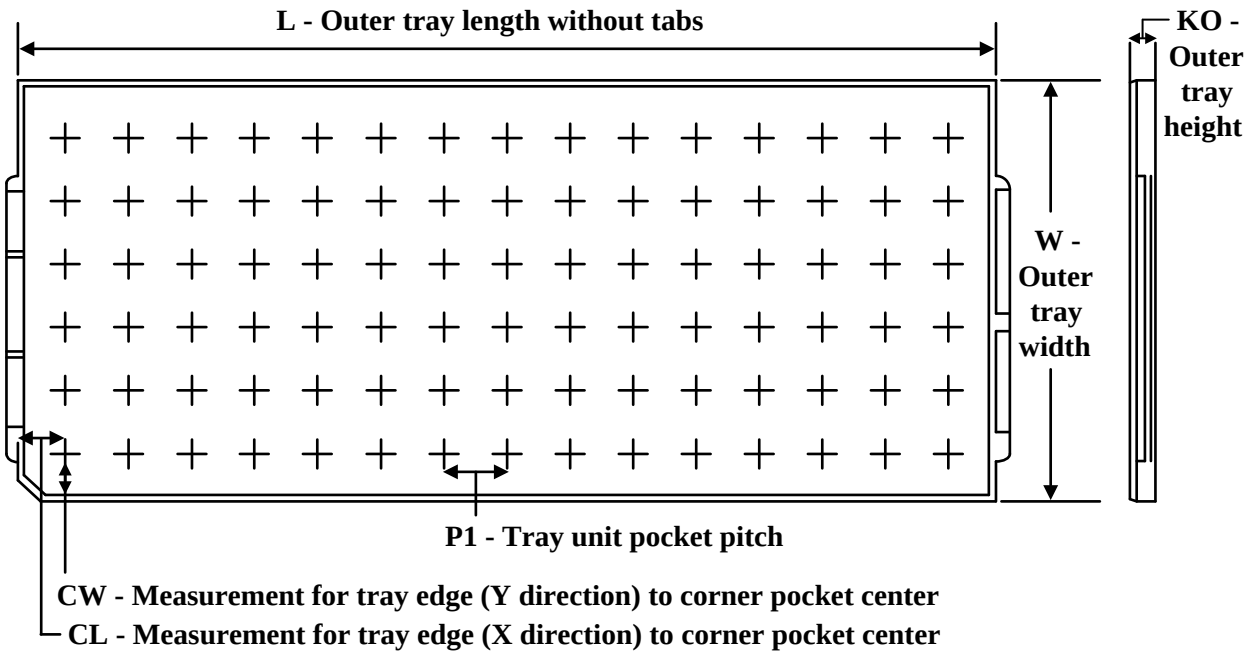
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMS320VC5509AGBBR | NFBGA | GBB | 179 | 1000 | 336.6 | 336.6 | 41.3 |
| TMS320VC5509AZAYR | NFBGA | ZAY | 179 | 1000 | 336.6 | 336.6 | 41.3 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

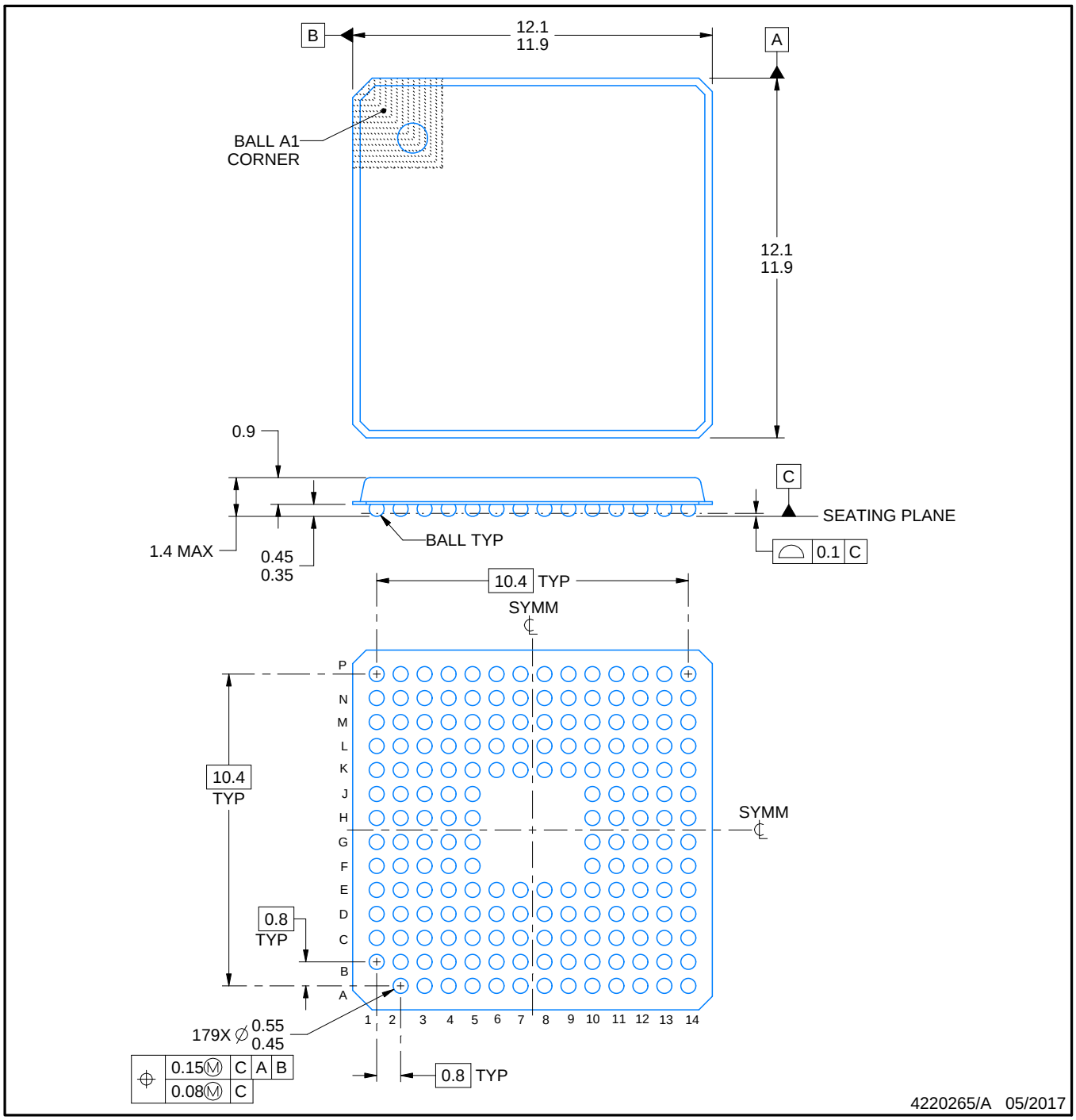
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMS320VC5509AGBB | GBB | NFBGA | 179 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| TMS320VC5509AGBB.A | GBB | NFBGA | 179 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| TMS320VC5509APGE | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS320VC5509APGE.A | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS320VC5509APGEG4 | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS320VC5509APGEG4.A | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| TMS320VC5509AZAY | ZAY | NFBGA | 179 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| TMS320VC5509AZAY.A | ZAY | NFBGA | 179 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| VC55GPSPGE | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |

# PACKAGE OUTLINE

## ZHH0179A

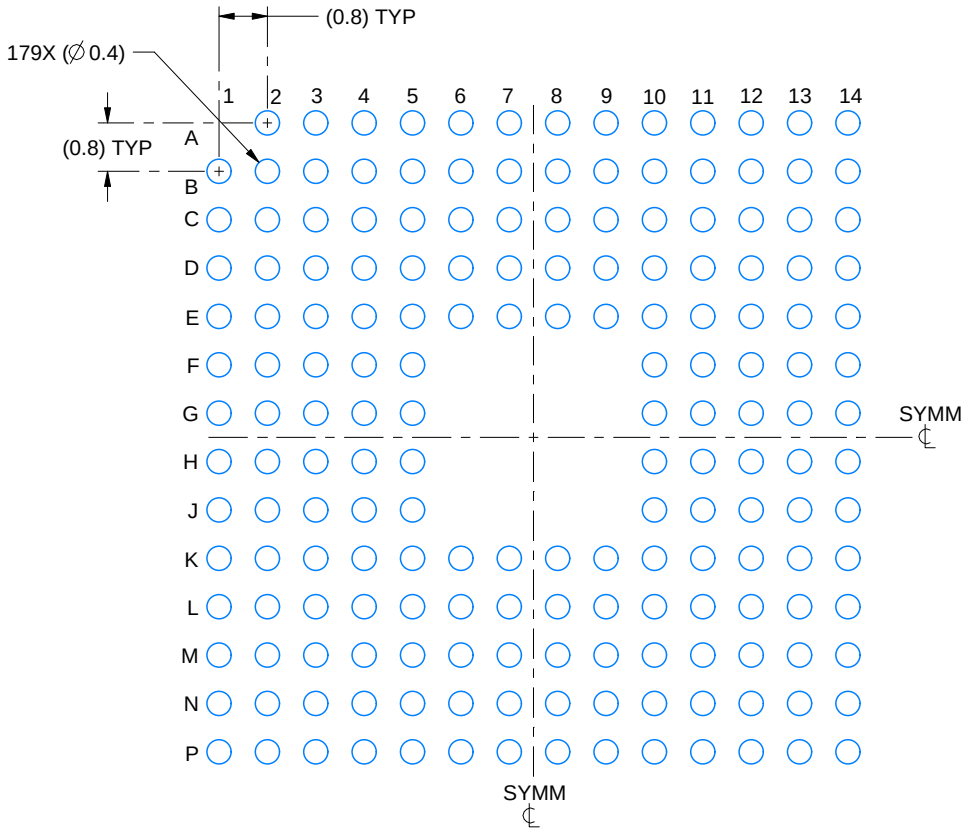
## UBGA - 1.4 mm max height

BALL GRID ARRAY

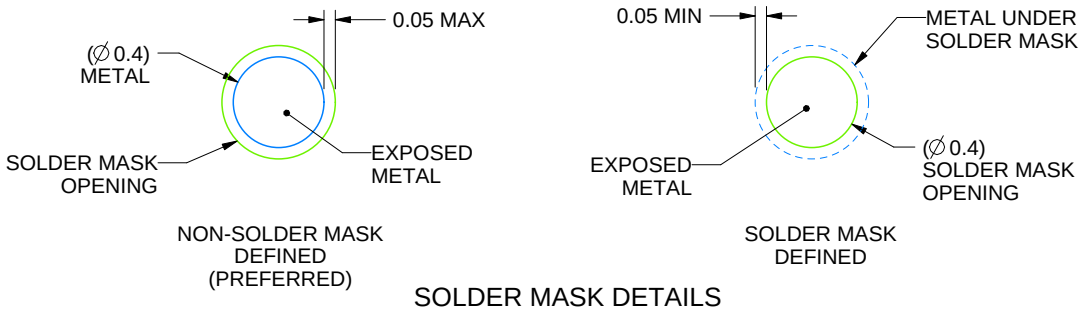



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X




SOLDER MASK DETAILS
NOT TO SCALE

4220265/A 05/2017

NOTES: (continued)

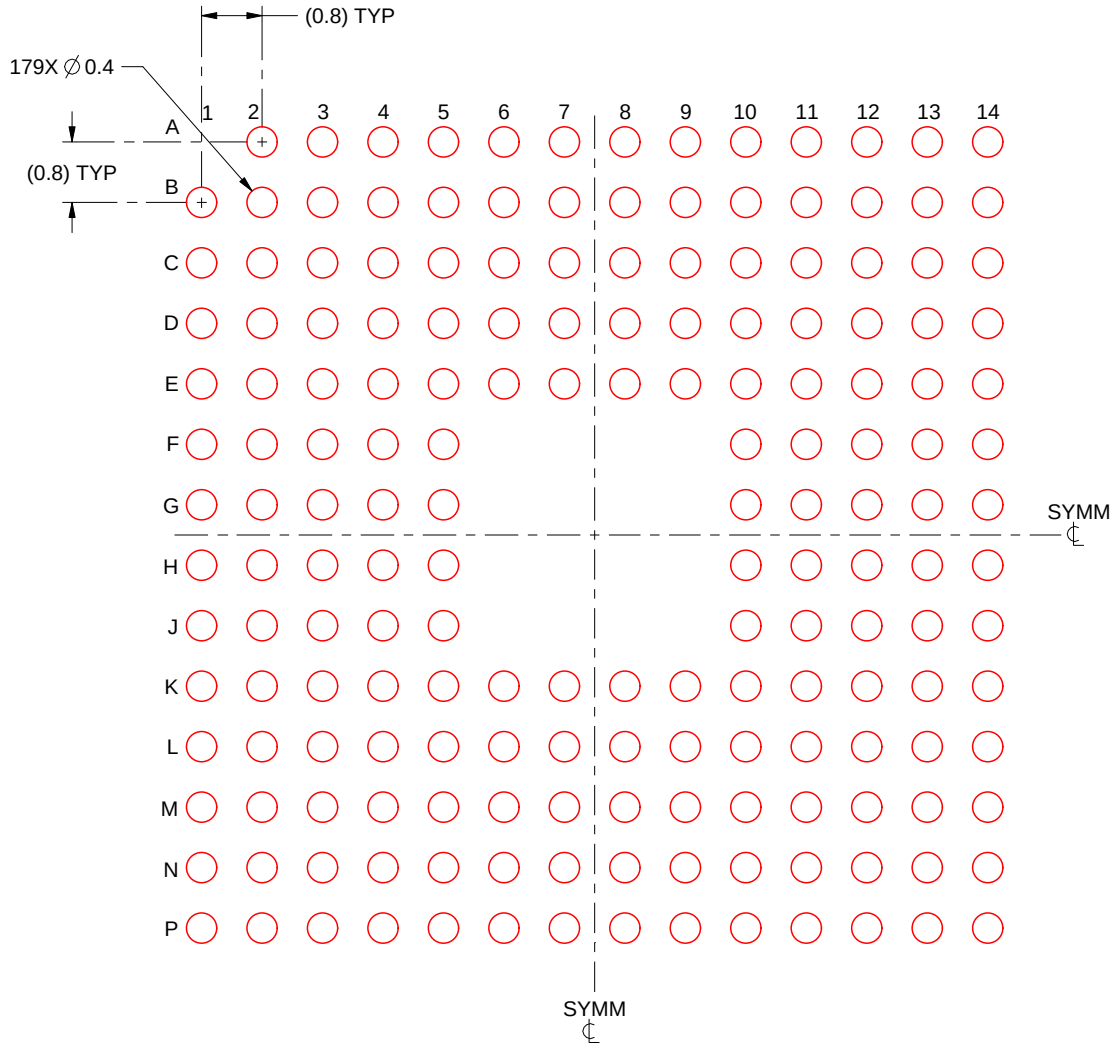
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SSZA002 (www.ti.com/lit/ssza002).

# EXAMPLE STENCIL DESIGN

## ZHH0179A

## UBGA - 1.4 mm max height

BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 10X

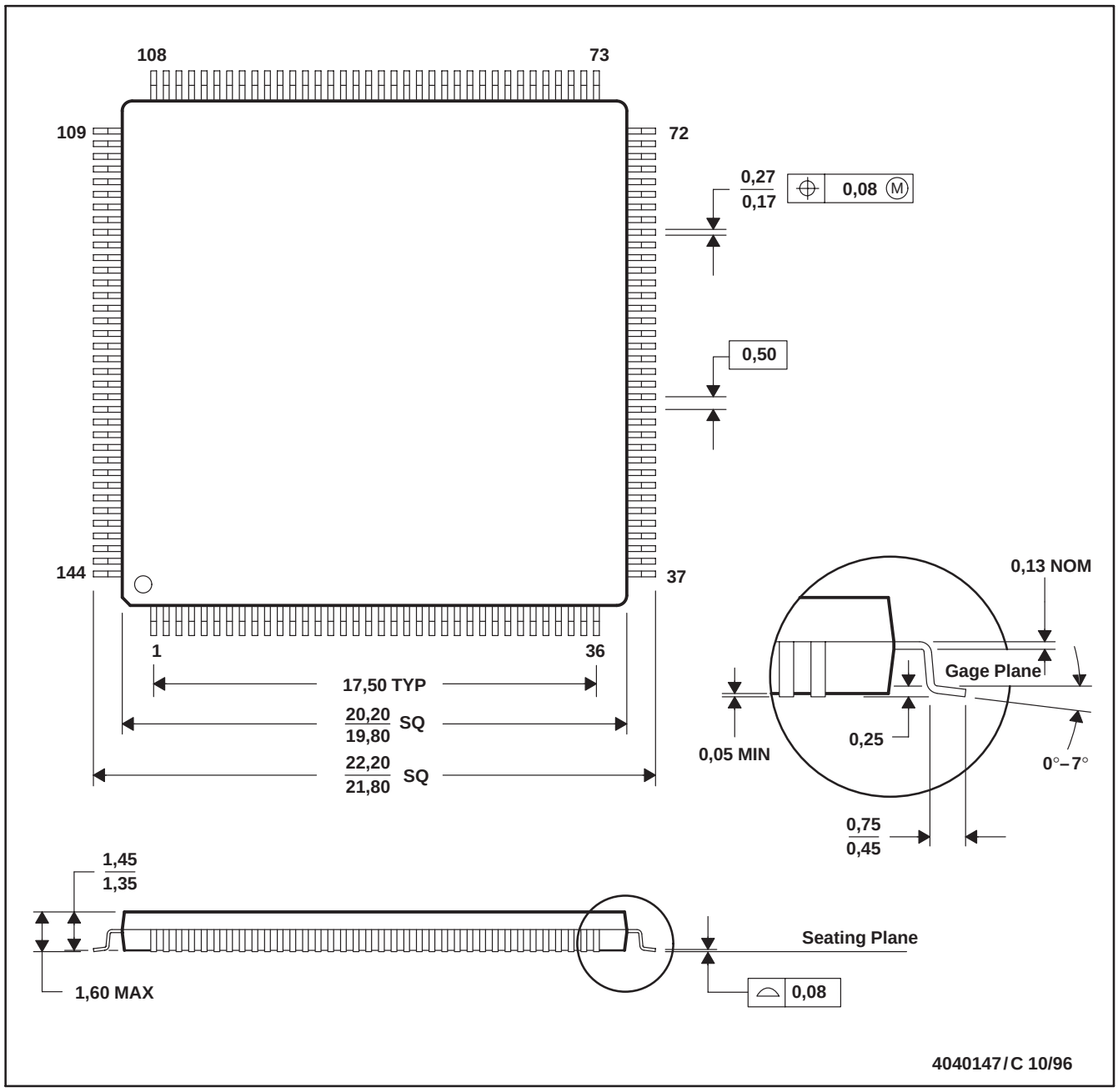
4220265/A 05/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

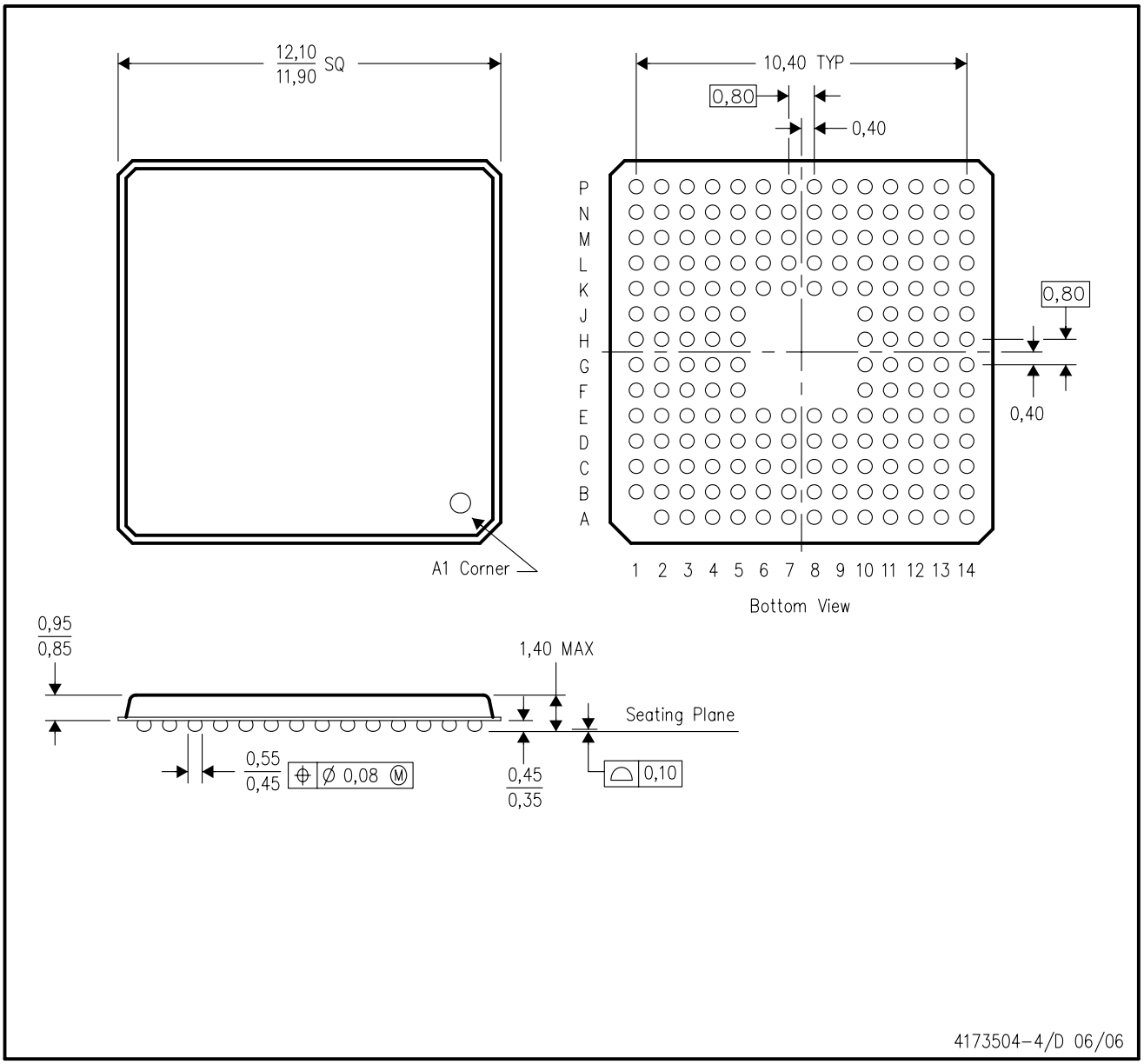
MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

**PGE (S-PQFP-G144)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

## GHH (S–PBGA–N179) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration

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