THE DATASHEET OF

TMS320DM355DZCE135

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TMS320DM355
Digital Media System-on-Chip (DMSoC)

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1 TMS320DM355 Digital Media System-on-Chip (DMSoC)

1.1 Features

- **Highlights**
  - **High-Performance Digital Media System-on-Chip (DMSoC)**
  - **Up to 270-MHz ARM926EJ-S™ Clock Rate**
  - **MPEG4/JPEG Coprocessor Supports**
    - **Up to 720p MPEG4 SP**
    - **Up to 50M Pixels per Second JPEG**
  - **Video Processing Subsystem**
    - **Hardware IPIPE for Real-Time Image Processing**
    - **Up to 14-bit CCD/CMOS Digital Interface**
    - **Histogram Module**
    - **Resize Image 1/16x to 8x**
    - **Hardware On-Screen Display**
    - **Supports digital HDTV (720p/1080i) output for connection to external encoder**
  - **Peripherals include DDR and mDDR SDRAM, 2 MMC/SD/SDIO and SmartMedia Flash Card Interfaces, USB 2.0, 3 UARTs and 3 SPIs**
  - **Configurable Power-Saving Modes**
  - **On-Chip ARM ROM Bootloader (RBL) to Boot From NAND Flash, MMC/SD, or UART**
  - **Extended Temperature 135- and 216-MHz Devices are Available**
  - **3.3-V and 1.8-V I/O, 1.3-V Core**
  - **Debug Interface Support**
  - **337-Pin Ball Grid Array at 65 nm Process Technology**
- **High-Performance Digital Media System-on-Chip (DMSoC)**
  - **135-, 216-, and 270-MHz ARM926EJ-S™ Clock Rate**
  - **Fully Software-Compatible With ARM9™**
  - **Extended temperature support for 135- and 216-MHz devices**
- **ARM926EJ-S Core**
  - **Support for 32-Bit and 16-Bit (Thumb Mode) Instruction Sets**
  - **DSP Instruction Extensions and Single Cycle MAC**
  - **ARM® Jazelle® Technology**
  - **EmbeddedICE-RT™ Logic for Real-Time Debug**
- **ARM9 Memory Architecture**
  - **16K-Byte Instruction Cache**
  - **8K-Byte Data Cache**
  - **32K-Byte RAM**
  - **8K-Byte ROM**
  - **Little Endian**
- **MPEG4/JPEG Coprocessor**
  - **Fixed Function Coprocessor Supports:**
    - **MPEG4 SP Codec at HD (720p), D1, VGA, SIF**
    - **JPEG Codec up to 50M Pixels per Second**
- **Video Processing Subsystem**
  - **Front End Provides:**
    - **Hardware IPIPE for Real-Time Image Processing**
    - **Up to 14-bit CCD/CMOS Digital Interface**
    - **16-/8-bit Generic YcBcR-4:2 Interface (BT.601)**
    - **10-/8-bit CCIR6565/BT655 Interface**
    - **Up to 75-MHz Pixel Clock**
    - **Histogram Module**
    - **Resize Engine**
      - **Resize Images From 1/16x to 8x**
      - **Separate Horizontal/Vertical Control**
      - **Two Simultaneous Output Paths**
  - **Back End Provides:**
    - **Hardware On-Screen Display (OSD)**
    - **Composite NTSC/PAL video encoder output**
    - **8-/16-bit YCC and Up to 18-Bit RGB666 Digital Output**
    - **BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface**
    - **Supports digital HDTV (720p/1080i) output for connection to external encoder**
- **External Memory Interfaces (EMIFs)**
  - **DDR2 and mDDR SDRAM 16-bit wide EMIF**

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With 256 MByte Address Space (1.8-V I/O)
  - Asynchronous16-/8-bit Wide EMIF (AEMIF)
    - Flash Memory Interfaces
      - NAND (8-/16-bit Wide Data)
      - OneNAND(16-bit Wide Data)
- Flash Card Interfaces
  - Two Multimedia Card (MMC) / Secure Digital (SD/SDIO)
  - SmartMedia
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- USB Port with Integrated 2.0 High-Speed PHY that Supports
  - USB 2.0 Full and High-Speed Device
  - USB 2.0 Low, Full, and High-Speed Host
- Three 64-Bit General-Purpose Timers (each configurable as two 32-bit timers)
- One 64-Bit Watch Dog Timer
- Three UARTs (One fast UART with RTS and CTS Flow Control)
- Three Serial Port Interfaces (SPI) each with two Chip-Selects
- One Master/Slave Inter-Integrated Circuit (I^2C) Bus®
- Two Audio Serial Port (ASP)
  - I2S and TDM I2S
  - AC97 Audio Codec Interface
  - S/PDIF via Software
  - Standard Voice Codec Interface (AIC12)
  - SPI Protocol (Master Mode Only)
- Four Pulse Width Modulator (PWM) Outputs
- Four RTO (Real Time Out) Outputs
- Up to 104 General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)
- On-Chip ARM ROM Bootloader (RBL) to Boot From NAND Flash (with SPI EEPROM Boot option), MMC/SD, or UART
- Configurable Power-Saving Modes
- Crystal or External Clock Input (typically 24 MHz or 36 MHz)
- Flexible PLL Clock Generators
- Debug Interface Support
  - IEEE-1149.1 (JTAG) Boundary-Scan-Compatible
  - ETB™ (Embedded Trace Buffer™) with 4K-Bytes Trace Buffer memory
  - Device Revision ID Readable by ARM
- 337-Pin Ball Grid Array (BGA) Package (ZCE Suffix), 0.65-mm Ball Pitch
- 90nm Process Technology
- 3.3-V and 1.8-V I/O, 1.3-V Internal
- Community Resources
  - TI E2E Community
  - TI Embedded Processors Wiki

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1.2 Description

The DM355 is a highly integrated, programmable platform for digital still camera, digital photo frames, IP security cameras, 4-channel digital video recorders, video door bell application, and other low cost portable digital video applications. Designed to offer portable video designers and manufacturers the ability to produce affordable portable digital video solutions with high picture quality, the DM355 combines high performance MPEG4 HD (720p) codecs and JPEG codecs up to 50M pixels per second, high quality, and low power consumption at a very low price point. The DM355 also enables seamless interface to most additional external devices required for a complete digital camera implementation. The interface is flexible enough to support various types of CCD and CMOS sensors, signal conditioning circuits, power management, DDR/mDDR memory, SRAM, NAND, shutter, Iris and auto-focus motor controls, etc.

The DM355 processor core is an ARM926EJ-S RISC processor. The ARM926EJ-S is a 32-bit processor core that performs 32-bit and 16-bit instructions and processes 32-bit, 16-bit, and 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously. The ARM core incorporates:

- A coprocessor 15 (CP15) and protection module
- Data and program Memory Management Units (MMUs) with table look-aside buffers.
- Separate 16K-byte instruction and 8K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT).

DM355 performance is enhanced by its MPEG4/JPEG coprocessor. The MPEG4/JPEG coprocessor performs the computational operations required for image processing; JPEG compression and MPEG4 video and imaging standard. The MPEG4/JPEG coprocessor supports MPEG4 SP at HD (720p), D1, VGA, SIF encode/decode resolutions and JPEG encode/decode up to 50M pixels per second.

The DM355 device has a Video Processing Subsystem (VPSS) with two configurable video/imaging peripherals:

- A Video Processing Front-End (VPFE)
- A Video Processing Back-End (VPBE)

The VPFE port provides an interface for CCD/CMOS imager modules and video decoders. The VPBE provides hardware On Screen Display (OSD) support and composite NTSC/PAL and digital LCD output.

The DM355 peripheral set includes:

- An inter-integrated circuit (I2C) Bus interface
- Two audio serial ports (ASP)
- Three 64-bit general-purpose timers each configurable as two independent 32-bit timers
- A 64-bit watchdog timer
- Up to 104-pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals
- Three UARTs with hardware handshaking support on one UART
- Three serial port Interfaces (SPI)
- Four pulse width modulator (PWM) peripherals
- Four real time out (RTO) outputs
- Two Multi-Media Card / Secure Digital (MMC/SD/SDIO) interfaces
- Wireless interfaces (Bluetooth, WLAN, WUSB) through SDIO
- A USB 2.0 full and high-speed device and host interface
- Two external memory interfaces:
  - An asynchronous external memory interface (AEMIF) for slower memories/peripherals such as NAND and OneNAND,
  - A high speed synchronous memory interface for DDR2/mDDR.

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For software development support the DM355 has a complete set of ARM development tools which include: C compilers, assembly optimizers to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

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1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the DM355 device.

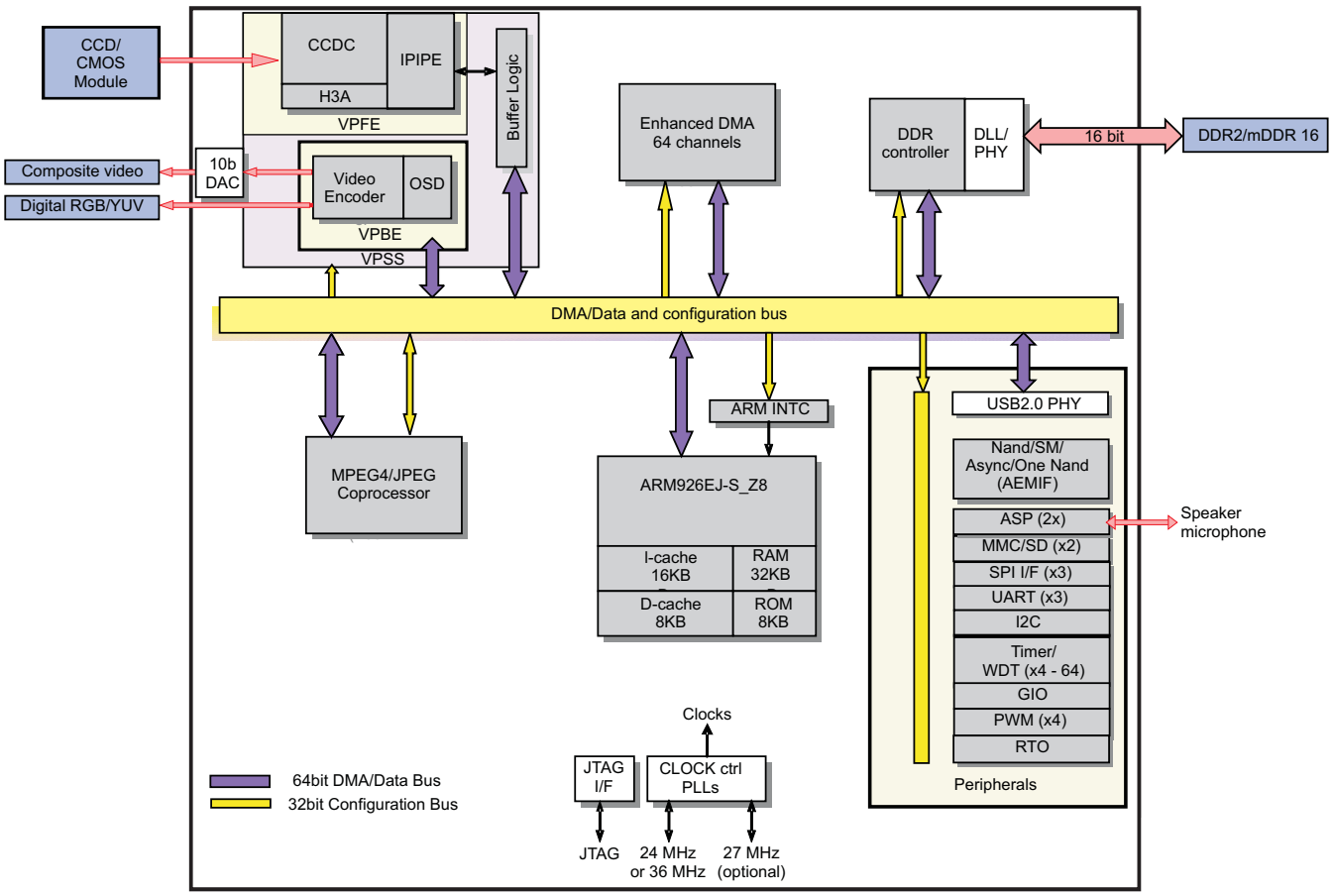

Figure 1-1. Functional Block Diagram

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data sheet revision history highlights the technical changes made to the SPRS463**F** device-specific data sheet to make it an SPRS463**G** revision.

Scope: Applicable updates to the DM35x DMSoC device family, specifically relating to the TMS320DM355 device, have been incorporated.

Note: DM355 27J supports 198MHz max DDR.

Revision G Updates

ADDS/CHANGES/DELETES	
Section 1.1	Changed Feature bullet from NAND Flash to NAND Flash (with SPI EEPROM Boot option).
Section 2.4	Table 2-9 and Table 2-11 • Added "Used to drive boot status LED signal (active low) in ROM boot modes." to pin number P16. • Deleted "Used to drive boot status LED signal (active low) in ROM boot modes." from pin number V19.
Section 2.21.2	Updated Figure 2-5, Device Nomenclature.
Section 2.20	Updated Table 2-23, changed Reset State values.
Section 3.2.4	Changed NAND to NAND (with SPI EEPROM Boot option).
Section 3.5	Table 3-4, Table 3-10, and Table 3-13: • Updated/Changed "(/2 or /1 programmable)" to "POSTDIV" and added "(/2 or /1 programmable)" to 2nd row
Section 3.5.4	• Added Section 3.5.4.1.3. • Added Section 3.5.4.2.3.
Table 3-21	Updated BTSEL Function and NAND configuration in table.
Table 3-22	Updated table: • Changed BTSEL[1:0] = 00 – Enable (NAND) to BTSEL[1:0] = 00 – Enable (NAND, SPI) Changed SPI0 Module State from SyncRst to: • BTSEL[1:0] = 00 – Enable (NAND, SPI) • BTSEL[1:0] = 01 – SyncRst (OneNAND) • BTSEL[1:0] = 10 – Enable (MMC/SD) • BTSEL[1:0] = 11 – Enable (UART)
Section 3.12	Added Section 3.12.2, "RBL NAND Boot Process" and associated Standard and Compatibility mode references throughout the document.
Section 3.12.1	Added ARM ROM Boot - SPI boot in NAND Mode bullet and sub-bullets.
Figure 3-6	Added SPI Flash to Diagram.
Section 4.2	Added last row to table including table note.
Section 4.3	Updated/Changed the following values in Section 4.3: • I_{OH} MAX value from "-100 µA" to "-4000 µA" • I_{OZ} TYP (IPU disabled) value from "±10 µA" to "±20 µA" • I_{OZ} TYP (IPU enabled) added value of ±100 µA" Added "Test Conditions" for I_{OH} and I_{OL} parameters
Table 5-5	Changed parameter 4 on table and added table note.
Table 5-6	Changed parameter 4 on table and added table note.
Table 5-45	Changed parameter 4 on table and added table note.
Section 5.7.1.3	Added table note to Table 5-14.

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2 Device Overview

2.1 Device Characteristics

Table 2-1 provides an overview of the DMSoC. The table shows significant features of the device, including the peripherals, capacity of on-chip RAM, ARM operating frequency, the package type with pin count, etc.

Table 2-1. Characteristics of the Processor

HARDWARE FEATURES		DM355
Peripherals Not all peripherals pins are available at the same time (For more detail, see the Device Configuration section).	DDR2 / mDDR Memory Controller	DDR2 / mDDR (16-bit bus width)
	Asynchronous EMIF (AEMIF)	Asynchronous (8/16-bit bus width) RAM, Flash (NAND, OneNAND)
	Flash Card Interfaces	Two MMC/SD One SmartMedia/xD
	EDMA	64 independent DMA channels Eight EDMA channels
	Timers	Three 64-Bit General Purpose (each configurable as two separate 32-bit timers) One 64-Bit Watch Dog
	UART	Three (one with RTS and CTS flow control)
	SPI	Three (each supports two slave devices)
	I^2C	One (Master/Slave)
	Audio Serial Port [ASP]	Two ASP
	General-Purpose Input/Output Port	Up to 104
	Pulse width modulator (PWM)	Four outputs
	Configurable Video Ports	One Input (VPFE) One Output (VPBE)
	USB 2.0	High, Full Speed Device High, Full, Low Speed Host
On-Chip CPU Memory	Organization	ARM 16-KB I-cache, 8-KB D-cache, 32-KB RAM, 8-KB ROM
JTAG BSDL_ID	JTAGID register (address location: 0x01C4 0028)	0x0B73B01F
CPU Frequency (Maximum)	MHz	ARM 135, 216 (1), and 270 MHz
Voltage	Core (V)	1.3 V
	I/O (V)	3.3 V, 1.8 V
PLL Options	Reference frequency options Configurable PLL controller	24 MHz (typical), 36 MHz PLL bypass, programmable PLL
BGA Package	13 x 13 mm	337-Pin BGA (ZCE)
Process Technology		90 nm
Product Status(2)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD

(1) Extended temperature supported for A216 and A135 devices.
(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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2.2 Memory Map Summary

Table 2-3 shows the memory map address ranges of the device. Table 2-3 depicts the expanded map of the Configuration Space (0x01C0 0000 through 0x01FF FFFF). The device has multiple on-chip memories associated with its processor and various subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters. The bus masters are the ARM, EDMA, USB, and VPSS.

Table 2-2. DM355 Memory Map

Start Address	End Address	Size (Bytes)	ARM Mem Map	EDMA Mem Map	USB Mem Map	VPSS Mem Map
0x0000 0000	0x0000 3FFF	16K	ARM RAM0 (Instruction)	Reserved	Reserved	Reserved
0x0000 4000	0x0000 7FFF	16K	ARM RAM1 (Instruction)			
0x0000 8000	0x0000 FFFF	32K	ARM ROM (Instruction) - only 8K used			
0x0001 0000	0x0001 3FFF	16K	ARM RAM0 (Data)	ARM RAM0	ARM RAM0	
0x0001 4000	0x0001 7FFF	16K	ARM RAM1 (Data)	ARM RAM1	ARM RAM1	
0x0001 8000	0x0001 FFFF	32K	ARM ROM (Data) - only 8K used	ARM ROM	ARM ROM	
0x0002 0000	0x000F FFFF	896K	Reserved	Reserved	Reserved	
0x0010 0000	0x01BB FFFF	26M				
0x01BC 0000	0x01BC 0FFF	4K	ARM ETB Mem			
0x01BC 1000	0x01BC 17FF	2K	ARM ETB Reg			
0x01BC 1800	0x01BC 18FF	256	ARM IceCrusher			
0x01BC 1900	0x01BC FFFF	59136	Reserved			
0x01BD 0000	0x01BF FFFF	192K				
0x01C0 0000	0x01FF FFFF	4M	CFG Bus Peripherals	CFG Bus Peripherals		
0x0200 0000	0x09FF FFFF	128M	ASYNC EMIF (Data)	ASYNC EMIF (Data)		
0x0A00 0000	0x11EF FFFF	127M - 16K	Reserved	Reserved		
0x11F0 0000	0x11F1 FFFF	128K				
0x11F2 0000	0x1FFF FFFF	141M-64K				
0x2000 0000	0x2000 7FFF	32K	DDR EMIF Control Regs	DDR EMIF Control Regs		
0x2000 8000	0x41FF FFFF	544M-32K	Reserved	Reserved		
0x4200 0000	0x49FF FFFF	128M		Reserved		
0x4A00 0000	0x7FFF FFFF	864M		Reserved		
0x8000 0000	0x8FFF FFFF	256M	DDR EMIF	DDR EMIF	DDR EMIF	DDR EMIF
0x9000 0000	0xFFFF FFFF	1792M	Reserved	Reserved	Reserved	Reserved

Table 2-3. DM355 ARM Configuration Bus Access to Peripherals

	Address			Accessibility	
Region	Start	End	Size	ARM	EDMA
EDMA CC	0x01C0 0000	0x01C0 FFFF	64K	√	√
EDMA TC0	0x01C1 0000	0x01C1 03FF	1K	√	√
EDMA TC1	0x01C1 0400	0x01C1 07FF	1K	√	√
Reserved	0x01C1 0800	0x01C1 9FFF	38K	√	√
Reserved	0x01C1 A000	0x01C1 FFFF	24K	√	√
UART0	0x01C2 0000	0x01C2 03FF	1K	√	√

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Table 2-3. DM355 ARM Configuration Bus Access to Peripherals (continued)

	Address			Accessibility	
UART1	0x01C2 0400	0x01C2 07FF	1K	√	√
Timer4/5	0x01C2 0800	0x01C2 0BFF	1K	√	√
Real-time out	0x01C2 0C00	0x01C2 0FFF	1K	√	√
I2C	0x01C2 1000	0x01C2 13FF	1K	√	√
Timer0/1	0x01C2 1400	0x01C2 17FF	1K	√	√
Timer2/3	0x01C2 1800	0x01C2 1BFF	1K	√	√
WatchDog Timer	0x01C2 1C00	0x01C2 1FFF	1K	√	√
PWM0	0x01C2 2000	0x01C2 23FF	1K	√	√
PWM1	0x01C2 2400	0x01C2 27FF	1K	√	√
PWM2	0x01C2 2800	0x01C2 2BFF	1K	√	√
PWM3	0x01C2 2C00	0x01C2 2FFF	1K	√	√
System Module	0x01C4 0000	0x01C4 07FF	2K	√	√
PLL Controller 0	0x01C4 0800	0x01C4 0BFF	1K	√	√
PLL Controller 1	0x01C4 0C00	0x01C4 0FFF	1K	√	√
Power/Sleep Controller	0x01C4 1000	0x01C4 1FFF	4K	√	√
Reserved	0x01C4 2000	0x01C4 7FFF	24K	√	√
ARM Interrupt Controller	0x01C4 8000	0x01C4 83FF	1K	√	√
Reserved	0x01C4 8400	0x01C6 3FFF	111K	√	√
USB OTG 2.0 Regs / RAM	0x01C6 4000	0x01C6 5FFF	8K	√	√
SPI0	0x01C6 6000	0x01C6 67FF	2K	√	√
SPI1	0x01C6 6800	0x01C6 6FFF	2K	√	√
GPIO	0x01C6 7000	0x01C6 77FF	2K	√	√
SPI2	0x01C6 7800	0x01C6 FFFF	2K	√	√
VPSS Subsystem	0x01C7 0000	0x01C7 FFFF	64K	√	√
VPSS Clock Control	0x01C7 0000	0x01C7 007F	128	√	√
Hardware 3A	0x01C7 0080	0x01C7 00FF	128	√	√
Image Pipe (IPIPE) Interface	0x01C7 0100	0x01C7 01FF	256	√	√
On Screen Display	0x01C7 0200	0x01C7 02FF	256	√	√
Reserved	0x01C7 0300	0x01C7 03FF	256	√	√
Video Encoder	0x01C7 0400	0x01C7 05FF	512	√	√
CCD Controller	0x01C7 0600	0x01C7 07FF	256	√	√
VPSS Buffer Logic	0x01C7 0800	0x01C7 08FF	256	√	√
Reserved	0x01C7 0900	0x01C7 09FF	256	√	√
Image Pipe (IPIPE)	0x01C7 1000	0x01C7 3FFF	12K	√	√
Reserved	0x01C7 4000	0x01CD FFFF	432K	√	√
Multimedia / SD 1	0x01E0 0000	0x01E0 1FFF	8K	√	√
ASP0	0x01E0 2000	0x01E0 3FFF	8K	√	√
ASP1	0x01E0 4000	0x01E0 5FFF	8K	√	√
UART2	0x01E0 6000	0x01E0 63FF	1K	√	√
Reserved	0x01E0 6400	0x01E0 FFFF	39K	√	√
ASYNC EMIF Control	0x01E1 0000	0x01E1 0FFF	4K	√	√
Multimedia / SD 0	0x01E1 1000	0x01E1 FFFF	60K	√	√
Reserved	0x01E2 0000	0x01FF FFFF	1792K	√	√
ASYNC EMIF Data (CE0)	0x0200 0000	0x03FF FFFF	32M	√	√
ASYNC EMIF Data (CE1)	0x0400 0000	0x05FF FFFF	32M	√	√
Reserved	0x0600 0000	0x09FF FFFF	64M	√	√
Reserved	0x0A00 0000	0x0BFF FFFF	32M	√	√

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Table 2-3. DM355 ARM Configuration Bus Access to Peripherals (continued)

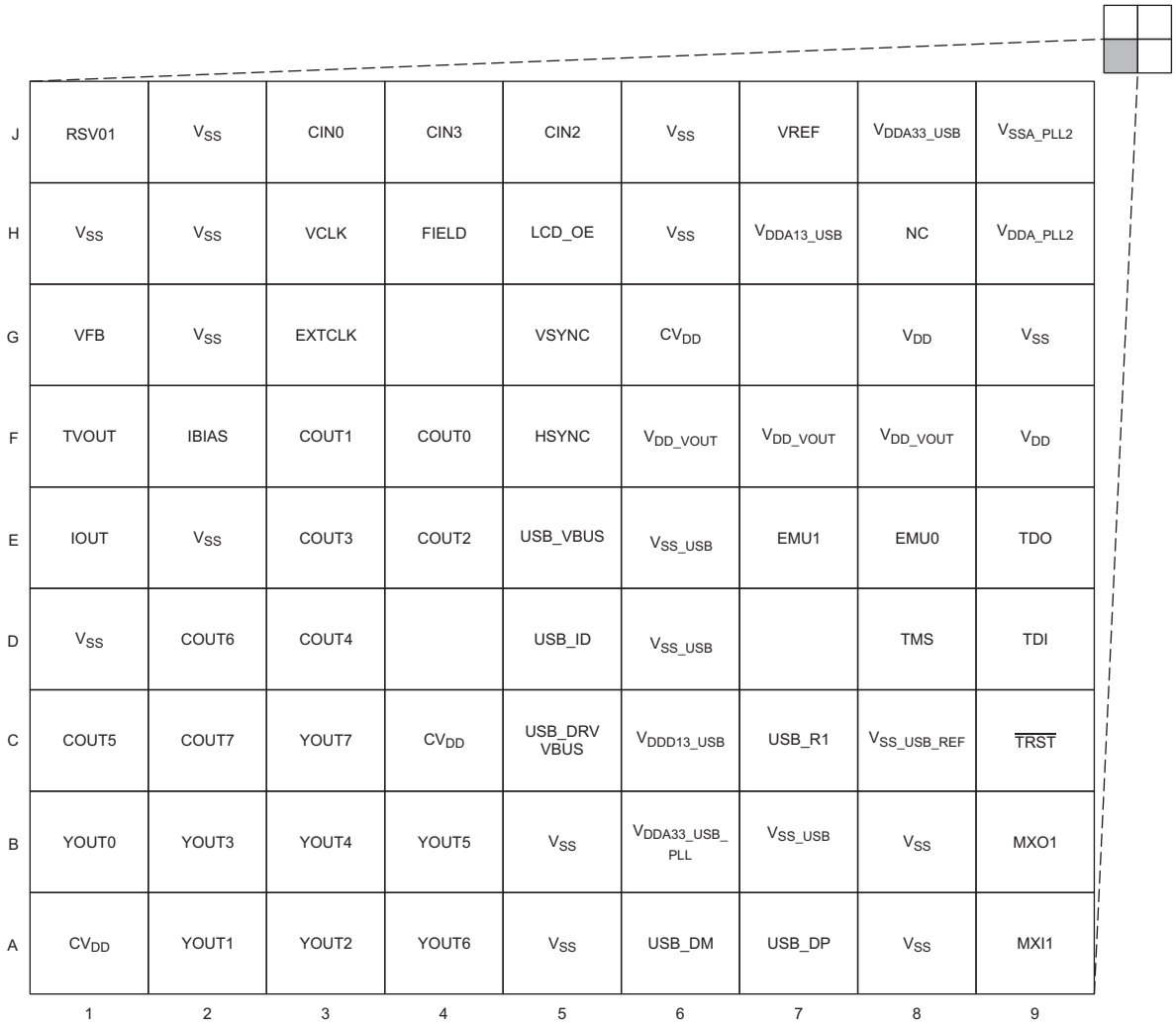
	Address			Accessibility	
Reserved	0x0C00 0000	0x0FFF FFFF	64M	√	√

2.3 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

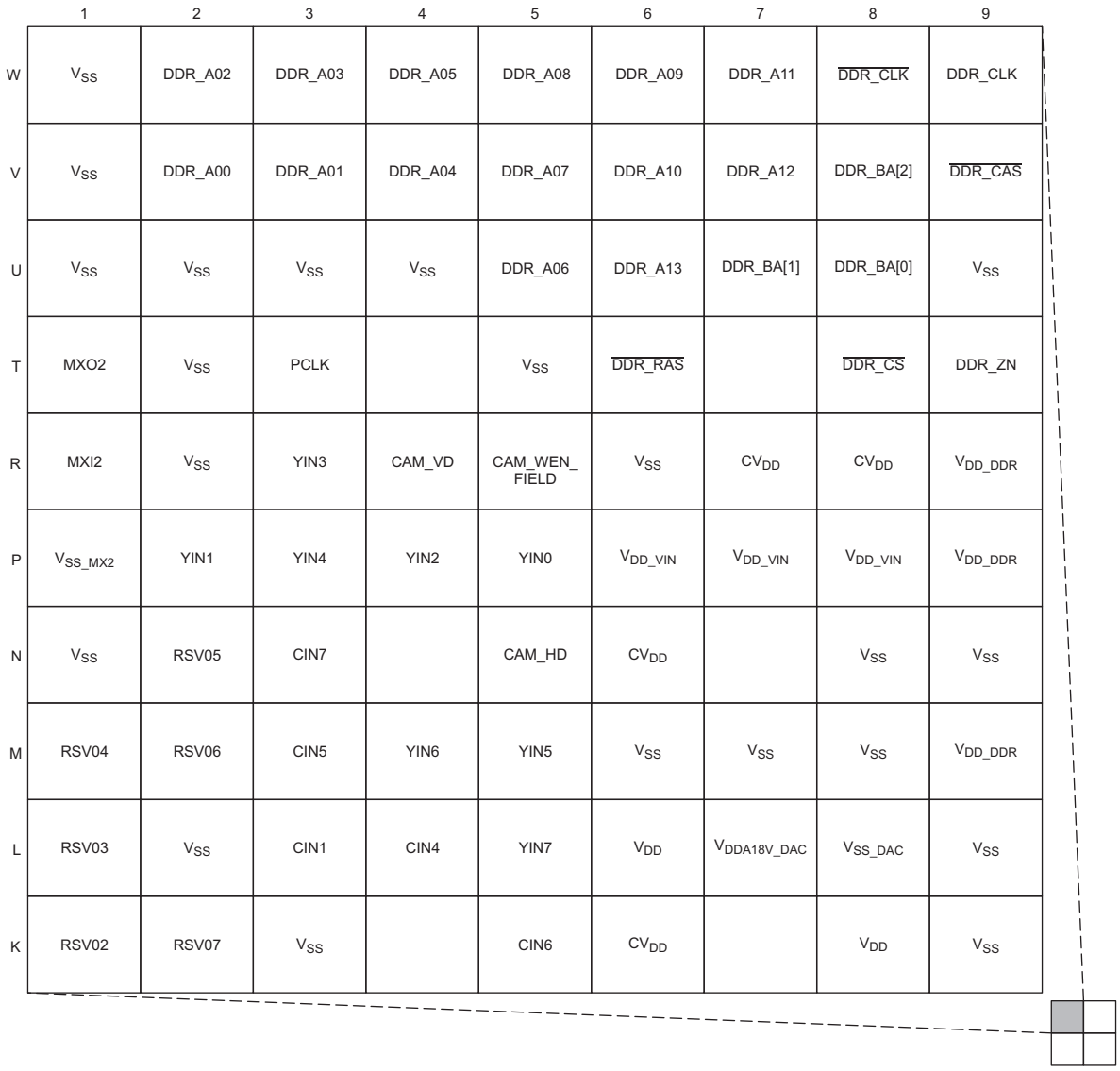
2.3.1 Pin Map (Bottom View)

Figure 2-1 through Figure 2-4 show the pin assignments in four quadrants (A, B, C, and D). Note that micro-vias are not required. Contact your TI representative for routing recommendations.



	1	2	3	4	5	6	7	8	9
J	RSV01	V_{SS}	CIN0	CIN3	CIN2	V_{SS}	VREF	V_{DDA33_USB}	V_{SSA_PLL2}
H	V_{SS}	V_{SS}	VCLK	FIELD	LCD_OE	V_{SS}	V_{DDA13_USB}	NC	V_{DDA_PLL2}
G	VFB	V_{SS}	EXTCLK		VSYNC	CV_{DD}		V_{DD}	V_{SS}
F	TVOUT	IBIAS	COUT1	COUT0	HSYNC	V_{DD_VOUT}	V_{DD_VOUT}	V_{DD_VOUT}	V_{DD}
E	IOUT	V_{SS}	COUT3	COUT2	USB_VBUS	V_{SS_USB}	EMU1	EMU0	TDO
D	V_{SS}	COUT6	COUT4		USB_ID	V_{SS_USB}		TMS	TDI
C	COUT5	COUT7	YOUT7	CV_{DD}	USB_DRV VBUS	V_{DDD13_USB}	USB_R1	$V_{SS_USB_REF}$	$\overline{TRST}$
B	YOUT0	YOUT3	YOUT4	YOUT5	V_{SS}	$V_{DDA33_USB_PLL}$	V_{SS_USB}	V_{SS}	MXO1
A	CV_{DD}	YOUT1	YOUT2	YOUT6	V_{SS}	USB_DM	USB_DP	V_{SS}	MXI1

Figure 2-1. Pin Map [Quadrant A]



	1	2	3	4	5	6	7	8	9
W	V_{SS}	DDR_A02	DDR_A03	DDR_A05	DDR_A08	DDR_A09	DDR_A11	$\overline{\text{DDR_CLK}}$	DDR_CLK
V	V_{SS}	DDR_A00	DDR_A01	DDR_A04	DDR_A07	DDR_A10	DDR_A12	DDR_BA[2]	$\overline{\text{DDR_CAS}}$
U	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DDR_A06	DDR_A13	DDR_BA[1]	DDR_BA[0]	V_{SS}
T	MXO2	V_{SS}	PCLK		V_{SS}	$\overline{\text{DDR_RAS}}$		$\overline{\text{DDR_CS}}$	DDR_ZN
R	MXI2	V_{SS}	YIN3	CAM_VD	CAM_WEN_ FIELD	V_{SS}	CV_{DD}	CV_{DD}	V_{DD_DDR}
P	V_{SS_MX2}	YIN1	YIN4	YIN2	YIN0	V_{DD_VIN}	V_{DD_VIN}	V_{DD_VIN}	V_{DD_DDR}
N	V_{SS}	RSV05	CIN7		CAM_HD	CV_{DD}		V_{SS}	V_{SS}
M	RSV04	RSV06	CIN5	YIN6	YIN5	V_{SS}	V_{SS}	V_{SS}	V_{DD_DDR}
L	RSV03	V_{SS}	CIN1	CIN4	YIN7	V_{DD}	V_{DDA18V_DAC}	V_{SS_DAC}	V_{SS}
K	RSV02	RSV07	V_{SS}		CIN6	CV_{DD}		V_{DD}	V_{SS}

Figure 2-2. Pin Map [Quadrant B]

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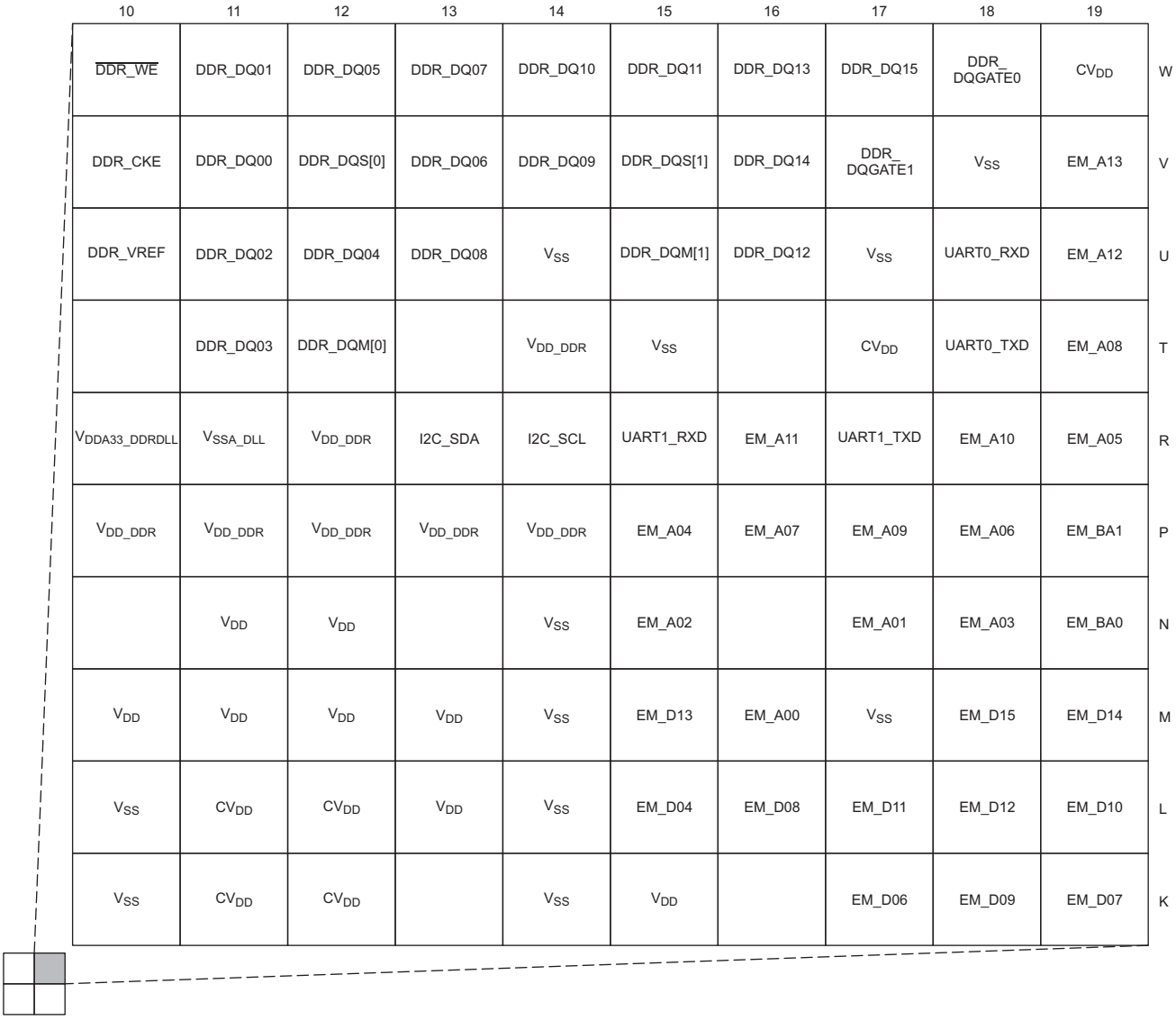

10	11	12	13	14	15	16	17	18	19	
$\overline{\text{DDR_WE}}$	DDR_DQ01	DDR_DQ05	DDR_DQ07	DDR_DQ10	DDR_DQ11	DDR_DQ13	DDR_DQ15	DDR_DQGATE0	CV_{DD}	W
DDR_CKE	DDR_DQ00	DDR_DQS[0]	DDR_DQ06	DDR_DQ09	DDR_DQS[1]	DDR_DQ14	DDR_DQGATE1	V_{SS}	EM_A13	V
DDR_VREF	DDR_DQ02	DDR_DQ04	DDR_DQ08	V_{SS}	DDR_DQM[1]	DDR_DQ12	V_{SS}	UART0_RXD	EM_A12	U
	DDR_DQ03	DDR_DQM[0]		V_{DD_DDR}	V_{SS}		CV_{DD}	UART0_TXD	EM_A08	T
V_{DDA33_DDRDLL}	V_{SSA_DLL}	V_{DD_DDR}	I2C_SDA	I2C_SCL	UART1_RXD	EM_A11	UART1_TXD	EM_A10	EM_A05	R
V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	EM_A04	EM_A07	EM_A09	EM_A06	EM_BA1	P
	V_{DD}	V_{DD}		V_{SS}	EM_A02		EM_A01	EM_A03	EM_BA0	N
V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	EM_D13	EM_A00	V_{SS}	EM_D15	EM_D14	M
V_{SS}	CV_{DD}	CV_{DD}	V_{DD}	V_{SS}	EM_D04	EM_D08	EM_D11	EM_D12	EM_D10	L
V_{SS}	CV_{DD}	CV_{DD}		V_{SS}	V_{DD}		EM_D06	EM_D09	EM_D07	K

Figure 2-3. Pin Map [Quadrant C]

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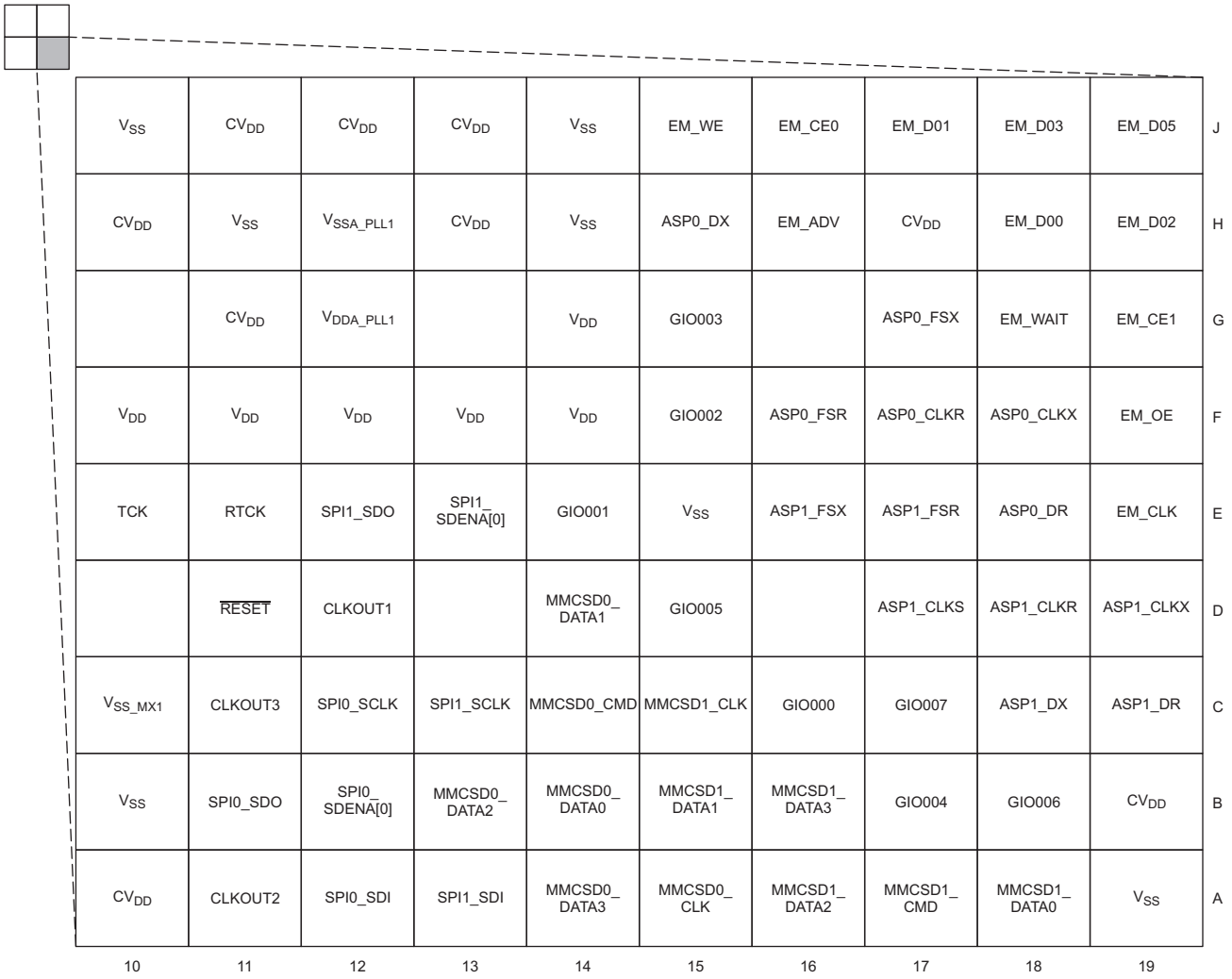

	10	11	12	13	14	15	16	17	18	19	
J	V_{SS}	CV_{DD}	CV_{DD}	CV_{DD}	V_{SS}	EM_WE	EM_CE0	EM_D01	EM_D03	EM_D05	J
H	CV_{DD}	V_{SS}	V_{SSA_PLL1}	CV_{DD}	V_{SS}	ASP0_DX	EM_ADV	CV_{DD}	EM_D00	EM_D02	H
G		CV_{DD}	V_{DDA_PLL1}		V_{DD}	GIO003		ASP0_FSX	EM_WAIT	EM_CE1	G
F	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GIO002	ASP0_FSR	ASP0_CLKR	ASP0_CLKX	EM_OE	F
E	TCK	RTCK	SPI1_SDO	SPI1_ SDENA[0]	GIO001	V_{SS}	ASP1_FSX	ASP1_FSR	ASP0_DR	EM_CLK	E
D		$\overline{\text{RESET}}$	CLKOUT1		MMCSD0_ DATA1	GIO005		ASP1_CLKS	ASP1_CLKR	ASP1_CLKX	D
C	V_{SS_MX1}	CLKOUT3	SPI0_SCLK	SPI1_SCLK	MMCSD0_CMD	MMCSD1_CLK	GIO000	GIO007	ASP1_DX	ASP1_DR	C
B	V_{SS}	SPI0_SDO	SPI0_ SDENA[0]	MMCSD0_ DATA2	MMCSD0_ DATA0	MMCSD1_ DATA1	MMCSD1_ DATA3	GIO004	GIO006	CV_{DD}	B
A	CV_{DD}	CLKOUT2	SPI0_SDI	SPI1_SDI	MMCSD0_ DATA3	MMCSD0_ CLK	MMCSD1_ DATA2	MMCSD1_ CMD	MMCSD1_ DATA0	V_{SS}	A

Figure 2-4. Pin Map [Quadrant D]

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2.4 Pin Functions

The pin functions tables (Table 2-4 through Table 2-22) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see Section 3. For the list of all pin in chronological order see Section 2.20

2.4.1 Image Data Input - Video Processing Front End

The CCD Controller module in the Video Processing Front End has an external signal interface for image data input. It supports YUV (YC) inputs as well as Bayer RGB and complementary input signals (I.e., image data input).

The definition of the CCD controller data input signals depend on the input mode selected.

- In 16-bit YCbCr mode, the Cb and Cr signals are multiplexed on the CI signals and the order is configurable (i.e., Cb first or Cr first).
- In 8-bit YCbCr mode, the Y, Cb, and Cr signals are multiplexed and not only is the order selectable, but also the half of the bus used.

Table 2-4. CCD Controller Signals for Each Input Mode

PIN NAME	CCD	16-BIT YCbCr	8-BIT YCbCr
CI7		Cb7,Cr7	Y7,Cb7,Cr7
CI6		Cb6,Cr6	Y6,Cb6,Cr6
CI5	CCD13	Cb5,Cr5	Y5,Cb5,Cr5
CI4	CCD12	Cb4,Cr4	Y4,Cb4,Cr4
CI3	CCD11	Cb3,Cr3	Y3,Cb3,Cr3
CI2	CCD10	Cb2,Cr2	Y2,Cb2,Cr2
CI1	CCD9	Cb1,Cr1	Y1,Cb1,Cr1
CI0	CCD8	Cb0,Cr0	Y0,Cb0,Cr0
YI7	CCD7	Y7	Y7,Cb7,Cr7
YI6	CCD6	Y6	Y6,Cb6,Cr6
YI5	CCD5	Y5	Y5,Cb5,Cr5
YI4	CCD4	Y4	Y4,Cb4,Cr4
YI3	CCD3	Y3	Y3,Cb3,Cr3
YI2	CCD2	Y2	Y2,Cb2,Cr2
YI1	CCD1	Y1	Y1,Cb1,Cr1
YI0	CCD0	Y0	Y0,Cb0,Cr0

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Table 2-5. CCD Controller/Video Input Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
CIN7/ GIO101/ SPI2_SCLK	N3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: NOT USED • YCC 16-bit: Time multiplexed between chroma: CB/CR[07] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] SPI: SPI2 Clock GIO: GIO[101]
CIN6/ GIO100/ SPI2_SDO	K5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: NOT USED • YCC 16-bit: Time multiplexed between chroma: CB/CR[06] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[06] SPI: SPI2 Data Out GIO: GIO[100]
CIN5/ GIO099/ SPI2_SDENA[0]	M3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[13] • YCC 16-bit: Time multiplexed between chroma: CB/CR[05] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[05] SPI: SPI2 Chip Select GIO: GIO[099]
CIN4/ GIO098/ SPI2_SDENA[1]	L4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[12] • YCC 16-bit: Time multiplexed between chroma: CB/CR[04] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[04] SPI: SPI2 Data In GIO: GIO[098]
CIN3/ GIO097/	J4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[11] • YCC 16-bit: Time multiplexed between chroma: CB/CR[03] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[03] GIO: GIO[097]
CIN2/ GIO096/	J5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[10] • YCC 16-bit: Time multiplexed between chroma: CB/CR[02] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[02] GIO: GIO[097]
CIN1/ GIO095/	L3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[09] • YCC 16-bit: Time multiplexed between chroma: CB/CR[01] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[01] GIO: GIO[095]
CIN0/ GIO094/	J3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[08] • YCC 16-bit: Time multiplexed between chroma: CB/CR[00] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[00] GIO: GIO[094]
YIN7/ GIO093	L5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[07] • YCC 16-bit: Time multiplexed between chroma: Y[07] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] GIO: GIO[093]
YIN6/ GIO092	M4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[06] • YCC 16-bit: Time multiplexed between chroma: Y[06] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[06] GIO: GIO[092]

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) PD = internal pull-down, PU = internal pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)
(3) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.

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Table 2-5. CCD Controller/Video Input Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
YIN5/ GIO091	M5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[05] • YCC 16-bit: Time multiplexed between chroma: Y[05] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[05] GIO: GIO[091]
YIN4/ GIO090	P3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[04] • YCC 16-bit: Time multiplexed between chroma: Y[04] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[04] GIO: GIO[090]
YIN3/ GIO089	R3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[03] • YCC 16-bit: Time multiplexed between chroma: Y[03] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[03] GIO: GIO[089]
YIN2/ GIO088	P4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[02] • YCC 16-bit: Time multiplexed between chroma: Y[02] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[02] GIO: GIO[088]
YIN1/ GIO087	P2	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[01] • YCC 16-bit: Time multiplexed between chroma: Y[01] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[01] GIO: GIO[087]
YIN0/ GIO086	P5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[00] • YCC 16-bit: Time multiplexed between chroma: Y[00] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[00] GIO: GIO[086]
CAM_HD/ GIO085	N5	I/O/Z	PD V_{DD_VIN}	Horizontal synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new line starts. GIO: GIO[085]
CAM_VD GIO084	R4	I/O/Z	PD V_{DD_VIN}	Vertical synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new frame starts. GIO: GIO[084]
CAM_WEN _FIELD\ GIO083	R5	I/O/Z	PD V_{DD_VIN}	Write enable input signal is used by external device (AFE/TG) to gate the DDR output of the CCDC module. Alternately, the field identification input signal is used by external device (AFE/TG) to indicate which of two frames is input to the CCDC module for sensors with interlaced output. CCDC handles 1- or 2-field sensors in hardware. GIO: GIO[083]
PCLK/ GIO082	T3	I/O/Z	PD V_{DD_VIN}	Pixel clock input (strobe for lines C17 through Y10) GIO: GIO[0082]

2.5 Image Data Output - Video Processing Back End (VPBE)

The Video Encoder/Digital LCD interface module in the video processing back end has an external signal interface for digital image data output as described in Table 2-7 and Table 2-8.

The digital image data output signals support multiple functions / interfaces, depending on the display mode selected. The following table describes these modes. Parallel RGB mode with more than RGB565 signals requires enabling pin multiplexing to support (i.e., for RGB666 mode).

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Table 2-6. Signals for VPBE Display Modes

PIN NAME	YCC16	YCC8/ REC656	PRGB	SRGB
HSYNC GIO073	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC GIO072	VSYNC	VSYNC	VSYNC	VSYNC
LCD_OE GIO071	As needed	As needed	As needed	As needed
FIELD GIO070 R2 PWM3C	As needed	As needed	As needed	As needed
EXTCLK GIO069 B2 PWM3D	As needed	As needed	As needed	As needed
VCLK GIO068	VCLK	VCLK	VCLK	VCLK
YOUT7	Y7	Y7,Cb7,Cr7	R7	Data7
YOUT6	Y6	Y6,Cb6,Cr6	R6	Data6
YOUT5	Y5	Y5,Cb5,Cr5	R5	Data5
YOUT4	Y4	Y4,Cb4,Cr4	R4	Data4
YOUT3	Y3	Y3,Cb3,Cr3	R3	Data3
YOUT2	Y2	Y2,Cb2,Cr2	G7	Data2
YOUT1	Y1	Y1,Cb1,Cr1	G6	Data1
YOUT0	Y0	Y0,Cb0,Cr0	G5	Data0
COUT7 GIO081 PWM0	C7	LCD_AC	G4	LCD_AC
COUT6 GIO080 PWM1	C6	LCD_OE	G3	LCD_OE
COUT5 GIO079 PWM2A RTO0	C5	BRIGHT	G2	BRIGHT
COUT4 GIO078 PWM2B RTO1	C4	PWM	B7	PWM
COUT3 GIO077 PWM2C RTO2	C3	CSYNC	B6	CSYNC
COUT2 GIO076 PWM2D RTO3	C2	-	B5	-
COUT1 GIO075 PWM3A	C1	-	B4	-
COUT0 GIO074 PWM3B	C0	-	B3	-

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Table 2-7. Digital Video Terminal Functions

TERMINAL		TYPE[1]	OTHER[2] [3]	DESCRIPTION[4]
NAME	NO.			
YOUT7-R7	C3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT6-R6	A4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT5-R5	B4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT4-R4	B3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT3-R3	B2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT2-G7	A3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT1-G6	A2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
YOUT0-G5	B1	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function
COUT7-G4/GIO081 /PWM0	C2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[081] PWM0
COUT6-G3 /GIO080 /PWM1	D2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[080] PWM1
COUT5-G2 / GIO079 / PWM2A / RTO0	C1	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[079] PWM2A RTO0
COUT4-B7 / GIO078 / PWM2B / RTO1	D3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[078] PWM2B RTO1
COUT3-B6 / GIO077 / PWM2C / RTO2	E3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[077] PWM2C RTO2
COUT2-B5 / GIO076 / PWM2D / RTO3	E4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[076] PWM2D RTO3
COUT1-B4 / GIO075 / PWM3A	F3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[075] PWM3A
COUT0-B3 / GIO074 / PWM3B	F4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[074] PWM3B
HSYNC / GIO073	F5	I/O/Z	PD V_{DD_VOUT}	Video Encoder: Horizontal Sync GIO: GIO[073]
VSYNC / GIO072	G5	I/O/Z	PD V_{DD_VOUT}	Video Encoder: Vertical Sync GIO: GIO[072]
FIELD / GIO070 / R2 / PWM3C	H4	I/O/Z	V_{DD_VOUT}	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C
EXTCLK / GIO069 / B2 / PWM3D	G3	I/O/Z	PD V_{DD_VOUT}	Video Encoder: External clock input, used if clock rates > 27 MHz are needed, e.g. 74.25 MHz for HDTV digital output GIO: GIO[069] Digital Video Out: B2 PWM3D
VCLK / GIO068	H3	I/O/Z	V_{DD_VOUT}	Video Encoder: Video Output Clock GIO: GIO[068]

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)
(4) To reduce EMI and reflections, depending on the trace length, approximately 22 Ω to 50 Ω damping resistors are recommend on the following outputs placed near the DM355: YOUT(0-7),COUT(0-7), HSYNC,VSYNC,LCD_OE,FIELD,EXTCLK,VCLK. The trace lengths should be minimized.

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Table 2-8. Analog Video Terminal Functions

TERMINAL		TYPE(1)	OTHER(2)	DESCRIPTION
NAME	NO.			
VREF	J7	A I/O/Z		Video DAC: Reference voltage output (0.45V, 0.1uF to GND). When the DAC is not used, the VREF signal should be connected to V_{SS}.
IOUT	E1	A I/O/Z		Video DAC: Pre video buffer DAC output (1000 ohm to VFB). When the DAC is not used, the IOUT signal should be connected to V_{SS}.
IBIAS	F2	A I/O/Z		Video DAC: External resistor (2550 Ohms to GND) connection for current bias configuration. When the DAC is not used, the IBIAS signal should be connected to V_{SS}.
VFB	G1	A I/O/Z		Video DAC: Pre video buffer DAC output (1000 Ohms to IOUT, 1070 Ohms to TVOUT). When the DAC is not used, the VFB signal should be connected to V_{SS}.
TVOUT	F1	A I/O/Z	V	Video DAC: Analog Composite NTSC/PAL output (SeeFigure 5-31 andFigure 5-32 for circuit connection). When the DAC is not used, the TVOUT signal should be left as a No Connect or connected to V_{SS}.
V_{DDA18_DAC}	L7	PWR		Video DAC: Analog 1.8V power. When the DAC is not used, the V_{DDA18_DAC} signal should be connected to V_{SS}.
V_{SSA_DAC}	L8	GND		Video DAC: Analog 1.8V ground. When the DAC is not used, the V_{SSA_DAC} signal should be connected to V_{SS}.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal. Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(2) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

2.6 Asynchronous External Memory Interface (AEMIF)

The Asynchronous External Memory Interface (AEMIF) signals support AEMIF, NAND, and OneNAND.

Table 2-9. Asynchronous EMIF/NAND/OneNAND Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
EM_A13/ GIO067/ BTSEL[1]	V19	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit[13] GIO: GIO[67] System: BTSEL[1:0] sampled at power-on-reset to determine boot method.
EM_A12/ GIO066/ BTSEL[0]	U19	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit[12] GIO: GIO[66] System: BTSEL[1:0] sampled at power-on-reset to determine boot method.
EM_A11/ GIO065/ AECFG[3]	R16	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit[11] GIO: GIO[65] AECFG[3:0] sampled at power-on-reset to AECFG configuration. AECFG[3] sets default for PinMux2_EM_D15_8: AEMIF default bus width (16 or 8 bits)
EM_A10/ GIO064/ AECFG[2]	R18	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit[10] GIO: GIO[64] AECFG[3:0] sampled at power-on-reset to AECFG configuration. AECFG[2:1] sets default for PinMux2_EM_BA0: AEMIF EM_BA0 definition (EM_BA0, EM_A14, GIO[054], rsvd)
EM_A09/ GIO063/ AECFG[1]	P17	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit[09] GIO: GIO[63] AECFG[3:0] sampled at power-on-reset to AECFG configuration. AECFG[2:1] sets default for PinMux2_EM_BA0: AEMIF EM_BA0 definition (EM_BA0, EM_A14, GIO[054], rsvd)
EM_A08/ GIO062/ AECFG[0]	T19	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit[08] GIO: GIO[62] AECFG[0] sets default for: • PinMux2_EM_A0_BA1: AEMIF address width (OneNAND or NAND) • PinMux2_EM_A13_3: AEMIF address width (OneNAND or NAND)
EM_A07/ GIO061	P16	I/O/Z	V_{DD}	Async EMIF: Address bus bit[07] GIO: GIO[61] Used to drive boot status LED signal (active low) in ROM boot modes.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-9. Asynchronous EMIF/NAND/OneNAND Terminal Functions (continued)

TERMINAL		TYPE[1]	OTHER[2] [3]	DESCRIPTION
NAME	NO.			
EM_A06/ GIO060	P18	I/O/Z	V_{DD}	Async EMIF: Address bus bit[06] GIO: GIO[60]
EM_A05/ GIO059	R19	I/O/Z	V_{DD}	Async EMIF: Address bus bit[05] GIO: GIO[59]
EM_A04/ GIO058	P15	I/O/Z	V_{DD}	Async EMIF: Address bus bit[04] GIO: GIO[58]
EM_A03/ GIO057	N18	I/O/Z	V_{DD}	Async EMIF: Address bus bit[03] GIO: GIO[57]
EM_A02/	N15	I/O/Z	V_{DD}	Async EMIF: Address bus bit[02] NAND/SM/xD: CLE - Command latch enable output
EM_A01/	N17	I/O/Z	V_{DD}	Async EMIF: Address bus bit[01] NAND/SM/xD: ALE - Address latch enable output
EM_A00/ GIO056	M16	I/O/Z	V_{DD}	Async EMIF: Address bus bit[00] GIO: GIO[56]
EM_BA1/ GIO055	P19	I/O/Z	V_{DD}	Async EMIF: Bank address 1 signal - 16-bit address: • In 16-bit mode, lowest address bit. • In 8-bit mode, second lowest address bit. GIO: GIO[055]
EM_BA0/ GIO054 EM_A14	N19	I/O/Z	V_{DD}	Async EMIF: Bank address 0 signal - 8-bit address: • In 8-bit mode, lowest address bit. or can be used as an extra address line (bit14) when using 16-bit memories. GIO: GIO[054]
EM_D15/ GIO053	M18	I/O/Z	V_{DD}	Async EMIF: Data bus bit 15 GIO: GIO[053]
EM_D14/ GIO052	M19	I/O/Z	V_{DD}	Async EMIF: Data bus bit 14 GIO: GIO[052]
EM_D13/ GIO051	M15	I/O/Z	V_{DD}	Async EMIF: Data bus bit 13 GIO: GIO[051]
EM_D12/ GIO050	L18	I/O/Z	V_{DD}	Async EMIF: Data bus bit 12 GIO: GIO[050]
EM_D11/ GIO049	L17	I/O/Z	V_{DD}	Async EMIF: Data bus bit 11 GIO: GIO[049]
EM_D10/ GIO048	L19	I/O/Z	V_{DD}	Async EMIF: Data bus bit 10 GIO: GIO[048]
EM_D09/ GIO047	K18	I/O/Z	V_{DD}	Async EMIF: Data bus bit 09 GIO: GIO[047]
EM_D08/ GIO046	L16	I/O/Z	V_{DD}	Async EMIF: Data bus bit 08 GIO: GIO[046]
EM_D07/ GIO045	K19	I/O/Z	V_{DD}	Async EMIF: Data bus bit 07 GIO: GIO[045]
EM_D06/ GIO044	K17	I/O/Z	V_{DD}	Async EMIF: Data bus bit 06 GIO: GIO[044]
EM_D05/ GIO043	J19	I/O/Z	V_{DD}	Async EMIF: Data bus bit 05 GIO: GIO[043]
EM_D04/ GIO042	L15	I/O/Z	V_{DD}	Async EMIF: Data bus bit 04 GIO: GIO[042]
EM_D03/ GIO041	J18	I/O/Z	V_{DD}	Async EMIF: Data bus bit 03 GIO: GIO[041]
EM_D02/ GIO040	H19	I/O/Z	V_{DD}	Async EMIF: Data bus bit 02 GIO: GIO[040]
EM_D01/ GIO039	J17	I/O/Z	V_{DD}	Async EMIF: Data bus bit 01 GIO: GIO[039]
EM_D00/ GIO038	H18	I/O/Z	V_{DD}	Async EMIF: Data bus bit 00 GIO: GIO[038]

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Table 2-9. Asynchronous EMIF/NAND/OneNAND Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
EM_CE0/ GIO037	J16	I/O/Z	V_{DD}	Async EMIF: Lowest numbered chip select. Can be programmed to be used for standard asynchronous memories (example: flash), OneNAND, or NAND memory. Used for the default boot and ROM boot modes. GIO: GIO[037]
EM_CE1/ GIO036	G19	I/O/Z	V_{DD}	Async EMIF: Second chip select. Can be programmed to be used for standard asynchronous memories(example: flash), OneNAND, or NAND memory. GIO: GIO[036]
EM_WE/ GIO035	J15	I/O/Z	V_{DD}	Async EMIF: Write Enable NAND/SM/xD: WE (Write Enable) output GIO: GIO[035]
EM_OE/ GIO034	F19	I/O/Z	V_{DD}	Async EMIF: Output Enable NAND/SM/xD: RE (Read Enable) output GIO: GIO[034]
EM_WAIT/ GIO033	G18	I/O/Z	V_{DD}	Async EMIF: Async WAIT NAND/SM/xD: RDY/ BSY input GIO: GIO[033]
EM_ADV/ GIO032	H16	I/O/Z	V_{DD}	OneNAND: Address valid detect for OneNAND interface GIO: GIO[032]
EM_CLK/ GIO031	E19	I/O/Z	V_{DD}	OneNAND: Clock for OneNAND flash interface GIO: GIO[031]

2.7 DDR Memory Interface

The DDR EMIF supports DDR2 and mobile DDR.

Table 2-10. DDR Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
DDR_CLK	W9	I/O/Z	V_{DD_DDR}	DDR Data Clock
$\overline{\text{DDR_CLK}}$	W8	I/O/Z	V_{DD_DDR}	DDR Complementary Data Clock
$\overline{\text{DDR_RAS}}$	T6	I/O/Z	V_{DD_DDR}	DDR Row Address Strobe
$\overline{\text{DDR_CAS}}$	V9	I/O/Z	V_{DD_DDR}	DDR Column Address Strobe
$\overline{\text{DDR_WE}}$	W10	I/O/Z	V_{DD_DDR}	DDR Write Enable
$\overline{\text{DDR_CS}}$	T8	I/O/Z	V_{DD_DDR}	DDR Chip Select
DDR_CKE	V10	I/O/Z	V_{DD_DDR}	DDR Clock Enable
DDR_DQM[1]	U15	I/O/Z	V_{DD_DDR}	Data mask outputs: • DDR_DQM[1] - For DDR_DQ[15:8] • DDR_DQM[0] - For DDR_DQ[7:0]
DDR_DQM[0]	T12	I/O/Z	V_{DD_DDR}	
DDR_DQS[1]	V15	I/O/Z	V_{DD_DDR}	Data strobe input/outputs for each byte of the 16-bit data bus used to synchronize the data transfers. Output to DDR when writing and inputs when reading. • DDR_DQS[1] - For DDR_DQ[15:8] • DDR_DQS[0] - For DDR_DQ[7:0]
DDR_DQS[0]	V12	I/O/Z	V_{DD_DDR}	
DDR_BA[2]	V8	I/O/Z	V_{DD_DDR}	Bank select outputs. Two are required for 1Gb DDR2 memories.
DDR_BA[1]	U7	I/O/Z	V_{DD_DDR}	Bank select outputs. Two are required for 1Gb DDR2 memories.
DDR_BA[0]	U8	I/O/Z	V_{DD_DDR}	Bank select outputs. Two are required for 1Gb DDR2 memories.
DDR_A13	U6	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 13
DDR_A12	V7	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 12
DDR_A11	W7	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 11
DDR_A10	V6	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 10

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-10. DDR Terminal Functions (continued)

TERMINAL		TYPE[1]	OTHER[2] [3]	DESCRIPTION
NAME	NO.			
DDR_A09	W6	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 09
DDR_A08	W5	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 08
DDR_A07	V5	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 07
DDR_A06	U5	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 06
DDR_A05	W4	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 05
DDR_A04	V4	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 04
DDR_A03	W3	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 03
DDR_A02	W2	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 02
DDR_A01	V3	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 01
DDR_A00	V2	I/O/Z	V_{DD_DDR}	DDR Address Bus bit 00
DDR_DQ15	W17	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 15
DDR_DQ14	V16	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 14
DDR_DQ13	W16	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 13
DDR_DQ12	U16	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 12
DDR_DQ11	W15	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 11
DDR_DQ10	W14	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 10
DDR_DQ09	V14	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 09
DDR_DQ08	U13	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 08
DDR_DQ07	W13	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 07
DDR_DQ06	V13	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 06
DDR_DQ05	W12	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 05
DDR_DQ04	U12	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 04
DDR_DQ03	T11	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 03
DDR_DQ02	U11	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 02
DDR_DQ01	W11	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 01
DDR_DQ00	V11	I/O/Z	V_{DD_DDR}	DDR Data Bus bit 00
DDR_ DQGATE0	W18	I/O/Z	V_{DD_DDR}	DDR: Loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE1 with same constraints as used for DDR clock and data.
DDR_ DQGATE1	V17	I/O/Z	V_{DD_DDR}	DDR: Loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data.
DDR_VREF	U10	I/O/Z	V_{DD_DDR}	DDR: Voltage input for the SSTL_18 I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary.
V_{SSA_DLL}	R11	I/O/Z	V_{SSA_DLL}	DDR: Ground for the DDR DLL
V_{DDA33_DDRDLL}	R10	I/O/Z	V_{DDA33_DDRDLL}	DDR: Power (3.3 V) for the DDR DLL
DDR_ZN	T9	I/O/Z	V_{DD_DDR}	DDR: Reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm resistor @ 0.5% tolerance.

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2.8 GPIO

The General Purpose I/O signals provide generic I/O to external devices. Most of the GIO signals are multiplexed with other functions.

Table 2-11. GPIO Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
GIO000	C16	I/O/Z	V_{DD}	GIO:GIO[000] is sampled at reset and stored in the GIO0_RESET bit of the BOOTCFG register. Active low during MMC/SD boot (can be used as MMC/SD power control). Can be used as external clock input for Timer 3. **Note**: The GIO000 pin ***must*** be held high during NAND boot for the boot process to fuction properly.
GIO001	E14	I/O/Z	V_{DD}	GIO: GIO[001] Can be used as external clock input for Timer 3.
GIO002	F15	I/O/Z	V_{DD}	GIO: GIO[002] Can be used as external clock input for Timer 3.
GIO003	G15	I/O/Z	V_{DD}	GIO: GIO[003] Can be used as external clock input for Timer 3.
GIO004	B17	I/O/Z	V_{DD}	GIO: GIO[004]
GIO005	D15	I/O/Z	V_{DD}	GIO: GIO[005]
GIO006	B18	I/O/Z	V_{DD}	GIO: GIO[006]
GIO007 / SPI0_SDENA[1]	C17	I/O/Z	V_{DD}	GIO: GIO[007] SPI0: Chip Select 1
SPI1_SDO / GIO008	E12	I/O/Z	V_{DD}	SPI1: Data Out GIO: GIO[008]
SPI1_SDI / GIO009 / SPI1_SDENA[1]	A13	I/O/Z	V_{DD}	SPI1: Data In -OR- SPI1: Chip Select 1 GIO: GIO[009]
SPI1_SCLK / GIO010	C13	I/O/Z	V_{DD}	SPI1: Clock GIO: GIO[010]
SPI1_SDENA[0] / GIO011	E13	I/O/Z	V_{DD}	SPI1: Chip Select 0 GIO: GIO[011]
UART1_TXD / GIO012	R17	I/O/Z	V_{DD}	UART1: Transmit Data GIO: GIO[012]
UART1_RXD / GIO013	R15	I/O/Z	V_{DD}	UART1: Receive Data GIO: GIO[013]
I2C_SCL / GIO014	R14	I/O/Z	V_{DD}	I2C: Serial Clock GIO: GIO[014]
I2C_SDA / GIO015	R13	I/O/Z	V_{DD}	I2C: Serial Data GIO: GIO[015]
CLKOUT3 / GIO016	C11	I/O/Z	V_{DD}	CLKOUT: Output Clock 3 GIO: GIO[016]
CLKOUT2 / GIO017	A11	I/O/Z	V_{DD}	CLKOUT: Output Clock 2 GIO: GIO[017]
CLKOUT1 / GIO018	D12	I/O/Z	V_{DD}	CLKOUT: Output Clock 1 GIO: GIO[018]
MMCSD1_DATA0 / GIO019 / UART2_TXD	A18	I/O/Z	V_{DD}	MMCSD1: DATA0 GIO: GIO[019] UART2: Transmit Data

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-11. GPIO Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
MMCSD1_DATA1 / GIO020 / UART2_RXD	B15	I/O/Z	V_{DD}	MMCSD1: DATA1 GIO: GIO[020] UART2: Receive Data
MMCSD1_DATA2 / GIO021 / UART2_CTS	A16	I/O/Z	V_{DD}	MMCSD1: DATA2 GIO: GIO[021] UART2: CTS
MMCSD1_DATA3 / GIO022 / UART2_RTS	B16	I/O/Z	V_{DD}	MMCSD1: DATA3 GIO: GIO[022] UART2: RTS
MMCSD1_CMD / GIO023	A17	I/O/Z	V_{DD}	MMCSD1: Command GIO: GIO[023]
MMCSD1_CLK / GIO024	C15	I/O/Z	V_{DD}	MMCSD1: Clock GIO: GIO[024]
ASP0_FSR / GIO025	F16	I/O/Z	V_{DD}	ASP0: Receive Frame Synch GIO: GIO[025]
ASP0_CLKR / GIO026	F17	I/O/Z	V_{DD}	ASP0: Receive Clock GIO: GIO[026]
ASP0_DR / GIO027	E18	I/O/Z	V_{DD}	ASP0: Receive Data GIO: GIO[027]
ASP0_FSX / GIO028	G17	I/O/Z	V_{DD}	ASP0: Transmit Frame Synch GIO: GIO[028]
ASP0_CLKX / GIO029	F18	I/O/Z	V_{DD}	ASP0: Transmit Clock GIO: GIO[029]
ASP0_DX / GIO030	H15	I/O/Z	V_{DD}	ASP0: Transmit Data GIO: GIO[030]
EM_CLK / GIO031	E19	I/O/Z	V_{DD}	OneNAND: Clock signal for OneNAND flash interface GIO: GIO[031]
EM_ADV / GIO032	H16	I/O/Z	PD V_{DD}	OneNAND: Address Valid Detect for OneNAND interface GIO: GIO[032]
EM_WAIT / GIO033	G18	I/O/Z	PU V_{DD}	Async EMIF: Async WAIT NAND/SM/xD: RDY/_BSY input GIO: GIO[033]
EM_OE / GIO034	F19	I/O/Z	V_{DD}	Async EMIF: Output Enable NAND/SM/xD: RE (Read Enable) output GIO: GIO[034]
EM_WE / GIO035	J15	I/O/Z	V_{DD}	Async EMIF: Write Enable NAND/SM/xD: WE (Write Enable) output GIO: GIO[035]
EM_CE1 / GIO036	G19	I/O/Z	V_{DD}	Async EMIF: Second Chip Select., Can be programmed to be used for standard asynchronous memories (example: flash), OneNand or NAND memory. GIO: GIO[036]
EM_CE0 / GIO037	J16	I/O/Z	V_{DD}	Async EMIF: Lowest numbered Chip Select. Can be programmed to be used for standard asynchronous memories (example: flash), OneNand or NAND memory. Used for the default boot and ROM boot modes. GIO: GIO[037]
EM_D00 / GIO038	H18	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[00] GIO: GIO[038]

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Table 2-11. GPIO Terminal Functions (continued)

TERMINAL		TYPE[1]	OTHER[2] [3]	DESCRIPTION
NAME	NO.			
EM_D01 / GIO039	J17	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[01] GIO: GIO[039]
EM_D02 / GIO040	H19	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[02] GIO: GIO[040]
EM_D03 / GIO041	J18	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[03] GIO: GIO[041]
EM_D04 / GIO042	L15	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[04] GIO: GIO[042]
EM_D05 / GIO043	J19	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[05] GIO: GIO[043]
EM_D06 / GIO044	K17	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[06] GIO: GIO[044]
EM_D07 / GIO045	K19	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[07] GIO: GIO[045]
EM_D08 / GIO046	L16	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[08] GIO: GIO[046]
EM_D09 / GIO047	K18	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[09] GIO: GIO[047]
EM_D10 / GIO048	L19	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[10] GIO: GIO[048]
EM_D11 / GIO049	L17	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[11] GIO: GIO[049]
EM_D12 / GIO050	L18	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[12] GIO: GIO[050]
EM_D13 / GIO051	M15	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[13] GIO: GIO[051]
EM_D14 / GIO052	M19	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[14] GIO: GIO[052]
EM_D15 / GIO053	M18	I/O/Z	V_{DD}	Async EMIF: Data Bus bit[15] GIO: GIO[053]
EM_BA0 / GIO054 / EM_A14	N19	I/O/Z	V_{DD}	Async EMIF: Bank Address 0 signal = 8-bit address. In 8-bit mode, lowest address bit. Or, can be used as an extra Address line (bit[14] when using 16-bit memories. GIO: GIO[054]
EM_BA1 / GIO055	P19	I/O/Z	V_{DD}	Async EMIF: Bank Address 1 signal = 16-bit address. In 16-bit mode, lowest address bit. In 8-bit mode, second lowest address bit GIO: GIO[055]
EM_A00 / GIO056	M16	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[00] Note that the EM_A0 is always a 32-bit address GIO: GIO[056]
EM_A03 / GIO057	N18	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[03] GIO: GIO[057]
EM_A04 / GIO058	P15	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[04] GIO: GIO[058]
EM_A05 / GIO059	R19	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[05] GIO: GIO[059]
EM_A06 / GIO060	P18	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[06] GIO: GIO[060]
EM_A07 / GIO061	P16	I/O/Z	V_{DD}	Async EMIF: Address Bus bit[07] GIO: GIO[061] - Used to drive boot status LED signal (active low) in ROM boot modes.
EM_A08 / GIO062 / AECFG[0]	T19	I/O/Z	PU V_{DD}	Async EMIF: Address Bus bit[08] GIO: GIO[062] AECFG[0] sets default for - PinMux2.EM_A0_BA1: AEMIF Address Width (OneNAND or NAND) - PinMux2.EM_A13_3: AEMIF Address Width (OneNAND or NAND)

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Table 2-11. GPIO Terminal Functions (continued)

TERMINAL		TYPE[1]	OTHER[2] [3]	DESCRIPTION
NAME	NO.			
EM_A09 / GIO063 / AECFG[1]	P17	I/O/Z	PD V_{DD}	Async EMIF: Address Bus bit[09] GIO: GIO[063] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[2:1] sets default for PinMux2.EM_BA0: AEMIF EM_BA0 Definition (EM_BA0, EM_A14, GIO[054], rsvd)
EM_A10 / GIO064 / AECFG[2]	R18	I/O/Z	PU V_{DD}	Async EMIF: Address Bus bit[10] GIO: GIO[064] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[2:1] sets default for PinMux2.EM_BA0: AEMIF EM_BA0 Definition (EM_BA0, EM_A14, GIO[054], rsvd)
EM_A11 / GIO065 / AECFG[3]	R16	I/O/Z	PU V_{DD}	Async EMIF: Address Bus bit[11] GIO: GIO[065] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[3] sets default for PinMux2.EM_D15_8: AEMIF Default Bus Width (16 or 8 bits)
EM_A12 / GIO066 / BTSEL[0]	U19	I/O/Z	PD V_{DD}	Async EMIF: Address Bus bit[12] GIO: GIO[066] System: BTSEL[1:0] sampled at Power-on-Reset to determine Boot method
EM_A13 / GIO067 / BTSEL[1]	V19	I/O/Z	PD V_{DD}	Async EMIF: Address Bus bit[13] GIO: GIO[067] System: BTSEL[1:0] sampled at Power-on-Reset to determine Boot method.
VCLK / GIO068	H3	I/O/Z	V_{DD_VOUT}	Video Encoder: Video Output Clock GIO: GIO[068]
EXTCLK / GIO069 / B2 / PWM3D	G3	I/O/Z	PD V_{DD_VOUT}	Video Encoder: External clock input, used if clock rates > 27 MHz are needed, e.g. 74.25 MHz for HDTV digital output GIO: GIO[069] Digital Video Out: B2 PWM3D
FIELD / GIO070 / R2 / PWM3C	H4	I/O/Z	V_{DD_VOUT}	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C
VSYNC / GIO072	G5	I/O/Z	PD V_{DD_VOUT}	Video Encoder: Vertical Sync GIO: GIO[072]
HSYNC / GIO073	F5	I/O/Z	PD V_{DD_VOUT}	Video Encoder: Horizontal Sync GIO: GIO[073]
COUT0-B3 / GIO074 / PWM3B	F4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[074] PWM3B
COUT1-B4 / GIO075 / PWM3A	F3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[075] PWM3A
COUT2-B5 / GIO076 / PWM2D / RTO3	E4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[076] PWM2D RTO3
COUT3-B6 / GIO077 / PWM2C / RTO2	E3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[077] PWM2C RTO2
COUT4-B7 / GIO078 / PWM2B / RTO1	D3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[078] PWM2B RTO1
COUT5-G2 / GIO079 / PWM2A / RTO0	C1	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[079] PWM2A RTO0

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Table 2-11. GPIO Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
COUT6-G3 / GIO080 / PWM1	D2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[080] PWM1
COUT7-G4 / GIO081 / PWM0	C2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[081] PWM0
PCLK / GIO082	T3	I/O/Z	PD V_{DD_VIN}	Pixel clock input (strobe for lines CI7 through YI0) GIO: GIO[082]
CAM_WEN_FIELD / GIO083	R5	I/O/Z	PD V_{DD_VIN}	Write enable input signal is used by external device (AFE/TG) to gate the DDR output of the CCDC module. Alternately, the field identification input signal is used by external device (AFE/TG) to indicate the which of two frames is input to the CCDC module for sensors with interlaced output. CCDC handles 1- or 2-field sensors in hardware. GIO: GIO[083]
CAM_VD / GIO084	R4	I/O/Z	PD V_{DD_VIN}	Vertical synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new frame starts. GIO: GIO[084]
CAM_HD / GIO085	N5	I/O/Z	PD V_{DD_VIN}	Horizontal synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new line starts. GIO: GIO[085]
YIN0 / GIO086	P5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[00] YCC 16-bit: time multiplexed between luma: Y[00] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[00] GIO: GIO[086]
YIN1 / GIO087	P2	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[01] YCC 16-bit: time multiplexed between luma: Y[01] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[01] GIO: GIO[087]
YIN2 / GIO088	P4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[02] YCC 16-bit: time multiplexed between luma: Y[02] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[02] GIO: GIO[088]
YIN3 / GIO089	R3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[03] YCC 16-bit: time multiplexed between luma: Y[03] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[03] GIO: GIO[089]
YIN4 / GIO090	P3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[04] YCC 16-bit: time multiplexed between luma: Y[04] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[04] GIO: GIO[090]
YIN5 / GIO091	M5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[05] YCC 16-bit: time multiplexed between luma: Y[05] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[05] GIO: GIO[091]
YIN6 / GIO092	M4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[06] YCC 16-bit: time multiplexed between luma: Y[06] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[06] GIO: GIO[092]
YIN7 / GIO093	L5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[07] YCC 16-bit: time multiplexed between luma: Y[07] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[07] GIO: GIO[093]
CIN0 / GIO094	J3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[08] YCC 16-bit: time multiplexed between chroma: CB/CR[00] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[00] GIO: GIO[094]

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Table 2-11. GPIO Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
CIN1 / GIO095	L3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[09] YCC 16-bit: time multiplexed between chroma: CB/CR[01] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[01] GIO: GIO[095]
CIN2 / GIO096	J5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[10] YCC 16-bit: time multiplexed between chroma: CB/CR[02] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[02] GIO: GIO[096]
CIN3 / GIO097	J4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[11] YCC 16-bit: time multiplexed between chroma: CB/CR[03] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[03] GIO: GIO[097]
CIN4 / GIO098 / SPI2_SDI / SPI2_SDENA[1]	L4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[12] YCC 16-bit: time multiplexed between chroma: CB/CR[04] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[04] SPI: SPI2 Data In -OR- SPI2 Chip select 1. GIO: GIO[098]
CIN5 / GIO099 / SPI2_SDENA[0]	M3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: raw[13] YCC 16-bit: time multiplexed between chroma: CB/CR[05] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[05] SPI: SPI2 Chip Select 0. GIO: GIO[99]
CIN6 / GIO100 / SPI2_SDO	K5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: NOT USED YCC 16-bit: time multiplexed between chroma: CB/CR[06] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[06] SPI: SPI2 Data Out GIO: GIO[100]
CIN7 / GIO101 / SPI2_SCLK	N3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: NOT USED YCC 16-bit: time multiplexed between chroma: CB/CR[07] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] SPI: SPI2 Clock GIO: GIO[101]
SPI0_SDI / GIO102	A12	I/O/Z	V_{DD}	SPI0: Data In GIO: GIO[102]
SPI0_SDENA[0] / GIO103	B12	I/O/Z	V_{DD}	SPI0: Chip Select 0 GIO: GIO[103]

2.9 Multi-Media Card/Secure Digital (MMC/SD) Interfaces

The DM355 includes two Multi-Media Card/Secure Digital card interfaces that are compatible with the MMC/SD and SDIO protocol.

Table 2-12. MMC/SD Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
MMCSD0_CLK	A15	I/O/Z	V_{DD}	MMCSD0: Clock
MMCSD0_CMD	C14	I/O/Z	V_{DD}	MMCSD0: Command
MMCSD0_DATA0	B14	I/O/Z	V_{DD}	MMCSD0: DATA0

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-12. MMC/SD Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
MMCSD0_ DATA1	D14	I/O/Z	V_{DD}	MMCSD0: DATA1
MMCSD0_ DATA2	B13	I/O/Z	V_{DD}	MMCSD0: DATA2
MMCSD0_ DATA3	A14	I/O/Z	V_{DD}	MMCSD0: DATA3
MMCSD1_ CLK/ GIO024	C15	I/O/Z	V_{DD}	MMCSD1: Clock GIO: GIO[024]
MMCSD1_ CMD/ GIO023	A17	I/O/Z	V_{DD}	MMCSD1: Command GIO: GIO[023]
MMCSD1_ DATA0/ GIO019/ UART2_T XD	A18	I/O/Z	V_{DD}	MMCSD1: DATA0 GIO: GIO[019] UART2: Transmit data
MMCSD1_ DATA1/ GIO020/ UART2_R XD	B15	I/O/Z	V_{DD}	MMCSD1: DATA1 GIO: GIO[020] UART2: Receive data
MMCSD1_ DATA2/ GIO021/ UART2_C TS	A16	I/O/Z	V_{DD}	MMCSD1: DATA2 GIO: GIO[021] UART2: CTS
MMCSD1_ DATA3/ GIO022/ UART2_R TS	B16	I/O/Z	V_{DD}	MMCSD1: DATA3 GIO: GIO[022] UART2: RTS

2.10 Universal Serial Bus (USB) Interface

The Universal Serial Bus (USB) interface supports the USB2.0 High-Speed protocol and includes dual-role Host/Slave support. However, no charge pump is included.

Table 2-13. USB Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
USB_DP	A7	A I/O/Z	V_{DDA33_USB}	USB D+ (differential signal pair). When USB is not used, this signal should be connected to V_{SS_USB}.
USB_DM	A6	A I/O/Z	V_{DDA33_USB}	USB D- (differential signal pair). When USB is not used, this signal should be connected to V_{SS_USB}.
USB_R1	C7	A I/O/Z		USB reference current output Connect to $V_{SS_USB_REF}$ via 10K ohm , 1% resistor placed as close to the device as possible. When USB is not used, this signal should be connected to V_{SS_USB}.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-13. USB Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
USB_ID	D5	A I/O/Z	V_{DDA33_USB}	USB operating mode identification pin For Device mode operation only, pull up this pin to V_{DD} with a 1.5K ohm resistor. For Host mode operation only, pull down this pin to ground (V_{SS}) with a 1.5K ohm resistor. If using an OTG or mini-USB connector, this pin will be set properly via the cable/connector configuration. When USB is not used, this signal should be connected to V_{SS_USB}.
USB_VBUS	E5	A I/O/Z	V_{DD}	For host or device mode operation, tie the VBUS/USB power signal to the USB connector. When used in OTG mode operation, tie VBUS to the external charge pump and to the VBUS signal on the USB connector. When the USB is not used, tie VBUS to V_{SS_USB}.
USB_DRVVBUS	C5	O/Z	V_{DD}	Digital output to control external 5 V supply When USB is not used, this signal should be left as a No Connect.
$V_{SS_USB_REF}$	C8	GND	V_{DD}	USB Ground Reference Connect directly to ground and to USB_R1 via 10K ohm, 1% resistor placed as close to the device as possible.
V_{DDA33_USB}	J8	PWR	V_{DD}	Analog 3.3 V power USBPHY When USB is not used, this signal should be connected to V_{SS_USB}.
$V_{DDA33_USB_PLL}$	B6	PWR	V_{DD}	Common mode 3.3 V power for USB PHY (PLL) When USB is not used, this signal should be connected to V_{SS_USB}.
V_{DDA13_USB}	H7	PWR	V_{DD}	Analog 1.3 V power for USB PHY When USB is not used, this signal should be connected to V_{SS_USB}.
V_{DDD13_USB}	C6	PWR	V_{DD}	Digital 1.3 V power for USB PHY When USB is not used, this signal should be connected to V_{SS_USB}.

2.11 Audio Interfaces

The DM355 includes two Audio Serial Ports (ASP ports), which are backward compatible with other TI ASP serial ports and provide I2S audio interface. One interface is multiplexed with GIO signals.

Table 2-14. ASP Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
ASP0_CLKR/ GIO026	F17	I/O/Z	V_{DD}	ASP0: Receive Clock GIO: GIO[026]
ASP0_CLKX / GIO029	F18	I/O/Z	V_{DD}	ASP0: Transmit Clock GIO: GIO[029]
ASP0_DR / GIO027	E18	I/O/Z	V_{DD}	ASP0: Receive Data GIO: GIO[027]
ASP0_DX / GIO030	H15	I/O/Z	V_{DD}	ASP0: Transmit Data GIO: GIO[030]
ASP0_FSR / GIO025	F16	I/O/Z	V_{DD}	ASP0: Receive Frame Synch GIO: GIO[025]
ASP0_FSX / GIO028	G17	I/O/Z	V_{DD}	ASP0: Transmit Frame SynchGIO: GIO[028]
ASP1_CLKR	D18	I/O/Z	V_{DD}	ASP1: Receive Clock

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-14. ASP Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
ASP1_CLKS	D17	I/Z	V_{DD}	ASP1: Master Clock
ASP1_CLKX	D19	I/O/Z	V_{DD}	ASP1: Transmit Clock
ASP1_DR	C19	I/O/Z	V_{DD}	ASP1: Receive Data
ASP1_DX	C18	I/O/Z	V_{DD}	ASP1: Transmit Data
ASP1_FSR	E17	I/O/Z	V_{DD}	ASP1: Receive Frame Synch
ASP1_FSX	E16	I/O/Z	V_{DD}	ASP1: Transmit Frame Sync

2.12 UART Interface

The DM355 includes three UART ports. These ports are multiplexed with GIO and other signals.

Table 2-15. UART Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
UART0_RXD	U18	I	V_{DD}	UART0: Receive data. Used for UART boot mode
UART0_TXD	T18	O	V_{DD}	UART0: Transmit data. Used for UART boot mode
UART1_RXD/ GIO013	R15	I/O/Z	V_{DD}	UART1: Receive data. GIO: GIO013
UART1_TXD/ GIO012	R17	I/O/Z	V_{DD}	UART1: Transmit data. GIO: GIO012
MMCSD1_DATA2/ GIO021/ UART2_CTS	A16	I/O/Z	V_{DD}	MMCSD1: DATA2 GIO: GIO021 UART2: CTS
MMCSD1_DATA3/ GIO022/ UART2_RTS	B16	I/O/Z	V_{DD}	MMCSD1: DATA3 GIO: GIO022 UART2: RTS
MMCSD1_DATA1/ GIO020/ UART2_RXD	B15	I/O/Z	V_{DD}	MMCSD1: DATA1 GIO: GIO020 UART2: RXD
MMCSD1_DATA0/ GIO019/ UART2_TXD	A18	I/O/Z	V_{DD}	MMCSD1: DATA0 GIO: GIO019 UART2: TXD

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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2.13 I²C Interface

The DM355 includes an I²C two-wire serial interface for control of external peripherals. This interface is multiplexed with GIO signals.

Table 2-16. I²C Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
I2C_SDA/ GIO015	R13	I/O/Z	V_{DD}	I2C: Serial data GIO: GIO015
I2C_SCL/ GIO014	R14	I/O/Z	V_{DD}	I2C: Serial clock GIO: GIO014

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

2.14 Serial Interface

The DM355 includes three independent serial ports. These interfaces are multiplexed with GIO and other signals.

Table 2-17. SPI Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
SPI0_SCLK	C12	I/O/Z	V_{DD}	SPI0: Clock
SPI0_SDENA[0]/ GIO103	B12	I/O/Z	V_{DD}	SPI0: Chip select 0 GIO: GIO[103]
GIO007 SPI0_SDENA[1]	C17	I/O/Z	V_{DD}	GIO: GIO[007] SPI0: Chip select 1
SPI0_SDI/ GIO102	A12	I/O/Z	V_{DD}	SPI0: Data in GIO: GIO[102]
SPI0_SDO	B11	I/O/Z	V_{DD}	SPI0: Data out
SPI1_SCLK/ GIO010	C13	I/O/Z	V_{DD}	SPI1: Clock GIO: GIO[010]
SPI1_SDENA[0]/ GIO011	E13	I/O/Z	V_{DD}	SPI1: Chip select 0 GIO: GIO[011] - Active low during MMC/SD boot (can be used as MMC/SD power control)
SPI1_SDI/ GIO009/ SPI1_SDENA[1]	A13	I/O/Z	V_{DD}	SPI1: Data in or SPI1: Chip select 1 GIO: GIO[09]
SPI1_SDO/ GIO008	E12	I/O/Z	V_{DD}	SPI1: Data out GIO: GIO[008]
CIN7/ GIO101/ SPI2_SCLK	N3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Not used • YCC 16-bit: time multiplexed between chroma. CB/CR[07] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] SPI: SPI2 clock GIO: GIO[101]
CIN5/ GIO099/ SPI2_SDENA[0]	M3	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[13] • YCC 16-bit: time multiplexed between chroma. CB/CR[05] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] SPI: SPI2 chip select 0 GIO: GIO[099]

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-17. SPI Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
CIN4/ GIO098/ SPI2_SDI/ SPI2_SDENA[1]	L4	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Raw[12] • YCC 16-bit: time multiplexed between chroma. CB/CR[04] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[04] SPI: SPI2 Data in -OR- SPI2 Chip select 1 GIO: GIO[0998]
CIN6/ GIO100/ SPI2_SDO/	K5	I/O/Z	PD V_{DD_VIN}	Standard CCD/CMOS input: Not used • YCC 16-bit: time multiplexed between chroma. CB/CR[06] • YCC 8-bit (which allows for two simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[06] SPI: SPI2 Data out GIO: GIO[100]

2.15 Clock Interface

The DM355 provides interface with the system clocks.

Table 2-18. Clocks Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
CLKOUT1 / GIO018	D12	I/O/Z	V_{DD}	CLKOUT: Output Clock 1 GIO: GIO[018]
CLKOUT2 / GIO017	A11	I/O/Z	V_{DD}	CLKOUT: Output Clock 2 GIO: GIO[017]
CLKOUT3 / GIO016	C11	I/O/Z	V_{DD}	CLKOUT: Output Clock 3 GIO: GIO[016]
MXI1	A9	I	V_{DD}	Crystal input for system oscillator (24 MHz or 36 MHz)
MXO1	B9	O	V_{DD}	Output for system oscillator (24 MHz or 36 MHz). When the MX02 is not used, the MX02 signal can be left open.
MXI2	R1	I	V_{DD}	Crystal input for video oscillator (27 MHz) Optional, use only if 27MHz derived from MXI1 and PLL does not provide sufficient performance for Video DAC. When the MXI2 is not used and powered down, the MXI2 signal should be left as a No Connect
MXO2	T1	O	V_{DD}	Output for video oscillator (27 MHz) Optional, use only if 27MHz derived from MXI1 and PLL does not provide sufficient performance for Video DAC When the MXO2 is not used and powered down, the MXO2 signal should be left as a No Connect.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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2.16 Real Time Output (RTO) Interface

The DM355 provides Real Time Output (RTO) interface.

Table 2-19. RTO Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
COUT5- G2 / GIO079 / PWM2A / RTO0	C1	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[079] PWM2A RTO0
COUT4- B7 / GIO078 / PWM2B / RTO1	D3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[078] PWM2B RTO1
COUT3- B6 / GIO077 / PWM2C / RTO2	E3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[077] PWM2C RTO2
COUT2- B5 / GIO076 / PWM2D / RTO3	E4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[076] PWM2D RTO3

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

2.17 Pulse Width Modulator (PWM) Interface

The DM355 provides Pulse Width Modulator (PWM) interface.

Table 2-20. PWM Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
COUT7- G4 / GIO081 / PWM0	C2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[081] PWM0
COUT6- G3 / GIO080 / PWM1	D2	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[080] PWM1
COUT5- G2 / GIO079 / PWM2A / RTO0	C1	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[079] PWM2A RTO0
COUT4- B7 / GIO078 / PWM2B / RTO1	D3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[078] PWM2B RTO1

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-20. PWM Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
COUT3- B6 / GIO077 / PWM2C / RTO2	E3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[077] PWM2C RTO2
COUT2- B5 / GIO076 / PWM2D / RTO3	E4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[076] PWM2D RTO3
COUT1- B4 / GIO075 / PWM3A	F3	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[075] PWM3A
COUT0- B3 / GIO074 / PWM3B	F4	I/O/Z	V_{DD_VOUT}	Digital Video Out: VENC settings determine function GIO: GIO[074] PWM3B
FIELD / GIO070 / R2 / PWM3C	H4	I/O/Z	V_{DD_VOUT}	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C
EXTCLK / GIO069 / B2 / PWM3D	G3	I/O/Z	PD V_{DD_VOUT}	Video Encoder: External clock input, used if clock rates > 27 MHz are needed, e.g. 74.25 MHz for HDTV digital output GIO: GIO[069] Digital Video Out: B2 PWM3D

2.18 System Configuration Interface

The DM355 provides interfaces for system configuration and boot load.

Table 2-21. System/Boot Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
EM_A13/ GIO067/ BTSEL[1]	V19	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit 13 GIO: GIO[067] System: BTSEL[1:0] sampled at power-on-reset to determine boot method.
EM_A12/ GIO066/ BTSEL[0]	U19	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit 12 GIO: GIO[066] System: BTSEL[1:0] sampled at power-on-reset to determine boot method.
EM_A11/ GIO065/ AECFG[3]	R16	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit 11 GIO: GIO[065] System: AECFG[3:0] sampled a power-on-reset to set AEMIF configuration. AECFG[3] sets default fo PinMux2.EM_D15_8. AEMIF default bus width (16 or 8 bits).
EM_A10/ GIO064/ AECFG[2]	R18	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit 10 GIO: GIO[064] System: AECFG[3:0] sampled a power-on-reset to set AEMIF configuration. AECFG[2:1] sets default fo PinMux2.EM_BA0. AEMIF EM_BA0 definition: (EM_BA0, EM_A14, GIO[054], rsvd)
EM_A09/ GIO063/ AECFG[1]	P17	I/O/Z	PD V_{DD}	Async EMIF: Address bus bit 09 GIO: GIO[063] System: AECFG[3:0] sampled a power-on-reset to set AEMIF configuration. AECFG[2:1] sets default fo PinMux2.EM_BA0. AEMIF EM_BA0 definition: (EM_BA0, EM_A14, GIO[054], rsvd)

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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Table 2-21. System/Boot Terminal Functions (continued)

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
EM_A08/ GIO062/ AECFG[0]	T19	I/O/Z	PU V_{DD}	Async EMIF: Address bus bit 08 GIO: GIO[062] System: AECFG[0] sets default for: • PinMux2.EM_A0_BA1 - AEMIF address width (OneNAND, or NAND) • PinMux2.EM_A13_3 - AEMIF address width (OneNAND, or NAND)

2.19 Emulation

The emulation interface allow software and hardware debugging.

Table 2-22. Emulation Terminal Functions

TERMINAL		TYPE(1)	OTHER(2) (3)	DESCRIPTION
NAME	NO.			
TCK	E10	I	V_{DD}	JTAG test clock input
TDI	D9	I	PU V_{DD}	JTAG test data input
TDO	E9	O	V_{DD}	JTAG test data output
TMS	D8	I	PU V_{DD}	JTAG test mode select
$\overline{\text{TRST}}$	C9	I	PD V_{DD}	JTAG test logic reset (active low)
RTCK	E11	O	V_{DD}	JTAG test clock output
EMU0	E8	I/O/Z	PU V_{DD}	JTAG emulation 0 I/O EMU[1:0] = 00 - Force Debug Scan chain (ARM and ARM ETB TAPs connected) EMU[1:0] = 11 - Normal Scan chain (ICEpick only)
EMU1	E7	I/O/Z	PU V_{DD}	JTAG emulation 1 I/O EMU[1:0] = 00 - Force Debug Scan chain (ARM and ARM ETB TAPs connected) EMU[1:0] = 11 - Normal Scan chain (ICEpick only)

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)

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2.20 Pin List

Table 2-23 provides a complete pin description list in pin number order.

Table 2-23. DM355 Pin Descriptions

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
CIN7 / GIO101 / SPI2_SCLK	N3	I/O	CCDC / GIO / SPI2	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: NOT USED YCC 16-bit: time multiplexed between chroma: CB/CR[07] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[07] SPI: SPI2 Clock GIO: GIO[101]	PINMUX0[1:0].CIN_7
CIN6 / GIO100 / SPI2_SDO	K5	I/O	CCDC / GIO / SPI2	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: NOT USED YCC 16-bit: time multiplexed between chroma: CB/CR[06] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[06] SPI: SPI2 Data Out GIO: GIO[100]	PINMUX0[3:2].CIN_6
CIN5 / GIO099 / SPI2_SDENA[0]	M3	I/O	CCDC / GIO / SPI2	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[13] YCC 16-bit: time multiplexed between chroma: CB/CR[05] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[05] SPI: SPI2 Chip Select 0 GIO: GIO[99]	PINMUX0[5:4].CIN_5
CIN4 / GIO098 / SPI2_SDI / SPI2_SDENA[1]	L4	I/O	CCDC / GIO / SPI2 / SPI2	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[12] YCC 16-bit: time multiplexed between chroma: CB/CR[04] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[04] SPI: SPI2 Data In -OR- SPI2 Chip select 1 GIO: GIO[098]	PINMUX0[7:6].CIN_4

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal.
(2) Specifies the operating I/O supply voltage for each signal. See Section 5.3 , *Power Supplies* for more detail.
(3) PD = pull-down, PU = pull-up. (To pull up a signal to the opposite supply rail, a 1 kΩ resistor should be used.)
(4) To reduce EMI and reflections, depending on the trace length, approximately 22 Ω to 50 Ω damping resistors are recommend on the following outputs placed near the DM355: YOUT(0-7),COUT(0-7), HSYNC,VSYNC,LCD_OE,FIELD,EXTCLK,VCLK. The trace lengths should be minimized.

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
CIN3 / GIO097	J4	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[11] YCC 16-bit: time multiplexed between chroma: CB/CR[03] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[03] GIO: GIO[097]	PINMUX0[8].CIN_32
CIN2 / GIO096	J5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[10] YCC 16-bit: time multiplexed between chroma: CB/CR[02] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[02] GIO: GIO[096]	PINMUX0[8].CIN_32
CIN1 / GIO095	L3	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[09] YCC 16-bit: time multiplexed between chroma: CB/CR[01] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[01] GIO: GIO[095]	PINMUX0[9].CIN_10
CIN0 / GIO094	J3	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[08] YCC 16-bit: time multiplexed between chroma: CB/CR[00] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the upper channel. Y/CB/CR[00] GIO: GIO[094]	PINMUX0[9].CIN_10
YIN7 / GIO093	L5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[07] YCC 16-bit: time multiplexed between luma: Y[07] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[07] GIO: GIO[093]	PINMUX0[10].YIN_70
YIN6 / GIO092	M4	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[06] YCC 16-bit: time multiplexed between luma: Y[06] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[06] GIO: GIO[092]	PINMUX0[10].YIN_70

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
YIN5 / GIO091	M5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[05] YCC 16-bit: time multiplexed between luma: Y[05] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[05] GIO: GIO[091]	PINMUX0[10].YIN_70
YIN4 / GIO090	P3	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[04] YCC 16-bit: time multiplexed between luma: Y[04] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[04] GIO: GIO[090]	PINMUX0[10].YIN_70
YIN3 / GIO089	R3	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[03] YCC 16-bit: time multiplexed between luma: Y[03] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[03] GIO: GIO[089]	PINMUX0[10].YIN_70
YIN2 / GIO088	P4	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[02] YCC 16-bit: time multiplexed between luma: Y[02] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[02] GIO: GIO[088]	PINMUX0[10].YIN_70
YIN1 / GIO087	P2	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[01] YCC 16-bit: time multiplexed between luma: Y[01] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[01] GIO: GIO[087]	PINMUX0[10].YIN_70
YIN0 / GIO086	P5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Standard CCD/CMOS input: raw[00] YCC 16-bit: time multiplexed between luma: Y[00] YCC 08-bit (which allows for 2 simultaneous decoder inputs), it is time multiplexed between luma and chroma of the lower channel. Y/CB/CR[00] GIO: GIO[086]	PINMUX0[10].YIN_70

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
CAM_HD / GIO085	N5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Horizontal synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new line starts. GIO: GIO[085]	PINMUX0[11].CAM_HD
CAM_VD / GIO084	R4	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Vertical synchronization signal that can be either an input (slave mode) or an output (master mode). Tells the CCDC when a new frame starts. GIO: GIO[084]	PINMUX0[12].CAM_VD
CAM_WEN_FIELD / GIO083	R5	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Write enable input signal is used by external device (AFE/TG) to gate the DDR output of the CCDC module. Alternately, the field identification input signal is used by external device (AFE/TG) to indicate the which of two frames is input to the CCDC module for sensors with interlaced output. CCDC handles 1- or 2-field sensors in hardware. GIO: GIO[083]	PINMUX0[13].CAM_WEN plus CCDC.MODE[7].CCDMD & CCDC.MODE[5].SWEN
PCLK / GIO082	T3	I/O	CCDC / GIO	V_{DD_VIN}	PD	in	Pixel clock input (strobe for lines CI7 through YI0) GIO: GIO[082]	PINMUX0[14].PCLK
YOUT7-R7	C3	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT6-R6	A4	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT5-R5	B4	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT4-R4	B3	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT3-R3	B2	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT2-G7	A3	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT1-G6	A2	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
YOUT0-G5	B1	I/O	VENC	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function (5)	
COUT7-G4 / GIO081 / PWM0	C2	I/O	VENC / GIO / PWM0	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[081] PWM0	PINMUX1[1:0].COUT_7
COUT6-G3 / GIO080 / PWM1	D2	I/O	VENC / GIO / PWM1	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[080] PWM1 (5)	PINMUX1[3:2].COUT_6

(5) To reduce EMI and reflections, depending on the trace length, approximately 22 Ω to 50 Ω damping resistors are recommend on the following outputs placed near the DM355: YOUT(0-7),COUT(0-7), HSYNC,VSYNC,LCD_OE,FIELD,EXTCLK,VCLK. The trace lengths should be minimized.

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
COUT5-G2 / GIO079 / PWM2A / RTO0	C1	I/O	VENC / GIO / PWM2 / RTO	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[079] PWM2A RTO0 (5)	PINMUX1[5:4].COUT_5
COUT4-B7 / GIO078 / PWM2B / RTO1	D3	I/O	VENC / GIO / PWM2 / RTO	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[078] PWM2B RTO1 (5)	PINMUX1[7:6].COUT_4
COUT3-B6 / GIO077 / PWM2C / RTO2	E3	I/O	VENC / GIO / PWM2 / RTO	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[077] PWM2C RTO2 (5)	PINMUX1[9:8].COUT_3
COUT2-B5 / GIO076 / PWM2D / RTO3	E4	I/O	VENC / GIO / PWM2 / RTO	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[076] PWM2D RTO3 (6)	PINMUX1[11:10].COUT_2
COUT1-B4 / GIO075 / PWM3A	F3	I/O	VENC / GIO / PWM3	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[075] PWM3A (6)	PINMUX1[13:12].COUT_1
COUT0-B3 / GIO074 / PWM3B	F4	I/O	VENC / GIO / PWM3	V_{DD_VOUT}		in	Digital Video Out: VENC settings determine function GIO: GIO[074] PWM3B (6)	PINMUX1[15:14].COUT_0
HSYNC / GIO073	F5	I/O	VENC / GIO	V_{DD_VOUT}	PD	in	Video Encoder: Horizontal Sync GIO: GIO[073] (6)	PINMUX1[16].HVSYNC
VSYNC / GIO072	G5	I/O	VENC / GIO	V_{DD_VOUT}	PD	in	Video Encoder: Vertical Sync GIO: GIO[072] (6)	PINMUX1[16].HVSYNC
LCD_OE / GIO071	H5	I/O	VENC / GIO	V_{DD_VOUT}		out	Video Encoder: LCD Output Enable or BRIGHT signal GIO: GIO[071] (6)	PINMUX1[17].DLCD

(6) To reduce EMI and reflections, depending on the trace length, approximately 22 Ω to 50 Ω damping resistors are recommend on the following outputs placed near the DM355: YOUT(0-7),COUT(0-7), HSYNC,VSYNC,LCD_OE,FIELD,EXTCLK,VCLK. The trace lengths should be minimized.

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
FIELD / GIO070 / R2 / PWM3C	H4	I/O	VENC / GIO / VENC / PWM3	V_{DD_VOUT}		in	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C (6)	PINMUX1[19:18].FIELD
EXTCLK / GIO069 / B2 / PWM3D	G3	I/O	VENC / GIO / VENC / PWM3	V_{DD_VOUT}	PD	in	Video Encoder: External clock input, used if clock rates > 27 MHz are needed, e.g. 74.25 MHz for HDTV digital output GIO: GIO[069] Digital Video Out: B2 PWM3D (6)	PINMUX1[21:20].EXTCLK
VCLK / GIO068	H3	I/O	VENC / GIO	V_{DD_VOUT}		in	Video Encoder: Video Output Clock GIO: GIO[068] (6)	PINMUX1[22].VCLK
VREF	J7	A I/O	Video DAC				Video DAC: Reference voltage output (0.45V, 0.1uF to GND)	
IOUT	E1	A I/O	Video DAC				Video DAC: Pre video buffer DAC output (1000 ohm to VFB)	
IBIAS	F2	A I/O	Video DAC				Video DAC: External resistor (2550 Ohms to GND) connection for current bias configuration	
VFB	G1	A I/O	Video DAC				Video DAC: Pre video buffer DAC output (1000 ohm to IOUT, 1070 ohm to TVOUT)	
TVOUT	F1	A I/O	Video DAC	V_{DDA18_DAC}			Video DAC: Analog Composite NTSC/PAL output (SeeFigure 5-31 andFigure 5-32 for circuit connection)	
V_{DDA18V_DAC}	L7	PWR	Video DAC				Video DAC: Analog 1.8V power	
V_{SSA_DAC}	L8	GND	Video DAC				Video DAC: Analog 1.8V ground	
DDR_CLK	W9	I/O	DDR	V_{DD_DDR}		out L	DDR Data Clock	
$\overline{\text{DDR_CLK}}$	W8	I/O	DDR	V_{DD_DDR}		out H	DDR Complementary Data Clock	
$\overline{\text{DDR_RAS}}$	T6	I/O	DDR	V_{DD_DDR}		out H	DDR Row Address Strobe	
$\overline{\text{DDR_CAS}}$	V9	I/O	DDR	V_{DD_DDR}		out H	DDR Column Address Strobe	
$\overline{\text{DDR_WE}}$	W10	I/O	DDR	V_{DD_DDR}		out H	DDR Write Enable (active low)	
$\overline{\text{DDR_CS}}$	T8	I/O	DDR	V_{DD_DDR}		out H	DDR Chip Select (active low)	
DDR_CKE	V10	I/O	DDR	V_{DD_DDR}		out L	DDR Clock Enable	
DDR_DQM[1]	U15	I/O	DDR	V_{DD_DDR}		in	Data mask outputs: DDR_DQM1: For DDR_DQ[15:8]	
DDR_DQM[0]	T12	I/O	DDR	V_{DD_DDR}		in	Data mask outputs: DDR_DQM0: For DDR_DQ[7:0]	
DDR_DQS[1]	V15	I/O	DDR	V_{DD_DDR}		in	Data strobe input/outputs for each byte of the 16 bit data bus used to synchronize the data transfers. Output to DDR when writing and inputs when reading. DDR_DQS1: For DDR_DQ[15:8]	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
DDR_DQS[0]	V12	I/O	DDR	V_{DD_DDR}		in	Data strobe input/outputs for each byte of the 16 bit data bus used to synchronize the data transfers. Output to DDR when writing and inputs when reading. DDR_DQS0: For DDR_DQ[7:0]	
DDR_BA[2]	V8	I/O	DDR	V_{DD_DDR}		out L	Bank select outputs. Two are required for 1Gb DDR2 memories.	
DDR_BA[1]	U7	I/O	DDR	V_{DD_DDR}		out L	Bank select outputs. Two are required for 1Gb DDR2 memories.	
DDR_BA[0]	U8	I/O	DDR	V_{DD_DDR}		out L	Bank select outputs. Two are required for 1Gb DDR2 memories.	
DDR_A13	U6	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 13	
DDR_A12	V7	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 12	
DDR_A11	W7	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 11	
DDR_A10	V6	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 10	
DDR_A09	W6	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 09	
DDR_A08	W5	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 08	
DDR_A07	V5	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 07	
DDR_A06	U5	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 06	
DDR_A05	W4	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 05	
DDR_A04	V4	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 04	
DDR_A03	W3	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 03	
DDR_A02	W2	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 02	
DDR_A01	V3	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 01	
DDR_A00	V2	I/O	DDR	V_{DD_DDR}		out L	DDR Address Bus bit 00	
DDR_DQ15	W17	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 15	
DDR_DQ14	V16	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 14	
DDR_DQ13	W16	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 13	
DDR_DQ12	U16	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 12	
DDR_DQ11	W15	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 11	
DDR_DQ10	W14	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 10	
DDR_DQ09	V14	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 09	
DDR_DQ08	U13	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 08	
DDR_DQ07	W13	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 07	
DDR_DQ06	V13	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 06	
DDR_DQ05	W12	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 05	
DDR_DQ04	U12	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 04	
DDR_DQ03	T11	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 03	
DDR_DQ02	U11	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 02	
DDR_DQ01	W11	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 01	
DDR_DQ00	V11	I/O	DDR	V_{DD_DDR}		in	DDR Data Bus bit 00	
DDR_ DQGATE0	W18	I/O	DDR	V_{DD_DDR}		out	DDR: Loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE1 with same constraints as used for DDR clock and data.	
DDR_ DQGATE1	V17	I/O	DDR	V_{DD_DDR}		in	DDR: Loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data.	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
DDR_VREF	U10	PWR	DDRIO	V_{DD_DDR}			DDR: Voltage input for the SSTL_18 IO buffers	
V_{SSA_DLL}	R11	GND	DDRDLL	V_{SSA_DLL}			DDR: Ground for the DDR DLL	
V_{DDA33_DDRDLL}	R10	PWR	DDRDLL	V_{DDA33_DDRDLL}			DDR: Power (3.3 Volts) for the DDR DLL	
DDR_ZN	T9	I/O	DDRIO	V_{DD_DDR}			DDR: Reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm resistor @ 0.5% tolerance.	
EM_A13 / GIO067 / BTSEL[1]	V19	I/O	AEMIF / GIO / system	V_{DD}	PD	in L	Async EMIF: Address Bus bit[13] GIO: GIO[067] System: BTSEL[1:0] sampled at Power-on-Reset to determine Boot method (00:NAND, 01:Flash, 10:MMC/SD, 11:UART)	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A12 / GIO066 / BTSEL[0]	U19	I/O	AEMIF / GIO / system	V_{DD}	PD	in L	Async EMIF: Address Bus bit[12] GIO: GIO[066] System: BTSEL[1:0] sampled at Power-on-Reset to determine Boot method (00:NAND, 01:Flash, 10:MMC/SD, 11:UART)	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A11 / GIO065 / AECFG[3]	R16	I/O	AEMIF / GIO / system	V_{DD}	PU	in H	Async EMIF: Address Bus bit[11] GIO: GIO[065] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[3] sets default for PinMux2.EM_D15_8: AEMIF Default Bus Width (0:16 or 1:8 bits)	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A10 / GIO064 / AECFG[2]	R18	I/O	AEMIF / GIO / system	V_{DD}	PU	in H	Async EMIF: Address Bus bit[10] GIO: GIO[064] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[2:1] sets default for PinMux2.EM_BA0: AEMIF EM_BA0 Definition (00: EM_BA0, 01: EM_A14, 10:GIO[054], 11:rsvd)	PINMUX2[0].EM_A13_3, default set by AECFG[0]

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
EM_A09 / GIO063 / AECFG[1]	P17	I/O	AEMIF / GIO / system	V_{DD}	PD	in L	Async EMIF: Address Bus bit[09] GIO: GIO[063] System: AECFG[3:0] sampled at Power-on-Reset to set AEMIF Configuration AECFG[2:1] sets default for PinMux2.EM_BA0: AEMIF EM_BA0 Definition (00: EM_BA0, 01: EM_A14, 10:GIO[054], 11:rsvd)	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A08 / GIO062 / AECFG[0]	T19	I/O	AEMIF / GIO / system	V_{DD}	PU	in H	Async EMIF: Address Bus bit[08] GIO: GIO[062] AECFG[0] sets default for - PinMux2.EM_A0_BA1: AEMIF Address Width (OneNAND or NAND) - PinMux2.EM_A13_3: AEMIF Address Width (OneNAND or NAND) (0:AEMIF address bits, 1:GIO[67:57])	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A07 / GIO061	P16	I/O	AEMIF / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[07] GIO: GIO[061] - Used to drive boot status LED signal (active low) in ROM boot modes.	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A06 / GIO060	P18	I/O	AEMIF / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[06] GIO: GIO[060]	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A05 / GIO059	R19	I/O	AEMIF / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[05] GIO: GIO[059]	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A04 / GIO058	P15	I/O	AEMIF / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[04] GIO: GIO[058]	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A03 / GIO057	N18	I/O	AEMIF / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[03] GIO: GIO[057]	PINMUX2[0].EM_A13_3, default set by AECFG[0]
EM_A02	N15	I/O	AEMIF	V_{DD}		out L	Async EMIF: Address Bus bit[02] NAND/SM/xD: CLE - Command Latch Enable output	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
EM_A01	N17	I/O	AEMI F	V_{DD}		out L	Async EMIF: Address Bus bit[01] NAND/SM/xD: ALE - Address Latch Enable output	
EM_A00 / GIO056	M16	I/O	AEMI F / GIO	V_{DD}		out L	Async EMIF: Address Bus bit[00] Note that the EM_A0 is always a 32-bit address GIO: GIO[056]	PINMUX2[1].EM_A0_BA1, default set by AECFG[0]
EM_BA1 / GIO055	P19	I/O	AEMI F / GIO	V_{DD}		out H	Async EMIF: Bank Address 1 signal = 16-bit address. In 16-bit mode, lowest address bit. In 8-bit mode, second lowest address bit GIO: GIO[055]	PINMUX2[1].EM_A0_BA1, default set by AECFG[0]
EM_BA0 / GIO054 / EM_A14	N19	I/O	AEMI F / GIO	V_{DD}		out H	Async EMIF: Bank Address 0 signal = 8-bit address. In 8-bit mode, lowest address bit. Or, can be used as an extra Address line (bit[14] when using 16-bit memories. GIO: GIO[054]	PINMUX2[3:2].EM_BA0, default set by AECFG[2:1]
EM_D15 / GIO053	M18	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[15] GIO: GIO[053]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D14 / GIO052	M19	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[14] GIO: GIO[052]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D13 / GIO051	M15	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[13] GIO: GIO[051]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D12 / GIO050	L18	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[12] GIO: GIO[050]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D11 / GIO049	L17	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[11] GIO: GIO[049]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D10 / GIO048	L19	I/O	AEMI F / GIO	V_{DD}		in	Async EMIF: Data Bus bit[10] GIO: GIO[048]	PINMUX2[4].EM_D15_8, default set by AECFG[3]

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
EM_D09 / GIO047	K18	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[09] GIO: GIO[047]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D08 / GIO046	L16	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[08] GIO: GIO[046]	PINMUX2[4].EM_D15_8, default set by AECFG[3]
EM_D07 / GIO045	K19	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[07] GIO: GIO[045]	PINMUX2[5].EM_D7_0
EM_D06 / GIO044	K17	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[06] GIO: GIO[044]	PINMUX2[5].EM_D7_0
EM_D05 / GIO043	J19	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[05] GIO: GIO[043]	PINMUX2[5].EM_D7_0
EM_D04 / GIO042	L15	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[04] GIO: GIO[042]	PINMUX2[5].EM_D7_0
EM_D03 / GIO041	J18	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[03] GIO: GIO[041]	PINMUX2[5].EM_D7_0
EM_D02 / GIO040	H19	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[02] GIO: GIO[040]	PINMUX2[5].EM_D7_0
EM_D01 / GIO039	J17	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[01] GIO: GIO[039]	PINMUX2[5].EM_D7_0
EM_D00 / GIO038	H18	I/O	AEMIF / GIO	V_{DD}		in	Async EMIF: Data Bus bit[00] GIO: GIO[038]	PINMUX2[5].EM_D7_0
EM_CE0 / GIO037	J16	I/O	AEMIF / GIO	V_{DD}		out H	Async EMIF: Lowest numbered Chip Select. Can be programmed to be used for standard asynchronous memories (example:flash), OneNand or NAND memory. Used for the default boot and ROM boot modes. GIO: GIO[037]	PINMUX2[6].EM_CE0
EM_CE1 / GIO036	G19	I/O	AEMIF / GIO	V_{DD}		out H	Async EMIF: Second Chip Select., Can be programmed to be used for standard asynchronous memories (example: flash), OneNand or NAND memory. GIO: GIO[036]	PINMUX2[7].EM_CE1

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
EM_WE / GIO035	J15	I/O	AEMIF / GIO	V_{DD}		out H	Async EMIF: Write Enable NAND/SM/xD: WE (Write Enable) output GIO: GIO[035]	PINMUX2[8].EM_WE_OE
EM_OE / GIO034	F19	I/O	AEMIF / GIO	V_{DD}		out H	Async EMIF: Output Enable NAND/SM/xD: RE (Read Enable) output GIO: GIO[034]	PINMUX2[8].EM_WE_OE
EM_WAIT / GIO033	G18	I/O	AEMIF / GIO	V_{DD}	PU	in H	Async EMIF: Async WAIT NAND/SM/xD: RDY/_BSY input GIO: GIO[033]	PINMUX2[9].EM_WAIT
EM_ADV / GIO032	H16	I/O	AEMIF / GIO	V_{DD}	PD	in L	OneNAND: Address Valid Detect for OneNAND interface GIO: GIO[032]	PINMUX2[10].EM_ADV
EM_CLK / GIO031	E19	I/O	AEMIF / GIO	V_{DD}		out L	OneNAND: Clock signal for OneNAND flash interface GIO: GIO[031]	PINMUX2[11].EM_CLK
ASP0_DX / GIO030	H15	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Transmit Data GIO: GIO[030]	PINMUX3[0].GIO30
ASP0_CLKX / GIO029	F18	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Transmit Clock GIO: GIO[029]	PINMUX3[1].GIO29
ASP0_FSX / GIO028	G17	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Transmit Frame Synch GIO: GIO[028]	PINMUX3[2].GIO28
ASP0_DR / GIO027	E18	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Receive Data GIO: GIO[027]	PINMUX3[3].GIO27
ASP0_CLKR / GIO026	F17	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Receive Clock GIO: GIO[026]	PINMUX3[4].GIO26
ASP0_FSR / GIO025	F16	I/O	ASP0 / GIO	V_{DD}		in	ASP0: Receive Frame Synch GIO: GIO[025]	PINMUX3[5].GIO25
MMCSD1_CLK / GIO024	C15	I/O	MMCSD / GIO	V_{DD}		in	MMCSD1: Clock GIO: GIO[024]	PINMUX3[6].GIO24
MMCSD1_CMD / GIO023	A17	I/O	MMCSD / GIO	V_{DD}		in	MMCSD1: Command GIO: GIO[023]	PINMUX3[7].GIO23

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
MMCSD1_DATA3 / GIO022 / UART2_RTS	B16	I/O	MMC SD / GIO / UART 2	V_{DD}		in	MMCSD1: DATA3 GIO: GIO[022] UART2: RTS	PINMUX3[9:8].GIO22
MMCSD1_DATA2 / GIO021 / UART2_CTS	A16	I/O	MMC SD / GIO / UART 2	V_{DD}		in	MMCSD1: DATA2 GIO: GIO[021] UART2: CTS	PINMUX3[11:10].GIO21
MMCSD1_DATA1 / GIO020 / UART2_RXD	B15	I/O	MMC SD / GIO / UART 2	V_{DD}		in	MMCSD1: DATA1 GIO: GIO[020] UART2: Receive Data	PINMUX3[13:12].GIO20
MMCSD1_DATA0 / GIO019 / UART2_TXD	A18	I/O	MMC SD / GIO / UART 2	V_{DD}		in	MMCSD1: DATA0 GIO: GIO[019] UART2: Transmit Data	PINMUX3[15:14].GIO19
CLKOUT1 / GIO018	D12	I/O	Clocks / GIO	V_{DD}		in	CLKOUT: Output Clock 1 GIO: GIO[018]	PINMUX3[16].GIO18
CLKOUT2 / GIO017	A11	I/O	Clocks / GIO	V_{DD}		in	CLKOUT: Output Clock 2 GIO: GIO[017]	PINMUX3[17].GIO17
CLKOUT3 / GIO016	C11	I/O	Clocks / GIO	V_{DD}		in	CLKOUT: Output Clock 3 GIO: GIO[016]	PINMUX3[18].GIO16
I2C_SDA / GIO015	R13	I/O	I2C / GIO	V_{DD}		in	I2C: Serial Data GIO: GIO[015]	PINMUX3[19].GIO15
I2C_SCL / GIO014	R14	I/O	I2C / GIO	V_{DD}		in	I2C: Serial Clock GIO: GIO[014]	PINMUX3[20].GIO14
UART1_RXD / GIO013	R15	I/O	UART 1 / GIO	V_{DD}		in	UART1: Receive Data GIO: GIO[013]	PINMUX3[21].GIO13
UART1_TXD / GIO012	R17	I/O	UART 1 / GIO	V_{DD}		in	UART1: Transmit Data GIO: GIO[012]	PINMUX3[22].GIO12
SPI1_SDENA[0] / GIO011	E13	I/O	SPI1 / GIO	V_{DD}		in	SPI1: Chip Select 0 GIO: GIO[011]	PINMUX3[23].GIO11

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
SPI1_SCLK / GIO010	C13	I/O	SPI1 / GIO	V_{DD}		in	SPI1: Clock GIO: GIO[010]	PINMUX3[24].GIO10
SPI1_SDI / GIO009 / SPI1_SDENA[1]	A13	I/O	SPI1 / GIO / SPI1	V_{DD}		in	SPI1: Data In -OR- SPI1: Chip Select 1 GIO: GIO[009]	PINMUX3[26:25].GIO9
SPI1_SDO / GIO008	E12	I/O	SPI1 / GIO	V_{DD}		in	SPI1: Data Out GIO: GIO[008]	PINMUX3[27].GIO8
GIO007 / SPI0_SDENA[1]	C17	I/O	GIO debounce / SPI0	V_{DD}		in	GIO: GIO[007] SPI0: Chip Select 1	PINMUX3[28].GIO7
GIO006	B18	I/O	GIO debounce	V_{DD}		in	GIO: GIO[006]	
GIO005	D15	I/O	GIO debounce	V_{DD}		in	GIO: GIO[005]	
GIO004	B17	I/O	GIO debounce	V_{DD}		in	GIO: GIO[004]	
GIO003	G15	I/O	GIO debounce	V_{DD}		in	GIO: GIO[003]	
GIO002	F15	I/O	GIO debounce	V_{DD}		in	GIO: GIO[002]	
GIO001	E14	I/O	GIO debounce	V_{DD}		in	GIO: GIO[001]	
GIO000	C16	I/O	GIO debounce	V_{DD}		in	GIO: GIO[000] **Note**: The GIO000 pin ***must*** be held high during NAND boot for the boot process to fuction properly.	
USB_DP	A7	A I/O	USBPHY	V_{DDA33_USB}			USB D+ (differential signal pair)	
USB_DM	A6	A I/O	USBPHY	V_{DDA33_USB}			USB D- (differential signal pair)	
USB_R1	C7	A I/O	USBPHY				USB Reference current output Connect to $V_{SS_USB_REF}$ via 10K Ω ±1% resistor placed as close to the device as possible.	
USB_ID	D5	A I/O	USBPHY	V_{DDA33_USB}			USB operating mode identification pin For Device mode operation only, pull up this pin to V_{DD} with a 1.5K ohm resistor. For Host mode operation only, pull down this pin to ground (V_{SS}) with a 1.5K ohm resistor. If using an OTG or mini-USB connector, this pin will be set properly via the cable/connector configuration.	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
USB_VBUS	E5	A I/O	USBP HY				For host or device mode operation, tie the VBUS/USB power signal to the USB connector. When used in OTG mode operation, tie VBUS to the external charge pump and to the VBUS signal on the USB connector. When the USB is not used, tie VBUS to V_{SS_USB}.	
USB_DRVVBUS	C5	O	USBP HY	V_{DD}			Digital output to control external 5 V supply	
$V_{SS_USB_REF}$	C8	GND	USBP HY	V_{DD}			USB Ground Reference Connect directly to ground and to USB_R1 via 10K Ω ±1% resistor placed as close to the device as possible.	
V_{DDA33_USB}	J8	PWR	USBP HY	V_{DD}			Analog 3.3 V power USB PHY (Transceiver)	
V_{SS_USB}	B7	GND	USBP HY	V_{DD}			Analog 3.3 V ground for USB PHY (Transceiver)	
$V_{DDA33_USB_PLL}$	B6	PWR	USBP HY	V_{DD}			Common mode 3.3 V power for USB PHY (PLL)	
V_{SS_USB}	D6	GND	USBP HY	V_{DD}			Common mode 3.3 V ground for USB PHY (PLL)	
V_{DDA13_USB}	H7	PWR	USBP HY	V_{DD}			Analog 1.3 V power for USB PHY	
V_{SS_USB}	E6	GND	USBP HY	V_{DD}			Analog 1.3 V ground for USB PHY	
V_{DDD13_USB}	C6	PWR	USBP HY	V_{DD}			Digital 1.3 V power for USB PHY	
MMCSD0_CLK	A15	I/O	MMC SD0	V_{DD}		out L	MMCSD0: Clock	PINMUX4[2].MMCSD0_MS
MMCSD0_CMD	C14	I/O	MMC SD0	V_{DD}		in	MMCSD0: Command	PINMUX4[2].MMCSD0_MS
MMCSD0_DATA3	A14	I/O	MMC SD0	V_{DD}		in	MMCSD0: DATA3	PINMUX4[2].MMCSD0_MS
MMCSD0_DATA2	B13	I/O	MMC SD0	V_{DD}		in	MMCSD0: DATA2	PINMUX4[2].MMCSD0_MS
MMCSD0_DATA1	D14	I/O	MMC SD0	V_{DD}		in	MMCSD0: DATA1	PINMUX4[2].MMCSD0_MS
MMCSD0_DATA0	B14	I/O	MMC SD0	V_{DD}		in	MMCSD0: DATA0	PINMUX4[2].MMCSD0_MS
UART0_RXD	U18	I	UART 0	V_{DD}		in	UART0: Receive Data Used for UART boot mode	
UART0_TXD	T18	O	UART 0	V_{DD}		out H	UART0: Transmit Data Used for UART boot mode	
SPI0_SDENA[0] / GIO103	B12	I/O	SPI0 / GIO	V_{DD}		in	SPI0: Enable / Chip Select 0 GIO: GIO[103]	PINMUX4[0].SPI0_SDENA
SPI0_SCLK	C12	I/O	SPI0	V_{DD}		in	SPI0: Clock	
SPI0_SDI / GIO102	A12	I/O	SPI0 / GIO	V_{DD}		in	SPI0: Data In GIO: GIO[102]	PINMUX4[1].SPI0_SDI
SPI0_SDO	B11	I/O	SPI0	V_{DD}		in	SPI0: Data Out	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
ASP1_DX	C18	I/O	ASP1	V_{DD}		in	ASP1: Transmit Data	
ASP1_CLKX	D19	I/O	ASP1	V_{DD}		in	ASP1: Transmit Clock	
ASP1_FSX	E16	I/O	ASP1	V_{DD}		in	ASP1: Transmit Frame Sync	
ASP1_DR	C19	I/O	ASP1	V_{DD}		in	ASP1: Receive Data	
ASP1_CLKR	D18	I/O	ASP1	V_{DD}		in	ASP1: Receive Clock	
ASP1_FSR	E17	I/O	ASP1	V_{DD}		in	ASP1: Receive Frame Synch	
ASP1_CLKS	D17	I	ASP1	V_{DD}		in	ASP1: Master Clock	
$\overline{\text{RESET}}$	D11	I		V_{DD}	PU	in	Global Chip Reset (active low)	
MXI1	A9	I	Clocks	V_{DD}		in	Crystal input for system oscillator (24 MHz)	
MXO1	B9	O	Clocks	V_{DD}		out	Output for system oscillator (24 MHz)	
MXI2	R1	I	Clocks	V_{DD}		in	Crystal input for video oscillator (27 MHz). This crystal is not required V_{DD}	
MXO2	T1	O	Clocks	V_{DD}		out	Output for video oscillator (27 MHz). This crystal is not required. V_{DD}	
TCK	E10	I	EMULATION	V_{DD}	PU	in	JTAG test clock input	
TDI	D9	I	EMULATION	V_{DD}	PU	in	JTAG test data input	
TDO	E9	O	EMULATION	V_{DD}		out L	JTAG test data output	
TMS	D8	I	EMULATION	V_{DD}	PU	in	JTAG test mode select	
$\overline{\text{TRST}}$	C9	I	EMULATION	V_{DD}	PD	in	JTAG test logic reset (active low)	
RTCK	E11	O	EMULATION	V_{DD}		out L	JTAG test clock output	
EMU0	E8	I/O	EMULATION	V_{DD}	PU	in	JTAG emulation 0 I/O V_{DD} V_{DD}	
EMU1	E7	I/O	EMULATION	V_{DD}	PU	in	JTAG emulation 1 I/O EMU[1:0] = 00 - Force Debug Scan chain (ARM and ARM ETB TAPs connected) EMU[1:0] = 11 - Normal Scan chain (ICEpick only)	
RSV01	J1	A I/O/Z					Reserved. This signal should be left as a No Connect or connected to V_{SS}.	
RSV02	K1	A I/O/Z					Reserved. This signal should be left as a No Connect or connected to V_{SS}.	
RSV03	L1	A I/O/Z					Reserved. This signal should be left as a No Connect or connected to V_{SS}.	
RSV04	M1	A I/O/Z					Reserved. This signal should be left as a No Connect or connected to V_{SS}.	
RSV05	N2	A I/O/Z					Reserved. This signal should be connected to V_{SS}.	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
RSV06	M2	PWR					Reserved. This signal should be connected to V_{SS}.	
RSV07	K2	GND					Reserved. This signal should be connected to V_{SS}.	
NC	H8						No connect	
V_{DD_VIN}	P6	PWR					Power for Digital Video Input IO (3.3 V)	
V_{DD_VIN}	P7	PWR					Power for Digital Video Input IO (3.3 V)	
V_{DD_VIN}	P8	PWR					Power for Digital Video Input IO (3.3 V)	
V_{DD_VOUT}	F6	PWR					Power for Digital Video Output IO (3.3 V)	
V_{DD_VOUT}	F7	PWR					Power for Digital Video Output IO (3.3 V)	
V_{DD_VOUT}	F8	PWR					Power for Digital Video Output IO (3.3 V)	
V_{DD_DDR}	M9	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P9	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P10	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P11	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P12	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P13	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	P14	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	R9	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	R12	PWR					Power for DDR I/O (1.8 V)	
V_{DD_DDR}	T14	PWR					Power for DDR I/O (1.8 V)	
V_{DDA_PLL1}	G12	PWR					Analog Power for PLL1 (1.3 V)	
V_{DDA_PLL2}	H9	PWR					Analog Power for PLL2 (1.3 V)	
CV_{DD}	A1	PWR					Core power (1.3 V)	
CV_{DD}	A10	PWR					Core power (1.3 V)	
CV_{DD}	B19	PWR					Core power (1.3 V)	
CV_{DD}	C4	PWR					Core power (1.3 V)	
CV_{DD}	G6	PWR					Core power (1.3 V)	
CV_{DD}	G11	PWR					Core power (1.3 V)	
CV_{DD}	H10	PWR					Core power (1.3 V)	
CV_{DD}	H13	PWR					Core power (1.3 V)	
CV_{DD}	H17	PWR					Core power (1.3 V)	
CV_{DD}	J11	PWR					Core power (1.3 V)	
CV_{DD}	J12	PWR					Core power (1.3 V)	
CV_{DD}	J13	PWR					Core power (1.3 V)	
CV_{DD}	K6	PWR					Core power (1.3 V)	
CV_{DD}	K11	PWR					Core power (1.3 V)	
CV_{DD}	K12	PWR					Core power (1.3 V)	
CV_{DD}	L11	PWR					Core power (1.3 V)	
CV_{DD}	L12	PWR					Core power (1.3 V)	
CV_{DD}	N6	PWR					Core power (1.3 V)	
CV_{DD}	R7	PWR					Core power (1.3 V)	
CV_{DD}	R8	PWR					Core power (1.3 V)	
CV_{DD}	T17	PWR					Core power (1.3 V)	
CV_{DD}	W19	PWR					Core power (1.3 V)	
V_{DD}	F9	PWR					Power for Digital IO (3.3 V)	
V_{DD}	F10	PWR					Power for Digital IO (3.3 V)	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
V_{DD}	F11	PWR					Power for Digital IO (3.3 V)	
V_{DD}	F12	PWR					Power for Digital IO (3.3 V)	
V_{DD}	F13	PWR					Power for Digital IO (3.3 V)	
V_{DD}	F14	PWR					Power for Digital IO (3.3 V)	
V_{DD}	G8	PWR					Power for Digital IO (3.3 V)	
V_{DD}	G14	PWR					Power for Digital IO (3.3 V)	
V_{DD}	K8	PWR					Power for Digital IO (3.3 V)	
V_{DD}	K15	PWR					Power for Digital IO (3.3 V)	
V_{DD}	L6	PWR					Power for Digital IO (3.3 V)	
V_{DD}	L13	PWR					Power for Digital IO (3.3 V)	
V_{DD}	M10	PWR					Power for Digital IO (3.3 V)	
V_{DD}	M11	PWR					Power for Digital IO (3.3 V)	
V_{DD}	M12	PWR					Power for Digital IO (3.3 V)	
V_{DD}	M13	PWR					Power for Digital IO (3.3 V)	
V_{DD}	N11	PWR					Power for Digital IO (3.3 V)	
V_{DD}	N12	PWR					Power for Digital IO (3.3 V)	
V_{SS_MX1}	C10	GND					System oscillator (24 MHz) - ground	
V_{SS_MX2}	P1	GND					Video oscillator (27 MHz) - ground	
V_{SSA_PLL1}	H12	GND					Analog Ground for PLL1	
V_{SSA_PLL2}	J9	GND					Analog Ground for PLL2	
V_{SS}	A5	GND					Digital ground	
V_{SS}	A8	GND					Digital ground	
V_{SS}	A19	GND					Digital ground	
V_{SS}	B5	GND					Digital ground	
V_{SS}	B8	GND					Digital ground	
V_{SS}	B10	GND					Digital ground	
V_{SS}	D1	GND					Digital ground	
V_{SS}	E2	GND					Digital ground	
V_{SS}	E15	GND					Digital ground	
V_{SS}	G2	GND					Digital ground	
V_{SS}	G9	GND					Digital ground	
V_{SS}	H1	GND					Digital ground	
V_{SS}	H2	GND					Digital ground	
V_{SS}	H6	GND					Digital ground	
V_{SS}	H11	GND					Digital ground	
V_{SS}	H14	GND					Digital ground	
V_{SS}	J2	GND					Digital ground	
V_{SS}	J6	GND					Digital ground	
V_{SS}	J10	GND					Digital ground	
V_{SS}	J14	GND					Digital ground	
V_{SS}	K3	GND					Digital ground	
V_{SS}	K9	GND					Digital ground	
V_{SS}	K10	GND					Digital ground	
V_{SS}	K14	GND					Digital ground	
V_{SS}	L2	GND					Digital ground	
V_{SS}	L9	GND					Digital ground	

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Table 2-23. DM355 Pin Descriptions (continued)

Name	BGA ID	Type (1)	Group	Power Supply (2)	PU PD (3)	Reset State	Description (4)	Mux Control
V_{SS}	L10	GND					Digital ground	
V_{SS}	L14	GND					Digital ground	
V_{SS}	M6	GND					Digital ground	
V_{SS}	M7	GND					Digital ground	
V_{SS}	M8	GND					Digital ground	
V_{SS}	M14	GND					Digital ground	
V_{SS}	M17	GND					Digital ground	
V_{SS}	N1	GND					Digital ground	
V_{SS}	N8	GND					Digital ground	
V_{SS}	N9	GND					Digital ground	
V_{SS}	N14	GND					Digital ground	
V_{SS}	R2	GND					Digital ground	
V_{SS}	R6	GND					Digital ground	
V_{SS}	T2	GND					Digital ground	
V_{SS}	T5	GND					Digital ground	
V_{SS}	T15	GND					Digital ground	
V_{SS}	U1	GND					Digital ground	
V_{SS}	U2	GND					Digital ground	
V_{SS}	U3	GND					Digital ground	
V_{SS}	U4	GND					Digital ground	
V_{SS}	U9	GND					Digital ground	
V_{SS}	U14	GND					Digital ground	
V_{SS}	U17	GND					Digital ground	
V_{SS}	V1	GND					Digital ground	
V_{SS}	V18	GND					Digital ground	
V_{SS}	W1	GND					Digital ground	

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2.21 Device Support

2.21.1 Development Tools

TI offers an extensive line of development tools for DM355 systems, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of DM355 based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Hardware Development Tools:

Extended Development System (XDS™) Emulator (supports TMS320DM355 DMSoC multiprocessor system debug) EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320DM355 DMSoC platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

2.21.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g.,). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is undefined. Only qualified production devices are to be used in production.

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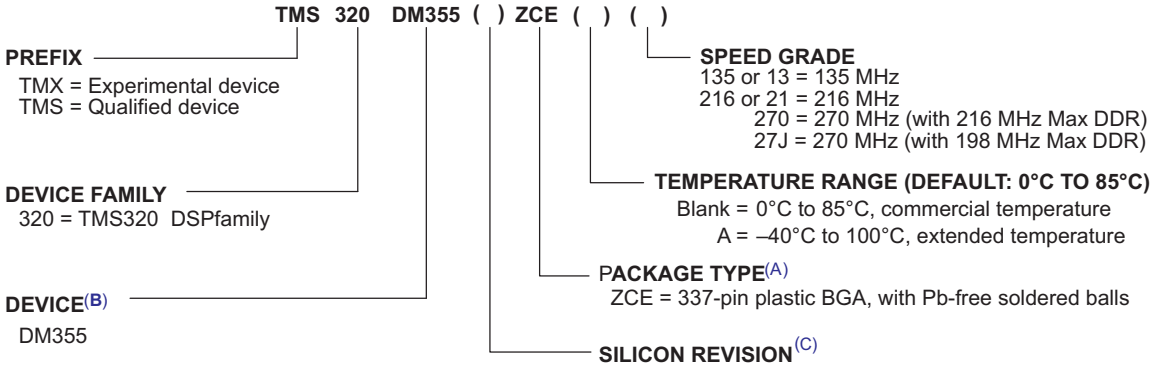
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZCE), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, 202 is 202.5 MHz). The following figure provides a legend for reading the complete device name for any TMS320DM355 DMSoC platform member.



A. BGA = Ball Grid Array

B. For actual device part numbers (P/Ns) and ordering information, contact your nearest TI Sales representative.

C. For more information on silicon revision, see *TMS320DM355 DMSoC Silicon Errata* (literature number SPRZ264).

Figure 2-5. Device Nomenclature

2.21.3 Device Documentation

2.21.3.1 Related Documentation From Texas Instruments

The following documents describe the TMS320DM35x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRS463 ***TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual*** This document describes the overall TMS320DM355 system, including device architecture and features, memory map, pin descriptions, timing characteristics and requirements, device mechanicals, etc.

SPRZ264 ***TMS320DM355 DMSoC Silicon Errata*** Describes the known exceptions to the functional specifications for the TMS320DM355 DMSoC.

SPRUFB3 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUED1 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Reference Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUED2 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Reference Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUED3 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP)***

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Reference Guide This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

SPRUED4 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Reference Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUED9 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Reference Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUEE0 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEE2 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUEE4 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUEE5 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) 64-bit Timer Reference Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM35x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUEE6 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide*** This document describes the general-purpose input/output (GPIO)

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peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUEE7 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Reference Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUEH7 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUF71 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Reference Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF72 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Reference Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF74 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Reference Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUFC8 ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Peripherals Overview Reference Guide*** This document provides an overview of the peripherals in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRAAR3 ***Implementing DDR2/mDDR PCB Layout on the TMS320DM35x DMSoC*** This provides board design recommendations and guidelines for DDR2 and mobile DDR.

SPRAAR7 ***USB 2.0 Board Design and Layout Guidelines*** This provides board design recommendations and guidelines for high speed USB.

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3 Detailed Device Description

This section provides a detailed overview of the DM355 device.

3.1 ARM Subsystem Overview

The ARM Subsystem contains components required to provide the ARM926EJ-S (ARM) master control of the overall DM355 system, including the components of the ARM Subsystem, the peripherals, and the external memories.

The ARM is responsible for handling system functions such as system-level initialization, configuration, user interface, user command execution, connectivity functions, interface and control of the subsystem, etc. The ARM is master and performs these functions because it has a large program memory space and fast context switching capability, and is thus suitable for complex, multi-tasking, and general-purpose control tasks.

3.1.1 Components of the ARM Subsystem

The ARM Subsystem in DM355 consists of the following components:

- ARM926EJ-S RISC processor, including:
  - coprocessor 15 (CP15)
  - MMU
  - 16KB Instruction cache
  - 8KB Data cache
  - Write Buffer
  - Java accelerator
- ARM Internal Memories
  - 32KB Internal RAM (32-bit wide access)
  - 8KB Internal ROM (ARM bootloader for non-AEMIF boot options)
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)
- System Control Peripherals
  - ARM Interrupt Controller
  - PLL Controller
  - Power and Sleep Controller
  - System Control Module

The ARM also manages/controls all the device peripherals:

- DDR2 / mDDR EMIF Controller
- AEMIF Controller, including the OneNAND and NAND flash interface
- Enhanced DMA (EDMA)
- UART
- Timers
- Real Time Out (RTO)
- Pulse Width Modulator (PWM)
- Inter-IC Communication (I2C)
- Multi-Media Card/Secure Digital (MMC/SD)
- Audio Serial Port (ASP)
- Universal Serial Bus Controller (USB)
- Serial Port Interface (SPI)
- Video Processing Front End (VPFE)
  - CCD Controller (CCDC)

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  - Image Pipe (IPIPE)
  - H3A Engine (Hardware engine for computing Auto-focus, Auto white balance, and Auto exposure)
- Video Processing Back End (VPBE)
  - On Screen Display (OSD)
  - Video Encoder Engine (VENC)

Figure 3-1 shows the functional block diagram of the DM355 ARM Subsystem.

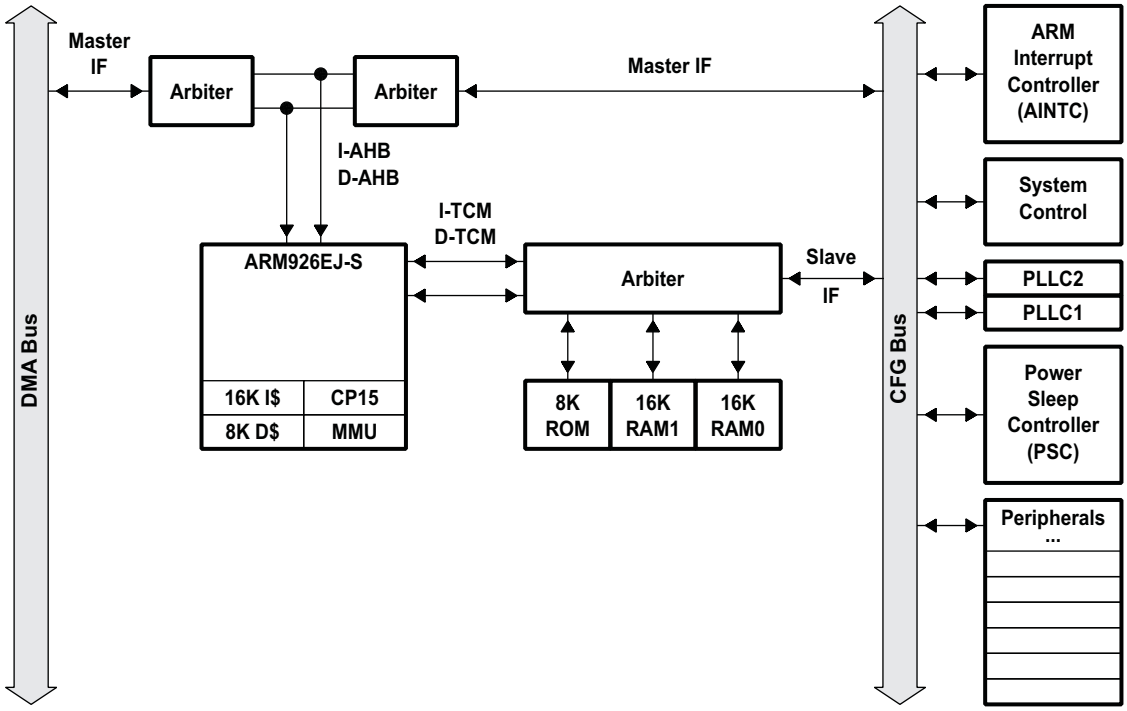

Figure 3-1. DM355 ARM Subsystem Block Diagram

3.2 ARM926EJ-S RISC CPU

The ARM Subsystem integrates the ARM926EJ-S processor. The ARM926EJ-S processor is a member of ARM9 family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S processor supports the 32-bit ARM and 16 bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. Specifically, the ARM926EJ-S processor supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ-S processor has a Harvard architecture and provides a complete high performance subsystem, including:

- ARM926EJ -S integer core
- CP15 system control coprocessor
- Memory Management Unit (MMU)
- Separate instruction and data Caches
- Write buffer
- Separate instruction and data Tightly-Coupled Memories (TCMs) [internal RAM] interfaces
- Separate instruction and data AHB bus interfaces

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- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)

For more complete details on the ARM9, refer to the ARM926EJ-S Technical Reference Manual, available at http://www.arm.com

3.2.1 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control instruction and data caches, Tightly-Coupled Memories (TCMs), Memory Management Unit (MMU), and other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR ARM instructions, when the ARM in a privileged mode such as supervisor or system mode.

3.2.2 MMU

The ARM926EJ-S MMU provides virtual memory features required by operating systems such as Linux, WindowCE, ultron, ThreadX, etc. A single set of two level page tables stored in main memory is used to control the address translation, permission checks and memory region attributes for both data and instruction accesses. The MMU uses a single unified Translation Lookaside Buffer (TLB) to cache the information held in the page tables. The MMU features are:

- Standard ARM architecture v4 and v5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes are:
  - 1MB (sections)
  - 64KB (large pages)
  - 4KB (small pages)
  - 1KB (tiny pages)
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpage permissions)
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8
- Invalidate TLB entry, selected by MVA, using CP15 register 8
- Lockdown of TLB entries, using CP15 register 10

3.2.3 Caches and Write Buffer

The size of the Instruction Cache is 16KB, Data cache is 8KB. Additionally, the Caches have the following features:

- Virtual index, virtual tag, and addressed using the Modified Virtual Address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32-bytes per line) and with two dirty bits in the Dcache
- Dcache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables.
- Critical-word first cache refilling
- Cache lockdown registers enable control over which cache ways are used for allocation on a line fill, providing a mechanism for both lockdown, and controlling cache corruption
- Dcache stores the Physical Address TAG (PA TAG) corresponding to each Dcache entry in the TAG RAM for use during the cache line write-backs, in addition to the Virtual Address TAG stored in the TAG RAM. This means that the MMU is not involved in Dcache write-back operations, removing the possibility of TLB misses related to the write-back address.
- Cache maintenance operations provide efficient invalidation of, the entire Dcache or Icache, regions of the Dcache or Icache, and regions of virtual memory.

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The write buffer is used for all writes to a noncachable bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the Dcache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The Dcache write-back has eight data word entries and a single address entry.

3.2.4 Tightly Coupled Memory (TCM)

ARM internal RAM is provided for storing real-time and performance-critical code/data and the Interrupt Vector table. ARM internal ROM boot options include—NAND (with SPI EEPROM Boot option), SPI, UART and MMC/SD. The RAM and ROM memories interfaced to the ARM926EJ-S via the tightly coupled memory interface that provides for separate instruction and data bus connections. Since the ARM TCM does not allow instructions on the D-TCM bus or data on the I-TCM bus, an arbiter is included so that both data and instructions can be stored in the internal RAM/ROM. The arbiter also allows accesses to the RAM/ROM from extra-ARM sources (e.g., EDMA or other masters). The ARM926EJ-S has built-in DMA support for direct accesses to the ARM internal memory from a non-ARM master. Because of the time-critical nature of the TCM link to the ARM internal memory, all accesses from non-ARM devices are treated as DMA transfers.

Instruction and Data accesses are differentiated via accessing different memory map regions, with the instruction region from 0x0000 through 0x7FFF and data from 0x10000 through 0x17FFF. Placing the instruction region at 0x0000 is necessary to allow the ARM Interrupt Vector table to be placed at 0x0000, as required by the ARM architecture. The internal 32-KB RAM is split into two physical banks of 16KB each, which allows simultaneous instruction and data accesses to be accomplished if the code and data are in separate banks.

3.2.5 Advanced High-performance Bus (AHB)

The ARM Subsystem uses the AHB port of the ARM926EJ-S to connect the ARM to the configuration bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the configuration bus and the external memories bus.

3.2.6 Embedded Trace Macrocell (ETM) and Embedded Trace Buffer (ETB)

To support real-time trace, the ARM926EJ-S processor provides an interface to enable connection of an Embedded Trace Macrocell (ETM). The ARM926ES-J Subsystem in DM355 also includes the Embedded Trace Buffer (ETB). The ETM consists of two parts:

- Trace Port provides real-time trace capability for the ARM9.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The DM355 trace port is not pinned out and is instead only connected to the Embedded Trace Buffer. The ETB has a 4KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

3.3 Memory Mapping

The ARM memory map is shown in Table 2-2 and Table 2-3. This section describes the memories and interfaces within the ARM's memory map.

3.3.1 ARM Internal Memories

The ARM has access to the following ARM internal memories:

- 32KB ARM Internal RAM on TCM interface, logically separated into two 16KB pages to allow simultaneous access on any given cycle if there are separate accesses for code (I-TCM bus) and data (D-TCM) to the different memory regions.
- 8KB ARM Internal ROM

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3.3.2 External Memories

The ARM has access to the following External memories:

- DDR2 / mDDR Synchronous DRAM
- Asynchronous EMIF / OneNAND
- NAND Flash
- Flash card devices:
  - MMC/SD
  - xD
  - SmartMedia

3.3.3 Peripherals

The ARM has access to all of the peripherals on the DM355 device.

3.4 ARM Interrupt Controller (AINTC)

The DM355 ARM Interrupt Controller (AINTC) has the following features:

- Supports up to 64 interrupt channels (16 external channels)
- Interrupt mask for each channel
- Each interrupt channel can be mapped to a Fast Interrupt Request (FIQ) or to an Interrupt Request (IRQ) type of interrupt.
- Hardware prioritization of simultaneous interrupts
- Configurable interrupt priority (2 levels of FIQ and 6 levels of IRQ)
- Configurable interrupt entry table (FIQ and IRQ priority table entry) to reduce interrupt processing time

The ARM core supports two interrupt types: FIQ and IRQ. See the ARM926EJ-S Technical Reference Manual for detailed information about the ARM's FIQ and IRQ interrupts. Each interrupt channel is mappable to an FIQ or to an IRQ type of interrupt, and each channel can be enabled or disabled. The INTC supports user-configurable interrupt-priority and interrupt entry addresses. Entry addresses minimize the time spent jumping to interrupt service routines (ISRs). When an interrupt occurs, the corresponding highest priority ISR's address is stored in the INTC's ENTRY register. The IRQ or FIQ interrupt routine can read the ENTRY register and jump to the corresponding ISR directly. Thus, the ARM does not require a software dispatcher to determine the asserted interrupt.

3.4.1 Interrupt Mapping

The AINTC takes up to 64 ARM device interrupts and maps them to either the IRQ or to the FIQ of the ARM. Each interrupt is also assigned one of 8 priority levels (2 for FIQ, 6 for IRQ). For interrupts with the same priority level, the priority is determined by the hardware interrupt number (the lowest number has the highest priority). Table 3-1 shows the connection of device interrupts to the ARM.

Table 3-1. AINTC Interrupt Connections(1)

Interrupt Number	Acronym	Source	Interrupt Number	Acronym	Source
0	VPSSINT0	VPSS - INT0, Configurable via VPSSBL register: INTSEL	32	TINT0	Timer 0 - TINT12
1	VPSSINT1	VPSS - INT1	33	TINT1	Timer 0 - TINT34
2	VPSSINT2	VPSS - INT2	34	TINT2	Timer 1 - TINT12

(1) The total number of interrupts in DM355 exceeds 64, which is the maximum value of the AINTC module. Therefore, several interrupts are multiplexed and you must use the register ARM_INTMUX in the System Control Module to select the interrupt source for multiplexed interrupts. Refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide (literature number SPRUFB3)* for more information on the System Control Module register ARM_INTMUX.

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Table 3-1. AINTC Interrupt Connections (1) (continued)

Interrupt Number	Acronym	Source	Interrupt Number	Acronym	Source
3	VPSSINT3	VPSS - INT3	35	TINT3	Timer 1 - TINT34
4	VPSSINT4	VPSS - INT4	36	PWMINT0	PWM0
5	VPSSINT5	VPSS - INT5	37	PWMINT1	PWM 1
6	VPSSINT6	VPSS - INT6	38	PWMINT2	PWM2
7	VPSSINT7	VPSS - INT7	39	I2CINT	I2C
8	VPSSINT8	VPSS - INT8	40	UARTINT0	UART0
9	Reserved		41	UARTINT1	UART1
10	Reserved		42	SPINT0-0	SPI0
11	Reserved		43	SPINT0-1	SPI0
12	USBINT	USB OTG Collector	44	GPIO0	GPIO
13	RTOINT or TINT4	RTO or Timer 2 - TINT12 SYS.ARM_INTMUX	45	GPIO1	GPIO
14	UARTINT2 or TINT5	UART2 or Timer 2 - TINT34	46	GPIO2	GPIO
15	TINT6	Timer 3 TINT12	47	GPIO3	GPIO
16	CCINT0	EDMA CC Region 0	48	GPIO4	GPIO
17	SPINT1-0 or CCERRINT	SPI1 or EDMA CC Error	49	GPIO5	GPIO
18	SPINT1-1 or TCERRINT0	SPI1 or EDMA TC0 Error	50	GPIO6	GPIO
19	SPINT2-0 or TCERRINT1	SPI2 or EDMA TC1 Error	51	GPIO7	GPIO
20	PSCINT	PSC - ALLINT	52	GPIO8	GPIO
21	SPINT2-1	SPI2	53	GPIO9	GPIO
22	TINT7	Timer3 - TINT34	54	GPIOBNK0	GPIO
23	SDIOINT0	MMC/SD0	55	GPIOBNK1	GPIO
24	MBXINT0 or MBXINT1	ASP0 or ASP1	56	GPIOBNK2	GPIO
25	MBRINT0 or MBRINT1	ASP0 or ASP1	57	GPIOBNK3	GPIO
26	MMCINT0	MMC/SD0	58	GPIOBNK4	GPIO
27	MMCINT1	MMC/SC1	59	GPIOBNK5	GPIO
28	PWMINT3	PWM3	60	GPIOBNK6	GPIO
29	DDRINT	DDR EMIF	61	COMMTX	ARMSS
30	AEMIFINT	Async EMIF	62	COMMRX	ARMSS
31	SDIOINT1	SDIO1	63	EMUINT	E2ICE

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3.5 Device Clocking

3.5.1 Overview

The DM355 requires one primary reference clock . The reference clock frequency may be generated either by crystal input or by external oscillator. The reference clock is the clock at the pins named MXI1/MXO1. The reference clock drives two separate PLL controllers (PLLC1 and PLLC2). PLLC1 generates the clocks required by the ARM, MPEG4 and JPEG coprocessor, VPBE, VPSS, and peripherals. PLL2 generates the clock required by the DDR PHY. A block diagram of DM355's clocking architecture is shown in Figure 3-2. The PLLs are described further in Section 3.6.

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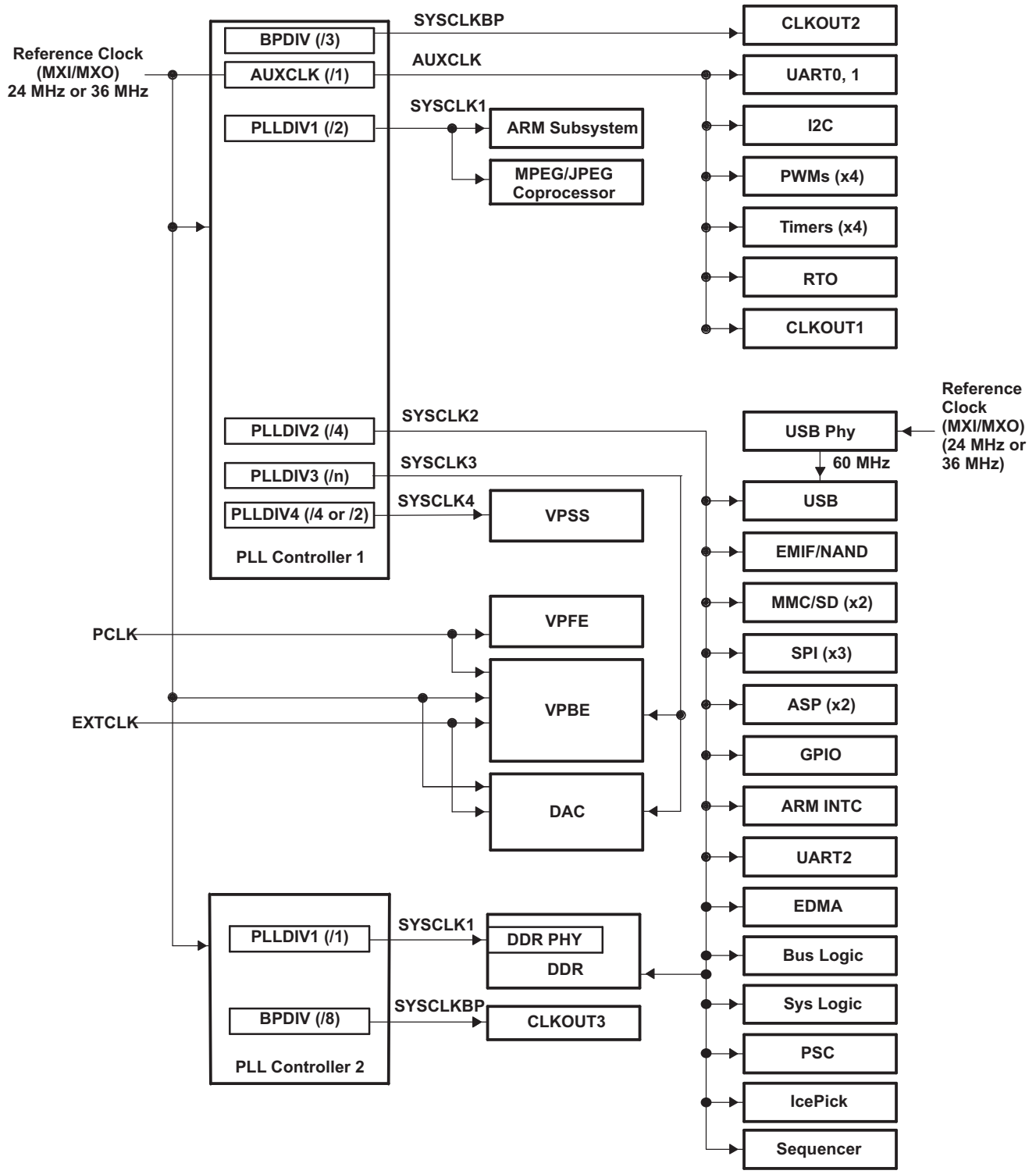

Figure 3-2. Device Clocking Block Diagram

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3.5.2 Supported Clocking Configurations for DM355-135

This section describes the only supported device clocking configurations for DM355-135. The DM355 supports either 24 MHz (typical) or 36 MHz reference clock (crystal or external oscillator input). Configurations are shown for both cases.

3.5.2.1 Supported Clocking Configurations for DM355-135 (24 MHz reference)

3.5.2.1.1 DM355-135 PLL1 (24 MHz reference)

All supported clocking configurations for DM355-135 PLL1 with 24 MHz reference clock are shown in Table 3-2.

Table 3-2. PLL1 Supported Clocking Configurations for DM355-135 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmable)	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	12	4	6	10	2.4	4	6
8	180	2	270	2	135	4	67.5	10	27	2	135
8	162	2	243	2	121.5	4	60.75	9	27	2	121.5
8	144	2	216	2	108	4	54	8	27	2	108
8	126	2	189	2	94.5	4	47.25	7	27	2	94.5
8	108	2	162	2	81	4	40.5	6	27	2	81

3.5.2.1.2 DM355-135 PLL2 (24 MHz reference)

All supported clocking configurations for DM355-135 PLL2 with 24 MHz reference clock are shown in Table 3-3.

Table 3-3. PLL2 Supported Clocking Configurations for DM355-135 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	24	12
12	133	1	266	1	266	133
12	100	1	200	1	200	100
15	100	1	160	1	160	80

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3.5.2.2 Supported Clocking Configurations for DM355-135 (36 MHz reference)

3.5.2.2.1 DM355-135PLL1 (36 MHz reference)

All supported clocking configurations for DM355-135 PLL1 with 36 MHz reference clock are shown in Table 3-4.

Table 3-4. PLL1 Supported Clocking Configurations DM355-135 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmable)	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	18	4	9	10	3.6	4	18
8	120	2	270	2	135	4	67.5	10	27	2	135
8	108	2	243	2	121.5	4	60.75	9	27	2	121.5
8	96	2	216	2	108	4	54	8	27	2	108

3.5.2.2.2 DM355-135 PLL2 (36 MHz reference)

All supported clocking configurations for DM355-135 PLL2 with 36 MHz reference clock are shown in Table 3-5.

Table 3-5. PLL2 Supported Clocking Configurations for DM355-135 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	36	18
18	133	1	266	1	266	133
27	150	1	200	1	200	100
27	120	1	160	1	160	80

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3.5.3 Supported Clocking Configurations for DM355-216

This section describes the only supported device clocking configurations for DM355-216. The DM355 supports either 24 MHz (typical) or 36 MHz reference clock (crystal or external oscillator input). Configurations are shown for both cases.

3.5.3.1 Supported Clocking Configurations for DM355-216 (24 MHz reference)

3.5.3.1.1 DM355-216 PLL1 (24 MHz reference)

All supported clocking configurations for DM355-216 PLL1 with 24 MHz reference clock are shown in Table 3-6.

Table 3-6. PLL1 Supported Clocking Configurations for DM355-216 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmable)	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	12	4	6	10	2.4	4	6
8	144	1	432	2	216	4	108	16	27	4	108
8	135	1	405	2	202.5	4	101.25	15	27	4	101.25
8	126	1	378	2	189	4	94.5	14	27	4	94.5
8	117	1	351	2	175.5	4	87.75	13	27	4	87.75
8	108	1	324	2	162	4	81	12	27	4	81
8	99	1	297	2	148.5	4	74.25	11	27	4	74.25
8	180	2	270	2	135	4	67.5	10	27	2	135
8	162	2	243	2	121.5	4	60.75	9	27	2	121.5
8	144	2	216	2	108	4	54	8	27	2	108
8	126	2	189	2	94.5	4	47.25	7	27	2	94.5
8	108	2	162	2	81	4	40.5	6	27	2	81

3.5.3.1.2 DM355-216 PLL2 (24 MHz reference)

All supported clocking configurations for DM355-216 PLL2 with 24 MHz reference clock are shown in Table 3-7.

Table 3-7. PLL2 Supported Clocking Configurations for DM355-216 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	24	12
8	114	1	342	1	342	171
8	108	1	324	1	324	162
8	102	1	306	1	306	153
8	96	1	288	1	288	144
12	133	1	266	1	266	133
12	100	1	200	1	200	100
15	100	1	160	1	160	80

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3.5.3.2 Supported Clocking Configurations for DM355-216 (36 MHz reference)

3.5.3.2.1 DM355-216 PLL1 (36 MHz reference)

All supported clocking configurations for DM355-216 PLL1 with 36 MHz reference clock are shown in Table 3-8.

Table 3-8. PLL1 Supported Clocking Configurations DM355-216 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmable)	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	18	4	9	10	3.6	4	9
8	96	1	432	2	216	4	108	16	27	4	108
8	180	2	405	2	202.5	4	101.25	15	27	4	101.25
8	168	2	378	2	189	4	94.5	14	27	4	94.5
8	156	2	351	2	175.5	4	87.75	13	27	4	87.75
8	144	2	324	2	162	4	81	12	27	4	81
8	132	2	297	2	148.5	4	74.25	11	27	4	74.25
8	120	2	270	2	135	4	67.5	10	27	2	135
8	108	2	243	2	121.5	4	60.75	9	27	2	121.5
8	96	2	216	2	108	4	54	8	27	2	108

3.5.3.2.2 DM355-216 PLL2 (36 MHz reference)

All supported clocking configurations for DM355-216 PLL2 with 36 MHz reference clock are shown in Table 3-9.

Table 3-9. PLL2 Supported Clocking Configurations for DM355-216 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	36	18
12	114	1	342	1	342	171
12	108	1	324	1	324	162
12	102	1	306	1	306	153
12	96	1	288	1	288	144
18	133	1	266	1	266	133
27	150	1	200	1	200	100
27	120	1	160	1	160	80

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3.5.4 Supported Clocking Configurations for DM355-270

This section describes the only supported device clocking configurations for DM355-270. The DM355 supports either 24 MHz (typical) or 36 MHz reference clock (crystal or external oscillator input). Configurations are shown for both cases.

Note : DM355-270 devices support only commercial temperature ranges.

3.5.4.1 Supported Clocking Configurations for DM355-270 (24 MHz reference)

3.5.4.1.1 DM355-270 PLL1 (24 MHz reference)

All supported clocking configurations for DM355-270 PLL1 with 24 MHz reference clock are shown in Table 3-10.

Table 3-10. PLL1 Supported Clocking Configurations for DM355-270 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmable)	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	12	4	6	10	2.4	4	6
8	180	1	540	2	270	4	135	20	27	4	135
8	171	1	513	2	256.5	4	128.25	19	27	4	128.25
8	162	1	486	2	243	4	121.5	18	27	4	121.5
8	153	1	459	2	229.5	4	114.75	17	27	4	114.75
8	144	1	432	2	216	4	108	16	27	4	108
8	135	1	405	2	202.5	4	101.25	15	27	4	101.25
8	126	1	378	2	189	4	94.5	14	27	4	94.5
8	117	1	351	2	175.5	4	87.75	13	27	4	87.75
8	108	1	324	2	162	4	81	12	27	4	81
8	99	1	297	2	148.5	4	74.25	11	27	4	74.25
8	180	2	270	2	135	4	67.5	10	27	2	135
8	162	2	243	2	121.5	4	60.75	9	27	2	121.5
8	144	2	216	2	108	4	54	8	27	2	108
8	126	2	189	2	94.5	4	47.25	7	27	2	94.5
8	108	2	162	2	81	4	40.5	6	27	2	81

3.5.4.1.2 DM355-270 PLL2 (24 MHz reference)

All supported clocking configurations for DM355-270 PLL2 with 24 MHz reference clock are shown in Table 3-11.

Table 3-11. PLL2 Supported Clocking Configurations for DM355-270 (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	24	12
8	144	1	432	1	432	216
8	138	1	414	1	414	207
8	132	1	396	1	396	198
8	126	1	378	1	378	189
8	120	1	360	1	360	180
8	114	1	342	1	342	171
8	108	1	324	1	324	162
8	102	1	306	1	306	153
8	96	1	288	1	288	144
12	133	1	266	1	266	133

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Table 3-11. PLL2 Supported Clocking Configurations for DM355-270 (24 MHz reference) (continued)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
12	100	1	200	1	200	100
15	100	1	160	1	160	80

3.5.4.1.3 DM355-27J PLL2 (24 MHz reference)

All supported clocking configurations for DM355-27J PLL2 with 24 MHz reference clock are shown in Table 3-12.

Table 3-12. PLL2 Supported Clocking Configurations for DM355-27J (24 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	24	12
8	132	1	396	1	396	198
8	126	1	378	1	378	189
8	120	1	360	1	360	180
8	114	1	342	1	342	171
8	108	1	324	1	324	162
8	102	1	306	1	306	153
8	96	1	288	1	288	144
12	133	1	266	1	266	133
12	100	1	200	1	200	100
15	100	1	160	1	160	80

3.5.4.2 Supported Clocking Configurations for DM355-270 (36 MHz reference)

3.5.4.2.1 DM355-270 PLL1 (36 MHz reference)

All supported clocking configurations for DM355-270 PLL1 with 36 MHz reference clock are shown in Table 3-13.

Table 3-13. PLL1 Supported Clocking Configurations for DM355-270 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL1 VCO	ARM / MPEG4 and JPEG Coprocessor		Peripherals		VENC		VPSS	
(/8 fixed)	(m programmable)	(/2 or /1 programmab	(MHz)	PLLDIV1 (/2 fixed)	SYSCLK1 (MHz)	PLLDIV2 (/4 fixed)	SYSCLK2 (MHz)	PLLDIV3 (/n programmable)	SYSCLK3 (MHz)	PLLDIV4 (/4 or /2 programmable)	SYSCLK4 (MHz)
bypass	bypass	bypass	bypass	2	18	4	9	10	3.6	4	18
8	120	1	540	2	270	4	135	20	27	4	135
8	114	1	513	2	256.5	4	128.25	19	27	4	128.25
8	108	1	486	2	243	4	121.5	18	27	4	121.5
8	102	1	459	2	229.5	4	114.75	17	27	4	114.75
8	96	2	432	2	216	4	108	16	27	4	108
8	180	2	405	2	202.5	4	101.25	15	27	2	202.5
8	168	2	378	2	189	4	94.5	14	27	2	189
8	156	2	351	2	175.5	4	87.75	13	27	2	175.5
8	144	2	324	2	162	4	81	12	27	2	162
8	132	2	297	2	148.5	4	74.25	11	27	2	148.5
8	120	2	270	2	135	4	67.5	10	27	2	135
8	108	2	243	2	121.5	4	60.75	9	27	2	121.5
8	96	2	216	2	108	4	54	8	27	2	108

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3.5.4.2.2 DM355-270 PLL2 (36 MHz reference)

All supported clocking configurations for DM355-270 PLL2 with 36 MHz reference clock are shown in Table 3-14.

Table 3-14. PLL2 Supported Clocking Configurations for DM355-270 (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	36	18
12	144	1	432	1	432	216
12	138	1	414	1	414	207
12	132	1	396	1	396	198
12	126	1	378	1	378	189
12	120	1	360	1	360	180
12	114	1	342	1	342	171
12	108	1	324	1	324	162
12	102	1	306	1	306	153
12	96	1	288	1	288	144
18	133	1	266	1	266	133
27	150	1	200	1	200	100
27	120	1	160	1	160	80

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3.5.4.2.3 DM355-27J PLL2 (36 MHz reference)

All supported clocking configurations for DM355-27J PLL2 with 36 MHz reference clock are shown in Table 3-15.

Table 3-15. PLL2 Supported Clocking Configurations for DM355-27J (36 MHz reference)

PREDIV	PLLM	POSTDIV	PLL2 VCO	DDR PHY		DDR Clock
(/n programmable)	(m programmable)	(/1 fixed)	(MHz)	PLLDIV1 (/1 fixed)	SYSCLK1 (MHz)	DDR_CLK (MHz)
bypass	bypass	bypass	bypass	1	36	18
12	132	1	396	1	396	198
12	126	1	378	1	378	189
12	120	1	360	1	360	180
12	114	1	342	1	342	171
12	108	1	324	1	324	162
12	102	1	306	1	306	153
12	96	1	288	1	288	144
18	133	1	266	1	266	133
27	150	1	200	1	200	100
27	120	1	160	1	160	80

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3.5.5 Peripheral Clocking Considerations

3.5.5.1 Video Processing Back End Clocking

The Video Processing Back End (VPBE) is a sub-module of the Video Processing Subsystem (VPSS).

The VPBE is designed to interface with a variety of LCDs and an internal DAC module. There are two asynchronous clock domains in the VPBE: an internal clock domain and an external clock domain. The internal clock domain is driven by the VPSS clock (PLL1 SYSCLK4). The external clock domain is configurable; you can select one of five source:

- 24 MHz crystal input at MXI1
- 27 MHz crystal input at MXI2 (optional feature, not typically used)
- PLL1 SYSCLK3
- EXTCLK pin (external VPBE clock input pin)
- PCLK pin (VPFE pixel clock input pin)

See the *TMS320DM35x Digital Media System-on-Chip Video Processing Back End (VPBE) Reference Guide* (literature number SPRUF72) for complete information on VPBE clocking.

3.5.5.2 USB Clocking

The USB Controller is driven by two clocks: an output clock of PLL1 (SYSCLK2) and an output clock of the USB PHY.

NOTE

For proper USB 2.0 function, SYSCLK2 must be greater than 60 MHz.

The USB PHY takes an input clock that is configurable by the USB PHY clock source bits (PHYCLKSRC) in the USB PHY control register (USB_PHY_CTL) in the System Control Module. When a 24 MHz crystal is used at MXI1/MXO1, set PHYCLKSRC to 0. This will present a 24 MHz clock to the USB PHY. When a 36 MHz crystal is used at MXI1/MXO1, set PHYCLKSRC to 1. This will present a 12 MHz clock (36 MHz divided internally by three) to the USB PHY. The USB PHY is capable of accepting only 24 MHz and 12 MHz; thus you must use either a 24 MHz or 36 MHz crystal at MXI1/MXO1. See the *TMS320DM355 DMSoC Universal Serial Bus (USB) Controller User's Guide* (literature number SPRUED2) for more information. See the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) for more information on the System Control Module.

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3.6 PLL Controller (PLLC)

This section describes the PLL Controllers for PLL1 and PLL2. See the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) for more information on the PLL controllers.

3.6.1 PLL Controller Module

The DM355 has two PLL controllers that provide clocks to different components of the chip. PLL controller 1 (PLLC1) provides clocks to most of the components of the chip. PLL controller 2 (PLLC2) provides clocks to the DDR PHY.

As a module, the PLL controller provides the following:

- Glitch-free transitions (on changing PLL settings)
- Domain clocks alignment
- Clock gating
- PLL bypass
- PLL power down

The various clock outputs given by the PLL controller are as follows:

- Domain clocks: SYSCLKn
- Bypass domain clock: SYSCLKBP
- Auxiliary clock from reference clock: AUXCLK

Various dividers that can be used are as follows:

- Pre-PLL divider: PREDIV
- Post-PLL divider: POSTDIV
- SYSCLK divider: PLLDIV1, …, PLLDIVn
- SYSCLKBP divider: BPDIV

Multipliers supported are as follows:

- PLL multiplier control: PLLM

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3.6.2 PLLC1

PLLC1 provides most of the DM355 clocks. Software controls PLLC1 operation through the PLLC1 registers. The following list, Table 3-16, and Figure 3-3 describe the customizations of PLLC1 in the DM355.

- Provides primary DM355 system clock
- Software configurable
- Accepts clock input or internal oscillator input
- PLL pre-divider value is fixed to (/8)
- PLL multiplier value is programmable
- PLL post-divider
- Only SYSCLK[4:1] are used
- SYSCLK1 divider value is fixed to (/2)
- SYSCLK2 divider value is fixed to (/4)
- SYSCLK3 divider value is programmable
- SYSCLK4 divider value is programmable to (/4) or (/2)
- SYSCLKBP divider value is fixed to (/3)
- SYSCLK1 is routed to the ARM Subsystem
- SYSCLK2 is routed to peripherals
- SYSCLK3 is routed to the VPBE module
- SYSCLK4 is routed to the VPSS module
- AUXCLK is routed to peripherals with fixed clock domain and also to the output pin CLKOUT1
- SYSCLKBP is routed to the output pin CLKOUT2

Table 3-16. PLLC1 Output Clocks

Output Clock	Used By	PLLDIV Divider	Notes
SYSCLK1	ARM Subsystem / MPEG4 and JPEG Coprocessor	/2	Fixed divider
SYSCLK2	Peripherals	/4	Fixed divider
SYSCLK3	VPBE (VENC module)	/n	Programmable divider (used to get 27 MHz for VENC)
SYSCLK4	VPSS	/4 or /2	Programmable divider
AUXCLK	Peripherals, CLKOUT1	none	No divider
SYSCLKBP	CLKOUT2	/3	Fixed divider

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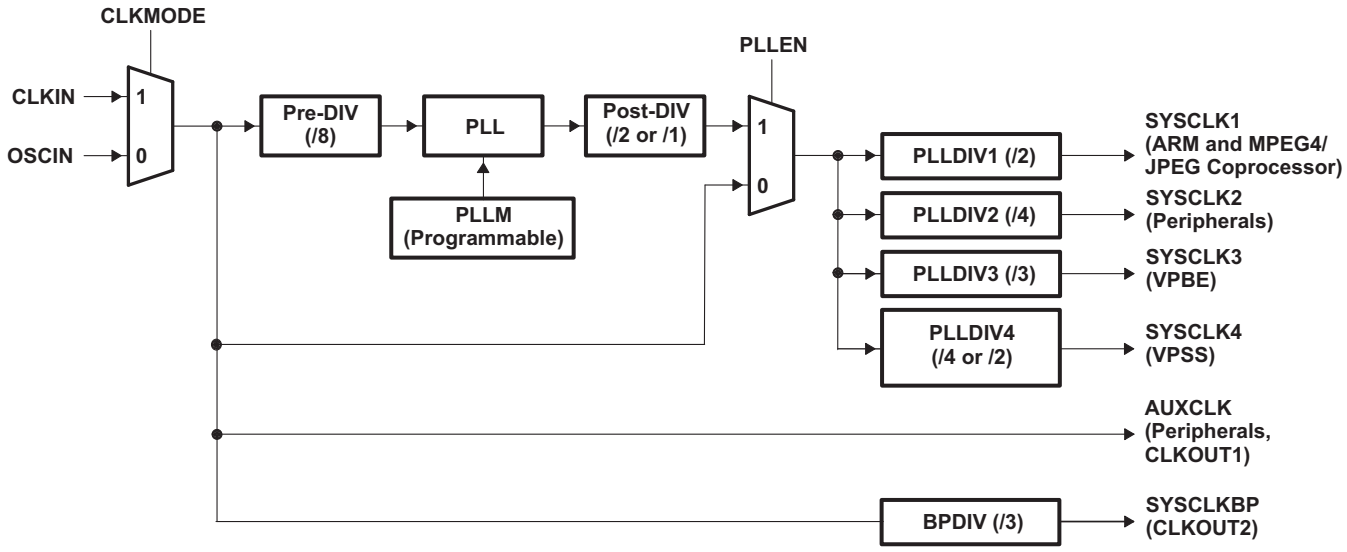

Figure 3-3. PLLC1 Configuration in DM355

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3.6.3 PLLC2

PLLC2 provides the DDR PHY clock and CLKOUT3. Software controls PLLC2 operation through the PLLC2 registers. The following list, Table 3-17, and Figure 3-4 describe the customizations of PLLC2 in the DM355.

- Provides DDR PHY clock and CLKOUT3
- Software configurable
- Accepts clock input or internal oscillator input (same input as PLLC1)
- PLL pre-divider value is programmable
- PLL multiplier value is programmable
- PLL post-divider value is fixed to (/1)
- Only SYSCLK[1] is used
- SYSCLK1 divider value is fixed to (/1)
- SYSCLKBP divider value is fixed to (/8)
- SYSCLK1 is routed to the DDR PHY
- SYSCLKBP is routed to the output pin CLKOUT3
- AUXCLK is not used.

Table 3-17. PLLC2 Output Clocks

Output Clock	Used by	PLLDIV Divider	Notes
SYSCLK1	DDR PHY	/1	Fixed divider
SYSCLKBP	CLKOUT3	/8	Fixed divider

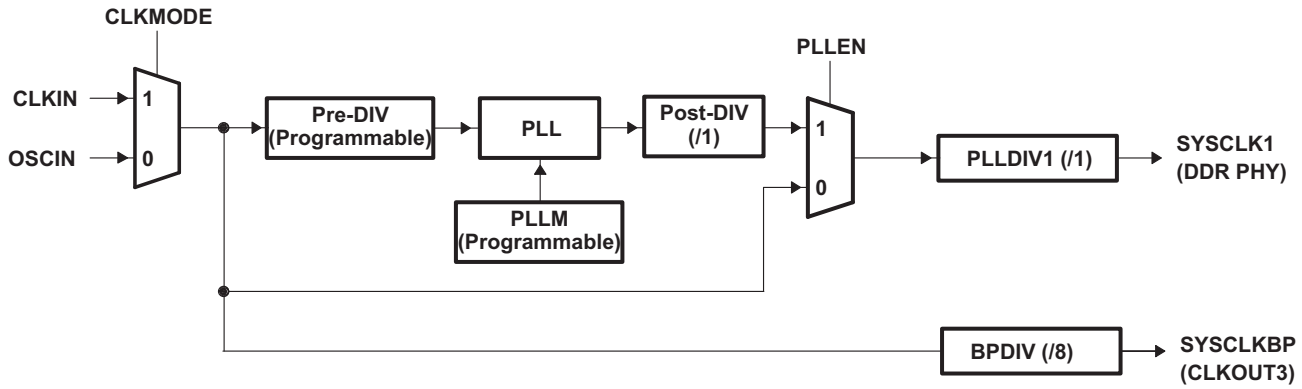

Figure 3-4. PLLC2 Configuration in DM355

3.7 Power and Sleep Controller (PSC)

In the DM355 system, the Power and Sleep Controller (PSC) is responsible for managing transitions of system power on/off, clock on/off, and reset. A block diagram of the PSC is shown in Figure 3-5. Many of the operations of the PSC are transparent to software, such as power-on-reset operations. However, the PSC provides you with an interface to control several important clock and reset operations.

The PSC includes the following features:

- Manages chip power-on/off, clock on/off, and resets
- Provides a software interface to:
  - Control module clock ON/OFF
  - Control module resets
- Supports IcePick emulation features: power, clock, and reset

For more information on the PSC, see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) .

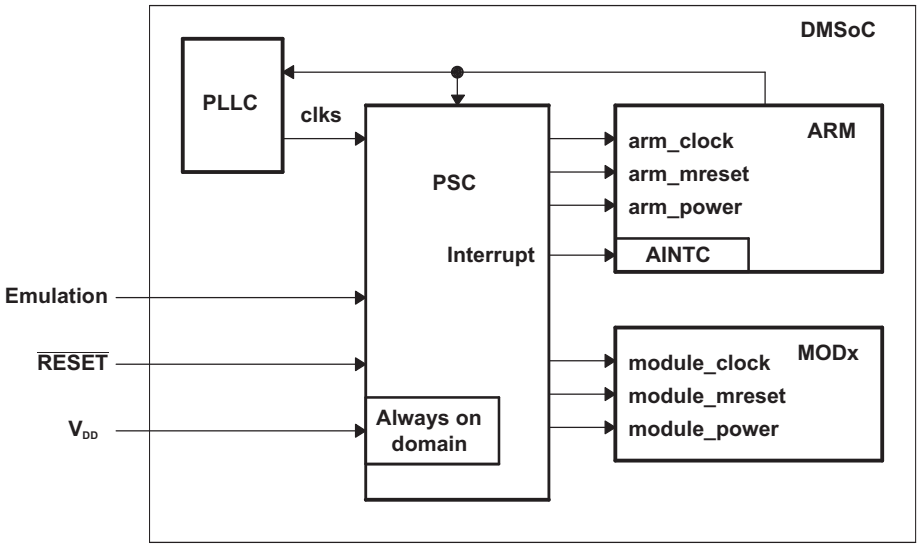

Figure 3-5. DM355 Power and Sleep Controller (PSC)

3.8 System Control Module

The DM355's system control module is a system-level module containing status and top-level control logic required by the device. The system control module consists of a miscellaneous set of status and control registers, accessible by the ARM and supporting all of the following system features and operations:

- Device identification
- Device configuration
  - Pin multiplexing control
  - Device boot configuration status
- ARM interrupt and EDMA event multiplexing control
- Special peripheral status and control
  - Timer64+
  - USB PHY control
  - VPSS clock and video DAC control and status
  - DDR VTP control
  - Clockout circuitry
  - GIO de-bounce control

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- Power management
  - Deep sleep mode
- Bandwidth Management
  - Bus master DMA priority control

  For more information on the System Control Module refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) .

3.9 Pin Multiplexing

The DM355 makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. In order to accomplish this, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and software control. No attempt is made by the DM355 hardware to ensure that the proper pin muxing has been selected for the peripherals or interface mode being used, thus proper pin muxing configuration is the responsibility of the board and software designers. An overview of the pin multiplexing is shown in Table 3-18.

Table 3-18. Peripheral Pin Mux Overview

Peripheral	Muxed With	Primary Function	Secondary Function	Tertiary Function
VPFE (video in)	GPIO and SPI2	VPFE (video in)	SPI2	GPIO
VPBE (video out)	GPIO, PWM, and RTO	VPBE (video out)	PWM and RTO	GPIO
AEMIF	GPIO	AEMIF	GPIO	none
ASP0	GPIO	ASP0	GPIO	none
MMC/SD1	GPIO and UART2	MMC/SD1	GPIO	UART2
CLKOUT	GPIO	CLKOUT	GPIO	none
I2C	GPIO	I2C	GPIO	none
UART1	GPIO	UART1	GPIO	none
SPI1	GPIO	SPI1	GPIO	none
SPI0	GPIO	SPI0	GPIO	none

3.9.1 *Hardware Controlled Pin Multiplexing*

Use the Asynchronous EMIF configuration pins (AECFG[3:0]) for hardware pin mux control. AECFG[3:0] control the partitioning of the AEMIF addresses and GPIOs at reset, which allows you to properly configure the number of AEMIF address pins required by the boot device while unused addresses pins are available as GPIOs. These settings may be changed by software after reset by programming the PinMux2 register The PinMux2 register is in the System Control Module. As shown in Table 3-19, the number of address bits enabled on the AEMIF is selectable from 0 to 16. Pins that are not assigned to another peripheral and not enabled as address signals become GPIOs (except EM_A[2:1]). The enabled address signals are always contiguous from EM_BA[1] upwards; bits cannot be skipped. The exception to this are EM_A[2:1]. These signals (can be used to) represent the ALE and CLE signals for the NAND Flash mode of the AEMIF and are always enabled. Note that EM_A[0] does not represent the lowest AEMIF address bit. DM355 supports only 16-bit and 8-bit data widths for the AEMIF. In 16-bit mode, EM_BA[1] represents the LS address bit (the half-word address) and EM_BA[0] represents the MS address bit (A[14]). In 8-bit mode, EM_BA[1:0] represent the 2 LS address bits. Note that additional selections are available by programming the PinMux2 register in software after boot. Note that AECFG selection of '0010' selects OneNAND interface. The AEMIF needs to operate in the half-rate mode (full_rate = 0) to meet frequency requirements. Software should not change the PINMUX2 register setting to affect the AEMIF rate operation. A soft reset of the AEMIF should be performed any time a rate change is made.

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Table 3-19. AECFG (Async EMIF Configuration) Pin Mux Coding

1101(NAND)	1100	1010	1000 (8-bit SRAM)	0010 (16-bit SRAM, OneNAND)	0000
GPIO[54]	GPIO[54]	EM_A[14]	EM_BA[0]	EM_A[14]	EM_BA[0]
GPIO[55]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]	EM_BA[1]
GPIO[56]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]	EM_A[0]
EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]	EM_A[1]
EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]	EM_A[2]
GPIO[57]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]	EM_A[3]
GPIO[58]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]	EM_A[4]
GPIO[59]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]	EM_A[5]
GPIO[60]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]	EM_A[6]
GPIO[61]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]	EM_A[7]
GPIO[62]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]	EM_A[8]
GPIO[63]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]	EM_A[9]
GPIO[64]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]	EM_A[10]
GPIO[65]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]	EM_A[11]
GPIO[66]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]	EM_A[12]
GPIO[67]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]	EM_A[13]
GPIO[46]	GPIO[46]	GPIO[46]	GPIO[46]	EM_D[8]	EM_D[8]
GPIO[47]	GPIO[47]	GPIO[47]	GPIO[47]	EM_D[9]	EM_D[9]
GPIO[48]	GPIO[48]	GPIO[48]	GPIO[48]	EM_D[10]	EM_D[10]
GPIO[49]	GPIO[49]	GPIO[49]	GPIO[49]	EM_D[11]	EM_D[11]
GPIO[50]	GPIO[50]	GPIO[50]	GPIO[50]	EM_D[12]	EM_D[12]
GPIO[51]	GPIO[51]	GPIO[51]	GPIO[51]	EM_D[13]	EM_D[13]
GPIO[52]	GPIO[52]	GPIO[52]	GPIO[52]	EM_D[14]	EM_D[14]
GPIO[53]	GPIO[53]	GPIO[53]	GPIO[53]	EM_D[15]	EM_D[15]

3.9.2 Software Controlled Pin Multiplexing

All pin multiplexing options are configurable by software via pin mux registers that reside in the System Control Module. The PinMux0 Register controls the Video In muxing, PinMux1 register controls Video Out signals, PinMux2 register controls AEMIF signals, PinMux3 registers control the multiplexing of the GIO signals, the PinMux4 register controls the SPI and MMC/SD0 signals. Refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature numberSPRUFB3) for complete descriptions of the pin mux registers.

3.10 Device Reset

There are five types of reset in DM355. The types of reset differ by how they are initiated and/or by their effect on the chip. Each type is briefly described in Table 3-20 and further described in *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3).

Table 3-20. Reset Types

Type	Initiator	Effect
POR (Power-On-Reset)	$\overline{\text{RESET}}$ pin low and $\overline{\text{TRST}}$ low	Total reset of the chip (cold reset). Resets all modules including memory and emulation.
Warm Reset	$\overline{\text{RESET}}$ pin low and $\overline{\text{TRST}}$ high (initiated by ARM emulator).	Resets all modules including memory, except ARM emulation.
Max Reset	ARM emulator or Watchdog Timer (WDT).	Same effect as warm reset.

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Table 3-20. Reset Types (continued)

Type	Initiator	Effect
System Reset	ARM emulator	Resets all modules except memory and ARM emulation. It is a soft reset that maintains memory contents and does not affect or reset clocks or power states.
Module Reset	ARM software	Resets a specific module. Allows the ARM to independently reset any module. Module reset is intended as a debug tool not as a tool to use in production.

3.11 Default Device Configurations

After POR, warm reset, and max reset, the chip is in its default configuration. This section highlights the default configurations associated with PLLs, clocks, ARM boot mode, and AEMIF.

NOTE

Default configuration is the configuration immediately after POR, warm reset, and max reset and just before the boot process begins. The boot ROM updates the configuration. See Section 3.12 for more information on the boot process.

3.11.1 Device Configuration Pins

The device configuration pins are described in Table 3-21. The device configuration pins are latched at reset and allow you to configure all of the following options at reset:

- ARM Boot Mode
- Asynchronous EMIF pin configuration

These pins are described further in the following sections.

NOTE

The device configuration pins are multiplexed with AEMIF pins. After the device configuration pins are sampled at reset, they automatically change to function as AEMIF pins. Pin multiplexing is described in Section 3.8.

Table 3-21. Device Configuration

Device Configuration Input	Function	Sampled Pin	Default Setting (by internal pull-up/ pull-down)	Device Configuration Affected
BTSEL[1:0]	Selects ARM boot mode 00 = Boot from ROM (NAND with SPI EEPROM boot option) 01 = Boot from AEMIF 10 = Boot from ROM (MMC/SD) 11 = Boot from ROM (UART)	EM_A[13:12]	00 (NAND)	If any ROM boot mode is selected, GIO61 is used to indicated boot status. If NAND boot is selected, CE0 is used for NAND and SPI0 is used for SPI boot option. Use AECFG[3:0] to configure AEMIF pins for NAND. If AEMIF boot is selected, CE0 is used for AEMIF device (OneNAND, ROM). Use AECFG[3:0] to configure AEMIF pins for NAND. If MMC/SD boot is selected, MMC/SD0 is used.
AECFG[3:0]	Selects AEMIF pin configuration	EM_A[11:8]	1101 (NAND)	Selects the AEMIF pin configuration. Refer to pin-muxing information in Section 3.9.1. Note that AECFG[3:0] affects both AEMIF (BTSEL[1:0]=01) and NAND (BTSEL[1:0]=00) boot modes.

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3.11.2 PLL Configuration

After POR, warm reset, and max reset, the PLLs and clocks are set to their default configurations. The PLLs are in bypass mode and disabled by default. This means that the input reference clock at MXI1 (typically 24 MHz) drives the chip after reset. For more information on device clocking, see Section 3.5 and Section 3.6. The default state of the PLLs is reflected in the default state of the register bits in the PLLC registers. Refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) for PLLC register descriptions.

3.11.3 Power Domain and Module State Configuration

Only a subset of modules are enabled after reset by default. Table 3-22 shows which modules are enabled after reset. Table 3-22 as shows that the following modules are enabled depending on the sampled state of the device configuration pins: EDMA (CC, TC0 and TC1), AEMIF, MMC/SD0, UART0, and Timer0. For example, UART0 is enabled after reset when the device configuration pins (BTSEL[1:0] = 11 - Enable UART) select UART boot mode. For more information on module configuration refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3).

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Table 3-22. Module Configuration

Module Number	Module Name	Power Domain	Default States	
			Power Domain State	Module State
0	VPSS Master	AlwaysOn	ON	SyncRst
1	VPSS Slave	AlwaysOn	ON	SyncRst
2	EDMA (CC)	AlwaysOn	ON	BTSEL[1:0] = 00 – Enable (NAND, SPI) BTSEL[1:0] = 01 – Enable (OneNAND) BTSEL[1:0] = 10 – SyncRst (MMC/SD) BTSEL[1:0] = 11 – Enable (UART)
3	EDMA (TC0)	AlwaysOn	ON	
4	EDMA (TC1)	AlwaysOn	ON	
5	Timer3	AlwaysOn	ON	SyncRst
6	SPI1	AlwaysOn	ON	SyncRst
7	MMC/SD1	AlwaysOn	ON	SyncRst
8	ASP1	AlwaysOn	ON	SyncRst
9	USB	AlwaysOn	ON	SyncRst
10	PWM3	AlwaysOn	ON	SyncRst
11	SPI2	AlwaysOn	ON	SyncRst
12	RTO	AlwaysOn	ON	SyncRst
13	DDR EMIF	AlwaysOn	ON	SyncRst
14	AEMIF	AlwaysOn	ON	BTSEL[1:0] = 00 – Enable (NAND, SPI) BTSEL[1:0] = 01 – Enable (OneNAND) BTSEL[1:0] = 10 – SyncRst (MMC/SD) BTSEL[1:0] = 11 – Enable (UART)
15	MMC/SD0	AlwaysOn	ON	BTSEL[1:0] = 00 – SyncRst (NAND, SPI) BTSEL[1:0] = 01 – SyncRst (OneNAND) BTSEL[1:0] = 10 – Enable (MMC/SD) BTSEL[1:0] = 11 – SyncRst (UART)
16	Reserved	Reserved	Reserved	Reserved
17	ASP	AlwaysOn	ON	SyncRst
18	I2C	AlwaysOn	ON	SyncRst
19	UART0	AlwaysOn	ON	BTSEL[1:0] = 00 – SyncRst (NAND, SPI) BTSEL[1:0] = 01 – SyncRst (OneNAND) BTSEL[1:0] = 10 – SyncRst (MMC/SD) BTSEL[1:0] = 11 – Enable (UART)
20	UART1	AlwaysOn	ON	SyncRst
21	UART2	AlwaysOn	ON	SyncRst
22	SPI0	AlwaysOn	ON	BTSEL[1:0] = 00 – Enable (NAND, SPI) BTSEL[1:0] = 01 – SyncRst (OneNAND) BTSEL[1:0] = 10 – Enable (MMC/SD) BTSEL[1:0] = 11 – Enable (UART)
23	PWM0	AlwaysOn	ON	SyncRst
24	PWM1	AlwaysOn	ON	SyncRst
25	PWM2	AlwaysOn	ON	SyncRst
26	GPIO	AlwaysOn	ON	SyncRst
27	TIMER0	AlwaysOn	ON	BTSEL[1:0] = 00 – Enable (NAND, SPI) BTSEL[1:0] = 01 – Enable (OneNAND) BTSEL[1:0] = 10 – Enable (MMC/SD) BTSEL[1:0] = 11 – Enable (UART)
28	TIMER1	AlwaysOn	ON	SyncRst

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Table 3-22. Module Configuration (continued)

			Default States	
29	TIMER2	AlwaysOn	ON	Enable
30	System Module	AlwaysOn	ON	Enable
31	ARM	AlwaysOn	ON	Enable
32	BUS	AlwaysOn	ON	Enable
33	BUS	AlwaysOn	ON	Enable
34	BUS	AlwaysOn	ON	Enable
35	BUS	AlwaysOn	ON	Enable
36	BUS	AlwaysOn	ON	Enable
37	BUS	AlwaysOn	ON	Enable
38	BUS	AlwaysOn	ON	Enable
39	Reserved	Reserved	Reserved	Reserved
40	VPSS DAC	Always On	ON	SyncRst

3.11.4 ARM Boot Mode Configuration

The input pins BTSEL[1:0] determine whether the ARM will boot from its ROM or from the Asynchronous EMIF (AEMIF). When ROM boot is selected (BTSEL[1:0] = 00, 10, or 11), a jump to the start of internal ROM (address 0x0000: 8000) is forced into the first fetched instruction word. The embedded ROM boot loader code (RBL) then performs certain configuration steps, reads the BOOTCFG register to determine the desired boot method, and branches to the appropriate boot routine (i.e., a NAND/SPI, MMC/SD, or UART loader routine).

If AEMIF boot is selected (BTSEL[1:0] = 01), a jump to the start of AEMIF (address 0x0200: 0000) is forced into the first fetched instruction word. The ARM then continues executing from external asynchronous memory using the default AEMIF timings until modified by software.

NOTE

For AEMIF boot, the OneNAND must be connected to the first AEMIF chip select space (EM_CE0). Also, the AEMIF does not support direct execution from NAND Flash.

Boot modes are further described in Section 3.12.

3.11.5 AEMIF Configuration

3.11.5.1 AEMIF Pin Configuration

The input pins AECFG[3:0] determine the AEMIF configuration immediately after reset. Use AECFG[3:0] to properly configure the pins of the AEMIF. Refer to the section on pin multiplexing in Section 3.9.

Also, see the *Asynchronous External Memory Interface (AEMIF) Peripheral Reference Guide* (literature number SPRUED1) for more information on the AEMIF.

3.11.5.2 AEMIF Timing Configuration

When AEMIF is enabled, the wait state registers are reset to the slowest possible configuration, which is 88 cycles per access (16 cycles of setup, 64 cycles of strobe, and 8 cycles of hold). Thus, with a 24 MHz clock at MXI1, the AEMIF is configured to run at 6 MHz/88 which equals approximately 68 kHz by default. See the *Asynchronous External Memory Interface (AEMIF) Peripheral Reference Guide* (literature number SPRUED1) for more information on the AEMIF.

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3.12 Device Boot Modes

The DM355 ARM can boot from either Async EMIF (AEMIF/OneNand) or from ARM ROM, as determined by the setting of the device configuration pins BTSEL[1:0]. The BTSEL[1:0] pins can define the ROM boot mode further as well.

The boot selection pins (BTSEL[1:0]) determine the ARM boot process. After reset (POR, warm reset, or max reset), ARM program execution begins in ARM ROM at 0x0000: 8000, except when BTSEL[1:0] = 01, indicating AEMIF (AEMIF/OneNand) boot. See Section 3.11.1 for information on the boot selection pins.

3.12.1 Boot Modes Overview

DM355's ARM ROM boot loader (RBL) executes when the BTSEL[1:0] pins indicate a condition other than the normal ARM EMIF boot.

- If BTSEL[1:0] = 01 - Asynchronous EMIF (AEMIF) boot. This mode is handled by hardware control and does not involve the ROM. In the case of OneNAND, the user is responsible for putting any necessary boot code in the OneNAND's boot page. This code shall configure the AEMIF module for the OneNAND device. After the AEMIF module is configured, booting will continue immediately after the OneNAND's boot page with the AEMIF module managing pages thereafter.
- The RBL supports 3 distinct boot modes:
  - BTSEL[1:0] = 00 - ARM NAND/SPI Boot
  - BTSEL[1:0] = 10 - ARM MMC/SD Boot
  - BTSEL[1:0] = 11 - ARM UART Boot
- In NAND mode if SPI boot fails, then NAND mode is tried. If NAND boot fails, then MMC/SD mode is tried.
- If MMC/SD boot fails, then MMC/SD boot is tried again.
- If UART boot fails, then UART boot is tried again.
- RBL uses GIO61 to indicate boot status (can use to blink LED):
  - After reset, GIO61 is initially driven low (e.g LED off)
  - If NAND boot fails, then GIO61 shall toggle at 4Hz while MMC/SD boot is tried.
  - If MMC/SD boot fails, then GIO61 shall toggle at 4Hz while MMC/SD boot is retried.
  - If UART boot fails, then GIO61 shall toggle at 2Hz while UART boot is retried.
  - When boot is successful, just before program control is given to UBL, GIO61 is driven high (e.g. LED on)
  - DM355 Timer0 shall be used to accurately toggle GIO61 at 4Hz and 2Hz
- ARM ROM Boot - SPI boot in NAND Mode
  - No support for a full firmware boot. Instead, copies a second stage User Boot Loader (UBL) from SPI to ARM Internal RAM (AIM) and transfers control to the user software.
  - Support for 16 and 24 bit SPI EEPROMs
  - Support for up to 30KB UBL (32KB - ~2KB for RBL stack)
  - RBL will copy UBL to ARM Internal RAM (AIM) via SPI interface from a SPI peripheral like SPI EEPROM. RBL will then transfer control to the UBL.
- ARM ROM Boot - NAND Mode (See Section 3.12.2 for a full explanation of the differences between Standard Mode and Compatibility Mode.):
  - No support for a full firmware boot. Instead, copies a second stage User Boot Loader (UBL) from NAND flash to ARM internal RAM (AIM) and transfers control to the user-defined UBL.
  - Support for NAND with page sizes up to 8192 bytes in Standard Mode and 2048 bytes in Compatibility Mode
    Note: At the time of documentation for this device, 8192-byte devices were not available for testing. The code does contain support for these devices; however, it has not yet been tested.
  - Support for magic number error detection and retry (up to 24 times) when loading UBL
  - Support for up to 30KB UBL (32KB IRAM - ~2KB for RBL stack)

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  - Optional, user-selectable, support for use of DMA and I-cache during RBL execution (i.e.,while loading UBL)
  - Supports booting from 8-bit NAND devices (16-bit NAND devices are not supported)
  - Uses/Requires 4-bit HW ECC (NAND devices with ECC requirements ≤ 4 bits per 512 bytes are supported)
  - Supports NAND flash that requires chip select to stay low during the tR read time

  Notes:
  - See Section 3.12.2 for a full explanation of the differences between Standard Mode and Compatibility Mode.
  - The GIO000 pin ***must*** be held high during NAND boot for the boot process to fuction properly.
- ARM ROM Boot - MMC/SD Mode
  - No support for a full firmware boot. Instead, copies a second stage User Boot Loader (UBL) from MMC/SD to ARM Internal RAM (AIM) and transfers control to the user software.
  - Support for MMC/SD Native protocol (MMC/SD SPI protocol is not supported)
  - Support for descriptor error detection and retry (up to 24 times) when loading UBL
  - Support for up to 30KB UBL (32KB - ~2KB for RBL stack)
- ARM ROM Boot - UART mode
  - No support for a full firmware boot. Instead, loads a second stage User Boot Loader (UBL) via UART to ARM internal RAM (AIM) and transfers control to the user software.
  - Support for up to 30KB UBL (32KB - ~2KB for RBL stack)

The general boot sequence is shown in Figure 3-6. For more information, refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3).

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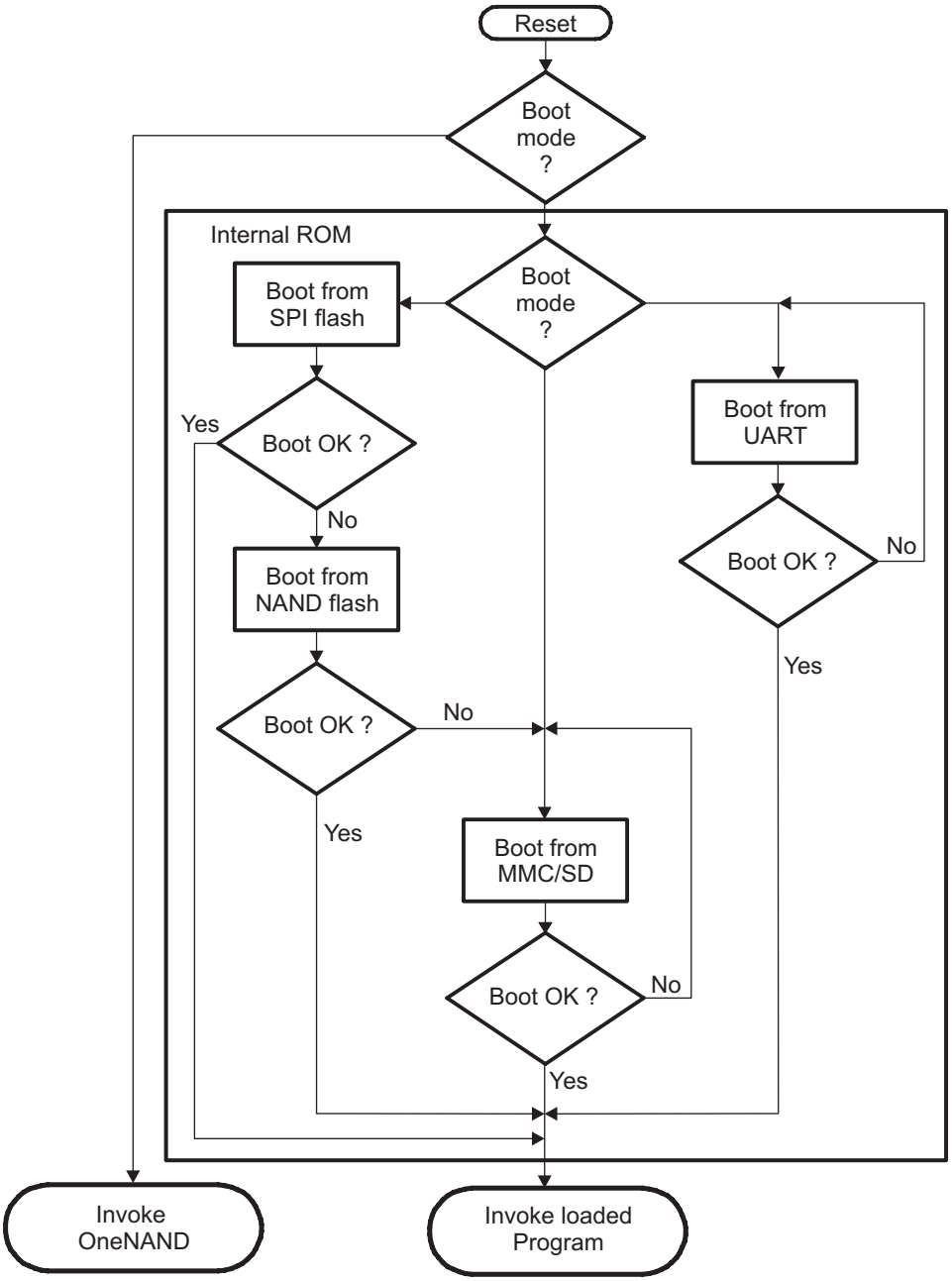

Figure 3-6. Boot Mode Functional Block Diagram

3.12.2 RBL NAND Boot Process

The RBL NAND boot process is described as follows:

- Upon NAND boot, if a SPI EEPROM is present, RBL reads first 32 bytes and look for magic pattern at offset 0x8. This magic number indicates if this is a SPI boot or beginning of NAND parameters.
- If SPI boot, then NAND boot is bypassed.
- Otherwise NAND boot is continued. If NAND parameters are found in the SPI EEPROM (as indicated by magic number), these parameters are used.
- Else the following steps are used to determine NAND parameters:
  - If the device is ONFI, read the parameters page. Else command is sent to the NAND device requesting four bytes (called the NAND READ_ID) which contain the manufacturer, device and 4th

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ID.

- The RBL contains an internal table with a list of known NAND devices. Table 3-23 shows the devices contained in the tables.
- If the device ID is not found in the table, then the RBL use the fourth byte of the NAND to decode this to obtain the necessary parameters.

- Once a device ID is identified, the first 24 blocks of the NAND are read sequentially starting with page 0 with an offset of 512 bytes. The purpose of the read is to locate a magic number which will identify the revision of the silicon. Table 3-24 contains magic numbers and their functions.
- If a Compatibility mode magic number is read, then the device enters compatibility mode. In compatibility mode, NAND layout is identical to that used in previous revisions of the silicon as shown in Table 3-25. Only 512-byte small blocks and 2048-byte big blocks are supported.
- If a Standard mode magic number is read, the NAND layout is as shown in Table 3-26: 512-bytes small block and 2048- and 4096- big block devices are supported. 8192-block devices are also supported. **Note**: At the time of production of this document revision, only 4096-block devices were available for testing.
- Once a magic number is identified, the User Boot Loader (UBL) is loaded from the NAND, stored to internal RAM, and executed.

Table 3-23. NAND Devices in NAND Device ID Table

DEVICE ID	PAGES PER BLOCK	BYTES PER PAGE	BLOCK SHIFT VALUE FOR ADDRESS	NUMBER OF ADDRESS CYCLES
0xE3	16	512+16	12	3
0xE5	16	512+16	12	3
0xE6	16	512+16	12	3
0x39(1)	16	512+16	13	3
0x6B	16	512+16	13	3
0x73	32	512+16	13	3
0x33	32	512+16	13	3
0x75	32	512+16	13	3
0x35	32	512+16	13	3
0x43	32	512+16	13	4
0x45	32	512+16	13	4
0x53	32	512+16	13	4
0x55	32	512+16	13	4
0x76	32	512+16	13	4
0x36	32	512+16	13	4
0x79	32	512+16	13	4
0x71	32	512+16	13	4
0x46	32	512+16	13	4
0x56	32	512+16	13	4
0x74	32	512+16	13	4
0xF1	64	2048+64	22	4
0xA1	64	2048+64	22	4
0xAA	64	2048+64	22	5
0xDA	64	2048+64	22	5
0xAC	64	2048+64	22	5
0xDC	64	2048+64	22	5
0xB1	64	2048+64	22	5
0xC1	64	2048+64	22	5

(1) Present only on silicon revision 1.1.

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Table 3-24. UBL Signature and Special Modes for NAND Boot Mode

MODE	VALUE(1)	DESCRIPTION
UBL_MAGIC_SAFE	0xA1AC ED00	Safe boot mode
UBL_MAGIC_DMA	0xA1AC ED11	DMA boot mode
UBL_MAGIC_IC	0xA1AC ED22	I Cache boot mode
UBL_MAGIC_FAST	0xA1AC ED33	Fast EMIF boot mode
UBL_MAGIC_DMA_IC	0xA1AC ED44	DMA + I Cache boot mode
UBL_MAGIC_DMA_IC_FAST	0xA1AC ED55	DMA + I Cache + Fast EMIF boot mode
UBL_MAGIC_SPI_PARAMS	0xA1AC EDAA	NAND parameters from SPI EEPROM

(1) The values listed only apply when operating in compatibility mode. These values follow the form 0xA1BCEDxx when operating in standard mode.
Example: UBL_MAGIC_SAFE VALUE = 0xA1ACED00; Safe boot mode will configure the device to run in safe boot mode and in compatibility mode. However, when using standard mode, the value should be 0xA1BCD00.

Table 3-25. NAND Layout (Compatibility Mode)

512 Byte Page Size	2048 Byte Page Size
512 bytes Data	512 bytes Data
16 bytes ECC Data	16 bytes ECC Data
	512 bytes Data
	16 bytes ECC Data
	512 bytes Data
	16 bytes ECC Data
	512 bytes Data
	16 bytes ECC Data

Table 3-26. NAND Layout (Standard Mode)

512 Byte Page Size	2048 Byte Page Size	4096 Byte Page Size
512 bytes Data	2048 bytes Data	4096 bytes Data
16 bytes ECC Data	64 bytes ECC Data	128 bytes ECC Data

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3.13 Power Management

The DM355 is designed for minimal power consumption. There are two components to power consumption: active power and leakage power. Active power is the power consumed to perform work and scales with clock frequency and the amount of computations being performed. Active power can be reduced by controlling the clocks in such a way as to either operate at a clock setting just high enough to complete the required operation in the required timeline or to run at a clock setting until the work is complete and then drastically cut the clocks (e.g. to PLL Bypass mode) until additional work must be performed. Leakage power is due to static current leakage and occurs regardless of the clock rate. Leakage, or standby power, is unavoidable while power is applied and scales roughly with the operating junction temperatures. Leakage power can only be avoided by removing power completely from a device or subsystem. The DM355 includes several power management features which are briefly described in Table 3-17. Refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) for more information on power management.

Table 3-27. Power Management Features

Power Management Features	Description
Clock Management	
Module clock disable	Module clocks can be disabled to reduce switching power
Module clock frequency scaling	Module clock frequency can be scaled to reduce switching power
PLL power-down	The PLLs can be powered-down when not in use to reduce switching power
ARM Sleep Mode	
ARM Wait-for-Interrupt sleep mode	Disable ARM clock to reduce active power
System Sleep Modes	
Deep Sleep mode	Stop all device clocks and power down internal oscillators to reduce active power to a minimum. Registers and memory are preserved.
I/O Management	
USB Phy power-down	The USB Phy can be powered-down to reduce USB I/O power
DAC power-down	The DAC's can be powered-down to reduce DAC power
DDR self-refresh and power down	The DDR / mDDR device can be put into self-refresh and power down states

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3.14 64-Bit Crossbar Architecture

The DM355 uses a 64-bit crossbar architecture to control access between device processors, subsystems and peripherals. It includes an EDMA Controller consisting of a DMA Transfer Controller (TC) and a DMA Channel Controller (CC). The TC provides two DMA channels for transfer between slave peripherals. The CC provides a user and event interface to the EDMA system. It includes up to 64 event channels to which all system synchronization events can be mapped and 8 auto submit “quick” channels (QDMA). In most ways, these channels are identical. A channel refers to a specific ‘event’ that can cause a transfer to be submitted to the TC as a Transfer Request.

3.14.1 Crossbar Connections

There are five transfer masters (TCs have separate read and write connections) connected to the crossbar; ARM, the Video Processing Sub-system (VPSS), the master peripherals (USB), and two EDMA transfer controllers. These can be connected to four separate slave ports; ARM, the DDR EMIF, and CFG bus peripherals. Not all masters may connect to all slaves. Connection paths are indicated by √ at intersection points shown in Table 3-28

Table 3-28. Crossbar Connection Matrix

	Slave Module			
DMA Master	ARM Internal Memory	MPEG4/JPEG Coprocessor Memory	Config Bus Registers and Memory	DDR EMIF Memory
ARM	√	√	√	√
VPSS				√
DMA Master Peripherals (USB)	√		√	√
EDMA3TC0	√	√	√	√
EDMA3TC1	√	√	√	√

3.14.2 EDMA Controller

The EDMA controller handles all data transfers between memories and the device slave peripherals on the DM355 device. These are summarized as follows:

- Transfer to/from on-chip memories
  - ARM program/data RAM
  - MPEG4/JPEG Coprocessor memory
- Transfer to/from external storage
  - DDR2 / mDDR SDRAM
  - Asynchronous EMIF
  - OneNAND flash
  - NAND flash
  - Smart Media, SD, MMC, xD media storage
- Transfer to/from peripherals
  - ASP
  - SPI
  - I2C
  - PWM
  - RTO
  - GPIO
  - Timer/WDT
  - UART
  - MMC/SD

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The EDMA Controller consists of two major blocks: the Transfer Controller (TC) and the Channel Controller (CC). The CC is a highly flexible Channel Controller that serves as the user interface and event interface for the EDMA system. The CC supports 64-event channels and 8 QDMA channels. The CC consists of a scalable Parameter RAM (PaRAM) that supports flexible ping-pong, circular buffering, channel-chaining, auto-reloading, and memory protection.

The EDMA Channel Controller has the following features:

- Fully orthogonal transfer description
  - Three transfer dimensions
  - A-synchronized transfers: one dimension serviced per event
  - AB- synchronized transfers: two dimensions serviced per event
  - Independent indexes on source and destination
  - Chaining feature allows 3-D transfer based on single event
- Flexible transfer definition
  - Increment and constant addressing modes
  - Linking mechanism allows automatic PaRAM set update
  - Chaining allows multiple transfers to execute with one event
- Interrupt generation for:
  - DMA completion
  - Error conditions
- Debug visibility
  - Queue watermarking/threshold
  - Error and status recording to facilitate debug
- 64 DMA channels
  - Event synchronization
  - Manual synchronization (CPU(s) write to event set register)
  - Chain synchronization (completion of one transfer chains to next)
- 8 QDMA channels
  - QDMA channels are triggered automatically upon writing to a PaRAM set entry
  - Support for programmable QDMA channel to PaRAM mapping
- 128 PaRAM sets
  - Each PaRAM set can be used for a DMA channel, QDMA channel, or link set (remaining)
- Two transfer controllers/event queues. The system-level priority of these queues is user programmable
- 16 event entries per event queue
- External events (for example, ASP TX Evt and RX Evt)

The EDMA Transfer Controller has the following features:

- Two transfer controllers
- 64-bit wide read and write ports per channel
- Up to four in-flight transfer requests (TR)
- Programmable priority level
- Supports two dimensional transfers with independent indexes on source and destination (EDMA3CC manages the 3rd dimension)
- Support for increment and constant addressing modes
- Interrupt and error support

Parameter RAM: Each EDMA is specified by an eight word (32-byte) parameter table contained in Parameter RAM (PaRAM) within the CC. DM355 provides 128 PaRAM entries, one for each of the 64 DMA channels and for 64 QDMA / Linked DMA entries.

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DMA Channels: Can be triggered by: " External events (for example, ASP TX Evt and RX Evt), " Software writing a '1' to the given bit location, or channel, of the Event Set register, or, " Chaining to other DMAs.

QDMA: The Quick DMA (QDMA) function is contained within the CC. DM355 implements 8 QDMA channels. Each QDMA channel has a selectable PaRAM entry used to specify the transfer. A QDMA transfer is submitted immediately upon writing of the "trigger" parameter (as opposed to the occurrence of an event as with EDMA). The QDMA parameter RAM may be written by any Config bus master through the Config Bus and by DMAs through the Config Bus bridge.

QDMA Channels: Triggered by a configuration bus write to a designated 'QDMA trigger word'. QDMAs allow a minimum number of linear writes (optimized for GEM IDMA feature) to be issued to the CC to force a series of transfers to take place.

3.14.2.1 EDMA Channel Synchronization Events

The EDMA supports up to 64 EDMA channels which service peripheral devices and external memory. Table 3-29 lists the source of EDMA synchronization events associated with each of the programmable EDMA channels. For the DM355 device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA event registers (ER, ERH) even if the events are disabled by the EDMA event enable registers (EER, EERH). For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide* (literature number SPRUEE4).

Table 3-29. DM355 EDMA Channel Synchronization Events(1) (2)

EDMA CHANNEL	EVENT NAME	EVENT DESCRIPTION
0	TIMER3: TINT6	Timer 3 Interrupt (TINT6) Event
1	TIMER3 TINT7	Timer 3 Interrupt (TINT7) Event
2	ASP0: XEVT	ASP0 Transmit Event
3	ASP0: REVT	ASP0 Receive Event
4	VPSS: EVT1	VPSS Event 1
5	VPSS: EVT2	VPSS Event 2
6	VPSS: EVT3	VPSS Event 3
7	VPSS: EVT4	VPSS Event 4
8	ASP1: XEVT or TIMER2: TINT4	ASP1 Transmit Event or Timer 2 interrupt (TINT4) Event
9	ASP1: REVT or TIMER2: TINT5	ASP1 Receive Event or Timer 2 interrupt (TINT5) Event
10	SPI2: SPI2XEVT	SPI2 Transmit Event
11	SPI2: SPI2REVT	SPI2 Receive Event
12	Reserved	
13	Reserved	
14	SPI1: SPI1XEVT	SPI1 Transmit Event
15	SPI1: SPI1REVT	SPI1 Receive Event
16	SPI0: SPI0XEVT	SP0I Transmit Event
17	SPI0: SPI0REVT	SPI0 Receive Event
18	UART0: URXEVT0	UART 0 Receive Event

(1) In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or intermediate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide* (literature number SPRUEE4).

(2) The total number of EDMA events in DM355 exceeds 64, which is the maximum value of the EDMA module. Therefore, several events are multiplexed and you must use the register EDMA_EVTMUX in the System Control Module to select the event source for multiplexed events. Refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) for more information on the System Control Module register EDMA_EVTMUX.

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Table 3-29. DM355 EDMA Channel Synchronization Events (1) (2) (continued)

EDMA CHANNEL	EVENT NAME	EVENT DESCRIPTION
19	UART0: UTXEVT0	UART 0 Transmit Event
20	UART1: URXEVT1	UART 1 Receive Event
21	UART1: UTXEVT1	UART 1 Transmit Event
22	UART2: URXEVT2	UART 2 Receive Event
23	UART2: UTXEVT2	UART 2 Transmit Event
24	Reserved	
25	GPIO: GPINT9	GPIO 9 Interrupt Event
26	MMC0RXEVT	MMC/SD0 Receive Event
27	MMC0TXEVT	MMC/SD0 Transmit Event
28	I2CREVT	I2C Receive Event
29	I2CXEVT	I2C Transmit Event
30	MMC1RXEVT	MMC/SD1 Receive Event
31	MMC1TXEVT	MMC/SD1 Transmit Event
32	GPINT0	GPIO 0 Interrupt Event
33	GPINT1	GPIO 1 Interrupt Event
34	GPINT2	GPIO 2 Interrupt Event
35	GPINT3	GPIO 3 Interrupt Event
36	GPINT4	GPIO 4 Interrupt Event
37	GPINT5	GPIO 5 Interrupt Event
38	GPINT6	GPIO 6 Interrupt Event
39	GPINT7	GPIO 7 Interrupt Event
40	GPBNKINT0	GPIO Bank 0 Interrupt Event
41	GPBNKINT1	GPIO Bank 1 Interrupt Event
42	GPBNKINT2	GPIO Bank 2 Interrupt Event
43	GPBNKINT3	GPIO Bank 3 Interrupt Event
44	GPBNKINT4	GPIO Bank 4 Interrupt Event
45	GPBNKINT5	GPIO Bank 5 Interrupt Event
46	GPBNKINT6	GPIO Bank 6 Interrupt Event
47	GPINT8	GPIO 8 Interrupt Event
48	TIMER0: TINT0	Timer 0 Interrupt Event
49	TIMER0: TINT1	Timer 1 Interrupt Event
50	TIMER1: TINT2	Timer 2 Interrupt Event
51	TIMER1: TINT3	Timer 3 Interrupt Event
52	PWM0	PWM 0 Event
53	PWM1	PWM 1 Event
54	PWM2	PWM 2 Event
55	PWM3	PWM 3 Event
56 - 63	Reserved	

3.15 MPEG4/JPEG Overview

The DM355 supports the computational operations used for image processing, JPEG compression and MPEG4 video and imaging standard.

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted) (1) (2)

Supply voltage ranges	All 1.3 V supplies	-0.5 V to 1.7 V
	All digital 1.8 V supplies	-0.5 V to 2.5 V
	All analog 1.8 V supplies	-0.5 V to 1.89 V
	All 3.3 V supplies	-0.5 V to 4.4 V
Input voltage ranges	All 1.8 V I/Os	-0.5 V to 2.3 V
	All 3.3 V I/Os	-0.5 V to 3.8 V
	VBUS	0.0 V to 5.5 V
Clamp current for input or output(3)	I_{clamp}	-20 mA to 20 mA
Operating case temperature ranges	Commercial T_c	0°C to 85 °C
	Extended Temperature [A216 and A135 devices] T_c	-40°C to 100 °C
Storage temperature ranges	T_{stg}	-65°C to 150 °C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.
(3) Clamp current flows from an input or output pad to a supply rail through a clamp circuit or an intrinsic diode. Positive current results from an applied input or output voltage that is more than 0.5 V higher (more positive) than the supply voltage, $V_{DD}/V_{DDA_PLL1/2}/V_{DD_USB}/V_{DD_DDR}$ for dual-supply macros. Negative current results from an applied voltage that is more than 0.5 V less (more negative) than the V_{SS} voltage..

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4.2 Recommended Operating Conditions

	NAME	DESCRIPTION		MIN	NOM	MAX	UNIT
Supply Voltage	CV_{DD}	Supply voltage, Core		1.235	1.3	1.365	V
	V_{DDA_PLL1}	Supply voltage, PLL1		1.235	1.3	1.365	V
	V_{DDA_PLL2}	Supply voltage, PLL2		1.235	1.3	1.365	V
	V_{DDD13_USB}	Supply voltage, USB Digital		1.235	1.3	1.365	V
	V_{DDA13_USB}	Supply voltage, USB Analog		1.235	1.3	1.365	V
	V_{DDA33_USB}	Supply voltage, USB Analog		3.135	3.3	3.465	V
	$V_{DDA33_USB_PLL}$	Supply voltage, USB Common PLL		3.135	3.3	3.465	V
	V_{DD_DDR}	Supply voltage, DDR2 / MDDR		1.71	1.8	1.89	V
	V_{DDA33_DDRDLL}	Supply voltage, DDR DLL Analog		3.135	3.3	3.465	V
	V_{DD_VIN}	Supply voltage, Digital video In		3.135	3.3	3.465	V
	V_{DD_VOUT}	Supply voltage, Digital Video Out		3.135	3.3	3.465	V
	V_{DDA18_DAC}	Supply voltage, DAC Analog		1.71	1.8	1.89	V
	V_{DD}	Supply voltage, I/Os		3.135	3.3	3.465	V
Supply Ground	V_{SS}	Supply ground, Core, USB Digital		0	0	0	V
	V_{SSA_PLL1}	Supply ground, PLL1		0	0	0	V
	V_{SSA_PLL2}	Supply ground, PLL2		0	0	0	V
	V_{SS_USB}	Supply ground, USB		0	0	0	V
	V_{SSA_DLL}	Supply ground, DLL		0	0	0	V
	V_{SSA_DAC}	Supply ground, DAC Analog		0	0	0	V
	V_{SS_MX1}	MXI1 osc ground(1)		0	0	0	V
	V_{SS_MX2}	MXI2 osc ground(1)		0	0	0	V
Voltage Input High	V_{IH}	High-level input voltage(2)		2			V
Voltage Input Low	V_{IL}	Low-level input voltage(2)				0.8	V
DAC(3)	V_{REF}	DAC reference voltage			450		mV
	R_{BIAS}	DAC full-scale current adjust resistor			2550		Ω
	R_{LOAD}	Output resistor			499		Ω
	C_{BG}	Bypass capacitor			0.1		µF
Video Buffer(3)	R_{OUT}	Output resistor (ROUT), between TVOUT and VFB pins			1070		Ω
	R_{FB}	Feedback resistor, between VFB and IOUT pins.			1000		
	R_{BIAS}	DAC full-scale current adjust resistor			2550		Ω
	C_{BG}	Bypass capacitor			0.1		µA
USB	USB_VBUS	USB external charge pump input		4.85	5	5.25	V
	R1	USB reference resistor(4)		9.9	10	10.1	kΩ
Temperature	T_c	Operating case temperature range	Commercial	0		85	°C
			Extended (A216 and A135 devices)	-40		100	°C
Transition Time	t_t	Transition time, 10% - 90%, All Inputs (unless otherwise specified in the electrical data sections)				0.25P or 10(5)	ns

(1) Oscillator ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground (see Section 5.5.1).
(2) These I/O specifications apply to regular 3.3 V I/Os and do not apply to DDR2/mDDR, USB I/Os. DDR2/mDDR I/Os are 1.8 V I/Os and adhere to JESD79-2A standard, USB I/Os adhere to USB2.0 spec.
(3) See Section 5.9.2.4 . Also, resistors should be E-96 spec line (3 digits with 1% accuracy).
(4) Connect USB_R1 to $V_{SS_USB_REF}$ via 10K ohm, 1% resistor placed as close to the device as possible.
(5) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

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4.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
Voltage Output	V_{OH}	High-level output voltage (2)	V_{DD}=MIN, I_{OH}=MAX	2.4			V
	V_{OL}	Low-level output voltage (2)	V_{DD}=MIN, I_{OL}=MAX			0.6	
Current Input/Output	I_I	Input current for I/O without internal pull-up/pull-down	V_I = V_{SS} to V_{DD}	-1		1	µA
	$I_{I(pullup)}$	Input current for I/O with internal pull-up (3) (4)	V_I = V_{SS} to V_{DD}	40		190	
	$I_{I(pulldown)}$	Input current for I/O with internal pull-down (3) (4)	V_I = V_{SS} to V_{DD}	-190		-40	
	I_{OH}	Current sink of high-level output current	V_{OH} = 2.4 V			-4000	
	I_{OL}	Current sink of low-level output current	V_{OL} = 0.6V			4000	
	I_{OZ}	I/O off-state output current	V_O = V_{DD} or V_{SS}; internal pull disabled			±20	
			V_O = V_{DD} or V_{SS}; internal pull enabled		±100		
Capacitance	C_I	Input capacitance				4	pF
	C_O	Output capacitance				4	
DAC	Resolution	Resolution			10		Bits
	INL	Integral non-linearity, best fit	R_{LOAD} = 499 Ω, Video buffer disabled		1		LSB
	DNL	Differential non-linearity	R_{LOAD} = 499 Ω, Video buffer disabled		0.5		LSB
	Compliance	Output compliance range	IFS = 1.4 mA, R_{LOAD} = 499 Ω	0		0.700	V
Video Buffer	$V_{OH(VIDBUF)}$	Output high voltage (top of 75% NTSC or PAL colorbar) (5)			1.55		V
	$V_{OL(VIDBUF)}$	Output low voltage (bottom of sync tip)			0.470		

(1) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.
(2) These I/O specifications apply to regular 3.3 V I/Os and do not apply to DDR2/mDDR, USB I/Os. DDR2/mDDR I/Os are 1.8 V I/Os and adhere to JESD79-2A standard, USB I/Os adhere to USB2.0 spec.
(3) This specification applies only to pins with an internal pullup (PU) or pulldown (PD). See Section 2.4 or Section 2.20 for pin descriptions.
(4) To pull up a signal to the opposite supply rail, a 1 kΩ resistor is recommended.
(5) 100% color bars are not supported. 100% color bars require 1.2 V peak-to-peak. The video buffer only provides 1.0 V peak-to-peak.

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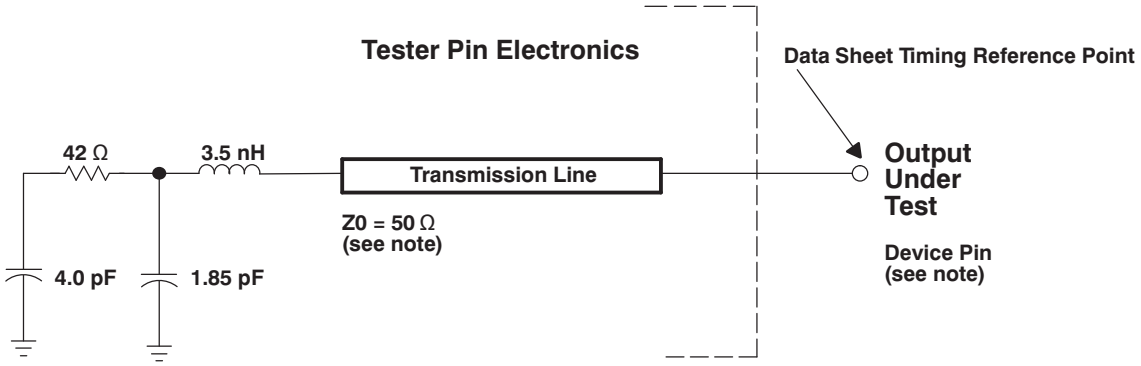
5 DM355 Peripheral Information and Electrical Specifications

5.1 Parameter Information Device-Specific Information



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.1.1 Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. For 3.3 V I/O, V_{ref} = 1.65 V. For 1.8 V I/O, V_{ref} = 0.9 V.

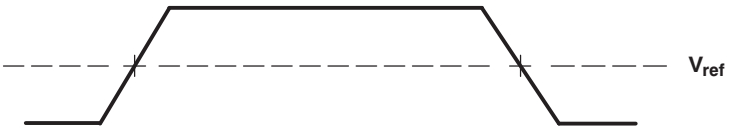


Figure 5-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL}MAX and V_{OH} MIN for output clocks.

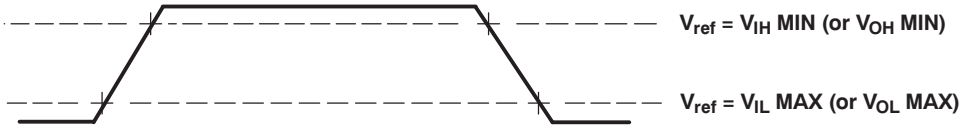


Figure 5-3. Rise and Fall Transition Time Voltage Reference Levels

5.1.2 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

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5.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals should transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.3 Power Supplies

The power supplies of DM355 are summarized in Table 5-1.

Table 5-1. Power Supplies

Customer Board Supply	Tolerance	Package Plane	Chip Plane Name	Description	Comments
1.3 V	±5%	1.3 V	CV_{DD}	Core V_{DD}	
			V_{DDA_PLL1}	PLL1 V_{DDA}	
			V_{DDA_PLL2}	PLL2 V_{DDA}	
			V_{DDD13_USB}	USB 1.3 V supply	
			V_{DDA13_USB}	USB 1.3 V supply	
3.3 V	±5%	3.3 V	V_{DD}	IO V_{DD} for LVCMOS	V_{DDSHV}
			V_{DD}	IO V_{DD} for MXI/O1	V_{DDSHV}
			V_{DD}	IO V_{DD} for MXI/O2	V_{DDSHV1}
			V_{DD}	IO V_{DD} for ISB DRVVBUS	V_{DDSHV2}
			V_{DDA33_DDRDLL}	DDR DLL analog V_{DD}	
			V_{DDA33_USB}	Analog 3.3 V power USB PHY	
			$V_{DDA33_USB_PLL}$	Common mode 3.3 V power for USB PHY (PLL)	
			V_{DD}	IO V_{DD} for peripherals	
3.3 V	±5%	3.3 V	V_{DD_VIN}	IO V_{DD} for VideoIN I/F	
			V_{DD_VOUT}	IO V_{DD} for VideoOUT I/F	
1.8 V	±5%	1.8 V	V_{DD_DDR}		
1.8 V	±5%	1.8 V	V_{DDA18}		Analog 1.8 V power
1.8 V	±5%	1.8 V	V_{DDA18_DAC}		Place decoupling caps (0.1µF/10µf) close to chip
0 V	n/a	0 V	V_{SS_MX1}		Connect to external crystal capacitor ground
0 V	n/a	0 V	V_{SS_MX2}		Connect to external crystal capacitor ground
0 V	n/a	0 V	V_{SS}	Chip ground	
				USB ESD ground	
				ground	V_{SS}
0 V	n/a	0 V	V_{SSA}	ground	Keep separate from digital ground V_{SS}
0 V	n/a	0 V	V_{SSA_PLL1}	PLL1 V_{SSA}	
0 V	n/a	0 V	V_{SSA_PLL2}	PLL2 V_{SSA}	
0 V	n/a	0 V	V_{SSA_DLL}	DLL ground	
0 V	n/a	0 V	V_{SS_USB}	USB ground	V_{SSA13_USB}
					V_{SSA13_USB}
					V_{SSA33_USB}
					$V_{SSA33_USB_PLL}$
0 V	n/a	0 V	$V_{SS_USB_REF}$	USB PHY reference ground	V_{SSREF}
0 V	n/a	0 V	V_{SSA_DAC}	DAC ground	Keep separate from digital ground V_{SS}
V_{DDS}*0.5		V_{DDS}*0.5	$V_{REFSSTL}$	DRR ref voltage	V_{DDS} divided by 2, through board resistors
5 V		5 V	USB_VBUS	VBUS	Connect to external charge pump

5.3.1 Power-Supply Sequencing

In order to ensure device reliability, the DM355 requires the following power supply power-on and power-off sequences. See table Table 5-1 for a description of DM355 power supplies.

Power-On:

1. Power on 1.3 V: CV_{DD}, $V_{DDA_PLL1/2}$, V_{DDD13_USB}, V_{DDA13_USB}
2. Power on 1.8 V: V_{DD_DDR}, V_{DDA18_DAC}
3. Power on 3.3 V: D_{VDD}, V_{DDA33_DDRDLL}, V_{DDA33_USB}, $V_{DDA33_USB_PLL}$, V_{DD_VIN}, V_{DD_VOUT}

You may power-on the 1.8 V and 3.3 V power supplies simultaneously.

Power-Off:

1. Power off 3.3 V: D_{VDD}, V_{DDA33_DDRDLL}, V_{DDA33_USB}, $V_{DDA33_USB_PLL}$, V_{DD_VIN}, V_{DD_VOUT}
2. Power off 1.8 V: V_{DD_DDR}, V_{DDA18_DAC}
3. Power off 1.3 V: CV_{DD}, $V_{DDA_PLL1/2}$, V_{DDD13_USB}, V_{DDA13_USB}

You may power-off the 1.8 V and 3.3 V power supplies simultaneously.

Power-off the 1.8v/3.3V supply before or within 10usec of power-off of the 1.3 V supply.

Note that when booting the DM355 from OneNAND, you must ensure that the OneNAND device is ready with valid program instructions before the DM355 attempts to read program instructions from it. In particular, before you release DM355 reset, you must allow time for OneNAND device power to stabilize and for the OneNAND device to complete its internal copy routine. During the internal copy routine, the OneNAND device copies boot code from its internal non-volatile memory to its internal boot memory section. Board designers typically achieve this requirement by design of the system power and reset supervisor circuit. Refer to your OneNAND device datasheet for OneNAND power ramp and stabilization times and for OneNAND boot copy times.

5.3.1.1 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DM355 to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the DM355 device, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

5.3.1.2 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to DM355. These caps need to be close to the DM355 power pins, no more than 1.25 cm maximum distance to be effective. Physically smaller caps, such as 0402, are better because of their lower parasitic inductance. Proper capacitance values are also important. Small bypass caps (near 560 pF) should be closest to the power pins. Medium bypass caps (220 nF or as large as can be obtained in a small package) should be next closest. TI recommends no less than 8 small and 8 medium caps per supply be placed immediately next to the BGA vias, using the "interior" BGA space and at least the corners of the "exterior".

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 100 μF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

Any cap selection needs to be evaluated from a yield/manufacturing point-of-view. As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered. See also Section 5.5.1 and Section 5.5.2 for additional recommendations on power supplies for the oscillator/PLL supplies.

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5.4 Reset

5.4.1 Reset Electrical Data/Timing

Table 5-2. Timing Requirements for Reset (1) (2) (see Figure 5-4)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{w(RESET)}$	Active low width of the $\overline{\text{RESET}}$ pulse	12C		ns
2	$t_{su(BOOT)}$	Setup time, boot configuration pins valid before $\overline{\text{RESET}}$ rising edge	12C		ns
3	$t_{h(BOOT)}$	Hold time, boot configuration pins valid after $\overline{\text{RESET}}$ rising edge	12C		ns

(1) BTSEL[1:0] and AECFG[4:0] are the boot configuration pins during device reset.
(2) C = MXI/CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 24 MHz use C = 41.$\overline{6}$ ns.

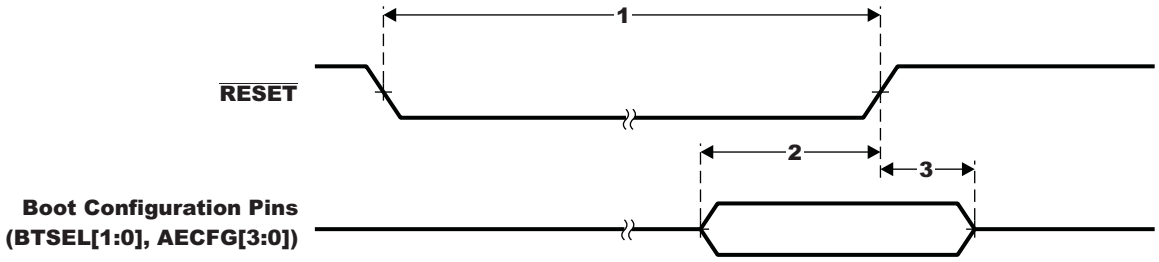

Figure 5-4. Reset Timing

5.5 Oscillators and Clocks

DM355 has two oscillator input/output pairs (MXI1/MXO1 and MXI2/MXO2) usable with external crystals or ceramic resonators to provide clock inputs. The optimal frequencies for the crystals are 24 MHz (MXI1/MXO1) and 27 MHz (MXI2/MXO2). Optionally, the oscillator inputs are configurable for use with external clock oscillators. If external clock oscillators are used, to minimize the clock jitter, a single clean power supply should power both the DM355 and the external oscillator circuit and the minimum CLKIN rise and fall times must be observed. The electrical requirements and characteristics are described in this section.

The timing parameters for CLKOUT[3:1] are also described in this section. The DM355 has three output clock pins (CLKOUT[3:1]). See Section 3.5 and Section 3.6 for more information on CLKOUT[3:1].

5.5.1 MXI1 (24-MHz) Oscillator

The MXI1 (typically 24 MHz, can also be 36 MHz) oscillator provides the primary reference clock for the DM355 device. The on-chip oscillator requires an external crystal connected across the MXI1 and MXO1 pins, along with two load capacitors, as shown in Figure 5-5. The external crystal load capacitors ***must*** be connected only to the oscillator ground pin (V_{SS_MX1}). ***Do not*** connect to board ground (V_{SS}). Also, the PLL power pin (V_{DDA_PLL1}) should be connected to the power supply through a ferrite bead, L1 in the example circuit shown in Figure 5-5.

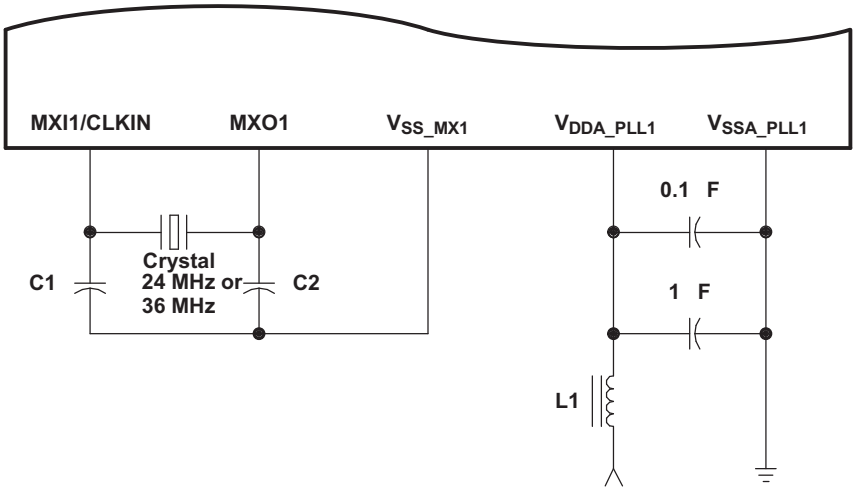

Figure 5-5. MXI1 (24-MHz) Oscillator

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (typical values are C1 = C2 = 10 pF). CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (MXI1 and MXO1) and to the V_{SS_MX1} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

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Table 5-3. Switching Characteristics Over Recommended Operating Conditions for 24-MHz System Oscillator

PARAMETER	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency)			4	ms
Oscillation frequency		24 or 36		MHz
ESR			60	Ω
Frequency stability			+/-50	ppm

5.5.2 MXI2 (27-MHz) Oscillator (optional oscillator)

The MXI2 (27 MHz) oscillator provides an optional reference clock for the DM355's VPSS module. The on-chip oscillator requires an external 27-MHz crystal connected across the MXI2 and MXO2 pins, along with two load capacitors, as shown in Figure 5-6. The external crystal load capacitors ***must*** be connected only to the 27-MHz oscillator ground pin (V_{SS_MX2}). ***Do not*** connect to board ground (V_{SS}). Also, the PLL power pin (V_{DDA_PLL2}) should be connected to the power supply through a ferrite bead, L1 in the example circuit shown in Figure 5-6.

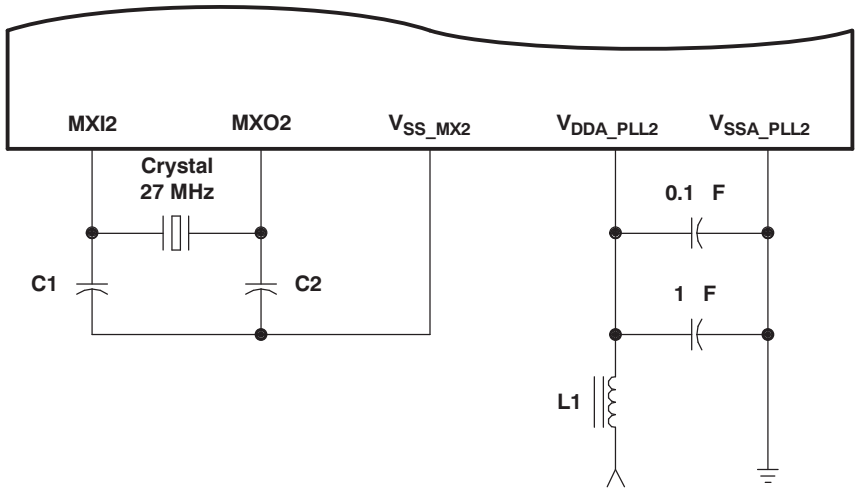

Figure 5-6. MXI2 (27-MHz) System Oscillator

The load capacitors, C1 and C2, should be chosen such that the equation is satisfied (typical values are C1 = C2 = 10 pF). CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (MXI and MXO) and to the V_{SS_MX2} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-4. Switching Characteristics Over Recommended Operating Conditions for 27-MHz System Oscillator

PARAMETER	MIN	TYP	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency)			4	ms
Oscillation frequency		27		MHz
ESR			60	Ω
Frequency stability			+/-50	ppm

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5.5.3 Clock PLL Electrical Data/Timing (Input and Output Clocks)

Table 5-5. Timing Requirements for MXI1/CLKIN1(1) (2) (see Figure 5-7)

NO.	PARAMETER		DM355			UNIT
			MIN	TYP	MAX	
1	$t_{c(MXI1)}$	Cycle time, MXI1/CLKIN1	27.$\overline{7}$ (3)		41.$\overline{6}$ (3)	ns
2	$t_{w(MXI1H)}$	Pulse duration, MXI1/CLKIN1 high	0.45C		0.55C	ns
3	$t_{w(MXI1L)}$	Pulse duration, MXI1/CLKIN1 low	0.45C		0.55C	ns
4	$t_{t(MXI1)}$	Transition time, MXI1/CLKIN1			0.25C or 10(4)	ns
5	$t_{J(MXI1)}$	Period jitter, MXI1/CLKIN1			0.02C	ns

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(2) C = MXI1/CLKIN1 cycle time in ns. For example, when MXI1/CLKIN1 frequency is 24 MHz use C = 41.$\overline{6}$ ns.
(3) tc(MXI1) = 41.$\overline{6}$ ns and tc(MXI1) = 27.$\overline{7}$ ns are the only supported cycle times for MXI1/CLKIN1.
(4) Whichever is smaller. C = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

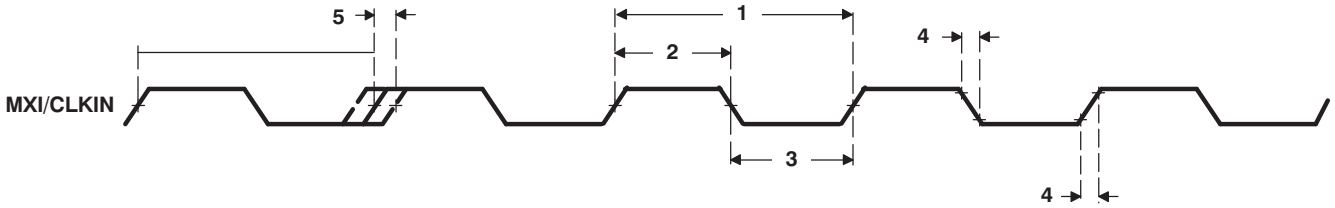

Figure 5-7. MXI1/CLKIN1 Timing

Table 5-6. Timing Requirements for MXI2/CLKIN2(1) (2) (see Figure 5-7)

NO.	PARAMETER		DM355			UNIT
			MIN	TYP	MAX	
1	$t_{c(MXI2)}$	Cycle time, MXI2/CLKIN2	37.$\overline{037}$ (3)		37.$\overline{037}$ (3)	ns
2	$t_{w(MXI2H)}$	Pulse duration, MXI2/CLKIN2 high	0.45C		0.55C	ns
3	$t_{w(MXI2L)}$	Pulse duration, MXI2/CLKIN2 low	0.45C		0.55C	ns
4	$t_{t(MXI2)}$	Transition time, MXI2/CLKIN2			0.25C or 10(4)	ns
5	$t_{J(MXI2)}$	Period jitter, MXI2/CLKIN2			0.02C	ns

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(2) C = MXI2/CLKIN2 cycle time in ns. For example, when MXI2/CLKIN2 frequency is 27 MHz use C = 37.$\overline{037}$ ns.
(3) tc(MXI2) = 37.$\overline{037}$ ns is the only supported cycle time for MXI2/CLKIN2.
(4) Whichever is smaller. C = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

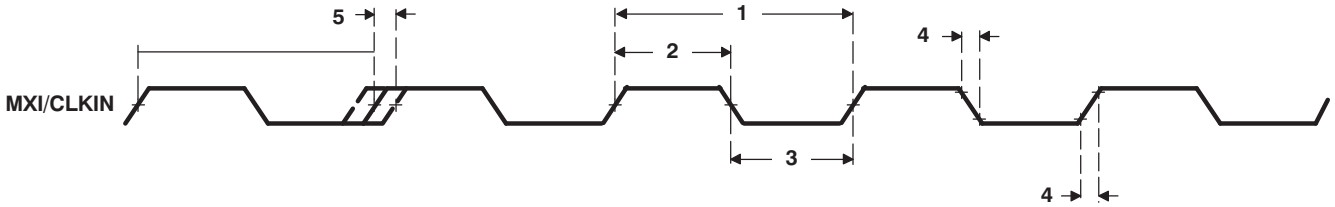

Figure 5-8. MXI2/CLKIN2 Timing

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Table 5-7. Switching Characteristics Over Recommended Operating Conditions for CLKOUT1(1) (2) (see Figure 5-9)

NO.	PARAMETER		DM355			UNIT
			MIN	TYP	MAX	
1	$t_{C(CLKOUT1)}$	Cycle time, CLKOUT1	$t_{c(MXI1)}$			ns
2	$t_{w(CLKOUT1H)}$	Pulse duration, CLKOUT1 high	0.45P		0.55P	ns
3	$t_{w(CLKOUT1L)}$	Pulse duration, CLKOUT1 low	0.45P		0.55P	ns
4	$t_{t(CLKOUT1)}$	Transition time, CLKOUT1			0.05P	ns
5	$t_{d(MXI1H-CLKOUT1H)}$	Delay time, MXI1/CLKIN1 high to CLKOUT1 high	1		8	ns
6	$t_{d(MXI1L-CLKOUT1L)}$	Delay time, MXI1/CLKIN1I low to CLKOUT1 low	1		8	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH}MIN.
(2) P = 1/CLKOUT1 clock frequency in nanoseconds (ns). For example, when CLKOUT1 frequency is 24 MHz use P = 41.$\overline{6}$ ns.

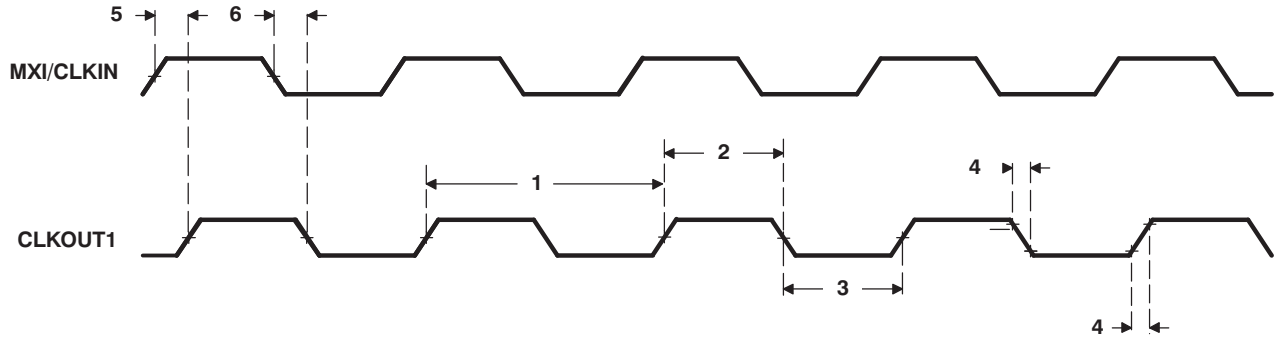

Figure 5-9. CLKOUT1 Timing

Table 5-8. Switching Characteristics Over Recommended Operating Conditions for CLKOUT2(1) (2) (see Figure 5-10)

NO.	PARAMETER		DM355			UNIT
			MIN	TYP	MAX	
1	$t_{C(CLKOUT2)}$	Cycle time, CLKOUT2	$t_{c(MXI1)}$ /3			
2	$t_{w(CLKOUT2H)}$	Pulse duration, CLKOUT2 high	0.45P		0.55P	ns
3	$t_{w(CLKOUT2L)}$	Pulse duration, CLKOUT2 low	0.45P		0.55P	ns
4	$t_{t(CLKOUT2)}$	Transition time, CLKOUT2			0.05P	ns
5	$t_{d(MXI1H-CLKOUT2H)}$	Delay time, MXI1/CLKIN1 high to CLKOUT2 high	1		8	ns
6	$t_{d(MXI1L-CLKOUT2L)}$	Delay time, MXI1/CLKIN1 low to CLKOUT2 low	1		8	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH}MIN.
(2) P = 1/CLKOUT2 clock frequency in nanoseconds (ns). For example, when CLKOUT2 frequency is 8 MHz use P = 125 ns.

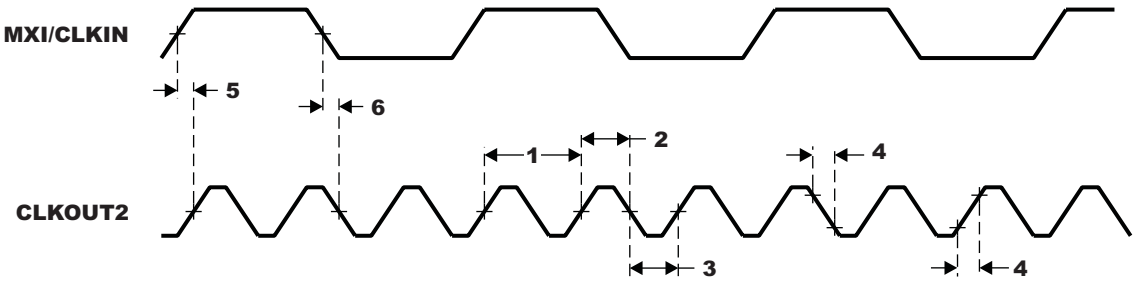

Figure 5-10. CLKOUT2 Timing

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for CLKOUT3(1) (2) (see

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH}MIN.
(2) P = 1/CLKOUT3 clock frequency in nanoseconds (ns). For example, when CLKOUT3 frequency is 3 MHz use P = 333.$\overline{3}$ ns.

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for CLKOUT3 (1) (2) (see Figure 5-11) (continued)

Figure 5-11)

NO.	PARAMETER		DM355			UNIT
			MIN	TYP	MAX	
1	$t_{C(CLKOUT3)}$	Cycle time, CLKOUT3	$t_{c(MXI1)}$ /8			
2	$t_{w(CLKOUT3H)}$	Pulse duration, CLKOUT3 high	0.45P		0.55P	ns
3	$t_{w(CLKOUT3L)}$	Pulse duration, CLKOUT3 low	0.45P		0.55P	ns
4	$t_{t(CLKOUT3)}$	Transition time, CLKOUT3			0.05P	ns
5	$t_{d(MXI2H-CLKOUT3H)}$	Delay time, CLKIN/MXI high to CLKOUT3 high	1		8	ns
6	$t_{d(MXI2L-CLKOUT3L)}$	Delay time, CLKIN/MXI low to CLKOUT3 low	1		8	ns

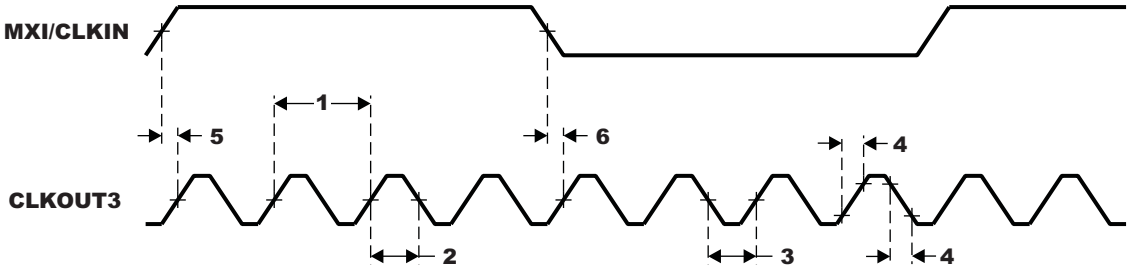

Figure 5-11. CLKOUT3 Timing

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5.6 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]). There are a total of 7 GPIO banks in the DM355, because the DM355 has 104 GPIOs.

The DM355 GPIO peripheral supports the following:

- Up to 104 3.3v GPIO pins, GPIO[103:0]
- Interrupts:
  - Up to 10 unique GPIO[9:0] interrupts from Bank 0
  - Up to 7 GPIO (bank aggregated) interrupt signals, one from each of the 7 banks of GPIOs
  - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- DMA events:
  - Up to 10 unique GPIO DMA events from Bank 0
  - Up to 7 GPIO (bank aggregated) DMA event signals, one from each of the 7 banks of GPIOs
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

For more detailed information on GPIOs, see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide* (literature number SPRUEE6).

5.6.1 GPIO Peripheral Input/Output Electrical Data/Timing

Table 5-10. Timing Requirements for GPIO Inputs (see Figure 5-12)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	52		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	52		ns

Table 5-11. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-12)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	26(1)		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	26(1)		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.

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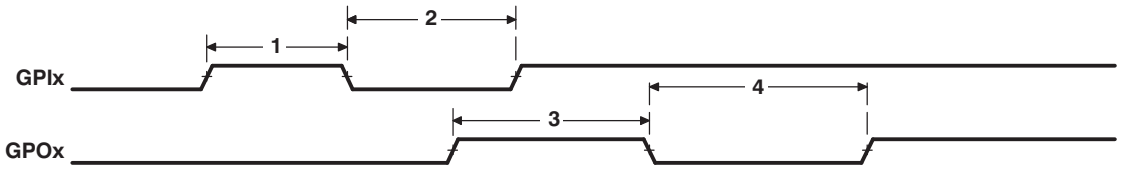

Figure 5-12. GPIO Port Timing

5.6.2 GPIO Peripheral External Interrupts Electrical Data/Timing

Table 5-12. Timing Requirements for External Interrupts/EDMA Events(1) (see Figure 5-13)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{w(ILOW)}$	Width of the external interrupt pulse low	52		ns
2	$t_{w(IHIGH)}$	Width of the external interrupt pulse high	52		ns

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have DM355 to recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow DM355 enough time to access the GPIO register through the internal bus.

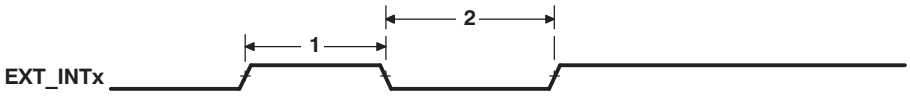

Figure 5-13. GPIO External Interrupt Timing

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5.7 External Memory Interface (EMIF)

DM355 supports several memory and external device interfaces, including:

- Asynchronous EMIF (AEMIF) for interfacing to SRAM.
  - OneNAND flash memories
  - NAND flash memories
- DDR2/mDDR Memory Controller for interfacing to SDRAM.

5.7.1 Asynchronous EMIF (AEMIF)

The EMIF supports the following features:

- SRAM, etc. on up to 2 asynchronous chip selects addressable up to 64KB each
- Supports 8-bit or 16-bit data bus widths
- Programmable asynchronous cycle timings
- Supports extended wait mode
- Supports Select Strobe mode

5.7.1.1 NAND (NAND, SmartMedia, xD)

The NAND features of the EMIF are as follows:

- NAND flash on up to 2 asynchronous chip selects
- 8 and 16-bit data bus widths
- Programmable cycle timings
- Performs 1-bit and 4-bit ECC calculation
- NAND Mode also supports SmartMedia/SSFDC (Solid State Floppy Disk Controller) and xD memory cards

5.7.1.2 OneNAND

The OneNAND features supported are as follows.

- NAND flash on up to 2 asynchronous chip selects
- Only 16-bit data bus widths
- Supports asynchronous writes and reads
- Supports synchronous reads with continuous linear burst mode (Does not support synchronous reads with wrap burst modes)
- Programmable cycle timings for each chip select in asynchronous mode

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5.7.1.3 AEMIF Electrical Data/Timing

Table 5-13. Timing Requirements for Asynchronous Memory Cycles for AEMIF Module(1) (see Figure 5-14 and Figure 5-15)

NO.	PARAMETER		DM355			UNIT
			MIN	Nom	MAX	
READS and WRITES						
2	$t_{w(EM_WAIT)}$	Pulse duration, EM_WAIT assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high	5			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high	0			ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup time EM_WAIT asserted before $\overline{EM_OE}$ high(2)		4E		ns
READS (OneNAND Synchronous Burst Read)						
30	$t_{su(EMDV-EMCLKH)}$	Setup time, EM_D[15:0] valid before EM_CLK high	4			ns
31	$t_{h(EMCLKH-EMDIV)}$	Hold time, EM_D[15:0] valid after EM_CLK high	4			ns
WRITES						
28	$t_{su(EMWEL-EMWAIT)}$	Setup time, EM_WAIT asserted before $\overline{EM_WE}$ high(2)		4E		ns

(1) E = PLLC1 SYSCLK2 period in ns. SYSCLK2 is the EMIF peripheral clock. SYSCLK2 is one-fourth the PLLC output clock. For example, when PLLC output clock = 432 MHz, E = 9.259 ns. See Section 3.5 for more information.

(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 5-16 and Figure 5-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-14. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for AEMIF Module(1) (2) (3) (see Figure 5-14 and Figure 5-15)

NO.	PARAMETER		DM355			UNIT
			MIN	Nom	MAX	
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time		(TA)*E		ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)		(RS+RST+RH)*E		ns
		EMIF read cycle time (EW = 1)		(RS+RST+RH+(EWC*16))*E		ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_OE}$ low (SS = 0)		(RS)*E		ns
		Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_OE}$ low (SS = 1)		0		ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 0)		(RH)*E		ns
		Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 1)		0		ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following range of values: TA[4-1], RS[16-1], RST[64-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256]. See the *TMS320DM355 DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (literature number SPRUED1) for more information.

(2) E = PLLC1 SYSCLK2 period in ns. SYSCLK2 is the EMIF peripheral clock. SYSCLK2 is one-fourth the PLLC output clock. For example, when PLLC output clock = 432 MHz, E = 9.259 ns. See Section 3.5 for more information

(3) EWC = external wait cycles determined by EM_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320DM355 DMSoC Asynchronous External Memory Interface (EMIF) User's Guide* (literature number SPRUED1) for more information.

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Table 5-14. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for AEMIF Module (1) (2) (3) (see Figure 5-14 and Figure 5-15) (continued)

NO.	PARAMETER		DM355			UNIT
			MIN	Nom	MAX	
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_BA[1:0] valid to EM_OE low		(RS)*E		ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, EM_OE high to EM_BA[1:0] invalid		(RH)*E		ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, EM_A[13:0] valid to EM_OE low		(RS)*E		ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, EM_OE high to EM_A[13:0] invalid		(RH)*E		ns
10	$t_{w(EMOEL)}$	EM_OE active low width (EW = 0)		(RST)*E		ns
		EM_OE active low width (EW = 1)		(RST+(EWC*16))*E		ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EM_WAIT deasserted to EM_OE high		4E		ns
READS (OneNAND Synchronous Burst Read)(4)						
32	$f_{c(EM_CLK)}$	Frequency, EM_CLK	1		66	MHz
33	$t_{c(EM_CLK)}$	Cycle time, EM_CLK	15		1000	ns
34	$t_{su(EM_ADVV-EM_CLKH)}$	Output setup time, EM_ADV valid before EM_CLK high	5			ns
35	$t_{h(EM_CLKH-EM_ADVIV)}$	Output hold time, EM_CLK high to EM_ADV invalid	6			ns
36	$t_{su(EM_AV-EM_CLKH)}$	Output setup time, EM_A[13:0]/EM_BA[1] valid before EM_CLK high	5			ns
37	$t_{h(EM_CLKH-EM_AIV)}$	Output hold time, EM_CLK high to EM_A[13:0]/EM_BA[1] invalid	6			ns
38	$t_{w(EM_CLKH)}$	Pulse duration, EM_CLK high	$t_{c(EM_CLK)}/3$			ns
39	$t_{w(EM_CLKL)}$	Pulse duration, EM_CLK low	$t_{c(EM_CLK)}/3$			ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)		(WS+WST+WH)*E		ns
		EMIF write cycle time (EW = 1)		(WS+WST+WH+(EWC*16))*E		ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, EM_CE[1:0] low to EM_WE low (SS = 0)		(WS)*E		ns
		Output setup time, EM_CE[1:0] low to EM_WE low (SS = 1)		0		ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, EM_WE high to EM_CE[1:0] high (SS = 0)		(WH)*E		ns
		Output hold time, EM_WE high to EM_CE[1:0] high (SS = 1)		0		ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EM_BA[1:0] valid to EM_WE low		(WS)*E		ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, EM_WE high to EM_BA[1:0] invalid		(WH)*E		ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EM_A[13:0] valid to EM_WE low		(WS)*E		ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, EM_WE high to EM_A[13:0] invalid		(WH)*E		ns
24	$t_{w(EMWEL)}$	EM_WE active low width (EW = 0)		(WST)*E		ns
		EM_WE active low width (EW = 1)		(WST+(EWC*16))*E		ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EM_WAIT deasserted to EM_WE high		4E		ns

(4) During OneNAND Mode the EM_CLK is driven by 1/2 PLLC1SYSCLK2 clk.

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Table 5-14. Switching Characteristics Over Recommended Operating Conditions for Asynchronous Memory Cycles for AEMIF Module (1) (2) (3) (see Figure 5-14 and Figure 5-15) (continued)

NO.	PARAMETER		DM355			UNIT
			MIN	Nom	MAX	
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EM_D[15:0] valid to EM_WE low		(WS)*E		ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, EM_WE high to EM_D[15:0] invalid		(WH)*E		ns

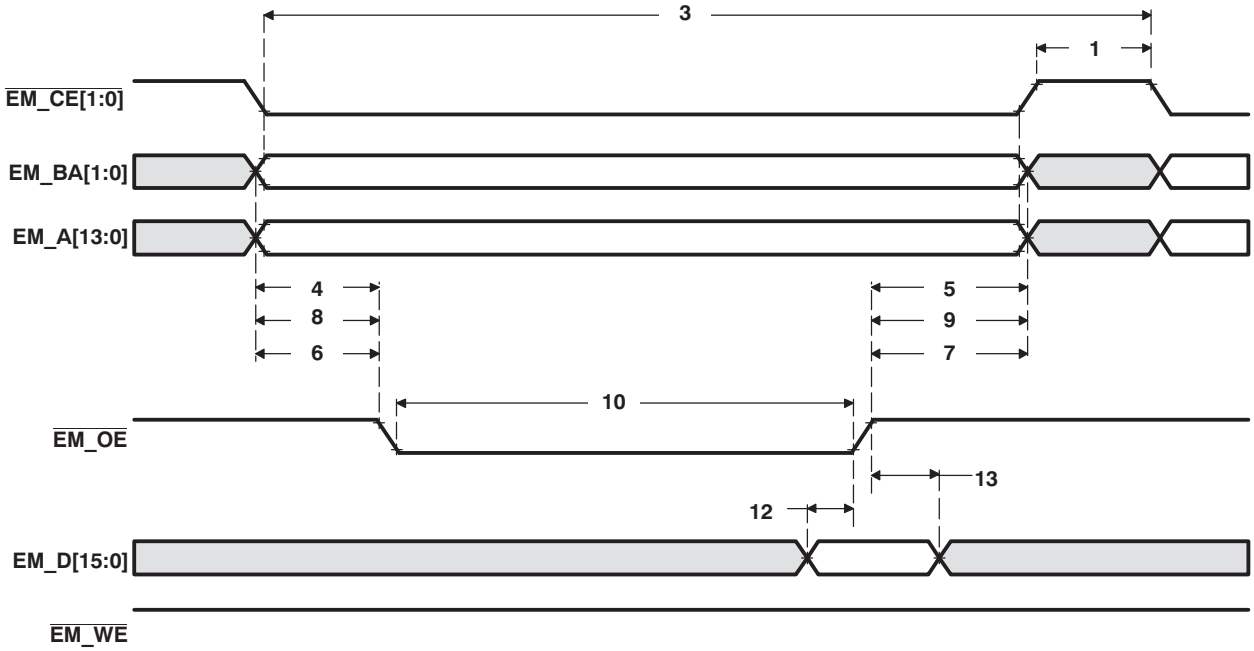

Figure 5-14. Asynchronous Memory Read Timing for EMIF

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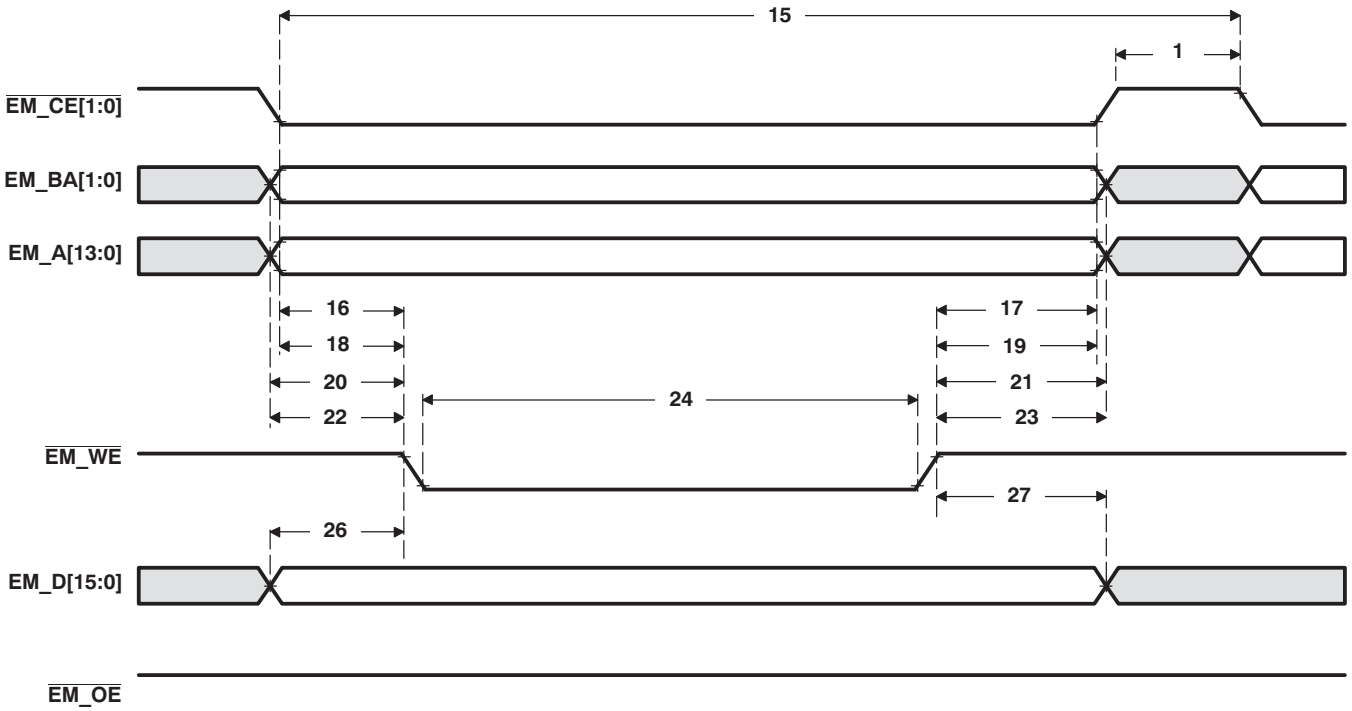

Figure 5-15. Asynchronous Memory Write Timing for EMIF

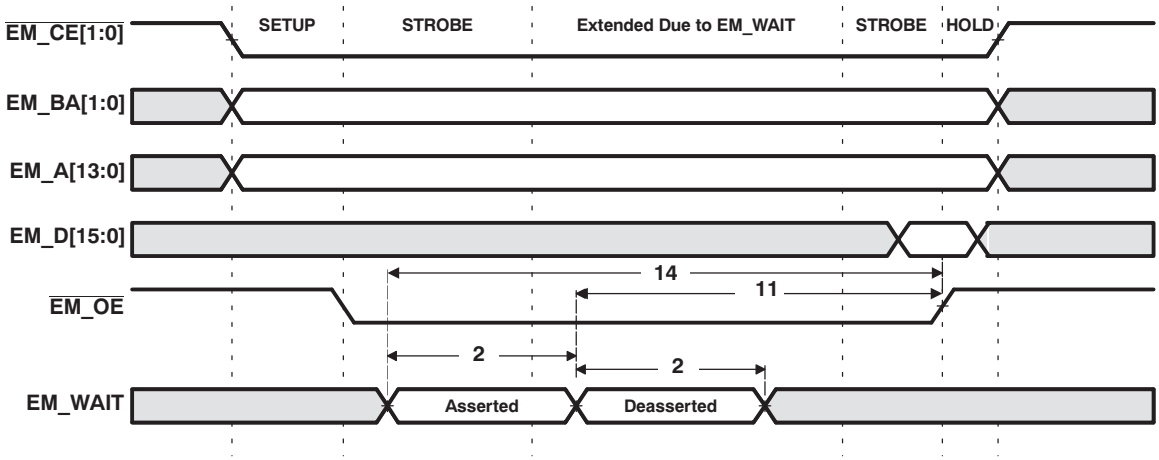

Figure 5-16. EM_WAIT Read Timing Requirements

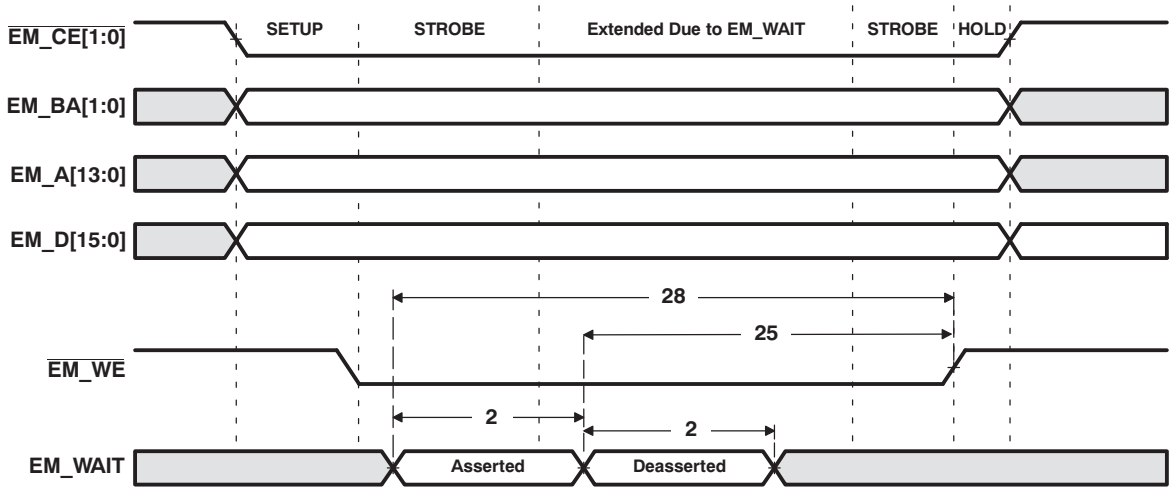

Figure 5-17. EM_WAIT Write Timing Requirements

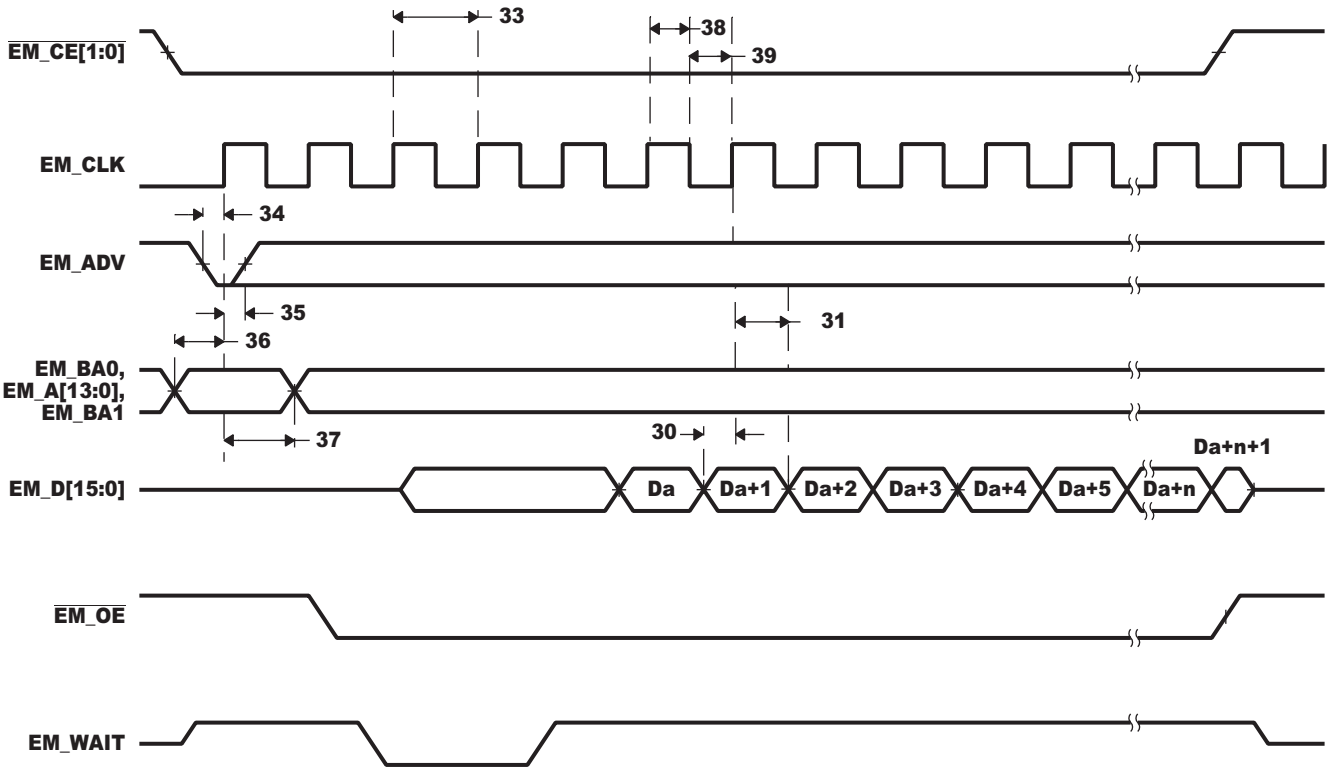

Figure 5-18. Synchronous OneNAND Flash Read Timing

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5.7.2 DDR2/mDDR Memory Controller

The DDR2 / mDDR Memory Controller is a dedicated interface to DDR2 / mDDR SDRAM. It supports JESD79D-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices. DDR2 / mDDR SDRAM plays a key role in a DM355-based system. Such a system is expected to require a significant amount of high-speed external memory for all of the following functions:

- Buffering of input image data from sensors or video sources
- Intermediate buffering for processing/resizing of image data in the VPFE
- Numerous OSD display buffers
- Intermediate buffering for large raw Bayer data image files while performing image processing functions
- Buffering for intermediate data while performing video encode and decode functions
- Storage of executable code for the ARM

The DDR2 / mDDR Memory Controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- Mobile DDR SDRAM
- 256 MByte memory space
- Data bus width 16 bits
- CAS latencies:
  - DDR2: 2, 3, 4, and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4, and 8
  - mDDR: 1, 2, and 4
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

For details on the DDR2 Memory Controller, refer to *TMS320DM35x Digital Media System-on-Chip (DMSoC) DDR2/mDDR Memory Controller Reference Guide* (literature number SPRUEH7).

5.7.2.1 DDR2/mDDR Memory Controller Electrical Data/Timing

The *Implementing DDR2/mDDR PCB Layout on the TMS320DM35x DMSoC* Application Report (literature number SPRAAR3) specifies a complete DDR2 and mDDR interface solution for the DM355 as well as a list of compatible DDR2/mDDR devices. TI has performed the simulation and system characterization to ensure all DDR2 and mDDR interface timings in this solution are met.

TI only supports board designs that follow the guidelines outlined in the *Implementing DDR2/mDDR PCB Layout on the TMS320DM35x DMSoC* Application Report (literature number SPRAAR3).

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5.8 MMC/SD

The DM355 includes two separate MMC/SD Controllers which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V1.1 and Secure Digital Input Output (SDIO) V1.0 specifications.

The DM355 MMC/SD Controller has following features:

- MultiMediaCard (MMC).
- Secure Digital (SD) Memory Card.
- MMC/SD protocol support.
- SDIO protocol support.
- Programmable clock frequency.
- 256 bit Read/Write FIFO to lower system overhead.
- Slave EDMA transfer capability.

The DM355 MMC/SD Controller does not support SPI mode.

5.8.1 MMC/SD Electrical Data/Timing

Table 5-15. Timing Requirements for MMC/SD Module (see Figure 5-20 and Figure 5-22)

NO.	PARAMETER		DM355				UNIT
			FAST MODE		STANDARD MODE		
			MIN	MAX	MIN	MAX	
1	$t_{su(CMDV-CLKH)}$	Setup time, SD_CMD valid before SD_CLK high	6		5		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, SD_CMD valid after SD_CLK high	2.5(1)		5		ns
3	$t_{su(DATV-CLKH)}$	Setup time, SD_DATx valid before SD_CLK high	6		5		ns
4	$t_{h(CLKH-DATV)}$	Hold time, SD_DATx valid after SD_CLK high	2.5		5		ns

(1) For this parameter, you may include margin in your board design so that the toh = 2.5 ns of the MMC/SD device is not degraded at the DM355 input pin.

Table 5-16. Switching Characteristics Over Recommended Operating Conditions for MMC/SD Module (see Figure 5-19 through Figure 5-22)

NO.	PARAMETER		DM355				UNIT
			FAST MODE		STANDARD MODE		
			MIN	MAX	MIN	MAX	
7	$f_{(CLK)}$	Operating frequency, SD_CLK	0	50	0	25	MHz
8	$f_{(CLK_ID)}$	Identification mode frequency, SD_CLK	0	400	0	400	KHz
9	$t_{W(CLKL)}$	Pulse width, SD_CLK low	7		10		ns
10	$t_{W(CLKH)}$	Pulse width, SD_CLK high	7		10		ns
11	$t_{r(CLK)}$	Rise time, SD_CLK		3		10	ns
12	$t_{f(CLK)}$	Fall time, SD_CLK		3		10	ns
13	$t_{d(CLKL-CMD)}$	Delay time, SD_CLK low to SD_CMD transition	-7.5	4	-7.5	14	ns
14	$t_{d(CLKL-DAT)}$	Delay time, SD_CLK low to SD_DATx transition	-7.5	4	-7.5	14	ns

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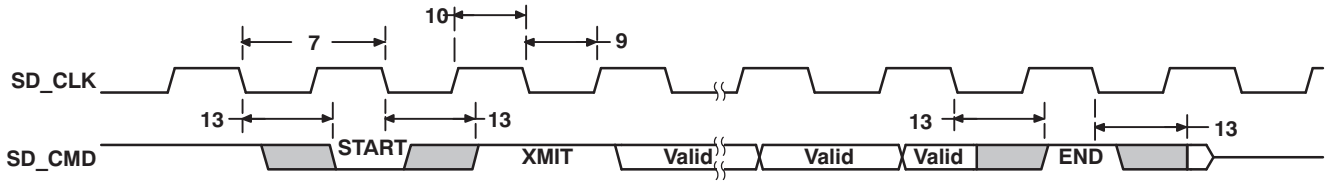

Figure 5-19. MMC/SD Host Command Timing

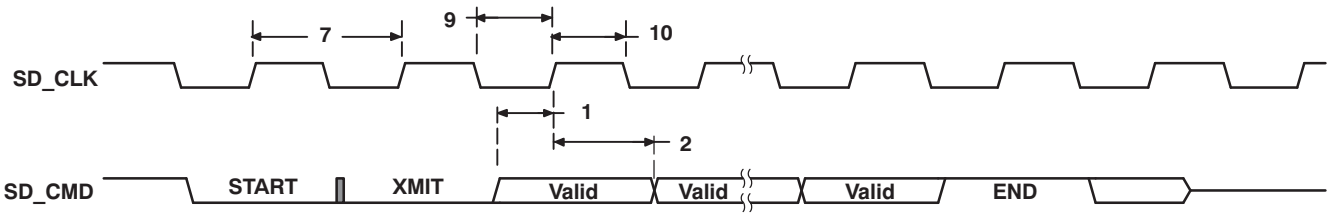

Figure 5-20. MMC/SD Card Response Timing

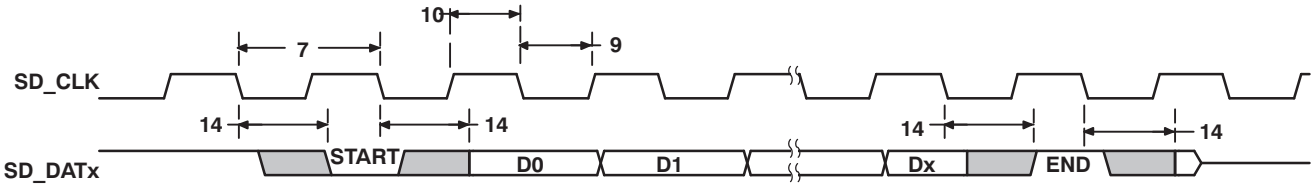

Figure 5-21. MMC/SD Host Write Timing

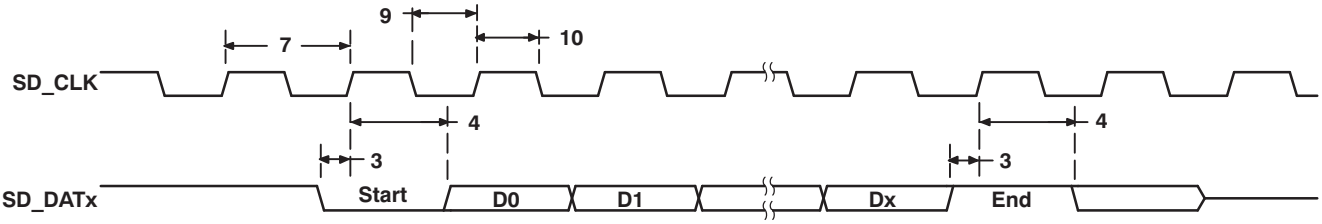

Figure 5-22. MMC/SD Host Read and Card CRC Status Timing

5.9 Video Processing Sub-System (VPSS) Overview

The DM355 contains a Video Processing Sub-System (VPSS) that provides an input interface (Video Processing Front End or VPFE) for external imaging peripherals such as image sensors, video decoders, etc.; and an output interface (Video Processing Back End or VPBE) for display devices, such as analog SDTV displays, digital LCD panels, HDTV video encoders, etc.

In addition to these peripherals, there is a set of common buffer memory and DMA control to ensure efficient use of the DDR2 burst bandwidth. The shared buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2. In order to efficiently utilize the external DDR2 bandwidth, the shared buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The shared buffer logic/memory also interfaces with all the VPFE and VPBE modules via a 128-bit wide bus. The shared buffer logic/memory (divided into the read & write buffers and arbitration logic) is capable of performing the following functions. It is imperative that the VPSS utilize DDR2 bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules. Because it is possible to configure the VPSS modules in such a way that DDR2 bandwidth is exceeded, a set of user accessible registers is provided to monitor overflows or failures in data transfers.

5.9.1 Video Processing Front-End (VPFE)

The VPFE or Video Processing Front-End block is comprised of the CCD Controller (CCDC), Image Pipe (IPIPE), and Hardware 3A Statistic Generator (H3A). These modules are described in the sections that follow.

5.9.1.1 CCD Controller (CCDC)

The CCDC is responsible for accepting raw (unprocessed) image/video data from a sensor (CMOS or CCD). In addition, the CCDC can accept YUV video data in numerous formats, typically from so-called video decoder devices. In the case of raw inputs, the CCDC output requires additional image processing to transform the raw input image to the final processed image. This processing can be done either on-the-fly in the Preview Engine hardware ISP or in software on the ARM and MPEG4/JPEG coprocessor subsystems. In parallel, raw data input to the CCDC can also used for computing various statistics (3A, Histogram) to eventually control the image/video tuning parameters. The CCDC is programmed via control and parameter registers. DM355 performance is enhanced by its dedicated hard-wired MPEG4/JPEG coprocessor (MJCP). The MJCP performs all the computational operations required for JPEG and MPEG4 compression. These operations can be invoked using the xDM (xDIAS for Digital Media) APIs. For more information, refer to the *xDIAS-DM (xDIAS for Digital Media) User's Guide* (literature number SPRUEC8). The following features are supported by the CCDC module.

- Support for conventional Bayer pattern.
- Generates HD/VD timing signals and field ID to an external timing generator or can synchronize to the external timing generator.
- Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors).
- Support for up to 75-MHZ sensor pixel clock if H3A is not used, otherwise the pixel clock must be less than 67.5 MHZ
- Support for ITU-R BT.656 standard format, either 8-bit or 16-bit.
- Support for YCbCr 422 format, either 8- or 16-bit with discrete HSYNC and VSYNC signals.
- Support for up to 14-bit input.
- Support for color space conversion
- Generates optical black clamping signals.
- Support for shutter signal control.
- Support for digital clamping and black level compensation.

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- Fault pixel correction based on a lookup table that contains row and column position of the pixel to be corrected.
- Support for program lens shading correction.
- Support for 10-bit to 8-bit A-law compression.
- Support for a low-pass filter prior to writing to SDRAM. If this filter is enabled, 2 pixels each in the left and right edges of each line are cropped from the output.
- Support for generating output to range from 14-bits to 8-bits wide (8-bits wide allows for 50% saving in storage area).
- Support for down sampling via programmable culling patterns.
- Ability to control output to the DDR2 via an external write enable signal.
- Support for up to 32K pixels (image size) in both the horizontal and vertical direction.

5.9.1.2 IPIPE - Image Pipe

The hardware Image Pipe (IPIPE) is a programmable hardware image processing module that is responsible for transforming raw (unprocessed) image/video data from a sensor (CMOS or CCD) into YCbCr 422 data that is amenable for compression or display. The IPIPE can also be configured to operate in a resize only mode, which allows YCbCr 422 to be resized without applying the processing of every module in the IPIPE. Typically, the output of the IPIPE is used for both video compression and displaying it on an external display device such as a NTSC/PAL analog encoder or a digital LCD. The IPIPE is programmed via control and parameter registers. The following features are supported by the IPIPE.

- The input interface extracts valid raw data from the CCD raw data, and then various modules in IPIPE process the raw CCD data.
- The 2D noise filter module reduces impulse noise in the raw data and adjusts the resolution of the input image.
- The 2D pre-filter adjusts the resolution of the input image and remove line crawl noise.
- The white balance module applies two gain adjustments to the data: a digital gain (total gain) and a white balance gain.
- The Color Filter Array (CFA) interpolation module implements CFA interpolation. The output from the CFA interpolation module is always RGB formatted data.
- The RGB2RGB blending module applies a 3x3 matrix transform to the RGB data generated by the CFA interpolation module.
- The gamma correction module independently applies gamma correction to each RGB component. Gamma is implemented using a piece-wise linear interpolation approach with a 512 entry look up table for each color.
- The RGB2YCbCr conversion module applies 3x3 matrix transformation to the RGB data to convert it to YCbCr data. This module also implements offset.
- The 4:2:2 conversion module applies the chroma low pass filter and down samples Cb and Cr, so that IPIPE output data is in YCbCr-4:2:2 format.
- The 2D edge enhancer module improves image clarity with luminance non-linear filter. This module also has contrast and brightness adjustment functions.
- The chroma suppression module reduces faulty-color using luminance (Y) value or high-pass-filtering Y value. The H-resizer and V-resizer modules resize horizontal and vertical image sizes, respectively.
- The output interface module transfers data from IPIPE to SDRAM, in the form of YCbCr-422 or RGB (32bit/16bit).
- The histogram function can record histograms of up to 4 distinct areas into up to 256 bins.
- IPIPE has three different processing paths:
  - Case 1: The CCD raw data directly leads to IPIPE and stores the YCbCr (or RGB) data to SDRAM.
  - Case 2: IPIPE reads CCD raw data and stores the Bayer pattern data after white balance to SDRAM.

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– Case 3: IPIPE reads YCbCr-422 data and apply edge enhance, chroma suppression and Resize to output YCbCr (or RGB) data to SDRAM.

5.9.1.3 Hardware 3A (H3A)

The H3A module is designed to support the control loops for Auto Focus, Auto White Balance and Auto Exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are 2 main blocks in the H3A module:

- Auto Focus (AF) engine
- Auto Exposure (AE) Auto White Balance (AWB) engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a "paxel" for the case of AF.

The AE/AWB Engine accumulates the values and checks for saturated values in a sub sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a "window". Thus, other than referring them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

The following features are supported by the AF engine:

- Support for input from DDR2 / mDDR SDRAM (in addition to the CCDC port)
- Support for a Peak Mode in a Paxel (a Paxel is defined as a two dimensional block of pixels).
- Accumulate the maximum Focus Value of each line in a Paxel
- Support for an Accumulation/Sum Mode (instead of Peak mode).
- Accumulate Focus Value in a Paxel.
- Support for up to 36 Paxels in the horizontal direction and up to 128 Paxels in the vertical direction. The number of horizontal paxels is limited by the memory size (and cost), while the vertical number of paxels is not. Therefore, the number of paxels in horizontal direction is smaller than the number of paxels in vertical direction.
- Programmable width and height for the Paxel. All paxels in the frame will be of same size.
- Programmable red, green, and blue position within a 2x2 matrix.
- Separate horizontal start for paxel and filtering.
- Programmable vertical line increments within a paxel.
- Parallel IIR filters configured in a dual-biquad configuration with individual coefficients (2 filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.

The following features are supported by the AE/AWB engine:

- Support for input from DDR2 / mDDR SDRAM (in addition to the CCDC port)
- Accumulate clipped pixels along with all non-saturated pixels
- Support for up to 36 horizontal windows.
- Support for up to 128 vertical windows.
- Programmable width and height for the windows. All windows in the frame will be of same size.
- Separate vertical start co-ordinate and height for a black row of paxels that is different than the remaining color paxels.
- Programmable Horizontal Sampling Points in a window
- Programmable Vertical Sampling Points in a window

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5.9.1.4 VPFE Electrical Data/Timing

Table 5-17. Timing Requirements for VPFE PCLK Master/Slave Mode(1) (see Figure 5-23)

NO.	PARAMETER			MIN	MAX	UNIT
1	$t_{c(PCLK)}$	Cycle time, PCLK	H3A not used	13.33 or P(2)	100	ns
			H3A used	2P + 1	100	ns
2	$t_{w(PCLKH)}$	Pulse duration, PCLK high		5.7		ns
3	$t_{w(PCLKL)}$	Pulse duration, PCLK low		5.7		ns
4	$t_{t(PCLK)}$	Transition time, PCLK			3	ns

(1) P = 1/SYSCLK4 in nanoseconds (ns). For example, if the SYSCLK4 frequency is 135 MHz, use P = 7.41 ns. See Section 3.5 , *Device Clocking*, for more information on the supported clock configurations of the DM355.
(2) Use whichever value is greater.

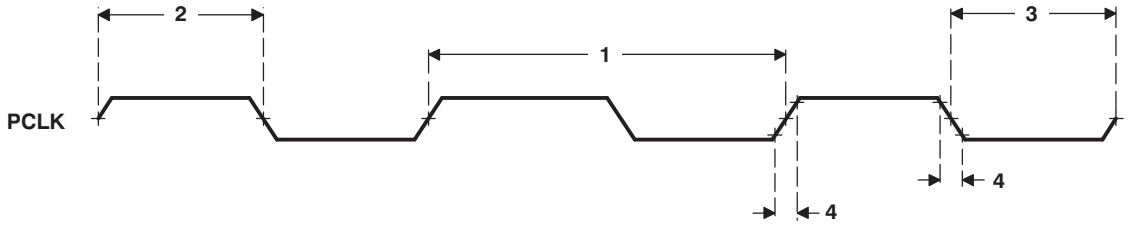

Figure 5-23. VPFE PCLK Timing

Table 5-18. Timing Requirements for VPFE (CCD) Slave Mode (see Figure 5-24)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
5	$t_{su(CCDV-PCLK)}$	Setup time, CCD valid before PCLK edge	3		ns
6	$t_{h(PCLK-CCDV)}$	Hold time, CCD valid after PCLK edge	2		ns
7	$t_{su(HDV-PCLK)}$	Setup time, HD valid before PCLK edge	3		ns
8	$t_{h(PCLK-HDV)}$	Hold time, HD valid after PCLK edge	2		ns
9	$t_{su(VDV-PCLK)}$	Setup time, VD valid before PCLK edge	3		ns
10	$t_{h(PCLK-VDV)}$	Hold time, VD valid after PCLK edge	2		ns
11	$t_{su(CAM_WEN_FIELDV-PCLK)}$	Setup time, CAM_WEN_FIELD valid before PCLK edge	3		ns
12	$t_{h(CAM_WEN_FIELDV-PCLK)}$	Hold time, C_WEN_FIELD valid after PCLK edge	2		ns

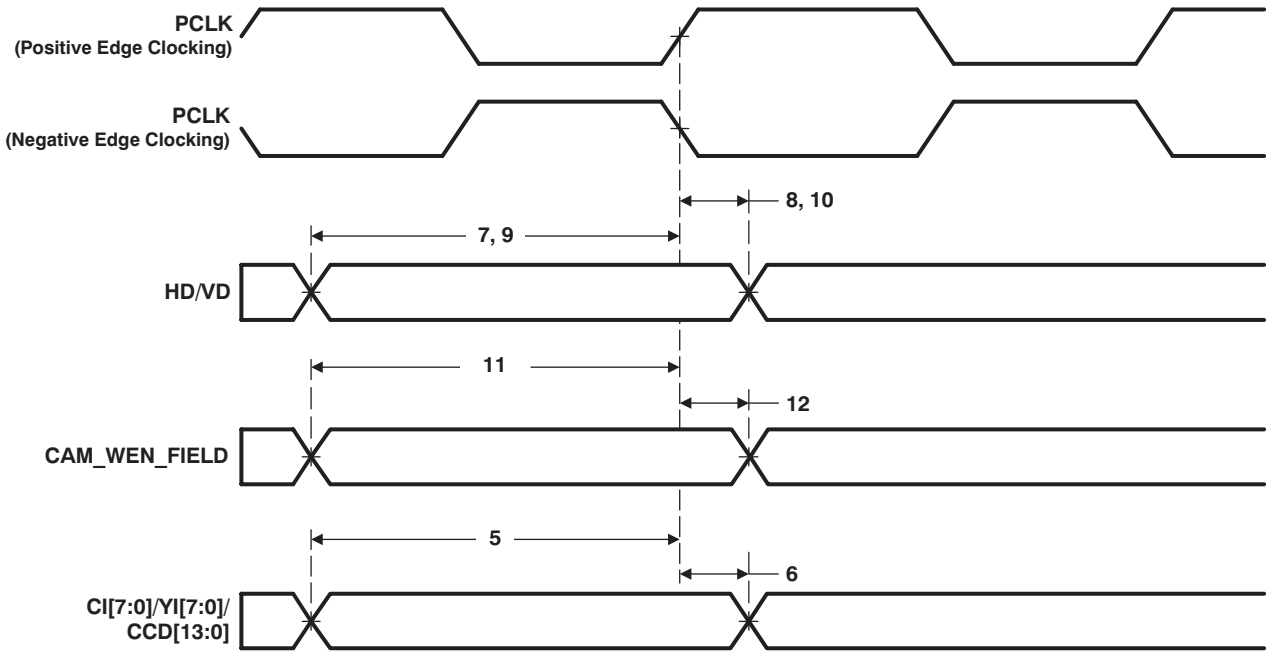

Figure 5-24. VPFE (CCD) Slave Mode Input Data Timing

Table 5-19. Timing Requirements for VPFE (CCD) Master Mode(1) (see Figure 5-25)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
15	$t_{su(CCDV-PCLK)}$	Setup time, CCD valid before PCLK edge	3		ns
16	$t_{h(PCLK-CCDV)}$	Hold time, CCD valid after PCLK edge	2		ns
23	$t_{su(CAM_WEN_FIELDV-PCLK)}$	Setup time, CAM_WEN_FIELD valid before PCLK edge	3		ns
24	$t_{h(PCLK-CAM_WEN_FIELDV)}$	Hold time, CAM_WEN_FIELD valid after PCLK edge	2		ns

(1) The VPFE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode the rising edge of PCLK is referenced. When in negative edge clocking mode the falling edge of PCLK is referenced.

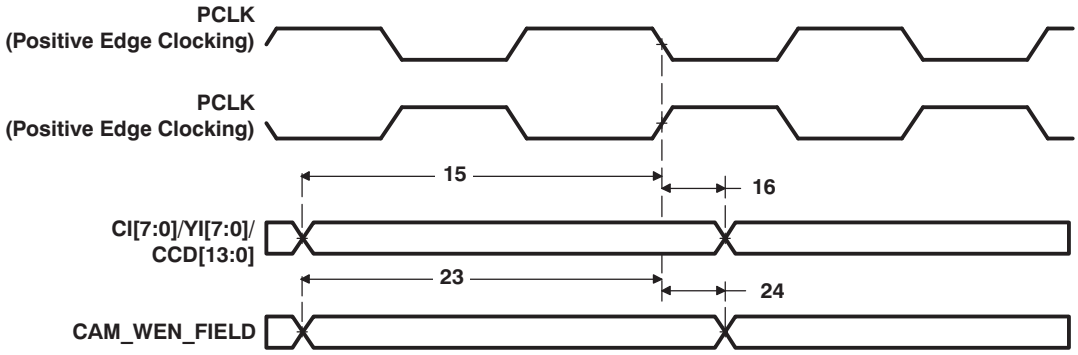

Figure 5-25. VPFE (CCD) Master Mode Input Data Timing

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Table 5-20. Switching Characteristics Over Recommended Operating Conditions for VPFE (CCD) Master Mode (see Figure 5-26)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
18	$t_{d(PCLKL-HDIV)}$	Delay time, PCLK edge to HD invalid	3	11	ns
20	$t_{d(PCLKL-VDIV)}$	Delay time, PCLK edge to VD invalid	3	11	ns

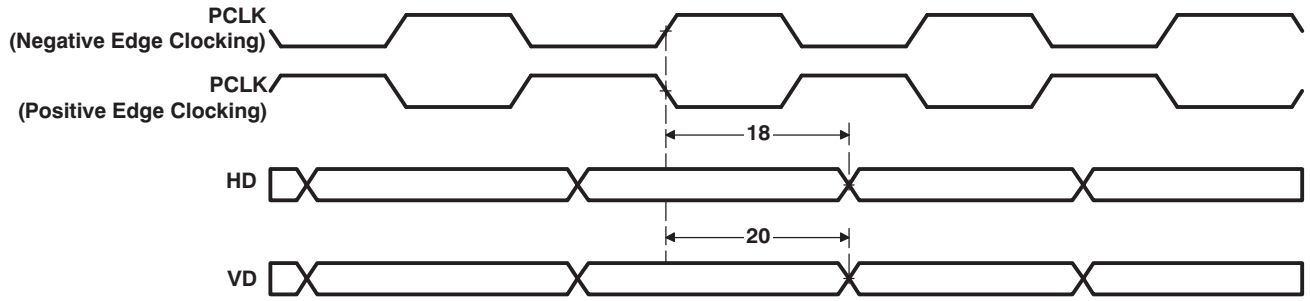

Figure 5-26. VPFE (CCD) Master Mode Control Output Data Timing

5.9.2 Video Processing Back-End (VPBE)

The Video Processing Back-End of VPBE module is comprised of the On Screen Display (OSD) module and the Video Encoder / Digital LCD Controller (VENC/DLCD).

5.9.2.1 On-Screen Display (OSD)

The primary function of the OSD module is to gather and blend video data and display/bitmap data and then pass it to the Video Encoder (VENC) in YCbCr format. The video and display data is read from external DDR2/mDDR memory. The OSD is programmed via control and parameter registers. The following are the primary features that are supported by the OSD.

- Support for two video windows and two OSD bitmapped windows that can be displayed simultaneously (VIDWIN0/VIDWIN1 and OSDWIN0/OSDWIN1).
- Video windows supports YCbCr data in 422 format from external memory, with the ability to interchange the order of the CbCr component in the 32-bit word
- OSD bitmap windows support ½/4/8 bit width index data of color palette
- In addition one OSD bitmap window at a time can be configured to one of the following:
  - YUV422 (same as video data)
  - RGB format data in 16-bit mode (R=5bit, G=6bit, B=5bit)
  - 24-bit mode (each R/G/B=8bit) with pixel level blending with video windows
- Programmable color palette with the ability to select between a RAM/ROM table with support for 256 colors.
- Support for 2 ROM tables, one of which can be selected at a given time
- Separate enable/disable control for each window
- Programmable width, height, and base starting coordinates for each window
- External memory address and offset registers for each window
- Support for x2 and x4 zoom in both the horizontal and vertical direction
- Pixel-level blending/transparency/blinking attributes can be defined for OSDWIN0 when OSDWIN1 is configured as an attribute window for OSDWIN0.
- Support for blinking intervals to the attribute window
- Ability to select either field/frame mode for the windows (interlaced/progressive)
- An eight step blending process between the bitmap and video windows
- Transparency support for the bitmap and video data (when a bitmap pixel is zero, there will be no

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blending for that corresponding video pixel)

- Ability to resize from VGA to NTSC/PAL (640x480 to 720x576) for both the OSD and video windows
- Horizontal rescaling x1.5 is supported
- Support for a rectangular cursor window and a programmable background color selection.
- The width, height, and color of the cursor is selectable
- The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module.

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another uses ROM.

5.9.2.2 Video Encoder / Digital LCD Controller (VENC/DLCD)

The VENC/DLCD consists of three major blocks; a) the video encoder that generates analog video output, b) the digital LCD controller that generates digital RGB/YCbCr data output and timing signals, and c) the timing generator.

The video encoder for analog video supports the following features:

- Master Clock Input - 27 MHz (x2 Upsampling)
- Programmable Timing Generator
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - Non-Interlace option
  - CGMS/WSS
  - Line 21 Closed Caption Data Encoding
  - Chroma Low Pass Filter 1.5MHz/3MHz
  - Programmable SC-H phase
- 10-bit Over-Sampling D/A Converter (27MHz)
- Internal analog video buffer
- Optional 7.5% Pedestal
- 16-235/0-255 Input Amplitude Selectable
- Programmable Luma Delay
- Master/Slave Operation
- Internal Color Bar Generation (75%)

The digital LCD controller supports the following features:

- Programmable DCLK
- Programmable Timing Generator
- Various Output Format
  - YCbCr 16bit
  - YCbCr 8bit
  - ITU-R BT. 656
  - Parallel RGB 16-bit/18-bit
  - Serial 8-bit RGB
- Low Pass Filter for Digital RGB Output

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- Master/Slave Operation
- Internal Color Bar Generation (100%/75%)
- YUV/RGB modes support HDTV output (720p/1080i) with 74.25 MHz external clock input

5.9.2.3 VPBE Electrical Data/Timing

Table 5-21. Timing Requirements for VPBE CLK Inputs (see Figure 5-27)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{c(PCLK)}$	Cycle time, PCLK(1)	13.33	160	ns
2	$t_{w(PCLKH)}$	Pulse duration, PCLK high	5.7		ns
3	$t_{w(PCLKL)}$	Pulse duration, PCLK low	5.7		ns
4	$t_{t(PCLK)}$	Transition time, PCLK		3	ns
5	$t_{c(EXTCLK)}$	Cycle time, EXTCLK	13.33	160	ns
6	$t_{w(EXTCLKH)}$	Pulse duration, EXTCLK high	5.7		ns
7	$t_{w(EXTCLKL)}$	Pulse duration, EXTCLK low	5.7		ns
8	$t_{t(EXTCLK)}$	Transition time, EXTCLK		3	ns

(1) For timing specifications relating to PCLK see Table 5-17 , *Timing Requirements for VPFE PCLK Master/Slave Mode*.

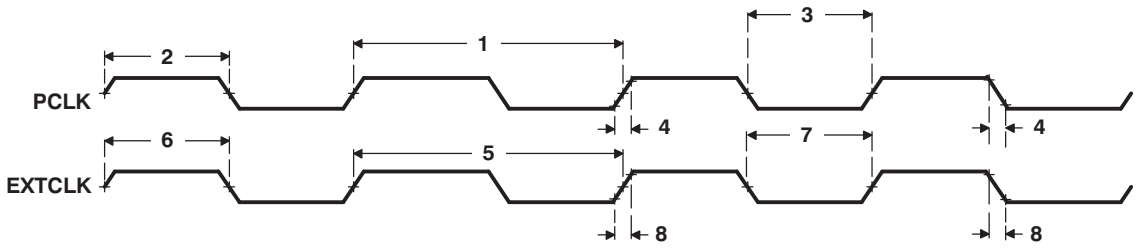

Figure 5-27. VPBE PCLK and EXTCLK Timing

Table 5-22. Timing Requirements for VPBE Control Input With Respect to PCLK and EXTCLK(1) (2) (3) (see Figure 5-28)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
9	$t_{su(VCTLV-VCLKIN)}$	Setup time, VCTL valid before VCLKIN edge	2		ns
10	$t_{h(VCLKIN-VCTLV)}$	Hold time, VCTL valid after VCLKIN edge	1		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLKIN is referenced. When in negative edge clocking mode, the falling edge of VCLKIN is referenced.
(2) VCTL = HSYNC, VSYNC, and FIELD
(3) VCLKIN = PCLK or EXTCLK

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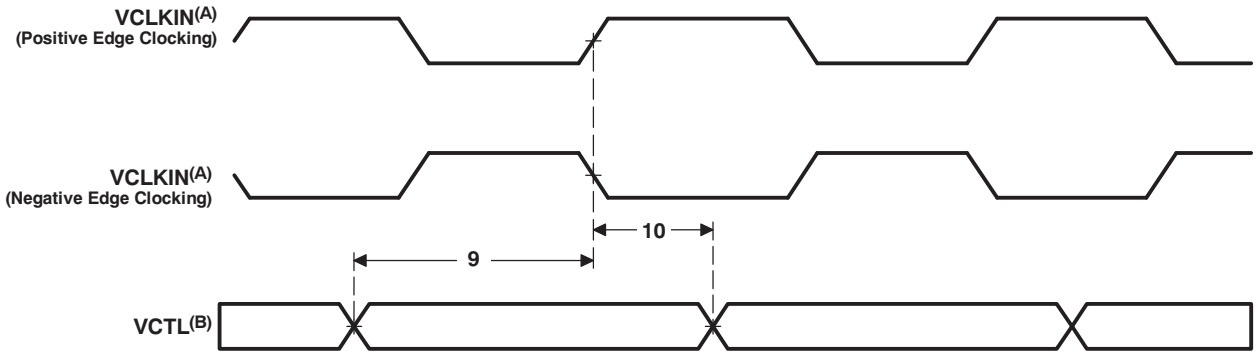


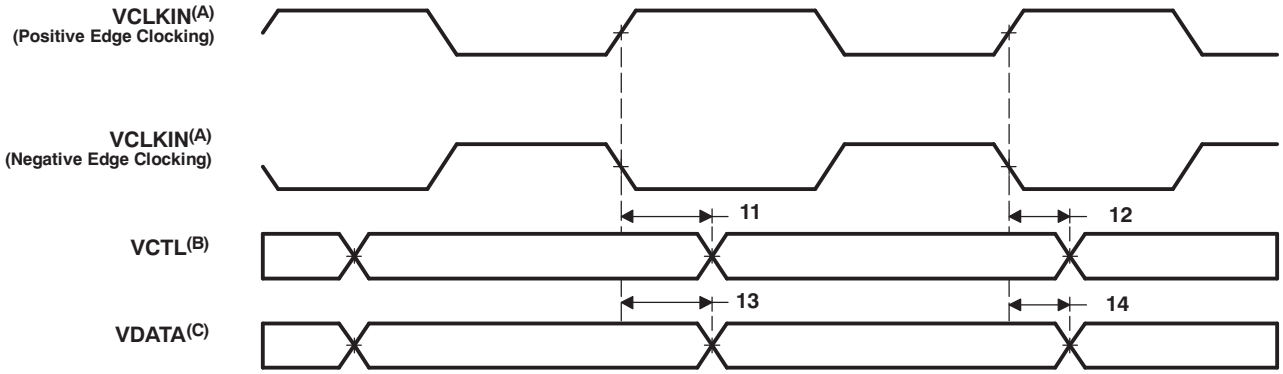
A. VCLKIN = PCLK or EXTCLK
B. VCTL = HSYNC, VSYNC, and FIELD

Figure 5-28. VPBE Input Timing With Respect to PCLK and EXTCLK

Table 5-23. Switching Characteristics Over Recommended Operating Conditions for VPBE Control and Data Output With Respect to PCLK and EXTCLK(1) (2) (3) (see Figure 5-29)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
11	$t_{d(VCLKIN-VCTLV)}$	Delay time, VCLKIN edge to VCTL valid		13.3	ns
12	$t_{d(VCLKIN-VCTLIV)}$	Delay time, VCLKIN edge to VCTL invalid	2		ns
13	$t_{d(VCLKIN-VDATAV)}$	Delay time, VCLKIN edge to VDATA valid		13.3	ns
14	$t_{d(VCLKIN-VDATAIV)}$	Delay time, VCLKIN edge to VDATA invalid	2		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLKIN is referenced. When in negative edge clocking mode, the falling edge of VCLKIN is referenced.
(2) VCLKIN = PCLK or EXTCLK
(3) VCTL = HSYNC, VSYNC, FIELD, and LCD_OE



A. VCLKIN = PCLK or EXTCLK
B. VCTL = HSYNC, VSYNC, FIELD, and LCD_OE
C. VDATA = COUT[7:0], YOUT[7:0], R[7:3], G[7:2], and B[7:3]

Figure 5-29. VPBE Control and Data Output With Respect to PCLK and EXTCLK

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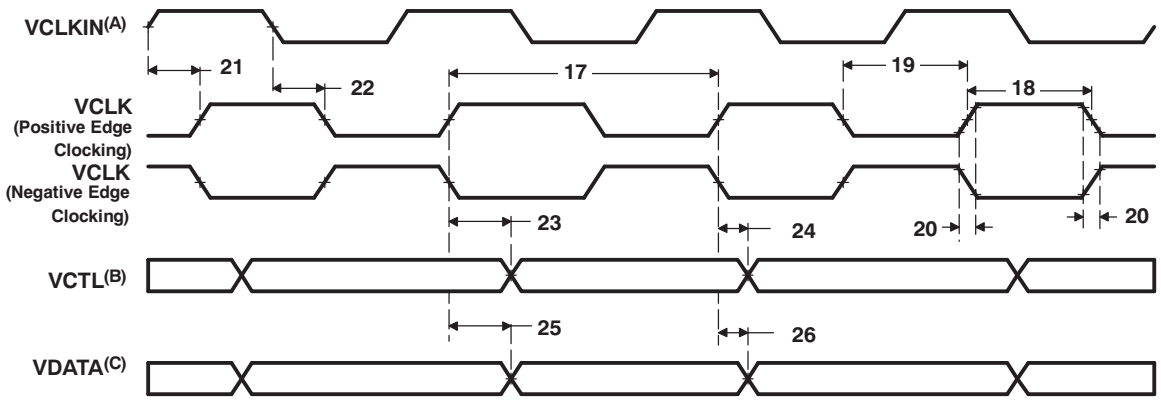
Table 5-24. Switching Characteristics Over Recommended Operating Conditions for VPBE Control and Data Output With Respect to VCLK(1) (2) (see Figure 5-30)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
17	$t_{c(VCLK)}$	Cycle time, VCLK	13.33	160	ns
18	$t_{w(VCLKH)}$	Pulse duration, VCLK high	5.7		ns
19	$t_{w(VCLKL)}$	Pulse duration, VCLK low	5.7		ns
20	$t_{t(VCLK)}$	Transition time, VCLK		3	ns
21	$t_{d(VCLKINH-VCLKH)}$	Delay time, VCLKIN high to VCLK high	2	12	ns
22	$t_{d(VCLKINL-VCLKL)}$	Delay time, VCLKIN low to VCLK low	2	12	ns
23	$t_{d(VCLK-VCTLV)}$	Delay time, VCLK edge to VCTL valid		4	ns
24	$t_{d(VCLK-VCTLIV)}$	Delay time, VCLK edge to VCTL invalid	0		ns
25	$t_{d(VCLK-VDATAV)}$	Delay time, VCLK edge to VDATA valid		4	ns
26	$t_{d(VCLK-VDATAIV)}$	Delay time, VCLK edge to VDATA invalid	0		ns

(1) The VPBE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode, the rising edge of VCLK is referenced. When in negative edge clocking mode, the falling edge of VCLK is referenced.
(2) VCLKIN = PCLK or EXTCLK. For timing specifications relating to PCLK, see Table 5-17 , *Timing Requirements for VPFE PCLK Master/Slave Mode*.



A. VCLKIN = PCLK or EXTCLK
B. VCTL = HSYNC, VSYNC, FIELD, and LCD_OE
C. VDATA = COUT[7:0], YOUT[7:0], R[7:3], G[7:2], and B[7:3]

Figure 5-30. VPBE Control and Data Output Timing With Respect to VCLK

5.9.2.4 DAC and Video Buffer Electrical Data/Timing

The DAC and video buffer can be configured in a DAC only configuration or in a DAC and video buffer configuration. In the DAC only configuration the internal video buffer is not used and an external video buffer is attached to the DAC. In the DAC and video buffer configuration, the DAC and internal video buffer are both used and a TV cable may be attached directly to the output of the video buffer. See Figure 5-31 and Figure 5-32 for recommenced circuits for each configuration.

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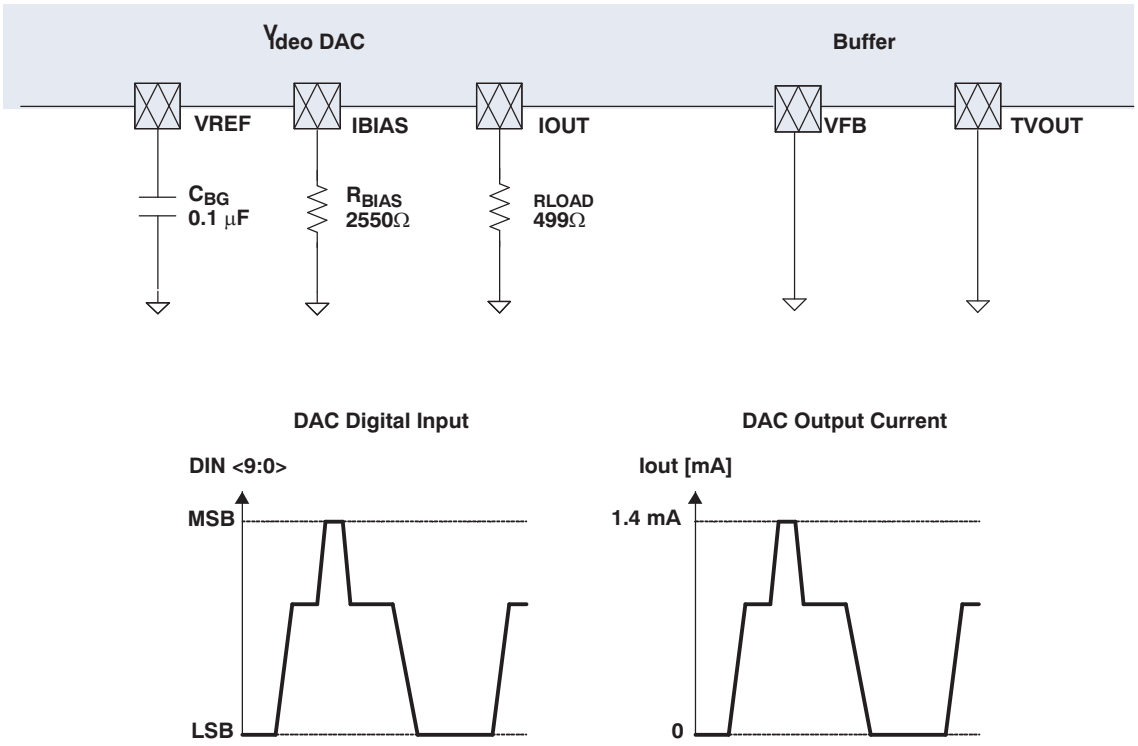

A. Connect IOUT to a high-impedance video buffer device.

B. Place capacitors and resistors as close as possible to the DM355.

C. Configure the VDAC_CONFIG register in the system control module as follows: DINV = 0, PWD_GBZ = 1, PWD_VBUFZ = 0, ACCUP_EN = X. See the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) and the *TMS320DM35x Digital Media System-on-Chip Video Processing Back End (VPBE) Reference Guide* (literature number SPRUF72) for more information on VDAC_CONFIG.

Figure 5-31. DAC Only Application Example

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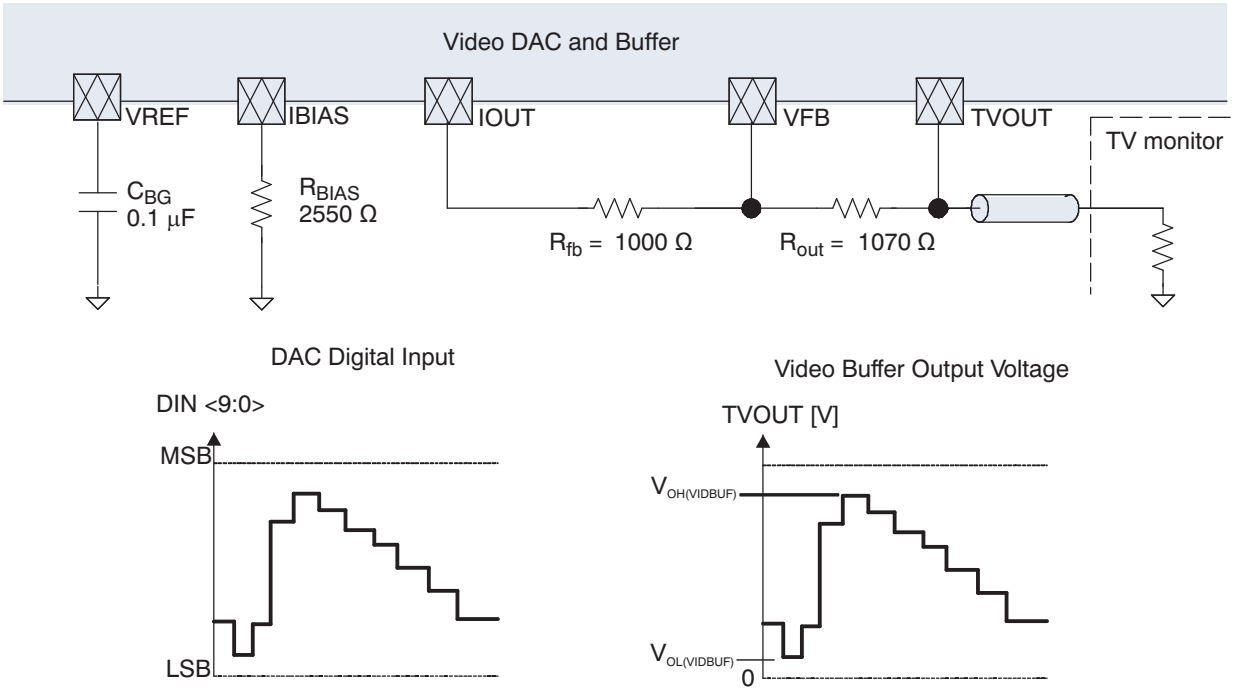

A. Place capacitors and resistors as close as possible to the DM355.

B. You must use the circuit shown in this diagram. Also you must configure the VDAC_CONFIG register in the System Control module as follows: TRESB4R4 = 0x3, TRESB4R2 = 0x8, TRESB4R1 = 0x8, TRIMBITS = 0x34, PWD_BGZ = 1 (power up VREF), SPEED = 1 (faster), TVINT = don't care, PWD_VBUFZ = 1 (power up video buffer), VREFSET = don't care, ACCUP_EN = 0 (no A/C coupling), DINV = 1 (invert). See *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (literature number SPRUFB3) and the *TMS320DM35x Digital Media System-on-Chip Video Processing Back End (VPBE) Reference Guide* (literature number SPRUF72) for more information on the VDAC_CONFIG register and Video Buffer.

C. For proper TVOUT voltage, you must connect the pin TVOUT directly to the TV. No A/C coupling capacitor or termination resistor is necessary on your DM355 board. Also, it is assumed that the TV has no internal A/C coupling capacitor but does have an internal termination resistor, as shown in this diagram. TVOUT voltage will range from $V_{OL(VIDBUF)}$ to $V_{OH(VIDBUF)}$. See Section 4.3 for the voltage specifications.

Figure 5-32. DAC With Buffer Circuit

5.10 USB 2.0

The DM355 USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- Four Transmit (TX) and four Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K bytes shared by all endpoints.
  - Programmable FIFO size
- Includes a DMA sub-module that supports four TX and four RX channels of CPPI 3.0 DMAs
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB
- USB OTG extensions, i.e. session request protocol (SRP) and host negotiation protocol (HNP)

The DM355 USB2.0 peripheral does not support the following features:

- On-chip charge pump
- High bandwidth ISO mode is not supported (triple buffering)
- RNDIS mode acceleration for USB sizes that are not multiples of 64 bytes
- Endpoint max USB packet sizes that do not conform to the USB 2.0 spec (for FS/LS: 8, 16, 32, 64, and 1023 are defined; for HS: 64, 128, 512, and 1024 are defined)

5.10.1 USB2.0 Electrical Data/Timing

Table 5-25. Switching Characteristics Over Recommended Operating Conditions for USB2.0 (see Figure 5-33)

NO.	PARAMETER		DM355						UNIT
			LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED(1) 480 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(2)	75	300	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(2)	75	300	4	20	0.5		ns
3	t_{frfm}	Rise/Fall time, matching(3)	80	125	90	111.11			%
4	V_{CRS}	Output signal cross-over voltage(2)	1.3	2	1.3	2			V
5	$t_{jr(source)NT}$	Source (Host) Driver jitter, next transition		2		2			ns
	$t_{jr(FUNC)NT}$	Function Driver jitter, next transition		25		2			ns
6	$t_{jr(source)PT}$	Source (Host) Driver jitter, paired transition(4)		1		1			ns
	$t_{jr(FUNC)PT}$	Function Driver jitter, paired transition		10		1			ns
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175			ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver	670		82				ns
9	$t_{(DRATE)}$	Data Rate		1.5		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	–	–	28	49.5	40.5	49.5	Ω

(1) For more detailed specification information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.
(2) Low Speed: C_L = 200 pF, Full Speed: C_L = 50 pF, High Speed: C_L = 50 pF
(3) $t_{frfm} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

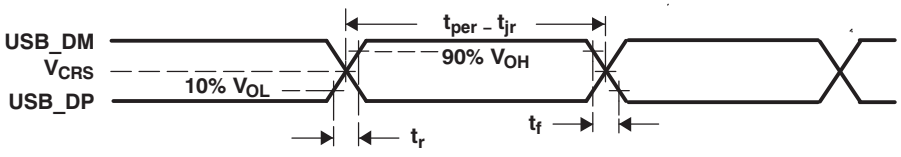

Figure 5-33. USB2.0 Integrated Transceiver Interface Timing

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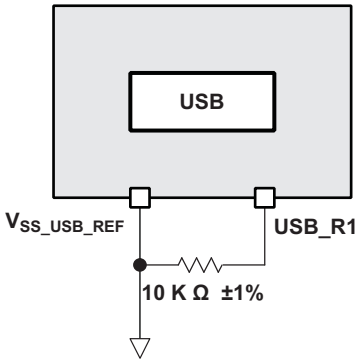

Figure 5-34. USB Reference Resistor Routing

5.11 Universal Asynchronous Receiver/Transmitter (UART)

The DM355 contains 3 separate UART modules (1 with hardware flow control). These modules performs serial-to-parallel conversion on data received from a peripheral device or modem, and parallel-to-serial conversion on data received from the CPU. Each UART also includes a programmable baud rate generator capable of dividing the 24MHz reference clock by divisors from 1 to 65,535 to produce a 16 x clock driving the internal logic. The UART modules support the following features:

- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- 16-byte storage space for both the transmitter and receiver FIFOs
- Unique interrupts, one for each UART
- Unique EDMA events, both received and transmitted data for each UART
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- Programmable auto-rts and auto-cts for autoflow control (supported on UART2)
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions: CTS, RTS (supported on UART2)

5.11.1 UART Electrical Data/Timing

Table 5-26. Timing Requirements for UARTx Receive (see Figure 5-35)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (RXDn)	0.99U(1)	1.05U(1)	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.99U(1)	1.05U(1)	ns

(1) U = UART baud time = 1/programmed baud rate.

Table 5-27. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit (see Figure 5-35)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$f_{(baud)}$	UART0/1 Maximum programmable baud rate		1.5	MHz
		UART2 Maximum programmable baud rate		5	
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (TXDn)	U - 2(1)	U + 2(1)	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit	U - 2(1)	U + 2(1)	ns

(1) U = UART baud time = 1/programmed baud rate.

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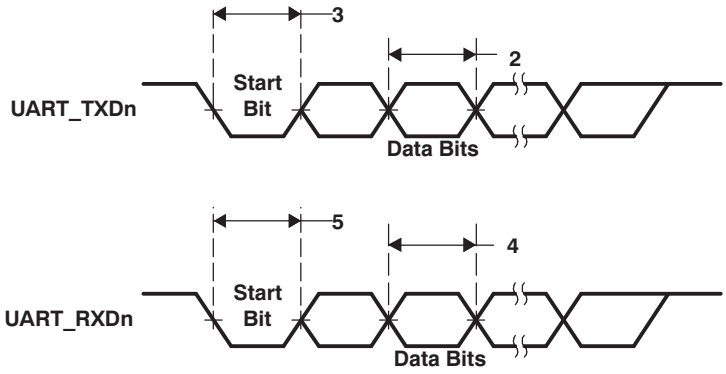

Figure 5-35. UART Transmit/Receive Timing

5.12 Serial Port Interface (SPI)

The DM355 contains 3 separate SPI modules. These modules provide a programmable length shift register which allows serial communication with other SPI devices through a 3 or 4 wire interface (Clock, Data In, Data Out, and Enable). The SPI supports the following features:

- Master mode operation
- 2 chip selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface (Clock, Data In, Data Out, and Enable)
- Unique interrupt for each SPI port
- Separate DMA events for SPI Receive and Transmit
- 16-bit shift register
- Receive buffer register
- Programmable character length (2 to 16 bits)
- Programmable SPI clock frequency range
- 8-bit clock prescaler
- Programmable clock phase (delay or no delay)
- Programmable clock polarity

The SPI modules do not support the following features:

- Slave mode. Only Master mode is supported in DM355 (Master mode means that DM355 provides the serial clock).
- GPIO mode. GPIO functionality is supported by the GIO modules for those SPI pins that are multiplexed with GPIO signals.

5.12.1 SPI Electrical Data/Timing

Table 5-28. Timing Requirements for SPI (All Modes)(1) (see Figure 5-36)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, SPI_CLK	37.$\overline{037}$ ns		ns
2	$t_{w(CLKH)}$	Pulse duration, SPI_CLK high (All Master Modes)	0.45*T	0.55*T	ns
3	$t_{w(CLKL)}$	Pulse duration, SPI_CLK low (All Master Modes	0.45*T	0.55*T	ns

(1) T = $t_{c(CLK)}$ = SPI_CLK period is equal to the SPI module clock divided by a configurable divider.

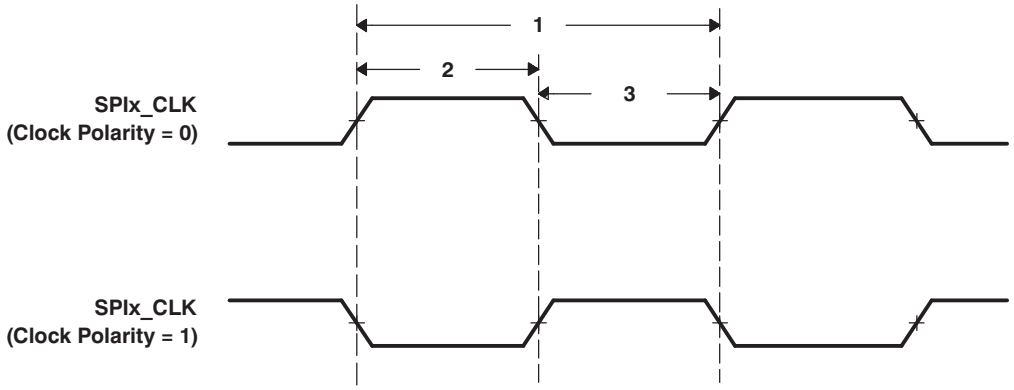

Figure 5-36. SPI_CLK Timing

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SPI Master Mode Timings (Clock Phase = 0)

Table 5-29. Timing Requirements for SPI Master Mode [Clock Phase = 0] (1)(see Figure 5-37)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
4	$t_{su(DIV-CLKL)}$	Setup time, SPI_DI (input) valid before SPI_CLK (output) falling edge	Clock Polarity = 0	.5P + 3		ns
5	$t_{su(DIV-CLKH)}$	Setup time, SPI_DI (in put) valid before SPI_CLK (output) rising edge	Clock Polarity = 1	.5P + 3		ns
6	$t_{h(CLKL-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) falling edge	Clock Polarity = 0	.5P + 3		ns
7	$t_{h(CLKH-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) rising edge	Clock Polarity = 1	2.5P + 3		ns

(1) P = 1/SYSCLK2 in nanoseconds (ns). For example, if the SYSCLK2 frequency is 135 MHz, use P = 7.41 ns. See Section 3.5 , *Device Clocking*, for more information on the supported clock configurations of the DM355.

Table 5-30. Switching Characteristics Over Recommended Operating Conditions for SPI Master Mode [Clock Phase = 0] (see Figure 5-37)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
8	$t_{d(CLKH-DOV)}$	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	Clock Polarity = 0	-4	5	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	Clock Polarity = 1	-4	5	ns
10	$t_{d(ENL-CLKH/L)}$	Delay time, SPI_EN[1:0] (output) falling edge to first SPI_CLK (output) rising or falling edge		2P (1)	(1)	ns
11	$t_{d(CLKH/L-ENH)}$	Delay time, SPI_CLK (output) rising or falling edge to SPI_EN[1:0] (output) rising edge		P+.5C (2)	(2)	ns

(1) The delay time can be adjusted using the SPI module register C2TDELAY. See the *TMS320DM355 DMSoC Serial Peripheral Interface (SPI) User's Guide* (literature number SPRUED4).
(2) The delay time can be adjusted using the SPI module register T2CDELAY. See the *TMS320DM355 DMSoC Serial Peripheral Interface (SPI) User's Guide* (literature number SPRUED4).

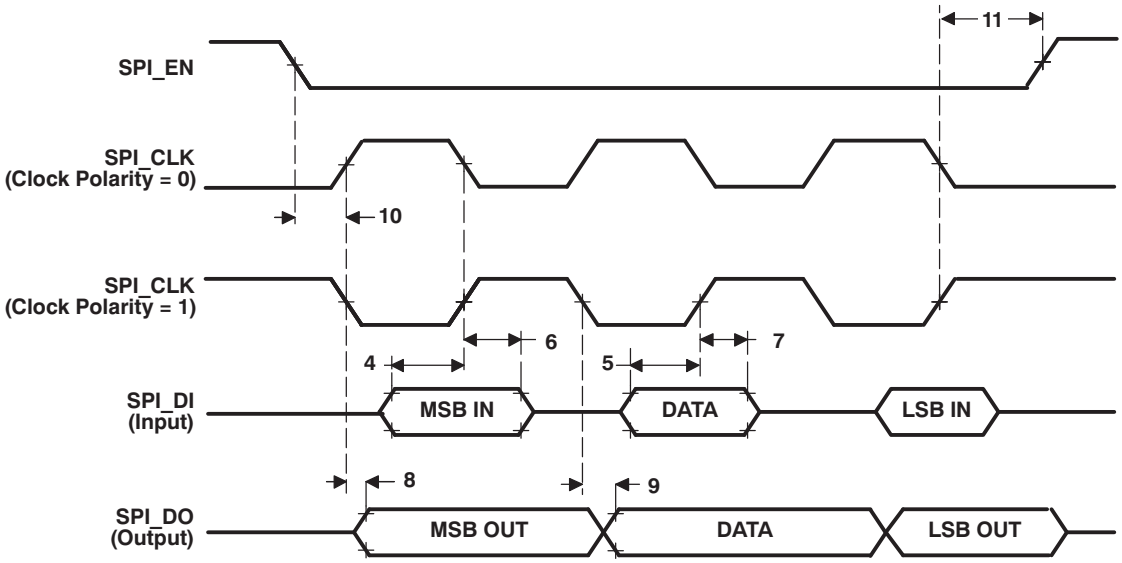

Figure 5-37. SPI Master Mode External Timing (Clock Phase = 0)

SPI Master Mode Timings (Clock Phase = 1)

Table 5-31. Timing Requirements for SPI Master Mode [Clock Phase = 1] (see Figure 5-38)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
13	$t_{su(DIV-CLKL)}$	Setup time, SPI_DI (input) valid before SPI_CLK (output) rising edge	Clock Polarity = 0	.5P + 3		ns
14	$t_{su(DIV-CLKH)}$	Setup time, SPI_DI (in put) valid before SPI_CLK (output) falling edge	Clock Polarity = 1	.5P + 3		ns
15	$t_{h(CLKL-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) rising edge	Clock Polarity = 0	.5P + 3		ns
16	$t_{h(CLKH-DIV)}$	Hold time, SPI_DI (input) valid after SPI_CLK (output) falling edge	Clock Polarity = 1	.5P + 3		ns

Table 5-32. Switching Characteristics Over Recommended Operating Conditions for SPI Master Mode [Clock Phase = 1] (see Figure 5-38)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
17	$t_{d(CLKL-DOV)}$	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	Clock Polarity = 0	-4	5	ns
18	$t_{d(CLKH-DOV)}$	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	Clock Polarity = 1	-4	5	ns
19	$t_{d(ENL-CLKH/L)}$	Delay time, SPI_EN[1:0] (output) falling edge to first SPI_CLK (output) rising or falling edge		2P+.5C (1)	(1)	ns
20	$t_{d(CLKL/H-DOHz)}$	Delay time, SPI_CLK (output) falling or rising edge to SPI_DO (output) high impedance		P (2)	(2)	ns

(1) The delay time can be adjusted using the SPI module register C2TDELAY. See the *TMS320DM355 DMSoC Serial Peripheral Interface (SPI) User's Guide* (literature number SPRUED4).
(2) The delay time can be adjusted using the SPI module register T2CDELAY. See the *TMS320DM355 DMSoC Serial Peripheral Interface (SPI) User's Guide* (literature number SPRUED4).

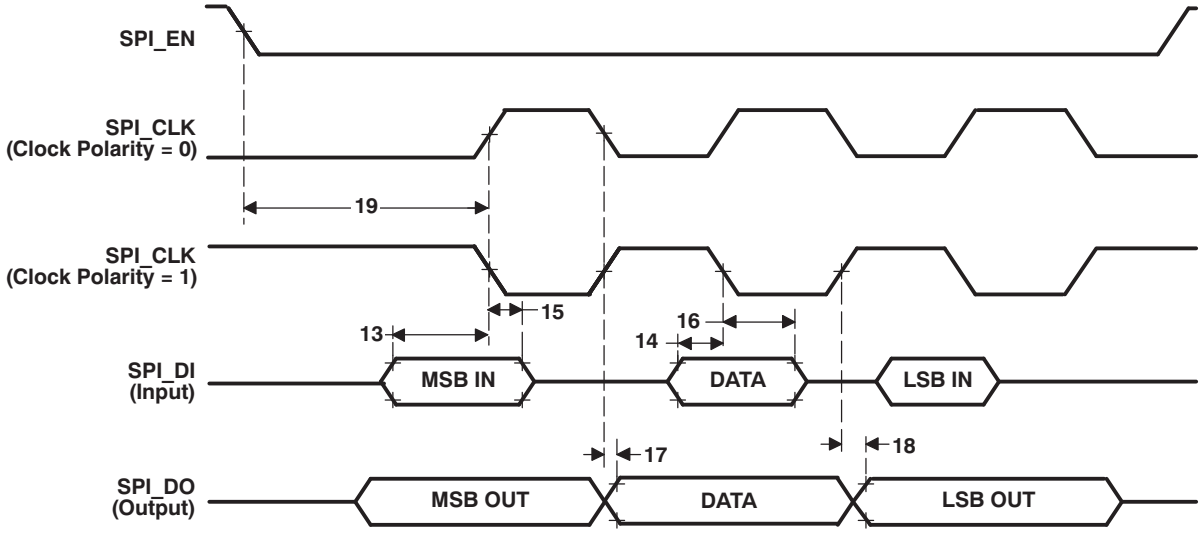

Figure 5-38. SPI Master Mode External Timing (Clock Phase = 1)

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5.13 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between DM355 and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DM355 through the I2C module.

The I2C port supports:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

For more detailed information on the I2C peripheral, see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide* (literature number SPRUEE0).

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5.13.1 I2C Electrical Data/Timing

5.13.1.1 Inter-Integrated Circuits (I2C) Timing

Table 5-33. Timing Requirements for I2C Timings(1) (see Figure 5-39)

NO.	PARAMETER		DM355				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low (For I^2C bus™ devices)	0(3)		0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (5)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (5)	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (5)	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (5)	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b (5)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode I^2C-bus™ device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$= 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

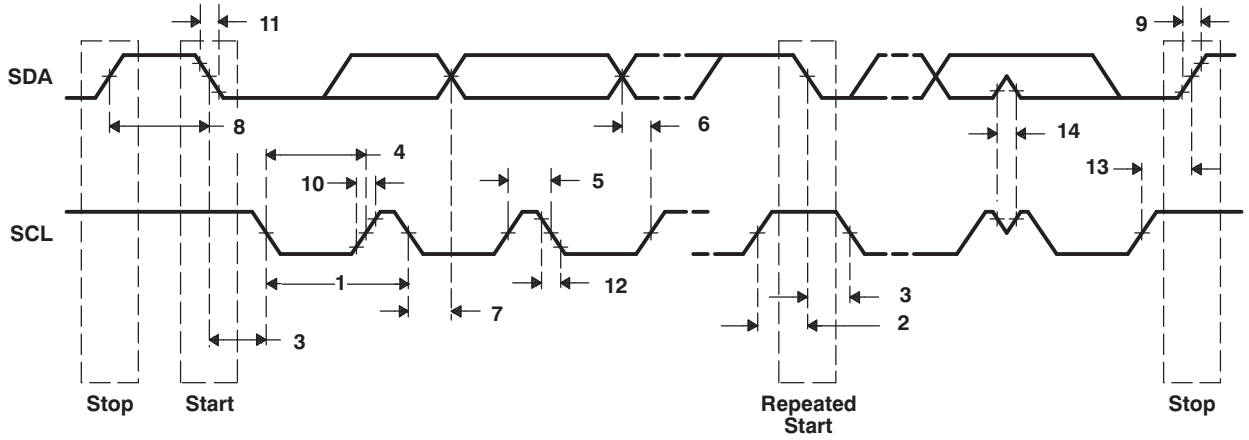

Figure 5-39. I2C Receive Timings

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Table 5-34. Switching Characteristics for I2C Timings[1] (see Figure 5-40)

NO.	PARAMETER		DM355				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low (For I2C devices)	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

CAUTION

The DM355 I^2C pins use a standard ±4-mA LVCMOS buffer, not the slow I/OP buffer defined in the I^2C specification. Series resistors may be necessary to reduce noise at the system level.

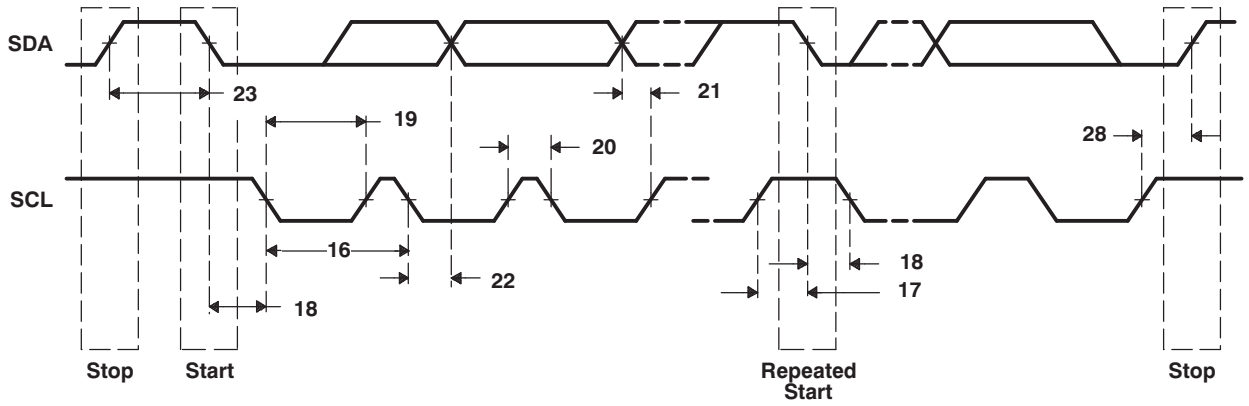

Figure 5-40. I2C Transmit Timings

5.14 Audio Serial Port (ASP)

DM355 includes two separate ASP controllers. The primary use for the audio serial port (ASP) is for audio interface purposes. The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface. The ASP is backward compatible with other TI ASPs. The ASP supports the following features:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- Direct interface to AC97 compliant devices (the necessary multiphase frame synchronization capability is provided)
- Direct interface to IIS compliant devices
- Direct interface to SPI protocol in master mode only
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- μ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation

For more detailed information on the ASP peripheral, see the *TMS320DM35x Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP) Reference Guide* (literature number SPRUED3).

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5.14.1 ASP Electrical Data/Timing

5.14.1.1 Audio Serial Port (ASP) Timing

Table 5-35. Timing Requirements for ASP(1) (see Figure 5-41)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
15	tc(CLK)	Cycle time, CLK	CLK ext	38.5 or 2P(2) (3)		ns
16	OTG(CLKS)	Pulse duration, CLKR/X high or CLKR/X low	CLKS ext	19.25 or P(2) (3) (4)		ns
5	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	21		ns
			CLKR ext	6		
6	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
7	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	21		ns
			CLKR ext	6		
8	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	6		
10	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	21		ns
			CLKX ext	6		
11	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	10		

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(3) Use which ever value is greater.
(4) The ASP does not have a duty cycle specification, just ensure that the minimum pulse duration specification is met.

Table 5-36. Switching Characteristics Over Recommended Operating Conditions for ASP(1) (2) (see Figure 5-41)

NO.	PARAMETER			DM355		UNIT
				MIN	MAX	
2	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X int	38.5 or 2P(3) (4) (5)		ns
17	td(CLKS-CLKRX)	Delay time, CLKS high to internal CLKR/X	CLKR/X int	1	24	
3	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X int	C - 1(6)	C + 1(6)	ns
4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid	CLKR int	3	25	ns
			CLKR ext	3	25	
9	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid	CLKX int	-4	8	ns
			CLKX ext	3	25	
12	tdis(CKXH-DXHZ)	Disable time, DX high impedance following last data bit from CLKX high	CLKX int		12	ns
			CLKX ext		12	ns
13	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	CLKX int	-5	12	ns
			CLKX ext	3	25	ns
14	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	FSX int		14	ns
			FSX ext		25	

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(5) Use which ever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = 1/SYSCLK2, where SYSCLK2 is an output of PLLC1 (see Section 3.5))
S = sample rate generator input clock = CLKS if CLKSM = 0
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the ASP bit rate *does not* exceed the maximum limit (see footnote (3) above).

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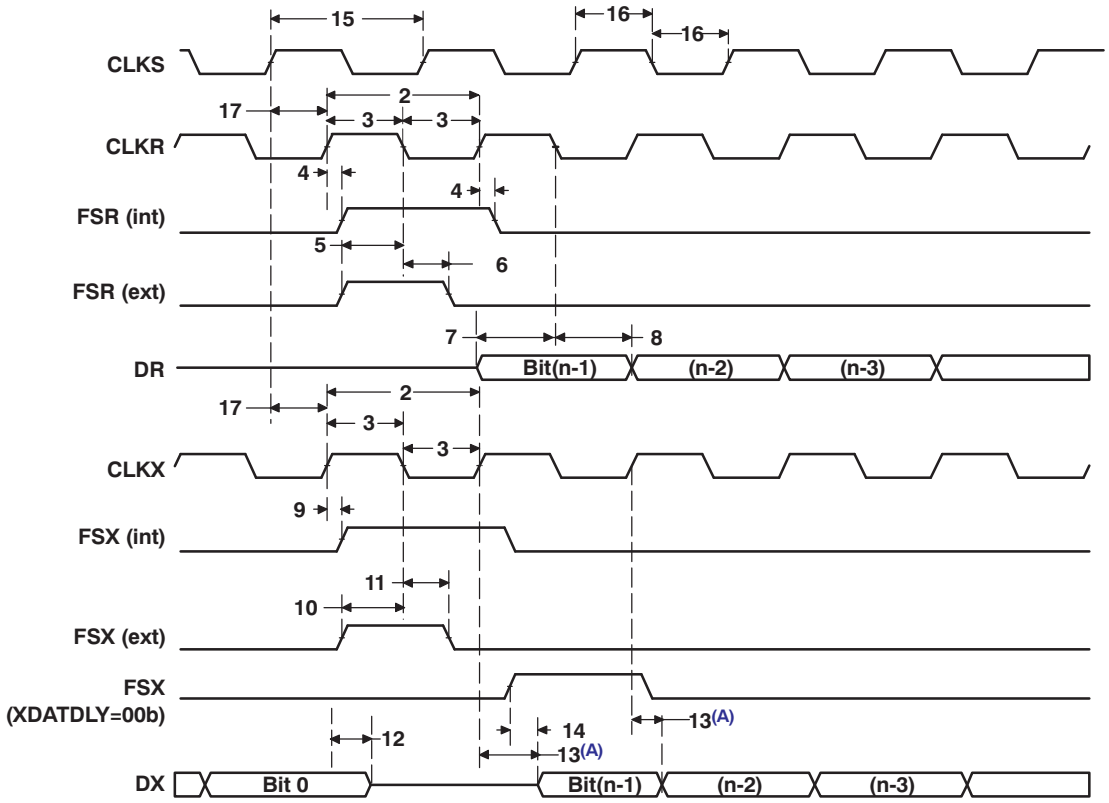

A. Parameter No. 13 applies to the first data bit only when XDATDLY ≠ 0.

Figure 5-41. ASP Timing

Table 5-37. ASP as SPI Timing Requirements

CLKSTP = 10b, CLKXP = 0 (see Figure 5-42)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	11		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	0		ns

Table 5-38. ASP as SPI Switching Characteristics(1) (2)

CLKSTP = 10b, CLKXP = 0 (see Figure 5-42)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M33	tc(CKX)	Cycle time, CLKX	38.5 or 2P(1) (3)		ns
M24	$t_{d(CKXL-FXH)}$	Delay time, CLKX low to FSX high(2)	T – 2	T + 3	ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high(4)	L_1 – 2	L_1 + 2	ns
M26	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	6	ns
M27	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	L_1 – 3	L_1 +3	ns

(1) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(2) T = CLKX period = (1 + CLKGDV) × 2P
L_1 = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) × 2P when CLKGDV is even
(3) Use which ever value is greater.
(4) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

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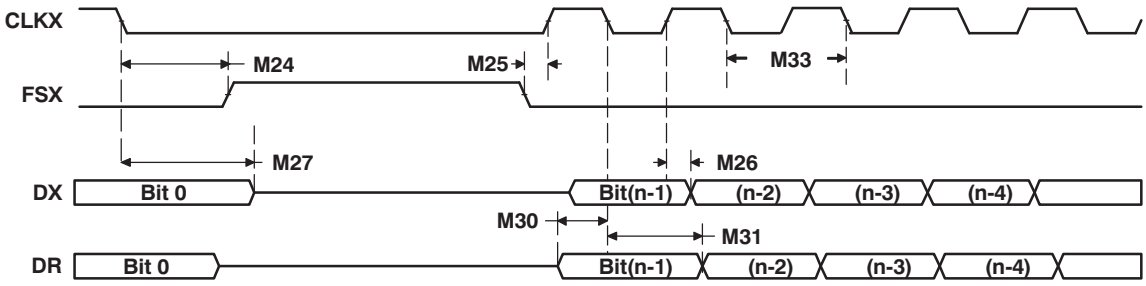

Figure 5-42. ASP as SPI: CLKSTP = 10b, CLKXP = 0

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Table 5-39. ASP as SPI Timing Requirements

CLKSTP = 11b, CLKXP = 0

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	11		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		ns

Table 5-40. ASP as SPI Switching Characteristics(1) (2)

CLKSTP = 11b, CLKXP = 0 (see Figure 5-43)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M42	tc(CKX)	Cycle time, CLKX	38.5 or 2P(1) (3)		ns
M34	$t_{d(CKXL-FXH)}$	Delay time, CLKX low to FSX high(4)	$L_1 - 2$	$L_1 + 3$	ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high(5)	T – 2	T + 2	ns
M36	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	6	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	–3	3	ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	$H_1 - 2$	$H_1 + 10$	ns

(1) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(2) T = CLKX period = (1 + CLKGDV) × 2P
L_1 = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) × 2P when CLKGDV is even
H_1 = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) × 2P when CLKGDV is even
(3) Use which ever value is greater.
(4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master ASP
(5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

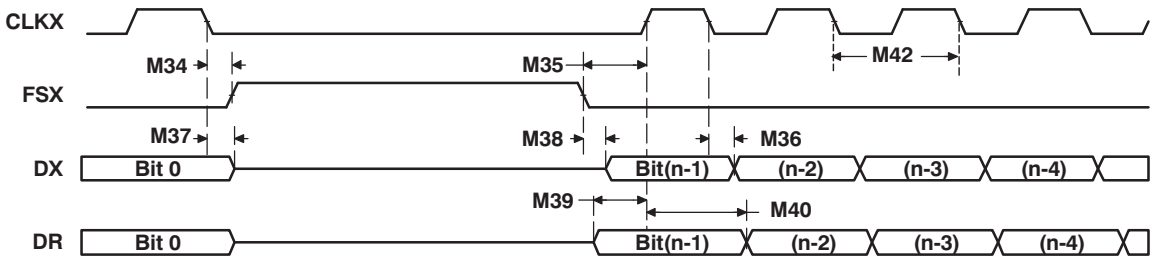

Figure 5-43. ASP as SPI: CLKSTP = 11b, CLKXP = 0

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Table 5-41. ASP as SPI Timing Requirements

CLKSTP = 10b, CLKXP = 1 (see Figure 5-44)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	11		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	0		ns

Table 5-42. ASP as SPI Switching Characteristics(1) (2)

CLKSTP = 10b, CLKXP = 1 (see Figure 5-44)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M52	tc(CKX)	Cycle time, CLKX	38.5 or 2P(1) (3)		ns
M43	$t_{d(CKXH-FXH)}$	Delay time, CLKX high to FSX high(4)	T – 1	T + 3	ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low(5)	H_1 – 2	H_1 + 2	ns
M45	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	6	ns
M46	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	H_1 – 3	H_1 + 3	ns

(1) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(2) T = CLKX period = (1 + CLKGDV) × 2P
H_1 = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) × 2P when CLKGDV is even
(3) Use which ever value is greater.
(4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master ASP
(5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

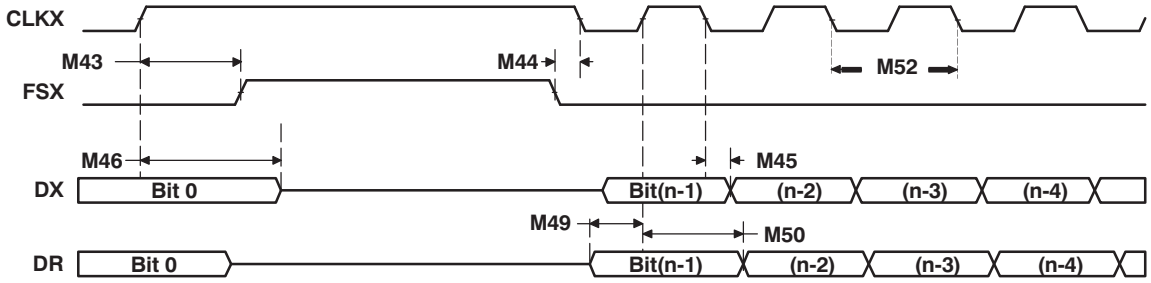

Figure 5-44. ASP as SPI: CLKSTP = 10b, CLKXP = 1

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Table 5-43. ASP as SPI Timing Requirements

CLKSTP = 11b, CLKXP = 1 (see Figure 5-45)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	11		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	0		ns

Table 5-44. ASP as SPI Switching Characteristics(1) (2)

CLKSTP = 11b, CLKXP = 1 (see Figure 5-45)

NO.	PARAMETER		MASTER		UNIT
			MIN	MAX	
M62	tc(CKX)	Cycle time, CLKX	38.5 or 2P(3) (3)		ns
M53	$t_{d(CKXH-FXH)}$	Delay time, CLKX high to FSX high(4)	$H_1 - 1$	$H_1 + 3$	ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low(5)	T – 2	T + 2	ns
M55	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	6	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	– 3	+ 3	ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	$L_1 - 1$	$L_1 + 10$	ns

(1) P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1 (see Section 3.5) .
(2) T = CLKX period = (1 + CLKGDV) × 2P
L_1 = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) × 2P when CLKGDV is even
H_1 = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) × 2P when CLKGDV is even
(3) Use which ever value is greater.
(4) FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master ASP
(5) FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

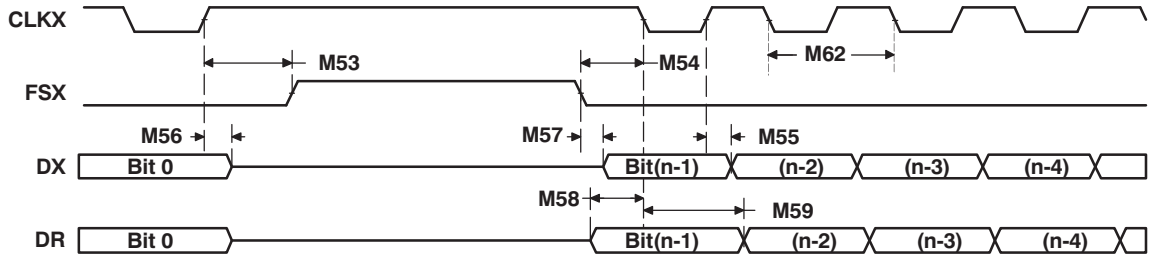

Figure 5-45. ASP as SPI: CLKSTP = 11b, CLKXP = 1

5.15 Timer

The DM355 contains four software-programmable timers. Timer 0, Timer 1, and Timer 3 (general-purpose timers) can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode. Timer 3 supports additional features over the other timers: external clock/event input, period reload, output event tied to Real Time Out (RTO) module, external event capture, and timer counter register read reset. Timer 2 is used only as a watchdog timer. Timer 2 is tied to device reset.

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode (Timer 0, 1, 3)
  - Dual 32-bit general-purpose timer mode (Timer 0, 1, 3)
  - Watchdog timer mode (Timer 2)
- Two possible clock sources:
  - Internal clock
  - External clock/event input via timer input pins (Timer 3)
- Three possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
  - Continuous operation with period reload (Timer 3)
- Generates interrupts to the ARM CPU
- Generates sync event to EDMA
- Generates output event to device reset (Timer 2)
- Generates output event to Real Timer Out (RTO) module (Timer 3)
- External event capture via timer input pins (Timer 3)

For more detailed information, see the *TMS320DM355 DMSoC 64-bit Timer User's Guide* for more information (literature number SPRUEE5).

5.15.1 Timer Electrical Data/Timing

Table 5-45. Timing Requirements for Timer Input(1) (2) (3) (see Figure 5-46)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{c(TIN)}$	Cycle time, TIM_IN	4P		ns
2	$t_{w(TINPH)}$	Pulse duration, TIM_IN high	0.45C	0.55C	ns
3	$t_{w(TINPL)}$	Pulse duration, TIM_IN low	0.45C	0.55C	ns
4	$t_{t(TIN)}$	Transition time, TIM_IN		0.25C or 10(4)	ns

(1) GPIO000, GPIO001, GPIO002, and GPIO003 can be used as external clock inputs for Timer 3. See the *TMS320DM355 DMSoC 64-bit Timer User's Guide* for more information (literature number SPRUEE5).
(2) P = MXI1/CLKIN cycle time in ns. For example, when MXI1/CLKIN frequency is 24 MHz use P = 41.$\overline{6}$ ns.
(3) C = TIM_IN cycle time in ns. For example, when TIM_IN frequency is 24 MHz use C = 41.$\overline{6}$ ns
(4) Whichever is smaller. C = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

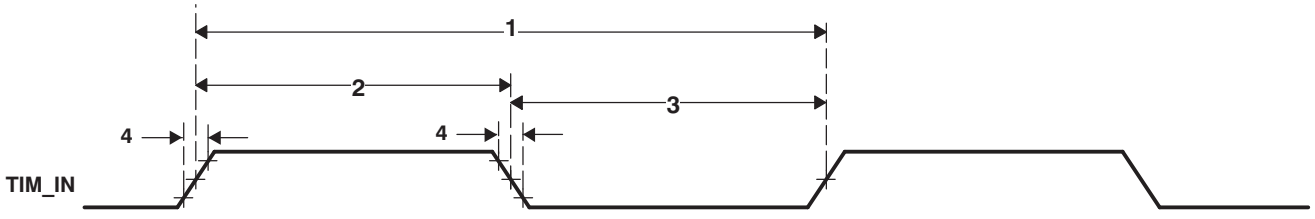

Figure 5-46. Timer Input Timing

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5.16 Pulse Width Modulator (PWM)

The DM355 contains 4 separate Pulse Width Modulator (PWM) modules. The pulse width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable. The Pulse Width Modulator (PWM) modules support the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- 8-bit repeat count for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value.
- Configurable to operate in either one-shot or continuous mode
- Buffered period and first-phase duration registers
- One-shot operation triggerable by hardware events with programmable edge transitions. (low-to-high or high-to-low).
- One-shot operation triggerable by the CCD VSYNC output of the video processing subsystem (VPSS), which allows any of the PWM instantiations to be used as a CCD timer. This allows the DM355 module to support the functions provided by the CCD timer feature (generating strobe and shutter signals).
- One-shot operation generates N+1 periods of waveform, N being the repeat count register value
- Configurable PWM output pin inactive state
- Interrupt and EDMA synchronization events

5.16.1 PWM0/1/2/3 Electrical/Timing Data

Table 5-46. Switching Characteristics Over Recommended Operating Conditions for PWM0/1/2/3 Outputs(1) (see Figure 5-47 and Figure 5-48)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{w(PWMH)}$	Pulse duration, PWMx high	P		ns
2	$t_{w(PWML)}$	Pulse duration, PWMx low	P		ns
3	$t_{t(PWM)}$	Transition time, PWMx		.05P	ns
4	$t_{d(CCDC-PWMV)}$	Delay time, CCDC(VD) trigger event to PWMx valid		10	ns

(1) P = MXI1/CLKIN cycle time in ns. For example, when MXI1/CLKIN frequency is 24 MHz use P = 41.$\overline{6}$ ns.

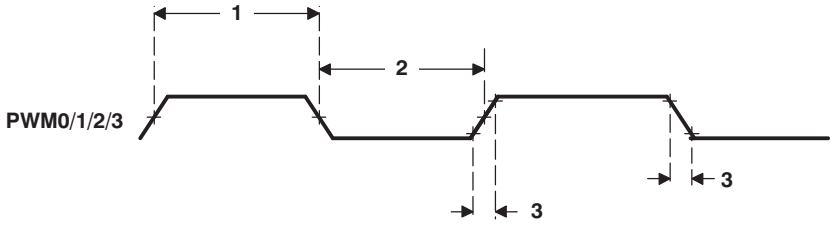

Figure 5-47. PWM Output Timing

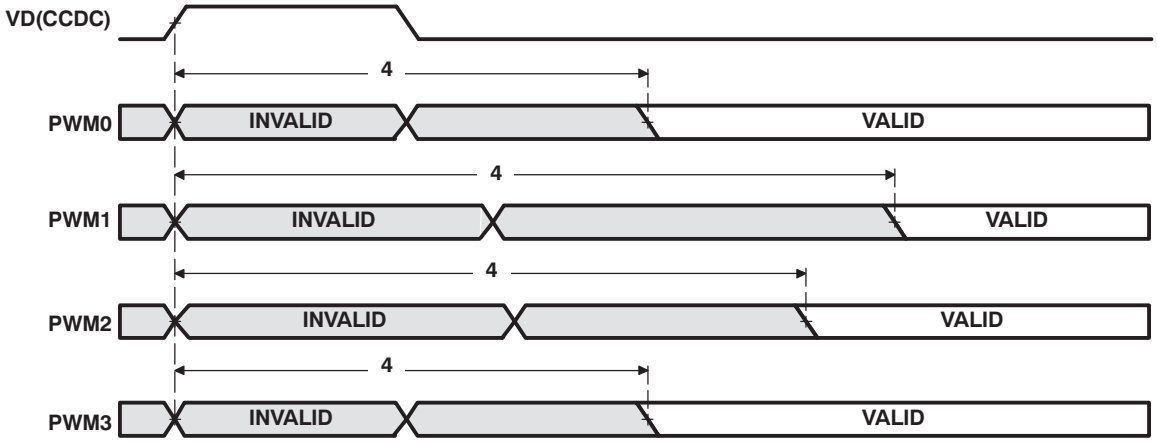

Figure 5-48. PWM Output Delay Timing

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5.17 Real Time Out (RTO)

The DM355 Real Time Out (RTO) peripheral supports the following features:

- Four separate outputs
- Trigger on Timer3 event

5.17.1 RTO Electrical/Timing Data

Table 5-47. Switching Characteristics Over Recommended Operating Conditions for RTO Outputs (see Figure 5-49 and Figure 5-50)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{w(RTOH)}$	Pulse duration, RTOx high	P		ns
2	$t_{w(RTOL)}$	Pulse duration, RTOx low	P		ns
3	$t_{t(RTO)}$	Transition time, RTOx		.1P	ns
4	$t_{d(TIMER3-RTOV)}$	Delay time, Timer 3 (TINT12 or TINT34) trigger event to RTOx valid		10	ns

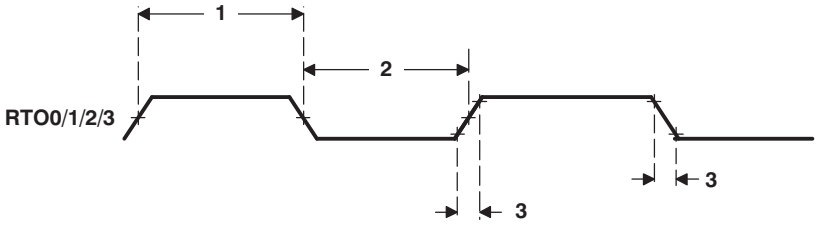

Figure 5-49. RTO Output Timing

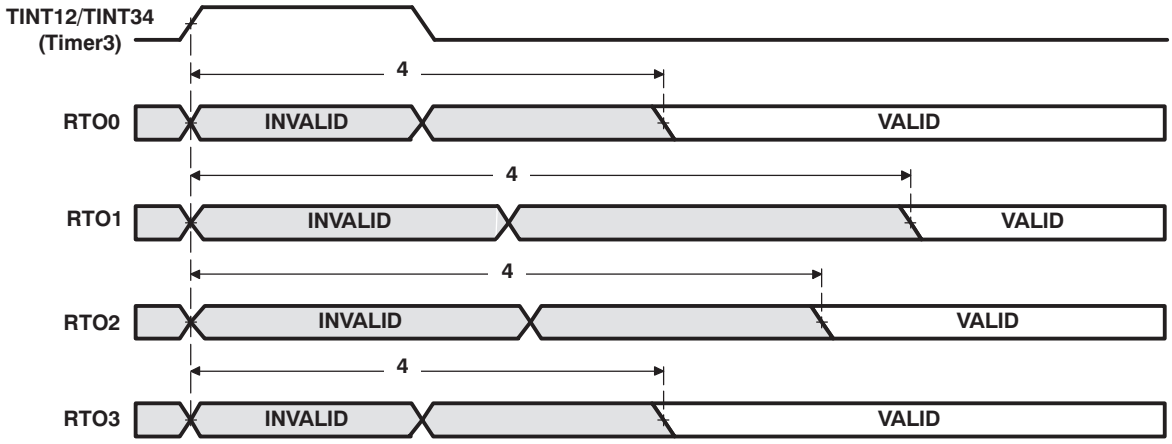

Figure 5-50. RTO Output Delay Timing

5.18 IEEE 1149.1 JTAG

The JTAG(1) interface is used for BSDL testing and emulation of the DM355 device.

The DM355 device requires that both TRST and RESET be asserted upon power up to be properly initialized. While RESET initializes the device, TRST initializes the device's emulation logic. Both resets are required for proper operation.

While both TRST and RESET need to be asserted upon power up, only RESET needs to be released for the device to boot properly. TRST may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state.

TRST only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. Note: TRST is synchronous and ***must*** be clocked by TCK; otherwise, the boundary scan logic may not respond as expected after TRST is asserted.

RESET must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of RESET.

For maximum reliability, DM355 includes an internal pulldown (PD) on the TRST pin to ensure that TRST will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST.

When using this type of JTAG controller, assert TRST to initialize the device after powerup and externally drive TRST high before attempting any emulation or boundary scan operations. Following the release of RESET, the low-to-high transition of TRST must be "seen" to latch the state of EMU1 and EMU0. The EMU[1:0] pins configure the device for either Boundary Scan mode or Emulation mode. For more detailed information, see the terminal functions section of this data sheet.

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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5.18.1 JTAG Test-Port Electrical Data/Timing

Table 5-48. Timing Requirements for JTAG Test Port (see Figure 5-51)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	20		ns
2	tw(TCKH)	Pulse duration, TCK high	8		ns
3	tw(TCKL)	Pulse duration, TCK low	8		ns
4	$t_{su(TDIV-RTCKH)}$	Setup time, TDI valid before RTCK high	10		ns
5	$t_{h(RTCKH-TDIIV)}$	Hold time, TDI valid after RTCK high	9		ns
6	$t_{su(TMSV-RTCKH)}$	Setup time, TMS valid before RTCK high	2		ns
7	$t_{h(RTCKH-TMSIV)}$	Hold time, TMS valid after RTCK high	5		ns

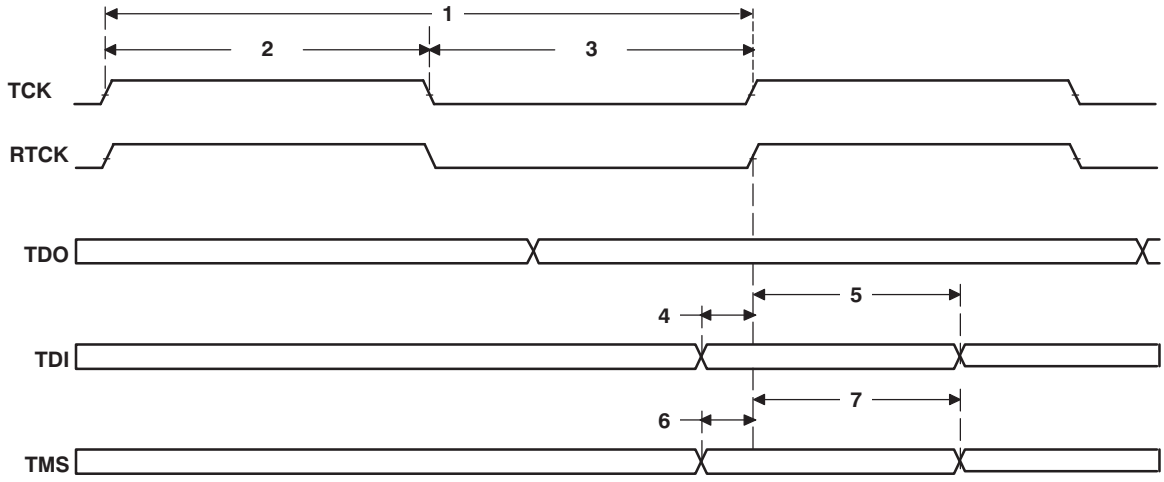

Figure 5-51. JTAG Input Timing

Table 5-49. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-51)

NO.	PARAMETER		DM355		UNIT
			MIN	MAX	
8	$t_{c(RTCK)}$	Cycle time, RTCK	20		ns
9	tw(RTCKH)	Pulse duration, RTCK high	10		
10	tw(RTCKL)	Pulse duration, RTCK low	10		
11	$t_{r(all\ JTAG\ outputs)}$	Rise time, all JTAG outputs		1.3	ns
12	$t_{f(all\ JTAG\ outputs)}$	Fall time, all JTAG outputs		1.3	ns
13	$t_{d(RTCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	0.25*tc(RTCK)	ns

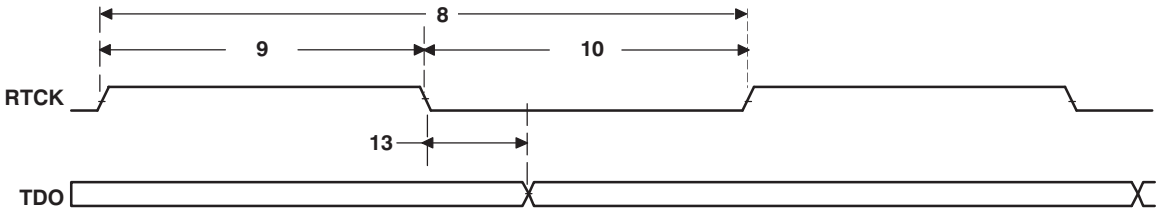

Figure 5-52. JTAG Output Timing

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6 Mechanical Data

The following table(s) show the thermal resistance characteristics for the PBGA − ZCE mechanical package. Note that micro-vias are not required. Contact your TI representative for routing recommendations.

6.1 Thermal Data for ZCE

The following table shows the thermal resistance characteristics for the PBGA − ZCE mechanical package.

Table 6-1. Thermal Resistance Characteristics (PBGA Package) [ZCE]

NO.			°C/W(1)
1	$R\Theta_{JC}$	Junction-to-case	7.2
2	$R\Theta_{JB}$	Junction-to-board	11.4
3	$R\Theta_{JA}$	Junction-to-free air	27.0
4	Psi_{JT}	Junction-to-package top	0.1
5	Psi_{JB}	Junction-to-board	11.3

(1) The junction-to-case measurement was conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these three EIA/JEDEC standards:
- EIA/JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- EIA/JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

6.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document. Note that micro-vias are not required for this package.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DM355SDZCEA216	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 100	TMS320 DM355DZCE A216	
TMS320DM355CZCE216	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR		DM355CZCE 216 TMS320	
TMS320DM355CZCEA21	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 100	DM355ZCE A216 TMS320 DM355CZCE A216	
TMS320DM355DZCE135	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	0 to 85	DM355DZCE 135 TMS320 DM355DZCE 135	
TMS320DM355DZCE216	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	0 to 85	DM355DZCE 216 TMS320 DM355DZCE 216	
TMS320DM355DZCE270	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	0 to 85	DM355DZCE 270 TMS320 DM355DZCE 270	
TMS320DM355DZCEA21	NRND	NFBGA	ZCE	337	160	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 100	TMS320 DM355DZCE A216	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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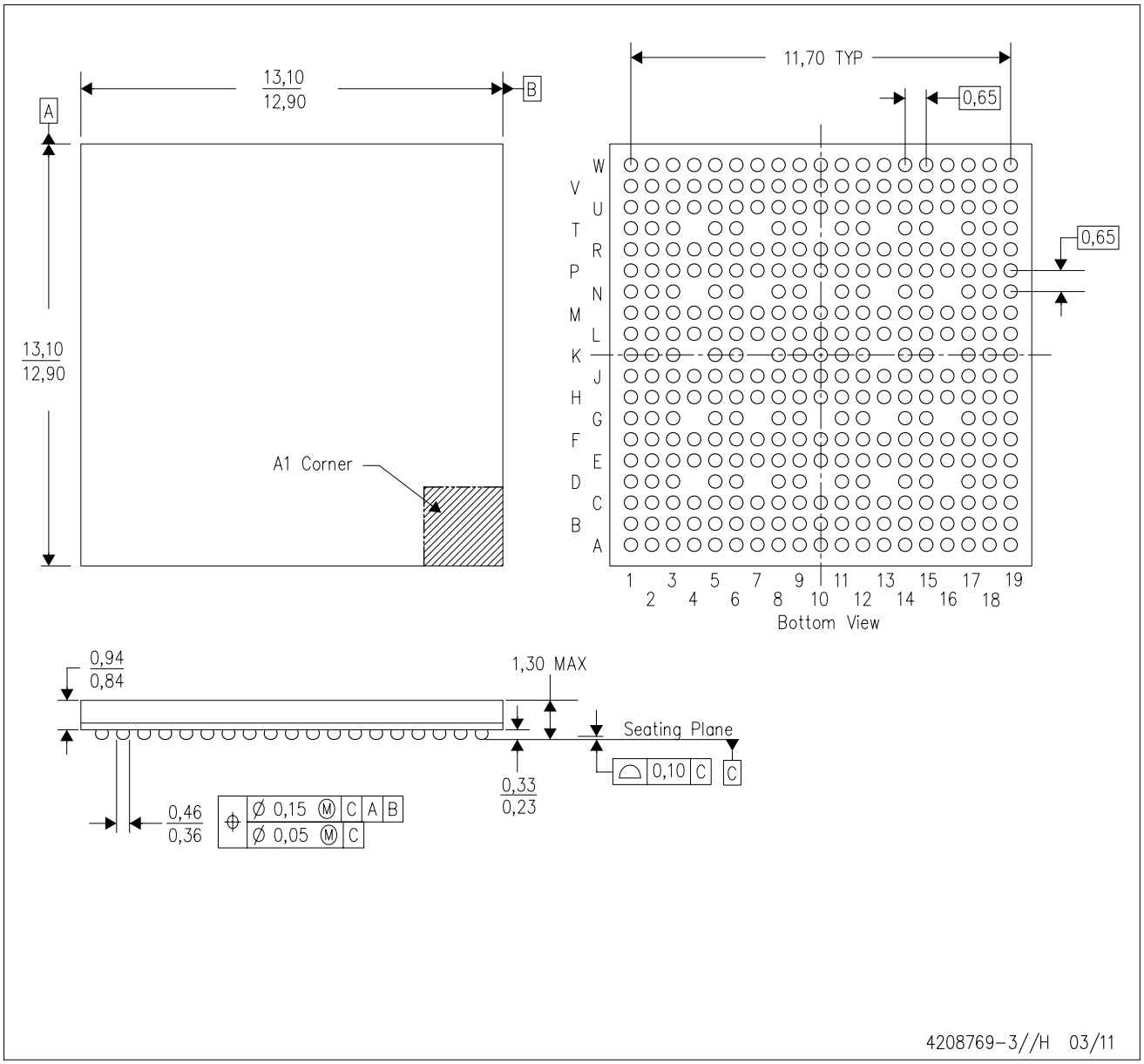
ZCE (S–PBGA–N337) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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