TMS320C6472 Fixed-Point Digital Signal Processor

1 Features

- Six On-Chip TMS320C64x+ Megamodules
- Endianess: Little Endian, Big Endian
- C64x+ Megamodule Main Features:
  - High-Performance, Fixed-Point TMS320C64x+ DSP
  - 500/625/700 MHz
  - Eight 32-Bit Instructions/Cycle
  - 4000 MIPS/MMACS (16-Bits) at 500 MHz
  - Dedicated SPLOOP Instruction
  - Compact Instructions (16-Bit)
  - Instruction Set Enhancements
  - Exception Handling
  - L1/L2 Memory Architecture:
    - 256K-Bit (32K-Byte) L1P Program RAM/Cache [Direct Mapped, Flexible Allocation]
    - 256K-Bit (32K-Byte) L1D RAM/Cache [2-Way Set-Associative, Flexible Allocation]
    - 4.75M-Bit (608K-Byte) L2 Unified Mapped RAM/Cache [4-Way Set-Associative, Flexible Allocation]
    - L1P Memory Controller
    - L1D Memory Controller
    - L2 Memory Controller
  - Time Stamp Counter
  - One 64-Bit General-Purpose/Watchdog Timer
- Shared Peripherals and Interfaces
  - EDMA Controller (64 Independent Channels)
  - Shared Memory Architecture
    - Shared L2 Memory Controller
    - 768K-Byte of RAM
    - Boot ROM
  - Three Telecom Serial Interface Ports (TSIPs)
    - Each TSIP is 8 Links of 8 Mbps per Direction
  - 32-Bit DDR2 Memory Controller (DDR2-533 SDRAM)
    - 256 M-Byte x 2 Addressable Memory Space
  - Two 1x Serial RapidIO® Links, v1.2 Compliant
    - 1.25-, 2.5-, 3.125-Gbps Link Rates
    - Message Passing, DirectIO Support, Error Management Extensions, and Congestion Control
    - IEEE 1149.6 Compliant I/Os
  - UTOPIA
    - UTOPIA Level 2 Slave ATM Controller
    - 8/16-Bit Transmit and Receive Operations up to 50 MHz per Direction
    - User-Defined Cell Format up to 64 Bytes
  - Two 10/100/1000 Mb/s Ethernet MACs (EMACs)
    - Both EMACs are IEEE 802.3 Compliant
    - EMAC0 Supports:
      - MII, RMII, SS-SMII, GMII, and RGMII
      - 8 Independent Transmit (TX) Channels
      - 8 Independent Receive (RX) Channels
    - EMAC1 Supports:
      - RMII, SS-SMII and RGMII
      - 8 Independent Transmit (TX) Channels
      - 8 Independent Receive (RX) Channels
    - Both EMACs (EMAC0 and EMAC1) Share MDIO Interface
  - 16-Bit Host-Port Interface (HPI)
  - One Inter-Integrated Circuit (I^2C) Bus
  - Six Shared 64-Bit General-Purpose Timers
- System PLL and PLL Controller
- Secondary PLL and PLL Controller, Dedicated to EMAC
- Third PLL and PLL Controller Dedicated to DDR2 Memory Controller
- 16 General-Purpose I/O (GPIO) Pins
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- 737-Pin Ball Grid Array (BGA) Package (CTZ or ZTZ Suffix), 0.8-mm Ball Pitch
- 0.09-µm/7-Level Cu Metal Process (CMOS)
- 3.3-, 1.8-, 1.5-, 1.2-V I/O Supplies
- 1.0-/1.1-, 1.2-V Core Supplies
- Commercial Temperature [0°C to 85°C]
- Extended Temperature [-40°C to 100°C]

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1.1 CTZ/ZTZ BGA Package (Bottom View)

The TMS320C6472 devices are designed for a package temperature range of 0°C to 85°C (commercial temperature range) or -40°C to 100°C (extended temperature range).

NOTE

Extended temperature (A) range is available only on 500-MHz and 625-MHz devices.

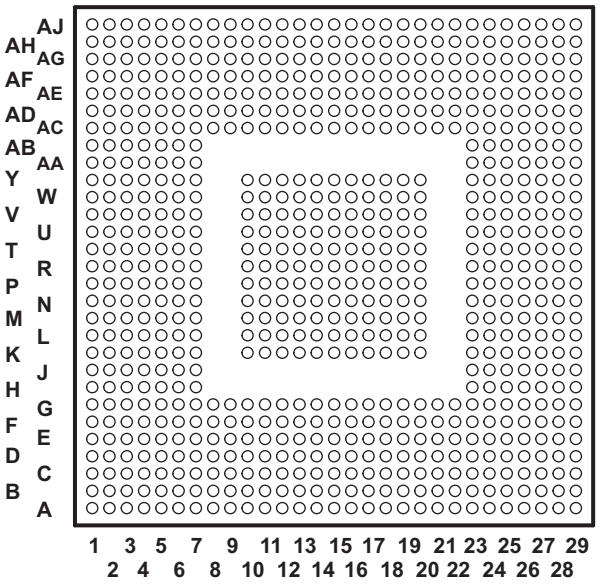

Figure 1-1. CTZ/ZTZ 737-Pin Ball Grid Array (BGA) Package (Bottom View)

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1.2 Description

The TMS320C6472 device is a Texas Instruments next-generation fixed-point digital signal processor (DSP) targeting high-performance computing applications, including high-end industrial, mission-critical, high-end image and video, communication, media gateways, and remote access servers. This device was designed with these applications in mind. A common key requirement of these applications is the availability of large on-chip memories to handle vast amounts of data during processing. With 768K-Byte of shared RAM and 608K-Byte local L2 RAM per C64x+ Megamodule, the TMS320C6472 device can eliminate the need for external memory, thereby reducing system power dissipation and system cost and optimizing board density.

The TMS320C6472 device has six optimized TMS320C64x+™ megamodules, which combine high performance with the lowest power dissipation per port. The TMS320C6472 device includes three different speeds: 500 MHz, 625 MHz, and 700 MHz. The C64x+ megamodules are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C64x+ megamodule is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making devices like TMS320C6472 an excellent choice for applications including video and telecom infrastructure, imaging/medical, and wireless infrastructure (WI). The C64x+™ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

The C64x+ megamodule core employs eight functional units, two register files, and two data paths. Like the earlier C6000 devices, two of these eight functional units are multipliers or .M units. Each C64x+ megamodule core .M unit doubles the multiply throughput versus the C64x core by performing four 16-bit x 16-bit multiply-accumulates (MACs) every clock cycle. Thus, eight 16-bit x 16-bit MACs can be executed every cycle on the C64x+ core. At a 500-MHz clock rate, this means 4000 16-bit MMACs can occur every second. Moreover, each multiplier on the C64x+ megamodule core can compute one 32-bit x 32-bit MAC or four 8-bit x 8-bit MACs every clock cycle.

The C64x+ megamodule integrates a large amount of on-chip memory organized as a two-level memory system. The level-1 (L1) program and data memories on this C64x+ megamodule are 32KB each. This memory can be configured as mapped RAM, cache, or some combination of the two. When configured as cache, L1 program (L1P) is a direct mapped cache where as L1 data (L1D) is a two-way set associative cache. The level 2 (L2) memory is shared between program and data space and is 608K-Byte in size. L2 memory can also be configured as mapped RAM, cache, or some combination of the two. The C64x+ megamodule also has a 32-bit peripheral configuration (CFG) port, an internal DMA (IDMA) controller, a system component with reset/boot control, interrupt/exception control, a power-down control, and a free-running 32-bit timer for time stamp.

The peripheral set includes: three Telecom Serial Interface Port (TSIPs); an 16/8 bit Universal Test and Operations PHY Interface for Asynchronous Transfer Mode (ATM) Slave [UTOPIA Slave] port; two 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the C6472 DSP core processor and the network; a management data input/output (MDIO) module (shared by both EMACs) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system; a Serial RapidIO® with two 1x lanes and support for packet forwarding; a 32-bit DDR2 SDRAM interface; 12 64-bit general-purpose timers; an inter-integrated circuit bus module (I2C); 16 general-purpose input/output ports (GPIO) with programmable interrupt/event generation modes; and a 16-bit multiplexed host-port interface (HPI16).

The C6472 device has a complete set of development tools which includes: a C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows® debugger interface for visibility into source code execution.

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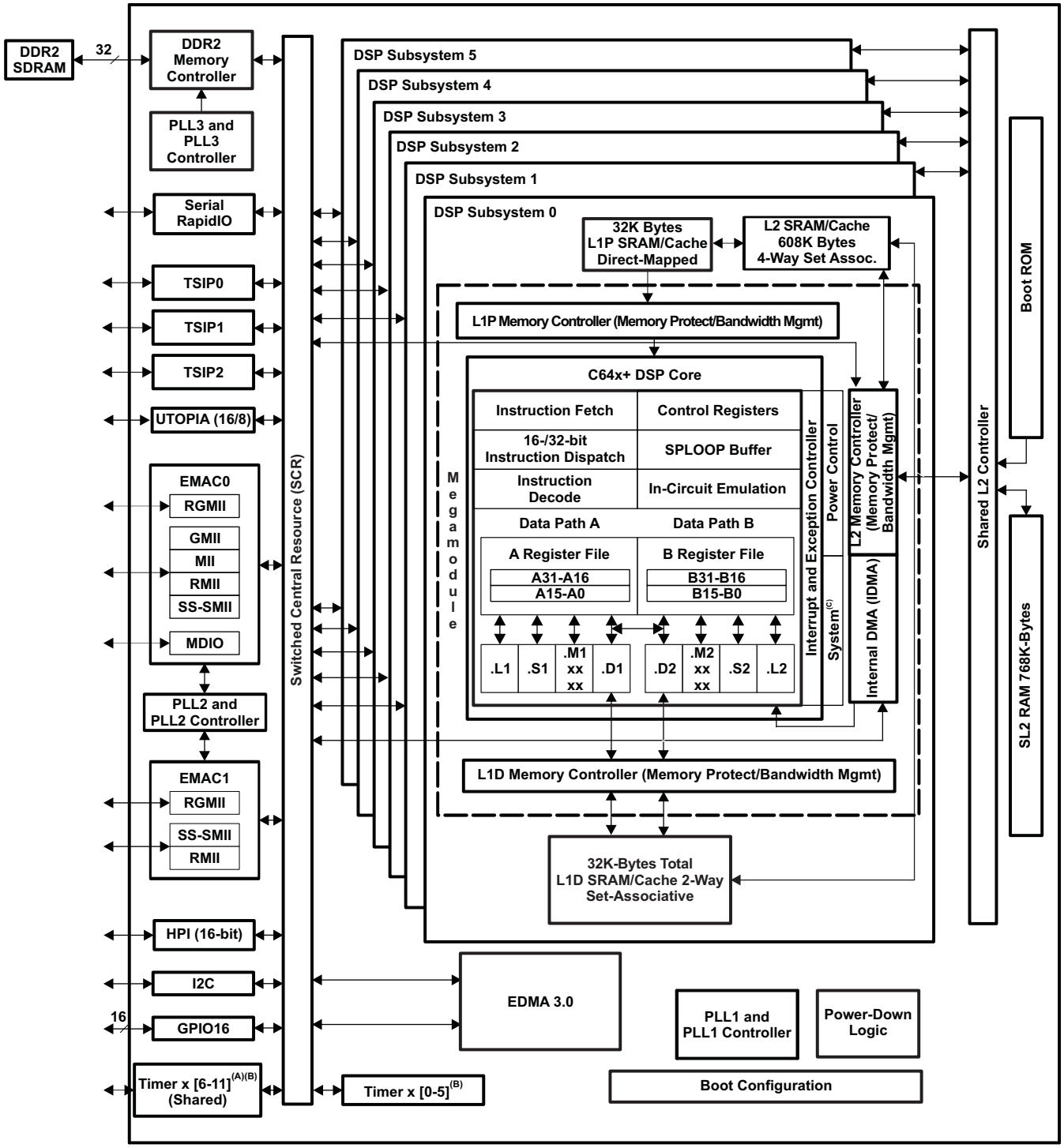
1.3 Functional Block Diagram

Figure 1-2 shows the functional block diagram of the C6472 device.



A. Timers 6-11 are shared.
B. Each of the Timer peripherals are configurable as either one 64-bit general-purpose timer *or* two 32-bit general-purpose timers *or* a watchdog timer.
C. System consists of Test, Emulation, Power Down, and Interrupt Controller.

Figure 1-2. C6472 Functional Block Diagram

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This revision history highlights the technical changes made to the document in this revision.

C6472 Revisions

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Section 1	Features:
	Added CTZ package to Features list item
Section 1.1	Changed section title to: CTZ/ZTZ BGA Package (Bottom View)
	Changed Figure 1-1 caption to: CTZ/ZTZ 737-Pin Ball Grid Array (BGA) Package (Bottom View)
Section 2.1	Device Characteristics:
	Modified Description for BGA Package in Table 2-1, Characteristics of the C6472 Processor
Section 2.8.2.1	Device and Development-Support Tool Nomenclature:
	Modified Figure 2-13, TMS320C64x+™ DSP Device Nomenclature (including the TMS320C6472 DSP)
Section 7.5.2	EDMA3 Peripheral Register Descriptions:
	Added DMAQNUM4-7 to Table 7-5, EDMA3 Registers
Section 8.1	Thermal Data:
	Changed Table 8-1 title to: Thermal Resistance Characteristics (S-PBGA Package) [CTZ/ZTZ]
Section 8.2	Packaging Information:
	Added CTZ mechanical package drawing

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2 Device Overview

NOTE

Unless otherwise noted, all address locations in this document are stated in hexidecimal numbers.

2.1 Device Characteristics

Table 2-1, provides an overview of the C6472 DSP. The table shows significant features of the C6472 device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count.

Table 2-1. Characteristics of the C6472 Processor

HARDWARE FEATURES		C6472
Peripherals Not all peripheral pins are available at the same time (for more detail, see Section 3).	DDR2 Memory Controller (32-bit bus width) [1.8 V I/O] (clock source = CLKIN3)	1
	EDMA (64 independent channels)	1
	High-speed Serial RapidIO Port	2
	I2C	1
	HPI (16 bit)	1
	Telecom Serial Interface Port (TSIP)	3
	UTOPIA (16/8-bit mode, 50-MHz, slave-only)	1
	10/100/1000 Mb/s Ethernet MAC (EMAC)	2
	Management Data Input/Output (MDIO)	1
	64-bit Timers (Configurable)	12 (6 dedicated [0-5], 1 per core; 6 shared [6-11]) 1 64-bit ***or*** 2 32-bit ***or*** WD each
	General-Purpose Input/Output Port (GPIO)	16
On-Chip Memory	Organization per C64x+ Megamodule	32K-Byte L1 Program Memory [SRAM/Cache] 32K-Byte L1 Data Memory [SRAM/Cache] 608K-Byte L2 Unified Memory [SRAM/Cache]
	Shared by all 6 C64x+ Megamodules	768K-byte SL2 Unified SRAM 768K-byte SL2 ROM
CPU MegaModule Revision ID	Revision ID Register (MM_REVID.[15:0]) Address 0181 2000	0003h
JTAG ID	JTAG ID register Address 02A8 0008	0009 102Fh
Frequency	MHz	500/625/700 MHz
Cycle Time	ns	2 ns/1.6 ns
Voltage	Core (V)	1.2 V (DDR2 EMIF) 1.0 V (500 MHz) / 1.1 V (625 MHz) / 1.2 V (700 MHz)
	I/O (V)	1.2 V [RapidIO], 1.5 V/1.8 V [EMAC RGMII], 1.8 V [DDR2 EMIF I/O], and 1.8 V and 3.3 V [I/O Supply Voltage]
PLL1 and PLL1 Controller Options	CLKIN frequency multiplier	Bypass (x1), x10-x32
PLL2 and PLL2 Controller Options	CLKIN frequency multiplier [EMAC support]	x20
PLL3 and PLL3 Controller Options	CLKIN frequency multiplier [DDR2 Memory Controller support only]	x20
BGA Package	24 x 24 mm	737-Pin Flip-Chip Plastic BGA (CTZ/ZTZ)
Process Technology	µm	0.09 µm

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Table 2-1. Characteristics of the C6472 Processor (continued)

HARDWARE FEATURES		C6472
Product Status(1)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PP
Device Part Numbers	(For more details on the C64x+™ DSP part numbering, see Figure 2-13)	TMX320C6472

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2.2 CPU (DSP Core) Description

The C64x+ Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 2-1. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C64x+ CPU extends the performance of the C64x core through enhancements and new features.

Each C64x+ .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes four 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produce one 32-bit packed output that contains 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or Arithmetic Logic Unit now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C64x+ core enhances the .S unit in several ways. In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C64x+ compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.

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- **Instruction Set Enhancements** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exception Handling** - Intended to aid the programmer in isolating bugs. The C64x+ CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.
- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C64x+ CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732)
- *TMS320C64x+ DSP Cache User's Guide* (literature number SPRU862)
- *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871)
- *TMS320C64x Technical Overview* (literature number SPRU395)
- *TMS320C64x to TMS320C64x+ CPU Migration Guide* (literature number SPRAA84)

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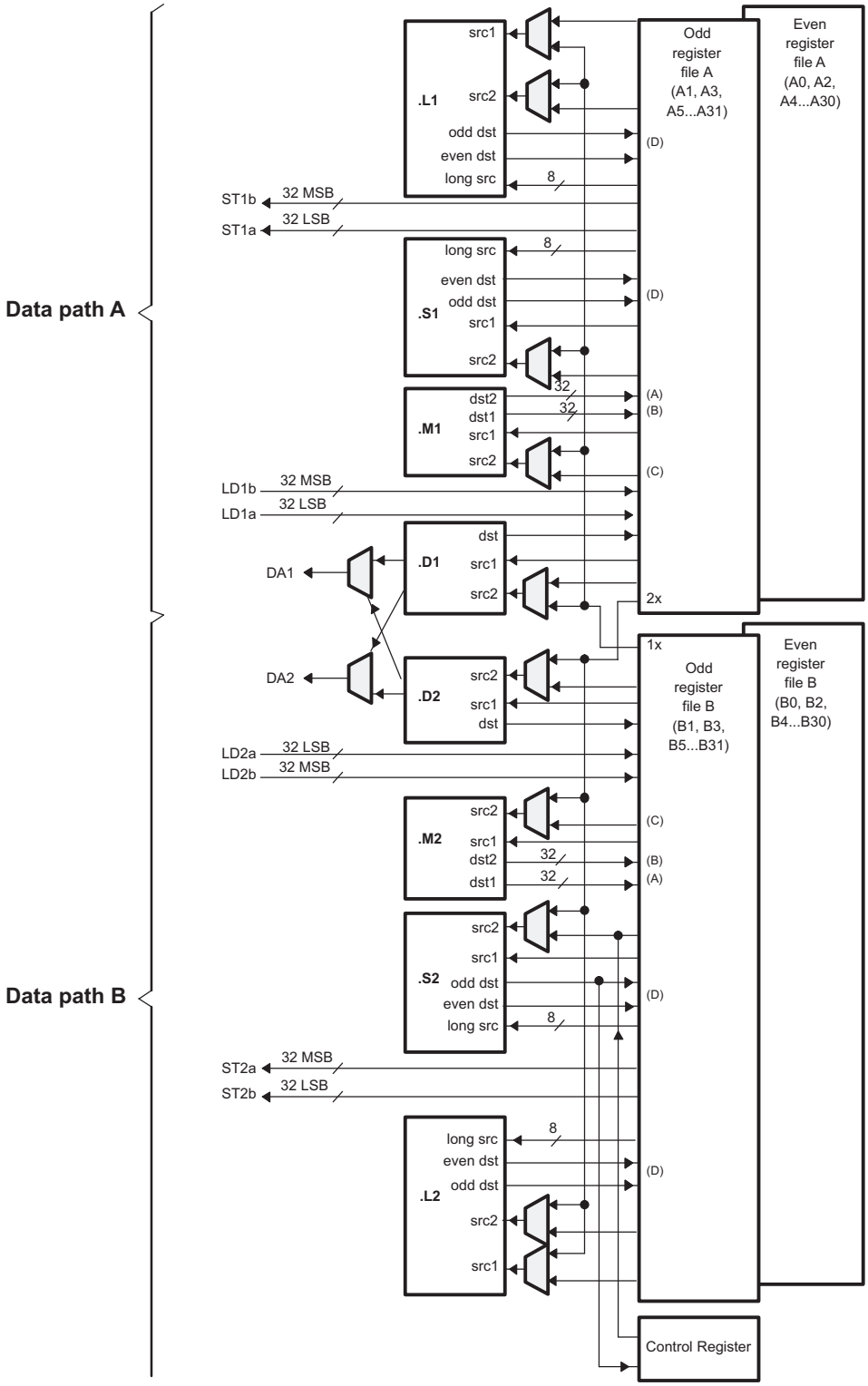

A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

Figure 2-1. TMS320C64x+™ CPU (DSP Core) Data Paths

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2.3 Memory Map Summary

Table 2-2 shows the memory map address ranges of the C6472 device. This table provides a combined view of both local and global addresses. The C64x+ megamodule local memories have both local and global addresses. The megamodule registers only have local addresses. Local addresses can only be resolved within the megamodule. They cannot be accessed from outside the megamodule. All of the other addresses listed in this table are global addresses. Global addresses can be accessed from any bus master including all six C64x+ megamodules, the transfer controllers within the EDMA3 block, and any peripheral that can master the bus.

Note: 1K = 1024, 1M = 1024K.

Table 2-2. C6472 Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
INTERNAL RAM AND ROM		
Reserved	2M	00000000 - 001FFFFF
SL2 RAM (Local address map)	768K	00200000 - 002BFFFF
Reserved	5.25M	002C0000 - 007FFFFF
Local L2 SRAM	608K	00800000 - 00897FFF
Reserved	5M + 416K	00898000 - 00DFFFFF
Local L1P SRAM	32K	00E00000 - 00E07FFF
Reserved	992K	00E08000 - 00EFFFFF
Local L1D SRAM	32K	00F00000 - 00F07FFF
Reserved	992K	00F08000 - 00FFFFFF
C64x+ MEGAMODULE REGISTERS		
Reserved	8M	01000000 - 017FFFFF
C64x+ Megamodule Registers	4M	01800000 - 01BFFFFF
CONTROL REGISTERS ON CONFIG SCR		
Reserved	9M	01C00000 - 024FFFFF
TSIP0	256K	02500000 - 0253FFFF
TSIP1	256K	02540000 - 0257FFFF
TSIP2	256K	02580000 - 025BFFFF
Reserved	128K	025C0000 - 025DFFFF
Timer0	64K	025E0000 - 025EFFFF
Timer1	64K	025F0000 - 025FFFFF
Timer2	64K	02600000 - 0260FFFF
Timer3	64K	02610000 - 0261FFFF
Timer4	64K	02620000 - 0262FFFF
Timer5	64K	02630000 - 0263FFFF
Timer6	64K	02640000 - 0264FFFF
Timer7	64K	02650000 - 0265FFFF
Timer8	64K	02660000 - 0266FFFF
Timer9	64K	02670000 - 0267FFFF
Timer10	64K	02680000 - 0268FFFF
Timer11	64K	02690000 - 0269FFFF
Reserved	1.875M	026A0000 - 0287FFFF
HPI Control	128K	02880000 - 0289FFFF
Reserved	1M	028A0000 - 0299FFFF
PLL Controller 1	1K	029A0000 - 029A03FF
Reserved	127K	029A0400 - 029BFFFF
PLL Controller 2	1K	029C0000 - 029C03FF

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Table 2-2. C6472 Memory Map Summary (continued)

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
PLL Controller 3	1K	029C0400 - 029C07FF
Reserved	254K	029C0800 - 029FFFFF
EDMA3 - EDMA3CC	32K	02A00000 - 02A07FFF
Reserved	96K	02A08000 - 02A1FFFF
EDMA3 - EDMA3TC0	32K	02A20000 - 02A27FFF
EDMA3 - EDMA3TC1	32K	02A28000 - 02A2FFFF
EDMA3 - EDMA3TC2	32K	02A30000 - 02A37FFF
EDMA3 - EDMA3TC3	32K	02A38000 - 02A3FFFF
Reserved	256K	02A40000 - 02A7FFFF
Chip-Level Registers	128K	02A80000 - 02A9FFFF
Reserved	32K	02AA0000 - 02AA7FFF
Shared Memory Controller	32K	02AA8000 - 02AAFFFF
Boot Controller	32K	02AB0000 - 02AB7FFF
Reserved	160K	02AB8000 - 02ADFFFF
PSC	128K	02AE0000 - 02AFFFFF
GPIO	16K	02B00000 - 02B03FFF
I2C Data and Control	16K	02B04000 - 02B07FFF
Reserved	224K	02B08000 - 02B3FFFF
UTOPIA	256K	02B40000 - 02B7FFFF
Reserved	256K	02B80000 - 02BBFFFF
UTOPIA-PDMA (PIM) Configuration	256K	02BC0000 - 02BFFFFF
Reserved	128K	02C00000 - 02C1FFFF
SMCP0	16K	02C20000 - 02C23FFF
SMCP1	16K	02C24000 - 02C27FFF
SMCP2	16K	02C28000 - 02C2BFFF
SMCP3	16K	02C2C000 - 02C2FFFF
SMCP4	16K	02C30000 - 02C33FFF
SMCP5	16K	02C34000 - 02C37FFF
Reserved	32K	02C38000 - 02C3FFFF
ETB0	4K	02C40000 - 02C40FFF
ETB1	4K	02C41000 - 02C41FFF
ETB2	4K	02C42000 - 02C42FFF
ETB3	4K	02C43000 - 02C43FFF
ETB4	4K	02C44000 - 02C44FFF
ETB5	4K	02C45000 - 02C45FFF
Reserved	232K	02C46000 - 02C7FFFF
EMAC0 Control	4K	02C80000 - 02C80FFF
EMIC0	2K	02C81000 - 02C817FF
MDIO Control Registers	2K	02C81800 - 02C81FFF
EMAC0 Descriptor Memory	8K	02C82000 - 02C83FFF
Reserved	240K	02C84000 - 02CBFFFF
EMAC1 Control	4K	02CC0000 - 02CC0FFF
EMIC1	2K	02CC1000 - 02CC17FF
Reserved	2K	02CC1800 - 02CC1FFF
EMAC1 Descriptor Memory	8K	02CC2000 - 02CC3FFF
Reserved	240K	02CC4000 - 02CFFFFF
RapidIO Control Registers	256K	02D00000 - 02D3FFFF

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Table 2-2. C6472 Memory Map Summary (continued)

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Reserved	768K	02D40000 - 02DFFFFF
RapidIO Descriptor Memory	16K	02E00000 - 02E03FFF
Reserved	209M + 1008K	02E04000 - 0FFFFFFF
INTERNAL RAM (GLOBAL MEMORY MAP)		
Reserved	2M	10000000 - 101FFFFF
SL2 RAM (through DSP0)	768K	10200000 - 102BFFFF
Reserved	5.25M	102C0000 - 107FFFFF
DSP0 L2 SRAM	608K	10800000 - 10897FFF
Reserved	5M + 416K	10898000 - 10DFFFFF
DSP0 L1P SRAM	32K	10E00000 - 10E07FFF
Reserved	992K	10E08000 - 10EFFFFF
DSP0 L1D SRAM	32K	10F00000 - 10F07FFF
Reserved	2M + 992K	10F08000 - 111FFFFF
SL2 RAM (through DSP1)	768K	11200000 - 112BFFFF
Reserved	5.25M	112C0000 - 117FFFFF
DSP1 L2 SRAM	608K	11800000 - 11897FFF
Reserved	5M + 416K	11898000 - 11DFFFFF
DSP1 L1P SRAM	32K	11E00000 - 11E07FFF
Reserved	992K	11E08000 - 11EFFFFF
DSP1 L1D SRAM	32K	11F00000 - 11F07FFF
Reserved	2M + 992K	11F08000 - 121FFFFF
SL2 RAM (through DSP2)	768K	12200000 - 122BFFFF
Reserved	5.25M	122C0000 - 127FFFFF
DSP2 L2 SRAM	608K	12800000 - 12897FFF
Reserved	5M + 416K	12898000 - 12DFFFFF
DSP2 L1P SRAM	32K	12E00000 - 12E07FFF
Reserved	992K	12E08000 - 12EFFFFF
DSP2 L1D SRAM	32K	12F00000 - 12F07FFF
Reserved	2M + 992K	12F08000 - 131FFFFF
SL2 RAM (through DSP3)	768K	13200000 - 132BFFFF
Reserved	5.25M	132C0000 - 137FFFFF
DSP3 L2 SRAM	608K	13800000 - 13897FFF
Reserved	5M + 416K	13898000 - 13DFFFFF
DSP3 L1P SRAM	32K	13E00000 - 13E07FFF
Reserved	992K	13E08000 - 13EFFFFF
DSP3 L1D SRAM	32K	13F00000 - 13F07FFF
Reserved	2M + 992K	13F08000 - 141FFFFF
SL2 RAM (through DSP4)	768K	14200000 - 142BFFFF
Reserved	5.25M	142C0000 - 147FFFFF
DSP4 L2 SRAM	608K	14800000 - 14897FFF
Reserved	5M + 416K	14898000 - 14DFFFFF
DSP4 L1P SRAM	32K	14E00000 - 14E07FFF
Reserved	992K	14E08000 - 14EFFFFF
DSP4 L1D SRAM	32K	14F00000 - 14F07FFF
Reserved	2M + 992K	14F08000 - 151FFFFF
SL2 RAM (through DSP5)	768K	15200000 - 152BFFFF
Reserved	5.25M	152C0000 - 157FFFFF

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Table 2-2. C6472 Memory Map Summary (continued)

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
DSP5 L2 SRAM	608K	15800000 - 15897FFF
Reserved	5M + 416K	15898000 - 15DFFFF
DSP5 L1P SRAM	32K	15E00000 - 15E07FFF
Reserved	992K	15E08000 - 15EFFFFF
DSP5 L1D SRAM	32K	15F00000 - 15F07FFF
Reserved	161M + 992K	15F08000 - 1FFFFFFF
DATA SPACE ON DMA		
Reserved	1408M	20000000 - 77FFFFFF
DDR2 EMIF Config	128M	78000000 - 7FFFFFFF
Reserved	1536M	80000000 - DFFFFFFF
CE0-CE1 DDR2 SDRAM	512M	E0000000 - FFFFFFFF

2.4 Boot Mode Sequence

The boot sequence is a process by which the DSP's internal memory is loaded with program and data sections and the DSP's internal registers are programmed with predetermined values. The boot sequence is started automatically after each power-on, warm, and system reset. For more details on the initiators of these resets, see Section 7.7, *Reset Controller*.

There are several methods by which the memory and register initialization can take place. Each of these methods is referred to as a boot mode. The boot mode to be used is selected at reset through the BOOTMODE[3:0] pins.

2.4.1 Boot Modes Supported

The TMS320C6472 has a dedicated Boot Controller, which is responsible for managing the boot process for single and multiple C64x+ megamodule core boots. There are two types of resets on the C6472 device:

1. Device-level Resets (Global Resets)
   - Power-on Reset; initiated by $\overline{\text{POR}}$
   - Chip-level Warm Reset (or Device Reset); initiated by $\overline{\text{RESET}}$
   - System Reset; initiated by a watchdog timeout or emulation
2. C64x+ megamodule-level Resets (Local Resets)
   - External C64x+ megamodule selectable LRESET
   - Local reset of the C64x+ megamodule initiated by on-chip Reset Controller
   - Power Sleep Controller initiated by local C64x+ megamodule reset

After $\overline{\text{POR}}$ and $\overline{\text{RESET}}$ asserted resets, the boot controller selects the boot mode based on the status of BOOTMODE[3:0] pins. When a system reset occurs, the boot mode used is determined by the BOOTMODE field in the DEVSTAT register. All possible bootmodes are listed in Table 2-3. For a detailed explanation of this operation, see the *TMS320C645x/C647x Bootloader User's Guide* (literature number SPRUEC6).

Following a device-level reset, each C64x+ megamodule core can set its boot mode choice for subsequent local resets using the registers BOOTMODE0 through BOOTMODE5 to either immediate boot mode or host boot mode. The default values of these registers are set to immediate boot mode.

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Table 2-3. Boot Mode Operation

BOOTMODE[3:0]	DESCRIPTION	TYPE	CFGGP[4:0]
0 (0000)	Immediate boot	Immediate Boot	Don't Care
1 (0001)	Host boot (HPI)	Host	Don't Care
2 (0010)	Master I2C boot for I2C address 50h	ROM	CFGGP[4] = 0 PLLx9 mode of main PLLCTL is selected 1 PLLx19 mode of main PLLCTL is selected CFGGP[3:0] = Boot PARAM index
3 (0011)	Master I2C boot for I2C address 51h	ROM	CFGGP[4] = 0 PLLx9 mode of main PLLCTL is selected 1 PLLx19 mode of main PLLCTL is selected CFGGP[3:0] = Boot PARAM index
4 (0100)	Slave I2C boot	ROM	CFGGP[4] = 0 PLLx9 mode of main PLLCTL is selected 1 PLLx19 mode of main PLLCTL is selected CFGGP[3:0] = Don't Care
5 (0101)	UTOPIA boot 8-bit PLLx10 of main PLLCTL	ROM	PHY ID
6 (0110)	UTOPIA boot 8-bit PLLx20 of main PLLCTL	ROM	PHY ID
7 (0111)	UTOPIA boot 16-bit PLLx10 of main PLLCTL	ROM	PHY ID
8 (1000)	UTOPIA boot 16-bit PLLx20 of main PLLCTL	ROM	PHY ID
9 (1001)	Ethernet MAC Port 0 boot (mode and speed determined by MACSEL0 pins)	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP[3:0]: Device ID (when RMII is selected, CFGGP[3] controls speed - 1 for 100 Mbs, 0 for 10 Mbps - and Device ID[3] is 0)
10 (1010)	Ethernet MAC Port 1 boot (mode and speed determined by MACSEL1 pins)	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP[3:0]: Device ID (when RMII is selected, CFGGP[3] controls speed - 1 for 100 Mbs, 0 for 10 Mbps - and Device ID[3] is 0)
11 (1011)	RIO1	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP [3:0]: Node (1111b for default)
12 (1100)	RIO2	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP [3:0]: Node (1111b for default)

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Table 2-3. Boot Mode Operation (continued)

BOOTMODE[3:0]	DESCRIPTION	TYPE	CFGGP[4:0]
13 (1101)	RIO3	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP [3:0]: Node (1111b for default)
14 (1110)	RIO4	ROM	CFGGP[4] = 0 PLLx10 mode of main PLLCTL is selected 1 PLLx20 mode of main PLLCTL is selected CFGGP [3:0]: Node (1111b for default)
15 (1111)	Reserved	ROM	Reserved

- Immediate boot

  When immediate boot is selected after global reset, the C64x+ megamodule core executes directly from the internal L2 SRAM address programmed in the DSP_BOOT_ADDRx register. Note: device operation is undefined if invalid code is address programmed in the DSP_BOOT_ADDRx register. Executing invalid code may prevent connection by an emulator.

  The default start addresses for megamodule core 0-5 boot are listed in Table 2-4.

Table 2-4. Megamodule Core 0-5 Boot Start Addresses

MEGAMODULE CORE NAME	DEFAULT START ADDRESSES FOR DEVICE RESET/ BOOT MODE 0-1	DEFAULT START ADDRESSES FOR DEVICE RESET/ BOOT MODE 2-15	DEFAULT START ADDRESSES FOR LOCAL RESET
Megamodule Core 0	0x0080_0000	0x0010_0000	0x0010_0000, if the device reset was boot mode 2-15; otherwise 0x0080_0000
Megamodule Core 1	0x0080_0000	0x0080_0000	0x0080_0000
Megamodule Core 2	0x0080_0000	0x0080_0000	0x0080_0000
Megamodule Core 3	0x0080_0000	0x0080_0000	0x0080_0000
Megamodule Core 4	0x0080_0000	0x0080_0000	0x0080_0000
Megamodule Core 5	0x0080_0000	0x0080_0000	0x0080_0000

  For boot mode 1, these addresses can be modifed by the host before it releases each megamodule core from reset; for details, see Section 3.9.5. For boot mode 2-15, it is possible to have megamodule core 0 modify the default address of megamodule core 1-5 before it releases each megamodule core from reset; for details, see Section 2.4.1. For local reset, if all cores are required to begin from a particular address, the default addresses have to be modified. One example is that only the megamodule core 0's default address is modified to match megamodule core 1-5.

- Host boot

  If host boot is selected after global reset, all C64x+ megamodule cores are internally "held in reset" while the remainder of the device (including all memory subsystems of the C64x+ megamodule) is released from reset. During this period, an external host can initialize the C6472 device memory space (shared memory as well as the C64x+ megamodule memory), as necessary through an HPI interface, including internal configuration registers such as those that control the DDR2 or other peripherals. Once the host is finished with all necessary initialization, it must write a 1 to bit fields BC0 through BC5 of the BOOT_COMPLETE_STAT register (inside the Boot Controller) indicating boot complete of the

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corresponding C64x+ megamodule. This transition causes the Boot Controller to bring the C64x+ megamodule core out of the "held-in-reset" state. The CPU then begins execution from the internal L2 SRAM address programmed in the DSP_BOOT_ADDRx register. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP, if required.

For the C6472 device, only the Host Port Interface (HPI) peripheral can be used for host boot. PLL1, which provides CPU/6 clock to the HPI module, will initially be running in bypass mode. Therefore, the HPI interface will be very slow and $\overline{\text{HRDY}}$ must be observed. Initial HPI accesses can configure PLL1 for full-speed operation to make HPI accesses shorter.

- Master I2C boot

  After global reset, the C64x+ megamodule core 0 comes out of RESET and starts executing the shared ROM code from the address provided by the Boot Controller based on the I2C boot mode selection. Then C64x+ megamodule core 0 configures I2C and acts as a master to the I2C bus and copies data from an I2C EPROM or a device acting as an I2C slave to the DSP using a predefined boot table format. The destination address and length are contained within the boot table. After initializing the on-chip memory to the known state and initializing the start address of the other C64x+ megamodule cores, C64x+ megamodule core 0 brings the other cores out of reset by writing a 1 to bit fields BC1 through BC5 of the BOOT_COMPLETE_STAT register. After this, C64x+ megamodule cores 1 through 5 start executing from the start address provided by C64x+ megamodule core 0.

- Slave I2C boot

  A Slave I2C boot is also implemented, which programs the DSP as an I2C slave. A DSP in I2C slave mode will never transmit on the I2C bus. The slave DSP must first receive a three-word transmission from the master. This transmission includes a 16-bit length field (length is in bytes, should be 6 for this block), a 16-bit checksum field for which a value of zero means ignore the checksum, and the 16-bit options field described in the boot parameter table for standard I2C boot. This option field informs the slave what information is contained in the next data blocks. Typically, the option field is set to 1 to indicate boot tables will be received next. Only core 0 is active during the boot process. Using the slave I2C boot, a single DSP or device acting as an I2C master can simultaneously boot multiple slave DSPs connected to the same I2C bus. Note that the master DSP may require booting via an I2C EEPROM before acting as a master and booting other DSPs.

- Ethernet MAC boot

  When BOOTMODE [3:0] = 1001 is selected, Ethernet MAC boot is initiated on EMAC0 with the mode specified by the MACSEL0[2:0] pins. Alternately, when BOOTMODE [3:0] = 1010 is selected, Ethernet MAC boot is initiated on EMAC1 with the mode specified by the MACSEL1[1:0] pins.

  After reset, the C64x+ megamodule core 0 comes out of RESET and starts executing the shared ROM code from the address provided by the Boot Controller based on the Ethernet boot mode selection (1001b or 1010b). The C64x+ megamodule core 0 configures the appropriate Ethernet MAC and brings the code image into the on-chip memory via the protocol defined. After initializing the on-chip memory to the known state and initializing the start address of the other C64x+ megamodule cores (1 through 5), C64x+ megamodule core 0 brings the other cores out of reset by writing a 1 to bit fields BC1 through BC5 of the BOOT_COMPLETE_STAT register. After this, C64x+ megamodule cores 1 through 5 start executing from the start address provided by C64x+ megamodule core 0.

- Serial RapidIO boot

  After reset, the C64x+ megamodule core 0 comes out of RESET and starts executing the shared ROM code from the address provided by the Boot Controller based on the Serial RapidIO boot mode selection (1011b, 1100b, 1101b, or 1110b). The C64x+ megamodule core 0 configures Serial RapidIO and EDMA, if required, and brings the code image into the on-chip memory via the protocol defined by the boot method (SRIO bootloader). After initializing the on-chip memory to the known state and initializing the start address of the other C64x+ megamodule cores (1 through 5), C64x+ megamodule core 0 brings the other cores out of reset by writing a 1 to bit fields BC1 through BC5 of the BOOT_COMPLETE_STAT register. After this, the C64x+ megamodule cores 1 through 5 start executing from the start address provided by C64x+ megamodule core 0.

- UTOPIA boot

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After reset, the C64x+ megamodule core 0 comes out of RESET and starts executing the shared ROM code from the address provided by the Boot Controller based on the UTOPIA boot mode selection (0101b, 0110b, 0111b, 1000b). The C64x+ megamodule core 0 configures the UTOPIA and brings the code image into the on-chip memory via the protocol defined. After initializing the on-chip memory to the known state and initializing the start address of the other C64x+ megamodule cores (1 through 5), C64x+ megamodule core 0 brings the other cores out of reset by writing a 1 to bit fields ofBC1 through BC5 the BOOT_COMPLETE_STAT register. After this, C64x+ megamodule cores 1 through 5 start executing from the start address provided by C64x+ megamodule core 0.

After local resets, the C6472 device supports two boot modes via BOOTMODE0-BOOTMODE5 device-level registers:

- Immediate boot

  When immediate boot is selected after global reset, the C64x+ megamodule core (x) executes directly from the internal L2 SRAM address programmed in the DSP_BOOT_ADDRx register upon being given a local reset. Note: device operation is undefined if invalid code is address programmed in the DSP_BOOT_ADDRx register. Executing invalid code may prevent connection by an emulator.

- Host boot

  If host boot is selected after global reset, the C64x+ megamodule core (x) is internally "held in reset" while the remainder of the C64x+ megamodule is released from reset upon being given a local reset. During this period, an external host can initialize the C64x+ megamodule (x) memory space, as necessary, through an HPI interface. Once the host is finished with all necessary initialization, it must write a 1 to the corresponding bit field BCx of the BOOT_COMPLETE_STAT register (inside the Boot Controller) indicating boot complete of the corresponding C64x+ megamodule. This transition causes the Boot Controller to bring the C64x+ megamodule core out of the "held-in-reset" state. The core (x) then begins execution from the internal L2 SRAM programmed in the DSP_BOOT_ADDRx register. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP, if required.

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2.4.2 BOOTACTIVE

The output pin, BOOTACTIVE, is asserted upon reset and de-asserted on boot complete. In the case of BOOTMODE 0, all cores are released from reset immediately. BOOTACTIVE also goes low within a small number of cycles, as all cores are out of reset and running. In the case of BOOTMODE 1, the host needs to write to the boot complete bit in the BOOT_COMPLETE_STAT register corresponding to each C64x+ megamodule that is to be taken out of reset. BOOTACTIVE will be high if any cores are held in reset. In the case of any other boot, core 0 comes out of RESET immediately, but all other cores are still in RESET, so BOOTACTIVE will be high. The ROM code will not write to either the BOOT_COMPLETE_STAT or the BOOT_ADDRESS register unless explicitly directed to do so by the data provided in the boot process. Any active core can set bits in BOOT_COMPLETE_STAT at any time to begin code execution on inactive cores. BOOTACTIVE will go low after the boot complete bit (BCx) in the BOOT_COMPLETE_STAT register is set for all six cores. For a detailed explanation of this operation, see the *TMS320C645x/C647x Bootloader User's Guide* (literature number SPRUEC6).

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2.5 Pin Assignments

2.5.1 Pin Map

Figure 2-2 through Figure 2-5 show the C6472 pin assigments in four quadrants (A, B, C, and D).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
AJ	DV_{DD33}	V_{SS}	RSV11	DV_{DD33}	V_{SS}	MRXD07	MTXD05/ RMTXD11	V_{SS}	MTCLK0/ REFCLK0/ SREFCLK0	MRXD03/ SRXSYNC1	MRXD02/ SRXD1	DV_{DD33}	MRXD06/ RMRXER1	V_{SS}	RGRD13	AJ
AH	V_{SS}	TX14	TR21	LENDIAN	MACSEL11	RSV10	MTXD01/ RMTXD01/ STXSYNC0	DV_{DD33}	MRXD04/ RMRXD10	GMDIO	MRXD00/ RMRXD00/ SRXD0	V_{SS}	CLKIN2	DV_{DD15}	RGRD12	AH
AG	TR17	TR16	TX27	RSV12	MACSEL01	GMTCLK0/ REFCLK1/ SREFCLK1	MRXD05/ RMRXD11	MTXD02/ STXD1	GMDCLK	MRCLK0/ SRXCLK1	MTXD07/ STXCLK0	MRXD01/ RMRXD01/ SRXSYNC0	$DV_{DD15MON}$	AV_{DDA2}	RGRXC1	AG
AF	FSA1	TX11	TR22	TX20	MACSEL10	MACSEL02	RSV09	MTXD00/ RMTXD00/ STXD0	MTXD03/ STXSYNC1	MCRS0/ RMCRSDV0	MTXEN0/ RMRTXEN0	MRXER0/ RMRXER0/ SRXCLK0	HHV15EN	PTV15P	RGRD11	AF
AE	V_{SS}	DV_{DD33}	TX26	TR24	TR23	MACSEL00	MTDX04/ RMTXD10/ STXCLK1	MCOL0	CV_{DDMON}	CV_{DD}	MTDX06/ RMTXEN1	MRXDV0/ RMCRSDV1	RSV14	PTV15N	RGRD10	AE
AD	TX16	TX15	TX13	TR26	TX22	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD15}	AD
AC	CLKB1	TR15	TR10	TX24	TX23	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD15}	V_{SS}	AC
AB	V_{SS}	DV_{DD33}	TR11	TR27	TR20	V_{SS}	DV_{DD33}									AB
AA	TR02	CLKB2	TX10	TR25	TX21	DV_{DD33}	V_{SS}									AA
Y	FSB0	TX17	TR12	TX12	TX25	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	Y
W	V_{SS}	DV_{DD33}	FSA2	TR14	TR13	DV_{DD33}	V_{SS}			CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	W
V	TR03	FSA0	CLKA1	CLKA2	$DV_{DD33MON}$	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V
U	TR07	TX00	CLKA0	TR01	FSB2	DV_{DD33}	V_{SS}			CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	U
T	V_{SS}	DV_{DD33}	TR00	TX02	FSB1	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	T
R	TX05	TR05	TR06	CLKB0	TX01	DV_{DD33}	V_{SS}			CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 2-2. C6472 Pin Map (Bottom View) [Quadrant A]

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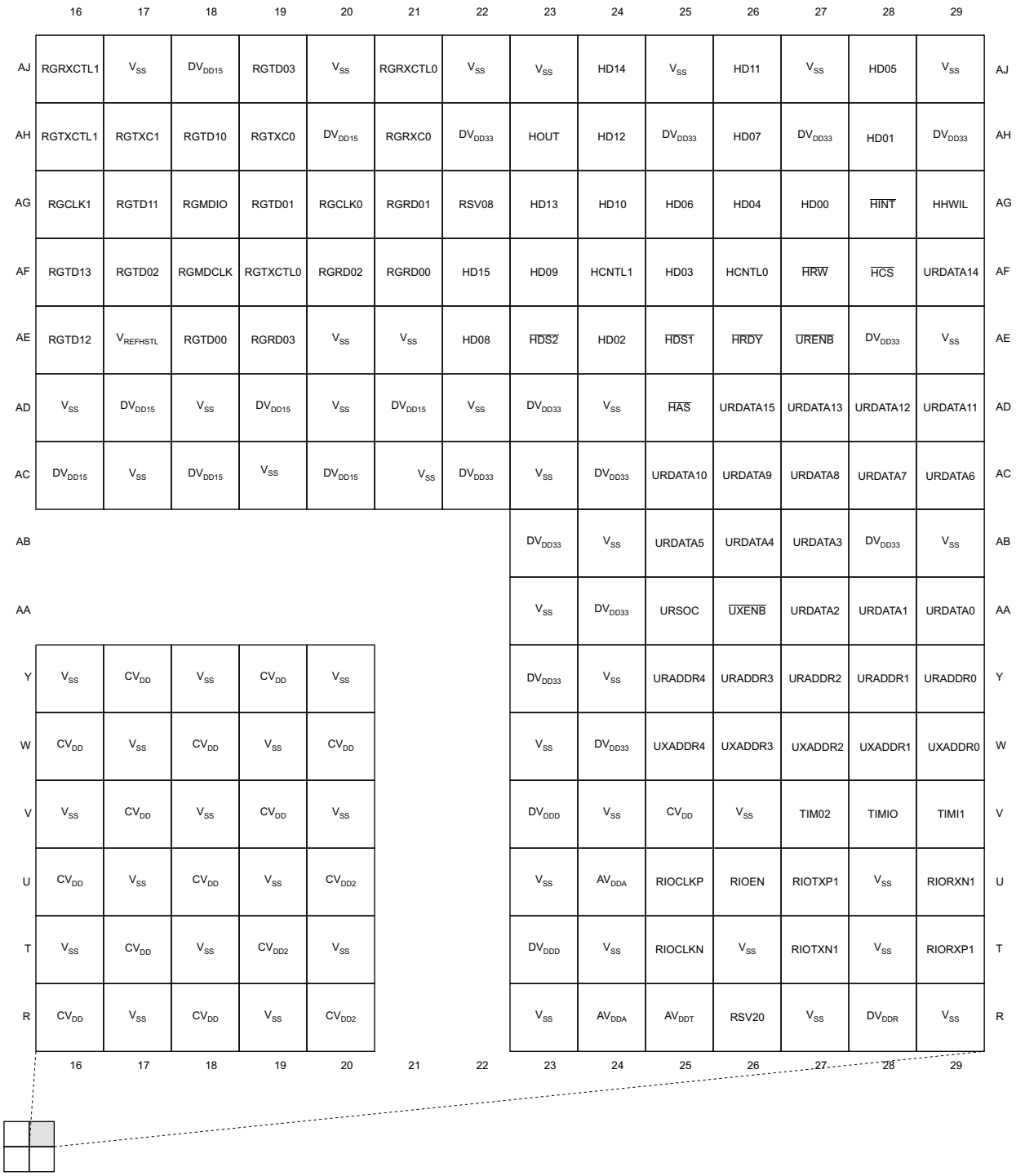

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AJ	RGRXCTL1	V_{SS}	DV_{DD15}	RGTD03	V_{SS}	RGRXCTL0	V_{SS}	V_{SS}	HD14	V_{SS}	HD11	V_{SS}	HD05	V_{SS}	AJ
AH	RGTXCTL1	RGTXC1	RGTD10	RGTXC0	DV_{DD15}	RGRXC0	DV_{DD33}	HOUT	HD12	DV_{DD33}	HD07	DV_{DD33}	HD01	DV_{DD33}	AH
AG	RGCLK1	RGTD11	RGMDIO	RGTD01	RGCLK0	RGRD01	RSV08	HD13	HD10	HD06	HD04	HD00	$\overline{HINT}$	HHWIL	AG
AF	RGTD13	RGTD02	RGMDCLK	RGTXCTL0	RGRD02	RGRD00	HD15	HD09	HCNTL1	HD03	HCNTL0	$\overline{HRW}$	$\overline{HCS}$	URDATA14	AF
AE	RGTD12	$V_{REFHSTL}$	RGTD00	RGRD03	V_{SS}	V_{SS}	HD08	$\overline{HDS2}$	HD02	$\overline{HDS1}$	$\overline{HRDY}$	$\overline{URENB}$	DV_{DD33}	V_{SS}	AE
AD	V_{SS}	DV_{DD15}	V_{SS}	DV_{DD15}	V_{SS}	DV_{DD15}	V_{SS}	DV_{DD33}	V_{SS}	$\overline{HAS}$	URDATA15	URDATA13	URDATA12	URDATA11	AD
AC	DV_{DD15}	V_{SS}	DV_{DD15}	V_{SS}	DV_{DD15}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	URDATA10	URDATA9	URDATA8	URDATA7	URDATA6	AC
AB								DV_{DD33}	V_{SS}	URDATA5	URDATA4	URDATA3	DV_{DD33}	V_{SS}	AB
AA								V_{SS}	DV_{DD33}	URSOC	$\overline{UXENB}$	URDATA2	URDATA1	URDATA0	AA
Y	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}			DV_{DD33}	V_{SS}	URADDR4	URADDR3	URADDR2	URADDR1	URADDR0	Y
W	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}			V_{SS}	DV_{DD33}	UXADDR4	UXADDR3	UXADDR2	UXADDR1	UXADDR0	W
V	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}			DV_{DDD}	V_{SS}	CV_{DD}	V_{SS}	TIM02	TIMIO	TIMI1	V
U	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD2}			V_{SS}	AV_{DDA}	RIOCLKP	RIOEN	RIOTXP1	V_{SS}	RIORXN1	U
T	V_{SS}	CV_{DD}	V_{SS}	CV_{DD2}	V_{SS}			DV_{DDD}	V_{SS}	RIOCLKN	V_{SS}	RIOTXN1	V_{SS}	RIORXP1	T
R	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD2}			V_{SS}	AV_{DDA}	AV_{DDT}	RSV20	V_{SS}	DV_{DDR}	V_{SS}	R
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-3. C6472 Pin Map (Bottom View) [Quadrant B]

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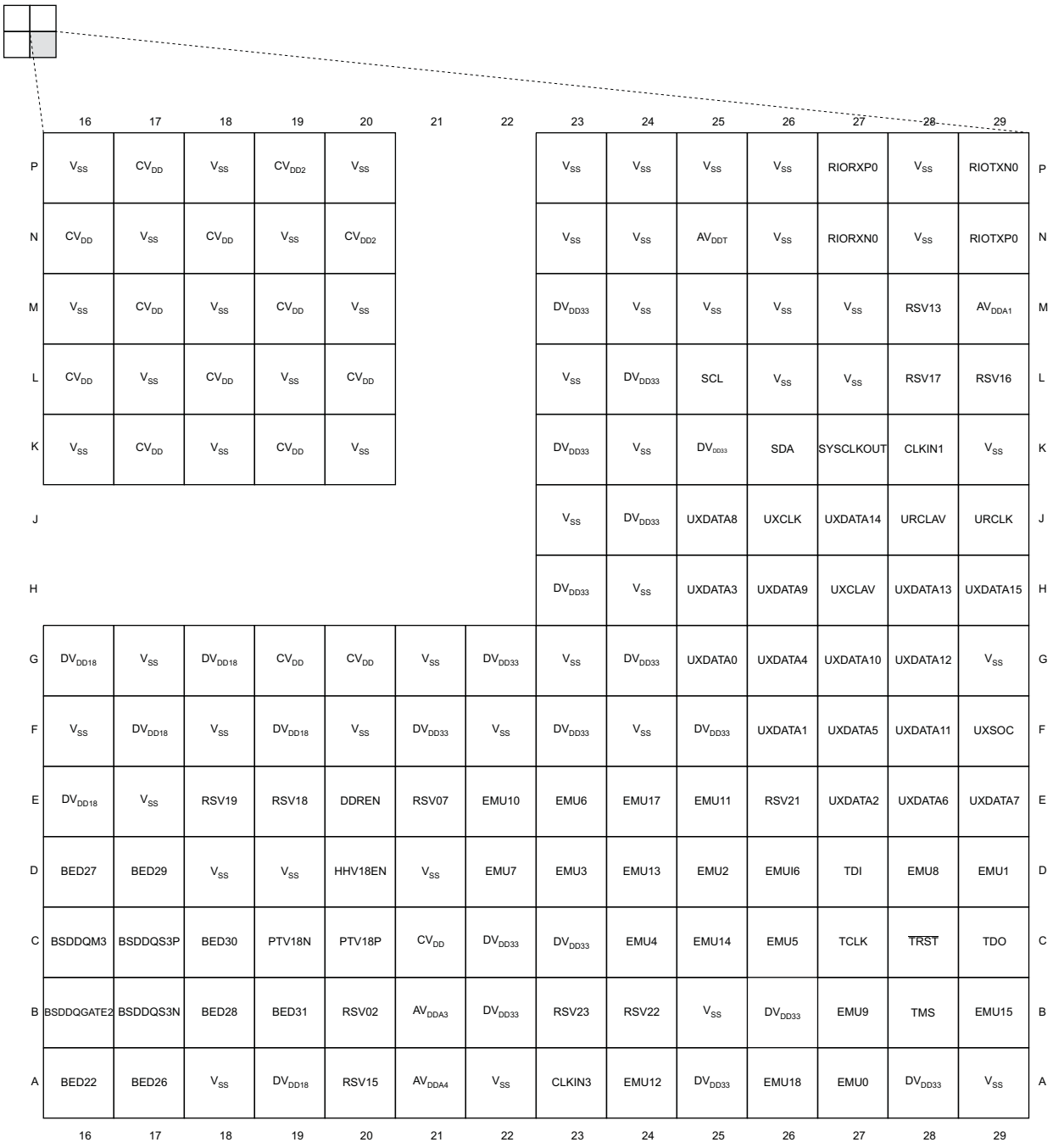

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
P	V_{SS}	CV_{DD}	V_{SS}	CV_{DD2}	V_{SS}			V_{SS}	V_{SS}	V_{SS}	V_{SS}	RIORXP0	V_{SS}	RIOTXN0	P
N	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD2}			V_{SS}	V_{SS}	AV_{DDT}	V_{SS}	RIORXN0	V_{SS}	RIOTXP0	N
M	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}			DV_{DD33}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	RSV13	AV_{DDA1}	M
L	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}			V_{SS}	DV_{DD33}	SCL	V_{SS}	V_{SS}	RSV17	RSV16	L
K	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}			DV_{DD33}	V_{SS}	DV_{DD33}	SDA	SYSCLKOUT	CLKIN1	V_{SS}	K
J								V_{SS}	DV_{DD33}	UXDATA8	UXCLK	UXDATA14	URCLAV	URCLK	J
H								DV_{DD33}	V_{SS}	UXDATA3	UXDATA9	UXCLAV	UXDATA13	UXDATA15	H
G	DV_{DD18}	V_{SS}	DV_{DD18}	CV_{DD}	CV_{DD}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	UXDATA0	UXDATA4	UXDATA10	UXDATA12	V_{SS}	G
F	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	UXDATA1	UXDATA5	UXDATA11	UXSOC	F
E	DV_{DD18}	V_{SS}	RSV19	RSV18	DDREN	RSV07	EMU10	EMU6	EMU17	EMU11	RSV21	UXDATA2	UXDATA6	UXDATA7	E
D	BED27	BED29	V_{SS}	V_{SS}	HHV18EN	V_{SS}	EMU7	EMU3	EMU13	EMU2	EMUI6	TDI	EMU8	EMU1	D
C	BSDDQM3	BSDDQS3P	BED30	PTV18N	PTV18P	CV_{DD}	DV_{DD33}	DV_{DD33}	EMU4	EMU14	EMU5	TCLK	$\overline{TRST}$	TDO	C
B	BSDDQGATE2	BSDDQS3N	BED28	BED31	RSV02	AV_{DDA3}	DV_{DD33}	RSV23	RSV22	V_{SS}	DV_{DD33}	EMU9	TMS	EMU15	B
A	BED22	BED26	V_{SS}	DV_{DD18}	RSV15	AV_{DDA4}	V_{SS}	CLKIN3	EMU12	DV_{DD33}	EMU18	EMU0	DV_{DD33}	V_{SS}	A
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-4. C6472 Pin Map (Bottom View) [Quadrant C]

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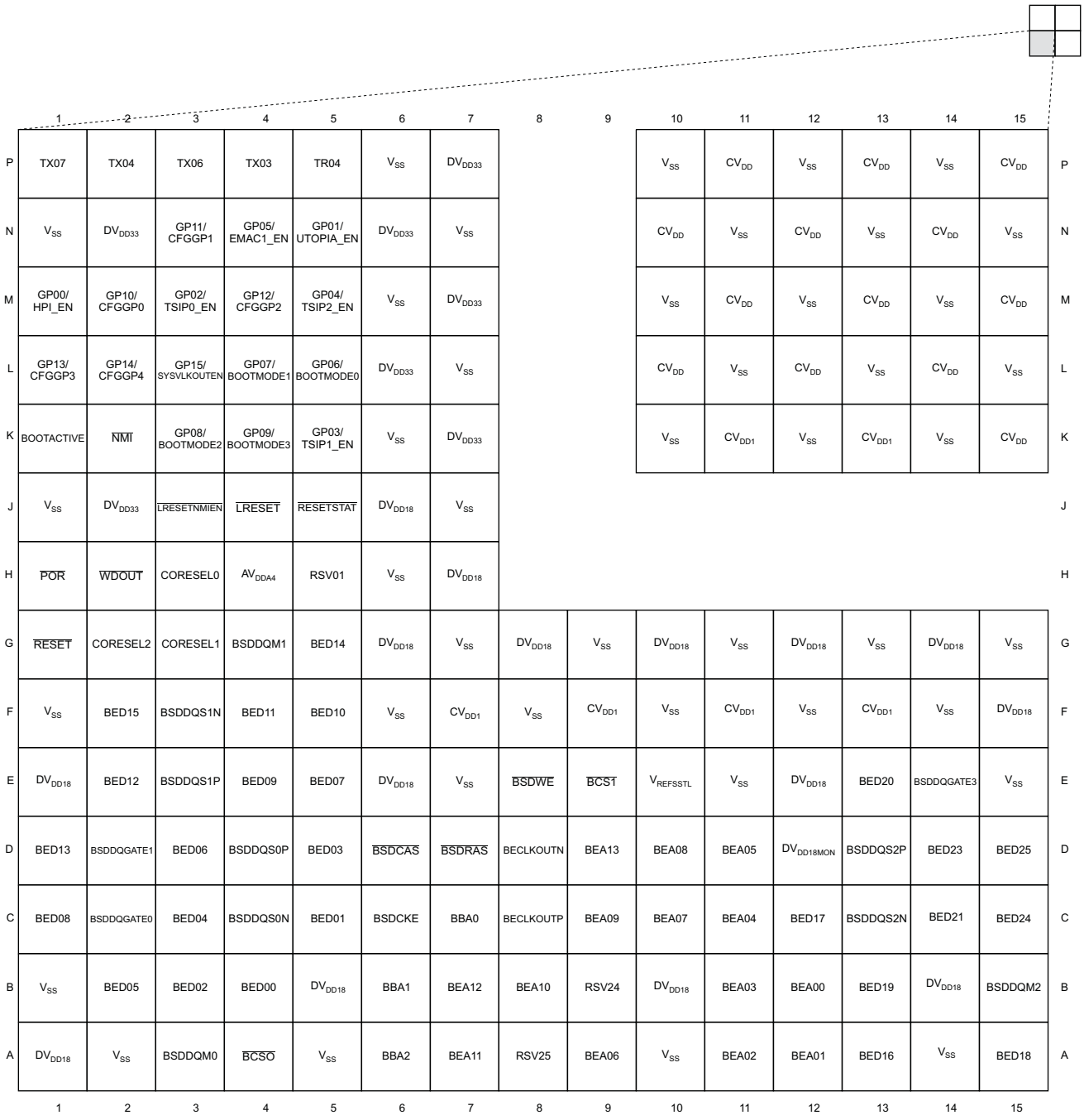

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
P	TX07	TX04	TX06	TX03	TR04	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	P
N	V_{SS}	DV_{DD33}	GP11/ CFGGP1	GP05/ EMAC1_EN	GP01/ UTOPIA_EN	DV_{DD33}	V_{SS}			CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	N
M	GP00/ HPI_EN	GP10/ CFGGP0	GP02/ TSIP0_EN	GP12/ CFGGP2	GP04/ TSIP2_EN	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	M
L	GP13/ CFGGP3	GP14/ CFGGP4	GP15/ SYSVLKOUTEN	GP07/ BOOTMODE1	GP06/ BOOTMODE0	DV_{DD33}	V_{SS}			CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	L
K	BOOTACTIVE	$\overline{NMI}$	GP08/ BOOTMODE2	GP09/ BOOTMODE3	GP03/ TSIP1_EN	V_{SS}	DV_{DD33}			V_{SS}	CV_{DD1}	V_{SS}	CV_{DD1}	V_{SS}	CV_{DD}	K
J	V_{SS}	DV_{DD33}	$\overline{LRESETNMIEN}$	$\overline{LRESET}$	$\overline{RESETSTAT}$	DV_{DD18}	V_{SS}									J
H	$\overline{POR}$	$\overline{WDOUT}$	CORESEL0	AV_{DDA4}	RSV01	V_{SS}	DV_{DD18}									H
G	$\overline{RESET}$	CORESEL2	CORESEL1	BSDDQM1	BED14	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	DV_{DD18}	V_{SS}	G
F	V_{SS}	BED15	BSDDQS1N	BED11	BED10	V_{SS}	CV_{DD1}	V_{SS}	CV_{DD1}	V_{SS}	CV_{DD1}	V_{SS}	CV_{DD1}	V_{SS}	DV_{DD18}	F
E	DV_{DD18}	BED12	BSDDQS1P	BED09	BED07	DV_{DD18}	V_{SS}	$\overline{BSDWE}$	$\overline{BCST}$	$V_{REFSSTL}$	V_{SS}	DV_{DD18}	BED20	BSDDQGATE3	V_{SS}	E
D	BED13	BSDDQGATE1	BED06	BSDDQS0P	BED03	$\overline{BSDCAS}$	$\overline{BSDRAS}$	BECLKOUTN	BEA13	BEA08	BEA05	$DV_{DD18MON}$	BSDDQS2P	BED23	BED25	D
C	BED08	BSDDQGATE0	BED04	BSDDQS0N	BED01	BSDCKE	BBA0	BECLKOUTP	BEA09	BEA07	BEA04	BED17	BSDDQS2N	BED21	BED24	C
B	V_{SS}	BED05	BED02	BED00	DV_{DD18}	BBA1	BEA12	BEA10	RSV24	DV_{DD18}	BEA03	BEA00	BED19	DV_{DD18}	BSDDQM2	B
A	DV_{DD18}	V_{SS}	BSDDQM0	$\overline{BCSO}$	V_{SS}	BBA2	BEA11	RSV25	BEA06	V_{SS}	BEA02	BEA01	BED16	V_{SS}	BED18	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 2-5. C6472 Pin Map (Bottom View) [Quadrant D]

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2.6 Signal Groups Description

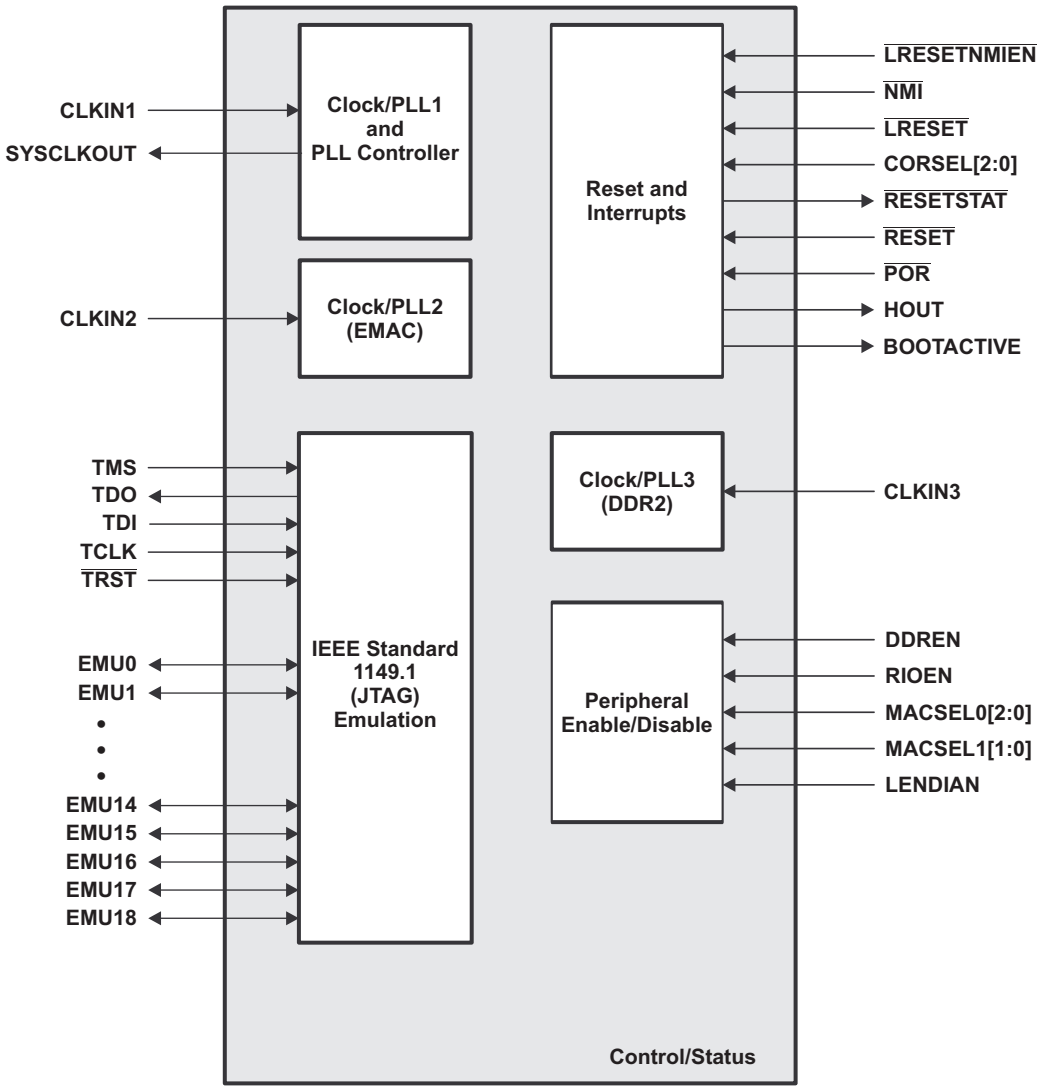

Figure 2-6. CPU and Peripheral Signals

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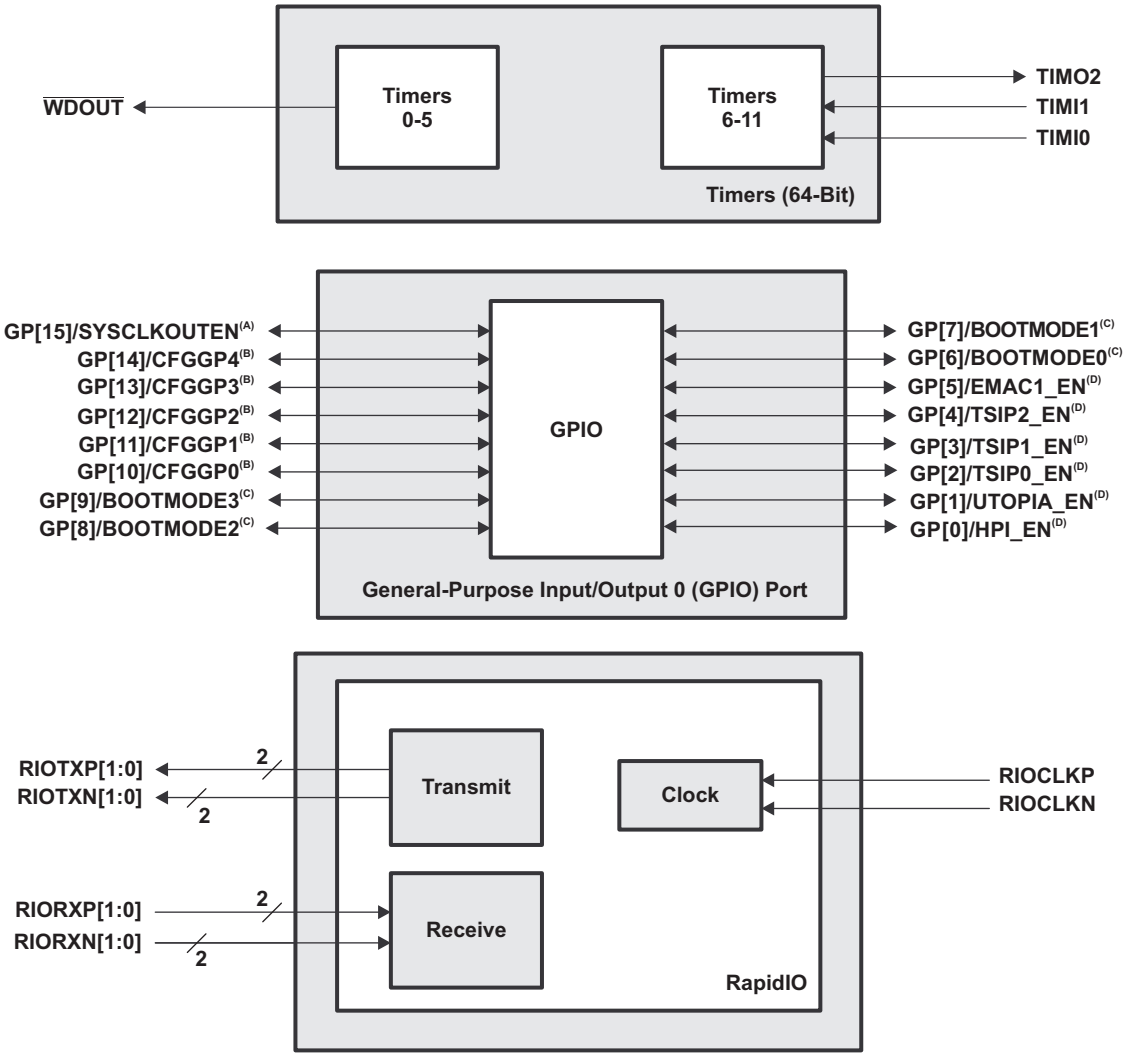

A. The SYSCLKOUTEN pin is muxed with GP[15]. For more details, see Section 3.
B. These CONFIG pins are muxed with the GPIO peripheral pins. For more details, see Section 3.
C. These BOOTMODE pins are muxed with the GPIO peripheral pins. For more details, see Section 3.
D. These pins are muxed with GPIO peripheral pins. For more details, see Section 3.

Figure 2-7. Timers/GPIO/RapidIO Peripheral Signals

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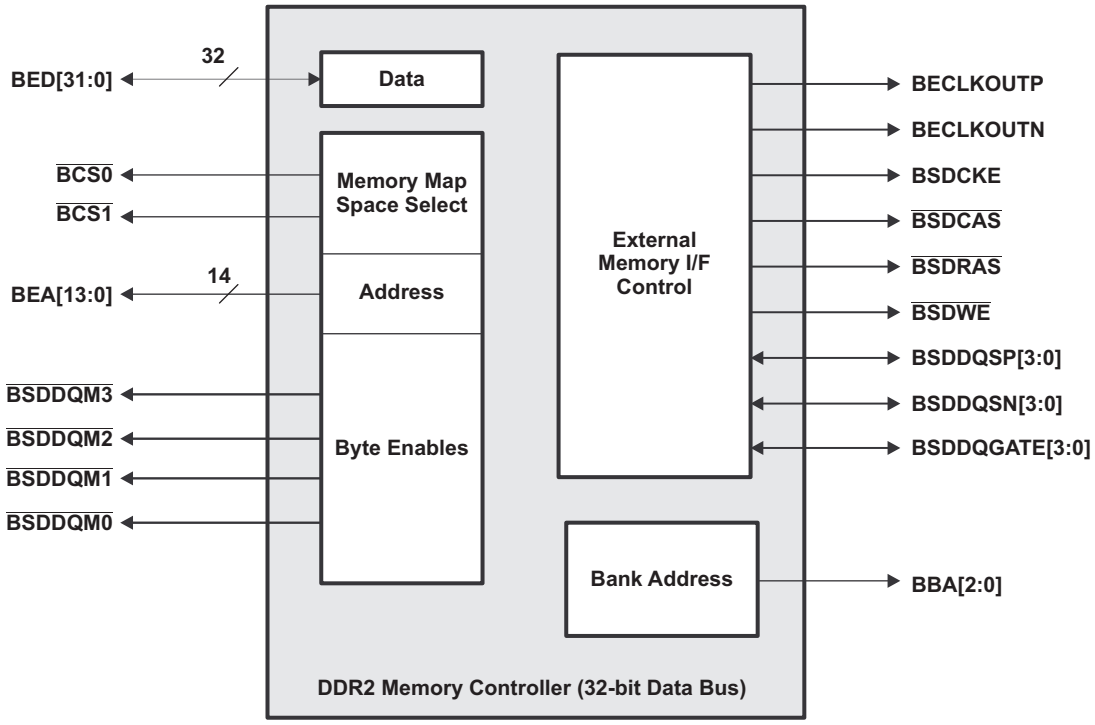

Figure 2-8. DDR2 Memory Controller Peripheral Signals

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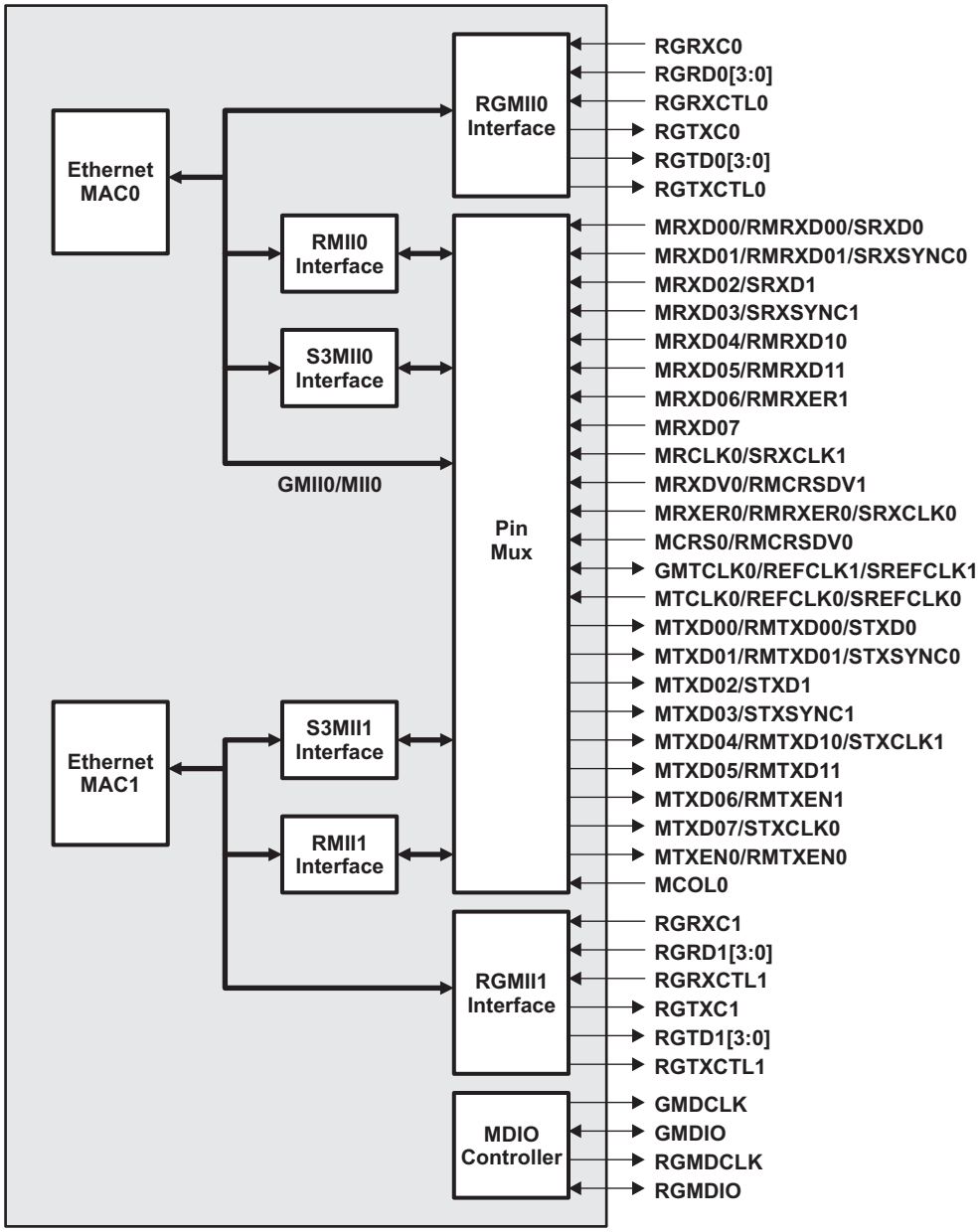

Figure 2-9. EMAC[1:0]/MDIO (RGMII[1:0], S3MII[1:0], MII0, RMII[1:0], and GMII0) Peripheral Signals

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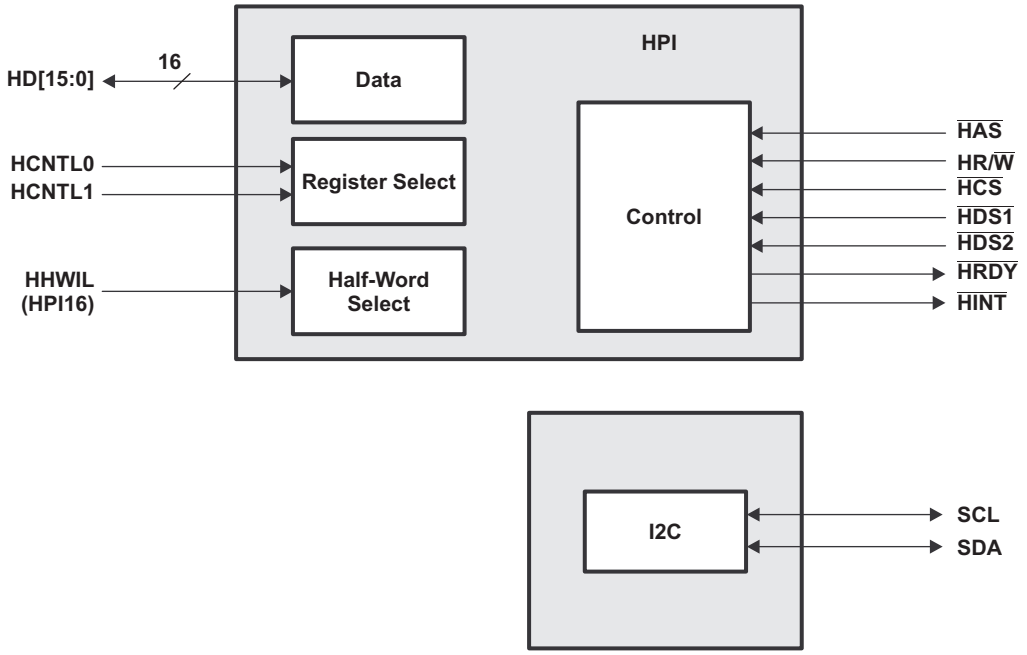

Figure 2-10. HPI/I2C Peripheral Signals

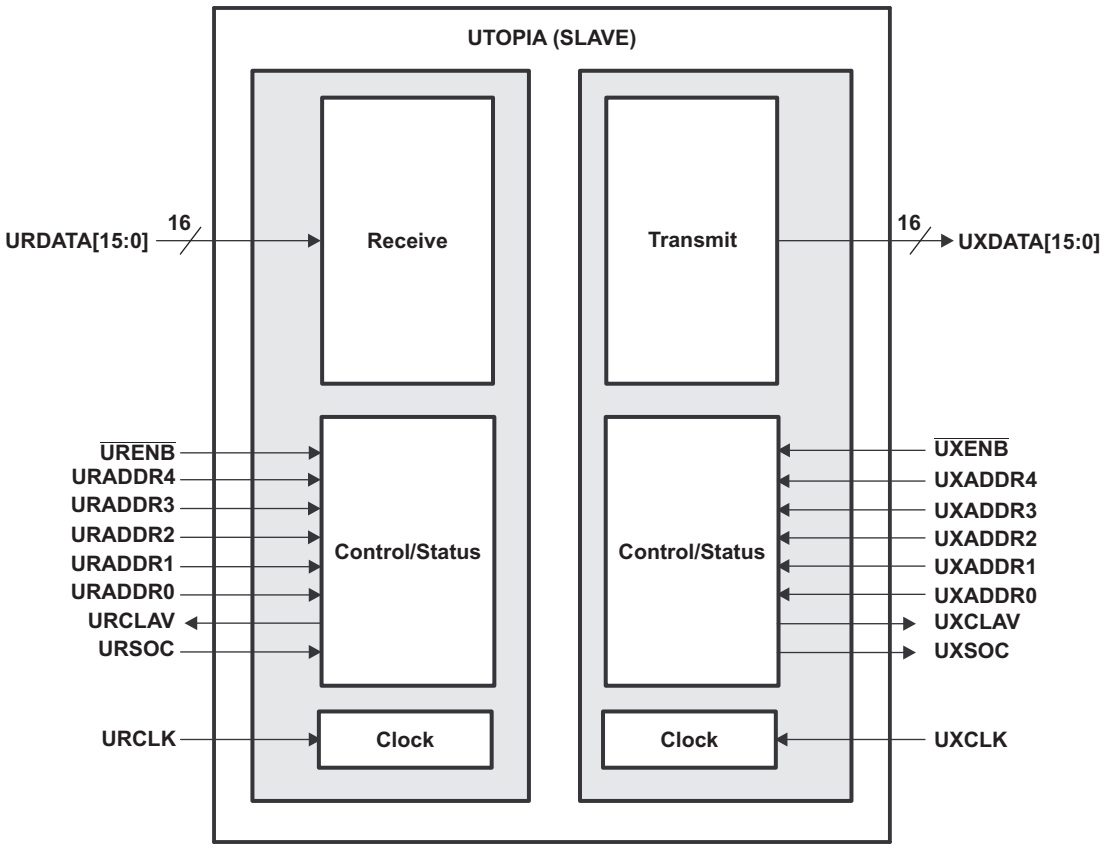

Figure 2-11. UTOPIA Peripheral Signals

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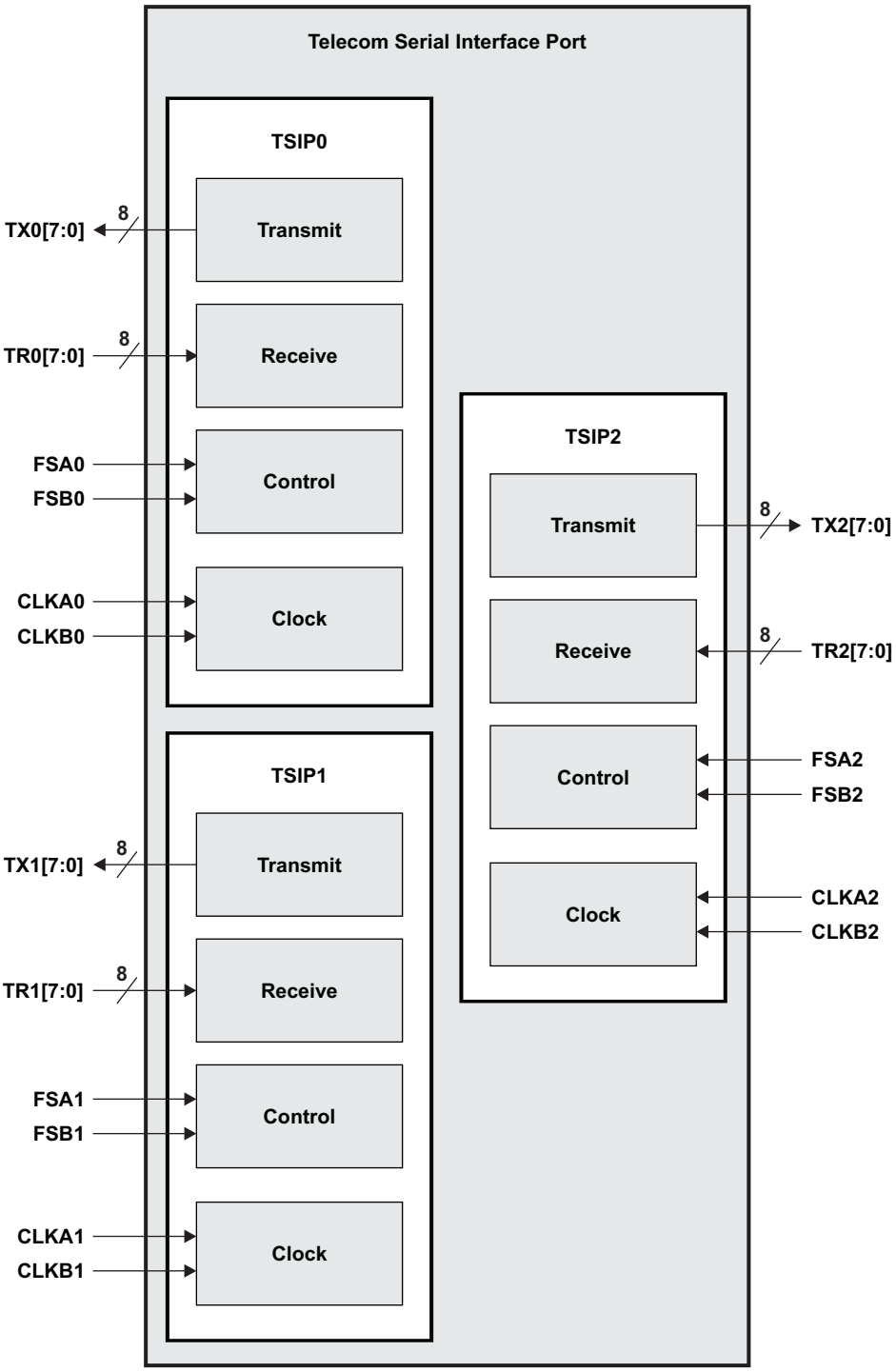

Figure 2-12. TSIP[2:0] Peripheral Signals

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2.7 Terminal Functions

The terminal functions table (Table 2-5) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see Section 3.

Table 2-5. Terminal Functions

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
CONFIGURATION PINS				
MACSEL0[0]	AE6	I	IPD	EMAC0 configuration select pin (for details, see Table 3-1).
MACSEL0[1]	AG5	I	IPD	
MACSEL0[2]	AF6	I	IPD	
LENDIAN	AH4	I	IPU	Device Endian pin. 0 = System operates in Big-Endian mode 1 = System operates in Little-Endian mode (default)
MACSEL1[0]	AF5	I	IPD	EMAC1 configuration select pin (for details, see Table 3-1).
MACSEL1[1]	AH5	I	IPD	
DDREN	E20	I	IPD	DDR2 Memory Controller enable 0 = disabled (only use this mode if DDR is not powered) 1 = enabled
RIOEN	U26	I	IPD	RapidIO enable 0 = disabled (only use this mode if RapidIO is not powered) 1 = enabled
HOST EVENT PINS				
HOUT	AH23	O/Z	IPU	Host event output.
GENERAL-PURPOSE INPUT/OUTPUT PINS				
GP00/HPI_EN	M1	I/O/Z	IPD	General-purpose input/output pin 0 multiplexed with HPI internal pulls enable/disable 0 = Internal pulls on HPI IO are enabled and buffers are turned off. 1 = Internal pulls on most HPI IO are disabled and all buffers are turned on. For more detail about internal pull options, see Section 3.3.1.
GP01/UTOPIA_EN	N5	I/O/Z	IPD	General-purpose input/output pin 1 multiplexed with UTOPIA internal pulls enable/disable 0 = Internal pulls on UTOPIA IO are enabled and buffers are turned off. 1 = Internal pulls on UTOPIA IO are disabled and buffers are turned on. For more detail about internal pull options, see Section 3.3.1.
GP02/TSIP0_EN	M3	I/O/Z	IPD	General-purpose input/output pin [4:2] multiplexed with TSIP[2:0] internal pulls enable/disable 0 = Internal pulls on TSIPx IO are enabled and buffers are turned off. 1 = Internal pulls on TSIPx IO are disabled and buffers are turned on. For more detail about internal pull options, see Section 3.3.1.
GP03/TSIP1_EN	K5	I/O/Z	IPD	
GP04/TSIP2_EN	M5	I/O/Z	IPD	
GP05/EMAC1_EN	N4	I/O/Z	IPD	General-purpose input/output pin 5 multiplexed with EMAC1 internal pulls enable/disable 0 = Internal pulls on EMAC1 IO are enabled and buffers are turned off. 1 = Internal pulls on EMAC1 IO are disabled and buffers are turned on. For more detail about internal pull options, see Section 3.3.1.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal
(2) IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)
(3) IPU/IPD logic on some pins can be disabled based on configuration. For more information, see .

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
GP06/BOOTMODE0	L5	I/O/Z	IPU	General-purpose input/output pin [9:6] multiplexed with BOOTMODE selection pin [3:0] (for details, see Table 3-1 and Section 2.4).
GP07/BOOTMODE1	L4	I/O/Z	IPU	
GP08/BOOTMODE2	K3	I/O/Z	IPU	
GP09/BOOTMODE3	K4	I/O/Z	IPU	
GP10/CFGGP0	M2	I/O/Z	IPD	General-purpose input/output pin [14:10] multiplexed with configuration selection pin [4:0].
GP11/CFGGP1	N3	I/O/Z	IPD	
GP12/CFGGP2	M4	I/O/Z	IPD	
GP13/CFGGP3	L1	I/O/Z	IPD	
GP14/CFGGP4	L2	I/O/Z	IPD	
GP15/SYSCLKOUTEN	L3	I/O/Z	IPD	General-purpose input/output pin 15 multiplexed with SYSCLKOUT enable. 0 = SYSCLKOUT is disabled (default) 1 = SYSCLKOUT is enabled
DDR2 MEMORY CONTROLLER				
BSDDQM3	C16	O/Z		DDR2 Memory Controller byte-enable controls • Decoded from the low-order address bits. The number of address bits or byte enables used depends on the width of external memory. • Byte-write enables for most types of memory. • Can be directly connected to SDRAM read and write mask signal (SDQM).
BSDDQM2	B15	O/Z		
BSDDQM1	G4	O/Z		
BSDDQM0	A3	O/Z		
$\overline{\text{BCS1}}$	E9	O/Z		DDR2 Memory Controller memory space enable. When the DDR2 Memory Controller is enabled, it first sets these pins low. Then as accesses occur to the DDR2 memory, only the chip select corresponding to the accessed DDR2 memory is low.
$\overline{\text{BCS0}}$	A4	O/Z		
BBA2	A6	O/Z		DDR2 Memory Controller bank address control
BBA1	B6	O/Z		
BBA0	C7	O/Z		
BEA00	B12	O/Z		DDR2 Memory Controller address bus
BEA01	A12			
BEA02	A11			
BEA03	B11			
BEA04	C11			
BEA05	D11			
BEA06	A9			
BEA07	C10			
BEA08	D10			
BEA09	C9			
BEA10	B8			
BEA11	A7			
BEA12	B7			
BEA13	D9			
BECLKOUTP	C8	O/Z		DDR2 Memory Controller output clock (CLKIN3 frequency × 10) - differential output
BECLKOUTN	D8	O/Z		

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
BED31	B19	I/O/Z		DDR2 Memory Controller data bus
BED30	C18			
BED29	D17			
BED28	B18			
BED27	D16			
BED26	A17			
BED25	D15			
BED24	C15			
BED23	D14			
BED22	A16			
BED21	C14			
BED20	E13			
BED19	B13			
BED18	A15			
BED17	C12			
BED16	A13			
BED15	F2			
BED14	G5			
BED13	D1			
BED12	E2			
BED11	F4			
BED10	F5			
BED09	E4			
BED08	C1			
BED07	E5			
BED06	D3			
BED05	B2			
BED04	C3			
BED03	D5			
BED02	B3			
BED01	C5			
BED00	B4			
$\overline{\text{BSDCAS}}$	D6	O/Z		DDR2 Memory Controller SDRAM column-address strobe
$\overline{\text{BSDRAS}}$	D7	O/Z		DDR2 Memory Controller SDRAM row-address strobe
$\overline{\text{BSDWE}}$	E8	O/Z		DDR2 Memory Controller SDRAM write-enable
BSDCKE	C6	O/Z		DDR2 Memory Controller SDRAM clock-enable (used for self-refresh mode)
BSDDQS3P	C17	I/O/Z		DDR2 Memory Controller data strobe 3 positive/negative
BSDDQS3N	B17	I/O/Z		
BSDDQS2P	D13	I/O/Z		DDR2 Memory Controller data strobe 2 positive/negative
BSDDQS2N	C13	I/O/Z		
BSDDQS1P	E3	I/O/Z		DDR2 Memory Controller data strobe 1 positive/negative
BSDDQS1N	F3	I/O/Z		
BSDDQS0P	D4	I/O/Z		DDR2 Memory Controller data strobe 0 positive/negative
BSDDQS0N	C4	I/O/Z		

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
BSDDQGATE3	E14	I/O/Z		DDR2 Memory Controller data strobe gate [3:0]
BSDDQGATE2	B16	I/O/Z		
BSDDQGATE1	D2	I/O/Z		
BSDDQGATE0	C2	I/O/Z		
RESETS				
$\overline{\text{LRESET}}$	J4	I	IPU	External $\overline{\text{LRESET}}$ input pin to assert/de-assert LRESET to the core specified by CORESEL[2:0] is latched when $\overline{\text{LRESETNMIEN}}$ is rising.
$\overline{\text{NMI}}$	K2	I	IPU	External nonmaskable interrupt input to assert/de-assert $\overline{\text{NMI}}$ to the core specified by CORESEL[2:0] is latched when $\overline{\text{LRESETNMIEN}}$ is rising.
CORESEL0	H3	I	IPU	Core Select input pins used to identify the designated megamodule(s) for $\overline{\text{LRESET}}$ or $\overline{\text{NMI}}$ 000 = C64x+ megamodule 0 001 = C64x+ megamodule 1 010 = C64x+ megamodule 2 011 = C64x+ megamodule 3 100 = C64x+ megamodule 4 101 = C64x+ megamodule 5 110 = Reserved 111 = All C64x+ megamodules
CORESEL1	G3	I	IPU	
CORESEL2	G2	I	IPU	
$\overline{\text{LRESETNMIEN}}$	J3	I	IPU	$\overline{\text{LRESET}}$ and $\overline{\text{NMI}}$ latch enable. The state of the $\overline{\text{LRESET}}$ and $\overline{\text{NMI}}$ inputs is latched to the selected megamodule(s) on the rising edge.
$\overline{\text{RESET}}$	G1	I		Device reset
$\overline{\text{RESETSTAT}}$	J5	O	IPU	Reset status pin. The $\overline{\text{RESETSTAT}}$ output is active (low) when the device is in reset.
BOOTACTIVE	K1	O/Z	IPU	Bootactive indication from the boot controller that boot is active (see Section 3.9.2).
$\overline{\text{POR}}$	H1	I		Power-on reset
PLL				
CLKIN1	K28	I	IPD	Clock input for PLL1 (core clock)
CLKIN2	AH13	I	IPD	Clock input for PLL2 (EMAC clock)
CLKIN3	A23	I	IPD	Clock input for PLL3 (DDR2 clock)
SYSCLKOUT	K27	O/Z	IPU	Clock output (PLL1 output clock/6)
RAPIDIO				
RIOCLKP	U25	I		RapidIO serial port source (reference) clock positive/negative
RIOCLKN	T25			
RIORXP0	P27	I		RapidIO receive port 0 positive/negative (differential)
RIORXN0	N27			
RIORXP1	T29	I		RapidIO receive port 1 positive/negative (differential)
RIORXN1	U29			
RIOTXP0	N29	O		RapidIO transmit port 0 positive/negative (differential)
RIOTXN0	P29			
RIOTXP1	U27	O		RapidIO transmit port 1 positive/negative (differential)
RIOTXN1	T27			
TIMERS				
$\overline{\text{WDOUT}}$	H2	O/Z	IPU	Watchdog timer output (logical combination of six watchdog timers)
TIMI0	V28	I	IPD	Timer input pin
TIMI1	V29	I	IPD	Timer input pin
TIMO2	V27	O/Z	IPD	Timer output pin

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
UNIVERSAL TEST AND OPERATIONS PHY INTERFACE FOR ASYNCHRONOUS TRANSFER MODE (ATM) [UTOPIA]				
URCLK	J29	I	IPD	Source clock for UTOPIA receive driven by Master ATM Controller.
URCLAV	J28	O/Z	IPD	Receive cell available status output signal from UTOPIA Slave. 0 indicates NO space is available to receive a cell from Master ATM Controller. 1 indicates space is available to receive a cell from Master ATM Controller.
URADDR0	Y29	I	IPD	UTOPIA receive address bus
URADDR1	Y28			
URADDR2	Y27			
URADDR3	Y26			
URADDR4	Y25			
URDATA0	AA29	I	IPD	UTOPIA 16-bit receive data bus (also supports 8-bit mode on pins [7:0])
URDATA1	AA28			
URDATA2	AA27			
URDATA3	AB27			
URDATA4	AB26			
URDATA5	AB25			
URDATA6	AC29			
URDATA7	AC28			
URDATA8	AC27			
URDATA9	AC26			
URDATA10	AC25			
URDATA11	AD29			
URDATA12	AD28			
URDATA13	AD27			
URDATA14	AF29			
URDATA15	AD26			
$\overline{\text{URENB}}$	AE27	I	IPU	UTOPIA receive interface enable input signal. Asserted by the Master ATM Controller to indicate to the UTOPIA slave to receive one or more cells on the URDATA bus with URSOC active on the first data cycle.
URSOC	AA25	I	IPD	Receive start-of-cell signal. This signal is output by the Master ATM Controller to indicate to the UTOPIA Slave that the first valid byte of the cell is available to sample on the 16-bit Receive Data Bus (URDATA[15:0]).
UXCLK	J26	I	IPD	Source clock for UTOPIA transmit driven by Master ATM Controller.
UXCLAV	H27	O/Z	IPD	Transmit cell available status output signal from UTOPIA Slave. 0 indicates a complete cell is NOT available for transmit. 1 indicates a complete cell is available for transmit.
UXADDR0	W29	I	IPD	UTOPIA transmit address bus
UXADDR1	W28			
UXADDR2	W27			
UXADDR3	W26			
UXADDR4	W25			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
UXDATA0	G25	O/Z	IPD	UTOPIA 16-bit transmit data bus (also supports 8-bit mode on pins [7:0])
UXDATA1	F26			
UXDATA2	E27			
UXDATA3	H25			
UXDATA4	G26			
UXDATA5	F27			
UXDATA6	E28			
UXDATA7	E29			
UXDATA8	J25			
UXDATA9	H26			
UXDATA10	G27			
UXDATA11	F28			
UXDATA12	G28			
UXDATA13	H28			
UXDATA14	J27			
UXDATA15	H29			
$\overline{\text{UXENB}}$	AA26	I	IPU	UTOPIA transmit interface enable input signal. Asserted by the Master ATM Controller to indicate that the UTOPIA slave should transmit one or more cells on the UXDATA bus with UXSOC active on the first data cycle.
UXSOC	F29	O/Z	IPD	Transmit start-of-cell signal. This signal is output by the UTOPIA Slave on the rising edge of the UXCLK, indicating that the first valid byte of the cell is available on the 16-bit Transmit Data Bus (UXDATA[15:0]).
MANAGEMENT DATA INPUT/OUTPUT (MDIO)				
GMDIO	AH10	I/O/Z	IPU	MDIO serial data input/output. Only active if MACSEL0[2:0] is any value but 011 (RGMII).
GMDCLK	AG9	O/Z	IPU	MDIO serial clock output. Only active if MACSEL0[2:0] is any value but 011 (RGMII).
RGMDIO	AG18	I/O		MDIO serial data input/output. Only active if MACSEL0[2:0] = 011 (RGMII).
RGMDCLK	AF18	O		MDIO serial clock output. Only active if MACSEL0[2:0] = 011 (RGMII).
ETHERNET MAC (EMAC0 and EMAC1) (MII0/GMII0/RMII[1:0]/S3MII[1:0])				
MRXD00/RMRXD00/SRXD0	AH11	I	IPU	EMAC Receive Data 0 (MRXD0) for MII0 [default], GMII0 and RMII0 or Receive Data (RXD) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MRXD01/RMRXD01/SRXSYNC0	AG12	I	IPU	EMAC Receive Data 1 (MRXD1) for MII0 [default], GMII0 and RMII0 or Receive Sync (RXSYNC) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MRXD02/SRXD1	AJ11	I	IPU	EMAC Receive Data 2 (MRXD2) for MII0 [default] and GMII0 or Receive Data (RXD) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXD03/SRXSYNC1	AJ10	I	IPU	EMAC Receive Data 3 (MRXD3) for MII0 [default] and GMII0 or Receive Sync (RXSYNC) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXD04/RMRXD10	AH9	I	IPU	EMAC Receive Data 4 (MRXD4) for GMII0 or Receive Data 0 (RXD0) for RMII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXD05/RMRXD11	AG7	I	IPU	EMAC Receive Data 5 (MRXD5) for GMII0 or Receive Data 1 (RXD1) for RMII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
MRXD06/RMRXER1	AJ13	I	IPU	EMAC Receive Data 6 (MRXD6) for GMII0 or Receive Error (RXER) for RMII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXD07	AJ6	I	IPU	EMAC Receive Data 7 (MRXD7) for GMII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MRCLK0/SRXCLK1	AG10	I	IPU	EMAC Receive Clock (MRCLK) for MII0 [default] and GMII0 or Receive Clock (RXCLK) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXDV0/RMCRSDV1	AE12	I	IPU	EMAC Receive Data Valid (MRDV) for MII0 [default] and GMII0 or Receive Carrier Sense/Data Valid (CRSDV) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MRXER0/RMRXER0/SRXCLK0	AF12	I	IPU	EMAC Receive Error (MRXER) for MII0 [default], GMII0 and RMII0 or Receive Clock (RXCLK) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MCRS0/RMCRSDV0	AF10	I	IPD	EMAC Receive Carrier Sense (MCRS) for MII0 [default] and GMII0 or Receive Carrier Sense/Data Valid (CRSDV) for RMII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
GMTCLK0/REFCLK1/SREFCLK1	AG6	I/O	IPU	EMAC Transmit Clock output (GMTCLK) for GMII0 or Reference clock input (REFCLK) for RMII1 and S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTCLK0/REFCLK0/SREFCLK0	AJ9	I	IPU	EMAC Transmit Clock input (MTCLK) for MII0 [default] and GMII0 or Reference clock input (REFCLK) for RMII0 and S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MTXD00/RMTXD00/STXD0	AF8	O	IPU	EMAC Transmit Data 0 (MTXD0) for MII0 [default], GMII0 and RMII0 or Transmit Data (TXD) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MTXD01/RMTXD01/STXSYNC0	AH7	O	IPU	EMAC Transmit Data 1 (MTXD1) for MII0 [default], GMII0 and RMII0 or Transmit Sync (TXSYNC) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MTXD02/STXD1	AG8	O	IPU	EMAC Transmit Data 2 (MTXD2) for MII0 [default] and GMII0 or Transmit Data (TXD) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTXD03/STXSYNC1	AF9	O	IPU	EMAC Transmit Data 3 (MTXD3) for MII0 [default] and GMII0 or Transmit Sync (TXSYNC) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTXD04/RMTXD10/STXCLK1	AE7	O	IPU	EMAC Transmit Data 4 (MTXD4) for GMII0 or Transmit Data 0 (TXD0) for RMII1 or Transmit Clock (TXCLK) for S3MII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTXD05/RMTXD11	AJ7	O	IPU	EMAC Transmit Data 5 (MTXD5) for GMII0 or Transmit Data 1 (TXD1) for RMII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTXD06/RMTXEN1	AE11	O	IPU	EMAC Transmit Data 6 (MTXD6) for GMII0 or Transmit Enable (TXEN) for RMII1. Pin function defined by MACSEL0[2:0] and MACSEL1[1:0] (see Table 3-1).
MTXD07/STXCLK0	AG11	O	IPU	EMAC Transmit Data 7 (MTXD7) for GMII0 or Transmit Clock (TXCLK) for S3MII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MTXEN0/RMTXEN0	AF11	O	IPU	EMAC Transmit Enable (MTXEN) for MII0 [default], GMII0 and RMII0. Pin function defined by MACSEL0[2:0] (see Table 3-1).
MCOL0	AE8	I	IPD	EMAC Collision (MCOL) for MII0 [default]. Pin function defined by MACSEL0[2:0] (see Table 3-1).

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
ETHERNET MAC (EMAC) (RGMII[1:0])				
RGTXC0	AH19	O		EMAC Transmit Clock (TXC) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGTD00	AE18	O		EMAC Transmit Data bus (TD[3:0]) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGTD01	AG19			
RGTD02	AF17			
RGTD03	AJ19			
RGTXCTL0	AF19	O		EMAC Transmit Control (TXCTL) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGRXC0	AH21	I		EMAC Receive Clock (RXC) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGRD00	AF21	I		EMAC Receive Data bus (RD[3:0]) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGRD01	AG21			
RGRD02	AF20			
RGRD03	AE19			
RGRXCTL0	AJ21	I		EMAC Receive Control (RXCTL) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGCLK0	AG20	O		EMAC Reference Clock (REFCLK) for RGMII0 if enabled by MACSEL0[2:0] (see Table 3-1).
RGTXC1	AH17	O		EMAC Transmit Clock (TXC) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGTD10	AH18	O		EMAC Transmit Data bus (TD[3:0]) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGTD11	AG17			
RGTD12	AE16			
RGTD13	AF16			
RGTXCTL1	AH16	O		EMAC Transmit Control (TXCTL) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGRXC1	AG15	I		EMAC Receive Clock (RXC) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGRD10	AE15	I		EMAC Receive Data bus (RD[3:0]) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGRD11	AF15			
RGRD12	AH15			
RGRD13	AJ15			
RGRXCTL1	AJ16	I		EMAC Receive Control (RXCTL) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
RGCLK1	AG16	O		EMAC Reference Clock (REFCLK) for RGMII1 if enabled by MACSEL1[1:0] (see Table 3-1).
I2C				
SDA	K26	I/O/Z		I2C data. When the I2C module is used, ensure that there is an external pull-up resistor.
SCL	L25	I/O/Z		I2C clock. When the I2C module is used, ensure that there is an external pull-up resistor.

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
JTAG EMULATION/TEST				
TCLK	C27	I	IPU	JTAG test-port clock
TDI	D27	I	IPU	JTAG test-port data in
TDO	C29	O/Z	IPU	JTAG test-port data out
TMS	B28	I	IPU	JTAG test-port mode select
$\overline{\text{TRST}}$	C28	I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG compatibility statement portion of this data sheet.
EMU0	A27	I/O/Z	IPU	Emulation pin 0
EMU1	D29	I/O/Z	IPU	Emulation pin 1
EMU2	D25	I/O/Z	IPU	Emulation pin 2
EMU3	D23	I/O/Z	IPU	Emulation pin 3
EMU4	C24	I/O/Z	IPU	Emulation pin 4
EMU5	C26	I/O/Z	IPU	Emulation pin 5
EMU6	E23	I/O/Z	IPU	Emulation pin 6
EMU7	D22	I/O/Z	IPU	Emulation pin 7
EMU8	D28	I/O/Z	IPU	Emulation pin 8
EMU9	B27	I/O/Z	IPU	Emulation pin 9
EMU10	E22	I/O/Z	IPU	Emulation pin 10
EMU11	E25	I/O/Z	IPU	Emulation pin 11
EMU12	A24	I/O/Z	IPU	Emulation pin 12
EMU13	D24	I/O/Z	IPU	Emulation pin 13
EMU14	C25	I/O/Z	IPU	Emulation pin 14
EMU15	B29	I/O/Z	IPU	Emulation pin 15
EMU16	D26	I/O/Z	IPU	Emulation pin 16
EMU17	E24	I/O/Z	IPU	Emulation pin 17
EMU18	A26	I/O/Z	IPU	Emulation pin 18
TELECOM SERIAL INTERFACE PORT 0 (TSIP0)				
CLKA0	U3	I	IPD	TSIP0 external clock A
CLKB0	R4	I	IPD	TSIP0 external clock B
FSA0	V2	I	IPD	TSIP0 frame sync A
FSB0	Y1	I	IPD	TSIP0 frame sync B
TR00	T3	I	IPD	TSIP0 receive data
TR01	U4			
TR02	AA1			
TR03	V1			
TR04	P5			
TR05	R2			
TR06	R3			
TR07	U1			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
TX00	U2	O/Z	IPD	TSIP0 transmit data
TX01	R5			
TX02	T4			
TX03	P4			
TX04	P2			
TX05	R1			
TX06	P3			
TX07	P1			
TELECOM SERIAL INTERFACE PORT 1 (TSIP1)				
CLKA1	V3	I	IPD	TSIP1 external clock A
CLKB1	AC1	I	IPD	TSIP1 external clock B
FSA1	AF1	I	IPD	TSIP1 frame sync A
FSB1	T5	I	IPD	TSIP1 frame sync B
TR10	AC3	I	IPD	TSIP1 receive data
TR11	AB3			
TR12	Y3			
TR13	W5			
TR14	W4			
TR15	AC2			
TR16	AG2			
TR17	AG1			
TX10	AA3	O/Z	IPD	TSIP1 transmit data
TX11	AF2			
TX12	Y4			
TX13	AD3			
TX14	AH2			
TX15	AD2			
TX16	AD1			
TX17	Y2			
TELECOM SERIAL INTERFACE PORT 2 (TSIP2)				
CLKA2	V4	I	IPD	TSIP2 external clock A
CLKB2	AA2	I	IPD	TSIP2 external clock B
FSA2	W3	I	IPD	TSIP2 frame sync A
FSB2	U5	I	IPD	TSIP2 frame sync B
TR20	AB5	I	IPD	TSIP2 receive data
TR21	AH3			
TR22	AF3			
TR23	AE5			
TR24	AE4			
TR25	AA4			
TR26	AD4			
TR27	AB4			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
TX20	AF4	O/Z	IPD	TSIP2 transmit data
TX21	AA5			
TX22	AD5			
TX23	AC5			
TX24	AC4			
TX25	Y5			
TX26	AE3			
TX27	AG3			
HOST-PORT INTERFACE (HPI16)				
HD00	AG27	I/O/Z	IPD	Host port multiplexed data bus
HD01	AH28			
HD02	AE24			
HD03	AF25			
HD04	AG26			
HD05	AJ28			
HD06	AG25			
HD07	AH26			
HD08	AE22			
HD09	AF23			
HD10	AG24			
HD11	AJ26			
HD12	AH24			
HD13	AG23			
HD14	AJ24			
HD15	AF22			
$\overline{HAS}$	AD25	I	IPU	Host port address strobe
HCNTL0	AF26	I	IPD	Host port control select. Selects between control, address, or data registers.
HCNTL1	AF24	I	IPD	
$\overline{HCS}$	AF28	I	IPU	Host port chip select
$\overline{HDS1}$	AE25	I	IPU	Host port data strobe
$\overline{HDS2}$	AE23	I	IPU	
HHWIL	AG29	I	IPU	Host port half-word select. First or second half-word (not necessarily high or low order).
$\overline{HINT}$	AG28	O/Z	IPU	Host port interrupt from DSP to host
HR/$\overline{W}$	AF27	I	IPU	Host port read or write select
$\overline{HRDY}$	AE26	O/Z	IPU	Host port ready indication
TEST/RESERVED				
RSV01	H5	NC		
RSV02	B20	NC		
RSV07	E21	NC		
RSV08	AG22	NC		
RSV09	AF7	NC		
RSV10	AH6	NC		
RSV11	AJ3	NC		
RSV12	AG4	NC		
RSV13	M28	NC		
RSV14	AE13	NC		

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
RSV15	A20	NC		
RSV16	L29	NC		
RSV17	L28	NC		
RSV18	E19	NC		
RSV19	E18	NC		
RSV20	R26	NC		
RSV21	E26	NC		
RSV22	B24	NC		
RSV23	B23	NC		
RSV24	B9	NC		
RSV25	A8	NC		
SUPPLY VOLTAGE MONITOR PINS				
CV_{DDMON}	AE9			Die-side core supply (CV_{DD}) voltage monitor pin. The monitor pins indicate the voltage on the die and, therefore, provide the best probe point for voltage monitoring purposes. For more information regarding the use of this and other voltage monitoring pins, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* application report (literature number SPRAAQ4). If the CV_{DDMON} pin is not used, it should be connected directly to the die-side core supply (CV_{DD}).
$DV_{DD15MON}$	AG13			Die-side 1.5-/1.8-V I/O supply (DV_{DD15}) voltage monitor pin. The monitor pins indicate the voltage on the die and, therefore, provide the best probe point for voltage monitoring purposes. For more information regarding the use of this and other voltage monitoring pins, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* application report (literature number SPRAAQ4). If the $DV_{DD15MON}$ pin is not used, it should be connected directly to the 1.5-/1.8-V I/O supply (DV_{DD15}). **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, PTV15N, and HHV15EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.
$DV_{DD18MON}$	D12			Die-side 1.8-V I/O supply (DV_{DD18}) voltage monitor pin. The monitor pins indicate the voltage on the die and, therefore, provide the best probe point for voltage monitoring purposes. For more information regarding the use of this and other voltage monitoring pins, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* application report (literature number SPRAAQ4). If the $DV_{DD18MON}$ pin is not used, it should be connected directly to the 1.8-V I/O supply (DV_{DD18}). When DDR is used, connect to DV_{DD18} (1.8V) NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DD3}, AV_{DD4}, CV_{DD1}, PTV18P, PTV18N, and HHV18EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
$DV_{DD33MON}$	V5			Die-side 3.3-V I/O supply (DV_{DD33}) voltage monitor pin. The monitor pins indicate the voltage on the die and, therefore, provide the best probe point for voltage monitoring purposes. For more information regarding the use of this and other voltage monitoring pins, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* application report (literature number SPRAAQ4). If the $DV_{DD33MON}$ pin is not used, it should be connected directly to the 3.3-V I/O supply (DV_{DD33}).

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
PTV PINS				
PTV18P	C20	I		If DDR is used, connect to V_{SS} (GND) via 200-Ω precision resistor NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DD3}, AV_{DD4}, CV_{DD1}, PTV18P, PTV18N, and HHV18EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
PTV18N	C19	I		If DDR is used, connect to DV_{DD18} (1.8 V) via 200-Ω precision resistor NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DD3}, AV_{DD4}, CV_{DD1}, PTV18P, PTV18N, and HHV18EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
PTV15P	AF14	I		If RGMII is used, connect to V_{SS} (GND) via 200-Ω precision resistor NC or connected to V_{SS}, if RGMII is not used **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, PTV15N, and HHV15EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.
PTV15N	AE14	I		If RGMII is used, connect to DV_{DD15} (1.5 V/1.8 V) via 200-Ω precision resistor NC or connected to V_{SS}, if RGMII is not used **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, PTV15N, and HHV15EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
SUPPLY VOLTAGE PINS				
HHV15EN	AF13	I		When RGMII is used, connect to DV_{DD15} (1.5V/1.8V) Connected to V_{SS}, if RGMII is not used **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, PTV15N, and HHV15EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.
HHV18EN	D20	I		When DDR is used, connect to DV_{DD18} (1.8V) Connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DD3}, AV_{DD4}, CV_{DD1}, PTV18P, PTV18N, and HHV18EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
CV_{DD}	AE10	I		1-V (500-MHz device), 1.1-V (625-MHz device), 1.2-V (700-MHz device) supply voltage for core logic
	C21			
	G19			
	G20			
	K15			
	K17			
	K19			
	L10			
	L12			
	L14			
	L16			
	L18			
	L20			
	M11			
	M13			
	M15			
	M17			
	M19			
	N10			
	N12			
	N14			
	N16			
	N18			
	P11			
	P13			
	P15			
	P17			
	R10			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
CV_{DD}	R12	I		1-V (500-MHz device), 1.1-V (625-MHz device), 1.2-V (700-MHz device) supply voltage for core logic
	R14			
	R16			
	R18			
	T11			
	T13			
	T15			
	T17			
	U10			
	U12			
	U14			
	U16			
	U18			
	V11			
	V13			
	V15			
	V17			
	V19			
	V25			
	W10			
	W12			
	W14			
	W16			
	W18			
	W20			
	Y11			
	Y13			
	Y15			
	Y17			
	Y19			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
	A25			
	A28			
	AA24			
	AA6			
	AB2			
	AB7			
	AB23			
	AB28			
	AC6			
	AC8			
	AC10			
	AC12			
	AC22			
	AC24			
	AD11			
	AD13			
	AD23			
	AD7			
DV_{DD33}	AD9	I		3.3-V I/O supply voltage
	AE2			
	AE28			
	AH22			
	AH25			
	AH27			
	AH29			
	AH8			
	AJ1			
	AJ12			
	AJ4			
	B22			
	B26			
	C22			
	C23			
	F21			
	F23			
	F25			
	G22			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
DV_{DD33}	G24	I		3.3-V I/O supply voltage
	H23			
	J2			
	J24			
	K23			
	K25			
	K7			
	L24			
	L6			
	M23			
	M7			
	N2			
	N6			
	P7			
	R6			
	T2			
	T7			
	U6			
	V7			
	W2			
	W24			
	W6			
	Y23			
	Y7			
CV_{DD1}	F7	I		1.2-V supply voltage for DDR EMIF NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DD3}, AV_{DD4}, CV_{DD1}, PTV18P, PTV18N, and HHV18EN pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
	F9			
	F11			
	F13			
	K11			
	K13			
CV_{DD2}	N20	I		1-V (500-MHz device), 1.1-V (625-MHz device), 1.2-V (700-MHz device) supply voltage for SRIO core logic NC or connected to V_{SS}, if RapidIO is not used **NOTE:** If the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to V_{SS} (GND) to reduce power use. However, connecting these pins in this way prevents boundary scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins, see Section 7.3.3.
	P19			
	R20			
	T19			
	U20			
AV_{DDA}	R24	I		1.2-V RapidIO analog supply voltage NC or connected to V_{SS}, if RapidIO is not used Do not connect this SERDES supply to CV_{DD1} **NOTE:** If the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to V_{SS} (GND) to reduce power use. However, connecting these pins in this way prevents boundary scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins, see Section 7.3.3.
	U24			
AV_{DDA1}	M29	I		1.8-V System PLL analog supply voltage
AV_{DDA2}	AG14	I		1.8-V EMAC PLL analog supply voltage

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE(1)	IPD/IPU(2) (3)	DESCRIPTION
AV_{DDA3}	B21	I		1.8-V DDR PLL analog supply voltage NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
AV_{DDA4}	H4 A21	I		1.8-V DDR analog supply voltage NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.
DV_{DDD}	T23 V23	I		1.2-V RapidIO digital supply voltage NC or connected to V_{SS}, if RapidIO is not used Do not connect this SERDES supply to CV_{DD1} **NOTE:** If the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to V_{SS} (GND) to reduce power use. However, connecting these pins in this way prevents boundary scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins, see Section 7.3.3.
DV_{DDR}	R28	I		1.5-V/1.8-V RapidIO regulator supply voltage NC or connected to V_{SS}, if RapidIO is not used **NOTE:** If the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to V_{SS} (GND) to reduce power use. However, connecting these pins in this way prevents boundary scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins, see Section 7.3.3.
DV_{DD18}	A1 A19 B10 B14 B5 E1 E12 E16 E6 F15 F17 F19 G10 G12 G14 G16 G18 G6 G8 H7 J6	I		1.8-V I/O supply voltage for DDR2 buffers NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
AV_{DDT}	N25 R25	I		1.2-V RapidIO termination supply voltage NC or connected to V_{SS}, if RapidIO is not used Do not connect this SERDES supply to CV_{DD1} **NOTE:** If the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to V_{SS} (GND) to reduce power use. However, connecting these pins in this way prevents boundary scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins, see Section 7.3.3.
DV_{DD15}	AC14 AC16 AC18 AC20 AD15 AD17 AD19 AD21 AH14 AH20 AJ18	I		1.5-V/1.8-V supply voltage for RGMII HSTL buffers NC or connected to V_{SS}, if RGMII is not used **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, and PTV15N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.
$V_{REFHSTL}$	AE17	I		0.75-V/0.9-V DV_{DD15} reference supply voltage NC or connected to V_{SS}, if RGMII is not used **NOTE:** If the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, and PTV15N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins in this way will prevent boundary-scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins, see Section 7.3.3.
$V_{REFSSTL}$	E10	I		DDR 0.9-V $V_{REFSSTL}$ reference supply voltage NC or connected to V_{SS}, if DDR is not used **NOTE:** If the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N pins can be NC or connected directly to V_{SS} (GND) to save power. However, connecting these pins this way prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins, see Section 7.3.3.

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
GROUND PINS				
V_{SS}	A10	GND		Ground pins
	A14			
	A18			
	A2			
	A22			
	A29			
	A5			
	AA23			
	AA7			
	AB1			
	AB6			
	AB24			
	AB29			
	AC7			
	AC9			
	AC11			
	AC13			
	AC15			
	AC17			
	AC19			
	AC21			
	AC23			
	AD10			
	AD12			
	AD14			
	AD16			
	AD18			
	AD20			
	AD22			
	AD24			
	AD6			
	AD8			
	AE1			
	AE20			
	AE21			
	AE29			
	AH1			
	AH12			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
V_{SS}	AJ14	GND		Ground pins
	AJ17			
	AJ2			
	AJ20			
	AJ22			
	AJ23			
	AJ25			
	AJ27			
	AJ29			
	AJ5			
	AJ8			
	B1			
	B25			
	D18			
	D19			
	D21			
	E11			
	E15			
	E17			
	E7			
	F1			
	F10			
	F12			
	F14			
	F16			
	F18			
	F20			
	F22			
	F24			
	F6			
	F8			
	G11			
	G13			
	G15			
	G17			
	G21			
	G23			
	G29			
	G7			
	G9			
	H24			
	H6			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
V_{SS}	J1	GND		Ground pins
	J23			
	J7			
	K10			
	K12			
	K14			
	K16			
	K18			
	K20			
	K24			
	K29			
	K6			
	L7			
	L11			
	L13			
	L15			
	L17			
	L19			
	L23			
	L26			
	L27			
	M10			
	M12			
	M14			
	M16			
	M18			
	M20			
	M24			
	M25			
	M26			
	M27			
	M6			
	N1			
	N11			
	N13			
	N15			
	N17			
	N19			
	N23			
	N24			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
V_{SS}	N26	GND		Ground pins
	N28			
	N7			
	P10			
	P12			
	P14			
	P16			
	P18			
	P20			
	P23			
	P24			
	P25			
	P26			
	P28			
	P6			
	R11			
	R13			
	R15			
	R17			
	R19			
	R23			
	R27			
	R29			
	R7			
	T1			
	T10			
	T12			
	T14			
	T16			
	T18			
	T20			
	T24			
	T26			
	T28			
	T6			
	U11			
	U13			

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Table 2-5. Terminal Functions (continued)

SIGNAL NAME	NO.	TYPE[1]	IPD/IPU[2] [3]	DESCRIPTION
V_{SS}	U15	GND		Ground pins
	U17			
	U19			
	U23			
	U28			
	U7			
	V10			
	V12			
	V14			
	V16			
	V18			
	V20			
	V24			
	V26			
	V6			
	W1			
	W11			
	W13			
	W15			
	W17			
	W19			
	W23			
	W7			
	Y10			
	Y12			
	Y14			
	Y16			
	Y18			
	Y20			
	Y24			
	Y6			

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2.8 Development

2.8.1 Development Support

For customers that will develop their own features and software on the C6472 device, TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of C6000™ DSP-based applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE) including Editor, C/C++/Assembly Code Generation, and Debug plus additional development tools scalable Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools: Extended Development System (XDS™) Emulators (support C6000/C64x+ DSP multiprocessor system debug) and Evaluation Module (EVM).

2.8.2 Device Support

2.8.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMX**320C6472CTZ). Texas Instruments recommends one of two prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device has been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

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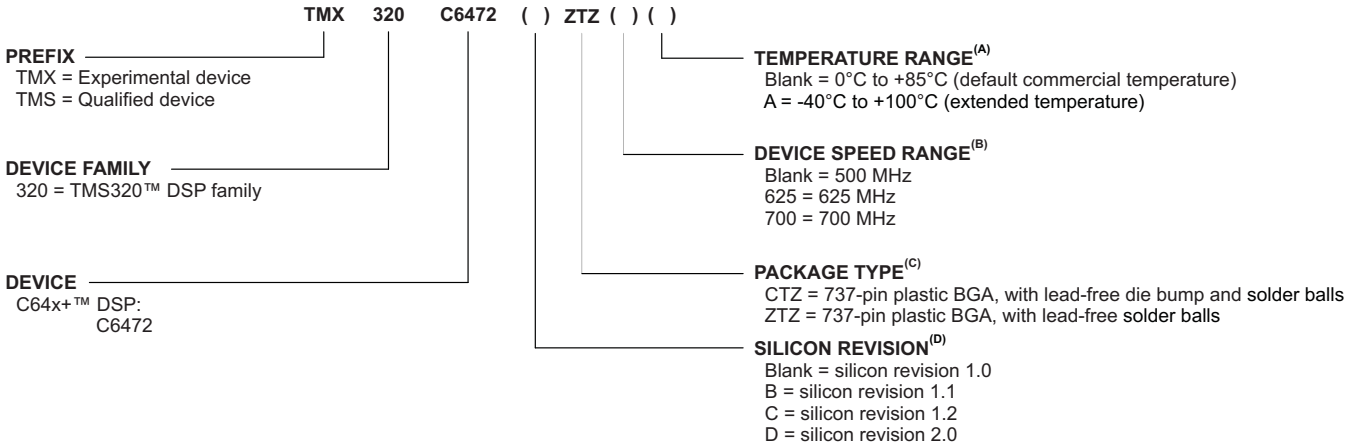
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, CTZ), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, blank is 500 MHz). Figure 2-13 provides a legend for reading the complete device name for any TMS320C64x+™ DSP generation member.

For a complete list of all valid device part numbers and further ordering information for TMS320C6472 in the CTZ and ZTZ package types, see online ordering at www.ti.com or contact your TI sales representative. For specific references to package symbolization as well as device errata and advisories, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).



A. A (extended temperature) temperature range is available only on 500-MHz and 625-MHz devices.
B. Device Speed Range marking is placed in upper right hand corner of device.
C. BGA = Ball Grid Array
D. Silicon revision correlates to the lot trace code found on the second line of the package marking. For more information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).

Figure 2-13. TMS320C64x+™ DSP Device Nomenclature (including the TMS320C6472 DSP)

2.8.2.2 Documentation Support

The following documents describe the TMS320C6472 Fixed-Point Digital Signal Processor. Copies of these documents are available on the Internet at www.ti.com. *Tip*: Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the TMS320C6472, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

User's Guides/Reference Manuals:

SPRZ300 ***TMS320C6472 Digital Signal Processor Silicon Errata.*** This document describes the silicon updates to the functional specifications for the TMS320C6472 digital signal processor.

SPRU732 ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

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SPRU862 ***TMS320C64x+ DSP Cache User's Guide.*** Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C64x+ digital signal processor (DSP) of the TMS320C6000 DSP family can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C64x+ DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

SPRU395 ***TMS320C64x Technical Overview.*** Provides an introduction to the TMS320C64x digital signal processors (DSPs) of the TMS320C6000 DSP family.

SPRU198 ***TMS320C6000 Programmer's Guide.*** Reference for programming the TMS320C6000 digital signal processors (DSPs). Before you use this manual, you should install your code generation and debugging tools. Includes a brief description of the C6000 DSP architecture and code development flow, includes C code examples and discusses optimization methods for the C code, describes the structure of assembly code and includes examples and discusses optimizations for the assembly code, and describes programming considerations for the C64x DSP.

SPRUEC6 ***TMS320C645x/C647x Bootloader User's Guide.*** This document describes the features of the on-chip bootloader provided with the TMS320C645x/C647x Digital Signal Processors (DSPs).

SPRU806 ***TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide.*** This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C6472/TMS320TCI648x digital signal processors (DSPs). The PLL controller offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the C6472/TCI648x DSP core, peripherals, and other modules inside the C6472/TCI648x DSP.

SPRUEG1 ***TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide.*** This guide describes the host port interface (HPI) on the TMS320C6472/TMS320TCI6486 digital signal processors (DSPs). The HPI enables an external host processor (host) to directly access the internal or external memory of the DSP using a 16-bit (HPI16) interface.

SPRUEG4 ***TMS320C6472/TMS320TCI6486 DSP Telecom Serial Interface Port (TSIP) User's Guide.*** This document describes the operation of the TMS320C6472/TMS320TCI6486 DSP Telecom Serial Interface Port (TSIP).

SPRU725 ***TMS320C6472/TMS320TCI648x DSP General-Purpose Input/Output (GPIO) User's Guide.*** This document describes the general-purpose input/output (GPIO) peripheral in the digital signal processors (DSPs) of the TMS320C6472/TMS320TCI648x DSP family.

SPRU818 ***TMS320C6472/TMS320TCI648x DSP 64-Bit Timer User's Guide.*** This document provides an overview of the 64-bit timer in the TMS320C6472/TMS320TCI648x DSP. The timer can be configured as a general-purpose 64-bit timer, dual general-purpose 32-bit timers, or a watchdog timer.

SPRU727 ***TMS320C6472/TMS320TCI648x DSP Enhanced DMA (EDMA3) Controller User's Guide.*** This document describes the Enhanced DMA (EDMA3) Controller in the TMS320C6472/TMS320TCI648x DSP.

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SPRUE11 ***TMS320C6472/TMS320TCI648x DSP Inter-Integrated Circuit (I2C) Module User's Guide.*** This document describes the inter-integrated circuit (I2C) module in the TMS320C6472/TMS320TCI648x Digital Signal Processor (DSP). The I2C provides an interface between the C6472/TCI648x device and other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEF8 ***TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide.*** This document provides a functional description of the Ethernet Media Access Controller (EMAC) and Physical layer (PHY) device Management Data Input/Output (MDIO) module integrated with TMS320C6472/TMS320TCI6486 DSPs.

SPRUEG2 ***TMS320C6472/TMS320TCI6486 DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2) User's Guide.*** This document describes the universal test and operations PHY interface for asynchronous transfer mode (ATM) 2 (UTOPIA2) in the TMS320C6472/TMS320TCI6486 digital signal processors (DSPs).

SPRUE13 ***TMS320C6472/TMS320TCI648x Serial RapidIO (SRIO) User's Guide.*** This document describes the Serial RapidIO (SRIO) on the TMS320C6472/TMS320TCI648x DSPs.

SPRU894 ***TMS320C6472/TMS320TCI648x DSP DDR2 Memory Controller User's Guide.*** This document describes the DDR2 memory controller in the TMS320C6472/TMS320TCI648x digital-signal processors (DSPs).

SPRU889 ***High-Speed DSP Systems Design Reference Guide.*** Provides recommendations for meeting the many challenges of high-speed DSP system design. These recommendations include information about DSP audio, video, and communications systems for the C5000 and C6000 DSP platforms.

SPRU655 ***Emulation and Trace Headers Technical Reference Manual.*** Describes how to incorporate Texas Instruments next-generation emulation header on a board with a TMS320C55x or TMS320C64x DSP with advanced emulation features, such as HS RTDX.

SPRU589 ***XDS560 Emulator Technical Reference.*** This technical reference describes the fundamentals of XDS560 Emulator and Pod and how to interface it to a target system. It also provides guidelines for implementing 14-pin emulation on the target design.

SPRU187 ***TMS320C6000 Optimizing Compiler User's Guide.*** Describes the TMS320C6000 C compiler and the assembly optimizer. This C compiler accepts ANSI standard C source code and produces assembly language source code for the TMS320C6000 platform of devices (including the C64x+ and C67x+ generations). The assembly optimizer helps you optimize your assembly code.

SPRU186 ***TMS320C6000 Assembly Language Tools User's Guide.*** Describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C6000 platform of devices (including the C64x+ and C67x+ generations).

SPRUEC5 ***TMS320C64x+ DSP Big-Endian DSP Library Programmer's Reference.*** This document describes the C64x+ digital signal processor big-endian (DSP) Library.

SPRUEB8 ***TMS320C64x+ DSP Little-Endian DSP Library Programmer's Reference.*** This document describes the C64x+ digital signal processor little-endian (DSP) Library, or DSPLIB for short.

SPRUEG3 ***TMS320C6472/TMS320TCI6486 PSC User's Guide.*** This document describes the power sleep controller (PSC) in the TMS320TCI6486 DSP.

SPRUEG5 ***TMS320C6472/TMS320TCI6486 Shared-Memory Controller User's Guide.*** This document describes the shared-memory controller (SMC) for the TMS320TCI6486 DSP.

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Application Reports:

SPRAA84 ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRAAQ4 ***TMS320C6472/TMS320TCI6486 Hardware Design Guide.*** This application report describes system design considerations for the TMS320C6472/TMS320TCI6486 digital signal processor (DSP).

SPRAAT9 ***TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines.*** This application report contains implementation instructions for the Serial RapidIO (SRIO) interface on the TMS320C6472/TMS320TCI6486 DSP.

SPRAAT7 ***TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines.*** This application report contains implementation instructions for the DDR2 interface contained on the TMS320C6472/TMS320TCI6486 DSP.

SPRAAU2 ***TMS320C6472/TMS320TCI6486 EMAC Implementation Guide.*** This application report contains implementation instructions for the Ethernet interface contained on the TMS320C6472/TMS320TCI6486 DSP.

SPRAAS4 ***TMS320C6472/TMS320TCI6486 Power Consumption Summary.*** This application report discusses the power consumption of the TMS320C6472/TMS320TCI6486 digital signal processor (DSP).

SPRAAY0 ***TMS320C6472/TMS320TCI6486 Throughput.*** This application report provides designers a basis for estimating memory access performance based on throughput measurements under various operating conditions. Some factors affecting memory access performance are discussed. It also addresses throughput to/from the interfaces to memories of the C6472/TCI6486 device. This can be used to estimate transport performance of the C6472/TCI6486 device to facilitate system design.

SPRA839 ***Using IBIS Models for Timing Analysis.*** Describes how to properly use IBIS models to attain accurate timing analysis for a given system.

SPRA753 ***Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs.*** Advanced Event Triggering (AET) provides a way to examine the system while it is in operation, and to trigger conditional events with no overhead. This document describes how to use these powerful tools to debug a system.

SPRA387 ***Using Advanced Event Triggering to Debug Real-Time Problems in High-Speed Embedded Microprocessor Systems.*** This application report instructs the user on how to take advantage of the advanced event triggering (AET) embedded components available on TI's new digital signal processors.

SPRM384 ***TMS320C6472 BSDL Model.***

SLVR307 ***TNETV3020/TCI6486 Power Reference Design.***

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2.9 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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3 Device Configuration

On the C6472 device, boot mode and certain device configurations/peripheral selections are determined at device reset. Following device reset, the software needs to enable and configure the desired peripheral modules.

3.1 Device Configuration at Device Reset

Table 3-1 describes the C6472 device configuration pins. The logic level of these pins is latched at reset to determine the device configuration. The logic level on the device configuration pins can be set by using external pullup/pulldown resistors or by using some control device (e.g., FPGA/CPLD) to intelligently drive these pins. When using a control device, care should be taken to ensure there is no contention on the lines when the device is out of reset. The RESETSTAT pin can be monitored for this purpose. The device configuration pins are sampled during reset and may be driven after the reset is removed. At this time, the control device should ensure it has stopped driving the device configuration pins of the DSP to avoid contention.

Table 3-1. C6472 Device Configuration Pins

CONFIGURATION PIN	NO.	IPD/ IPU(1)	FUNCTIONAL DESCRIPTION
GP[9:6]_BOOTMODE[3:0]		IPU	For more detailed information on the boot modes, see Section 2.4, *Boot Mode Sequence*, of this document.
GP[14:10]_CFGGP[4:0]		IPD	Configuration GPI (General-Purpose Inputs for Configuration purposes CFGGP[4:0]) These pins are used in S/W routines located in internal ROM for boot operations. For more detailed information on the use of the configuration pins for boot operation, see Section 2.4, *Boot Mode Sequence*, of this document.
GP[15]_SYSCLKOUTEN		IPD	Enable SYSCLKOUT 0 - SYSCLKOUT is disabled (default) 1 - SYSCLKOUT is enabled
MACSEL1[1:0]		IPD	EMAC Interface selection for EMAC 1 (EMAC1_EN in the DEVCTL register must be a 1 for these to be functional) 00 - Reserved 01 - SS-SMII (SS Mode) 10 - RGMII 11 - RMII
MACSEL0[2:0]		IPD	EMAC Interface selection for EMAC 0 000 - MII 001 - RMII 010 - GMII 011 - RGMII 100 - Reserved 101 - SS-SMII (SS Mode) 110 - Reserved 111 - Disabled
LENDIAN		IPU	Device Endian mode (LENDIAN) 0 - System operates in Big Endian mode 1 - System operates in Little Endian mode (default)
DDREN		IPD	DDR2 Memory Controller enable (DDR2_EN) 0 - DDR2 Memory Controller module and pins are disabled (default) 1 - DDR2 Memory Controller module and pins are enabled Note that this is a static configuration input from reset.
RIOEN		IPD	RIOEN RapidIO enable 0 - RapidIO module and pins are disabled (default) 1 - RapidIO module and pins are enabled Note that this is a static configuration input from reset.

(1) IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

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3.1.1 Debugging Considerations

It is recommended that external connections be provided to device configuration pins, including all GPIO, MACSEL, DDREN, and RIOEN pins. Although internal pullup/pulldown resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes. It also improves noise immunity for critical mode control inputs.

For the internal pullup/pulldown resistors for all device pins, see Table 2-5, *Terminal Functions*.

3.2 Device Configuration Register Descriptions

Table 3-2 is a summary of the primary chip-level registers that are discussed in Section 3.3 through Section 3.11.

Table 3-2. Device Configuration Registers (Chip-Level Registers)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
02A8 0000	DEVSTAT	Device Status Register	Provides status of the user's device configuration on reset.
02A8 0004	PRI_ALLOC	Priority Allocation Register	Sets DMA access priorities for master peripherals.
02A8 0008	DEVICE_ID	Device ID Register	Identifies the device.
02A8 000C - 02A8 01FC	-	Reserved	
02A8 0200	DEVCTL	Device Control Register	Controls the internal pulls on I/O interfaces.
02A8 0204	DEVCTL_KEY	Device Control Key Register	This key register controls the writes to DEVCTL register. Key value is 0A1E 183Ah.
02A8 0208	RMIIRESET0	RMII0 Reset Register	Provides reset to RMII. Used when changing speed or duplex setting.
02A8 020C	RMIIRESET1	RMII1 Reset Register	
02A8 0210 - 02A8 0408	-	Reserved	
02A8 040C	HOSTPRIV	Host Memory Privilege Register	This register configures privilege modes.
02A8 0410 - 02A8 0418	-	Reserved	
02A8 041C	PRIVPERM	Memory Privilege Permission Register	This register overrides the memory protection for leaf node in the CFG SCR.
02A8 0420	PRIVKEY	Memory Privilege Key Register	This register is used for key based protection of HOSTPRIV and PRIVPERM to control the changes in the permission levels.
02A8 0424 - 02A8 04FC	-	Reserved	
02A8 0500	NMIGR0	NMI Generation Registers	NMIGRx register creates NMI event to C64x+ Megamodulex
02A8 0504	NMIGR1		
02A8 0508	NMIGR2		
02A8 050C	NMIGR3		
02A8 0510	NMIGR4		
02A8 0514	NMIGR5		
02A8 0518 - 02A8 053C	-	Reserved	
02A8 0540	IPCGR0	IPC Generation Registers	IPCGRx register generates an interrupt pulse to C64x+ Megamodulex.
02A8 0544	IPCGR1		
02A8 0548	IPCGR2		
02A8 054C	IPCGR3		
02A8 0550	IPCGR4		
02A8 0554	IPCGR5		
02A8 0558 - 02A8 0578	-	Reserved	

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Table 3-2. Device Configuration Registers (Chip-Level Registers) (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
02A8 057C	IPCGR15 or IPCGRH	Host Interrupt Pulse Generation Register	IPCGRH register generates an interrupt pulse to host.
02A8 0580	IPCAR0	IPC Acknowledgment Registers	IPCARx register acknowledges an interrupt pulse to C64x+ Megamodulex.
02A8 0584	IPCAR1		
02A8 0588	IPCAR2		
02A8 058C	IPCAR3		
02A8 0590	IPCAR4		
02A8 0594	IPCAR5		
02A8 0598 - 02A8 05B8	-	Reserved	
02A8 05BC	IPCAR15 or IPCARH	Host Interrupt pulse Acknowledgment Register	IPCARH register acknowledges an interrupt pulse to host.
02A8 05C0 - 02A8 06FC	-	Reserved	
02A8 0700		MAC ID	
02A8 0708 - 02A8 0710	-	Reserved	
02A8 0714	TPMGR	Timer Pin Manager Register	TPMGR register configures the timer pin manager block.
02A8 0718	RSTMUX0	Reset Mux Registers	These registers decide the actions taken upon receiving a timer event/watchdog reset event.
02A8 071C	RSTMUX1		
02A8 0720	RSTMUX2		
02A8 0724	RSTMUX3		
02A8 0728	RSTMUX4		
02A8 072C	RSTMUX5		

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Table 3-2. Device Configuration Registers (Chip-Level Registers) (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
BOOT CONTROLLER REGISTERS			
02AB 0000	RESET_STAT	Reset Status	This register tells the status of the local reset for all 6 C64x+ megamodules.
02AB 0004	BOOT_COMPLETE_STAT	Boot Complete Status Register	signals the Boot Completion process to Boot Controller
02AB 0008	BOOTPROGRESS	Boot Progress Register	This register tracks the progress of the boot sequence
02AB 000C - 02AB 01FC	-	Reserved	
02AB 0200	BOOTMODE0	Boot Mode 0 Register	Sets the local boot option for C64x+ Megamodule0.
02AB 0204	DSP_BOOT_ADDR0	DSP Boot Address Register 0	Boot address for C64x+ Megamodule0.
02AB 0208 - 02AB 021C	-	Reserved	
02AB 0220	BOOTMODE1	Boot Mode 1 Register	Sets the local boot option for C64x+ Megamodule1.
02AB 0224	DSP_BOOT_ADDR1	DSP Boot Address Register 1	Boot address for C64x+ Megamodule1.
02AB 0228 - 02AB 023C	-	Reserved	
02AB 0240	BOOTMODE2	Boot Mode 2 Register	Sets the local boot option for C64x+ Megamodule2.
02AB 0244	DSP_BOOT_ADDR2	DSP Boot Address Register 2	Boot address for C64x+ Megamodule2.
02AB 0248 - 02AB 025C	-	Reserved	
02AB 0260	BOOTMODE3	Boot Mode 3 Register	Sets the local boot option for C64x+ Megamodule3.
02AB 0264	DSP_BOOT_ADDR3	DSP Boot Address Register 3	Boot address for C64x+ Megamodule3.
02AB 0268 - 02AB 027C	-	Reserved	
02AB 0280	BOOTMODE4	Boot Mode 4 Register	Sets the local boot option for C64x+ Megamodule4.
02AB 0284	DSP_BOOT_ADDR4	DSP Boot Address Register 4	Boot address for C64x+ Megamodule4.
02AB 0288 - 02AB 029C	-	Reserved	
02AB 02A0	BOOTMODE5	Boot Mode 5 Register	Sets the local boot option for C64x+ Megamodule5.
02AB 02A4	DSP_BOOT_ADDR5	DSP Boot Address Register 5	Boot address for C64x+ Megamodule5.
02AB 02A8 - 02AB 7FFC	-	Reserved	

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3.3 Peripheral Selection After Device Reset

3.3.1 Controlling Internal Pulls on the Peripherals

3.3.1.1 Device Control Register (DEVCTL)

The device control register (DEVCTL) controls the internal pulls on the I/O interfaces. The bits are initialized on the rising edge of the Power-On Reset from the GPIO pins [5:0], then software can override these latched values. When the DSP is out of reset, the DEVCTL bits control the pullup and pulldown resistors. When the DSP is held in reset, the GPIO pins enable the pullup and pulldown resistors, directly. These bits also enable or disable the output buffers on these interfaces. When the pull-up or pull-down resistors are enabled, the output buffers are disabled. When not in use, all the inputs should be in a known state (i.e., needs to be internally pulled) and the corresponding I/O buffers should be powered down to save I/O power. The DEVCTL register is shown in Figure 3-1 and described in Table 3-3.

Section 3.3.1.3 contains more detail about the operation of the internal resistor pulls and the output buffer operation. It explicitly lists the relevant pins individually under all possible configurations and states whether the output buffers are enabled or disabled and whether the internal pull resistors are enabled or disabled.

31	16
Reserved	
R-0000 0000	

15	13	12	11	9	8
Reserved		EMAC1_EN	TSIP2_EN[2:0]		TSIP1_EN2
R/W-0		R/W-x	R/W-xxx		R/W-xxx

7	6	5	3	2	1	0
TSIP1_EN[1:0]		TSIP0_EN[2:0]		UTOPIA_EN[1:0]		HPI_EN
R/W-xxx		R/W-xxx		R/W-xx		R/W-x

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-1. Device Control Register (DEVCTL)

Table 3-3. Device Control Register (DEVCTL) Field Descriptions

Bit	Field	Value	Description
31:13	Reserved		Reserved
12	EMAC1_EN		EMAC1 Internal Pulls Enable. Initialized at reset from GP05/EMAC1_EN pin.
		0	Enable the pulls on the 3.3-V EMAC1 I/O pins and power down the corresponding I/O buffers. Also disable the EMAC1 RGMII I/O pins.
		1	Allow the pulls on the 3.3-V EMAC1 I/O to be disabled and the corresponding I/O buffers to be powered up. Also allow the RGMII I/O buffers to be powered up. This input is combined with the MACSEL1[1:0] configuration inputs to determine which I/O pins are enabled and which are disabled. All disabled 3.3-V I/O pins will have internal pulls active.
11	TSIP2_EN[2]		TSIP2 Internal Pulls Enable[2]. Initialized at reset from GP04/TSIP2_EN pin.
		0	Enable the pulls on TX[7:4] and TR[7:4] of the TSIP2 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[7:4] and TR[7:4] of the TSIP2 I/O pins and power up the corresponding I/O buffers.
10	TSIP2_EN[1]		TSIP2 Internal Pulls Enable[1]. Initialized at reset from GP04/TSIP2_EN pin.
		0	Enable the pulls on TX[3:2] and TR[3:2] of the TSIP2 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[3:2] and TR[3:2] of the TSIP2 I/O pins and power up the corresponding I/O buffers.

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Table 3-3. Device Control Register (DEVCTL) Field Descriptions (continued)

Bit	Field	Value	Description
9	TSIP2_EN[0]		TSIP2 Internal Pulls Enable[0]. Initialized at reset from GP04/TSIP2_EN pin.
		0	Enable the pulls on all TSIP2 I/O pins and power down the I/O buffers. When this bit is low, the values of TSIP2_EN[2:1] = don't care.
		1	Disable the pulls on CLKA, CLKB, FSA, FSB, TX[1:0], and TR[1:0] of the TSIP2 I/O pins and power up the corresponding I/O buffers.
8	TSIP1_EN[2]		TSIP1 Internal Pulls Enable[2]. Initialized at reset from GP03/TSIP1_EN pin.
		0	Enable the pulls on TX[7:4] and TR[7:4] of the TSIP1 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[7:4] and TR[7:4] of the TSIP1 I/O pins and power up the corresponding I/O buffers.
7	TSIP1_EN[1]		TSIP1 Internal Pulls Enable[1]. Initialized at reset from GP03/TSIP1_EN pin.
		0	Enable the pulls on TX[3:2] and TR[3:2] of the TSIP1 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[3:2] and TR[3:2] of the TSIP1 I/O pins and power up the corresponding I/O buffers.
6	TSIP1_EN[0]		TSIP1 Internal Pulls Enable[0]. Initialized at reset from GP03/TSIP1_EN pin.
		0	Enable the pulls on all TSIP1 I/O pins and power down the I/O buffers. When this bit is low, the values of TSIP1_EN[2:1] = don't care.
		1	Disable the pulls on CLKA, CLKB, FSA, FSB, TX[1:0], and TR[1:0] of the TSIP1 I/O pins and power up the corresponding I/O buffers.
5	TSIP0_EN[2]		TSIP0 Internal Pulls Enable[2]. Initialized at reset from GP02/TSIP0_EN pin.
		0	Enable the pulls on TX[7:4] and TR[7:4] of the TSIP0 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[7:4] and TR[7:4] of the TSIP0 I/O pins and power up the corresponding I/O buffers.
4	TSIP0_EN[1]		TSIP0 Internal Pulls Enable[1]. Initialized at reset from GP02/TSIP0_EN pin.
		0	Enable the pulls on TX[3:2] and TR[3:2] of the TSIP0 I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on TX[3:2] and TR[3:2] of the TSIP0 I/O pins and power up the corresponding I/O buffers.
3	TSIP0_EN[0]		TSIP0 Internal Pulls Enable[0]. Initialized at reset from GP02/TSIP0_EN pin.
		0	Enable the pulls on all TSIP0 I/O pins and power down the I/O buffers. When this bit is low, the values of TSIP0_EN[2:1] = don't care.
		1	Disable the pulls on the clock inputs and control inputs and outputs of the UTOPIA I/O pins and power up the corresponding I/O buffers.
2	UTOPIA_EN[1]		UTOPIA Internal Pulls Enable[1]. Initialized at reset from GP01/UTOPIA_EN pin.
		0	Enable the pulls on UXDATA[15:8] and URDATA[15:8] of the UTOPIA I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on UXDATA[15:8] and URDATA[15:8] of the UTOPIA I/O pins and power up the corresponding I/O buffers.
1	UTOPIA_EN[0]		UTOPIA Internal Pulls Enable [0]. Initialized at reset from GP01/UTOPIA_EN pin.
		0	Enable the pulls on all UTOPIA I/O pins and power down the I/O buffers. When this bit is low, the value of UTOPIA_EN[1] = don't care.
		1	Disable the pulls on the UTOPIA clock inputs, control inputs and outputs, UXDATA[7:0], and URDATA[7:0] and power up the corresponding I/O buffers.
0	HPI_EN		HPI Internal Pulls Enable. Initialized at reset from GP01/UTOPIA_EN pin.
		0	Enable the pulls on the HPI I/O pins and power down the corresponding I/O buffers.
		1	Disable the pulls on all HPI I/O pins except $\overline{\text{HAS}}$, $\overline{\text{HCS}}$, and $\overline{\text{HINT}}$ and power up all HPI I/O buffers.

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3.3.1.2 Device Control Key Register (DEVCTL_KEY)

The device control key register (DEVCTL_KEY) protects against inadvertently updating the DEVCTL register with errant software. The DEVCTL_KEY register is shown in Figure 3-2.

31	0
KEY	
R/W-0000 0000 0000 0000	

LEGEND: R/W = Read/Write; *-n* = value after reset

Figure 3-2. Device Control Key Register (DEVCTL_KEY)

To update/write the DEVCTL register:

1. When the *correct* key value (KEY = 0A1E 183Ah) is written to the DEVCTL_KEY register, the DEVCTL register becomes amenable for a single write anytime after this.
2. Once the DEVCTL register is written, no further writes to the DEVCTL register are allowed without repeating Step 1.

The software should disable all the interrupts during the update of the DEVCTL register.

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3.3.1.3 IPU/IPD Control

This section augments Table 3-3 in Section 3.3.1.1. It contains more detail about the operation of the internal resistor pulls and the output buffer operation. It explicitly lists the relevant pins individually under all possible configurations and states whether internal pull resistors are enabled or disabled. The 3.3-V EMAC0 and EMAC1 pins are listed in Table 3-4, the HPI pins are listed in Table 3-5, the TSIP pins are listed in Table 3-6, Table 3-7, Table 3-8 and the UTOPIA pins are listed in Table 3-9.

Use the following legend for Table 3-4 through Table 3-9:

- EN = Internal pull-up or pull-down resistors are enabled and output buffers are disabled.
- DIS = Internal pull-up or pull-down resistors are disabled and output buffers are enabled.

This is true for all cases except for three HPI control signals ($\overline{\text{HAS}}$, $\overline{\text{HCS}}$, and $\overline{\text{HINT}}$) that always have their internal pull resistors activated (see Table 3-5).

Table 3-4. EMAC IPU/IPD Control(1)(2)

SIGNAL NAME	EMAC0 AS SPECIFIED BY MACSEL0[2:0]													
	MII	GMII	RMII	S3MII	RGMII	Disabled	RMII	S3MII	RGMII	Disabled	RMII	S3MII	RGMII	Disabled
	EMAC1 AS SPECIFIED BY EMAC1_EN AND MACSEL1[1:0]													
	RGMII or Disabled	RGMII or Disabled	RGMII or Disabled	RGMII or Disabled	RGMII or Disabled	RGMII or Disabled	RMII	RMII	RMII	RMII	S3MII	S3MII	S3MII	S3MII
MRXD00/RMRXD00/ SRXD0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MRXD01/RMRXD01/ SRXSYNC0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MRXD02/SRXD1	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	DIS	DIS	DIS	DIS
MRCLK0/SRXCLK1	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	DIS	DIS	DIS	DIS
MRXD03/SRXSYNC1	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	DIS	DIS	DIS	DIS
MRXD04/RMRXD10	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MRXD05/RMRXD11	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MRXD06/RMRXER1	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MRXD07	EN	DIS	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN
MRXDV0/RMCRSDV1	DIS	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MRXER0/RMRXER0/ SRXCLK0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MCRS0/RMCRSDV0	DIS	DIS	DIS	EN	EN	EN	DIS	EN	EN	EN	DIS	EN	EN	EN
GMTCLK0/REFCLK1/ SREFCLK1	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	DIS	DIS	DIS	DIS
MTCLK0/REFCLK0/ SREFCLK0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MTXD00/RMTXD00/ STXD0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MTXD01/RMTXD01/ STXSYNC0	DIS	DIS	DIS	DIS	EN	EN	DIS	DIS	EN	EN	DIS	DIS	EN	EN
MTXD02/STXD1	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	DIS	DIS	DIS	DIS
MTXD03/STXSYNC1	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	DIS	DIS	DIS	DIS
MTXD04/RMTXD10/ STXCLK1	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	DIS	DIS	DIS	DIS
MTXD05/RMTXD11	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MTXD06/RMTXEN1	EN	DIS	EN	EN	EN	EN	DIS	DIS	DIS	DIS	EN	EN	EN	EN
MTXD07/STXCLK0	EN	DIS	EN	DIS	EN	EN	EN	DIS	EN	EN	EN	DIS	EN	EN
MTXEN0/RMTXEN0	DIS	DIS	DIS	EN	EN	EN	DIS	EN	EN	EN	DIS	EN	EN	EN
MCOL0	DIS	DIS	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN
GMDIO	DIS	DIS	DIS	DIS	EN	DIS	DIS	DIS	EN	DIS	DIS	DIS	EN	DIS
GMDCLK	DIS	DIS	DIS	DIS	EN	DIS	DIS	DIS	EN	DIS	DIS	DIS	EN	DIS

(1) DIS = Disabled internal pull resistor and enabled output buffer; EN = Enabled internal pull resistor and disabled output buffer.
(2) Although MDIO is shared between EMAC0 and EMAC1, only MACSEL0 (i.e., EMAC0) configuration pins are used to control the MDIO interface. For example, when EMAC0 is in RGMII mode the 1.8-V MDIO pins are used (3.3-V MDIO pins are not used) and when EMAC0 is in non-RGMII mode the 3.3-V MDIO pins are used (1.8-V RGMII MDIO pins are not used).

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Table 3-5. HPI IPU/IPD Control(1)(2)(3)

SIGNAL NAME	HPI_EN =	
	1	0
HD00	DIS	EN
HD01	DIS	EN
HD02	DIS	EN
HD03	DIS	EN
HD04	DIS	EN
HD05	DIS	EN
HD06	DIS	EN
HD07	DIS	EN
HD08	DIS	EN
HD09	DIS	EN
HD10	DIS	EN
HD11	DIS	EN
HD12	DIS	EN
HD13	DIS	EN
HD14	DIS	EN
HD15	DIS	EN
$\overline{\text{HAS}}$	EN	EN
HCNTL0	DIS	EN
HCNTL1	DIS	EN
$\overline{\text{HCS}}$	EN	EN
$\overline{\text{HDS1}}$	DIS	EN
$\overline{\text{HDS2}}$	DIS	EN
HHWIL	DIS	EN
$\overline{\text{HINT}}$	EN	EN
$\overline{\text{HRW}}$	DIS	EN
$\overline{\text{HRDY}}$	DIS	EN

(1) DIS = Disabled internal pull resistor; EN = Enabled internal pull resistor.
(2) HOUT is not part of the HPI and HPI_EN does not affect its operation.
(3) Although the internal pull resistors are enabled for $\overline{\text{HAS}}$, $\overline{\text{HCS}}$, and $\overline{\text{HINT}}$ when HPI_EN = 1, the buffers remain on.

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Table 3-6. TSIP0 IPD Control(1)

SIGNAL NAME	TSIP0_ EN[2:0] =			
	111	011	001	xx0
CLKA0	DIS	DIS	DIS	EN
CLKB0	DIS	DIS	DIS	EN
FSA0	DIS	DIS	DIS	EN
FSB0	DIS	DIS	DIS	EN
TR00	DIS	DIS	DIS	EN
TR01	DIS	DIS	DIS	EN
TR02	DIS	DIS	EN	EN
TR03	DIS	DIS	EN	EN
TR04	DIS	EN	EN	EN
TR05	DIS	EN	EN	EN
TR06	DIS	EN	EN	EN
TR07	DIS	EN	EN	EN
TX00	DIS	DIS	DIS	EN
TX01	DIS	DIS	DIS	EN
TX02	DIS	DIS	EN	EN
TX03	DIS	DIS	EN	EN
TX04	DIS	EN	EN	EN
TX05	DIS	EN	EN	EN
TX06	DIS	EN	EN	EN
TX07	DIS	EN	EN	EN

(1) DIS = Disabled internal pull resistor; EN = Enabled internal pull resistor.

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Table 3-7. TSIP1 IPD Control(1)

SIGNAL NAME	TSIP1_ EN[2:0] =			
	111	011	001	xx0
CLKA1	DIS	DIS	DIS	EN
CLKB1	DIS	DIS	DIS	EN
FSA1	DIS	DIS	DIS	EN
FSB1	DIS	DIS	DIS	EN
TR10	DIS	DIS	DIS	EN
TR11	DIS	DIS	DIS	EN
TR12	DIS	DIS	EN	EN
TR13	DIS	DIS	EN	EN
TR14	DIS	EN	EN	EN
TR15	DIS	EN	EN	EN
TR16	DIS	EN	EN	EN
TR17	DIS	EN	EN	EN
TX10	DIS	DIS	DIS	EN
TX11	DIS	DIS	DIS	EN
TX12	DIS	DIS	EN	EN
TX13	DIS	DIS	EN	EN
TX14	DIS	EN	EN	EN
TX15	DIS	EN	EN	EN
TX16	DIS	EN	EN	EN
TX17	DIS	EN	EN	EN

(1) DIS = Disabled internal pull resistor; EN = Enabled internal pull resistor.

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Table 3-8. TSIP2 IPD Control(1)

SIGNAL NAME	TSIP2_ EN[2:0] =			
	111	011	001	xx0
CLKA2	DIS	DIS	DIS	EN
CLKB2	DIS	DIS	DIS	EN
FSA2	DIS	DIS	DIS	EN
FSB2	DIS	DIS	DIS	EN
TR20	DIS	DIS	DIS	EN
TR21	DIS	DIS	DIS	EN
TR22	DIS	DIS	EN	EN
TR23	DIS	DIS	EN	EN
TR24	DIS	EN	EN	EN
TR25	DIS	EN	EN	EN
TR26	DIS	EN	EN	EN
TR27	DIS	EN	EN	EN
TX20	DIS	DIS	DIS	EN
TX21	DIS	DIS	DIS	EN
TX22	DIS	DIS	EN	EN
TX23	DIS	DIS	EN	EN
TX24	DIS	EN	EN	EN
TX25	DIS	EN	EN	EN
TX26	DIS	EN	EN	EN
TX27	DIS	EN	EN	EN

(1) DIS = Disabled internal pull resistor; EN = Enabled internal pull resistor.

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Table 3-9. UTOPIA IPU/IPD Control(1)

SIGNAL NAME	UTOPIA_EN =		
	11	01	x0
URCLK	DIS	DIS	EN
URCLAV	DIS	DIS	EN
URADDR0	DIS	DIS	EN
URADDR1	DIS	DIS	EN
URADDR2	DIS	DIS	EN
URADDR3	DIS	DIS	EN
URADDR4	DIS	DIS	EN
URDATA0	DIS	DIS	EN
URDATA1	DIS	DIS	EN
URDATA2	DIS	DIS	EN
URDATA3	DIS	DIS	EN
URDATA4	DIS	DIS	EN
URDATA5	DIS	DIS	EN
URDATA6	DIS	DIS	EN
URDATA7	DIS	DIS	EN
URDATA8	DIS	EN	EN
URDATA9	DIS	EN	EN
URDATA10	DIS	EN	EN
URDATA11	DIS	EN	EN
URDATA12	DIS	EN	EN
URDATA13	DIS	EN	EN
URDATA14	DIS	EN	EN
URDATA15	DIS	EN	EN
$\overline{\text{URENB}}$	DIS	DIS	EN
URSOC	DIS	DIS	EN
UXADDR0	DIS	DIS	EN
UXADDR1	DIS	DIS	EN
UXADDR2	DIS	DIS	EN
UXADDR3	DIS	DIS	EN
UXADDR4	DIS	DIS	EN
UXCLAV	DIS	DIS	EN
UXCLK	DIS	DIS	EN
UXDATA0	DIS	DIS	EN
UXDATA1	DIS	DIS	EN
UXDATA2	DIS	DIS	EN
UXDATA3	DIS	DIS	EN
UXDATA4	DIS	DIS	EN
UXDATA5	DIS	DIS	EN
UXDATA6	DIS	DIS	EN
UXDATA7	DIS	DIS	EN
UXDATA8	DIS	EN	EN
UXDATA9	DIS	EN	EN
UXDATA10	DIS	EN	EN
UXDATA11	DIS	EN	EN
UXDATA12	DIS	EN	EN

(1) DIS = Disabled internal pull resistor; EN = Enabled internal pull resistor.

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Table 3-9. UTOPIA IPU/IPD Control[1] (continued)

SIGNAL NAME	UTOPIA_EN =		
	11	01	x0
UXDATA13	DIS	EN	EN
UXDATA14	DIS	EN	EN
UXDATA15	DIS	EN	EN
$\overline{\text{UXENB}}$	DIS	DIS	EN
UXSOC	DIS	DIS	EN

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3.4 Device Status Register (DEVSTAT)

The device status register (DEVSTAT) depicts the status of the device configuration inputs that were captured at device reset. The DEVSTAT register is shown in Figure 3-3.

31	30	29	28	27	26	25	24
Reserved				Reserved	Reserved		
0000				R-0	R-0		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MACSEL11	MACSEL10	CFGGP4	CFGGP3	CFGGP2	CFGGP1	CFGGP0	RIOEN
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SYSCLKOUTEN	Reserved		Reserved	Reserved	MACSEL02	MACSEL01	MACSEL00
R-x	R-0		R-0	R-0	R-x	R-x	R-x
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	LENDIAN	DDREN	Reserved	BOOTMODE3	BOOTMODE2	BOOTMODE1	BOOTMODE0
R-0	R-x	R-x	R-0	R-x	R-x	R-x	R-x

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-3. Device Status Register (DEVSTAT)

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3.5 RMII*n* Reset Registers (RMIIRESET0 and RMIIRESET1)

RMII supports switching of 10/100 Mbps modes and switching between half and full-duplex. The RMIIRESET0 and RMIIRESET1 registers are used to reset the RMII interface to switch the speed and duplex settings. The selection of 10/100 Mbps and half- and full-duplex modes is determined by registers in the EMAC modules. For more information, see the *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (literature number SPRUEF8).

31	16
Reserved	
R-0	

15	1	0
Reserved		RESET
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-4. RMII*n* Reset Registers (RMIIRESET0 and RMIIRESET1)

Table 3-10. RMII*n* Reset Registers (RMIIRESET0 and RMIIRESET1) Field Descriptions

Bit	Field	Value	Description
31:1	Reserved		Reserved
0	RESET		RMII Reset
		0	Reset is deasserted.
		1	Reset is asserted.

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3.6 Memory Privilege Registers

3.6.1 Host Memory Privilege Permission Register (HOSTPRIV)

Memory privilege is an extension of the memory protection defined in the C64x+ megamodule. It defines the supervisor user mode privilege required to access peripherals that do not inherently have the protection built in. For more information, see the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

The host memory privilege permission register (HOSTPRIV) configures host memory privilege modes. HOSTPRIV defines the privilege to be used when an external host uses direct IO with SRIO or HPI to access any on-chip memory or peripherals or external memory via the EMIF. Writing a 1 makes supervisor-mode accesses from the peripheral; writing a 0 makes user-mode accesses from the peripheral. The default for these bits is supervisor-mode access.

31	16
Reserved	
R-1111 1111 1111 1111 1111 1111 1111 11	

15	2	1	0
Reserved		SRIO	HPI
R-1111 1111 1111 1111 1111 1111 1111 11		R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-5. Host Memory Privilege Permission Register (HOSTPRIV)

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3.6.2 Memory Privilege Permission Register (PRIVPERM)

The memory privilege permission register (PRIVPERM) defines the permission level necessary to access peripheral registers on the CFG SCR. The defaults allow both user- and supervisor-level accesses to these peripheral groups. If desired, the software can override accesses to these peripheral groups by writing the values shown in Table 3-11 to the register bits. For the purposes of protection, certain peripherals are grouped together (see Table 3-12), thus, the selected protection applies to the entire group; i.e., setting 0 to the RIO bit field would make user-mode accesses to SRIO and SRIO wrappers configuration space.

Table 3-11. Permission Values

ACCESSES	PERMISSION VALUE
Supervisor and user modes	00
Supervisor mode	10
User mode	01
None	11

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
GPIO	HPI	EMAC	UTOPIA	RIO	TSIP	TIMER64	IIC
R/W-00	R/W-00	R/W-00	R/W-00	R/W-00	R/W-00	R/W-00	R/W-00
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
SMC	CLRF1	CLRF0	PLL_CTRL	PSC	SEC_CTL	BOOT_CTL	ETB
R/W-00	R/W-00	R/W-0, R-0	R/W-00	R/W-00	R/W-00	R/W-00	R/W-00

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 3-6. Memory Privilege Permission Register (PRIVPERM)

Table 3-12. PRIVPERM Register Peripheral Grouping

PERIPHERAL GROUP	GROUP CONTENTS
GPIO	GPIO module
HPI	HPI module
EMAC	EMAC0, EMAC1, MDIO, EMAC0 Descriptor Memory, EMIC0, EMAC1 Descriptor Memory, EMIC1
UTOPIA	UTOPIA, PIM-PDMA
RIO	SRIO, SRIO Descriptor Memory
TSIP	TSIP2, TSIP1, TSIP0
TIMER64	12 Timer64s
IIC	IIC
SMC	SMC and 6 SMCPs
CLRF1	Chip-level register file class 1
CLRF0	Chip-level register file class 0
PLL_CTRL	PLL1, PLL2, and PLL3 controllers
PSC	Power and sleep controllers
SEC_CTL	Security control
BOOT_CTL	Boot controller
ETB	6 ETBs

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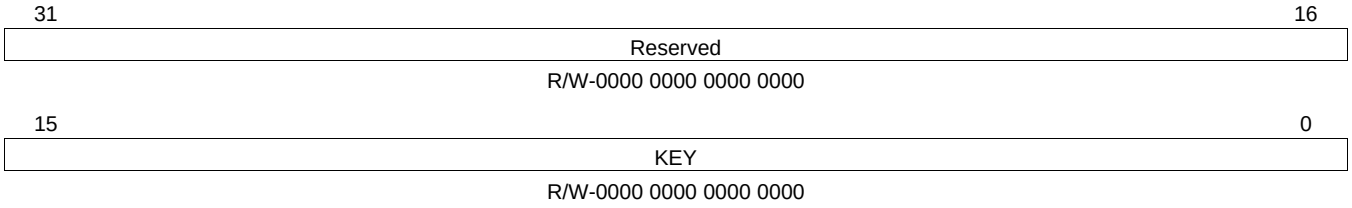
3.6.3 Key-Based Protection for HOSTPRIV and PRIVPERM Registers (PRIVKEY)

Key-based protection of HOSTPRIV and PRIVPERM is provided for a higher level of protection or control over changing the permission levels. The PRIVKEY register, shown in Figure 3-7 and described in Table 3-13, is needed to service the key requirement. Updates to the HOSTPRIV and PRIVPERM registers are only allowed when PRIVKEY contains the lower 16-bit key value (BEA7h). Protection is provided by a following write to PRIVKEY to clear the register. The PRIVKEY is a 32-bit register with the lower 16 bits as key field and upper 16 bits reserved to 0.



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 3-7. Key-Based Protection Register (PRIVKEY)

Table 3-13. Key-Based Protection Register (PRIVKEY) Field Descriptions

Bit	Field	Value	Description
31:16	Reserved		Reserved
15:0	KEY		Key (BEA7h). These fields, [15:0], get updated only when KEY = BEA7h. Returns 0000h on read.

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3.7 Host and Inter-DSP Interrupt Registers

3.7.1 NMI Generator Registers (NMIGR0-NMIGR5)

The NMI generator registers (NMIGR0-NMIGR5) create an NMI event to each C64x+ megamodule. The NMIGR0 register generates an NMI event to C64x+ Megamodule0, the NMIGR1 register generates an NMI event to C64x+ Megamodule1, etc. Writing a 1 to the NMIG field generates an NMI pulse. Writing a 0 has no effect; reads return 0 and have no other effect. The source ID fields found in IPCGR0-IPCGR5 can be used along with the NMI generation registers to identify the source of the NMI.

31	16
Reserved	
R-0000 0000 0000 0000 0000 0000 0000 000	

15	1	0
Reserved		NMIG
R-0000 0000 0000 0000 0000 0000 0000 000		R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 3-8. NMI Generator Registers (NMIGR0-NMIGR5)

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3.7.2 Inter-DSP Interrupt Registers (IPCGR0-IPCGR5 and IPCAR0-IPCAR5)

The IPCGR*n* (IPCGR0 thru IPCGR5) and IPCAR*n* (IPCAR0 thru IPCAR5) registers facilitate inter-DSP interrupts. This can be utilized by external hosts or C64x+ megamodules to generate interrupts to other DSPs. A write of 1 to the IPCG field of IPCGR*n* register generates an interrupt pulse to C64x+ Megamodule*n* (*n* = 0-5). These registers also provide a source ID, by which up to 28 different sources of interrupts can be identified.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRCS27	SRCS26	SRCS25	SRCS24	SRCS23	SRCS22	SRCS21	SRCS20	SRCS19	SRCS18	SRCS17	SRCS16	SRCS15	SRCS14	SRCS13	SRCS12
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3		1	0
SRCS11	SRCS10	SRCS9	SRCS8	SRCS7	SRCS6	SRCS5	SRCS4	SRCS3	SRCS2	SRCS1	SRCS0	Reserved			IPCG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-000			R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-9. IPC Generation Registers (IPCGR0-IPCGR5)

Table 3-14. IPC Generation Registers (IPCGR0-IPCGR5) Field Descriptions

Bit	Field	Value	Description
31:4	SRCS[27:0]		Write:
		0	No effect
		1	Set register bit
			Read:
			Returns current value of internal register bit
3:1	Reserved		Reserved
0	IPCG		Write:
		0	No effect
		1	Create an inter-DSP interrupt pulse to the corresponding C64x+ megamodule (C64x+ Megamodule0 for IPCGR0, etc.)
			Read:
			Returns 0, no effect

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRCC27	SRCC26	SRCC25	SRCC24	SRCC23	SRCC22	SRCC21	SRCC20	SRCC19	SRCC18	SRCC17	SRCC16	SRCC15	SRCC14	SRCC13	SRCC12
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	0
SRCC11	SRCC10	SRCC9	SRCC8	SRCC7	SRCC6	SRCC5	SRCC4	SRCC3	SRCC2	SRCC1	SRCC0	Reserved	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0000	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 3-10. IPC Acknowledgment Registers (IPCAR0-IPCAR5)

Table 3-15. IPC Acknowledgment Registers (IPCAR0-IPCAR5) Field Descriptions

Bit	Field	Value	Description
31:4	SRCC[27:0]		Write:
		0	No effect
		1	Clear corresponding SRCS bit in the IPCGR register
			Read:
			Returns current value of internal register bit
3:0	Reserved		Reserved

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3.7.3 Host Interrupt and Event Pulse Generation Registers (IPCGR15 and IPCAR15)

The host interrupt and event pulse generation registers (IPCGR15 (or IPCGRH) and IPCAR15 (or IPCARH)) facilitate host CPU interrupt. Operation and use of the IPCGR15 register is the same as registers IPCGR0-5 and the IPCAR15 register is the same as registers IPCAR0-5. The interrupt output pulse created by the IPCGR15 register is driven on a device pin host interrupt/event output (HOUT). The interrupt output pulse is asserted for 4 CPU/6 cycles followed by a deassertion of 4 CPU/6 cycles.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRCS27	SRCS26	SRCS25	SRCS24	SRCS23	SRCS22	SRCS21	SRCS20	SRCS19	SRCS18	SRCS17	SRCS16	SRCS15	SRCS14	SRCS13	SRCS12
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	1	0
SRCS11	SRCS10	SRCS9	SRCS8	SRCS7	SRCS6	SRCS5	SRCS4	SRCS3	SRCS2	SRCS1	SRCS0	Reserved		IPCG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-000		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-11. IPC Generation Register (IPCGR15)

Table 3-16. IPC Generation Register (IPCGR15) Field Descriptions

Bit	Field	Value	Description
31:4	SRCS[27:0]		Write:
		0	No effect
		1	Set register bit
			Read:
			Returns current value of internal register bit
3:1	Reserved		Reserved
0	IPCG		Write:
		0	No effect
		1	Create an interrupt pulse on the device pin (HOUT)
			Read:
			Returns 0, no effect

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRCC27	SRCC26	SRCC25	SRCC24	SRCC23	SRCC22	SRCC21	SRCC20	SRCC19	SRCC18	SRCC17	SRCC16	SRCC15	SRCC14	SRCC13	SRCC12
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8	7	6	5	4	3	0
SRCC11	SRCC10	SRCC9	SRCC8	SRCC7	SRCC6	SRCC5	SRCC4	SRCC3	SRCC2	SRCC1	SRCC0	Reserved	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-12. IPC Acknowledgment Register (IPCAR15)

Table 3-17. IPC Acknowledgment Register (IPCAR15) Field Descriptions

Bit	Field	Value	Description
31:4	SRCC[27:0]		Write:
		0	No effect
		1	Clear corresponding SRCS bit in the IPCGR register
			Read:
			Returns current value of internal register bit
3:0	Reserved		Reserved

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3.8 Timer Event Manager Registers

3.8.1 Timer Pin Manager Register (TPMGR)

The timer pin manager register (TPMGR) configures the timer output pin. The TPMGR register details are shown in Figure 3-13 and described in Table 3-18.

31	4	3	0
Reserved		TOUTSEL	
R-0000 0000 0000 0000 0000 0000 0000		R/W-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-13. Timer Pin Manager Register (TPMGR)

Table 3-18. Timer Pin Manager Register (TPMGR) Field Descriptions

Bit	Field	Value	Description
31:4	Reserved		Reserved
3:0	TOUTSEL	0000	Nothing selected for TIMO2
		0001	Timer64 6 - TOUTL selected for TIMO2
		0010	Timer64 6 - TOUTH selected for TIMO2
		0011	Timer64 7 - TOUTL selected for TIMO2
		0100	Timer64 7 - TOUTH selected for TIMO2
		0101	Timer64 8 - TOUTL selected for TIMO2
		0110	Timer64 8 - TOUTH selected for TIMO2
		0111	Timer64 9 - TOUTL selected for TIMO2
		1000	Timer64 9 - TOUTH selected for TIMO2
		1001	Timer64 10 - TOUTL selected for TIMO2
		1010	Timer64 10 - TOUTH selected for TIMO2
		1011	Timer64 11 - TOUTL selected for TIMO2
		1100	Timer64 11 - TOUTH selected for TIMO2
		1101-1111	Reserved

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3.8.2 Reset Mux Registers (RSTMUX0-RSTMUX5)

The reset controller has inputs for each of the watchdog timer outputs. The reset mux registers determine the method of reset that will be used when a watchdog timeout occurs.

31															16
Reserved															
R-0000 0000 0000 0000 0000 000															

15														9	8
Reserved															DELAY
R-0000 0000 0000 0000 0000 000															R/W-100

7	6	5	4	3	2	1	0
DELAY		Reserved	EVTSTAT	OMODE			LOCK
R/W-100		R-0	RC-0	R/W-000			R/W-0

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

Figure 3-14. Reset Mux Registers (RSTMUX0-RSTMUX5)

Table 3-19. Reset Mux Registers (RSTMUX0-RSTMUX5) Field Descriptions

Bit	Field	Value	Description
31:9	Reserved		Reserved
8:6	DELAY	000	256 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		001	512 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		010	1024 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		011	2048 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		100	4096 CPU/6 cycles delay between NMI and local reset, when OMODE = 100 (default).
		101	8192 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		110	16384 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
		111	32768 CPU/6 cycles delay between NMI and local reset, when OMODE = 100.
5	Reserved		Reserved
4	EVTSTAT		The EVTSTAT bit indicates if any local timer event is received. The event could be a timeout event (when the timer is configured in watchdog mode). Since there is only one output pin of a watchdog event (WDOUT), the software can read this bit to know which one of the 6 timers has timed out. Writing a 0 clears this bit.
		0	No event received (default).
		1	Timer event received by the reset mux block.
3:1	OMODE		The OMODE bits determine how to handle the local timer events.
		000	Timer event input to the reset mux block does not cause any output event (default).
		001	Reserved
		010	Timer event input to the reset mux block causes local reset input to C64x+ megamodule.
		011	Timer event input to the reset mux block causes NMI input to C64x+ megamodule.
		100	Timer event input to the reset mux block causes NMI input followed by local reset input to C64x+ megamodule. Delay between NMI and local reset is set in the DELAY bit field.
		101	Timer event input to the reset mux block causes system reset to the PLL controller.
		110	Reserved
		111	Reserved
0	LOCK		The LOCK field prevents further writes to the register when set to 1. After the software configures the timer in watchdog mode and the appropriate routing of events to C64x+ megamodule, it is expected to set the LOCK bit to 1. This will prevent accidental modification of the bit fields of this register. The LOCK bit is reset to 0 only on the next reset that resets the Timer64.
		0	Register fields are not locked (default).
		1	Register fields are locked until the next timer reset.

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3.9 Reset and Boot Registers

3.9.1 Reset Status Register (RESET_STAT)

The reset status register (RESET_STAT) indicates the status of global (device) reset and of the local reset for all six C64x+ megamodules.

31	30	16
GR	Reserved	
RC-0	R-000 0000 0000 0000	

15	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		LR5		LR4		LR3		LR2		LR1		LR0	
R-00 0000 0000 0000		RC-10		RC-10		RC-10		RC-10		RC-10		RC-10	

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

Figure 3-15. Reset Status Register (RESET_STAT)

Table 3-20. Reset Status Register (RESET_STAT) Field Descriptions

Bit	Field	Value	Description
31	GR	1	Global Reset. Writing a 1 to GR clears the bit, writing a 0 has no effect.
30:12	Reserved		Reserved
11:10	LR5		Local Reset 5. Writing a 1 to LR5 clears the bit; writing a 0 has no effect.
		00	Core 5 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 5.
		10	Reserved
		11	Core 5 has responded with lreset_out.
9:8	LR4		Local Reset 4. Writing a 1 to LR4 clears the bit; writing a 0 has no effect.
		00	Core 4 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 4.
		10	Reserved
		11	Core 4 has responded with lreset_out.
7:6	LR3		Local Reset 3. Writing a 1 to LR3 clears the bit; writing a 0 has no effect.
		00	Core 3 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 3.
		10	Reserved
		11	Core 3 has responded with lreset_out.
5:4	LR2		Local Reset 2. Writing a 1 to LR2 clears the bit; writing a 0 has no effect.
		00	Core 2 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 2.
		10	Reserved
		11	Core 2 has responded with lreset_out.
3:2	LR1		Local Reset 1. Writing a 1 to LR1 clears the bit; writing a 0 has no effect.
		00	Core 1 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 1.
		10	Reserved
		11	Core 1 has responded with lreset_out.
1:0	LR0		Local Reset 0. Writing a 1 to LR0 clears the bit; writing a 0 has no effect.
		00	Core 0 has not received a local reset.
		01	A local reset (lreset_in) has been asserted to Core 0.
		10	Core 0 has responded with lreset_out in global boot situation.
		11	Core 0 has responded with lreset_out.

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3.9.2 Boot Complete Status Register (BOOT_COMPLETE_STAT)

The boot complete status register (BOOT_COMPLETE_STAT) indicates if the boot process is complete.

31	16
Reserved	
R-0000 0000 0000 0000	

15	6	5	4	3	2	1	0
Reserved		BC5	BC4	BC3	BC2	BC1	BC0
R-00 0000 0000		RS-0	RS-0	RS-0	RS-0	RS-0	RS-0

LEGEND: R/W = Read/Write; R = Read only; S = Set; -*n* = value after reset

Figure 3-16. Boot Complete Status Register (BOOT_COMPLETE_STAT)

Table 3-21. Boot Complete Status Register (BOOT_COMPLETE_STAT) Field Descriptions

Bit	Field	Value	Description
31:6	Reserved		Reserved
5	BC5		Boot Complete 5
		0	Core 5 did not complete boot
		1	Core 5 completed boot
4	BC4		Boot Complete 4
		0	Core 4 did not complete boot
		1	Core 4 completed boot
3	BC3		Boot Complete 3
		0	Core 3 did not complete boot
		1	Core 3 completed boot
2	BC2		Boot Complete 2
		0	Core 2 did not complete boot
		1	Core 2 completed boot
1	BC1		Boot Complete 1
		0	Core 1 did not complete boot
		1	Core 1 completed boot
0	BC0		Boot Complete 0
		0	Core 0 did not complete boot
		1	Core 0 completed boot

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3.9.3 Boot Progress Register (BOOTPROGRESS)

The boot progress register (BOOTPROGRESS) tracks the progress of the boot sequence. The ROM boot code periodically writes values to this register to indicate progress. This can also be used by other software as a debugging tool.

31	0
BOOTPROGRESS	
R/W-0000 0000 0000 0000 0000 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-17. Boot Progress Register (BOOTPROGRESS)

3.9.4 BOOTMODEn Register (BOOTMODE0-BOOTMODE5)

The chip-level boot modes are set using the BOOTMODE[3:0] device pins. In addition to this, for local boot purposes, each core can set its BOOTMODE choice using the registers BOOTMODE0 through BOOTMODE5. The default values of these registers are set to immediate boot mode.

31	4	3	0
Reserved		BOOTMODE	
R-0000 0000 0000 0000 0000 0000 0000		R/W-0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-18. BOOTMODE*n* Register (BOOTMODE0-BOOTMODE5)

Table 3-22. BOOTMODE*n* Register (BOOTMODE0-BOOTMODE5) Field Descriptions

Bit	Field	Value	Description
31:4	Reserved		Reserved
3:0	BOOTMODE		Boot Mode [3:0].
		0000	Immediate boot (default).
		0001	Host boot.
		0010-1111	Reserved

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3.9.5 DSP_BOOT_ADDRn Register (DSP_BOOT_ADDR0-DSP_BOOT_ADDR5)

Each C64x+ megamodule has its own boot address register (DSP_BOOT_ADDR*n*) associated with it. The contents of these registers are the 22 MSBs of the initial fetch address of the C64x+ megamodule*n* from where it starts executing after the boot complete bit is set.

In Immediate Boot (Boot mode 0) and HPI Boot (Boot mode 1) modes, all six registers have the L2 RAM base address tie-off value 00 2000h as default, which corresponds to 0080 0000h. In the case of HPI boot mode, the host can overwrite these registers before boot complete is set to change the boot address for each C64x+ megamodule.

For other boot modes (boot modes 2 - 15), DSP_BOOT_ADDR0 has SL2 ROM base address tie-off value 00 0400h as the default. Other GEM_BOOT_ADDR*n* registers have L2 RAM base address tie-off values 00 2000h as default. In this mode, the application can set individual boot addresses for individual C64x+ megamodules by programming different values in the GEM_BOOT_ADDR*n* registers.

31	22	21	16
Reserved		DSP_BOOT_ADDR(A)	
R-0		R/W-00 0000 0010 0000 0000 0000	

15	0
DSP_BOOT_ADDR(A)	
R/W-00 0000 0010 0000 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

A. For boot modes 2 - 15, DSP_BOOT_ADDR0 has default address 00 0400h and DSP_BOOT_ADDR1 - DSP_BOOT_ADDR5 have default address 00 2000h. For boot mode 0 and 1, all registers have default address 00 2000h.

Figure 3-19. DSP_BOOT_ADDR*n* Register (DSP_BOOT_ADDR0-DSP_BOOT_ADDR5)

Table 3-23. DSP_BOOT_ADDR*n* Register (DSP_BOOT_ADDR0-DSP_BOOT_ADDR5) Field Descriptions

Bit	Field	Value	Description
31:22	Reserved		Reserved
21:0	DSP_BOOT_ADDR		DSP Boot Address.(1)

(1) For boot modes 2 - 15, DSP_BOOT_ADDR0 has default address 00 0400h and DSP_BOOT_ADDR1 - DSP_BOOT_ADDR5 have default address 00 2000h. For boot mode 0 and 1, all registers have default address 00 2000h.

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3.10 JTAG ID Register Description

The JTAG ID register is a read-only register that identifies to the customer the JTAG ID (DEVICE_ID). For the C6472 device, the JTAG ID register resides at address location 02A8 0008h. It reads 0009 102Fh. For the actual register bit names and their associated bit field descriptions, see Figure 3-20 and Table 3-24.

31 28	27 12	11 1	0
VARIANT (4-bit)	PART NUMBER (16-bit)	MANUFACTURER (11-bit)	LSB
R-0000	R-0000 0000 1001 0001	R-0000 0010 111	R-1

LEGEND: R = Read only; -*n* = value after reset

Figure 3-20. JTAG ID (DEVICE_ID) Register - C6472 Register Value

Table 3-24. JTAG ID (DEVICE_ID) Register Field Descriptions

Bit	Field	Value	Description
31:28	VARIANT	0000	Variant (4-Bit) value.(1) **Note:** The VARIANT field may be invalid if no CLKIN1 signal is applied. The value of this field depends on the silicon revision being used. For more information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).
27:12	PART NUMBER	0000 0000 1001 0001	Part Number (16-Bit) value.(2)
11:1	MANUFACTURER	0000 0010 111	Manufacturer (11-Bit) value.(2)
0	LSB	1	LSB value.(2)

(1) Fixed value for each silicon revision. This table shows silicon revision 1.0, as an example.
(2) Fixed value irrespective of the silicon revision.

3.11 Silicon Revision ID Register Description

The silicon revision ID is a read-only register that provides silicon revision details. For the C6472 device, the silicon revision ID register is at address location 02A8 070Ch. It reads 0010 0091h. The silicon revision ID Register is shown in Figure 3-21 and described inTable 3-25.

31 24	23 20	19 16
Reserved 8-bit	MAJOR REVISION 4-bit	MINOR REVISION 4-bit
R-0000 0000	R-0001	R-0000

15 0
PART NUMBER 16-bit
R-0000 0000 1001 0001

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-21. Silicon Revision ID Register

Table 3-25. Silicon Revision ID Register Field Descriptions

Bit	Field	Value	Description
31:24	Reserved	0000 0000	Reserved
23:20	MAJOR REVISION	0001	Major revision of the silicon(1)
19:16	MINOR REVISION	0000	Minor revision of the silicon(1)
15:0	PART NUMBER	0000 0000 1001 0001	Part number of the silicon(2)

(1) Fixed value for each silicon revision. This table shows silicon revision 1.0, as an example.
(2) Fixed value irrespective of the silicon revision.

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4 System Interconnect

On the C6472 device, the C64x+ megamodule, the EDMA3 transfer controllers, and the system peripherals are interconnected through two switch fabrics. The switch fabrics allow for low-latency, concurrent data transfers between peripherals and memories. The switch fabrics also allow for seamless arbitration between the system masters when accessing system slaves.

4.1 Internal Buses, Bridges, and Switch Fabrics

Two types of buses exist in the C6472 device: data buses and configuration buses. Some C6472 peripherals have both a data bus and a configuration bus interface, while others only have one type of interface. Furthermore, the bus interface width and speed varies from peripheral to peripheral. Configuration buses are mainly used to access the register space of a peripheral and the data buses are used mainly for data transfers.

The C64x+ megamodule, the EDMA3 transfer controllers, and the various system peripherals can be classified into two categories: masters and slaves. Masters are capable of initiating read and write transfers in the system and do not rely on the EDMA3 for their data transfers. Slaves, on the other hand, rely on the EDMA3 to perform transfers to and from them. Masters include the EDMA3 transfer controllers, EMAC, TSIP, HPI, UTOPIA, and SRIO. Slaves include the EMIF and I2C.

The C6472 device contains two switch fabrics through which masters and slaves communicate: the data switch fabric, known as the data switched central resource (SCR) and configuration switch fabric, known as the configuration switched central resource (SCR). The data SCR is a high-throughput interconnect mainly used to move data across the system (for more information, see Section 4.2). The data SCR connects masters to slaves via 128-bit data buses running at a SYSCLK7 frequency, generated from the PLL1 controller. Peripherals that have a 128-bit data bus interface running at this speed can connect directly to the data SCR; other peripherals require a bridge. The configuration SCR is mainly used by the C64x+ megamodules to access peripheral registers (for more information, see Section 4.4). The configuration SCR connects C64x+ megamodules to slaves via 32-bit configuration buses also running at a SYSCLK7 frequency. As with the data SCR, some peripherals require the use of a bridge to interface to the configuration SCR. Note that the data SCR also connects to the configuration SCR.

Bridges perform a variety of functions:

- Conversion between configuration bus and data bus.
- Width conversion between peripheral bus width and SCR bus width.
- Frequency conversion between peripheral bus frequency and SCR bus frequency.

For example, TSIP modules require a bridge to convert their 32-bit data bus interface into a 128-bit interface so that they can connect to the data SCR. Note that some peripherals can be accessed through the data SCR and also through the configuration SCR.

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4.2 Data Switch Fabric Connections

Figure 4-1 shows the connection between slaves and masters through the data switched central resource (SCR). Masters are shown on the right and slaves on the left. The data SCR connects masters to slaves via 128-bit data buses running at frequency equal to the CPU frequency divided by 3.

Some peripherals and the C64x+ megamodule have both slave and master ports. Note that each EDMA3 transfer controller has an independent connection to the data SCR.

The Serial RapidIO (SRIO) peripheral has two connections to the data SCR. The first connection is used when descriptors are being fetched from system memory. The other connection is used for all other data transfers.

Note that masters can access the configuration SCR through the data SCR. The configuration SCR is described in Section 4.4. Not all masters on the C6472 DSP may connect to all slaves. Allowed connections are summarized in Table 4-1.

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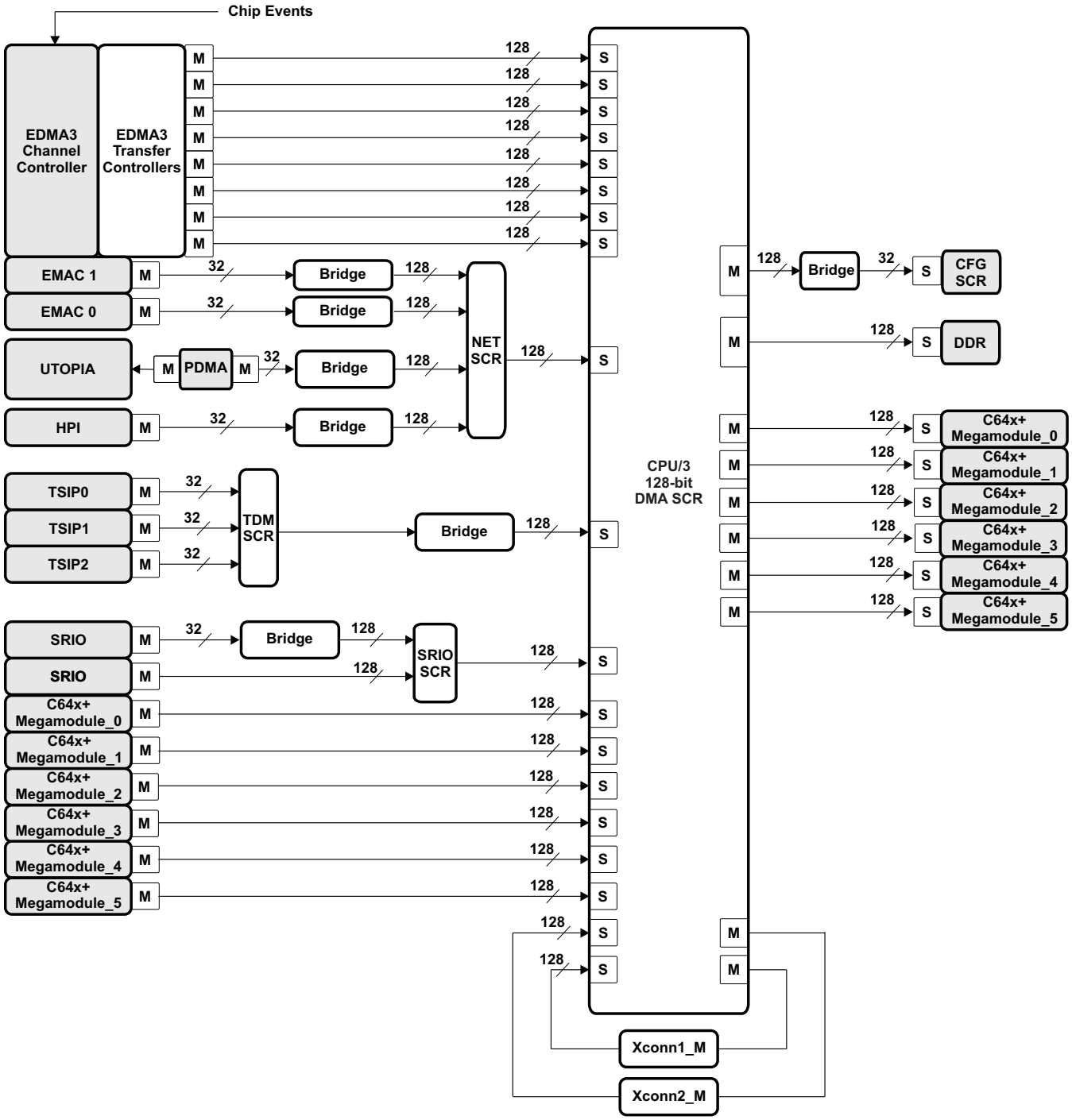

Figure 4-1. DMA Switched Central Resource

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Table 4-1. DMA SCR Connection Matrix(1)

MASTERS	SLAVES									
	CFGSCR	DDR2	C64x+ Megamodule0	C64x+ Megamodule1	C64x+ Megamodule2	C64x+ Megamodule3	C64x+ Megamodule4	C64x+ Megamodule5	Xconn1_S	Xconn2_S
EDMA3 Transfer Controller0_R	Y	Y	C	C	C	C	C	C	Y	N
EDMA3 Transfer Controller0_W	Y	Y	C	C	C	C	C	C	Y	N
EDMA3 Transfer Controller1_R	Y	Y	C	C	C	C	C	C	N	Y
EDMA3 Transfer Controller1_W	Y	Y	C	C	C	C	C	C	N	Y
EDMA3 Transfer Controller2_R	Y	Y	Y	Y	Y	Y	Y	Y	N	N
EDMA3 Transfer Controller2_W	Y	Y	Y	Y	Y	Y	Y	Y	N	N
EDMA3 Transfer Controller3_R	N	Y	Y	Y	Y	Y	Y	Y	N	N
EDMA3 Transfer Controller3_W	N	Y	Y	Y	Y	Y	Y	Y	N	N
EMAC0	Y	Y	Y	Y	Y	Y	Y	Y	N	N
EMAC1	Y	Y	Y	Y	Y	Y	Y	Y	N	N
UTOPIA	Y	Y	Y	Y	Y	Y	Y	Y	N	N
HPI	Y	Y	Y	Y	Y	Y	Y	Y	N	N
3x TSIP	N	Y	Y	Y	Y	Y	Y	Y	N	N
RapidIO	Y	Y	Y	Y	Y	Y	Y	Y	N	N
C64x+ Megamodule0	N	Y	N	C	C	C	C	C	Y	N
C64x+ Megamodule1	N	Y	C	N	C	C	C	C	Y	N
C64x+ Megamodule2	N	Y	C	C	N	C	C	C	Y	N
C64x+ Megamodule3	N	Y	C	C	C	N	C	C	N	Y
C64x+ Megamodule4	N	Y	C	C	C	C	N	C	N	Y
C64x+ Megamodule5	N	Y	C	C	C	C	C	N	N	Y
Xconn1_M	N	N	Y	Y	Y	Y	Y	Y	N	N
Xconn2_M	N	N	Y	Y	Y	Y	Y	Y	N	N

(1) Y = Direct connection in SCR.
C = Logical connection through Xconn1 or Xconn2 bridges.
N = No physical connection.

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4.3 Priority Allocation

On the C6472 device, DMA data transfers use a priority-based arbitration. The C64x+ megamodule, EDMA, TSIP, and SRIO peripherals define their own priorities. The Ethernet and HPI peripherals do not define their own priorities, while the UTOPIA-PDMA only partially defines its own priority. Priorities for Ethernet, HPI, and UTOPIA-PDMA transfers should be assigned via the Priority Allocation (PRI_ALLOC) register (see Figure 4-2). A value of 000b has the highest priority, while 111b has the lowest priority. (For more information on the default priority values in the C64x+ megamodule, EDMA, TSIP, and SRIO peripheral registers, see the device-compatible reference guides). TI recommends that these priority registers be reprogrammed upon initial use.

31															16
Reserved															
R-1111 1111 1111 1111															

15	14		12	11					8
UTOPIA-PDMA(A)	EMAC1			Reserved					
R/W-1	R/W-111			R-1111					

7	6	5			3	2			0
Reserved		HPI				EMAC0			
R-11		R/W-111				R/W-111			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value at reset

A. UTOPIA-PDMA has 2 bits of priority in the module. The PRI_ALLOC register supplies only the **middle significant bit** of the priority for this module.

Figure 4-2. Priority Allocation Register (PRI_ALLOC)

4.4 Configuration Switch Fabric

Figure 4-3 shows the connection between the C64x+ megamodule and the configuration switched central resource (SCR). The configuration SCR is mainly used by the C64x+ megamodules to access peripheral registers. The data SCR also has a connection to the configuration SCR which allows masters to access most peripheral registers. The only registers not accessible by the data SCR through the configuration SCR are the C64x+ megamodule configuration registers; these can only be accessed by the C64x+ megamodules.

The configuration SCR uses 32-bit configuration buses running at a frequency equal to the CPU frequency divided by 3.

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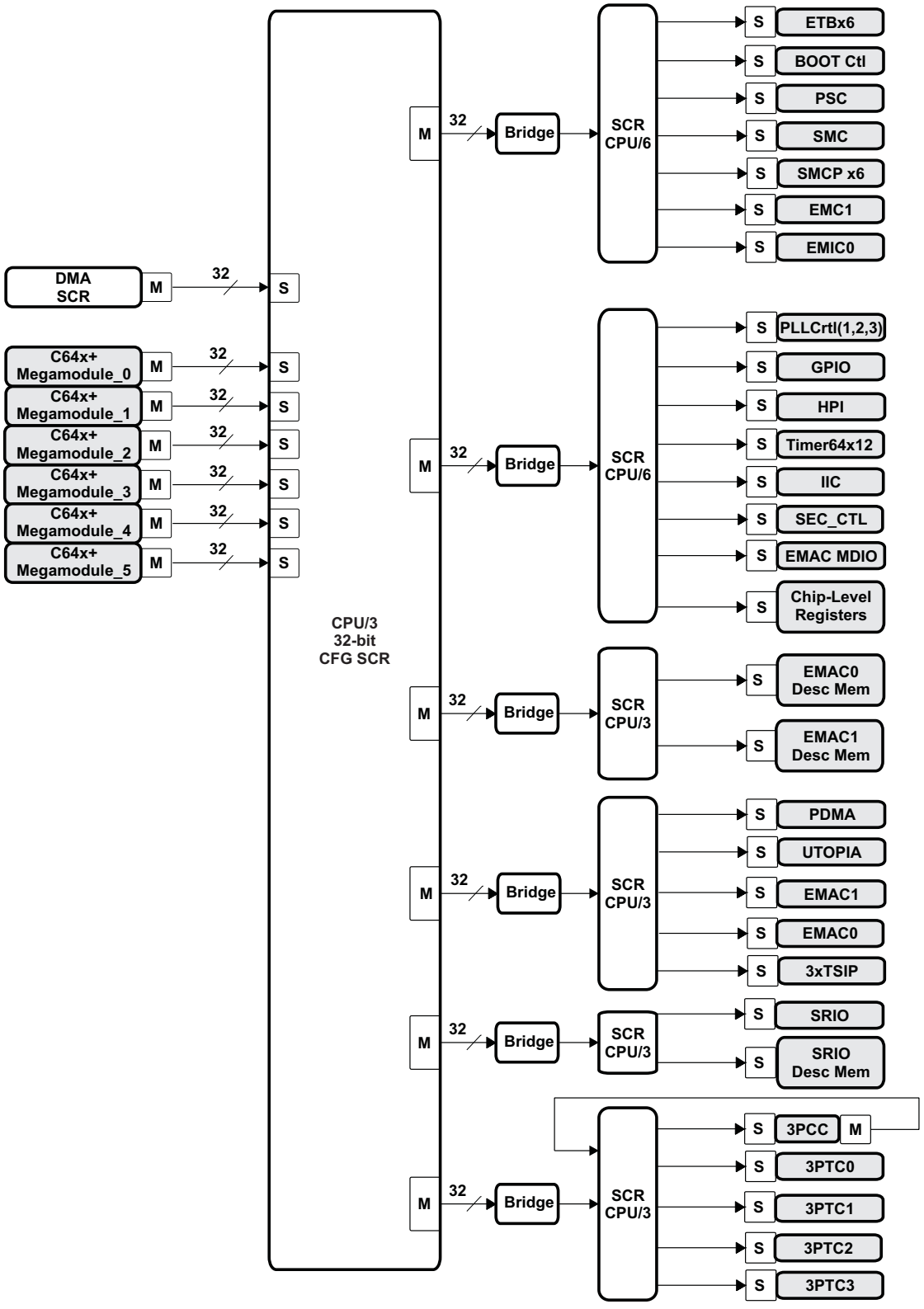

Figure 4-3. Configuration Switched Central Resource

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5 C64x+ Megamodule

The C64x+ Megamodule consists of several components — the C64x+ CPU, the L1 program and data memory controllers, the L2 memory controller, the internal DMA (IDMA), the interrupt controller, power-down controller, and external memory controller. The C64x+ Megamodule also provides support for memory protection (for L1P, L1D, and L2 memories) and bandwidth management (for resources local to the C64x+ Megamodule). Figure 5-1 shows a block diagram of the C64x+ Megamodule.

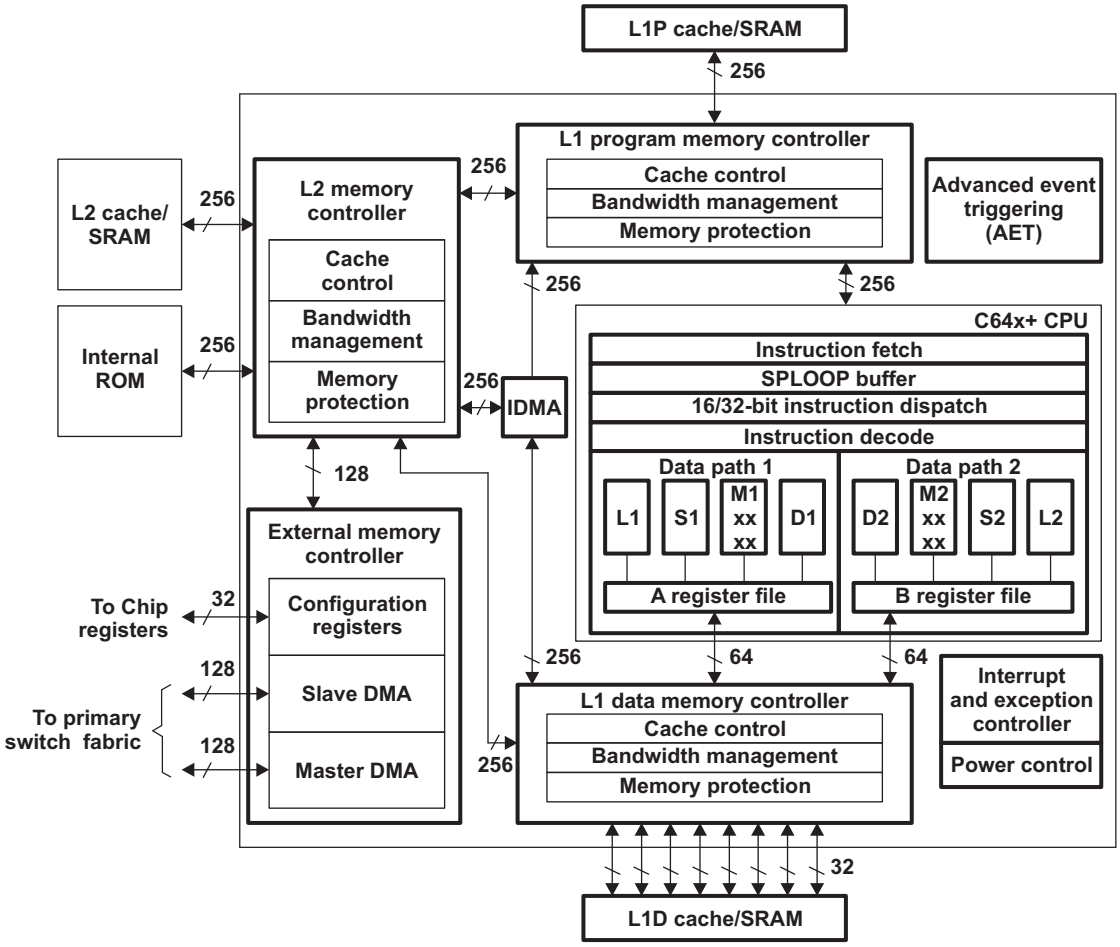

Figure 5-1. 64x+ Megamodule Block Diagram

For more detailed information on the TMS320C64x+ megamodule on the C6472 device, see the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

5.1 Memory Architecture

The TMS320C6472 device contains a 608KB level-2 memory (L2), a 32KB level-1 program memory (L1P), and a 32KB level-1 data memory (L1D).

The L1P memory configuration for the C6472 device is as follows:

- Region 0 size is 0K bytes (disabled).
- Region 1 size is 32K bytes with no wait states.

The L1D memory configuration for the C6472 device is as follows:

- Region 0 size is 0K bytes (disabled).
- Region 1 size is 32K bytes with no wait states.

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L1D is a two-way set-associative cache while L1P is a direct-mapped cache.

The L1P and L1D cache can be reconfigured via software through the L1PMODE field of the L1P Configuration Register (L1PCFG) and the L1DMODE field of the L1D Configuration Register (L1DCFG) of the C64x+ Megamodule. After device reset, L1P and L1D cache are configured as all cache or all SRAM. The on-chip Bootloader changes the reset configuration for L1P and L1D. For more information, see the *TMS320C645x/C647x Bootloader User's Guide* (literature number SPRUEC6).

Figure 5-2 and Figure 5-3 show the available SRAM/cache configurations for L1P and L1D, respectively.

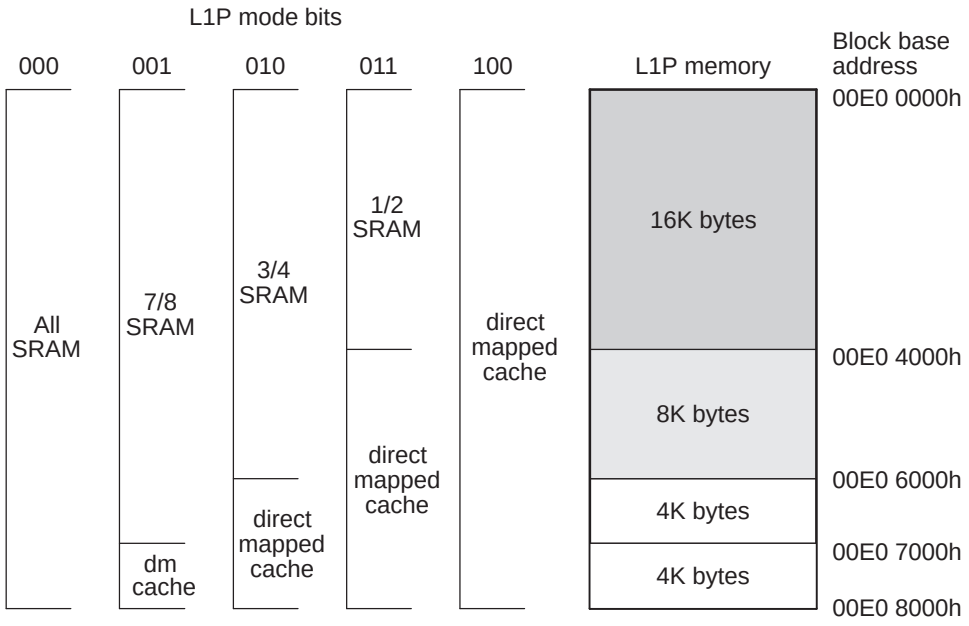

Figure 5-2. TMS320C6472 L1P Memory Configurations

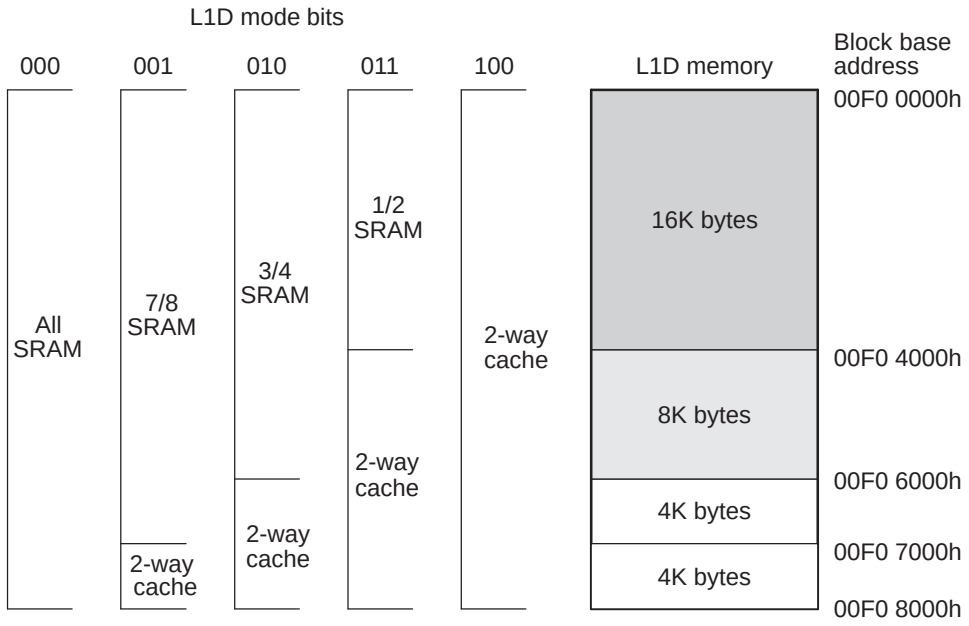

Figure 5-3. TMS320C6472 L1D Memory Configurations

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The L2 memory configuration for the C6472 device is as follows:

- Port 0 configuration:
  - Memory size is 608KB
  - Starting address is 0080 0000h
  - 2-cycle latency
  - 4 × 128-bit bank configuration
- Port 1 configuration:
  - Memory size 768K ROM, starting address is 0010 0000h
  - Memory size is 768KB shared RAM, starting address is 0020 0000h
  - 1-cycle latency
  - 4 × 256-bit bank configuration

Table 5-1. SL2 Prefetch Enabled Memory Regions

HEX ADDRESS RANGE	DESCRIPTION
ROM	
0010 0000 - 0010 FFFF	Shared Memory Controller Page 0
0011 0000 - 0011 FFFF	Shared Memory Controller Page 1
0012 0000 - 0012 FFFF	Shared Memory Controller Page 2
0013 0000 - 0013 FFFF	Shared Memory Controller Page 3
0014 0000 - 0014 FFFF	Shared Memory Controller Page 4
0015 0000 - 0015 FFFF	Shared Memory Controller Page 5
0016 0000 - 0016 FFFF	Shared Memory Controller Page 6
0017 0000 - 0017 FFFF	Shared Memory Controller Page 7
0018 0000 - 0018 FFFF	Shared Memory Controller Page 8
0019 0000 - 0019 FFFF	Shared Memory Controller Page 9
001A 0000 - 001A FFFF	Shared Memory Controller Page 10
001B 0000 - 001B FFFF	Shared Memory Controller Page 11
001C 0000 - 001F FFFF	Reserved
RAM	
0020 0000 - 0020 FFFF	Shared Memory Controller Page 16
0021 0000 - 0021 FFFF	Shared Memory Controller Page 17
0022 0000 - 0022 FFFF	Shared Memory Controller Page 18
0023 0000 - 0023 FFFF	Shared Memory Controller Page 19
0024 0000 - 0024 FFFF	Shared Memory Controller Page 20
0025 0000 - 0025 FFFF	Shared Memory Controller Page 21
0026 0000 - 0026 FFFF	Shared Memory Controller Page 22
0027 0000 - 0027 FFFF	Shared Memory Controller Page 23
0028 0000 - 0028 FFFF	Shared Memory Controller Page 24
0029 0000 - 0029 FFFF	Shared Memory Controller Page 25
002A 0000 - 002A FFFF	Shared Memory Controller Page 26
002B 0000 - 002B FFFF	Shared Memory Controller Page 27
002C 0000 - 002F FFFF	Reserved

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L2 memory can be configured as all SRAM or as part 4-way set-associative cache. The amount of L2 memory that is configured as cache is controlled through the L2MODE field of the L2 Configuration Register (L2CFG) of the C64x+ Megamodule. Figure 5-4 shows the available SRAM/cache configurations for L2. By default, L2 is configured as all SRAM after device reset.

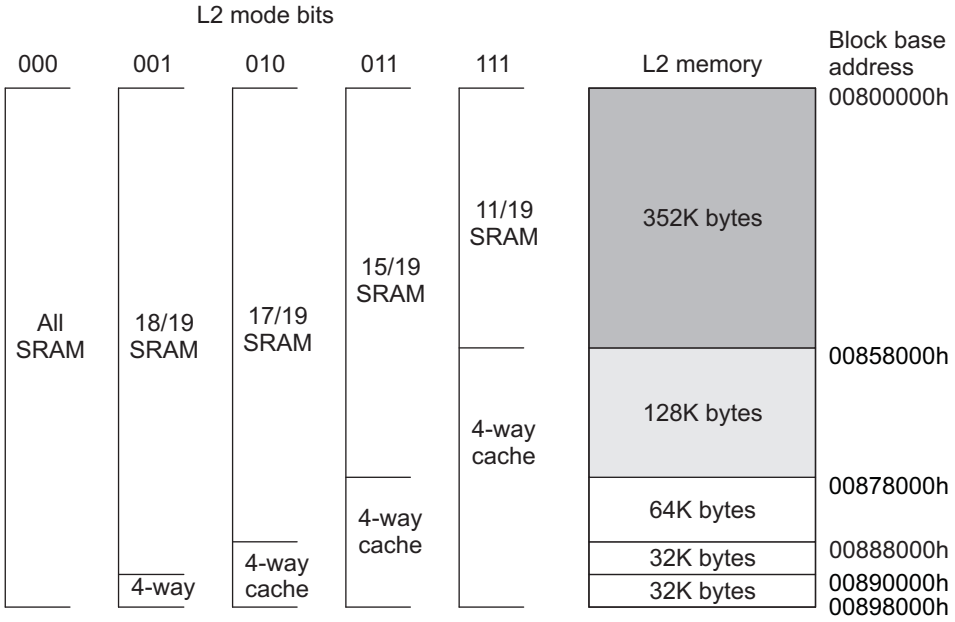

Figure 5-4. TMS320C6472 L2 Memory Configurations

For more information on the operation L1 and L2 caches, see the *TMS320C64x+ DSP Cache User's Guide* (literature number SPRU862).

All memory on the C6472 has a unique location in the memory map (see Table 2-2, *C6472 Memory Map Summary*).

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5.2 Memory Protection Support

Memory protection allows an operating system to define who or what is authorized to access L1D, L1P, and L2 memory. To accomplish this, the L1D, L1P, and L2 memories are divided into pages. There are 16 pages of L1P (2KB each), 16 pages of L1D (2KB each), and up to 64 pages of L2. The L1D, L1P, and L2 memory controllers in the C64x+ Megamodule are equipped with a set of registers that specify the permissions for each memory page. For L2, the number of protection pages and their sizes depend on the L2 configuration of the device, as defined in the previous section. The actual sizes are listed in Table 5-2.

Table 5-2 shows the memory addresses used to access the L2 memory.

Table 5-2. L2 Memory Protection Page Sizes

ADDRESS	L2					
	C64x+ MEGAMODULE CORE 0	C64x+ MEGAMODULE CORE 1	C64x+ MEGAMODULE CORE 2	C64x+ MEGAMODULE CORE 3	C64x+ MEGAMODULE CORE 4	C64x+ MEGAMODULE CORE 5
Shared L2						
0020 0000h - 002B FFFFh	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
002C 0000h - 002F FFFFh	N/A	N/A	N/A	N/A	N/A	N/A
Local L2						
0080 0000h - 0089 7FFFh	32 KB	32 KB	32 KB	32 KB	32 KB	32 KB
0089 8000h - 008F FFFFh	N/A	N/A	N/A	N/A	N/A	N/A

Each page may be assigned with fully orthogonal user and supervisor read, write, and execute permissions. Additionally, a page may be marked as either (or both) locally or globally accessible. A local access is a direct CPU access to L1D, L1P, and L2, while a global access is initiated by a DMA (either IDMA or the EDMA3) or by other system masters.

The assignment of privilege IDs for CPU 0 and all non-EDMA system masters is based on silicon revision. For silicon revisions ≤1.2, CPU 0 and all non-EDMA system masters on the device are assigned the same privilege ID of 0. For silicon revsions >1.2, CPU 0 is assigned the privilege ID of 6 and all non-EDMA system masters are assigned the same privilege ID of 0. CPUs 1-5 are each assigned a unique privilege ID (see Table 5-3). It is only possible to specify whether the memory pages are locally or globally accessible. The AIDx (x=0,1,2,3,4,5, or X) and LOCAL bits of the memory protection page attribute registers specify the memory page protection scheme as listed in Table 5-4.

Whenever the CPU is the initiator of a memory transaction, the privilege mode (user or supervisor) in which the CPU is running at that time is carried with those transactions. This includes EDMA3 transfers that are programmed by the CPU. For most peripheral masters (EMAC0, EMAC1, UTOPIA, TSIP0, TSIP1, and TSIP2), the privilege mode is always user mode. Two peripherals (HPI and SRIO) have programmable privilege modes through a chip-level register, HOSTPRIV, and can be either user or supervisor.

Table 5-3. Available Memory Page Protection Scheme with Privilege ID

PRIVID MODULE	CORRESPONDING FIELD IN MEMORY PROTECTION PAGE ATTRIBUTE REGISTERS	PRIVILEGE MODE	DESCRIPTION
0 (Core 0, silicon revisions ≤1.2)	AID0	Inherited from CPU(1)	C64x+ Megamodule Core 0
0 (not SRIO or HPI or Core 0)	AID0	User	All peripheral masters except SRIO and HPI
0 (SRIO or HPI)	AID0	User/Supervisor (configured in HOSTPRIV)	SRIO and HPI

(1) Also applies to EDMA transfers that are programmed by the CPU.

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Table 5-3. Available Memory Page Protection Scheme with Privilege ID (continued)

PRIVID MODULE	CORRESPONDING FIELD IN MEMORY PROTECTION PAGE ATTRIBUTE REGISTERS	PRIVILEGE MODE	DESCRIPTION
1	AID1	Inherited from CPU(1)	C64x+ Megamodule Core 1
2	AID2	Inherited from CPU(1)	C64x+ Megamodule Core 2
3	AID3	Inherited from CPU(1)	C64x+ Megamodule Core 3
4	AID4	Inherited from CPU(1)	C64x+ Megamodule Core 4
5	AID5	Inherited from CPU(1)	C64x+ Megamodule Core 5
6 (Core 0, silicon revisions ≤1.2)	AIDX	Reserved	Reserved
6 (Core 0, silicon revisions >1.2)	AIDX	Inherited from CPU(1)	C64x+ Megamodule Core 0
>6	AIDX	Reserved	Reserved

Table 5-4. Available Memory Page Protection Scheme with AIDx and Local Bits

PRIVID MODULE	LOCAL BIT	DESCRIPTION
0	0	No access to memory page is permitted.
0	1	Only direct access by CPU is permitted.
1	0	Only accesses by system masters and IDMA are permitted (includes EDMA and IDMA accesses initiated by the CPU).
1	1	All accesses permitted

Faults are handled by software in an interrupt (or exception, programmable within each C64x+ Megamodule interrupt controller) service routine. A CPU or DMA access to a page without the proper permissions will:

- Block the access - reads return zero, writes are voided.
- Capture the initiator in a status register - ID, address, and access type are stored.
- Signal event to CPU interrupt controller.

The software is responsible for taking corrective action to respond to the event and resetting the error status in the memory controller.

For more information on memory protection for L1D, L1P, and L2, see the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

5.3 Bandwidth Management

When multiple requestors contend for a single C64x+ Megamodule resource, the conflict is solved by granting access to the highest priority requestor. The following four resources are managed by the Bandwidth Management control hardware:

- Level 1 Program (L1P) SRAM/Cache
- Level 1 Data (L1D) SRAM/Cache
- Level 2 (L2) SRAM/Cache
- Memory-mapped registers configuration bus

The priority level for operations initiated within the C64x+ Megamodule; e.g., CPU-initiated transfers, user-programmed cache coherency operations, and IDMA-initiated transfers, are declared through registers in the C64x+ Megamodule. The priority level for operations initiated outside the C64x+ Megamodule by system peripherals is declared through the Priority Allocation Register (PRI_ALLOC), see Figure 4-2. System peripherals with no fields in PRI_ALLOC have their own registers to program their priorities.

More information on the bandwidth management features of the C64x+ Megamodule can be found in the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

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5.4 Power-Down Control

The C64x+ Megamodule supports the ability to power-down various parts of the C64x+ Megamodule. The power-down controller (PDC) of the C64x+ Megamodule can be used to power down L1P, the cache control hardware, the CPU, and the entire C64x+ Megamodule. These power-down features can be used to design systems for lower overall system power requirements.

NOTE

The C6472 does not support power-down modes for the L2 memory at this time.

More information on the power-down features of the C64x+ Megamodule can be found in the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

5.5 Megamodule Resets

Table 5-5 shows the reset types supported on the C6472 device and they affect the resetting of the Megamodule, either both globally or just locally.

Table 5-5. Megamodule Reset (Global or Local)

RESET TYPE	GLOBAL MEGAMODULE RESET	LOCAL MEGAMODULE RESET
Power-On Reset	Y	Y
Warm Reset	Y	Y
System Reset	Y	Y
CPU Reset	N	Y

For more detailed information on the global and local Megamodule resets, see the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871). For more detailed information on device resets, see Section 7.7, *Reset Controller*.

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5.6 Megamodule Revision

The version and revision of the C64x+ Megamodule can be read from the Megamodule Revision ID Register (MM_REVID) located at address 0181 2000h. The MM_REVID register is shown in Figure 5-5 and described in Table 5-6. The C64x+ Megamodule revision is dependant on the silicon revision being used. For more information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).

31	16	15	0
VERSION		REVISION(A)	
R-1h		R-n	

LEGEND: R = Read only; -*n* = value after reset

A. The C64x+ Megamodule revision is dependant on the silicon revision being used. For more information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).

Figure 5-5. Megamodule Revision ID Register (MM_REVID) [Hex Address: 0181 2000h]

Table 5-6. Megamodule Revision ID Register (MM_REVID) Field Descriptions

Bit	Field	Value	Description
31:16	VERSION	1h	Version of the C64x+ Megamodule implemented on the device. This field is always read as 1h.
15:0	REVISION		Revision of the C64x+ Megamodule version implemented on the device. The C64x+ Megamodule revision is dependant on the silicon revision being used. For more information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300).

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5.7 C64x+ Megamodule Register Descriptions

Table 5-7. Megamodule Interrupt Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	EVTFLAG0	Event Flag Register 0 (Events [31:0])
0180 0004	EVTFLAG1	Event Flag Register 1
0180 0008	EVTFLAG2	Event Flag Register 2
0180 000C	EVTFLAG3	Event Flag Register 3
0180 0010 - 0180 001C	-	Reserved
0180 0020	EVTSET0	Event Set Register 0 (Events [31:0])
0180 0024	EVTSET1	Event Set Register 1
0180 0028	EVTSET2	Event Set Register 2
0180 002C	EVTSET3	Event Set Register 3
0180 0030 - 0180 003C	-	Reserved
0180 0040	EVTCLR0	Event Clear Register 0 (Events [31:0])
0180 0044	EVTCLR1	Event Clear Register 1
0180 0048	EVTCLR2	Event Clear Register 2
0180 004C	EVTCLR3	Event Clear Register 3
0180 0050 - 0180 007C	-	Reserved
0180 0080	EVTMASK0	Event Mask Register 0 (Events [31:0])
0180 0084	EVTMASK1	Event Mask Register 1
0180 0088	EVTMASK2	Event Mask Register 2
0180 008C	EVTMASK3	Event Mask Register 3
0180 0090 - 0180 009C	-	Reserved
0180 00A0	MEVTFLAG0	Masked Event Flag Status Register 0 (Events [31:0])
0180 00A4	MEVTFLAG1	Masked Event Flag Status Register 1
0180 00A8	MEVTFLAG2	Masked Event Flag Status Register 2
0180 00AC	MEVTFLAG3	Masked Event Flag Status Register 3
0180 00B0 - 0180 00BC	-	Reserved
0180 00C0	EXPMASK0	Exception Mask Register 0 (Events [31:0])
0180 00C4	EXPMASK1	Exception Mask Register 1
0180 00C8	EXPMASK2	Exception Mask Register 2
0180 00CC	EXPMASK3	Exception Mask Register 3
0180 00D0 - 0180 00DC	-	Reserved
0180 00E0	MEXPFLAG0	Masked Exception Flag Register 0
0180 00E4	MEXPFLAG1	Masked Exception Flag Register 1
0180 00E8	MEXPFLAG2	Masked Exception Flag Register 2
0180 00EC	MEXPFLAG3	Masked Exception Flag Register 3
0180 00F0 - 0180 00FC	-	Reserved
0180 0100	-	Reserved
0180 0104	INTMUX1	Interrupt Multiplexor Register 1
0180 0108	INTMUX2	Interrupt Multiplexor Register 2
0180 010C	INTMUX3	Interrupt Multiplexor Register 3
0180 0110 - 0180 013C	-	Reserved
0180 0140	AEGMUX0	Advanced Event Generator Mux Register 0
0180 0144	AEGMUX1	Advanced Event Generator Mux Register 1
0180 0148 - 0180 017C	-	Reserved
0180 0180	INTXSTAT	Interrupt Exception Status Register
0180 0184	INTXCLR	Interrupt Exception Clear Register

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Table 5-7. Megamodule Interrupt Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0188	INTDMASK	Dropped Interrupt Mask Register
0180 0188 - 0180 01BC	-	Reserved
0180 01C0	EVTASRT	Event Asserting Register
0180 01C4 - 0180 FFFC	-	Reserved

Table 5-8. Megamodule Powerdown Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0181 0000	PDCCMD	Power-down controller command register
0181 0004 - 0181 1FFC	-	Reserved

Table 5-9. Megamodule Revision Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0181 2000	MM_REVID	Megamodule Revision ID Register
0181 2004 - 0181 2FFC	-	Reserved

Table 5-10. Megamodule IDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0182 0000	IDMA0STAT	IDMA Channel 0 Status Register
0182 0004	IDMA0MASK	IDMA Channel 0 Mask Register
0182 0008	IDMA0SRC	IDMA Channel 0 Source Address Register
0182 000C	IDMA0DST	IDMA Channel 0 Destination Address Register
0182 0010	IDMA0CNT	IDMA Channel 0 Count Register
0182 0014 - 0182 00FC	-	Reserved
0182 0100	IDMA1STAT	IDMA Channel 1 Status Register
0182 0104	-	Reserved
0182 0108	IDMA1SRC	IDMA Channel 1 Source Address Register
0182 010C	IDMA1DST	IDMA Channel 1 Destination Address Register
0182 0110	IDMA1CNT	IDMA Channel 1 Count Register
0182 0114 - 0182 01FC	-	Reserved

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Table 5-11. Megamodule Cache Configuration Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 0000	L2CFG	L2 Cache Configuration Register
0184 0004 - 0184 001C	-	Reserved
0184 0020	L1PCFG	L1P Configuration Register
0184 0024	L1PCC	L1P Cache Control Register
0184 0028 - 0184 003C	-	Reserved
0184 0040	L1DCFG	L1D Configuration Register
0184 0044	L1DCC	L1D Cache Control Register
0184 0048 - 0184 0FFC	-	Reserved
0184 1000 - 0184 104C	-	See Table 5-14, *CPU Megamodule Bandwidth Management Registers*
0184 1050 - 0184 3FFC	-	Reserved
0184 4000	L2WBAR	L2 Writeback Base Address Register - for Block Writebacks
0184 4004	L2WWC	L2 Writeback Word Count Register
0184 4008 - 0184 400C	-	Reserved
0184 4010	L2WIBAR	L2 Writeback and Invalidate Base Address Register - for Block Writebacks
0184 4014	L2WIWC	L2 Writeback and Invalidate word count register
0184 4018	L2IBAR	L2 Invalidate Base Address Register
0184 401C	L2IWC	L2 Invalidate Word Count Register
0184 4020	L1PIBAR	L1P Invalidate Base Address Register
0184 4024	L1PIWC	L1P Invalidate Word Count Register
0184 4030	L1DWIBAR	L1D Writeback and Invalidate Base Address Register
0184 4034	L1DWIWC	L1D Writeback and Invalidate Word Count Register
0184 4038	-	Reserved
0184 4040	L1DWBAR	L1D Writeback Base Address Register - for Block Writebacks
0184 4044	L1DWWC	L1D Writeback Word Count Register
0184 4048	L1DIBAR	L1D Invalidate Base Address Register
0184 404C	L1DIWC	L1D Invalidate Word Count Register
0184 4050 - 0184 4FFC	-	Reserved
0184 5000	L2WB	L2 Global Writeback Register
0184 5004	L2WBINV	L2 Global Writeback and Invalidate Register
0184 5008	L2INV	L2 Global Invalidate Register
0184 500C - 0184 5024	-	Reserved
0184 5028	L1PINV	L1P Global Invalidate Register
0184 502C - 0184 503C	-	Reserved
0184 5040	L1DWB	L1D Global Writeback Register
0184 5044	L1DWBINV	L1D Global Writeback and Invalidate Register
0184 5048	L1DINV	L1D Global Invalidate Register
0184 504C - 0184 5FFC	-	Reserved
0184 6000 - 0184 640C	-	See Table 5-12, *Megamodule Error Detection Correct Registers*
0184 6410 - 0184 7FFC	-	Reserved
0184 8000 - 0184 803C	-	Reserved
0184 8040	MAR16	Controls C64x+ Subsystem 0 Range 1000 0000 - 10FF FFFF
0184 8044	MAR17	Controls C64x+ Subsystem 1 Range 1100 0000 - 11FF FFFF
0184 8048	MAR18	Controls C64x+ Subsystem 2 Range 1200 0000 - 12FF FFFF
0184 804C	MAR19	Controls C64x+ Subsystem 3 Range 1300 0000 - 13FF FFFF
0184 8050	MAR20	Controls C64x+ Subsystem 4 Range 1400 0000 - 14FF FFFF
0184 8054	MAR21	Controls C64x+ Subsystem 5 Range 1500 0000 - 15FF FFFF
0184 8058 - 0184 837C	-	Reserved

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Table 5-11. Megamodule Cache Configuration Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 8380	MAR224	Controls DDR2 Range E000 0000 - E0FF FFFF
0184 8384	MAR225	Controls DDR2 Range E100 0000 - E1FF FFFF
0184 8388	MAR226	Controls DDR2 Range E200 0000 - E2FF FFFF
0184 838C	MAR227	Controls DDR2 Range E300 0000 - E3FF FFFF
0184 8390	MAR228	Controls DDR2 Range E400 0000 - E4FF FFFF
0184 8394	MAR229	Controls DDR2 Range E500 0000 - E5FF FFFF
0184 8398	MAR230	Controls DDR2 Range E600 0000 - E6FF FFFF
0184 839C	MAR231	Controls DDR2 Range E700 0000 - E7FF FFFF
0184 83A0	MAR232	Controls DDR2 Range E800 0000 - E8FF FFFF
0184 83A4	MAR233	Controls DDR2 Range E900 0000 - E9FF FFFF
0184 83A8	MAR234	Controls DDR2 Range EA00 0000 - EAFF FFFF
0184 83AC	MAR235	Controls DDR2 Range EB00 0000 - EBFF FFFF
0184 83B0	MAR236	Controls DDR2 Range EC00 0000 - ECFF FFFF
0184 83B4	MAR237	Controls DDR2 Range ED00 0000 - EDFF FFFF
0184 83B8	MAR238	Controls DDR2 Range EE00 0000 - EEFF FFFF
0184 83BC	MAR239	Controls DDR2 Range EF00 0000 - EFFF FFFF
0184 83C0	MAR240	Controls DDR2 Range F000 0000 - F0FF FFFF
0184 83C4	MAR241	Controls DDR2 Range F100 0000 - F1FF FFFF
0184 83C8	MAR242	Controls DDR2 Range F200 0000 - F2FF FFFF
0184 83CC	MAR243	Controls DDR2 Range F300 0000 - F3FF FFFF
0184 83D0	MAR244	Controls DDR2 Range F400 0000 - F4FF FFFF
0184 83D4	MAR245	Controls DDR2 Range F500 0000 - F5FF FFFF
0184 83D8	MAR246	Controls DDR2 Range F600 0000 - F6FF FFFF
0184 83DC	MAR247	Controls DDR2 Range F700 0000 - F7FF FFFF
0184 83E0	MAR248	Controls DDR2 Range F800 0000 - F8FF FFFF
0184 83E4	MAR249	Controls DDR2 Range F900 0000 - F9FF FFFF
0184 83E8	MAR250	Controls DDR2 Range FA00 0000 - FAFF FFFF
0184 83EC	MAR251	Controls DDR2 Range FB00 0000 - FBFF FFFF
0184 83F0	MAR252	Controls DDR2 Range FC00 0000 - FCFF FFFF
0184 83F4	MAR253	Controls DDR2 Range FD00 0000 - FDFF FFFF
0184 83F8	MAR254	Controls DDR2 Range FE00 0000 - FEFF FFFF
0184 83FC	MAR255	Controls DDR2 Range FF00 0000 - FFFF FFFF

Table 5-12. Megamodule Error Detection Correct Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 6000	-	Reserved
0184 6004	L2EDSTAT	L2 Error Detection Status Register
0184 6008	L2EDCMD	L2 Error Detection Command Register
0184 600C	L2EDADDR	L2 Error Detection Address Register
0184 6010	L2EDEN0	L2 Error Detection Enable Map 0 Register
0184 6014	L2EDEN1	L2 Error Detection Enable Map 1 Register
0184 6018	L2EDCPEC	L2 Error Detection - Correctable Parity Error Count Register
0184 601C	L2EDNPEC	L2 Error Detection - Non-Correctable Parity Error Count Register
0184 6020 - 0184 6400	-	Reserved
0184 6404	L1PEDSTAT	L1P Error Detection Status Register
0184 6408	L1PEDCMD	L1P Error Detection Command Register
0184 640C	L1PEDADDR	L1P Error Detection Address Register

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Table 5-13. Megamodule L1/L2 Memory Protection Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A000	L2MPFAR	L2 Memory Protection Fault Address Register
0184 A004	L2MPFSR	L2 Memory Protection Fault Status Register
0184 A008	L2MPFCR	L2 Memory Protection Fault Command Register
0184 A00C - 0184 A0FC	-	Reserved
0184 A100	L2MPLK0	L2 Memory Protection Lock Key Bits [31:0]
0184 A104	L2MPLK1	L2 Memory Protection Lock Key Bits [63:32]
0184 A108	L2MPLK2	L2 Memory Protection Lock Key Bits [95:64]
0184 A10C	L2MPLK3	L2 Memory Protection Lock Key Bits [127:96]
0184 A110	L2MPLKCMD	L2 Memory Protection Lock Key Command Register
0184 A114	L2MPLKSTAT	L2 Memory Protection Lock Key Status Register
0184 A118 - 0184 A1FC	-	Reserved
0184 A200	L2MPPA0	L2 Memory Protection Page Attribute Register 0 0080 0000 - 0080 7FFF
0184 A204	L2MPPA1	L2 Memory Protection Page Attribute Register 1 0080 8000 - 0080 FFFF
0184 A208	L2MPPA2	L2 Memory Protection Page Attribute Register 2 0081 0000 - 0081 7FFF
0184 A20C	L2MPPA3	L2 Memory Protection Page Attribute Register 3 0081 8000 - 0081 FFFF
0184 A210	L2MPPA4	L2 Memory Protection Page Attribute Register 4 0082 0000 - 0082 7FFF
0184 A214	L2MPPA5	L2 Memory Protection Page Attribute Register 5 0082 8000 - 0082 FFFF
0184 A218	L2MPPA6	L2 Memory Protection Page Attribute Register 6 0083 0000 - 0083 7FFF
0184 A21C	L2MPPA7	L2 Memory Protection Page Attribute Register 7 0083 8000 - 0083 FFFF
0184 A220	L2MPPA8	L2 Memory Protection Page Attribute Register 8 0084 0000 - 0084 7FFF
0184 A224	L2MPPA9	L2 Memory Protection Page Attribute Register 9 0084 8000 - 0084 FFFF
0184 A228	L2MPPA10	L2 Memory Protection Page Attribute Register 10 0085 0000 - 0085 7FFF
0184 A22C	L2MPPA11	L2 Memory Protection Page Attribute Register 11 0085 8000 - 0085 FFFF
0184 A230	L2MPPA12	L2 Memory Protection Page Attribute Register 12 0086 0000 - 0086 7FFF
0184 A234	L2MPPA13	L2 Memory Protection Page Attribute Register 13 0086 8000 - 0086 FFFF
0184 A238	L2MPPA14	L2 Memory Protection Page Attribute Register 14 0087 0000 - 0087 7FFF
0184 A23C	L2MPPA15	L2 Memory Protection Page Attribute Register 15 0087 8000 - 0087 FFFF
0184 A240	L2MPPA16	L2 Memory Protection Page Attribute Register 16 0088 0000 - 0088 7FFF
0184 A244	L2MPPA17	L2 Memory Protection Page Attribute Register 17 0088 8000 - 0088 FFFF
0184 A248	L2MPPA18	L2 Memory Protection Page Attribute Register 18 0089 0000 - 0089 7FFF
0184 A24C	L2MPPA19	L2 Memory Protection Page Attribute Register 19 Reserved
0184 A250	L2MPPA20	L2 Memory Protection Page Attribute Register 20 Reserved

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Table 5-13. Megamodule L1/L2 Memory Protection Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A254	L2MPPA21	L2 Memory Protection Page Attribute Register 21 Reserved
0184 A258	L2MPPA22	L2 Memory Protection Page Attribute Register 22 Reserved
0184 A25C	L2MPPA23	L2 Memory Protection Page Attribute Register 23 Reserved
0184 A260	L2MPPA24	L2 Memory Protection Page Attribute Register 24 Reserved
0184 A264	L2MPPA25	L2 Memory Protection Page Attribute Register 25 Reserved
0184 A268	L2MPPA26	L2 Memory Protection Page Attribute Register 26 Reserved
0184 A26C	L2MPPA27	L2 Memory Protection Page Attribute Register 27 Reserved
0184 A270	L2MPPA28	L2 Memory Protection Page Attribute Register 28 Reserved
0184 A274	L2MPPA29	L2 Memory Protection Page Attribute Register 29 Reserved
0184 A278	L2MPPA30	L2 Memory Protection Page Attribute Register 30 Reserved
0184 A27C	L2MPPA31	L2 Memory Protection Page Attribute Register 31 Reserved
0184 A280	L2MPPA32	L2 Memory Protection Page Attribute Register 32 0020 0000 - 0020 FFFF
0184 A284	L2MPPA33	L2 Memory Protection Page Attribute Register 33 0021 0000 - 0021 FFFF
0184 A288	L2MPPA34	L2 Memory Protection Page Attribute Register 34 0022 0000 - 0022 FFFF
0184 A28C	L2MPPA35	L2 Memory Protection Page Attribute Register 35 0023 0000 - 0023 FFFF
0184 A290	L2MPPA36	L2 Memory Protection Page Attribute Register 36 0024 0000 - 0024 FFFF
0184 A294	L2MPPA37	L2 Memory Protection Page Attribute Register 37 0025 0000 - 0025 FFFF
0184 A298	L2MPPA38	L2 Memory Protection Page Attribute Register 38 0026 0000 - 0026 FFFF
0184 A29C	L2MPPA39	L2 Memory Protection Page Attribute Register 39 0027 0000 - 0027 FFFF
0184 A2A0	L2MPPA40	L2 Memory Protection Page Attribute Register 40 0028 0000 - 0028 FFFF
0184 A2A4	L2MPPA41	L2 Memory Protection Page Attribute Register 41 0029 0000 - 0029 FFFF
0184 A2A8	L2MPPA42	L2 Memory Protection Page Attribute Register 42 002A 0000 - 002A FFFF
0184 A2AC	L2MPPA43	L2 Memory Protection Page Attribute Register 43 002B 0000 - 002B FFFF
0184 A2B0	L2MPPA44	L2 Memory Protection Page Attribute Register 44 Reserved
0184 A2B4	L2MPPA45	L2 Memory Protection Page Attribute Register 45 Reserved
0184 A2B8	L2MPPA46	L2 Memory Protection Page Attribute Register 46 Reserved
0184 A2BC	L2MPPA47	L2 Memory Protection Page Attribute Register 47 Reserved
0184 A2C0	L2MPPA48	L2 Memory Protection Page Attribute Register 48 Reserved

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Table 5-13. Megamodule L1/L2 Memory Protection Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A2C4	L2MPPA49	L2 Memory Protection Page Attribute Register 49 Reserved
0184 A2C8	L2MPPA50	L2 Memory Protection Page Attribute Register 50 Reserved
0184 A2CC	L2MPPA51	L2 Memory Protection Page Attribute Register 51 Reserved
0184 A2D0	L2MPPA52	L2 Memory Protection Page Attribute Register 52 Reserved
0184 A2D4	L2MPPA53	L2 Memory Protection Page Attribute Register 53 Reserved
0184 A2D8	L2MPPA54	L2 Memory Protection Page Attribute Register 54 Reserved
0184 A2DC	L2MPPA55	L2 Memory Protection Page Attribute Register 55 Reserved
0184 A2E0	L2MPPA56	L2 Memory Protection Page Attribute Register 56 Reserved
0184 A2E4	L2MPPA57	L2 Memory Protection Page Attribute Register 57 Reserved
0184 A2E8	L2MPPA58	L2 Memory Protection Page Attribute Register 58 Reserved
0184 A2EC	L2MPPA59	L2 Memory Protection Page Attribute Register 59 Reserved
0184 A2F0	L2MPPA60	L2 Memory Protection Page Attribute Register 60 Reserved
0184 A2F4	L2MPPA61	L2 Memory Protection Page Attribute Register 61 Reserved
0184 A2F8	L2MPPA62	L2 Memory Protection Page Attribute Register 62 Reserved
0184 A2FC	L2MPPA63	L2 Memory Protection Page Attribute Register 63 Reserved
0184 A300 - 0184 A3FC	-	Reserved
0184 A400	L1PMPFAR	L1 Program (L1P) Memory Protection Fault Address Register
0184 A404	L1PMPFSR	L1P Memory Protection Fault Status Register
0184 A408	L1PMPFCR	L1P Memory Protection Fault Command Register
0184 A40C - 0184 A4FC	-	Reserved
0184 A500	L1PMPLK0	L1P Memory Protection Lock Key Bits [31:0]
0184 A504	L1PMPLK1	L1P Memory Protection Lock Key Bits [63:32]
0184 A508	L1PMPLK2	L1P Memory Protection Lock Key Bits [95:64]
0184 A50C	L1PMPLK3	L1P Memory Protection Lock Key Bits [127:96]
0184 A510	L1PMPLKCMD	L1P Memory Protection Lock Key Command Register
0184 A514	L1PMPLKSTAT	L1P Memory Protection Lock Key Status Register
0184 A518 - 0184 A63C	-	Reserved
0184 A640	L1PMPPA16	L1P Memory Protection Page Attribute Register 16 00E0 0000 - 00E0 07FF
0184 A644	L1PMPPA17	L1P Memory Protection Page Attribute Register 17 00E0 0800 - 00E0 0FFF
0184 A648	L1PMPPA18	L1P Memory Protection Page Attribute Register 18 00E0 1000 - 00E0 17FF
0184 A64C	L1PMPPA19	L1P Memory Protection Page Attribute Register 19 00E0 1800 - 00E0 1FFF
0184 A650	L1PMPPA20	L1P Memory Protection Page Attribute Register 20 00E0 2000 - 00E0 27FF
0184 A654	L1PMPPA21	L1P Memory Protection Page Attribute Register 21 00E0 2800 - 00E0 2FFF

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Table 5-13. Megamodule L1/L2 Memory Protection Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A658	L1PMPPA22	L1P Memory Protection Page Attribute Register 22 00E0 3000 - 00E0 37FF
0184 A65C	L1PMPPA23	L1P Memory Protection Page Attribute Register 23 00E0 3800 - 00E0 3FFF
0184 A660	L1PMPPA24	L1P Memory Protection Page Attribute Register 24 00E0 4000 - 00E0 47FF
0184 A664	L1PMPPA25	L1P Memory Protection Page Attribute Register 25 00E0 4800 - 00E0 4FFF
0184 A668	L1PMPPA26	L1P Memory Protection Page Attribute Register 26 00E0 5000 - 00E0 57FF
0184 A66C	L1PMPPA27	L1P Memory Protection Page Attribute Register 27 00E0 5800 - 00E0 5FFF
0184 A670	L1PMPPA28	L1P Memory Protection Page Attribute Register 28 00E0 6000 - 00E0 67FF
0184 A674	L1PMPPA29	L1P Memory Protection Page Attribute Register 29 00E0 6800 - 00E0 6FFF
0184 A678	L1PMPPA30	L1P Memory Protection Page Attribute Register 30 00E0 7000 - 00E0 77FF
0184 A67C	L1PMPPA31	L1P Memory Protection Page Attribute Register 31 00E0 7800 - 00E0 7FFF
0184 A680 - 0184 ABFF	-	Reserved
0184 AC00	L1DMPFAR	L1 Data (L1D) Memory Protection Fault Address Register
0184 AC04	L1DMPFSR	L1D Memory Protection Fault Status Register
0184 AC08	L1DMPFCR	L1D Memory Protection Fault Command Register
0184 AC0C - 0184 ACFC	-	Reserved
0184 AD00	L1DMPLK0	L1D Memory Protection Lock Key Bits [31:0]
0184 AD04	L1DMPLK1	L1D Memory Protection Lock Key Bits [63:32]
0184 AD08	L1DMPLK2	L1D Memory Protection Lock Key Bits [95:64]
0184 AD0C	L1DMPLK3	L1D Memory Protection Lock Key Bits [127:96]
0184 AD10	L1DMPLKCMD	L1D Memory Protection Lock Key Command Register
0184 AD14	L1DMPLKSTAT	L1D Memory Protection Lock Key Status Register
0184 AD18 - 0184 AE3C	-	Reserved
0184 AE40	L1DMPPA16	L1D Memory Protection Page Attribute Register 16 00F0 0000 - 00F0 07FF
0184 AE44	L1DMPPA17	L1D Memory Protection Page Attribute Register 17 00F0 0800 - 00F0 0FFF
0184 AE48	L1DMPPA18	L1D Memory Protection Page Attribute Register 18 00F0 1000 - 00F0 17FF
0184 AE4C	L1DMPPA19	L1D Memory Protection Page Attribute Register 19 00F0 1800 - 00F0 1FFF
0184 AE50	L1DMPPA20	L1D Memory Protection Page Attribute Register 20 00F0 2000 - 00F0 27FF
0184 AE54	L1DMPPA21	L1D Memory Protection Page Attribute Register 21 00F0 2800 - 00F0 2FFF
0184 AE58	L1DMPPA22	L1D Memory Protection Page Attribute Register 22 00F0 3000 - 00F0 37FF
0184 AE5C	L1DMPPA23	L1D Memory Protection Page Attribute Register 23 00F0 3800 - 00F0 3FFF
0184 AE60	L1DMPPA24	L1D Memory Protection Page Attribute Register 24 00F0 4000 - 00F0 47FF
0184 AE64	L1DMPPA25	L1D Memory Protection Page Attribute Register 25 00F0 4800 - 00F0 4FFF
0184 AE68	L1DMPPA26	L1D Memory Protection Page Attribute Register 26 00F0 5000 - 00F0 57FF

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Table 5-13. Megamodule L1/L2 Memory Protection Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 AE6C	L1DMPPA27	L1D Memory Protection Page Attribute Register 27 00F0 5800 - 00F0 5FFF
0184 AE70	L1DMPPA28	L1D Memory Protection Page Attribute Register 28 00F0 6000 - 00F0 67FF
0184 AE74	L1DMPPA29	L1D Memory Protection Page Attribute Register 29 00F0 6800 - 00F0 6FFF
0184 AE78	L1DMPPA30	L1D Memory Protection Page Attribute Register 30 00F0 7000 - 00F0 77FF
0184 AE7C	L1DMPPA31	L1D Memory Protection Page Attribute Register 31 00F0 7800 - 00F0 7FFF
0184 AE80 - 0185 FFFF	-	Reserved

Table 5-14. CPU Megamodule Bandwidth Management Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0182 0200	EMCCPUARBE	EMC CPU Arbitration Control Register
0182 0204	EMCIDMAARBE	EMC IDMA Arbitration Control Register
0182 0208	EMCSDMAARBE	EMC Slave DMA Arbitration Control Register
0182 020C	EMCMDMAARBE	EMC Master DMA Arbitration Control Resgiter
0182 0210 - 0182 02FC	-	Reserved
0184 1000	L2DCPUARBU	L2D CPU Arbitration Control Register
0184 1004	L2DIDMAARBU	L2D IDMA Arbitration Control Register
0184 1008	L2DSDMAARBU	L2D Slave DMA Arbitration Control Register
0184 100C	L2DUCARBU	L2D User Coherence Arbitration Control Resgiter
0184 1010 - 0184 103C	-	Reserved
0184 1040	L1DCPUARBD	L1D CPU Arbitration Control Register
0184 1044	L1DIDMAARBD	L1D IDMA Arbitration Control Register
0184 1048	L1DSDMAARBD	L1D Slave DMA Arbitration Control Register
0184 104C	L1DUCARBD	L1D User Coherence Arbitration Control Resgiter

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5.8 CPU Revision ID

Each 64x+ Megamodule contains a 64x+ CPU processing core. This 64x+ CPU processing core also contains an additional CPU ID and Revision ID independent from the Megamodule Revision ID. It is contained in the control status resister (CSR) which is part of the control register file within the CPU core. The CPU ID field (bits 31:24) identifies the CPU core as 64x+ by returning the value 10h when read. The REVISION ID field (bits 23:16) returns the value 00h when read. For more CPU Revision ID related information, see the *TMS320C6472 Digital Signal Processor Silicon Errata* (literature number SPRZ300). For more CPU CSR related information, see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732).

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6 Device Operating Conditions

6.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted)(1)(2)(3)

Supply voltage range:	CV_{DD}	-0.5 V to 1.5 V
	CV_{DD2}	-0.5 V to 1.5 V
	DV_{DD33}	-0.5 V to 4.2 V
	DV_{DD18}, AV_{DDA3}, AV_{DDA4}	-0.5 V to 2.5 V
	AV_{DDA1}, AV_{DDA2}	-0.5 V to 2.5 V
	DV_{DD15}	-0.5 V to 2.5 V
	DV_{DDR}	-0.5 V to 2.5 V
	CV_{DD1}	-0.5 V to 1.5 V
	AV_{DDA}, DV_{DDD}, AV_{DDT}	-0.5 V to 1.5 V
Input voltage (V_I) range:	3.3-V pins	-0.5 V to DV_{DD33} + 0.5 V
	RGMII pins	-0.3 V to DV_{DD15} + 0.3 V
	DDR2 memory controller pins	-0.3 V to DV_{DD18} + 0.3 V
	RIO pins	0 V to 1.32 V
Output voltage (V_O) range:	3.3-V pins	-0.5 V to DV_{DD33} + 0.5 V
	RGMII pins	-0.3 V to DV_{DD15} + 0.3 V
	DDR2 memory controller pins	-0.3 V to DV_{DD18} + 0.3 V
	RIO pins	0 V to 1.32 V
Operating case temperature range, T_C:	Standard	0°C to 85°C
	A version(4)	-40°C to 100°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.
(3) Overshoot and undershoot transients due to impedance mismatch on 3.3-V pins can be up to 30% of the supply voltage for up to 30% of the signal period without significantly impacting reliability. For RGMII and DDR2 pins, limit overshoot/undershoot to 20% of supply voltage for up to 20% of the duty cycle. These period limits assume continuous operation.
(4) Extended temperature (A version) range is available only on 500-MHz and 625-MHz devices.

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6.2 Recommended Operating Conditions[1]

PARAMETER			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core	500 MHz	0.95	1.0	1.05	V
		625 MHz	1.05	1.1	1.16	
		700 MHz	1.14	1.2	1.26	
CV_{DD2}	Supply voltage, SRIO Core	500 MHz	0.95	1.0	1.05	V
		625 MHz	1.05	1.1	1.16	
		700 MHz	1.14	1.2	1.26	
CV_{DD1}	Supply volttage, 1.2-V DDR Core		1.14	1.2	1.26	V
DV_{DD33}	Supply voltage, 3.3-V I/O		3.135	3.3	3.465	V
DV_{DD18}	Supply voltage, 1.8-V I/O (DDR)		1.71	1.8	1.89	V
DV_{DD15}	Supply voltage, 1.8-V/1.5-V I/O (RGMII)		1.4		1.9	V
$V_{REFHSTL}$ ($0.5 * DV_{DD15}$)	Reference voltage, RGMII I/O		0.7		0.95	V
$V_{REFSSTL}$ ($0.5 * DV_{DD18}$)	Reference voltage, DDR2 I/O		0.855	0.9	0.945	V
AV_{DDA1}	Analog supply voltage, PLL1 (System PLL)		1.71	1.8	1.89	V
AV_{DDA2}	Analog supply voltage, PLL2 (EMAC PLL)		1.71	1.8	1.89	V
AV_{DDA3}	Analog supply voltage, PLL3 (DDR PLL)		1.71	1.8	1.89	V
AV_{DDA4}	Analog supply voltage, DDR		1.71	1.8	1.89	V
DV_{DDD}	SRIO Digital supply voltage		1.14	1.2	1.26	V
AV_{DDA}	SRIO Analog supply voltage		1.14	1.2	1.26	V
AV_{DDT}	SRIO Termination voltage		1.14	1.2	1.26	V
DV_{DDR}	SRIO Regulator supply voltage		1.35	1.5/1.8	1.98	V
V_{IH}	High-level input voltage	3.3-V pins (except I2C pins)	2.0		DV_{DD33} + 0.5	V
		I2C pins	0.7 * DV_{DD33}		DV_{DD33} + 0.5	
		RGMII pins	$V_{REFHSTL}$ + 0.10		DV_{DD15} + 0.3	
		DDR2 memory controller pins	$V_{REFSSTL}$ + 0.125		DV_{DD18} + 0.3	
V_{IL}	Low-level input voltage	3.3-V pins (except I2C pins)	-0.5		0.8	V
		I2C pins	-0.5		0.3 * DV_{DD33}	
		RGMII pins	-0.3		$V_{REFHSTL}$ - 0.1	
		DDR2 memory controller pins	-0.3		$V_{REFSSTL}$ - 0.125	
P_{CDD}	Core supply power[2]	CV_{DD} = CV_{DD2} = 1.0 V, CPU frequency = 500 MHz		2.38		W
		CV_{DD} = CV_{DD2} = 1.1 V, CPU frequency = 625 MHz		3.76		
		CV_{DD} = CV_{DD2} = 1.2 V, CPU frequency = 700 MHz		5.42		

(1) Operating conditions are at 500 MHz, 625 MHz, or 700 MHz.
(2) Assumes the following conditions: CPU utilization 30% DSP/60% control; DDR2 at 30% utilization (266 MHz), 35% writes, 32 bits, 15% bit switching; TSIP0, TSIP1, and TSIP2 at 20% utilization, 15% switching; UTOPIA 50 MHz, 16-bit at 50% utilization, 15% switching EMAC0, 1000 Mbps, RGMII, 50% utilization, 50% switching; EMAC1 disabled; SRIO both lanes disabled; all timers active; HPI disabled; I2C enabled at 10% utilization; room temperature (25°C). The actual power consumption is application-dependent. For more details on core and I/O activity, see the *TMS320C6472/TMS320TCI6486 Power Consumption Summary* (literature number SPRAAS4).

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Recommended Operating Conditions[1] *(continued)*

PARAMETER			MIN	NOM	MAX	UNIT
P_{DDD}	I/O supply power[2]	3.3-V Supply (DV_{DD33})		0.2		W
		1.8-V Supplies, including PLLs (DV_{DD18}, AV_{DDA1}, AV_{DDA2}, AV_{DDA3}, AV_{DDA4}		0.26		
		1.5-V Supplies (DV_{DD15}, DV_{DDR})		0.05		
		1.2-V Supplies (CV_{DD1}, AV_{DDA}, DV_{DDD}, AV_{DDT})		0.28		

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6.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{OH}	High-level ouput voltage	3.3 V pins (except I2C pins)	DV_{DD33} = MIN, I_{OH} = MAX	0.8 * DV_{DD33}			V
		I2C pins	DV_{DD33} = MIN, I_{OH} = MAX	0.8 * DV_{DD33}			V
		RGMII pins		DV_{DD15} - 0.4			V
		DDR2 memory controller pins		DV_{DD18} - 0.4			V
V_{OL}	Low-level ouput voltage	3.3-V pins (except I2C pins)	DV_{DD33} = MIN, I_{OL} = MAX			0.4	V
		I2C pins	Pulled up to 3.3 V, 3 mA sink current			0.4	V
		RGMII pins				0.4	V
		DDR2 memory controller pins				0.4	V
I_I	Input current (DC)	3.3-V pins (except I2C pins)	V_I = V_{SS} to DV_{DD33}, pins without internal pull-up or pull-down resistor	-1		1	uA
			V_I = V_{SS} to DV_{DD33}, pins with internal pull-up resistor	50	100	400	uA
			V_I = V_{SS} to DV_{DD33}, pins with internal pull-down resistor	-400	-100	-50	uA
		I2C pins	0.1 * DV_{DD33} ≤ V_I ≤ 0.9 * DV_{DD33}	-10		10	uA
		RGMII pins		-1		1	uA
		DDR2 memory controller pins		-1		1	uA
I_{OH}	High-level output current	E Class Buffers - EMU[18:0] and all 3.3-V Ethernet, except MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				-7	mA
		D Class Buffers - GPIO[15:0], TDO, HOUT, and SYSCLKOUT				-3	mA
		C Class Buffers - HPI, TSIP, UTOPIA, BOOTACTIVE, WDOUT, RESETSTAT, TIMO2, MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				-3	mA
		RGMII pins				-8	mA
		DDR pins				-13.4	mA

(1) For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

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Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature (Unless Otherwise Noted) *(continued)*

PARAMETER			TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	E Class Buffers - EMU[18:0] and all 3.3-V Ethernet, except MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				7	mA
		D Class Buffers - GPIO[15:0], TDO, HOUT, and SYSCLKOUT				3	mA
		C Class Buffers - HPI, TSIP, UTOPIA, BOOTACTIVE, WDOUT, RESETSTAT, TIMO2, MCRS0_RMCRSDV0, MCOL0, GMDIO, and GMDCLK				3	mA
		RGMII pins				8	mA
		DDR pins				13.4	mA
I_{OZ}	Off-state output current	3.3-V pins		-10		20	uA
		RGMII pins		-10		10	uA
		DDR pins		-10		10	uA
T_C	Operating case temperature	commercial temperature		0		85	°C
		extended temperature(2)		-40		100	

(2) Extended temperature (A) range is available only on 500-MHz and 625-MHz devices.

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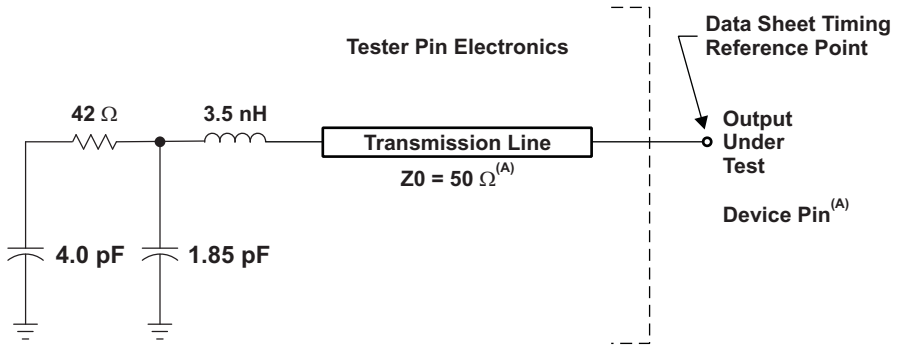
7 C64x+ Peripheral Information and Electrical Specifications

7.1 Parameter Information



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings. Input requirements in this data sheet are tested with an input slew rate of ≤ 4 Volts per nanosecond (V/ns) at the device pin.

Figure 7-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.1.1 3.3-V Signal Transition Levels

All input and output timing parameters are referenced to 1.5 V for both "0" and "1" logic levels.

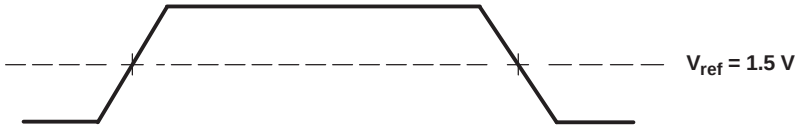


Figure 7-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL}MAX and V_{OH} MIN for output clocks.

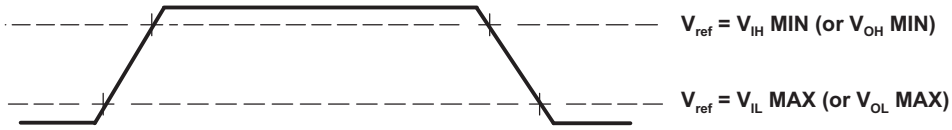


Figure 7-3. Rise and Fall Transition Time Voltage Reference Levels

7.1.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of ≤4 Volts per nanosecond (V/ns).

7.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data sheet do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be

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adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

7.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

7.3 Power Supplies

7.3.1 Power-Supply Sequencing

TI recommends the power-supply sequence options shown in Figure 7-4 and Figure 7-5. For Option 2, after the DV_{DD33} supply is stable, the remaining power supplies can be powered up at the same time as CV_{DD} as long as their supply voltage never exceeds the CV_{DD} voltage until CV_{DD} is stable. Note that the word *stable* means voltages that have reached a valid level as described in Section 6.2. Some TI power-supply devices include an "auto-track" feature that can be used to ensure multiple supply outputs ramp at the same time to prevent one being higher than another during startup. In all of these sequencing requirements, the intent is to prevent a subsequent power supply voltage from exceeding a previous power supply until the previous supply has reached a stable value.

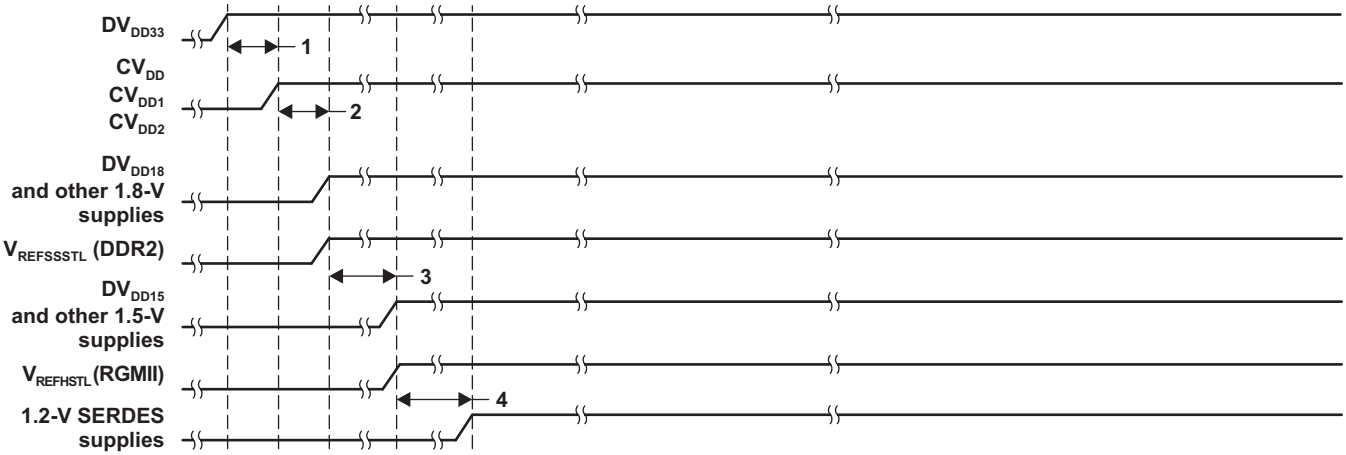

Figure 7-4. Power-Supply Sequence (Option 1)

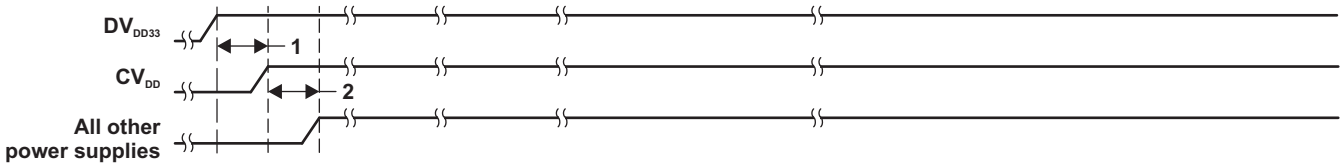

Figure 7-5. Power-Supply Sequence (Option 2)

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Table 7-1. Timing Requirements for Power-Supply Sequence (Option 1)(1)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{su(DVDD33-CVDD)}$	Setup time, DV_{DD33} supply stable before CV_{DD} supply stable	0.5	200	ms
2	$t_{su(CVDD-DVDD18)}$	Setup time, CV_{DD} supply stable before DV_{DD18} supply and $V_{REFSSTL}$ reference voltage stable	0	200	ms
3	$t_{su(DVDD18-DVDD15)}$	Setup time, DV_{DD18} supply and $V_{REFSSTL}$ reference voltage stable before DV_{DD15} supply and $V_{REFHSTL}$ reference voltage stable	0	200	ms
4	$t_{su(DVDD15-DVDD)}$	Setup time, DV_{DD15} supply and $V_{REFHSTL}$ reference voltage stable before DV_{DD} supply stable	0	200	ms

(1) **Note:** The word *stable* means voltages that have reached a valid level as described in .

Table 7-2. Timing Requirements for Power-Supply Sequence (Option 2)(1)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{su(DVDD33-CVDD)}$	Setup time, DV_{DD33} supply stable before CV_{DD} supply stable	0.5	200	ms
2	$t_{su(CVDD-ALLSUP)}$	Setup time, CV_{DD} supply stable before all other supplies stable	0	200	ms

(1) **Note:** The word *stable* means voltages that have reached a valid level as described in .

For detailed information, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* (literature number SPRAAQ4).

7.3.2 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. These caps need to be close to the DSP, no more than 1.25 cm maximum distance to be effective. Physically smaller caps are better, such as 0402, but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

7.3.3 Preserving Boundary-Scan Functionality on DDR2, RGMII, and RapidIO Interface Pins

When the DDR2 Memory Controller is not used, the DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N pins can be NC or connected directly to ground (V_{SS}) to save power. However, this prevents boundary scan from functioning on the DDR2 Memory Controller pins. To preserve boundary-scan functionality on the DDR2 Memory Controller pins DV_{DD18}, $DV_{DD18MON}$, $V_{REFSSTL}$, AV_{DDA3}, AV_{DDA4}, CV_{DD1}, PTV18P, and PTV18N should be connected as follows:

- DV_{DD18}, $DV_{DD18MON}$, AV_{DDA3}, and AV_{DDA4} - connect these pins to the 1.8-V supply.
- CV_{DD1} - connect these pins to the 1.2-V supply.
- $V_{REFSSTL}$ - connect this pin to a voltage of 0.9 V. This voltage can be generated directly from the 1.8-V supply using two 1-kΩ resistors to form a resistor-divider circuit.
- PTV18P - connect this pin to ground (V_{SS}) via a 200-Ω resistor.
- PTV18N - connect this pin to the 1.8-V supply via a 200-Ω resistor.

When the RGMII mode of the EMAC is not used, the DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, and PTV15N pins can be NC or connected directly to ground (V_{SS}) to save power. However, this prevents boundary scan from functioning on the RGMII pins of the EMAC. To preserve boundary-scan functionality on the RGMII pins DV_{DD15}, $DV_{DD15MON}$, $V_{REFHSTL}$, PTV15P, and PTV15N should be connected as follows:

- DV_{DD15} and $DV_{DD15MON}$ - connect these pins to the 1.8-V supply.
- $V_{REFHSTL}$ - connect to a voltage of 0.9 V. This voltage can be generated directly from the 1.8-V supply using two 1-kΩ resistors to form a resistor-divider circuit.
- PTV15P - connect this pin to ground (V_{SS}) via a 200-Ω resistor.

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- PTV15N - connect this pin to the 1.8-V supply via a 200-Ω resistor.

When the RapidIO interface is not used, the CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} pins can be NC or connected directly to ground (V_{SS}) to reduce power use. However, this prevents boundary-scan from functioning on the RapidIO pins. To preserve boundary-scan functionality on the RapidIO pins CV_{DD2}, AV_{DDA}, DV_{DDD}, DV_{DDR}, and AV_{DDT} should be connected as follows:

- CV_{DD2} - connect these pins to the 1.0/1.1-V core supply.
- AV_{DDA}, DV_{DDD}, and AV_{DDT} - connect these pins to the 1.2-V supply.
- DV_{DDR} - connect these pins to the 1.8-V supply.

7.4 Power and Sleep Controller (PSC)

The Power and Sleep Controller (PSC) controls TMS320C6472 device power by gating off clocks to individual peripherals/modules. The PSC consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, power domain control, PSC interrupt control, and a state machine for each peripheral/module. An LPSC is associated with each peripheral/module and provides clock and reset control. The GPSC controls all of the TMS320C6472 LPSCs.

Figure 7-6 shows the PSC components and the power and clock domains they control. For more details on the PSC, see the *TMS320C6472/TMS320TCI6486 PSC User's Guide* (literature number SPRUEG3).

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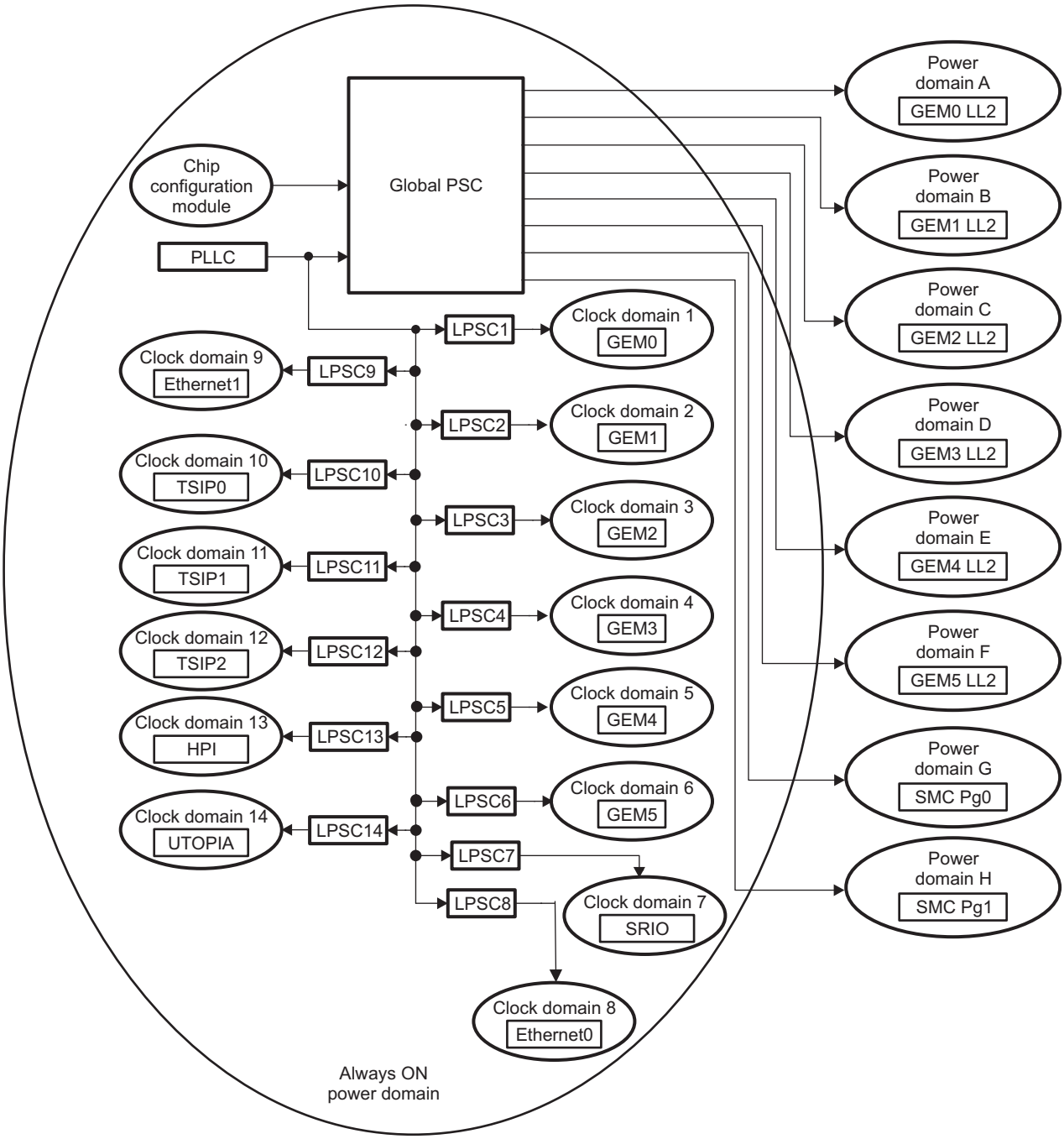

Figure 7-6. TMS320C6472 Power and Clock Domains

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7.4.1 PSC Peripheral Register Descriptions

Table 7-3. PSC Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02AE 0000	PID	Peripheral ID Register
02AE 0004 - 02AE 0014	-	Reserved
02AE 0018	INTEVAL	Interrupt Evaluation Register
02AE 001C - 02AE 003C	-	Reserved
02AE 0040	MERRPR	Module Error Pending Register
02AE 0044 - 02AE 004C	-	Reserved
02AE 0050	MERRCR	Module Error Clear Register
02AE 0054 - 02AE 011C	-	Reserved
02AE 0120	PTCMD	Power Transition Command Register
02AE 0124	-	Reserved
02AE 0128	PTSTAT	Power Domain Transition Status Register
02AE 012C - 02AE 07FC	-	Reserved
02AE 0800	MDSTAT0	Module Status Register
02AE 0804	MDSTAT1	Module Status Register
02AE 0808	MDSTAT2	Module Status Register
02AE 080C	MDSTAT3	Module Status Register
02AE 0810	MDSTAT4	Module Status Register
02AE 0814	MDSTAT5	Module Status Register
02AE 0818	MDSTAT6	Module Status Register
02AE 081C	MDSTAT7	Module Status Register
02AE 0820	MDSTAT8	Module Status Register
02AE 0824	MDSTAT9	Module Status Register
02AE 0828	MDSTAT10	Module Status Register
02AE 082C	MDSTAT11	Module Status Register
02AE 0830	MDSTAT12	Module Status Register
02AE 0834	MDSTAT13	Module Status Register
02AE 0838 - 02AE 09FC	-	Reserved
02AE 0A00	MDCTL0	Module Control Register
02AE 0A04	MDCTL1	Module Control Register
02AE 0A08	MDCTL2	Module Control Register
02AE 0A0C	MDCTL3	Module Control Register
02AE 0A10	MDCTL4	Module Control Register
02AE 0A14	MDCTL5	Module Control Register
02AE 0A18	MDCTL6	Module Control Register
02AE 0A1C	MDCTL7	Module Control Register
02AE 0A20	MDCTL8	Module Control Register
02AE 0A24	MDCTL9	Module Control Register
02AE 0A28	MDCTL10	Module Control Register
02AE 0A2C	MDCTL11	Module Control Register
02AE 0A30	MDCTL12	Module Control Register
02AE 0A34	MDCTL13	Module Control Register
02AE 0A38 - 02AF FFFF	-	Reserved

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7.5 Enhanced Direct Memory Access (EDMA3) Controller

The primary purpose of the EDMA3 is to service user-programmed data transfers between two memory-mapped slave endpoints on the device. The EDMA3 services software-driven paging transfers (e.g., data movement between external memory and internal memory), performs sorting or subframe extraction of various data structures and offloads data transfers from the device CPU.

The EDMA3 includes the following features:

- Fully orthogonal transfer description
  - 3 transfer dimensions: array (multiple bytes), frame (multiple arrays), and block (multiple frames)
  - Single event can trigger transfer of array, frame, or entire block
  - Independent indexes on source and destination
- Flexible transfer definition:
  - Increment or FIFO transfer addressing modes
  - Linking mechanism allows for ping-pong buffering, circular buffering, and repetitive/continuous transfers, all with no CPU intervention
  - Chaining allows multiple transfers to execute with one event
- 256 PaRAM entries
  - Used to define transfer context for channels
  - Each PaRAM entry can be used as a DMA entry, QDMA entry, or link entry
- 64 DMA channels
  - Manually triggered (CPU writes to channel controller register), external event triggered, and chain triggered (completion of one transfer triggers another)
- 4 Quick DMA (QDMA) channels
  - Used for software-driven transfers
  - Triggered upon writing to a single PaRAM set entry
- 4 transfer controllers/event queues with programmable system-level priority
- Interrupt generation for transfer completion and error conditions
- Debug visibility
  - Queue watermarking/threshold allows detection of maximum usage of event queues
  - Error and status recording to facilitate debug

Each of the transfer controllers has a direct connection to the switched central resource (SCR). Table 4-1 lists the peripherals that can be accessed by the transfer controllers.

7.5.1 EDMA3 Channel Synchronization Events

The C64x+ EDMA3 supports up to 64 EDMA channels which service peripheral devices and external memory. Table 7-4 lists the source of C64x+ EDMA3 synchronization events associated with each of the programmable EDMA channels. For the C6472 device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA event registers (ERL, ERH) even if the events are disabled by the EDMA event enable registers (EERL, EERH). The priority of each event can be specified independently in the transfer parameters stored in the EDMA parameter RAM. For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the *TMS320C6472/TMS320TCI648x DSP Enhanced DMA (EDMA3) Controller User's Guide* (literature number SPRU727).

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Table 7-4. C6472 EDMA3 Channel Synchronization Events(1)

EDMA CHANNEL	BINARY	EVENT NAME	EVENT DESCRIPTION
0	0000000	GPINT0	GPIO 0 Event
1	0000001	GPINT1	GPIO 1 Event
2	0000010	GPINT2	GPIO 2 Event
3	0000011	GPINT3	GPIO 3 Event
4	0000100	GPINT4	GPIO 4 Event
5	0000101	GPINT5	GPIO 5 Event
6	0000110	GPINT6	GPIO 6 Event
7	0000111	GPINT7	GPIO 7 Event
8	0001000	TINT6L	Timer 6 Lower Counter Event
9	0001001	TINT6H	Timer 6 High Counter Event
10	0001010	TINT7L	Timer 7 Lower Counter Event
11	0001011	TINT7H	Timer 7 High Counter Event
12	0001100	TINT8L	Timer 8 Lower Counter Event
13	0001101	TINT8H	Timer 8 High Counter Event
14	0001110	TINT9L	Timer 9 Lower Counter Event
15	0001111	TINT9H	Timer 9 High Counter Event
16	0010000	TINT10L	Timer 10 Lower Counter Event
17	0010001	TINT10H	Timer 10 High Counter Event
18	0010010	TINT11L	Timer 11 Lower Counter Event
19	0010011	TINT11H	Timer 11 High Counter Event
20	0010100	ICREVT	I2C Receive Event
21	0010101	ICXEVT	I2C Transmit Event
22	0010110	PXINT0	UTOPIA 0 Transmit Event
23	0010111	PXINT1	UTOPIA 1 Transmit Event
24	0011000	PXINT2	UTOPIA 2 Transmit Event
25	0011001	PXINT3	UTOPIA 3 Transmit Event
26	0011010	PXINT4	UTOPIA 4 Transmit Event
27	0011011	PXINT5	UTOPIA 5 Transmit Event
28	0011100	INTDST4	RapidIO 4 Event
29	0011101	INTDST5	RapidIO 5 Event
30	0011110	INTDST6	RapidIO 6 Event
31	0011111	INTDST7	RapidIO 7 Event
32	0100000	-	Unused
33	0100001	-	Unused
34	0100010	-	Unused
35	0100011	-	Unused
36	0100100	-	Unused
37	0100101	-	Unused
38	0100110	-	Unused
39	0100111	-	Unused
40	0101000	-	Unused
41	0101001	-	Unused
42	0101010	-	Unused
43	0101011	-	Unused

(1) In addition to the events shown in this table, each of the 64 channels can also be synchronized with the transfer completion or alternate transfer completion events. For more detailed information on EDMA event-transfer chaining, see the *TMS320C6472/TMS320TCI648x DSP Enhanced DMA (EDMA3) Controller User's Guide* (literature number SPRU727).

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Table 7-4. C6472 EDMA3 Channel Synchronization Events[1] (continued)

EDMA CHANNEL	BINARY	EVENT NAME	EVENT DESCRIPTION
44	0101100	-	Unused
45	0101101	-	Unused
46	0101110	-	Unused
47	0101111	-	Unused
48	0110000	-	Unused
49	0110001	-	Unused
50	0110010	-	Unused
51	0110011	-	Unused
52	0110100	-	Unused
53	0110101	-	Unused
54	0110110	-	Unused
55	0110111	-	Unused
56	0111000	-	Unused
57	0111001	-	Unused
58	0111010	-	Unused
59	0111011	-	Unused
60	0111100	-	Unused
61	0111101	-	Unused
62	0111110	-	Unused
63	0111111	-	Unused

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7.5.2 EDMA3 Peripheral Register Descriptions

Table 7-5. EDMA3 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0000	PID	Peripheral ID Register
02A0 0004	CCCFG	EDMA3CC Configuration Register
02A0 0008 - 02A0 00FC	-	Reserved
02A0 0100	DCHMAP0	EDMA Channel 0 Mapping to PaRAM
02A0 0104	DCHMAP1	EDMA Channel 1 Mapping to PaRAM
02A0 0108	DCHMAP2	EDMA Channel 2 Mapping to PaRAM
02A0 010C	DCHMAP3	EDMA Channel 3 Mapping to PaRAM
02A0 0110	DCHMAP4	EDMA Channel 4 Mapping to PaRAM
02A0 0114	DCHMAP5	EDMA Channel 5 Mapping to PaRAM
02A0 0118	DCHMAP6	EDMA Channel 6 Mapping to PaRAM
02A0 011C	DCHMAP7	EDMA Channel 7 Mapping to PaRAM
02A0 0120	DCHMAP8	EDMA Channel 8 Mapping to PaRAM
02A0 0124	DCHMAP9	EDMA Channel 9 Mapping to PaRAM
02A0 0128	DCHMAP10	EDMA Channel 10 Mapping to PaRAM
02A0 012C	DCHMAP11	EDMA Channel 11 Mapping to PaRAM
02A0 0130	DCHMAP12	EDMA Channel 12 Mapping to PaRAM
02A0 0134	DCHMAP13	EDMA Channel 13 Mapping to PaRAM
02A0 0138	DCHMAP14	EDMA Channel 14 Mapping to PaRAM
02A0 013C	DCHMAP15	EDMA Channel 15 Mapping to PaRAM
02A0 0140	DCHMAP16	EDMA Channel 16 Mapping to PaRAM
02A0 0144	DCHMAP17	EDMA Channel 17 Mapping to PaRAM

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0148	DCHMAP18	EDMA Channel 18 Mapping to PaRAM
02A0 014C	DCHMAP19	EDMA Channel 19 Mapping to PaRAM
02A0 0150	DCHMAP20	EDMA Channel 20 Mapping to PaRAM
02A0 0154	DCHMAP21	EDMA Channel 21 Mapping to PaRAM
02A0 0158	DCHMAP22	EDMA Channel 22 Mapping to PaRAM
02A0 015C	DCHMAP23	EDMA Channel 23 Mapping to PaRAM
02A0 0160	DCHMAP24	EDMA Channel 24 Mapping to PaRAM
02A0 0164	DCHMAP25	EDMA Channel 25 Mapping to PaRAM
02A0 0168	DCHMAP26	EDMA Channel 26 Mapping to PaRAM
02A0 016C	DCHMAP27	EDMA Channel 27 Mapping to PaRAM
02A0 0170	DCHMAP28	EDMA Channel 28 Mapping to PaRAM
02A0 0174	DCHMAP29	EDMA Channel 29 Mapping to PaRAM
02A0 0178	DCHMAP30	EDMA Channel 30 Mapping to PaRAM
02A0 017C	DCHMAP31	EDMA Channel 31 Mapping to PaRAM
02A0 0180	DCHMAP32	EDMA Channel 32 Mapping to PaRAM
02A0 0184	DCHMAP33	EDMA Channel 33 Mapping to PaRAM
02A0 0188	DCHMAP34	EDMA Channel 34 Mapping to PaRAM
02A0 018C	DCHMAP35	EDMA Channel 35 Mapping to PaRAM
02A0 0190	DCHMAP36	EDMA Channel 36 Mapping to PaRAM
02A0 0194	DCHMAP37	EDMA Channel 37 Mapping to PaRAM
02A0 0198	DCHMAP38	EDMA Channel 38 Mapping to PaRAM
02A0 019C	DCHMAP39	EDMA Channel 39 Mapping to PaRAM
02A0 01A0	DCHMAP40	EDMA Channel 40 Mapping to PaRAM
02A0 01A4	DCHMAP41	EDMA Channel 41 Mapping to PaRAM
02A0 01A8	DCHMAP42	EDMA Channel 42 Mapping to PaRAM
02A0 01AC	DCHMAP43	EDMA Channel 43 Mapping to PaRAM
02A0 01B0	DCHMAP44	EDMA Channel 44 Mapping to PaRAM
02A0 01B4	DCHMAP45	EDMA Channel 45 Mapping to PaRAM
02A0 01B8	DCHMAP46	EDMA Channel 46 Mapping to PaRAM
02A0 01BC	DCHMAP47	EDMA Channel 47 Mapping to PaRAM
02A0 01C0	DCHMAP48	EDMA Channel 48 Mapping to PaRAM
02A0 01C4	DCHMAP49	EDMA Channel 49 Mapping to PaRAM
02A0 01C8	DCHMAP50	EDMA Channel 50 Mapping to PaRAM
02A0 01CC	DCHMAP51	EDMA Channel 51 Mapping to PaRAM
02A0 01D0	DCHMAP52	EDMA Channel 52 Mapping to PaRAM
02A0 01D4	DCHMAP53	EDMA Channel 53 Mapping to PaRAM
02A0 01D8	DCHMAP54	EDMA Channel 54 Mapping to PaRAM
02A0 01DC	DCHMAP55	EDMA Channel 55 Mapping to PaRAM
02A0 01E0	DCHMAP56	EDMA Channel 56 Mapping to PaRAM
02A0 01E4	DCHMAP57	EDMA Channel 57 Mapping to PaRAM
02A0 01E8	DCHMAP58	EDMA Channel 58 Mapping to PaRAM
02A0 01EC	DCHMAP59	EDMA Channel 59 Mapping to PaRAM
02A0 01F0	DCHMAP60	EDMA Channel 60 Mapping to PaRAM
02A0 01F4	DCHMAP61	EDMA Channel 61 Mapping to PaRAM
02A0 01F8	DCHMAP62	EDMA Channel 62 Mapping to PaRAM
02A0 01FC	DCHMAP63	EDMA Channel 63 Mapping to PaRAM
02A0 0200	QCHMAP0	QDMA Channel 0 Mapping to PaRAM

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0204	QCHMAP1	QDMA Channel 1 Mapping to PaRAM
02A0 0208	QCHMAP2	QDMA Channel 2 Mapping to PaRAM
02A0 020C	QCHMAP3	QDMA Channel 3 Mapping to PaRAM
02A0 0210 - 02A0 021C	-	Reserved
02A0 0220 - 02A0 023C	-	Reserved
02A0 0240	DMAQNUM0	EDMA Queue Number 0; Channels 00 thru 07
02A0 0244	DMAQNUM1	EDMA Queue Number 1; Channels 08 thru 15
02A0 0248	DMAQNUM2	EDMA Queue Number 2; Channels 16 thru 23
02A0 024C	DMAQNUM3	EDMA Queue Number 3; Channels 24 thru 31
02A0 0250	DMAQNUM4	EDMA Queue Number 4; Channels 32 thru 39
02A0 0254	DMAQNUM5	EDMA Queue Number 5; Channels 40 thru 47
02A0 0258	DMAQNUM6	EDMA Queue Number 6; Channels 48 thru 23
02A0 025C	DMAQNUM7	EDMA Queue Number 7; Channels 56 thru 63
02A0 0260	QDMAQNUM	EDMA QDMA Queue Number
02A0 0264 - 02A0 027C	-	Reserved
02A0 0280	QUETCMAP	EDMA Queue to TC Mapping
02A0 0284	QUEPRI	EDMA Queue Priority
02A0 0288 - 02A0 02FC	-	Reserved
02A0 0300	EMR	EDMA Event Miss Register
02A0 0304	EMRH	EDMA Event Miss Register High
02A0 0308	EMCR	EDMA Event Miss Clear Register
02A0 030C	EMCRH	EDMA Event Miss Clear Register High
02A0 0310	QEMR	QDMA Event Miss Register
02A0 0314	QEMCR	QDMA Event Miss Clear Register
02A0 0318	CCERR	EDMA CC Error Register
02A0 031C	CCERRCLR	EDMA CC Error Clear Register
02A0 0320	EEVAL	EDMA Error Evaluation Register
02A0 0324 - 02A0 033C	-	Reserved
02A0 0340	DRAE0	EDMA Region Access Enable 0 Register
02A0 0344	DRAEH0	EDMA Region Access High Enable 0 Register
02A0 0348	DRAE1	EDMA Region Access Enable 1 Register
02A0 034C	DRAEH1	EDMA Region Access High Enable 1 Register
02A0 0350	DRAE2	EDMA Region Access Enable 2 Register
02A0 0354	DRAEH2	EDMA Region Access High Enable 2 Register
02A0 0358	DRAE3	EDMA Region Access Enable 3 Register
02A0 035C	DRAEH3	EDMA Region Access High Enable 3 Register
02A0 0360	DRAE4	EDMA Region Access Enable 4 Register
02A0 0364	DRAEH4	EDMA Region Access High Enable 4 Register
02A0 0368	DRAE5	EDMA Region Access Enable 5 Register
02A0 036C	DRAEH5	EDMA Region Access High Enable 5 Register
02A0 0370	DRAE6	EDMA Region Access Enable 6 Register
02A0 0374	DRAEH6	EDMA Region Access High Enable 6 Register
02A0 0378	DRAE7	EDMA Region Access Enable 7 Register
02A0 037C	DRAEH7	EDMA Region Access High Enable 7 Register
02A0 0380	QRAE0	QDMA Region Access Enable 0
02A0 0384	QRAE1	QDMA Region Access Enable 1
02A0 0388	QRAE2	QDMA Region Access Enable 2

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 038C	QRAE3	QDMA Region Access Enable 3
02A0 0390 - 02A0 039C	-	Reserved
02A0 0400	Q0E0	EDMA Event Q0 Entry 0/Event Q0 Base
02A0 0404	Q0E1	EDMA Event Q0 Entry 1/Event Q0 Base
02A0 0408	Q0E2	EDMA Event Q0 Entry 2/Event Q0 Base
02A0 040C	Q0E3	EDMA Event Q0 Entry 3/Event Q0 Base
02A0 0410	Q0E4	EDMA Event Q0 Entry 4/Event Q0 Base
02A0 0414	Q0E5	EDMA Event Q0 Entry 5/Event Q0 Base
02A0 0418	Q0E6	EDMA Event Q0 Entry 6/Event Q0 Base
02A0 041C	Q0E7	EDMA Event Q0 Entry 7/Event Q0 Base
02A0 0420	Q0E8	EDMA Event Q0 Entry 8/Event Q0 Base
02A0 0424	Q0E9	EDMA Event Q0 Entry 9/Event Q0 Base
02A0 0428	Q0E10	EDMA Event Q0 Entry 10/Event Q0 Base
02A0 042C	Q0E11	EDMA Event Q0 Entry 11/Event Q0 Base
02A0 0430	Q0E12	EDMA Event Q0 Entry 12/Event Q0 Base
02A0 0434	Q0E13	EDMA Event Q0 Entry 13/Event Q0 Base
02A0 0438	Q0E14	EDMA Event Q0 Entry 14/Event Q0 Base
02A0 043C	Q0E15	EDMA Event Q0 Entry 15/Event Q0 Base
02A0 0440	Q1E0	EDMA Event Q1 Entry 0/Event Q1 Base
02A0 0444	Q1E1	EDMA Event Q1 Entry 1/Event Q1 Base
02A0 0448	Q1E2	EDMA Event Q1 Entry 2/Event Q1 Base
02A0 044C	Q1E3	EDMA Event Q1 Entry 3/Event Q1 Base
02A0 0450	Q1E4	EDMA Event Q1 Entry 4/Event Q1 Base
02A0 0454	Q1E5	EDMA Event Q1 Entry 5/Event Q1 Base
02A0 0458	Q1E6	EDMA Event Q1 Entry 6/Event Q1 Base
02A0 045C	Q1E7	EDMA Event Q1 Entry 7/Event Q1 Base
02A0 0460	Q1E8	EDMA Event Q1 Entry 8/Event Q1 Base
02A0 0464	Q1E9	EDMA Event Q1 Entry 9/Event Q1 Base
02A0 0468	Q1E10	EDMA Event Q1 Entry 10/Event Q1 Base
02A0 046C	Q1E11	EDMA Event Q1 Entry 11/Event Q1 Base
02A0 0470	Q1E12	EDMA Event Q1 Entry 12/Event Q1 Base
02A0 0474	Q1E13	EDMA Event Q1 Entry 13/Event Q1 Base
02A0 0478	Q1E14	EDMA Event Q1 Entry 14/Event Q1 Base
02A0 047C	Q1E15	EDMA Event Q1 Entry 15/Event Q1 Base
02A0 0480	Q2E0	EDMA Event Q2 Entry 0/Event Q2 Base
02A0 0484	Q2E1	EDMA Event Q2 Entry 1/Event Q2 Base
02A0 0488	Q2E2	EDMA Event Q2 Entry 2/Event Q2 Base
02A0 048C	Q2E3	EDMA Event Q2 Entry 3/Event Q2 Base
02A0 0490	Q2E4	EDMA Event Q2 Entry 4/Event Q2 Base
02A0 0494	Q2E5	EDMA Event Q2 Entry 5/Event Q2 Base
02A0 0498	Q2E6	EDMA Event Q2 Entry 6/Event Q2 Base
02A0 049C	Q2E7	EDMA Event Q2 Entry 7/Event Q2 Base
02A0 04A0	Q2E8	EDMA Event Q2 Entry 8/Event Q2 Base
02A0 04A4	Q2E9	EDMA Event Q2 Entry 9/Event Q2 Base
02A0 04A8	Q2E10	EDMA Event Q2 Entry 10/Event Q2 Base
02A0 04AC	Q2E11	EDMA Event Q2 Entry 11/Event Q2 Base
02A0 04B0	Q2E12	EDMA Event Q2 Entry 12/Event Q2 Base

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 04B4	Q2E13	EDMA Event Q2 Entry 13/Event Q2 Base
02A0 04B8	Q2E14	EDMA Event Q2 Entry 14/Event Q2 Base
02A0 04BC	Q2E15	EDMA Event Q2 Entry 15/Event Q2 Base
02A0 04C0	Q3E0	EDMA Event Q3 Entry 0/Event Q3 Base
02A0 04C4	Q3E1	EDMA Event Q3 Entry 1/Event Q3 Base
02A0 04C8	Q3E2	EDMA Event Q3 Entry 2/Event Q3 Base
02A0 04CC	Q3E3	EDMA Event Q3 Entry 3/Event Q3 Base
02A0 04D0	Q3E4	EDMA Event Q3 Entry 4/Event Q3 Base
02A0 04D4	Q3E5	EDMA Event Q3 Entry 5/Event Q3 Base
02A0 04D8	Q3E6	EDMA Event Q3 Entry 6/Event Q3 Base
02A0 04DC	Q3E7	EDMA Event Q3 Entry 7/Event Q3 Base
02A0 04E0	Q3E8	EDMA Event Q3 Entry 8/Event Q3 Base
02A0 04E4	Q3E9	EDMA Event Q3 Entry 9/Event Q3 Base
02A0 04E8	Q3E10	EDMA Event Q3 Entry 10/Event Q3 Base
02A0 04EC	Q3E11	EDMA Event Q3 Entry 11/Event Q3 Base
02A0 04F0	Q3E12	EDMA Event Q3 Entry 12/Event Q3 Base
02A0 04F4	Q3E13	EDMA Event Q3 Entry 13/Event Q3 Base
02A0 04F8	Q3E14	EDMA Event Q3 Entry 14/Event Q3 Base
02A0 04FC	Q3E15	EDMA Event Q3 Entry 15/Event Q3 Base
02A0 0500 - 02A0 05FC	-	Reserved
02A0 0600	QSTAT0	EDMA Queue 0 Status
02A0 0604	QSTAT1	EDMA Queue 1 Status
02A0 0608	QSTAT2	EDMA Queue 2 Status
02A0 060C	QSTAT3	EDMA Queue 3 Status
02A0 0610 - 02A0 061C	-	Reserved
02A0 0620	QWMTHRA	EDMA Queue Threshold A, for Q[3:0]
02A0 0624 - 02A0 063C	-	Reserved
02A0 0640	CCSTAT	Channel Controller Status
02A0 0644 - 02A0 07FC	-	Reserved
02A0 0800	MPFAR	Memory Protection Fault Address Register
02A0 0804	MPFSR	Memory Protection Fault Status Register
02A0 0808	MPFCR	Memory Protection Fault Command Register
02A0 080C	MPPA0	Memory Protection Page Attribute 0 Register
02A0 0810	MPPA1	Memory Protection Page Attribute 1 Register
02A0 0814	MPPA2	Memory Protection Page Attribute 2 Register
02A0 0818	MPPA3	Memory Protection Page Attribute 3 Register
02A0 081C	MPPA4	Memory Protection Page Attribute 4 Register
02A0 0820	MPPA5	Memory Protection Page Attribute 5 Register
02A0 0824	MPPA6	Memory Protection Page Attribute 6 Register
02A0 0828	MPPA7	Memory Protection Page Attribute 7 Register
02A0 082C - 02A0 09FC	-	Reserved
02A0 1000	ER (ERL)	EDMA Event Register
02A0 1004	ERH	EDMA Event Register High
02A0 1008	ECR	EDMA Event Clear Register
02A0 100C	ECRH	EDMA Event Clear Register High
02A0 1010	ESR	EDMA Event Set Register
02A0 1014	ESRH	EDMA Event Set Register High

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 1018	CER	EDMA Chained Event Register
02A0 101C	CERH	EDMA Chained Event Register High
02A0 1020	EER (EERL)	EDMA Event Enable Register
02A0 1024	EERH	EDMA Event Enable Register High
02A0 1028	EECR	EDMA Event Enable Clear Register
02A0 102C	EECRH	EDMA Event Enable Clear Register High
02A0 1030	EESR	EDMA Event Enable Set Register
02A0 1034	EESRH	EDMA Event Enable Set Register High
02A0 1038	SER	EDMA Secondary Event Register
02A0 103C	SERH	EDMA Secondary Event Register High
02A0 1040	SECR	EDMA Secondary Event Clear Register
02A0 1044	SECRH	EDMA Secondary Event Clear Register High
02A0 1048 - 02A0 104C	-	Reserved
02A0 1050	IER	EDMA Interrupt Enable Register
02A0 1054	IERH	EDMA Interrupt Enable Register High
02A0 1058	IECR	EDMA Interrupt Enable Clear Register
02A0 105C	IECRH	EDMA Interrupt Enable Clear Register High
02A0 1060	IESR	EDMA Interrupt Enable Set Register
02A0 1064	IESRH	EDMA Interrupt Enable Set Register High
02A0 1068	IPR	EDMA Interrupt Pending Register
02A0 106C	IPRH	EDMA Interrupt Pending Register High
02A0 1070	ICR	EDMA Interrupt Clear Register
02A0 1074	ICRH	EDMA Interrupt Clear Register High
02A0 1078	IEVAL	EDMA Interrupt Evaluation Register (Set/Eval)
02A0 107C	-	Reserved
02A0 1080	QER	QDMA Event Register
02A0 1084	QEER	QDMA Event Enable Register
02A0 1088	QEECR	QDMA Event Enable Clear Register
02A0 108C	QEESR	QDMA Event Enable Set Register
02A0 1090	QSER	QDMA Secondary Event Register
02A0 1094	QSECR	QDMA Secondary Event Clear Register
02A0 1098 - 02A0 1FFC	-	Reserved
Parameter RAM		
02A0 4000 - 02A0 401C	-	Parameter Set 0
02A0 4020 - 02A0 403C	-	Parameter Set 1
02A0 4040 - 02A0 405C	-	Parameter Set 2
02A0 4060 - 02A0 407C	-	Parameter Set 3
02A0 4080 - 02A0 409C	-	Parameter Set 4
02A0 40A0 - 02A0 40BC	-	Parameter Set 5
02A0 40C0 - 02A0 40DC	-	Parameter Set 6
02A0 40E0 - 02A0 40FC	-	Parameter Set 7
02A0 4100 - 02A0 411C	-	Parameter Set 8
02A0 4120 - 02A0 413C	-	Parameter Set 9
...		...
02A0 47E0 - 02A0 47FC	-	Parameter Set 63
02A0 4800 - 02A0 481C	-	Parameter Set 64
02A0 4820 - 02A0 483C	-	Parameter Set 65

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Table 7-5. EDMA3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
...		...
02A0 5FC0 - 02A0 5FDC	-	Parameter Set 254
02A0 5FE0 - 02A0 5FFC	-	Parameter Set 255

Table 7-6. EDMA3 Transfer Controller 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A2 0000	PID	Peripheral Identification Register
02A2 0004	TCCFG	EDMA3TC Configuration Register
02A2 0008 - 02A2 00FC	-	Reserved
02A2 0100	TCSTAT	EDMA3TC Channel Status Register
02A2 0104 - 02A2 011C	-	Reserved
02A2 0120	ERRSTAT	Error Register
02A2 0124	ERREN	Error Enable Register
02A2 0128	ERRCLR	Error Clear Register
02A2 012C	ERRDET	Error Details Register
02A2 0130	ERRCMD	Error Interrupt Command Register
02A2 0134 - 02A2 013C	-	Reserved
02A2 0140	RDRATE	Read Rate Register
02A2 0144 - 02A2 023C	-	Reserved
02A2 0240	SAOPT	Source Active Options Register
02A2 0244	SASRC	Source Active Source Address Register
02A2 0248	SACNT	Source Active Count Register
02A2 024C	SADST	Source Active Destination Address Register
02A2 0250	SABIDX	Source Active Source B-Index Register
02A2 0254	SAMPPRXY	Source Active Memory Protection Proxy Register
02A2 0258	SACNTRLD	Source Active Count Reload Register
02A2 025C	SASRCBREF	Source Active Source Address B-Reference Register
02A2 0260	SADSTBREF	Source Active Destination Address B-Reference Register
02A2 0264 - 02A2 027C	-	Reserved
02A2 0280	DFCNTRLD	Destination FIFO Set Count Reload
02A2 0284	DFSRCBREF	Destination FIFO Set Destination Address B Reference Register
02A2 0288	DFDSTBREF	Destination FIFO Set Destination Address B Reference Register
02A2 028C - 02A2 02FC	-	Reserved
02A2 0300	DFOPT0	Destination FIFO Options Register 0
02A2 0304	DFSRC0	Destination FIFO Source Address Register 0
02A2 0308	DFCNT0	Destination FIFO Count Register 0
02A2 030C	DFDST0	Destination FIFO Destination Address Register 0
02A2 0310	DFBIDX0	Destination FIFO BIDX Register 0
02A2 0314	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
02A2 0318 - 02A2 033C	-	Reserved
02A2 0340	DFOPT1	Destination FIFO Options Register 1
02A2 0344	DFSRC1	Destination FIFO Source Address Register 1
02A2 0348	DFCNT1	Destination FIFO Count Register 1
02A2 034C	DFDST1	Destination FIFO Destination Address Register 1
02A2 0350	DFBIDX1	Destination FIFO BIDX Register 1
02A2 0354	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
02A2 0358 - 02A2 037C	-	Reserved

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Table 7-6. EDMA3 Transfer Controller 0 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A2 0380	DFOPT2	Destination FIFO Options Register 2
02A2 0384	DFSRC2	Destination FIFO Source Address Register 2
02A2 0388	DFCNT2	Destination FIFO Count Register 2
02A2 038C	DFDST2	Destination FIFO Destination Address Register 2
02A2 0390	DFBIDX2	Destination FIFO BIDX Register 2
02A2 0394	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
02A2 0398 - 02A2 03BC	-	Reserved
02A2 03C0	DFOPT3	Destination FIFO Options Register 3
02A2 03C4	DFSRC3	Destination FIFO Source Address Register 3
02A2 03C8	DFCNT3	Destination FIFO Count Register 3
02A2 03CC	DFDST3	Destination FIFO Destination Address Register 3
02A2 03D0	DFBIDX3	Destination FIFO BIDX Register 3
02A2 03D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3
02A2 03D8 - 02A2 7FFC	-	Reserved

Table 7-7. EDMA3 Transfer Controller 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A2 8000	PID	Peripheral Identification Register
02A2 8004	TCCFG	EDMA3TC Configuration Register
02A2 8008 - 02A2 80FC	-	Reserved
02A2 8100	TCSTAT	EDMA3TC Channel Status Register
02A2 8104 - 02A2 811C	-	Reserved
02A2 8120	ERRSTAT	Error Register
02A2 8124	ERREN	Error Enable Register
02A2 8128	ERRCLR	Error Clear Register
02A2 812C	ERRDET	Error Details Register
02A2 8130	ERRCMD	Error Interrupt Command Register
02A2 8134 - 02A2 813C	-	Reserved
02A2 8140	RDRATE	Read Rate Register
02A2 8144 - 02A2 823C	-	Reserved
02A2 8240	SAOPT	Source Active Options Register
02A2 8244	SASRC	Source Active Source Address Register
02A2 8248	SACNT	Source Active Count Register
02A2 824C	SADST	Source Active Destination Address Register
02A2 8250	SABIDX	Source Active Source B-Index Register
02A2 8254	SAMPPRXY	Source Active Memory Protection Proxy Register
02A2 8258	SACNTRLD	Source Active Count Reload Register
02A2 825C	SASRCBREF	Source Active Source Address B-Reference Register
02A2 8260	SADSTBREF	Source Active Destination Address B-Reference Register
02A2 8264 - 02A2 827C	-	Reserved
02A2 8280	DFCNTRLD	Destination FIFO Set Count Reload
02A2 8284	DFSRCBREF	Destination FIFO Set Destination Address B Reference Register
02A2 8288	DFDSTBREF	Destination FIFO Set Destination Address B Reference Register
02A2 828C - 02A2 82FC	-	Reserved
02A2 8300	DFOPT0	Destination FIFO Options Register 0
02A2 8304	DFSRC0	Destination FIFO Source Address Register 0
02A2 8308	DFCNT0	Destination FIFO Count Register 0

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Table 7-7. EDMA3 Transfer Controller 1 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A2 830C	DFDST0	Destination FIFO Destination Address Register 0
02A2 8310	DFBIDX0	Destination FIFO BIDX Register 0
02A2 8314	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
02A2 8318 - 02A2 833C	-	Reserved
02A2 8340	DFOPT1	Destination FIFO Options Register 1
02A2 8344	DFSRC1	Destination FIFO Source Address Register 1
02A2 8348	DFCNT1	Destination FIFO Count Register 1
02A2 834C	DFDST1	Destination FIFO Destination Address Register 1
02A2 8350	DFBIDX1	Destination FIFO BIDX Register 1
02A2 8354	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
02A2 8358 - 02A2 837C	-	Reserved
02A2 8380	DFOPT2	Destination FIFO Options Register 2
02A2 8384	DFSRC2	Destination FIFO Source Address Register 2
02A2 8388	DFCNT2	Destination FIFO Count Register 2
02A2 838C	DFDST2	Destination FIFO Destination Address Register 2
02A2 8390	DFBIDX2	Destination FIFO BIDX Register 2
02A2 8394	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
02A2 8398 - 02A2 83BC	-	Reserved
02A2 83C0	DFOPT3	Destination FIFO Options Register 3
02A2 83C4	DFSRC3	Destination FIFO Source Address Register 3
02A2 83C8	DFCNT3	Destination FIFO Count Register 3
02A2 83CC	DFDST3	Destination FIFO Destination Address Register 3
02A2 83D0	DFBIDX3	Destination FIFO BIDX Register 3
02A2 83D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3
02A2 83D8 - 02A2 FFFC	-	Reserved

Table 7-8. EDMA3 Transfer Controller 2 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A3 0000	PID	Peripheral Identification Register
02A3 0004	TCCFG	EDMA3TC Configuration Register
02A3 0008 - 02A3 00FC	-	Reserved
02A3 0100	TCSTAT	EDMA3TC Channel Status Register
02A3 0104 - 02A3 011C	-	Reserved
02A3 0120	ERRSTAT	Error Register
02A3 0124	ERREN	Error Enable Register
02A3 0128	ERRCLR	Error Clear Register
02A3 012C	ERRDET	Error Details Register
02A3 0130	ERRCMD	Error Interrupt Command Register
02A3 0134 - 02A3 013C	-	Reserved
02A3 0140	RDRATE	Read Rate Register
02A3 0144 - 02A3 023C	-	Reserved
02A3 0240	SAOPT	Source Active Options Register
02A3 0244	SASRC	Source Active Source Address Register
02A3 0248	SACNT	Source Active Count Register
02A3 024C	SADST	Source Active Destination Address Register
02A3 0250	SABIDX	Source Active Source B-Index Register
02A3 0254	SAMPPRXY	Source Active Memory Protection Proxy Register

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Table 7-8. EDMA3 Transfer Controller 2 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A3 0258	SACNTRLD	Source Active Count Reload Register
02A3 025C	SASRCBREF	Source Active Source Address B-Reference Register
02A3 0260	SADSTBREF	Source Active Destination Address B-Reference Register
02A3 0264 - 02A3 027C	-	Reserved
02A3 0280	DFCNTRLD	Destination FIFO Set Count Reload
02A3 0284	DFSRCBREF	Destination FIFO Set Destination Address B Reference Register
02A3 0288	DFDSTBREF	Destination FIFO Set Destination Address B Reference Register
02A3 028C - 02A3 02FC	-	Reserved
02A3 0300	DFOPT0	Destination FIFO Options Register 0
02A3 0304	DFSRC0	Destination FIFO Source Address Register 0
02A3 0308	DFCNT0	Destination FIFO Count Register 0
02A3 030C	DFDST0	Destination FIFO Destination Address Register 0
02A3 0310	DFBIDX0	Destination FIFO BIDX Register 0
02A3 0314	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
02A3 0318 - 02A3 033C	-	Reserved
02A3 0340	DFOPT1	Destination FIFO Options Register 1
02A3 0344	DFSRC1	Destination FIFO Source Address Register 1
02A3 0348	DFCNT1	Destination FIFO Count Register 1
02A3 034C	DFDST1	Destination FIFO Destination Address Register 1
02A3 0350	DFBIDX1	Destination FIFO BIDX Register 1
02A3 0354	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
02A3 0358 - 02A3 037C	-	Reserved
02A3 0380	DFOPT2	Destination FIFO Options Register 2
02A3 0384	DFSRC2	Destination FIFO Source Address Register 2
02A3 0388	DFCNT2	Destination FIFO Count Register 2
02A3 038C	DFDST2	Destination FIFO Destination Address Register 2
02A3 0390	DFBIDX2	Destination FIFO BIDX Register 2
02A3 0394	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
02A3 0398 - 02A3 03BC	-	Reserved
02A3 03C0	DFOPT3	Destination FIFO Options Register 3
02A3 03C4	DFSRC3	Destination FIFO Source Address Register 3
02A3 03C8	DFCNT3	Destination FIFO Count Register 3
02A3 03CC	DFDST3	Destination FIFO Destination Address Register 3
02A3 03D0	DFBIDX3	Destination FIFO BIDX Register 3
02A3 03D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3
02A3 03D8 - 02A3 7FFC	-	Reserved

Table 7-9. EDMA3 Transfer Controller 3 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A3 8000	PID	Peripheral Identification Register
02A3 8004	TCCFG	EDMA3TC Configuration Register
02A3 8008 - 02A3 80FC	-	Reserved
02A3 8100	TCSTAT	EDMA3TC Channel Status Register
02A3 8104 - 02A3 811C	-	Reserved
02A3 8120	ERRSTAT	Error Register
02A3 8124	ERREN	Error Enable Register
02A3 8128	ERRCLR	Error Clear Register

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Table 7-9. EDMA3 Transfer Controller 3 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A3 812C	ERRDET	Error Details Register
02A3 8130	ERRCMD	Error Interrupt Command Register
02A3 8134 - 02A3 813C	-	Reserved
02A3 8140	RDRATE	Read Rate Register
02A3 8144 - 02A3 823C	-	Reserved
02A3 8240	SAOPT	Source Active Options Register
02A3 8244	SASRC	Source Active Source Address Register
02A3 8248	SACNT	Source Active Count Register
02A3 824C	SADST	Source Active Destination Address Register
02A3 8250	SABIDX	Source Active Source B-Index Register
02A3 8254	SAMPPRXY	Source Active Memory Protection Proxy Register
02A3 8258	SACNTRLD	Source Active Count Reload Register
02A3 825C	SASRCBREF	Source Active Source Address B-Reference Register
02A3 8260	SADSTBREF	Source Active Destination Address B-Reference Register
02A3 8264 - 02A3 827C	-	Reserved
02A3 8280	DFCNTRLD	Destination FIFO Set Count Reload
02A3 8284	DFSRCBREF	Destination FIFO Set Destination Address B Reference Register
02A3 8288	DFDSTBREF	Destination FIFO Set Destination Address B Reference Register
02A3 828C - 02A3 82FC	-	Reserved
02A3 8300	DFOPT0	Destination FIFO Options Register 0
02A3 8304	DFSRC0	Destination FIFO Source Address Register 0
02A3 8308	DFCNT0	Destination FIFO Count Register 0
02A3 830C	DFDST0	Destination FIFO Destination Address Register 0
02A3 8310	DFBIDX0	Destination FIFO BIDX Register 0
02A3 8314	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
02A3 8318 - 02A3 833C	-	Reserved
02A3 8340	DFOPT1	Destination FIFO Options Register 1
02A3 8344	DFSRC1	Destination FIFO Source Address Register 1
02A3 8348	DFCNT1	Destination FIFO Count Register 1
02A3 834C	DFDST1	Destination FIFO Destination Address Register 1
02A3 8350	DFBIDX1	Destination FIFO BIDX Register 1
02A3 8354	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
02A3 8358 - 02A3 837C	-	Reserved
02A3 8380	DFOPT2	Destination FIFO Options Register 2
02A3 8384	DFSRC2	Destination FIFO Source Address Register 2
02A3 8388	DFCNT2	Destination FIFO Count Register 2
02A3 838C	DFDST2	Destination FIFO Destination Address Register 2
02A3 8390	DFBIDX2	Destination FIFO BIDX Register 2
02A3 8394	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
02A3 8398 - 02A3 83BC	-	Reserved
02A3 83C0	DFOPT3	Destination FIFO Options Register 3
02A3 83C4	DFSRC3	Destination FIFO Source Address Register 3
02A3 83C8	DFCNT3	Destination FIFO Count Register 3
02A3 83CC	DFDST3	Destination FIFO Destination Address Register 3
02A3 83D0	DFBIDX3	Destination FIFO BIDX Register 3
02A3 83D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3
02A3 83D8 - 02A3 FFFC	-	Reserved

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7.6 Interrupts

7.6.1 Interrupt Sources and Interrupt Controller

The CPU interrupts on the C6472 device are configured through the C64x+ megamodule interrupt controller. The interrupt controller allows for up to 128 system events to be programmed to any of the twelve CPU interrupt inputs, the CPU exception input, or the advanced emulation logic. Table 8-4 shows the mapping of system events to the interrupt controller inputs. Event numbers 0-31 correspond to the default interrupt mapping of the device. The remaining events must be mapped using software.

For more information on the Interrupt Controller, see the *TMS320C64x+ DSP Megamodule Reference Guide* (literature number SPRU871).

Table 7-10. C6472 DSP Interrupts

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
0(1)	EVT0	Event Combiner 0 Output
1(1)	EVT1	Event Combiner 1 Output
2(1)	EVT2	Event Combiner 2 Output
3(1)	EVT3	Event Combiner 3 Output
4(2)	RIOINT_LOCAL	RapidIO Individual Interrupt
5	MACRXINT0	Ethernet MAC0 Receive Interrupt
6	MACTXINT0	Ethernet MAC0 Transmit Interrupt
7	MACRXINT1	Ethernet MAC1 Receive Interrupt
8	MACTXINT1	Ethernet MAC1 Transmit Interrupt
9(1)	EMU_D	ECM Interrupt for: • Host scan access • DTDMA transfer complete • AET interrupt
10	Reserved	
11(1)	EMU_RTDXRX	RTDX Receive Complete
12(1)	EMU_RTDXTX	RTDX Transmit Complete
13(1)	IDMA0	IDMA Channel 0 Interrupt
14(1)	IDMA1	IDMA Channel 1 Interrupt
15(3)	EDMA3CCINT_LOCAL	EDMA3CC Individual Completion Interrupt
16	TINTL	Local Timer Interrupt Low
17	TINTH	Local Timer Interrupt High
18	TINT6L	Timer 6 Interrupt Low
19	TINT6H	Timer 6 Interrupt High
20	TINT7L	Timer 7 Interrupt Low
21	TINT7H	Timer 7 Interrupt High
22	TINT8L	Timer 8 Interrupt Low
23	TINT8H	Timer 8 Interrupt High
24	TINT9L	Timer 9 Interrupt Low
25	TINT9H	Timer 9 Interrupt High
26	TINT10L	Timer 10 Interrupt Low
27	TINT10H	Timer 10 Interrupt High
28	TINT11L	Timer 11 Interrupt Low
29	TINT11H	Timer 11 Interrupt High
30	PRINT	UTOPIA-PDMA Receive Interrupt
31	PXINT	UTOPIA-PDMA Transmit Interrupt

(1) This system event is generated from within the C64x+ megamodule.
(2) RIO_INT0 to RIO_INT5 are routed to Core0 to Core5, respectively.
(3) EDMA3CC_INT0 (MASK 0) to EDMA3CC_INT5 (MASK 5) are routed to Core0 to Core5, respectively.

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Table 7-10. C6472 DSP Interrupts (continued)

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
32	RFSINT0	TSIP0 Receive Frame Sync Interrupt
33	RSFINT0	TSIP0 Receive Super Frame Interrupt
34	XFSINT0	TSIP0 Transmit Frame Sync Interrupt
35	XSFINT0	TSIP0 Transmit Super Frame Interrupt
36	RFSINT1	TSIP1 Receive Frame Sync Interrupt
37	RSFINT1	TSIP1 Receive Super Frame Interrupt
38	XFSINT1	TSIP1 Transmit Frame Sync Interrupt
39	XSFINT1	TSIP1 Transmit Super Frame Interrupt
40	RFSINT2	TSIP2 Receive Frame Sync Interrupt
41	RSFINT2	TSIP2 Receive Super Frame Interrupt
42	XFSINT2	TSIP2 Transmit Frame Sync Interrupt
43	XSFINT2	TSIP2 Transmit Super Frame Interrupt
44	RIOINT6	RapidIO Common/Error Interrupt
45	RIOINT7	RapidIO Common/Error Interrupt
46 - 49	Reserved	
50	ERRINT0	TSIP0 Receive/Transmit Error Interrupt
51	Reserved	
52	ERRINT1	TSIP1 Receive/Transmit Error Interrupt
53	Reserved	
54	ERRINT2	TSIP2 Receive/Transmit Error Interrupt
55	Reserved	
56	UINT	UTOPIA Interrupt
57	EDMA3CC_ERRINT	EDMA3CC Error Interrrupt
58	EDMA3CC_MPINT	EDMA3CC Memory Protection Interrupt
59	EDMA3TC_ERRINT0	EDMA3TC0 Error Interrupt
60	EDMA3TC_ERRINT1	EDMA3TC1 Error Interrupt
61	EDMA3TC_ERRINT2	EDMA3TC2 Error Interrupt
62	EDMA3TC_ERRINT3	EDMA3TC3 Error Interrupt
63	SMCMPINT	SMC Memory Protection Interrupt
64	SMCPEVT	SMC Profiler Consolidated Event
65	PSC_ALLINT	Power & Sleep Controller Interrupt
66	EDMA3CC_AETEVT	EDMA3CC AET Event
67 (4)	EDMA3CC_INT6	EDMA3CC Completion Interrupt – Mask 6
68 (4)	EDMA3CC_INT7	EDMA3CC Completion Interrupt – Mask 7
69	EDMA3CC_GINT	EDMA3CC GINT
70	MACINT0	Ethernet MAC0 Common Interrupt
71	MACINT1	Ethernet MAC1 Common Interrupt
72	I2CINT	I2C Interrupt
73	GPINT_LOCAL	Local GPIO Interrupt
74	GPINT6	GPIO Interrupt
75	GPINT7	GPIO Interrupt
76	GPINT8	GPIO Interrupt
77	GPINT9	GPIO Interrupt
78	GPINT10	GPIO Interrupt
79	GPINT11	GPIO Interrupt
80	GPINT12	GPIO Interrupt

(4) Routed to all six cores.

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Table 7-10. C6472 DSP Interrupts (continued)

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
81	GPINT13	GPIO Interrupt
82	GPINT14	GPIO Interrupt
83	GPINT15	GPIO Interrupt
84	IPC_LOCAL	Inter-DSP Interrupt (from IPCGRx register)
85	HPI_INT	Host Common Interrupt (from DSPINT bit of the HPIC register)
86	Reserved	
87	CPUINT0	Interrupt from CPU0
88	CPUINT1	Interrupt from CPU1
89	CPUINT2	Interrupt from CPU2
90	CPUINT3	Interrupt from CPU3
91	CPUINT4	Interrupt from CPU4
92	CPUINT5	Interrupt from CPU5
93	L2PDWAKE	L2 Wake Interrupt
94 - 95	Reserved	
96 (5)	INTERR	Dropped CPU Interrupt Event
97 (5)	EMC_IDMAERR	Invalid IDMA Parameters
98 (5)	PBISTINT	PBIST Interrupt
99 - 112	Reserved	
113 (5)	PMC_ED	Single Bit Error Detected During DMA Read
114 - 115	Reserved	
116 (5)	UMC_ED1	Corrected Bit Error Detected
117 (5)	UMC_ED2	Uncorrected Bit Error Detected
118 (5)	PDC_INT	Power Down Sleep Interrupt
119	Reserved	
120 (5)	PMC_CMPA	CPU Memory Protection Fault
121 (5)	PMC_DMPA	DMA Memory Protection Fault
122 (5)	DMC_CMPA	CPU Memory Protection Fault
123 (5)	DMC_DMPA	DMA Memory Protection Fault
124 (5)	UMC_CMPA	CPU Memory Protection Fault
125 (5)	UMC_DMPA	DMA Memory Protection Fault
126 (5)	EMC_CMPA	CPU Memory Protection Fault
127 (5)	EMC_BUSERR	Bus Error Interrupt

(5) This system event is generated from within the C64x+ megamodule.

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7.6.2 NMI Pin-Generated Interrupts

An NMI interrupt may be asserted to individual C64x+ megamodules from the device pins. The NMI interrupt is initiated by asserting the NMI input (low), selecting the intended C64x+ megamodule(s) with the CORESEL[2:0] inputs, and then latching it with the rising LRESETNMIEN input. The NMI interrupt input must be removed (or de-asserted) from the C64x+ megamodule. This is done by the NMI pin being latched high by the rising LRESETNMIEN input while selecting the intended C64x+ megamodule with the CORESEL[2:0] inputs. Therefore, to assert and de-assert NMI, two LRESETNMIEN pulses are required where the first latches NMI low and the second latches NMI high. Timing requirements for NMI can be found in Table 7-16 and Figure 7-12.

7.6.3 GPIO Pin-Generated Interrupts

The C6472 device has 16 GPIOs. All GPIOs can be configured to generate interrupts. GPIO0-5 provide interrupts that are assigned one per core. Interrupts from GPIO6-15 are available to all cores. GPIO0-7 are also provided as event inputs to the EDMA. Timing for the GPIO interrupts can be found in Table 7-152 and Figure 7-65.

7.6.4 Host and Inter-DSP Interrupts

The C64x+ megamodules can assert an event to a host processor using HOUT. Table 7-11 provides the timing for the HOUT pulses. The external host or any of the six C64x+ megamodules can generate interrupts to other C64x+ megamodules. For more details, see Section 3.7.

Table 7-11. Switching Characteristics Over Recommended Operating Conditions for HOUT External Event(1)

(see Figure 7-7)

NO.			500/625/700			UNIT
			MIN	TYP	MAX	
1	$t_{w(HOUTH)}$	HOUT pulse duration high		24P		ns
2	$t_{w(HOUTL)}$	HOUT pulse duration low	24P			ns

(1) P = 1/CPU clock frequency in nanoseconds (ns).

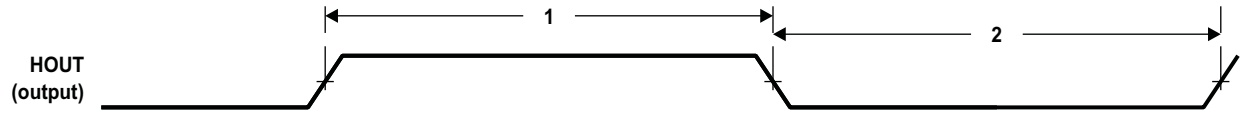

Figure 7-7. HOUT External Event

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7.7 Reset Controller

The reset controller detects the different type of resets supported on the C6472 device and manages the distribution of those resets throughout the device.

The C6472 device has several types of resets: power-on reset, system reset, warm reset, CPU local reset, and module reset. Table 7-12 explains further the types of reset, the reset initiator, and the effects of each reset on the chip. See Section 7.7.8, *Reset Electrical Data/Timing*, for more information on the effects of each reset on the PLL controllers and their clocks.

Table 7-12. Reset Types

TYPE	INITIATOR	EFFECT(s)
Power-on Reset	$\overline{\text{POR}}$ pin	Resets the entire chip including the emulation logic. Device configuration inputs are latched. Memory contents are not preserved. Device reset status output ($\overline{\text{RESETSTAT}}$) pin asserted (low).
Warm Reset	$\overline{\text{RESET}}$ pin	Reset on all chip components, except for emulation and PLL3. Device configuration inputs are latched. Memory contents are not preserved. Device reset status output ($\overline{\text{RESETSTAT}}$) pin asserted (low).
System Reset	Emulator Watchdog timer timeout	A system reset maintains memory contents and does not reset the emulation logic. The device configuration pins are not re-latched and the state of the peripherals (enabled/disabled) is not affected. This is a software-initiated reset that has the effect of a warm reset. Device reset status output ($\overline{\text{RESETSTAT}}$) pin asserted (low).
C64x+ Megamodule Local Reset	$\overline{\text{LRESET}}$ pin PSC Watchdog timer timeout	Provides a local reset of the C64x+ megamodule only. Memory contents are maintained. The device configuration pins are not re-latched. C64x+ megamodule slave DMA port remains alive when the C64x+ megamodule is in local reset.
Module Reset	Software (PSC MMR bit)	Only the module controlled by the LPSC gets reset

7.7.1 Power-on Reset

Power-on Reset is initiated by the $\overline{\text{POR}}$ pin and is used to reset the entire chip, including the emulation logic. Power-on Reset is also referred to as a cold reset since the device usually goes through a power-up cycle. During power-up, the $\overline{\text{POR}}$ pin must be asserted (driven low) until the power supplies have reached their normal operating conditions. Note that a device power-up cycle is not required to initiate a Power-on Reset.

The following sequence must be followed during a Power-on Reset:

1. Wait for all power supplies to reach normal operating conditions while keeping the $\overline{\text{POR}}$ pin asserted (driven low). While $\overline{\text{POR}}$ is asserted, all output buffers are set to high-impedance and the internal pull-up and pull-down resistors, on those buffers that have them, are enabled (except for those disabled by the six multiplexed GPIO pins). All peripherals, except those selected for boot purposes, are disabled after a power-on reset and must be enabled through the device state control registers; for more details, see Section 3.3, *Peripheral Selection After Device Reset*.
2. Once all the power supplies are within valid operating conditions, the $\overline{\text{POR}}$ pin must remain asserted (low) for a minimum of 256 CLKIN cycles; where CLKIN is the slowest of the active inputs CLKIN1, CLKIN2, and CLKIN3. The PLL1 controller input clock (CLKIN1), the PLL2 controller input clock (CLKIN2), and the PLL3 controller input clock (CLKIN3) must be valid during this time, if they are used. If the DDR2 memory controller is not needed, CLKIN3 can be tied low. Similarly, if the EMAC peripheral is not needed, CLKIN2 can be tied low. If both CLKIN2 and CLKIN3 are tied low, the $\overline{\text{POR}}$ pin must remain asserted (low) for a minimum of 256 CLKIN1 cycles after all power supplies have reached valid operating conditions.

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Within the low period of the POR pin, the following happens:
- The reset signals flow to the entire chip (including the emulation logic), resetting modules that use reset asynchronously.
- The PLL1 controller clocks are started at the frequency of the system reference clock. The clocks are propagated throughout the chip to reset modules that use reset synchronously. By default, PLL1 is in reset and unlocked.
- The PLL2 controller clocks are started at the frequency of the EMAC reference clock. The clocks are propagated throughout the chip to reset modules that use reset synchronously. By default, PLL2 is in reset and unlocked.
- The PLL3 controller clocks are started at the frequency of the DDR2 reference clock. PLL3 is held in reset. Since the PLL3 controller always operates in PLL mode, the system reference clock and all the DDR2 clocks are invalid at this point.
- The RESETSTAT pin stays asserted (low), indicating the device is in reset.

3. The POR pin may now be deasserted (driven high) after the appropriate delay. When the POR pin is deasserted, the configuration pin values are latched and the PLL controllers change their system clocks to their default divide-down values. PLL3 is taken out of reset and automatically starts its locking sequence. Other device initialization is also started. PLL1 and PLL2 are held in reset.
4. After device initialization is complete, the RESETSTAT pin is deasserted (driven high). By this time, PLL3 has already completed its locking sequence and is outputting a valid clock.
5. The device is now out of reset, device execution begins as dictated by the selected boot mode (see Section 2.4, *Boot Mode Sequence*).

NOTE

To most of the device, reset is de-asserted only when the POR and RESET pins are both de-asserted (driven high). Therefore, in the sequence described above, if the RESET pin is held low past the low period of the POR pin, most of the device will remain in reset. The only exception being that PLL3 is taken out of reset as soon as POR is de-asserted (driven high), regardless of the state of the RESET pin. The RESET pin should not be tied together with the POR pin.

7.7.2 Warm Reset (RESET Pin)

A Warm Reset has the same effects as a Power-on Reset, except that in this case, the emulation logic and PLL3 are not reset.

The following sequence must be followed during a Warm Reset:

1. Hold the RESET pin low for a minimum of 24 CLKIN1 cycles. Within the low period of the RESET pin, the following happens:
   - All output buffers are set to high impedance and the internal pull-up and pull-down resistors, on those buffers that have them, are enabled (except for those disabled by the six multiplexed GPIO pins).
   - The reset signals flow to the entire chip (excluding the emulation logic), resetting modules that use reset asynchronously.
   - The PLL1 controller is reset, thereby switching back to bypass mode and resetting all its registers to their default values. PLL1 is placed in reset and loses lock. The PLL1 controller clocks start running at the frequency of the system reference clock. The clocks are propagated throughout the chip to reset modules that use reset synchronously.
   - The PLL2 controller is reset thereby switching back to bypass mode and resetting all its registers to their default values. PLL2 is placed in reset and loses lock. The PLL2 controller clocks start running at the frequency of the system reference clock. The clocks are propagated throughout the chip to reset modules that use reset synchronously.
   - The PLL3 controller is reset, thereby resetting all its registers to their default values. The PLL3 controller clocks start running at the frequency of the DDR2 reference clock. PLL3 is not reset, therefore it remains locked.

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– The RESETSTAT pin becomes active (low), indicating the device is in reset.

2. The RESET pin may now be released (driven inactive high). When the RESET pin is released, the configuration pin values are latched and the PLL controllers immediately change their system clocks to their default divide-down values. Other device initialization is also started.
3. After device initialization is complete, the RESETSTAT pin goes inactive (high).
4. The device is now out of reset, device execution begins as dictated by the selected boot mode (see Section 2.4, *Boot Mode Sequence*).

NOTE

The POR pin should be held inactive (high) throughout the Warm Reset sequence. Otherwise, if POR is activated (brought low), the minimum POR pulse width must be met. The RESET pin should not be tied together with the POR pin.

7.7.3 System Reset

System Reset is initiated by:

- The emulator
- The local watchdog timeout (when Reset mux is configured to route this as System Reset)

A System Reset maintains memory contents and does not reset the clock logic or the emulation circuitry. The device configuration pins are also not re-latched and the state of the peripherals (enabled/disabled) is also not affected. A System Reset is initiated by the emulator or watchdog timer. For information on how to configure the action corresponding to a watchdog timeout, see Section 3.8.2, *Reset Mux Registers*.

During a System Reset, the following happens:

1. The reset is allowed to propagate through the system. Internal system clocks are not affected.
2. The PLL controllers retain their configuration. The PLLs also remain locked.
3. The RESETSTAT pin goes low to indicate an internal reset is being generated.
4. The boot sequence is started after the system clocks are re-aligned. Since the configuration pins (including the BOOTMODE[3:0] pins) are not latched with a System Reset, the previous values, as shown in the DEVSTAT register, are used to select the boot mode.

NOTE

A System Reset should not be used if the peripheral used for boot loading was disabled following boot.

7.7.4 Local Reset

The Local Reset provides a local reset to the C64x+ megamodule, without destroying clock alignment or memory contents. It does not affect any chip components. Local reset is initiated by asserting the LRESET input (low), selecting the intended C64x+ megamodule(s) with the CORESEL[2:0] inputs, and then latching it with the rising LRESETNMIEN input. The C64x+ megamodule(s) are held in reset until LRESET input is latched high by the rising LRESETNMIEN input while selecting the intended C64x+ megamodule with the CORESEL[2:0] inputs. Therefore, to assert and de-assert LRESET, two LRESETNMIEN pulses are required where the first latches LRESET low and the second latches LRESET high. Timing requirements for Local Reset can be found in Table 7-16 and Figure 7-12.

The external system is not notified of this reset. Once LRESET is deasserted, C64x+ megamodule goes through a local boot sequence. In certain cases, a watchdog timeout may also cause a local reset of an individual C64x+ megamodule. For information on how to configure the action corresponding to a watchdog timeout, see Section 3.8.2, *Reset Mux Registers*.

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7.7.5 Module Reset

Module reset is initiated by LPSC and only resets the module controlled by that LPSC. To prevent stalls, care must be taken when using this reset.

7.7.6 Reset Priority

If any of the above reset sources occur simultaneously, the PLLCTRL only processes the highest priority reset request. The rest request priorities are as follows (high to low):

- Power-on Reset
- Warm Reset
- System Reset
- Local Reset

7.7.7 Reset Controller Register

The reset type status (RSTYPE) register (029A 00E4) is the only register for the reset controller. This register falls in the same memory range as the PLL1 controller registers [029A 0000 - 029A 01FF].

7.7.7.1 Reset Type Status Register Description

The rest type status (RSTYPE) register latches the cause of the last reset. If multiple reset sources occur simultaneously, this register latches the highest priority reset source. The reset type status register is shown in Figure 7-8 and described in Table 7-13.

31	16
Reserved	
R-0	

15	4	3	2	1	0
Reserved		SRST	Rsvd	WRST	POR
R-0		R-x	R-0	R-x	R-x

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 7-8. Reset Type Status Register (RSTYPE) [Hex Address: 029A 00E4]

Table 7-13. Reset Type Status Register (RSTYPE) Field Descriptions

Bit	Field	Value	Description
31:4	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
3	SRST		System reset.
		0	System Reset was not the last reset to occur.
		1	System Reset was the last reset to occur.
2	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	WRST		Warm reset.
		0	Warm Reset was not the last reset to occur.
		1	Warm Reset was the last reset to occur.
0	POR		Power-on reset.
		0	Power-on Reset was not the last reset to occur.
		1	Power-on Reset was the last reset to occur.

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7.7.8 Reset Electrical Data/Timing

NOTE

If a configuration pin must be routed out from the device, the internal pullup/pulldown (IPU/IPD) resistor should not be relied upon; TI recommends the use of an external pullup/pulldown resistor.

For Figure 7-9, note the following:

- Low group pins consist of all 3.3-V I/O/Z and O/Z pins that have active internal pull-down (IPD) resistors. These pins become low as soon as the DV_{DD33} power supply has reached normal operating conditions. (These pins are high impedance prior to DV_{DD33} reaching a valid level.) These pins remain low until configured otherwise by their respective peripheral. For a list of pins containing IPD resistors, see Table 2-5, *Terminal Functions*.
- High group pins consist of all 3.3-V I/O/Z and O/Z pins that have active internal pull-up (IPU) resistors. These pins become high as soon as the DV_{DD33} power supply has reached normal operating conditions. (These pins are high impedance prior to DV_{DD33} reaching a valid level.) These pins remain high until configured otherwise by their respective peripheral. For a list of pins containing IPU resistors, see Table 2-5, *Terminal Functions*.
- Z group pins consist of all I/O/Z and O/Z pins associated with I2C, RGMII, DDR2 and RapidIO, as well as 3.3-V pins that have IPU/IPD functionality disabled by one of the six multiplexed GPIO pins. These pins are high impedance prior to power supply ramp and remain that way when their respective power supply has reached normal operating conditions. These pins remain in high impedance until configured otherwise by their respective peripheral.
- Each peripheral must be enabled through software to use it following a Power-on Reset; for more details, see Section 7.7.1, *Power-on Reset*, of this document.
- For power-supply sequence requirements, see Section 7.3.1, *Power-Supply Sequencing*.

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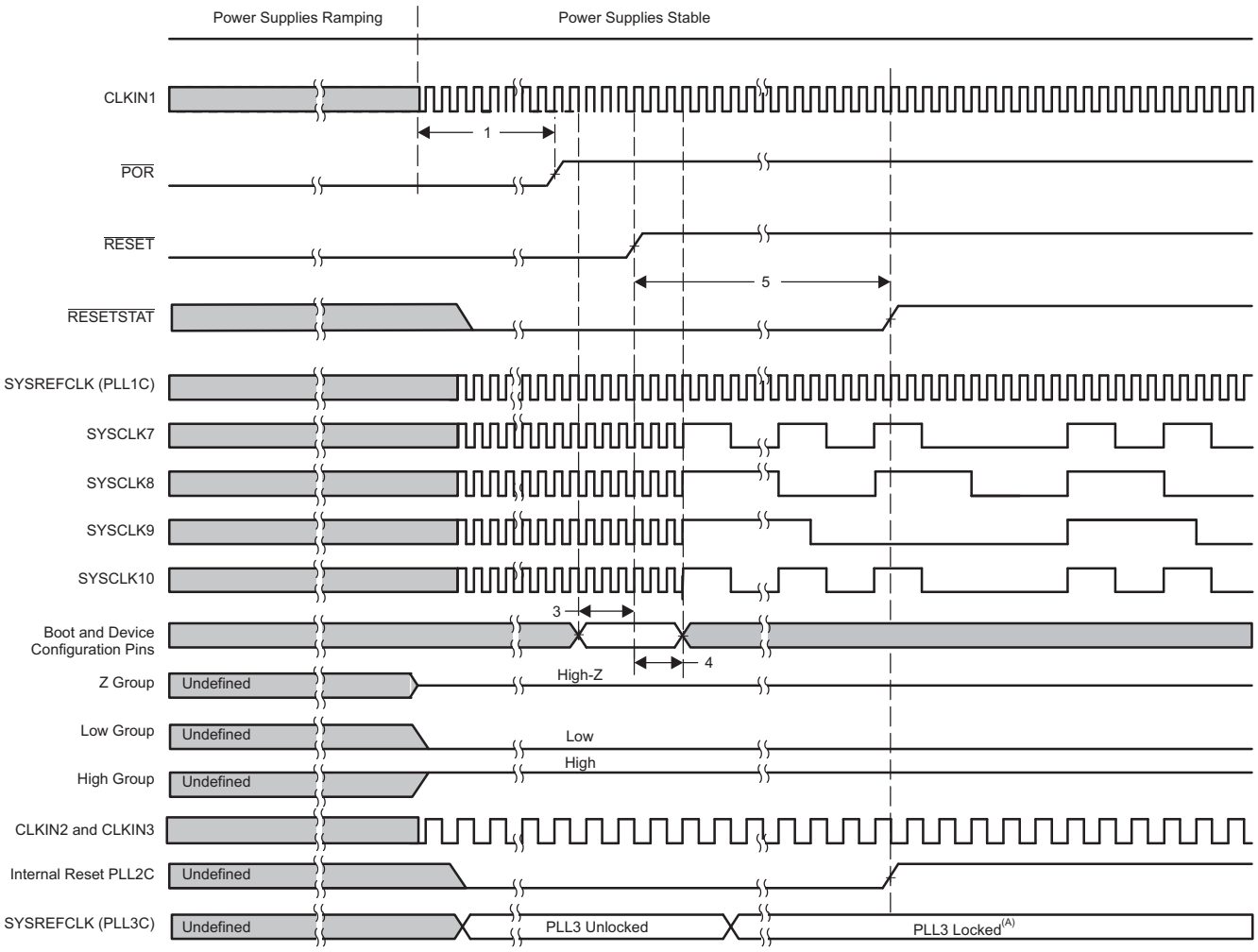

A. SYSREFCLK of the PLL2 controller and PLL3 controller runs at CLKIN2 ×20 and CLKIN3 ×20, respectively.

B. Power supplies, CLKIN1, CLKIN2 and CLKIN3 (if used) must be stable before the start of $t_{w(POR)}$.

Figure 7-9. Power-Up Timing

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Table 7-14. Timing Requirements for Reset(1)

(see Figure 7-10 and Figure 7-11)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(POR)}$	Width of the $\overline{POR}$ pulse	20(2)		µs
			256D(3)		
2	$t_{w(RST)}$	Width of the $\overline{RESET}$ pulse	20(2)		µs
			24C		
3	$t_{su(boot)}$	Setup time, boot configuration bits valid before $\overline{POR}$ or $\overline{RESET}$ high	12C		ns
4	$t_{h(boot)}$	Hold time, boot configuration bits valid after $\overline{POR}$ or $\overline{RESET}$ high	20		ns

(1) P = 1/CPU clock frequency in nanoseconds (ns); C = 1/CLKIN1 clock frequency in ns; D = 1/CLKIN* clock frequency in ns, where * is the slowest of CLKIN1, CLKIN2, or CLKIN3.
(2) No external pulls on GPIO.
(3) With board assistance to reduce the RC time constant.

Table 7-15. Switching Characteristics Over Recommended Operating Conditions for Reset

(see Figure 7-10 and Figure 7-11)

NO.			500/625/700		UNIT
			MIN	MAX	
5	$t_{d(PORH-RSTATH)}$	Delay time, $\overline{POR}$ high and/or $\overline{RESET}$ high to $\overline{RESETSTAT}$ high		15000C	ns

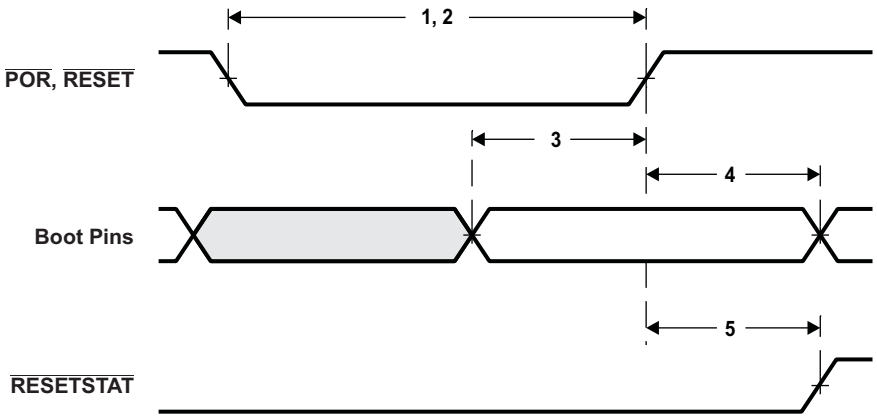
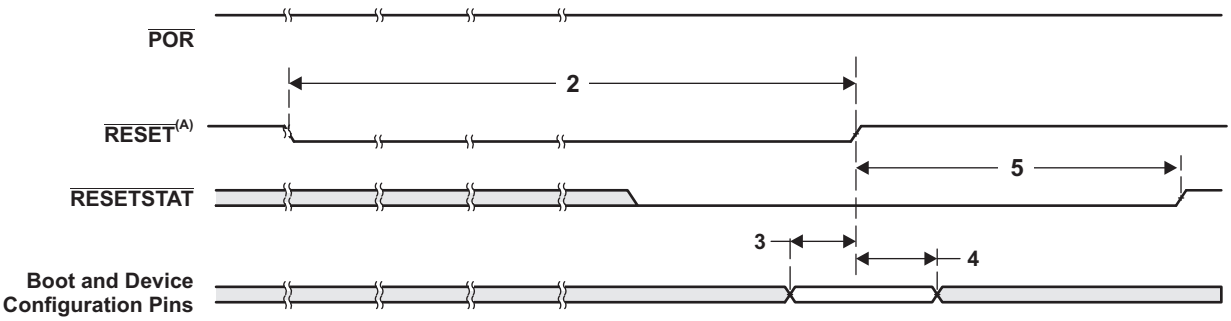


Figure 7-10. Power-on Reset Timing



A. $\overline{RESET}$ should only be used after device has been powered up.

Figure 7-11. Warm Reset Timing

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Table 7-16. Timing Requirements for Local Reset[1]

(see Figure 7-12)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(\overline{LRESETNMIEN})}$	Width of the $\overline{LRESETNMIEN}$ pulse	12P		ns
2	$t_{su(\overline{LRESET}, \overline{NMI}, \text{and CORESEL[2:0]})}$	Setup time, $\overline{LRESET}$, $\overline{NMI}$, and CORESEL[2:0] valid before $\overline{LRESETNMIEN}$ low	12P		ns
3	$t_{h(\overline{LRESET}, \overline{NMI}, \text{and CORESEL[2:0]})}$	Hold time, $\overline{LRESET}$, $\overline{NMI}$, and CORESEL[2:0] valid after $\overline{LRESETNMIEN}$ high	12P		ns

(1) P = 1/CPU clock frequency in nanoseconds (ns).

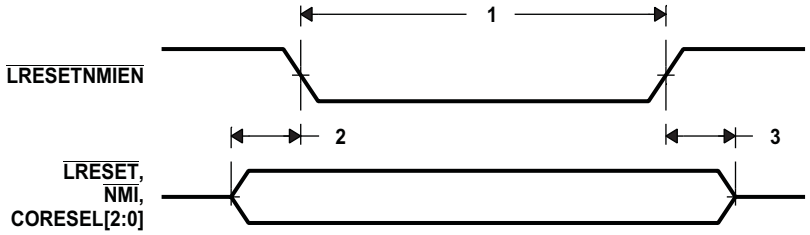

Figure 7-12. Local Reset Timing

Table 7-17. Switching Characteristics Over Recommended Operating Conditions for Boot Timing[1]

(see Figure 7-13)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(BOOTACTIVE)}$	Pulse duration, BOOTACTIVE high edge to BOOTACTIVE low edge	12P		ns

(1) P = 1/CPU clock frequency in nanoseconds (ns).

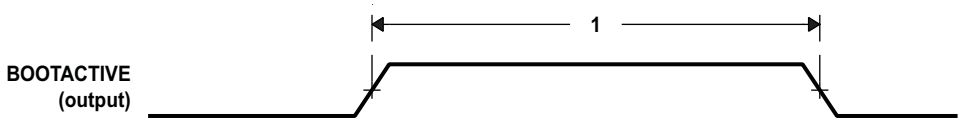

Figure 7-13. BOOTACTIVE Timing

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7.8 PLL1 and PLL1 Controller

The C6472 device includes a PLL1 and a software-programmable PLL1 controller. The PLL1 controller is able to generate different clocks for different parts of the system (i.e., megamodule, DSP core, Peripheral Data Bus, and other peripherals). There is no hardware CLKMODE selection on the C6472 device. The PLL multiply factor is set in software after reset.

NOTE

The PLL controller module as described in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) includes a superset of features, some of which are not supported on the C6472 DSP. The following sections describe the features that are supported; it should be assumed that any feature not included in these sections is not supported by the C6472 DSP.

7.8.1 PLL1 Controller Device-Specific Information

7.8.1.1 Internal Clocks and Maximum Operating Frequencies

As shown in Figure 7-14, the PLL1 controller generates several internal clocks including the system clock output (SYSCLKOUT) and the system clocks (SYSCLK1 through SYSCLK10). SYSCLK10 has a programmable divider. All other SYSCLK*n* clocks have a fixed relationship to the CPU clock.

- SYSCLK1 through SYSCLK6 are used to clock C64x+ Megamodule0 through C64x+ Megamodule5.
- SYSCLK7 is used for EDMA3CC, EDMA3TC, DMA SCR, Config SCR, boot controller, bridges, and some peripherals.
- SYSCLK8 is used for PSC, some peripherals, and SYSCLKOUT external pin.
- SYSCLK9 is used for shared memory controller and memory.
- SYSCLK10 is used for C64x+ megamodule trace logic.

NOTE

There is a minimum and maximum operating frequency for CLKIN1 and SYSCLK*n*. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). See Table 7-18 for the PLL clocks input and output frequency ranges.

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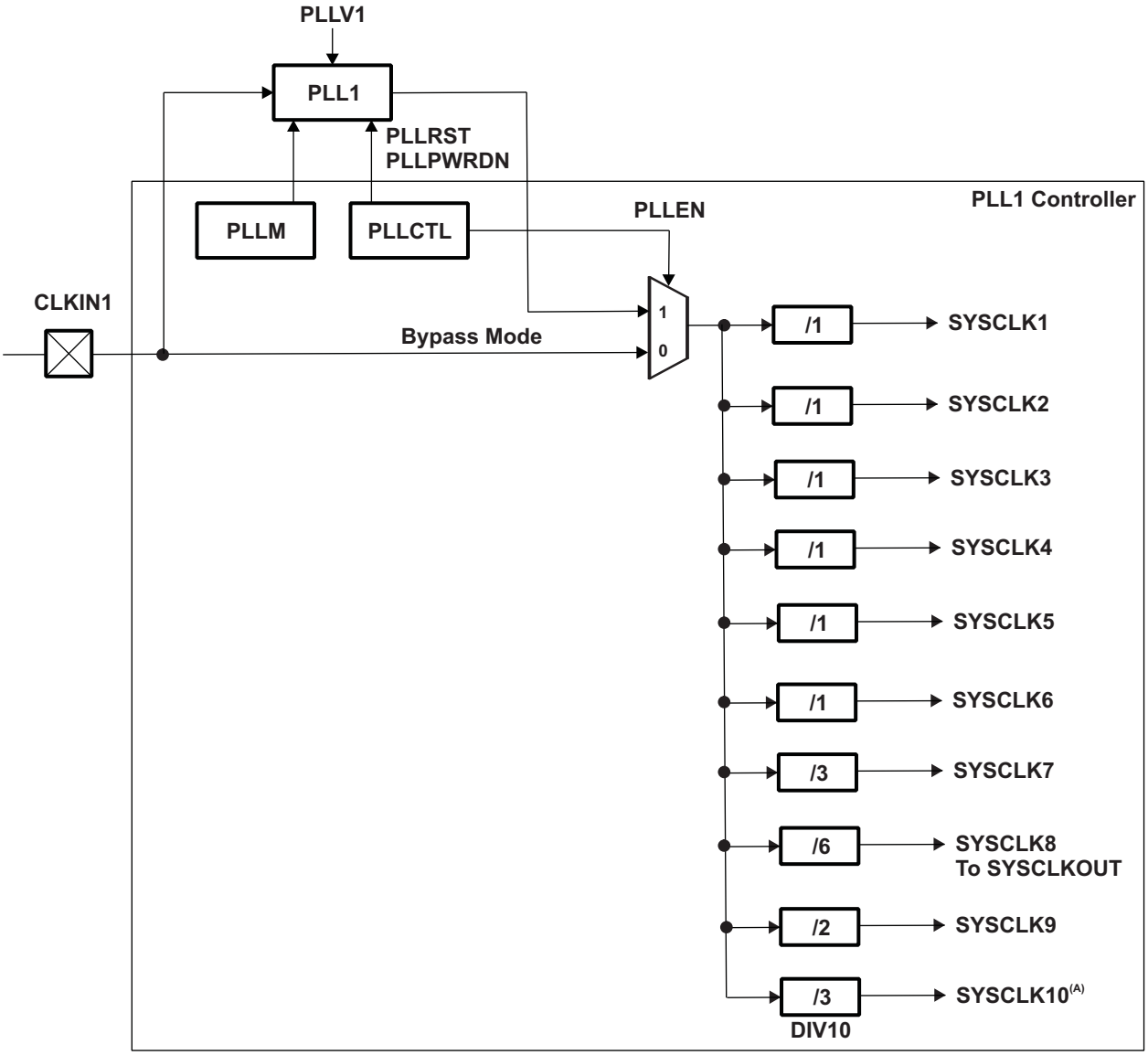

A. SYSCLK10 is programmable.

Figure 7-14. PLL1 and PLL1 Controller

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Table 7-18. PLL1 Clock Frequency Ranges

CLOCK SIGNAL	REQUIRED FREQUENCY FOR 500-MHz OPERATION	REQUIRED FREQUENCY FOR 625-MHz OPERATION	REQUIRED FREQUENCY FOR 700-MHz OPERATION	UNIT
CLKIN1	15.625 - 50.0	19.531 - 50.0	21.875 - 50.0	MHz
SYSCLK1	500.0	625.0	700.0	MHz
SYSCLK2	500.0	625.0	700.0	MHz
SYSCLK3	500.0	625.0	700.0	MHz
SYSCLK4	500.0	625.0	700.0	MHz
SYSCLK5	500.0	625.0	700.0	MHz
SYSCLK6	500.0	625.0	700.0	MHz
SYSCLK7	166.7	208.4	233.3	MHz
SYSCLK8	83.3	104.1	116.7	MHz
SYSCLK9	250.0	312.5	350.0	MHz
SYSCLK10	166.7(1)	208.4(1)	233.3(1)	MHz

(1) This frequency may be changed by reprogramming SYSCLK10.

7.8.1.2 PLL1 Controller Operating Modes

The PLL1 controller has two modes of operation: bypass mode and PLL mode. The mode of operation is determined by the PLLEN bit of the PLL control register (PLLCTL). In PLL mode, SYSREFCLK is generated from the device input clock, CLKIN1, using the the PLL multiplier, PLLM. In bypass mode, CLKIN1 is fed directly to SYSREFCLK. All hosts (HPI, etc.) must hold off accesses to the DSP while the frequency of its internal clocks is changing. A mechanism must be in place such that the DSP notifies the host when the PLL configuration has completed.

The PLL3 controller provides the control to reset PLL3. It is also capable of placing it in a power-down condition for systems where DDR2 EMIF is not being used.

7.8.1.3 PLL1 Stabilization, Lock, and Reset Times

The PLL stabilization time is the amount of time that must be allotted for the internal PLL regulators to become stable after device powerup. The PLL output should not be used until this stabilization time has expired. The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL1 reset time value, see Table 7-19.The PLL lock time is the amount of time needed from when the PLL is taken out of reset (PLLRST = 1 with PLLEN = 0) to when the PLL controller can be switched to PLL mode (PLLEN=1). The PLL1 lock time is given in Table 7-19.

Table 7-19. PLL1 Stabilization, Lock, and Reset Times

	MIN	TYP	MAX	UNIT
PLL1 stabilization time	50			µs
PLL1 lock time			2000 * C(1)	ns
PLL1 reset time	256 * C(1)			ns

(1) C = CLKIN1 cycle time in ns. For example, when CLKIN1 frequency is 50 MHz, use C = 20 ns.

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7.8.2 PLL1 Controller Peripheral Register Descriptions

The memory map of the PLL1 controller is shown in Table 7-20. Note that only registers documented here are accessible on the C6472. Other addresses in the PLL1 controller memory map are reserved and should not be modified.

Table 7-20. PLL1 Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
029A 0000	PID	Peripheral Identification Register [value: 0001 0802h]
029A 0004 - 029A 00E0	-	Reserved
029A 00E4	RSTYPE	Reset Type Status Register
029A 00E8 - 029A 00FC	-	Reserved
029A 0100	PLLCTL	PLL Control Register
029A 0104 - 029A 010C	-	Reserved
029A 0110	PLLM	PLL Multiplier Control Register
029A 0114 - 029A 0134	-	Reserved
029A 0138	PLLCMD	PLL Controller Command Register
029A 013C	PLLSTAT	PLL Controller Status Register
029A 0140	-	Reserved
029A 0144	DCHANGE	PLLDIV Ratio Change Status Register
029A 0148 - 029A 01FC	-	Reserved
029A 0150	SYSTAT	SYSCLK Status Register
029A 0154 - 029A 0174	-	Reserved
029A 0178	PLLDIV10	PLL Controller Divider 10 Register for SYSCLK10
029A 017C - 029A 03FC	-	Reserved

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7.8.3 PLL1 Controller Registers

This section provides a description of the PLL1 controller registers. For details on the operation of the PLL controller module, see the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806).

NOTE

Not all of the registers documented in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) are supported on the C6472. Only those registers documented in this section are supported. Furthermore, only the bits within the registers described here are supported. Users should not write to any reserved memory location or change the value of reserved bits.

7.8.3.1 PLL1 Peripheral ID Register (PID)

The peripheral identification register (PID) is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect).

31–24	23–16	15–8	7–0
Reserved	TYPE	CLASS	REV
R-0	R-01	R-08	R-0D

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 7-15. Peripheral ID Register (PID)

Table 7-21. Peripheral ID Register (PID) Field Descriptions

Bit	Field	Value	Description
31:24	Reserved		Reserved
23:16	TYPE	01h	Peripheral Type
15:8	CLASS	08h	Peripheral Class
7:0	REV	0Dh	Peripheral Revision. Identifies the revision level of the specific instance of the peripheral.

7.8.3.2 Reset Type Status Register (RSTYPE)

The reset type status register (RSTYPE) is described in Section 7.7.7.1.

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7.8.3.3 PLL1 PLL Control Register (PLLCTL)

The PLL control register (PLLCTL) is shown in Figure 7-16 and described in Table 7-22.

31								16
Reserved								
R-00 0001h								

15	8	7	6	5	4	3	2	1	0
Reserved		Rsvd	Rsvd	Reserved		PLLRST	Rsvd	PLL PWRDN	PLLEN
R-00 0001h		R/W-0	R-1	R/W-10		R/W-1	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-16. PLL Control Register (PLLCTL)

Table 7-22. PLL Control Register (PLLCTL) Field Descriptions(1)

Bit	Field	Value	Description
31:8	Reserved		Reserved. The reserved bit location is always read as 00 0001h. A value written to this field has no effect.
7	Reserved		Reserved. Writes to this register must keep this bit as 0.
6	Reserved		Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
5:4	Reserved		Reserved. Writes to this register must always program these bits as 00.
3	PLLRST		PLL reset bit
		0	PLL reset is released
		1	PLL reset is asserted
2	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	PLLPWRDN		PLL power-down mode select bit
		0	PLL is operational
		1	PLL is placed in power-down state, i.e., all analog circuitry in the PLL is turned-off
0	PLLEN		PLL enable bit
		0	Bypass mode. PLL is bypassed. All the system clocks (SYSCLK*n*) are divided down directly from input reference clock (CLKIN1).
		1	PLL mode. PLL is not bypassed. PLL output path is enabled. All the system clocks (SYSCLK*n*) are divided down from PLL output.

(1) The value of this register is changed by the ROM bootloader.

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7.8.3.4 PLL1 PLL Multiply Control Register (PLLM)

The PLL multiplier control register (PLLM) defines the input reference clock frequency multiplier. The multiplier should be chosen such that the output frequency should not exceed device frequency; i.e., no more than 700 MHz for the 700-MHz device. The PLLM register is shown in Figure 7-16 and described in Table 7-23.

31	5	4	0
Reserved		PLLM	
R-0		R/W-13h	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-17. PLL Multiply Control Register (PLLM)

Table 7-23. PLL Multiply Control Register (PLLM) Field Descriptions

Bit	Field	Value	Description
31:5	Reserved		Reserved.
4:0	PLLM		PLL1 Multiplier Bits Defines the frequency multiplier of the input reference clock (CLKIN1).
		09h - 1Fh	x10 - x32 multiplier rate (multiplier is value + 1)

7.8.3.5 PLL1 PLL Controller Divider Register (PLLDIV10)

The (SYSREFCLK) frequency is divided by PLLDIV10 to get SYSCLK10. The PLL controller divider register (PLLDIV10) is shown in Figure 7-18 and described in Table 7-24.

31	16
Reserved	
R-0	

15	14	5	4	0
D*n*EN	Reserved		RATIO	
R/W-1	R-0		R/W-3	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-18. PLL Controller Divider Register (PLLDIV10)

Table 7-24. PLL Controller Divider Register (PLLDIV10) Field Descriptions

Bit	Field	Value	Description
31:16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	D*n*EN		Divider D*n* enable bit.
		0	Divider *n* is disabled. No clock output.
		1	Divider *n* is enabled.
14:5	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4:0	RATIO	0-1Fh	Divider ratio bits.
		0	Reserved
		1h	Reserved
		2h-1Fh	÷3 to ÷32. Divide frequency by 3 to divide frequency by 32.

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7.8.3.6 PLL1 PLL Controller Command Register (PLLCMD)

The PLL controller command register (PLLCMD) controls the SYSCLK rate change and phase alignment. The PLLCMD register is shown in Figure 7-19 and described in Table 7-25.

31	16
Reserved	
R-0	

15	2	1	0
Reserved		Rsvd	GOSET
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-19. PLL Controller Command Register (PLLCMD)

Table 7-25. PLL Controller Command Register (PLLCMD) Field Descriptions

Bit	Field	Value	Description
31:1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSET		GO operation command for SYSCLK rate change and phase alignment. Before setting this bit to 1 to initiate a GO operation, check the GOSTAT bit in the PLLSTAT register to ensure all previous GO operations have completed.
		0	No effect. Write of 0 clears bit to 0.
		1	Initiates GO operation. Write of 1 initiates GO operation. Once set, GOSET remains set but further writes of 1 can initiate the GO operation.

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7.8.3.7 PLL1 PLL Controller Status Register (PLLSTAT)

The PLL controller status register (PLLSTAT) shows the PLL controller status. PLLSTAT is shown in Figure 7-20 and described in Table 7-26.

31	16
Reserved	
R-0000 0000 0000 0000 0000 0000 0000 001	

15	1	0
Reserved		GOSTAT
R-0000 0000 0000 0000 0000 0000 0000 001		R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-20. PLL Controller Status Register (PLLSTAT)

Table 7-26. PLL Controller Status Register (PLLSTAT) Field Descriptions

Bit	Field	Value	Description
31:1	Reserved	0000 0000 0000 0000 0000 0000 0000 001	Reserved. A value written to this field has no effect.
0	GOSTAT		GO operation status.
		0	GO operation is not in progress. SYSCLK divide ratios are not being changed.
		1	GO operation is in progress. SYSCLK divide ratios are being changed.

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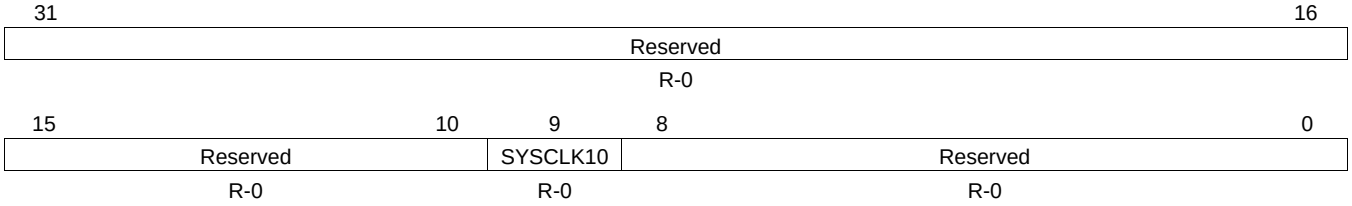
7.8.3.8 PLL1 PLLDIV Ratio Change Status Register (DCHANGE)

Whenever a different ratio is written to the PLLDIV10 register, the PLLCTRL flags the change in the PLLDIV ratio change status register (DCHANGE). During the GO operation, the PLL controller will only change the divide ratio of the SYSCLK with the bit set in DCHANGE. Note that changed clocks will be automatically aligned to other clocks if the corresponding ALN bit is set. The PLLDIV divider ratio change status register is shown in Figure 7-21 and described in Table 7-27.



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-21. PLLDIV Divider Ratio Change Status Register (DCHANGE)

Table 7-27. PLLDIV Divider Ratio Change Status Register (DCHANGE) Field Descriptions

Bit	Field	Value	Description
31:10	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to these fields has no effect.
9	SYSCLK10		Identifies when the SYSCLK10 divide ratio has been modified.
		0	SYSCLK10 ratio has not been modified. When GOSET is set, SYSCLK10 will not be affected.
		1	SYSCLK10 ratio has been modified. When GOSET is set, SYSCLK10 will change to the new ratio.
8:0	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to these fields has no effect.

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7.8.3.9 PLL1 SYSCLK Status Register (SYSTAT)

The SYSCLK status register (SYSTAT) shows the status of the system clocks (SYSCLK*n*). SYSTAT is shown in Figure 7-22 and described in Table 7-28.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved						SYS10ON	SYS9ON
R-0						R-1	R-1

7	6	5	4	3	2	1	0
SYS8ON	SYS7ON	SYS6ON	SYS5ON	SYS4ON	SYS3ON	SYS2ON	SYS1ON
R-1	R-1	R-1	R-1	R-1	R-1	R-1	R-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-22. SYSCLK Status Register (SYSTAT)

Table 7-28. SYSCLK Status Register (SYSTAT) Field Descriptions

Bit	Field	Value	Description
31:10	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
9:0	SYS*n*ON		SYSCLK*n* on status.
		0	SYSCLK*n* is gated.
		1	SYSCLK*n* is on.

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7.8.4 PLL1 Controller Input and Output Clock Electrical Data/Timing

Table 7-29. Timing Requirements for CLKIN1 Devices

(see Figure 7-23)

NO.			500/625/700 PLL MODES x10 to x32		UNIT
			MIN	MAX	
1	$t_{c(CLKIN1)}$	Cycle time, CLKIN1	20	80	ns
2	$t_{w(CLKIN1H)}$	Pulse duration, CLKIN1 high	0.4 * $t_{c(CLKIN1)}$		ns
3	$t_{w(CLKIN1L)}$	Pulse duration, CLKIN1 low	0.4 * $t_{c(CLKIN1)}$		ns
4	$t_{t(CLKIN1)}$	Transition time, CLKIN1		1.2	ns
5	$t_{J(CLKIN1)}$	Period jitter (peak-to-peak), CLKIN1		100	ps

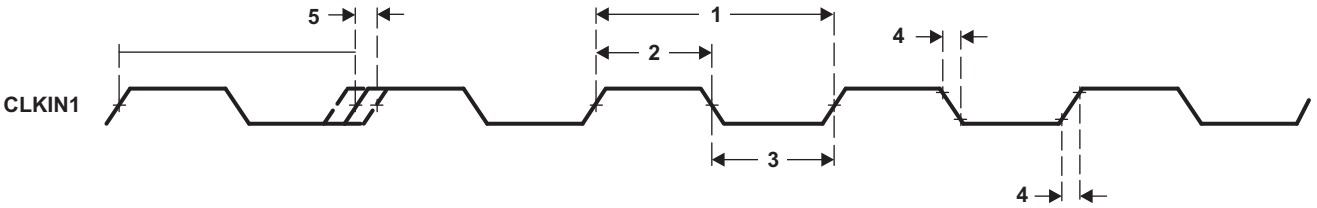

Figure 7-23. CLKIN1 Timing

Table 7-30. Switching Characteristics Over Recommended Operating Conditions for SYSCLKOUT [CPU/6](1)(2)

(see Figure 7-24)

NO.	PARAMETER		500/625/700 TYP	UNIT
1	$t_{c(CLK)}$	Cycle time, SYSCLKOUT	6P	ns
2	$t_{w(CLKH)}$	Pulse duration, SYSCLKOUT high	3P	ns
3	$t_{w(CLKL)}$	Pulse duration, SYSCLKOUT low	3P	ns

(1) The reference points for the rise and fall transitions are measured at 3.3 V V_{OL} MAX and V_{OH} MIN.
(2) P = 1/CPU clock frequency in nanoseconds (ns).

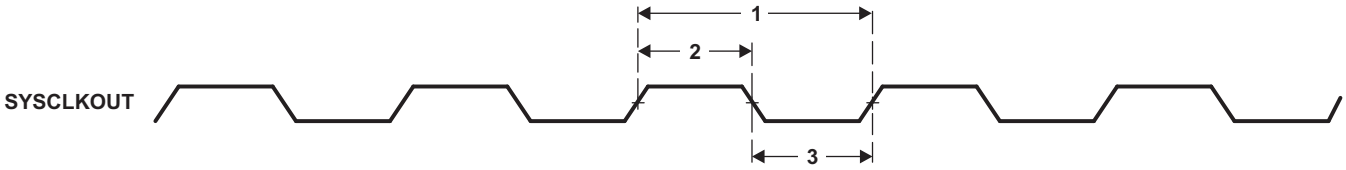

Figure 7-24. SYSCLKOUT Timing

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7.9 PLL2 and PLL2 Controller

The C6472 device includes a PLL2 and a software-programmable PLL2 controller. The PLL2 controller generates different clocks required for Gigabit Ethernet. The PLL multiply factor is set to x20 for PLL2.

NOTE

The PLL controller module as described in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) includes a superset of features, some of which are not supported on the C6472 DSP. The following sections describe the features that are supported; it should be assumed that any feature not included in these sections is not supported by the C6472 DSP.

7.9.1 PLL2 Controller Device-Specific Information

7.9.1.1 Internal Clocks and Maximum Operating Frequencies

As shown in Figure 7-25, the PLL2 controller generates EMAC reference clocks.

- SYSCLK13 is used by RGMII0 (1000Mbps mode)
- SYSCLK14 is used by RGMII0 (100Mbps mode) and GMII (1000Mbps mode)
- SYSCLK15 is used by RGMII0 (10Mbps mode)
- SYSCLK16 is used by RGMII1 (1000Mbps mode)
- SYSCLK17 is used by RGMII1 (100Mbps mode)
- SYSCLK18 is used by RGMII1 (10Mbps mode)

NOTE

There is a fixed operating frequency for CLKIN2 and SYSCLK13-18. The clock generator must not be configured to exceed any of these constraints (certain combinations of external clock input, internal dividers, and PLL multiply ratios might not be supported). For the PLL clocks input and output frequencies, see Table 7-31.

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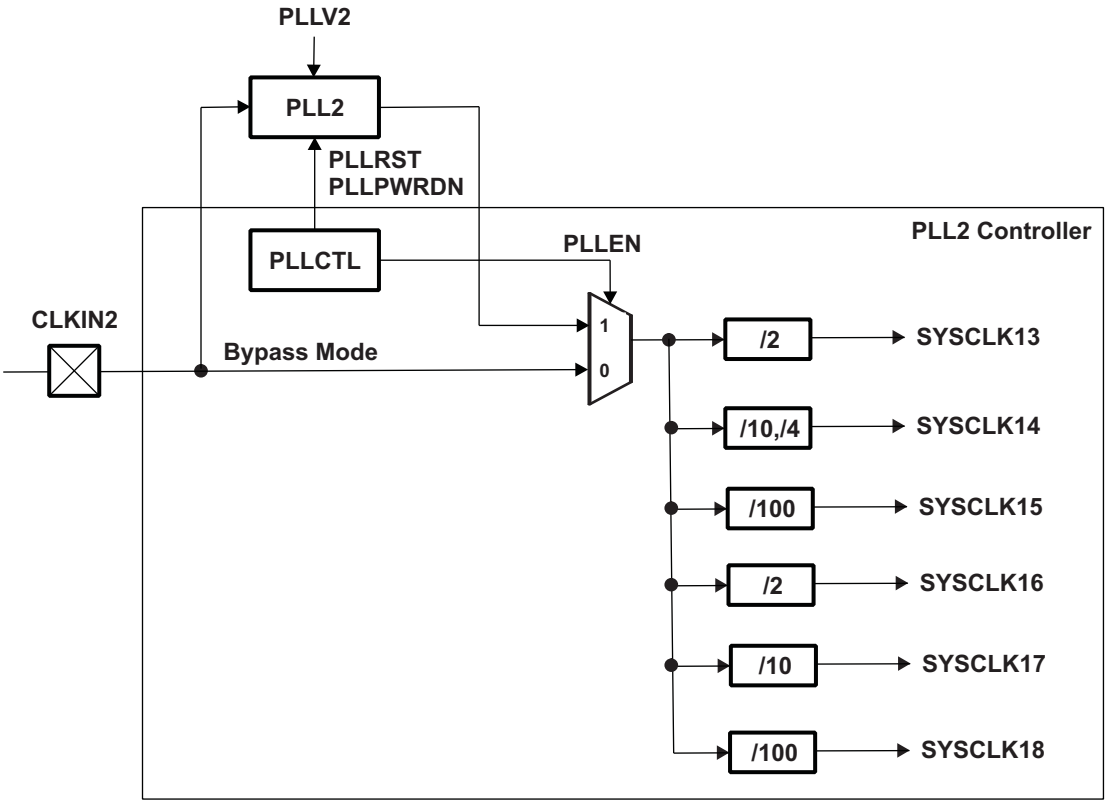

Figure 7-25. PLL2 and PLL2 Controller

Table 7-31. PLL2 Clock Frequency Ranges

CLOCK SIGNAL	REQUIRED FREQUENCY	UNIT
CLKIN2	25	MHz
SYSCLK13	250	MHz
SYSCLK14	50 or 125	MHz
SYSCLK15	5	MHz
SYSCLK16	250	MHz
SYSCLK17	50	MHz
SYSCLK18	5	MHz

7.9.1.2 PLL2 Controller

The PLL2 controller provides the control to reset PLL2. It is also capable of placing it in a power-down condition for systems where Ethernet is not being used.

7.9.1.3 PLL2 Stabilization, Lock, and Reset Times

The PLL stabilization time is the amount of time that must be allotted for the internal PLL regulators to become stable after device powerup. The PLL should not be operated until this stabilization time has expired. The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL2 reset time value, see Table 7-32. The PLL lock time is the amount of time needed from when the PLL is taken out of reset (PLLRST = 1 with PLLEN = 0) to when the PLL controller can be switched to PLL mode (PLLEN=1). The PLL2 lock time is given in Table 7-32.

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Table 7-32. PLL2 Stabilization, Lock, and Reset Times

	MIN	TYP	MAX	UNIT
PLL2 stabilization time	500			µs
PLL2 lock time			2000 * C(1)	ns
PLL2 reset time	128 * C(1)			ns

(1) C = CLKIN2 cycle time in ns. For example, when CLKIN2 frequency is 25 MHz, use C = 40 ns.

7.9.2 PLL2 Controller Peripheral Register Descriptions

The memory map of the PLL2 controller is shown in Table 7-33. Note that only registers documented here are accessible on the C6472. Other addresses in the PLL2 controller memory map should not be modified.

Table 7-33. PLL2 Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
029C 0000	PID	Constant Peripheral Identification Register
029C 0004 - 029C 00FC	-	Reserved
029C 0100	PLLCTL	PLL Control Register
029C 0104 - 029C 0114	-	Reserved
029C 0118	PLLDIV1	PLL Controller Divider 1 Register for SYSCLK13
029C 011C	PLLDIV2	PLL Controller Divider 2 Register for SYSCLK14
029C 0120	PLLDIV3	PLL Controller Divider 3 Register for SYSCLK15
029C 0124 - 029C 0134	-	Reserved
029C 0138	PLLCMD	PLL Controller Command Register
029C 013C	PLLSTAT	PLL Controller Status Register
029C 0140	-	Reserved
029C 0144	DCHANGE	PLLDIV Ratio Change Status Register
029C 0148 - 029C 014C	-	Reserved
029C 0150	SYSTAT	SYSCLK Status Register
029C 0154 - 029C 015C	-	Reserved
029C 0160	PLLDIV4	PLL Controller Divider 4 Register for SYSCLK16
029C 0164	PLLDIV5	PLL Controller Divider 5 Register for SYSCLK17
029C 0168	PLLDIV6	PLL Controller Divider 6 Register for SYSCLK18
029C 016C - 029C 03FC	-	Reserved

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7.9.3 PLL2 Controller Registers

This section provides a description of the PLL2 controller registers. For details on the operation of the PLL controller module, see the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806).

NOTE

Not all of the registers documented in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) are supported on the C6472. Only those registers documented in this section are supported. Furthermore, only the bits within the registers described here are supported. You should not write to any reserved memory location or change the value of reserved bits.

7.9.3.1 PLL2 Peripheral ID Register (PID)

The peripheral identification register (PID) is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect).

31 – 24	23 – 16	15 – 8	7 – 0
Reserved	TYPE	CLASS	REV
R-0	R-01	R-08	R-0D

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 7-26. Peripheral ID Register (PID)

Table 7-34. Peripheral ID Register (PID) Field Descriptions

Bit	Field	Value	Description
31:24	Reserved		Reserved
23:16	TYPE	01h	Peripheral Type
15:8	CLASS	08h	Peripheral Class
7	REV	0Dh	Peripheral Revision. Identifies the revision level of the specific instance of the peripheral.

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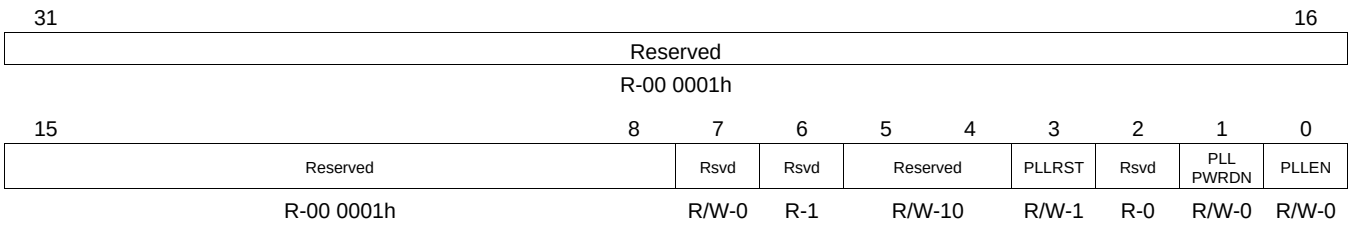
7.9.3.2 PLL2 PLL Control Register (PLLCTL)

The PLL control register (PLLCTL) is shown in Figure 7-27 and described in Table 7-35.



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-27. PLL Control Register (PLLCTL)

Table 7-35. PLL Control Register (PLLCTL) Field Descriptions[1]

Bit	Field	Value	Description
31:8	Reserved		Reserved. The reserved bit location is always read as 00 0001h. A value written to this field has no effect.
7	Reserved		Reserved. Writes to this register must keep this bit as 0.
6	Reserved		Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
5:4	Reserved		Reserved. Writes to this register must always program these bits as 00.
3	PLLRST		PLL reset bit
		0	PLL reset is released
		1	PLL reset is asserted
2	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	PLLPWRDN		PLL power-down mode select bit
		0	PLL is operational
		1	PLL is placed in power-down state, i.e., all analog circuitry in the PLL is turned-off
0	PLLEN		PLL enable bit
		0	Bypass mode. PLL is bypassed. All the system clocks (SYSCLK*n*) are divided down directly from input reference clock.
		1	PLL mode. PLL is not bypassed. PLL output path is enabled. All the system clocks (SYSCLK*n*) are divided down from PLL output.

(1) The value of this register is changed by the ROM bootloader.

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7.9.3.3 PLL2 PLL Controller Divider*n* Register (PLLDIV*n*)

The PLL controller divider registers 1 through 6 decide the frequency ratio for SYSCLK13 through SYSCLK18. The PLLDIV*n* register is shown in Figure 7-28 and described in Table 7-36.

31															16
Reserved															
R-0															

15	14						7	6							0
D*n*EN	Reserved							RATIO							
R/W-1	R-0							R/W-x							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-28. PLL Controller Divider Register (PLLDIV*n*)

Table 7-36. PLL Controller Divider Register (PLLDIV*n*) Field Descriptions

Bit	Field	Value	Description
31:16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	D*n*EN		Divider D*n* enable bit.
		0	Divider *n* is disabled. No clock output.
		1	Divider *n* is enabled.
14:7	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6:0	RATIO		Divider ratio bits.(1)
		0-7Fh	÷1 to ÷128. Divide frequency by 1 to divide frequency by 128.

(1) The divider ratio bits for each divider should be left at the default value.

Table 7-37. PLLDIV*n* Default Values

	PLLDIV1 SYSCLK13	PLLDIV2 SYSCLK14	PLLDIV3 SYSCLK15	PLLDIV4 SYSCLK16	PLLDIV5 SYSCLK17	PLLDIV6 SYSCLK18
MACSEL0[2:0] = all values except 010	1	9	99	1	9	99
MACSEL0[2:0] = 010	1	3	99	1	9	99

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7.9.3.4 PLL2 PLL Controller Command Register (PLLCMD)

The PLL controller command register (PLLCMD) contains the command bit for GO operation. PLLCMD is shown in Figure 7-29 and described in Table 7-38.

31	16
Reserved	
R-0	

15	2	1	0
Reserved		Rsvd	GOSET
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-29. PLL Controller Command Register (PLLCMD)

Table 7-38. PLL Controller Command Register (PLLCMD) Field Descriptions

Bit	Field	Value	Description
31:2	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSET		GO operation command for SYSCLK rate change and phase alignment. Before setting this bit to 1 to initiate a GO operation, check the GOSTAT bit in the PLLSTAT register to ensure all previous GO operations have completed.
		0	No effect. Write of 0 clears bit to 0.
		1	Initiates GO operation. Write of 1 initiates GO operation. Once set, GOSET remains set but further writes of 1 can initiate the GO operation.

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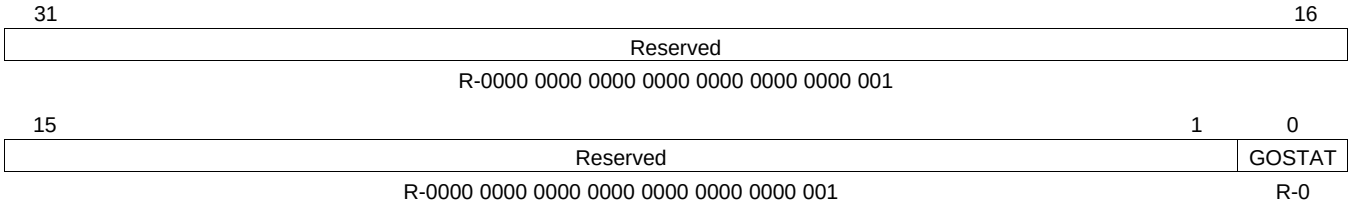
7.9.3.5 PLL2 PLL Controller Status Register (PLLSTAT)

The PLL controller status register (PLLSTAT) shows the PLL controller status. PLLSTAT is shown in Figure 7-30 and described in Table 7-39.



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-30. PLL Controller Status Register (PLLSTAT)

Table 7-39. PLL Controller Status Register (PLLSTAT) Field Descriptions

Bit	Field	Value	Description
31:1	Reserved	0000 0000 0000 0000 0000 0000 0000 001	Reserved. A value written to this field has no effect.
0	GOSTAT		GO operation status.
		0	GO operation is not in progress. SYSCLK divide ratios are not being changed.
		1	GO operation is in progress. SYSCLK divide ratios are being changed.

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7.9.3.6 PLL2 PLLDIV Ratio Change Status Register (DCHANGE)

Whenever a different ratio is written to the PLLDIV*n* registers, the PLLCTRL flags the change in the PLLDIV ratio change status registers (DCHANGE). During the GO operation, the PLL controller will only change the divide ratio of the SYSCLKs with the bit set in DCHANGE. Note that changed clocks will be automatically aligned to other clocks. The PLLDIV divider ratio change status register is shown in Figure 7-31 and described in Table 7-40.

31	16
Reserved	
R-0	

15	6	5	4	3	2	1	0
Reserved		SYSCLK18	SYSCLK17	SYSCLK16	SYSCLK15	SYSCLK14	SYSCLK13
R-0		R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 7-31. PLLDIV Divider Ratio Change Status Register (DCHANGE)

Table 7-40. PLLDIV Divider Ratio Change Status Register (DCHANGE) Field Descriptions

Bit	Field	Value	Description
31:6	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
5	SYSCLK18		Identifies when the SYSCLK18 divide ratio has been modified.
		0	SYSCLK18 ratio has not been modified. When GOSET is set, SYSCLK18 will not be affected.
		1	SYSCLK18 ratio has been modified. When GOSET is set, SYSCLK18 will change to the new ratio.
4	SYSCLK17		Identifies when the SYSCLK17 divide ratio has been modified.
		0	SYSCLK17 ratio has not been modified. When GOSET is set, SYSCLK17 will not be affected.
		1	SYSCLK17 ratio has been modified. When GOSET is set, SYSCLK17 will change to the new ratio.
3	SYSCLK16		Identifies when the SYSCLK16 divide ratio has been modified.
		0	SYSCLK16 ratio has not been modified. When GOSET is set, SYSCLK16 will not be affected.
		1	SYSCLK16 ratio has been modified. When GOSET is set, SYSCLK16 will change to the new ratio.
2	SYSCLK15		Identifies when the SYSCLK15 divide ratio has been modified.
		0	SYSCLK15 ratio has not been modified. When GOSET is set, SYSCLK15 will not be affected.
		1	SYSCLK15 ratio has been modified. When GOSET is set, SYSCLK15 will change to the new ratio.
1	SYSCLK14		Identifies when the SYSCLK14 divide ratio has been modified.
		0	SYSCLK14 ratio has not been modified. When GOSET is set, SYSCLK14 will not be affected.
		1	SYSCLK14 ratio has been modified. When GOSET is set, SYSCLK14 will change to the new ratio.
0	SYSCLK13		Identifies when the SYSCLK13 divide ratio has been modified.
		0	SYSCLK13 ratio has not been modified. When GOSET is set, SYSCLK13 will not be affected.
		1	SYSCLK13 ratio has been modified. When GOSET is set, SYSCLK13 will change to the new ratio.

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7.9.3.7 PLL2 SYSCLK Status Register (SYSTAT)

The SYSCLK status register (SYSTAT) shows the status of the system clocks (SYSCLK*n*). SYSTAT is shown in Figure 7-32 and described in Table 7-41.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved		SYS18ON	SYS17ON	SYS16ON	SYS15ON	SYS14ON	SYS13ON
R-0		R-1	R-1	R-1	R-1	R-1	R-1

LEGEND: R = Read only; -*n* = value after reset

Figure 7-32. SYSCLK Status Register (SYSTAT)

Table 7-41. SYSCLK Status Register (SYSTAT) Field Descriptions

Bit	Field	Value	Description
31:6	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
5:0	SYS*n*ON		SYSCLK*n* on status.
		0	SYSCLK*n* is gated.
		1	SYSCLK*n* is on.

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7.9.4 PLL2 Controller Input Clock Electrical Data/Timing

Table 7-42. Timing Requirements for CLKIN2 Devices

(see Figure 7-33)

NO.			500/625/700 PLL MODE x20		UNIT
			MIN	MAX	
1	$t_{c(CLKIN2)}$	Cycle time, CLKIN2	40	40	ns
2	$t_{w(CLKIN2H)}$	Pulse duration, CLKIN2 high	0.4 * $t_{c(CLKIN2)}$		ns
3	$t_{w(CLKIN2L)}$	Pulse duration, CLKIN2 low	0.4 * $t_{c(CLKIN2)}$		ns
4	$t_{t(CLKIN2)}$	Transition time, CLKIN2		1.2	ns
5	$t_{J(CLKIN2)}$	Period jitter (peak-to-peak), CLKIN2		100	ps

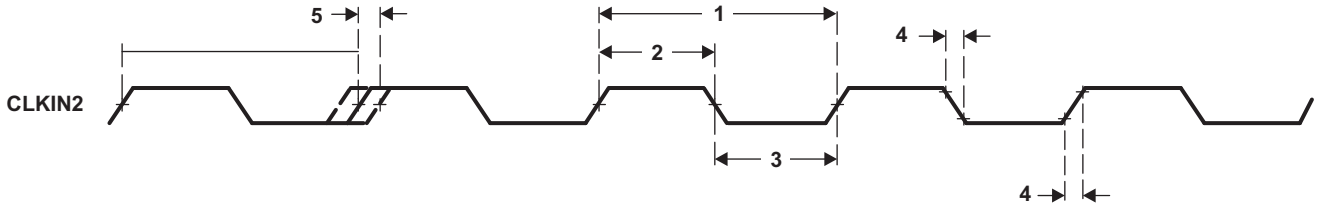

Figure 7-33. CLKIN2 Timing

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7.10 PLL3 and PLL3 Controller

The C6472 device includes a PLL3 and a software-programmable PLL3 controller. The PLL3 controller generates the clock. The PLL multiply factor is set to x20 for PLL3.

NOTE

The PLL controller module as described in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) includes a superset of features, some of which are not supported on the C6472 DSP. The following sections describe the features that are supported; it should be assumed that any feature not included in these sections is not supported by the C6472 DSP.

7.10.1 PLL3 Controller Device-Specific Information

7.10.1.1 Internal Clocks and Maximum Operating Frequencies

As shown in Figure 7-34, the PLL3 controller generates only one clock which is used for DDR2.

NOTE

There is a minimum and maximum operating frequency for CLKIN3 and DDR2 clock (the multiplier is fixed). The clock generator must not be configured to exceed any of these constraints. For the PLL clocks input and output frequencies, see Table 7-43.

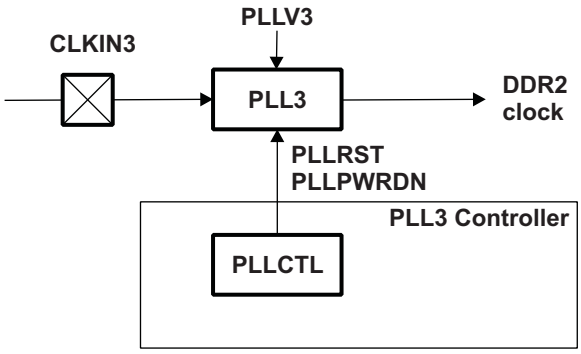

Figure 7-34. PLL3 and PLL3 Controller

Table 7-43. PLL3 Clock Frequency Ranges

CLOCK SIGNAL	REQUIRED FREQUENCY	UNIT
CLKIN3	20 - 26.66	MHz
PLLOUT (DDR2 clock)	400 - 533.33	MHz

7.10.1.2 PLL3 Controller

The PLL3 controller provides the control to reset PLL3. It is also capable of placing it in a power-down condition for systems where DDR2 EMIF is not being used.

7.10.1.3 PLL3 Stabilization, Lock, and Reset Times

The PLL stabilization time is the amount of time that must be allotted for the internal PLL regulators to become stable after device powerup. The PLL should not be operated until this stabilization time has

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expired. The PLL reset time is the amount of wait time needed when resetting the PLL (writing PLLRST = 1), in order for the PLL to properly reset, before bringing the PLL out of reset (writing PLLRST = 0). For the PLL3 reset time value, see Table 7-44. The PLL lock time is the amount of time needed from when the PLL is taken out of reset to when the output clock is ready for use. The PLL3 lock time is given in Table 7-44.

Table 7-44. PLL3 Stabilization, Lock, and Reset Times

	MIN	TYP	MAX	UNIT
PLL3 stabilization time	150			µs
PLL3 lock time			2000 * C(1)	ns
PLL3 reset time	128 * C(1)			ns

(1) C = CLKIN3 cycle time in ns. For example, when CLKIN3 frequency is 25 MHz, use C = 40 ns.

7.10.2 PLL3 Controller Peripheral Register Descriptions

The memory map of the PLL3 controller is shown in Table 7-45. Note that only registers documented here are accessible on the C6472. Other addresses in the PLL3 controller memory map should not be modified.

Table 7-45. PLL3 Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
029C 0400	PID	Constant Peripheral Identification Register
029C 0404 - 029C 04FC	-	Reserved
029C 0500	PLLCTL	PLL Control Register
029C 0504 - 029C 07FC	-	Reserved

7.10.3 PLL3 Controller Registers

This section provides a description of the PLL3 controller registers. For details on the operation of the PLL controller module, see the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806).

NOTE

The PLL3 controller registers can only be accessed using the CPU or the emulator. Not all of the registers documented in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (literature number SPRU806) are supported on the C6472. Only those registers documented in this section are supported. Furthermore, only the bits within the registers described here are supported. You should not write to any reserved memory location or change the value of reserved bits.

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7.10.3.1 PLL3 Peripheral ID Register

The peripheral identification register (PID) is a constant register that contains the ID and ID revision number for that module. The PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect).

31–24	23–16	15–8	7–0
Reserved	TYPE	CLASS	REV
R-0	R-01	R-08	R-0D

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 7-35. Peripheral ID Register (PID)

Table 7-46. Peripheral ID Register (PID) Field Descriptions

Bit	Field	Value	Description
31:24	Reserved		Reserved
23:16	TYPE	01h	Peripheral Type
15:8	CLASS	08h	Peripheral Class
7	REV	0Dh	Peripheral Revision. Identifies the revision level of the specific instance of the peripheral.

7.10.3.2 PLL3 PLL Control Register (PLLCTL)

The PLL control register (PLLCTL) is shown in Figure 7-36 and described in Table 7-47.

31–16
Reserved
R-00 0001h

15–8	7	6	5–4	3	2	1	0
Reserved	Rsvd	Rsvd	Reserved	PLLRST	Rsvd	PLL PWRDN	PLLEN
R-00 0001h	R/W-0	R-1	R/W-10	R/W-1	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 7-36. PLL Control Register (PLLCTL)

Table 7-47. PLL Control Register (PLLCTL) Field Descriptions[1]

Bit	Field	Value	Description
31:8	Reserved		Reserved. The reserved bit location is always read as 00 0001h. A value written to this field has no effect.
7	Reserved		Reserved. Writes to this register must keep this bit as 0.
6	Reserved		Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
5:4	Reserved		Reserved. Writes to this register must keep these bits as 10.
3	PLLRST		PLL reset bit
		0	PLL reset is released
		1	PLL reset is asserted
2	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	PLLPWRDN		PLL power-down mode select bit
		0	PLL is operational
		1	PLL is placed in power-down state; i.e., all analog circuitry in the PLL is turned-off
0	Reserved		Reserved. Writes to this register should set this bit as 1.

(1) The value of this register is changed by the ROM bootloader.

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7.10.4 PLL3 Controller Input and Output Clock Electrical Data/Timing

Table 7-48. Timing Requirements for CLKIN3 Devices

(see Figure 7-37)

NO.			500/625/700 PLL MODE x20		UNIT
			MIN	MAX	
1	$t_{c(CLKIN3)}$	Cycle time, CLKIN3	37.5	50	ns
2	$t_{w(CLKIN3H)}$	Pulse duration, CLKIN3 high	0.4 * $t_{c(CLKIN3)}$		ns
3	$t_{w(CLKIN3L)}$	Pulse duration, CLKIN3 low	0.4 * $t_{c(CLKIN3)}$		ns
4	$t_{t(CLKIN3)}$	Transition time, CLKIN3		1.2	ns
5	$t_{J(CLKIN3)}$	Period jitter (peak-to-peak), CLKIN3		100	ps

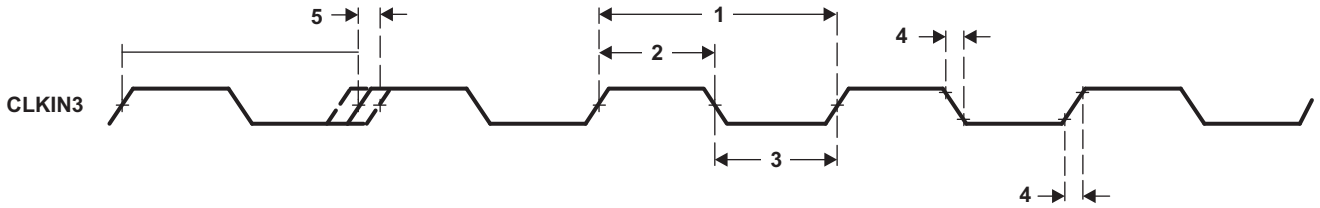

Figure 7-37. CLKIN3 Timing

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7.11 DDR2 Memory Controller

The 32-bit DDR2 Memory Controller bus of the C6472 is used to interface to JEDEC DDR2 SDRAM devices. The DDR2 bus is designed to sustain a throughput of up to 2.13 GBps at a 533-MHz data rate (267-MHz clock rate) as long as data requests are pending in the DDR2 Memory Controller. The DDR2 external bus only interfaces to DDR2 devices; it does not share the bus with any other types of peripherals.

7.11.1 DDR2 Memory Controller Device-Specific Information

The approach to specifying interface timing for the DDR2 memory bus is different than on other interfaces such as HPI and TSIP. For these other interfaces, the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models. For the C6472 DDR2 memory bus, the approach is to specify compatible DDR2 devices and provide the printed circuit board (PCB) solution and guidelines directly to the user. Texas Instruments (TI) has performed the simulation and system characterization to ensure all DDR2 interface timings in this solution are met. The complete DDR2 system solution is documented in the *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* application report (literature number SPRAAT7).

TI *only* supports designs that follow the board design guidelines outlined in the SPRAAT7 application report.

The DDR2 Memory Controller pins must be enabled by setting the DDREN configuration pin high during device reset. The DDREN pin must remain high at all times if the DDR2 Memory Controller is enabled. If DDREN is low, all data accessed destined for the DDR2 will be NULL terminated at the SCR. For more details, see Section 3.1, *Device Configuration at Device Reset*. The DDR2 Memory Controller on the TMS320C6472 device supports the following memory topologies:

- A 32-bit wide configuration interfacing to two 16-bit wide DDR2 SDRAM devices.
- A 16-bit wide configuration interfacing to a single 16-bit wide DDR2 SDRAM device.

7.11.2 DDR2 Memory Controller Peripheral Register Descriptions

Table 7-49. DDR2 Memory Controller Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
7800 0000	MIDR	DDR2 Memory Controller Module and Revision Register
7800 0004	DMCSTAT	DDR2 Memory Controller Status Register
7800 0008	SDCFG	DDR2 Memory Controller SDRAM Configuration Register
7800 000C	SDRFC	DDR2 Memory Controller SDRAM Refresh Control Register
7800 0010	SDTIM1	DDR2 Memory Controller SDRAM Timing 1 Register
7800 0014	SDTIM2	DDR2 Memory Controller SDRAM Timing 2 Register
7800 0018	-	Reserved
7800 0020	BPRIO	DDR2 Memory Controller Burst Priority Register
7800 0024 - 7800 00E0	-	Reserved
7800 00E4	DMCCTL	DDR2 Memory Controller Control Register
7800 00E8 - 7FFF FFC	-	Reserved

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7.11.3 DDR2 Memory Controller Electrical Data/Timing

The *TMS320C6472/TMS320TCI6486 DDR2 Implementation Guidelines* application report (literature number SPRAAT7) specifies a complete DDR2 interface solution for the C6472 device as well as a list of compatible DDR2 devices. TI has performed the simulation and system characterization to ensure all DDR2 interface timings in this solution are met; therefore, no electrical data/timing information is supplied here for this interface.

TI *only* supports designs that follow the board design guidelines outlined in the SPRAAT7 application report.

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7.12 I2C Peripheral

The inter-integrated circuit (I2C) module provides an interface between a C64x+ DSP and other devices compliant with Philips Semiconductors Inter-IC bus™ (I2C bus) specification version 2.1 and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I2C module.

7.12.1 I2C Device-Specific Information

The C6472 device includes an I2C peripheral module (I2C). NOTE: when using the I2C module, ensure there are external pullup resistors on the SDA and SCL pins.

The I2C modules on the C6472 device may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C port supports:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Glitch filter to suppress glitches 50 ns or shorter
- 7- and 10-Bit Device Addressing Modes
- Multi-Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

Figure 7-38 is a block diagram of the I2C module.

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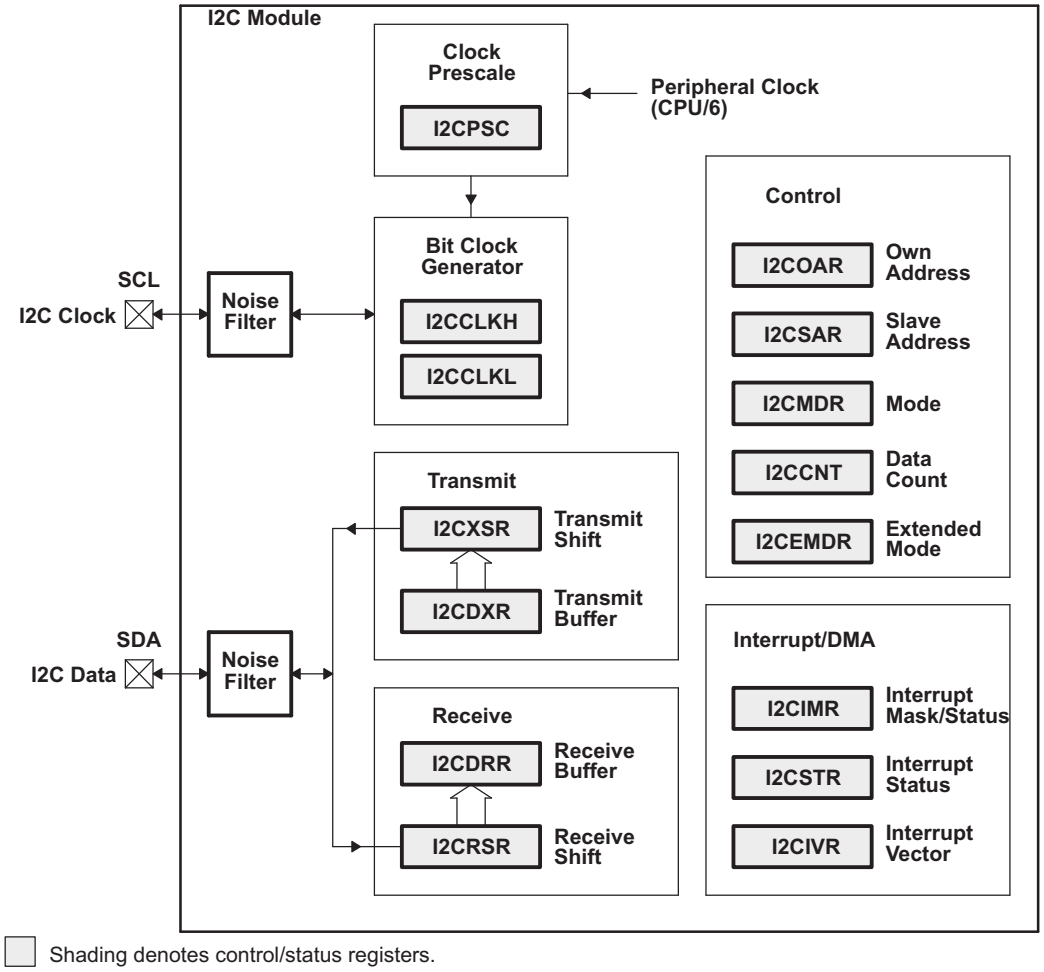

Figure 7-38. I2C Module Block Diagram

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7.12.2 I2C Peripheral Register Descriptions

Table 7-50. I2C Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B0 4000	ICOAR	I2C own address register
02B0 4004	ICIMR	I2C interrupt mask/status register
02B0 4008	ICSTR	I2C interrupt status register
02B0 400C	ICCLKL	I2C clock low-time divider register
02B0 4010	ICCLKH	I2C clock high-time divider register
02B0 4014	ICCNT	I2C data count register
02B0 4018	ICDRR	I2C data receive register
02B0 401C	ICSAR	I2C slave address register
02B0 4020	ICDXR	I2C data transmit register
02B0 4024	ICMDR	I2C mode register
02B0 4028	ICIVR	I2C interrupt vector register
02B0 402C	ICEMDR	I2C Extended mode register
02B0 4030	ICPSC	I2C prescaler register
02B0 4034 - 02B3 FFFC	-	Reserved

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7.12.3 I2C Electrical Data/Timing

Table 7-51. Timing Requirements for I2C Input(1)

(see Figure 7-39)

NO.			500/625/700				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SDLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SDA-SDLL)}$	Hold time, SDA valid after SCL low (For I2C bus™ devices)	0(3)		0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1C_b (5)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1C_b (5)	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1C_b (5)	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1C_b (5)	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b (5)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode I2C-bus™ device can be used in a Standard-mode I2C-bus™ system, but the requirement $t_{su(SDA-SCLH)}$ ≥250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

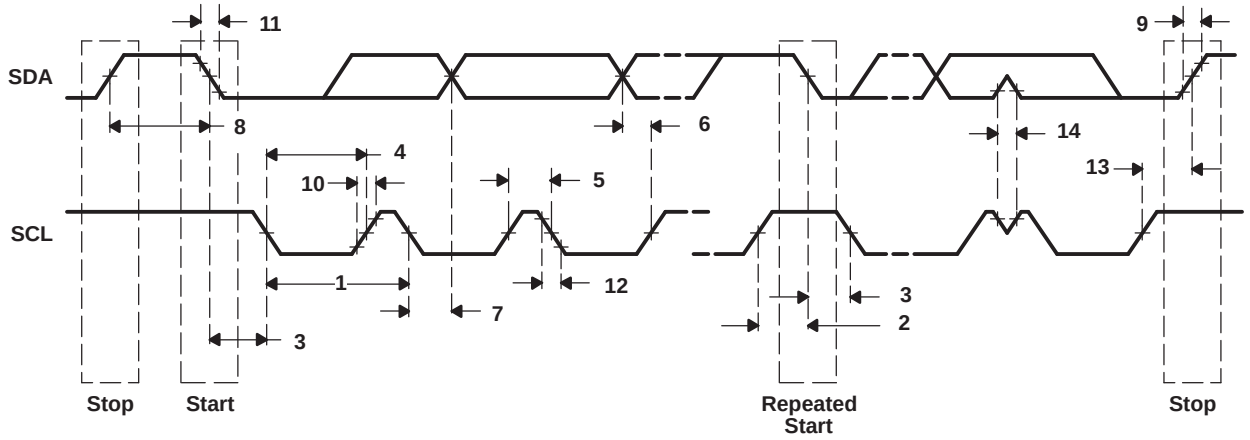

Figure 7-39. I2C Input Timing

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Table 7-52. Switching Characteristics Over Recommended Operating Conditions for I2C Output

(see Figure 7-40)

NO.	PARAMETER		500/625/700				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SDLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SDLL-SDAV)}$	Valid time, SDA valid after SCL low (For I2C bus™ devices)	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (1)	300	ns
25	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (1)	300	ns
26	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (1)	300	ns
27	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (1)	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_b (1)	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

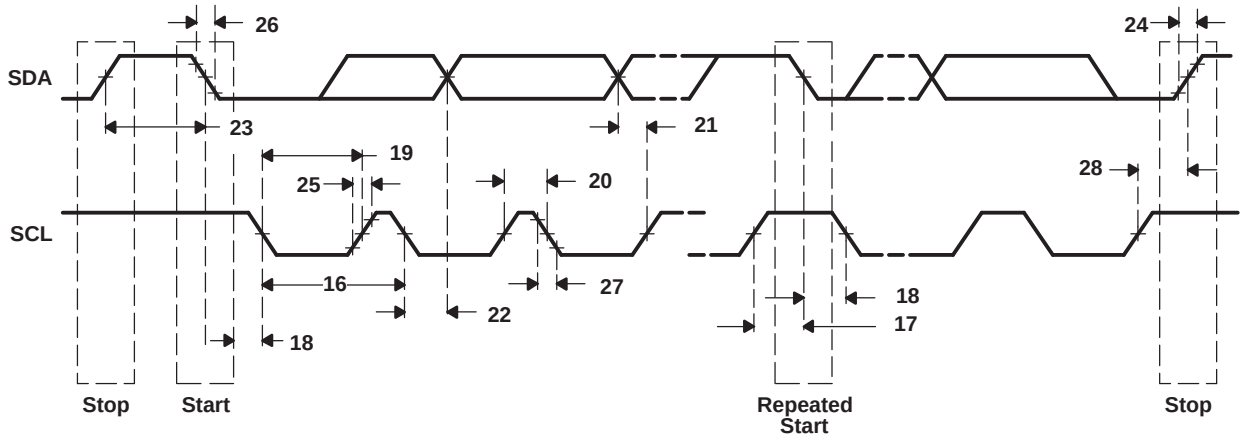

Figure 7-40. I2C Output Timing

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7.13 Host-Port Interface (HPI) Peripheral

7.13.1 HPI Device-Specific Information

The C6472 device includes a user-configurable 16-bit host-port interface (HPI16).

A host processor uses HPI to access internal registers and C6472 memory or external memory through the C6472 DDR2 EMIF. This accessibility may be useful for initializing the device in connection with the host boot mode and reading internal memory in connection with a software failure. Software handshaking, via the HRDY bit of the HPI control register (HPIC), is not supported on the C6472 device. For details about the HPI registers and their modes, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

7.13.2 HPI Peripheral Register Descriptions

Table 7-53 discusses access to the HPI registers from the C6472 C64x+ megamodules.

Table 7-53. HPI Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0288 0000	HPIPID	HPI Peripheral ID Register	
0288 0004	PWREMU_MGMT	HPI Power and Emulation Management Register	PWREMU_MGMT has both Host/CPU read/write access.
0288 0008 - 0288 002C	-	Reserved	
0288 0030	HPIC	HPI Control Register	The Host has read/write access to the HPIC register. The CPU has primarily read access to the HPIC register.(1)
0288 0034	HPID	Data register	The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers.
0288 0038	HPIAR/HPIAW(2)	HPI Address Registers	
0288 003C - 0289 FFFC	-	Reserved	

(1) The CPU can write 1 to the HINT bit to generate an interrupt to the host and it can write 1 to the DSPINT bit to clear/acknowledge an interrupt from the host.
(2) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the host. The CPU can access HPIAW and HPIAR independently. For details about the HPIA registers and their modes, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

7.13.3 Host Access to HPI

The host-port interface pins comprise a multiplexed access to the HPI module that contains the registers described in Table 7-53. This external interface can only directly access the HPIC, HPID, and the two HPIA registers. The select lines, HCNTL[1:0], are used to determine which of these registers is being accessed. The remaining control lines, HR/W and HHWIL, qualify the external accesses and the strobes, HCS, HDS1, and HDS2, latch data into the HPI registers. Optionally, HAS can be used to latch the select and control inputs.

Write and read accesses to these HPI registers initiate DMA-like transfers within the DSP. The HRDY (host ready) output from the HPI must be monitored to determine when a requested access is complete before initiating the next access. Since the HPI module operates on the CPU/6 clock, these access cycles are slow when PLL1 is in bypass mode; i.e., at the beginning of host boot mode. HPI accesses are used to configure PLL1 to shorten these cycles.

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7.13.4 HPI Electrical Data/Timing

Table 7-54. Timing Requirements for Host-Port Interface Cycles(1)(2)

(see Figure 7-41 through Figure 7-44)

NO.			500/625/700		UNIT
			MIN	MAX	
9	$t_{su(HASL-HSTBL)}$	Setup time, $\overline{HAS}$ low before $\overline{HSTROBE}$ low	5		ns
10	$t_{h(HSTBL-HASL)}$	Hold time, $\overline{HAS}$ low after $\overline{HSTROBE}$ low	2		ns
11	$t_{su(SELV-HASL)}$	Setup time, select signals(3) valid before $\overline{HAS}$ low	5		ns
12	$t_{h(HASL-SELV)}$	Hold time, select signals(3) valid after $\overline{HAS}$ low	5		ns
13	$t_{w(HSTBL)}$	Pulse duration, $\overline{HSTROBE}$ low	2M		ns
14	$t_{w(HSTBH)}$	Pulse duration, $\overline{HSTROBE}$ high between consecutive accesses	2M		ns
15	$t_{su(SELV-HSTBL)}$	Setup time, select signals(3) valid before $\overline{HSTROBE}$ low	5		ns
16	$t_{h(HSTBL-SELV)}$	Hold time, select signals(3) valid after $\overline{HSTROBE}$ low	5		ns
17	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{HSTROBE}$ high	6		ns
18	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{HSTROBE}$ high	0		ns
37	$t_{su(HCSL-HSTBL)}$	Setup time, $\overline{HCS}$ low before $\overline{HSTROBE}$ low	0		ns
38	$t_{h(HRDYL-HSTBL)}$	Hold time, $\overline{HSTROBE}$ low after $\overline{HRDY}$ low. $\overline{HSTROBE}$ should not be inactivated until $\overline{HRDY}$ is active (low); otherwise, HPI writes will not complete properly.	0		ns

(1) $\overline{HSTROBE}$ refers to the following logical operation on $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$: [NOT($\overline{HDS1}$ XOR $\overline{HDS2}$)] OR $\overline{HCS}$.
(2) M = HPI module clock period = 6 * CPU clock period or 12 ns at 500 MHz. (This duration will be much longer when PLL1 is in bypass mode.)
(3) Select signals (SELV) include: HCNTL[1:0] and HR/$\overline{W}$ and HHWIL.

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Table 7-55. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface Cycles(1)(2)(3)

(see Figure 7-41 through Figure 7-44)

NO.	PARAMETER			500/625/700		UNIT
				MIN	MAX	
1	$t_{d(HSTBL-HDV)}$	Delay time, $\overline{HSTROBE}$ low to DSP data valid	Case 1. HPIC or HPIA read	3	20	ns
			Case 2. HPID read with no auto-increment		17 * M + 20	
			Case 3. HPID read with auto-increment and read FIFO initially empty		16 * M + 20	
			Case 4. HPID read with auto-increment and data previously prefetched into the read FIFO	3	20	
2	$t_{dis(HSTBH-HDV)}$	Disable time, HD high-impedance from $\overline{HSTROBE}$ high		1	12	ns
3	$t_{en(HSTBL-HD)}$	Enable time, HD driven from $\overline{HSTROBE}$ low		2	20	ns
4	$t_{d(HSTBL-HRDYH)}$	Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ high			20	ns
5	$t_{d(HSTBH-HRDYH)}$	Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ high			20	ns
6	$t_{d(HSTBL-HRDYL)}$	Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ low	Case 1. HPID read with no auto-increment		18 * M + 20	ns
			Case 2. HPID read with auto-increment and read FIFO initially empty		17 * M + 20	
7	$t_{d(HDV-HRDYL)}$	Delay time, HD valid to $\overline{HRDY}$ low		0		ns
34	$t_{d(DSH-HRDYL)}$	Delay time, $\overline{HSTROBE}$ high to $\overline{HRDY}$ low	Case 1. HPIA write		5 * M + 20	ns
			Case 2. HPID write with no auto-increment		5 * M + 20	
35	$t_{d(HSTBL-HRDYL)}$	Delay time, $\overline{HSTROBE}$ low to $\overline{HRDY}$ low for HPIA write and FIFO not empty			40 * M + 20	ns
36	$t_{d(HASL-HRDYH)}$	Delay time, $\overline{HAS}$ low to $\overline{HRDY}$ high			20	ns

(1) M = HPI module clock period = 6 * CPU clock period or 12 ns at 500 MHz. (This duration will be much longer when PLL1 is in bypass mode.)
(2) $\overline{HSTROBE}$ refers to the following logical operation on $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$: [NOT($\overline{HDS1}$ XOR $\overline{HDS2}$)] OR $\overline{HCS}$.
(3) Maximum delays for 1 (cases 2 and 3), 6, 34, and 35 assume no conflict with SCR. The true maximum delay during application execution is dependent on internal congestion delays. $\overline{HRDY}$ must be used to guarantee valid cycle completion.

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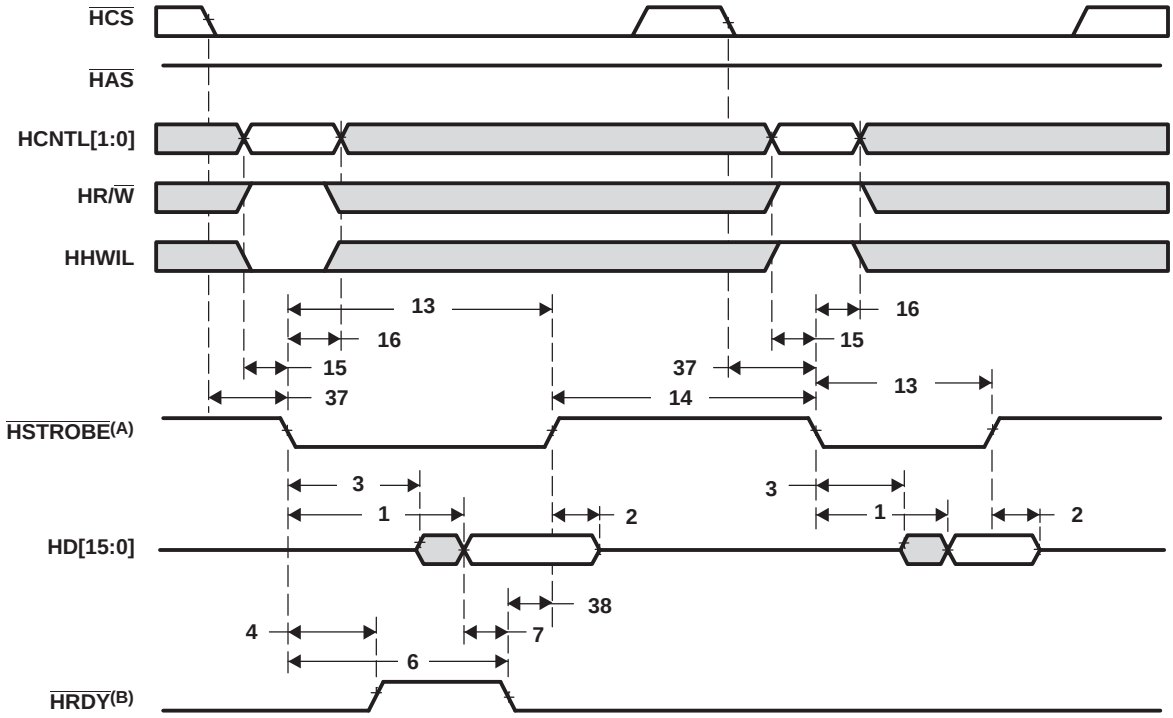

A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

Figure 7-41. HPI16 Read Timing (HAS Not Used, Tied High)

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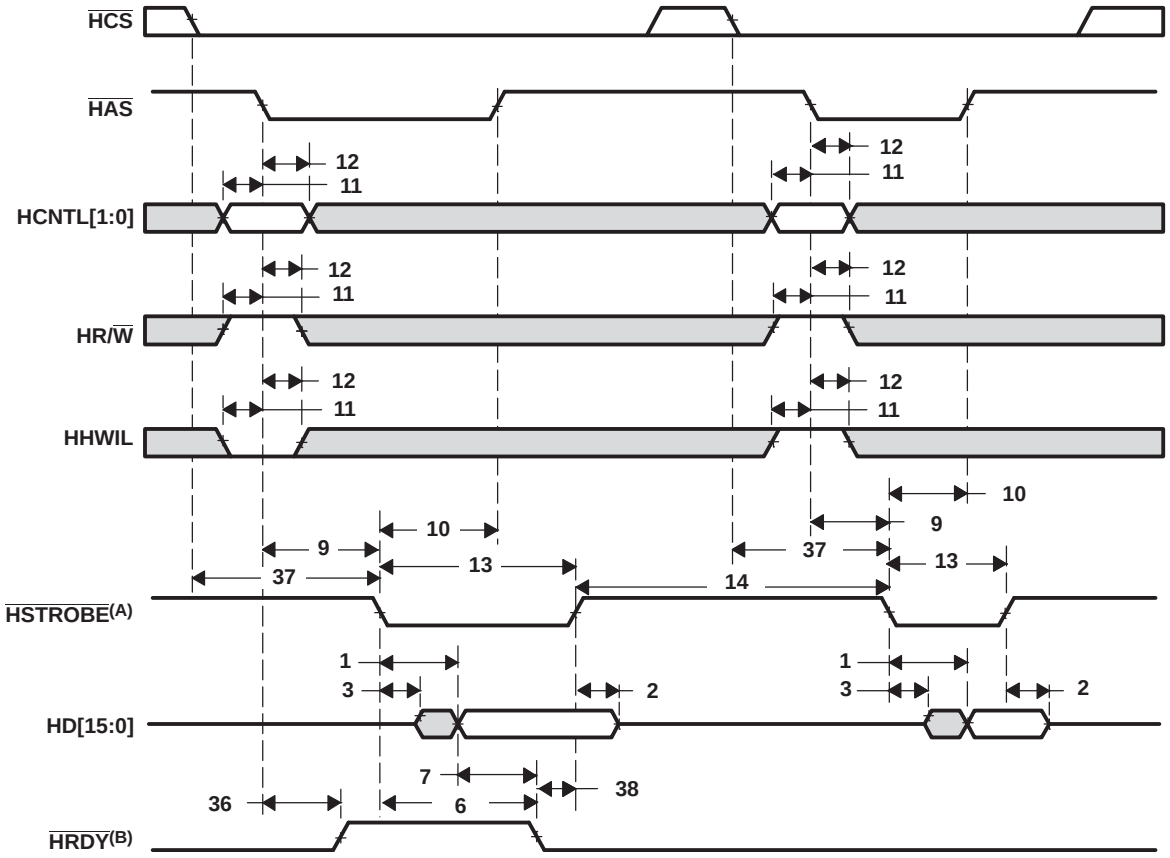

A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

Figure 7-42. HPI16 Read Timing (HAS Used)

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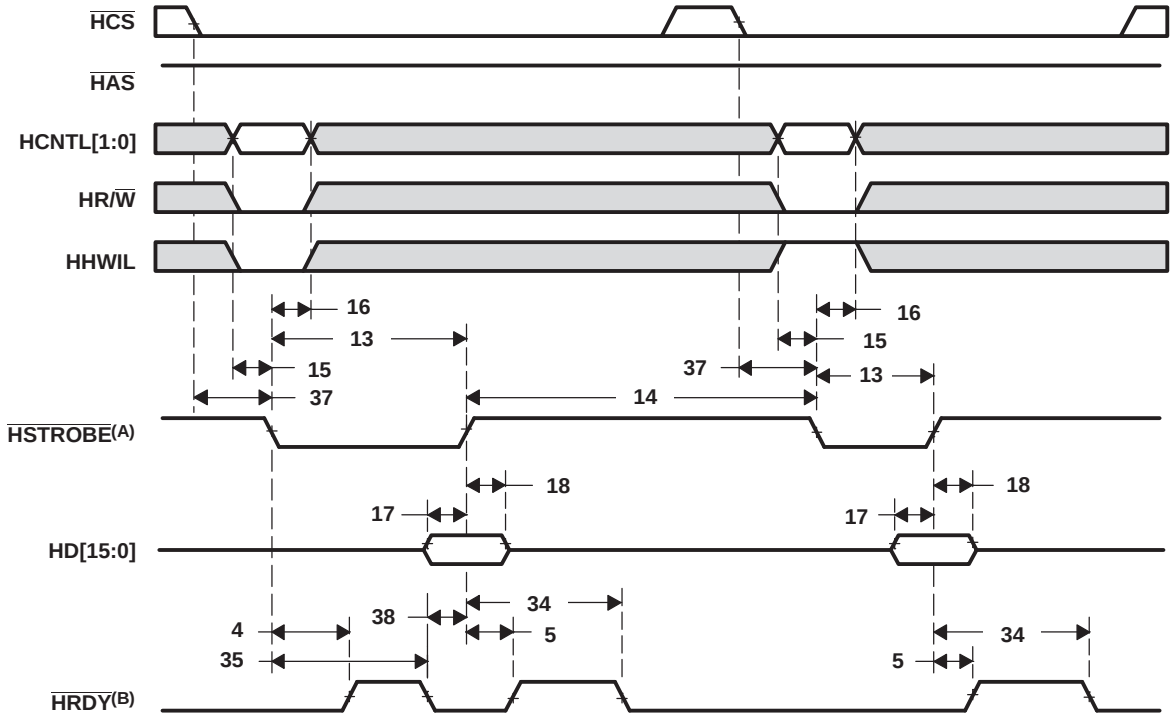

A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

Figure 7-43. HPI16 Write Timing (HAS Not Used, Tied High)

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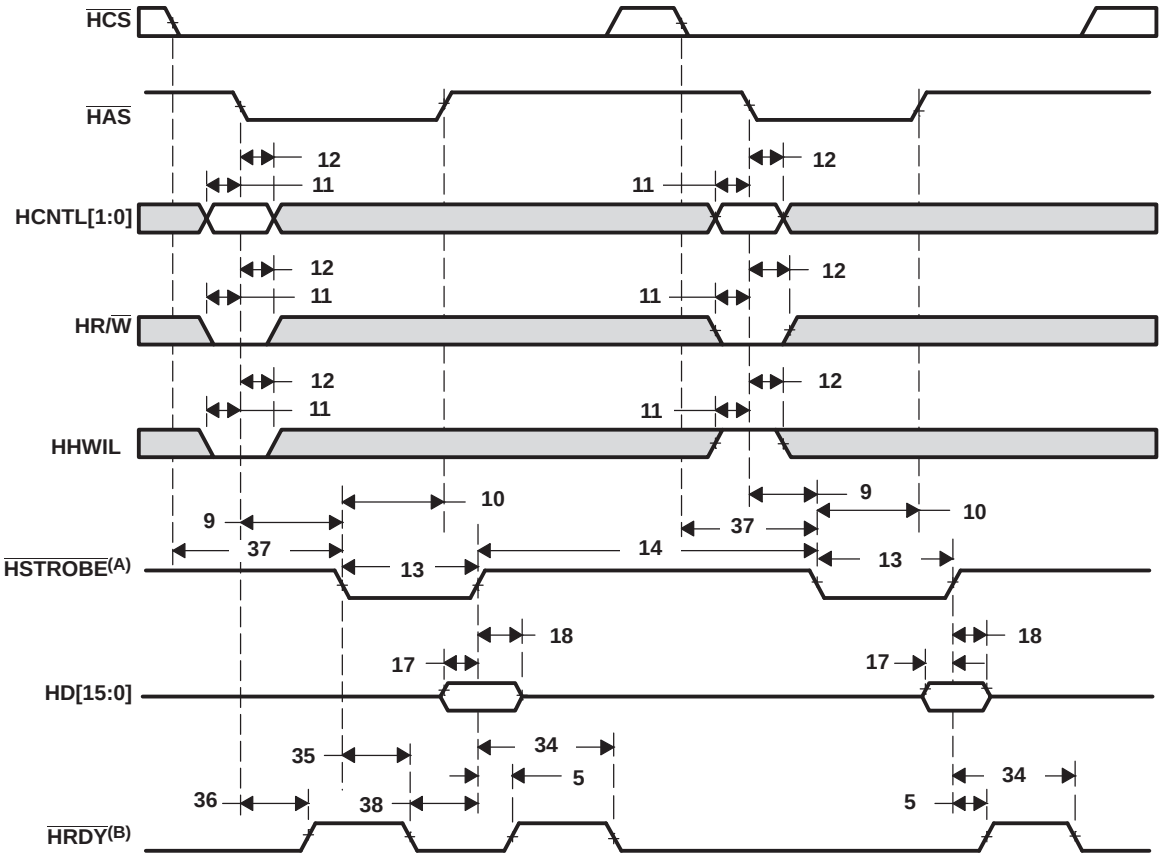

A. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed information on the HPI peripheral, see the *TMS320C6472/TMS320TCI6486 DSP Host Port Interface (HPI) User's Guide* (literature number SPRUEG1).

Figure 7-44. HPI16 Write Timing (HAS Used)

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7.14 TSIP

The TSIP is a multi-link serial interface consisting of a maximum of eight transmit data signals (or links), eight receive data signals (or links), two frame sync input signals, and two serial clock inputs. The TSIP module offers support for a maximum of 1024 timeslots for transmit and receive. Typically, 672 timeslots (DS3) for transmit and receive are utilized on these links. The TSIP module can be configured to use the frame sync signals and the serial clocks as redundant sources for all transmit and receive data signals or one frame sync and serial clock for transmit and the second frame sync and clock for receive. The standard serial data rate for each TSIP transmit and receive data signal is 8.192 Mbps. The standard frame sync is a one- (or more) bit wide pulse that occurs once every 125 µs or a minimum of one serial clock period every 1024 serial clocks. At the standard rate and default configuration there are 8 transmit and 8 receive links that are active. Each serial interface link supports up to 128 8-bit timeslots. This corresponds to an HMVIP or H.110 serial data rate interface. The serial interface clock frequency may be either 16.384 MHz (default) or 8.192 MHz. (The clock can be either 1x or 2x the data-bit rate.) Typical timeslot occupation is 96 timeslots (DS2) for each serial interface link. Seven transmit data links and seven receive data links are utilized to support the DS3 timeslot requirement. The eighth transmit and receive links are available to support common channel signaling (CCS). The data rate for the serial interface links can also be set to 16.384 Mbps or 32.768 Mbps. The maximum number of active serial links is reduced to four and two, respectively, in these configurations. The serial interface clock frequency may be either 32.768 MHz or 16.384 MHz for 16.384 Mbps serial links and either 65.536 MHz or 32.768 MHz for 32.768 Mbps serial links.

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7.14.1 TSIP0 Peripheral Register Descriptions

Table 7-56. TSIP Module Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0000	PID	PID Register
0250 0004	EMUTST	Emulation and Test Register
0250 0008	RST	Reset Register
0250 000C - 0250 007C	-	Reserved

Table 7-57. Serial Interface Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0080	SIUCTL	SIU Global Control Register
0250 0084 - 0250 009C	-	Reserved
0250 00A0	XCLK	Transmit Clock Source Register
0250 00A4	XCTL	Transmit Control Register
0250 00A8	XSIZE	Transmit Size Register
0250 00AC - 0250 00BC	-	Reserved
0250 00C0	RCLK	Receive Clock Source Register
0250 00C4	RCTL	Receive Control Register
0250 00C8	RSIZE	Receive Size Register
0250 00CC - 0250 00FC	-	Reserved

Table 7-58. TDMU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0100	TDMUCTL	TDMU Global Control Register
0250 0104	XFRFC	Transmit Free-Running Frame Counter
0250 0108	RFRFC	Receive Free-Running Frame Counter
0250 010C	TDMUCFG	TDMU Global Configuration Register
0250 0110	XBMST	Transmit Channel Bitmap Active Status Register

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Table 7-58. TDMU Global Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0114	RBMST	Receive Channel Active Status Register
0250 0118 - 0250 017C	-	Reserved

Table 7-59. DMATCU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0180	DMACTL	DMATCU Global Control Register
0250 0184	XDLY	Transmit Timeslot Delay Counter
0250 0188	RDLY	Receive Timeslot Delay Counter
0250 018C	-	Reserved
0250 0190	XCHST	Transmit Channel Configuration Active Status Register
0250 0194	RCHST	Receive Channel Active Status Register
0250 019C - 0250 01FC	-	Reserved

Table 7-60. TDMU Channel Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0200 - 0250 020C	-	TX/RX Channel 0 Error Log Registers
0250 0210 - 0250 021C	-	TX/RX Channel 1 Error Log Registers
0250 0220 - 0250 022C	-	TX/RX Channel 2 Error Log Registers
0250 0230 - 0250 023C	-	TX/RX Channel 3 Error Log Registers
0250 0240 - 0250 024C	-	TX/RX Channel 4 Error Log Registers
0250 0250 - 0250 025C	-	TX/RX Channel 5 Error Log Registers
0250 0260 - 0250 03FC	-	Reserved

Table 7-61. TX/RX Channels 0-5 Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0200	ERRCTL0	TX/RX Channel 0 Error control Register
0250 0204	ERRCNT0	TX/RX Channel 0 Error Count Register
0250 0208	ERRQ0	TX/RX Channel 0 Error Queue Register
0250 020C	-	Reserved
0250 0210	ERRCTL1	TX/RX Channel 1 Error control Register
0250 0214	ERRCNT1	TX/RX Channel 1 Error Count Register
0250 0218	ERRQ1	TX/RX Channel 1 Error Queue Register
0250 021C	-	Reserved
0250 0220	ERRCTL2	TX/RX Channel 2 Error control Register
0250 0224	ERRCNT2	TX/RX Channel 2 Error Count Register
0250 0228	ERRQ2	TX/RX Channel 2 Error Queue Register
0250 022C	-	Reserved
0250 0230	ERRCTL3	TX/RX Channel 3 Error control Register
0250 0234	ERRCNT3	TX/RX Channel 3 Error Count Register
0250 0238	ERRQ3	TX/RX Channel 3 Error Queue Register
0250 023C	-	Reserved
0250 0240	ERRCTL4	TX/RX Channel 4 Error control Register
0250 0244	ERRCNT4	TX/RX Channel 4 Error Count Register
0250 0248	ERRQ4	TX/RX Channel 4 Error Queue Register
0250 024C	-	Reserved
0250 0250	ERRCTL5	TX/RX Channel 5 Error control Register

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Table 7-61. TX/RX Channels 0-5 Error Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0254	ERRCNT5	TX/RX Channel 5 Error Count Register
0250 0258	ERRQ5	TX/RX Channel 5 Error Queue Register
0250 025C	-	Reserved

Table 7-62. TDMU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0800 - 0250 081C	-	Transmit Channel 0 Registers
0250 0820 - 0250 083C	-	Transmit Channel 1 Registers
0250 0840 - 0250 085C	-	Transmit Channel 2 Registers
0250 0860 - 0250 087C	-	Transmit Channel 3 Registers
0250 0880 - 0250 089C	-	Transmit Channel 4 Registers
0250 08A0 - 0250 08BC	-	Transmit Channel 5 Registers
0250 08C0 - 0250 0BFC	-	Reserved
0250 0C00 - 0250 0C1C	-	Receive Channel 0 Registers
0250 0C20 - 0250 0C3C	-	Receive Channel 1 Registers
0250 0C40 - 0250 0C5C	-	Receive Channel 2 Registers
0250 0C60 - 0250 0C7C	-	Receive Channel 3 Registers
0250 0C80 - 0250 0C9C	-	Receive Channel 4 Registers
0250 0CA0 - 0250 0CBC	-	Receive Channel 5 Registers
0250 0CC0 - 0250 0FFC	-	Reserved

Table 7-63. TDMU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0800	XCHEN0	Transmit Channel 0 Enable Register
0250 0804 - 0250 081C	-	Reserved
0250 0820	XCHEN1	Transmit Channel 1 Enable Register
0250 0824 - 0250 083C	-	Reserved
0250 0840	XCHEN2	Transmit Channel 2 Enable Register
0250 0844 - 0250 085C	-	Reserved
0250 0860	XCHEN3	Transmit Channel 3 Enable Register
0250 0864 - 0250 087C	-	Reserved
0250 0880	XCHEN4	Transmit Channel 4 Enable Register
0250 0884 - 0250 089C	-	Reserved
0250 08A0	XCHEN5	Transmit Channel 5 Enable Register
0250 08A4 - 0250 08BC	-	Reserved

Table 7-64. TDMU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0C00	RCHEN0	Receive Channel 0 Enable Register
0250 0C04 - 0250 0C1C	-	Reserved
0250 0C20	RCHEN1	Receive Channel 1 Enable Register
0250 0C24 - 0250 0C3C	-	Reserved
0250 0C40	RCHEN2	Receive Channel 2 Enable Register
0250 0C44 - 0250 0C5C	-	Reserved
0250 0C60	RCHEN3	Receive Channel 3 Enable Register
0250 0C64 - 0250 0C7C	-	Reserved

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Table 7-64. TDMU Receive Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 0C80	RCHEN4	Receive Channel 4 Enable Register
0250 0C84 - 0250 0C9C	-	Reserved
0250 0CA0	RCHEN5	Receive Channel 5 Enable Register
0250 0CA4 - 0250 0CBC	-	Reserved

Table 7-65. DMATCU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 1000 - 0250 101C	-	Transmit Channel 0 Config A Registers
0250 1020 - 0250 103C	-	Transmit Channel 0 Config B Registers
0250 1040 - 0250 105C	-	Transmit Channel 1 Config A Registers
0250 1060 - 0250 107C	-	Transmit Channel 1 Config B Registers
0250 1080 - 0250 109C	-	Transmit Channel 2 Config A Registers
0250 10A0 - 0250 10BC	-	Transmit Channel 2 Config B Registers
0250 10C0 - 0250 10DC	-	Transmit Channel 3 Config A Registers
0250 10E0 - 0250 10FC	-	Transmit Channel 3 Config B Registers
0250 1100 - 0250 111C	-	Transmit Channel 4 Config A Registers
0250 1120 - 0250 113C	-	Transmit Channel 4 Config B Registers
0250 1140 - 0250 115C	-	Transmit Channel 5 Config A Registers
0250 1160 - 0250 117C	-	Transmit Channel 5 Config B Registers
0250 1180 - 0250 17FC	-	Reserved
0250 1800 - 0250 181C	-	Receive Channel 0 Config A Registers
0250 1820 - 0250 183C	-	Receive Channel 0 Config B Registers
0250 1840 - 0250 185C	-	Receive Channel 1 Config A Registers
0250 1860 - 0250 187C	-	Receive Channel 1 Config B Registers
0250 1880 - 0250 189C	-	Receive Channel 2 Config A Registers
0250 18A0 - 0250 18BC	-	Receive Channel 2 Config B Registers
0250 18C0 - 0250 18DC	-	Receive Channel 3 Config A Registers
0250 18E0 - 0250 18FC	-	Receive Channel 3 Config B Registers
0250 1900 - 0250 191C	-	Receive Channel 4 Config A Registers
0250 1920 - 0250 193C	-	Receive Channel 4 Config B Registers
0250 1940 - 0250 195C	-	Receive Channel 5 Config A Registers
0250 1960 - 0250 197C	-	Receive Channel 5 Config B Registers
0250 1980 - 0250 19FC	-	Reserved

Table 7-66. DMATCU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 1000	DXCH_ABASE0	Transmit Channel 0 Memory Base Address Register A
0250 1004	DXCH_AFALLOC0	Transmit Channel 0 Frame Allocation Register A
0250 1008	DXCH_AFSIZE0	Transmit Channel 0 Frame Size Register A
0250 100C	DXCH_AFCNT0	Transmit Channel 0 Frame Count Register A
0250 1010 - 0250 101C	-	Reserved
0250 1020	DXCH_BBASE0	Transmit Channel 0 Memory Base Address Register B
0250 1024	DXCH_BFALLOC0	Transmit Channel 0 Frame Allocation Register B
0250 1028	DXCH_BFSIZE0	Transmit Channel 0 Frame Size Register B
0250 102C	DXCH_BFCNT0	Transmit Channel 0 Frame Count Register B
0250 1030 - 0250 103C	-	Reserved
0250 1040	DXCH_ABASE1	Transmit Channel 1 Memory Base Address Register A

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Table 7-66. DMATCU Transmit Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 1044	DXCH_AFALLOC1	Transmit Channel 1 Frame Allocation Register A
0250 1048	DXCH_AFSIZE1	Transmit Channel 1 Frame Size Register A
0250 104C	DXCH_AFCNT1	Transmit Channel 1 Frame Count Register A
0250 1050 - 0250 105C	-	Reserved
0250 1060	DXCH_BBASE1	Transmit Channel 1 Memory Base Address Register B
0250 1064	DXCH_BFALLOC1	Transmit Channel 1 Frame Allocation Register B
0250 1068	DXCH_BFSIZE1	Transmit Channel 1 Frame Size Register B
0250 106C	DXCH_BFCNT1	Transmit Channel 1 Frame Count Register B
0250 1070 - 0250 107C	-	Reserved
0250 1080	DXCH_ABASE2	Transmit Channel 2 Memory Base Address Register A
0250 1084	DXCH_AFALLOC2	Transmit Channel 2 Frame Allocation Register A
0250 1088	DXCH_AFSIZE2	Transmit Channel 2 Frame Size Register A
0250 108C	DXCH_AFCNT2	Transmit Channel 2 Frame Count Register A
0250 1090 - 0250 109C	-	Reserved
0250 10A0	DXCH_BBASE2	Transmit Channel 2 Memory Base Address Register B
0250 10A4	DXCH_BFALLOC2	Transmit Channel 2 Frame Allocation Register B
0250 10A8	DXCH_BFSIZE2	Transmit Channel 2 Frame Size Register B
0250 10AC	DXCH_BFCNT2	Transmit Channel 2 Frame Count Register B
0250 10B0 - 0250 10BC	-	Reserved
0250 10C0	DXCH_ABASE3	Transmit Channel 3 Memory Base Address Register A
0250 10C4	DXCH_AFALLOC3	Transmit Channel 3 Frame Allocation Register A
0250 10C8	DXCH_AFSIZE3	Transmit Channel 3 Frame Size Register A
0250 10CC	DXCH_AFCNT3	Transmit Channel 3 Frame Count Register A
0250 10D0 - 0250 10DC	-	Reserved
0250 10E0	DXCH_BBASE3	Transmit Channel 3 Memory Base Address Register B
0250 10E4	DXCH_BFALLOC3	Transmit Channel 3 Frame Allocation Register B
0250 10E8	DXCH_BFSIZE3	Transmit Channel 3 Frame Size Register B
0250 10EC	DXCH_BFCNT3	Transmit Channel 3 Frame Count Register B
0250 10F0 - 0250 10FC	-	Reserved
0250 1100	DXCH_ABASE4	Transmit Channel 4 Memory Base Address Register A
0250 1104	DXCH_AFALLOC4	Transmit Channel 4 Frame Allocation Register A
0250 1108	DXCH_AFSIZE4	Transmit Channel 4 Frame Size Register A
0250 110C	DXCH_AFCNT4	Transmit Channel 4 Frame Count Register A
0250 1110 - 0250 111C	-	Reserved
0250 1120	DXCH_BBASE4	Transmit Channel 4 Memory Base Address Register B
0250 1124	DXCH_BFALLOC4	Transmit Channel 4 Frame Allocation Register B
0250 1128	DXCH_BFSIZE4	Transmit Channel 4 Frame Size Register B
0250 112C	DXCH_BFCNT4	Transmit Channel 4 Frame Count Register B
0250 1130 - 0250 113C	-	Reserved
0250 1140	DXCH_ABASE5	Transmit Channel 5 Memory Base Address Register A
0250 1144	DXCH_AFALLOC5	Transmit Channel 5 Frame Allocation Register A
0250 1148	DXCH_AFSIZE5	Transmit Channel 5 Frame Size Register A
0250 114C	DXCH_AFCNT5	Transmit Channel 5 Frame Count Register A
0250 1150 - 0250 115C	-	Reserved
0250 1160	DXCH_BBASE5	Transmit Channel 5 Memory Base Address Register B
0250 1164	DXCH_BFALLOC5	Transmit Channel 5 Frame Allocation Register B
0250 1168	DXCH_BFSIZE5	Transmit Channel 5 Frame Size Register B

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Table 7-66. DMATCU Transmit Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 116C	DXCH_BFCNT5	Transmit Channel 5 Frame Count Register B
0250 1170 - 0250 117C	-	Reserved

Table 7-67. DMATCU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 1800	DRCH_ABASE0	Receive Channel 0 Memory Base Address Register A
0250 1804	DRCH_AFALLOC0	Receive Channel 0 Frame Allocation Register A
0250 1808	DRCH_AFSIZE0	Receive Channel 0 Frame Size Register A
0250 180C	DRCH_AFCNT0	Receive Channel 0 Frame Count Register A
0250 1810 - 0250 181C	-	Reserved
0250 1820	DRCH_BBASE0	Receive Channel 0 Memory Base Address Register B
0250 1824	DRCH_BFALLOC0	Receive Channel 0 Frame Allocation Register B
0250 1828	DRCH _BFSIZE0	Receive Channel 0 Frame Size Register B
0250 182C	DRCH _BFCNT0	Receive Channel 0 Frame Count Register B
0250 1830 - 0250 183C	-	Reserved
0250 1840	DRCH_ABASE1	Receive Channel 1 Memory Base Address Register A
0250 1844	DRCH_AFALLOC1	Receive Channel 1 Frame Allocation Register A
0250 1848	DRCH_AFSIZE1	Receive Channel 1 Frame Size Register A
0250 184C	DRCH_AFCNT1	Receive Channel 1 Frame Count Register A
0250 1850 - 0250 185C	-	Reserved
0250 1860	DRCH_BBASE1	Receive Channel 1 Memory Base Address Register B
0250 1864	DRCH_BFALLOC1	Receive Channel 1 Frame Allocation Register B
0250 1868	DRCH _BFSIZE1	Receive Channel 1 Frame Size Register B
0250 186C	DRCH _BFCNT1	Receive Channel 1 Frame Count Register B
0250 1870 - 0250 187C	-	Reserved
0250 1880	DRCH_ABASE2	Receive Channel 2 Memory Base Address Register A
0250 1884	DRCH_AFALLOC2	Receive Channel 2 Frame Allocation Register A
0250 1888	DRCH_AFSIZE2	Receive Channel 2 Frame Size Register A
0250 188C	DRCH_AFCNT2	Receive Channel 2 Frame Count Register A
0250 1890 - 0250 189C	-	Reserved
0250 18A0	DRCH_BBASE2	Receive Channel 2 Memory Base Address Register B
0250 18A4	DRCH_BFALLOC2	Receive Channel 2 Frame Allocation Register B
0250 18A8	DRCH _BFSIZE2	Receive Channel 2 Frame Size Register B
0250 18AC	DRCH _BFCNT2	Receive Channel 2 Frame Count Register B
0250 18B0 - 0250 18BC	-	Reserved
0250 18C0	DRCH_ABASE3	Receive Channel 3 Memory Base Address Register A
0250 18C4	DRCH_AFALLOC3	Receive Channel 3 Frame Allocation Register A
0250 18C8	DRCH_AFSIZE3	Receive Channel 3 Frame Size Register A
0250 18CC	DRCH_AFCNT3	Receive Channel 3 Frame Count Register A
0250 18D0 - 0250 18DC	-	Reserved
0250 18E0	DRCH_BBASE3	Receive Channel 3 Memory Base Address Register B
0250 18E4	DRCH_BFALLOC3	Receive Channel 3 Frame Allocation Register B
0250 18E8	DRCH _BFSIZE3	Receive Channel 3 Frame Size Register B
0250 18EC	DRCH _BFCNT3	Receive Channel 3 Frame Count Register B
0250 18F0 - 0250 18FC	-	Reserved
0250 1900	DRCH_ABASE4	Receive Channel 4 Memory Base Address Register A
0250 1904	DRCH_AFALLOC4	Receive Channel 4 Frame Allocation Register A

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Table 7-67. DMATCU Receive Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 1908	DRCH_AFSIZE4	Receive Channel 4 Frame Size Register A
0250 190C	DRCH_AFCNT4	Receive Channel 4 Frame Count Register A
0250 1910 - 0250 191C	-	Reserved
0250 1920	DRCH_BBASE4	Receive Channel 4 Memory Base Address Register B
0250 1924	DRCH_BFALLOC4	Receive Channel 4 Frame Allocation Register B
0250 1928	DRCH _BFSIZE4	Receive Channel 4 Frame Size Register B
0250 192C	DRCH _BFCNT4	Receive Channel 4 Frame Count Register B
0250 1930 - 0250 193C	-	Reserved
0250 1940	DRCH_ABASE5	Receive Channel 5 Memory Base Address Register A
0250 1944	DRCH_AFALLOC5	Receive Channel 5 Frame Allocation Register A
0250 1948	DRCH_AFSIZE5	Receive Channel 5 Frame Size Register A
0250 194C	DRCH_AFCNT5	Receive Channel 5 Frame Count Register A
0250 1950 - 0250 195C	-	Reserved
0250 1960	DRCH_BBASE5	Receive Channel 5 Memory Base Address Register B
0250 1964	DRCH_BFALLOC5	Receive Channel 5 Frame Allocation Register B
0250 1968	DRCH _BFSIZE5	Receive Channel 5 Frame Size Register B
0250 196C	DRCH _BFCNT5	Receive Channel 5 Frame Count Register B
0250 1970 - 0250 197C	-	Reserved

Table 7-68. TDMU Channel Bitmaps

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0250 8000 - 0250 80FC	XBM_XBMA0	Transmit Channel 0 Bitmap A
0250 8100 - 0250 81FC	XBM_XBMB0	Transmit Channel 0 Bitmap B
0250 8200 - 0250 82FC	XBM_XBMA1	Transmit Channel 1 Bitmap A
0250 8300 - 0250 83FC	XBM_XBMB1	Transmit Channel 1 Bitmap B
0250 8400 - 0250 84FC	XBM_XBMA2	Transmit Channel 2 Bitmap A
0250 8500 - 0250 85FC	XBM_XBMB2	Transmit Channel 2 Bitmap B
0250 8600 - 0250 86FC	XBM_XBMA3	Transmit Channel 3 Bitmap A
0250 8700 - 0250 87FC	XBM_XBMB3	Transmit Channel 3 Bitmap B
0250 8800 - 0250 88FC	XBM_XBMA4	Transmit Channel 4 Bitmap A
0250 8900 - 0250 89FC	XBM_XBMB4	Transmit Channel 4 Bitmap B
0250 8A00 - 0250 8AFC	XBM_XBMA5	Transmit Channel 5 Bitmap A
0250 8B00 - 0250 8BFC	XBM_XBMB5	Transmit Channel 5 Bitmap B
0250 8C00 - 0250 BFFC	-	Reserved
0250 C000 - 0250 C0FC	RBM_RBMA0	Receive Channel 0 Bitmap A
0250 C100 - 0250 C1FC	RBM_RBMB0	Receive Channel 0 Bitmap B
0250 C200 - 0250 C2FC	RBM_RBMA1	Receive Channel 1 Bitmap A
0250 C300 - 0250 C3FC	RBM_RBMB1	Receive Channel 1 Bitmap B
0250 C400 - 0250 C4FC	RBM_RBMA2	Receive Channel 2 Bitmap A
0250 C500 - 0250 C5FC	RBM_RBMB2	Receive Channel 2 Bitmap B
0250 C600 - 0250 C6FC	RBM_RBMA3	Receive Channel 3 Bitmap A
0250 C700 - 0250 C7FC	RBM_RBMB3	Receive Channel 3 Bitmap B
0250 C800 - 0250 C8FC	RBM_RBMA4	Receive Channel 4 Bitmap A
0250 C900 - 0250 C9FC	RBM_RBMB4	Receive Channel 4 Bitmap B
0250 CA00 - 0250 CAFC	RBM_RBMA5	Receive Channel 5 Bitmap A
0250 CB00 - 0250 CBFC	RBM_RBMB5	Receive Channel 5 Bitmap B
0250 CC00 - 0250 FFFC	-	Reserved

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Table 7-69. TDMU Channel Buffers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0251 0000 - 0251 0DFC	XPING0	Transmit Channel 0 PING Buffer
0251 0100 - 0251 03FC	-	Reserved
0251 0400 - 0251 04FC	XPONG0	Transmit Channel 0 PONG Buffer
0251 0500 - 0251 07FC	-	Reserved
0251 0800 - 0251 08FC	XPING1	Transmit Channel 1 PING Buffer
0251 0900 - 0251 0BFC	-	Reserved
0251 0C00 - 0251 0CFC	XPONG1	Transmit Channel 1 PONG Buffer
0251 0D00 - 0251 0FFC	-	Reserved
0251 1000 - 0251 1DFC	XPING2	Transmit Channel 2 PING Buffer
0251 1100 - 0251 13FC	-	Reserved
0251 1400 - 0251 14FC	XPONG2	Transmit Channel 2 PONG Buffer
0251 1500 - 0251 17FC	-	Reserved
0251 1800 - 0251 18FC	XPING3	Transmit Channel 3 PING Buffer
0251 1900 - 0251 1BFC	-	Reserved
0251 1C00 - 0251 1CFC	XPONG3	Transmit Channel 3 PONG Buffer
0251 1D00 - 0251 1FFC	-	Reserved
0251 2000 - 0251 2DFC	XPING4	Transmit Channel 4 PING Buffer
0251 2100 - 0251 23FC	-	Reserved
0251 2400 - 0251 24FC	XPONG4	Transmit Channel 4 PONG Buffer
0251 2500 - 0251 27FC	-	Reserved
0251 2800 - 0251 28FC	XPING5	Transmit Channel 5 PING Buffer
0251 2900 - 0251 2BFC	-	Reserved
0251 2C00 - 0251 2CFC	XPONG5	Transmit Channel 5 PONG Buffer
0251 2D00 - 0251 7FFC	-	Reserved
0251 8000 - 0251 8DFC	RPING0	Receive Channel 0 PING Buffer
0251 8100 - 0251 83FC	-	Reserved
0251 8400 - 0251 84FC	RPONG0	Receive Channel 0 PONG Buffer
0251 8500 - 0251 87FC	-	Reserved
0251 8800 - 0251 88FC	RPING1	Receive Channel 1 PING Buffer
0251 8900 - 0251 8BFC	-	Reserved
0251 8C00 - 0251 8CFC	RPONG1	Receive Channel 1 PONG Buffer
0251 8D00 - 0251 8FFC	-	Reserved
0251 9000 - 0251 9DFC	RPING2	Receive Channel 2 PING Buffer
0251 9100 - 0251 93FC	-	Reserved
0251 9400 - 0251 94FC	RPONG2	Receive Channel 2 PONG Buffer
0251 9500 - 0251 97FC	-	Reserved
0251 9800 - 0251 98FC	RPING3	Receive Channel 3 PING Buffer
0251 9900 - 0251 9BFC	-	Reserved
0251 9C00 - 0251 9CFC	RPONG3	Receive Channel 3 PONG Buffer
0251 9D00 - 0251 9FFC	-	Reserved
0251 A000 - 0251 ADFC	RPING4	Receive Channel 4 PING Buffer
0251 A100 - 0251 A3FC	-	Reserved
0251 A400 - 0251 A4FC	RPONG4	Receive Channel 4 PONG Buffer
0251 A500 - 0251 A7FC	-	Reserved
0251 A800 - 0251 A8FC	RPING5	Receive Channel 5 PING Buffer
0251 A900 - 0251 ABFC	-	Reserved
0251 AC00 - 0251 ACFC	RPONG5	Receive Channel 5 PONG Buffer

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Table 7-69. TDMU Channel Buffers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0251 AD00 - 0253 FFFC	-	Reserved

7.14.2 TSIP1 Peripheral Register Descriptions

Table 7-70. TSIP Module Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0000	PID	PID Register
0254 0004	EMUTST	Emulation and Test Register
0254 0008	RST	Reset Register
0254 000C - 0254 007C	-	Reserved

Table 7-71. Serial Interface Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0080	SIUCTL	SIU Global Control Register
0254 0084 - 0254 009C	-	Reserved
0254 00A0	XCLK	Transmit Clock Source Register
0254 00A4	XCTL	Transmit Control Register
0254 00A8	XSIZE	Transmit Size Register
0254 00AC - 0254 00BC	-	Reserved
0254 00C0	RCLK	Receive Clock Source Register
0254 00C4	RCTL	Receive Control Register
0254 00C8	RSIZE	Receive Size Register
0254 00CC - 0254 00FC	-	Reserved

Table 7-72. TDMU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0100	TDMUCTL	TDMU Global Control Register
0254 0104	XFRFC	Transmit Free-Running Frame Counter
0254 0108	RFRFC	Receive Free-Running Frame Counter
0254 010C	TDMUCFG	TDMU Global Configuration Register
0254 0110	XBMST	Transmit Channel Active Status Register
0254 0114	RBMST	Receive Channel Active Status Register
0254 0118 - 0254 017C	-	Reserved

Table 7-73. DMATCU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0180	DMACTL	DMATCU Global Control Register
0254 0184	XDLY	Transmit Timeslot Delay Counter
0254 0188	RDLY	Receive Timeslot Delay Counter
0254 018C	-	Reserved
0254 0190	XCHST	Transmit Channel Active Status Register
0254 0194	RCHST	Receive Channel Active Status Register
0254 019C - 0254 01FC	-	Reserved

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Table 7-74. TDMU Channel Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0200 - 0254 020C	-	TX/RX Channel 0 Error Log Registers
0254 0210 - 0254 021C	-	TX/RX Channel 1 Error Log Registers
0254 0220 - 0254 022C	-	TX/RX Channel 2 Error Log Registers
0254 0230 - 0254 023C	-	TX/RX Channel 3 Error Log Registers
0254 0240 - 0254 024C	-	TX/RX Channel 4 Error Log Registers
0254 0250 - 0254 025C	-	TX/RX Channel 5 Error Log Registers
0254 0260 - 0254 03FC	-	Reserved

Table 7-75. TX/RX Channels 0-5 Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0200	ERRCTL0	TX/RX Channel 0 Error control Register
0254 0204	ERRCNT0	TX/RX Channel 0 Error Count Register
0254 0208	ERRQ0	TX/RX Channel 0 Error Queue Register
0254 020C	-	Reserved
0254 0210	ERRCTL1	TX/RX Channel 1 Error control Register
0254 0214	ERRCNT1	TX/RX Channel 1 Error Count Register
0254 0218	ERRQ1	TX/RX Channel 1 Error Queue Register
0254 021C	-	Reserved
0254 0220	ERRCTL2	TX/RX Channel 2 Error control Register
0254 0224	ERRCNT2	TX/RX Channel 2 Error Count Register
0254 0228	ERRQ2	TX/RX Channel 2 Error Queue Register
0254 022C	-	Reserved
0254 0230	ERRCTL3	TX/RX Channel 3 Error control Register
0254 0234	ERRCNT3	TX/RX Channel 3 Error Count Register
0254 0238	ERRQ3	TX/RX Channel 3 Error Queue Register
0254 023C	-	Reserved
0254 0240	ERRCTL4	TX/RX Channel 4 Error control Register
0254 0244	ERRCNT4	TX/RX Channel 4 Error Count Register
0254 0248	ERRQ4	TX/RX Channel 4 Error Queue Register
0254 024C	-	Reserved
0254 0250	ERRCTL5	TX/RX Channel 5 Error control Register
0254 0254	ERRCNT5	TX/RX Channel 5 Error Count Register
0254 0258	ERRQ5	TX/RX Channel 5 Error Queue Register
0254 025C	-	Reserved

Table 7-76. TDMU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0800 - 0254 081C	-	Transmit Channel 0 Registers
0254 0820 - 0254 083C	-	Transmit Channel 1 Registers
0254 0840 - 0254 085C	-	Transmit Channel 2 Registers
0254 0860 - 0254 087C	-	Transmit Channel 3 Registers
0254 0880 - 0254 089C	-	Transmit Channel 4 Registers
0254 08A0 - 0254 08BC	-	Transmit Channel 5 Registers
0254 08C0 - 0254 0BFC	-	Reserved
0254 0C00 - 0254 0C1C	-	Receive Channel 0 Registers
0254 0C20 - 0254 0C3C	-	Receive Channel 1 Registers
0254 0C40 - 0254 0C5C	-	Receive Channel 2 Registers

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Table 7-76. TDMU Channel Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0C60 - 0254 0C7C	-	Receive Channel 3 Registers
0254 0C80 - 0254 0C9C	-	Receive Channel 4 Registers
0254 0CA0 - 0254 0CBC	-	Receive Channel 5 Registers
0254 0CC0 - 0254 0FFC	-	Reserved

Table 7-77. TDMU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0800	XCHEN0	Transmit Channel 0 Enable Register
0254 0804 - 0254 081C	-	Reserved
0254 0820	XCHEN1	Transmit Channel 1 Enable Register
0254 0824 - 0254 083C	-	Reserved
0254 0840	XCHEN2	Transmit Channel 2 Enable Register
0254 0844 - 0254 085C	-	Reserved
0254 0860	XCHEN3	Transmit Channel 3 Enable Register
0254 0864 - 0254 087C	-	Reserved
0254 0880	XCHEN4	Transmit Channel 4 Enable Register
0254 0884 - 0254 089C	-	Reserved
0254 08A0	XCHEN5	Transmit Channel 5 Enable Register
0254 08A4 - 0254 08BC	-	Reserved

Table 7-78. TDMU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 0C00	RCHEN0	Receive Channel 0 Enable Register
0254 0C04 - 0254 0C1C	-	Reserved
0254 0C20	RCHEN1	Receive Channel 1 Enable Register
0254 0C24 - 0254 0C3C	-	Reserved
0254 0C40	RCHEN2	Receive Channel 2 Enable Register
0254 0C44 - 0254 0C5C	-	Reserved
0254 0C60	RCHEN3	Receive Channel 3 Enable Register
0254 0C64 - 0254 0C7C	-	Reserved
0254 0C80	RCHEN4	Receive Channel 4 Enable Register
0254 0C84 - 0254 0C9C	-	Reserved
0254 0CA0	RCHEN5	Receive Channel 5 Enable Register
0254 0CA4 - 0254 0CBC	-	Reserved

Table 7-79. DMATCU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 1000 - 0254 101C	-	Transmit Channel 0 Config A Registers
0254 1020 - 0254 103C	-	Transmit Channel 0 Config B Registers
0254 1040 - 0254 105C	-	Transmit Channel 1 Config A Registers
0254 1060 - 0254 107C	-	Transmit Channel 1 Config B Registers
0254 1080 - 0254 109C	-	Transmit Channel 2 Config A Registers
0254 10A0 - 0254 10BC	-	Transmit Channel 2 Config B Registers
0254 10C0 - 0254 10DC	-	Transmit Channel 3 Config A Registers
0254 10E0 - 0254 10FC	-	Transmit Channel 3 Config B Registers
0254 1100 - 0254 111C	-	Transmit Channel 4 Config A Registers

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Table 7-79. DMATCU Channel Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 1120 - 0254 113C	-	Transmit Channel 4 Config B Registers
0254 1140 - 0254 115C	-	Transmit Channel 5 Config A Registers
0254 1160 - 0254 117C	-	Transmit Channel 5 Config B Registers
0254 1180 - 0254 17FC	-	Reserved
0254 1800 - 0254 181C	-	Receive Channel 0 Config A Registers
0254 1820 - 0254 183C	-	Receive Channel 0 Config B Registers
0254 1840 - 0254 185C	-	Receive Channel 1 Config A Registers
0254 1860 - 0254 187C	-	Receive Channel 1 Config B Registers
0254 1880 - 0254 189C	-	Receive Channel 2 Config A Registers
0254 18A0 - 0254 18BC	-	Receive Channel 2 Config B Registers
0254 18C0 - 0254 18DC	-	Receive Channel 3 Config A Registers
0254 18E0 - 0254 18FC	-	Receive Channel 3 Config B Registers
0254 1900 - 0254 191C	-	Receive Channel 4 Config A Registers
0254 1920 - 0254 193C	-	Receive Channel 4 Config B Registers
0254 1940 - 0254 195C	-	Receive Channel 5 Config A Registers
0254 1960 - 0254 197C	-	Receive Channel 5 Config B Registers
0254 1980 - 0254 19FC	-	Reserved

Table 7-80. DMATCU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 1000	DXCH_ABASE0	Transmit Channel 0 Memory Base Address Register A
0254 1004	DXCH_AFALLOC0	Transmit Channel 0 Frame Allocation Register A
0254 1008	DXCH_AFSIZE0	Transmit Channel 0 Frame Size Register A
0254 100C	DXCH_AFCNT0	Transmit Channel 0 Frame Count Register A
0254 1010 - 0254 101C	-	Reserved
0254 1020	DXCH_BBASE0	Transmit Channel 0 Memory Base Address Register B
0254 1024	DXCH_BFALLOC0	Transmit Channel 0 Frame Allocation Register B
0254 1028	DXCH_BFSIZE0	Transmit Channel 0 Frame Size Register B
0254 102C	DXCH_BFCNT0	Transmit Channel 0 Frame Count Register B
0254 1030 - 0254 103C	-	Reserved
0254 1040	DXCH_ABASE1	Transmit Channel 1 Memory Base Address Register A
0254 1044	DXCH_AFALLOC1	Transmit Channel 1 Frame Allocation Register A
0254 1048	DXCH_AFSIZE1	Transmit Channel 1 Frame Size Register A
0254 104C	DXCH_AFCNT1	Transmit Channel 1 Frame Count Register A
0254 1050 - 0254 105C	-	Reserved
0254 1060	DXCH_BBASE1	Transmit Channel 1 Memory Base Address Register B
0254 1064	DXCH_BFALLOC1	Transmit Channel 1 Frame Allocation Register B
0254 1068	DXCH_BFSIZE1	Transmit Channel 1 Frame Size Register B
0254 106C	DXCH_BFCNT1	Transmit Channel 1 Frame Count Register B
0254 1070 - 0254 107C	-	Reserved
0254 1080	DXCH_ABASE2	Transmit Channel 2 Memory Base Address Register A
0254 1084	DXCH_AFALLOC2	Transmit Channel 2 Frame Allocation Register A
0254 1088	DXCH_AFSIZE2	Transmit Channel 2 Frame Size Register A
0254 108C	DXCH_AFCNT2	Transmit Channel 2 Frame Count Register A
0254 1090 - 0254 109C	-	Reserved
0254 10A0	DXCH_BBASE2	Transmit Channel 2 Memory Base Address Register B
0254 10A4	DXCH_BFALLOC2	Transmit Channel 2 Frame Allocation Register B

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Table 7-80. DMATCU Transmit Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 10A8	DXCH_BFSIZE2	Transmit Channel 2 Frame Size Register B
0254 10AC	DXCH_BFCNT2	Transmit Channel 2 Frame Count Register B
0254 10B0 - 0254 10BC	-	Reserved
0254 10C0	DXCH_ABASE3	Transmit Channel 3 Memory Base Address Register A
0254 10C4	DXCH_AFALLOC3	Transmit Channel 3 Frame Allocation Register A
0254 10C8	DXCH_AFSIZE3	Transmit Channel 3 Frame Size Register A
0254 10CC	DXCH_AFCNT3	Transmit Channel 3 Frame Count Register A
0254 10D0 - 0254 10DC	-	Reserved
0254 10E0	DXCH_BBASE3	Transmit Channel 3 Memory Base Address Register B
0254 10E4	DXCH_BFALLOC3	Transmit Channel 3 Frame Allocation Register B
0254 10E8	DXCH_BFSIZE3	Transmit Channel 3 Frame Size Register B
0254 10EC	DXCH_BFCNT3	Transmit Channel 3 Frame Count Register B
0254 10F0 - 0254 10FC	-	Reserved
0254 1100	DXCH_ABASE4	Transmit Channel 4 Memory Base Address Register A
0254 1104	DXCH_AFALLOC4	Transmit Channel 4 Frame Allocation Register A
0254 1108	DXCH_AFSIZE4	Transmit Channel 4 Frame Size Register A
0254 110C	DXCH_AFCNT4	Transmit Channel 4 Frame Count Register A
0254 1110 - 0254 111C	-	Reserved
0254 1120	DXCH_BBASE4	Transmit Channel 4 Memory Base Address Register B
0254 1124	DXCH_BFALLOC4	Transmit Channel 4 Frame Allocation Register B
0254 1128	DXCH_BFSIZE4	Transmit Channel 4 Frame Size Register B
0254 112C	DXCH_BFCNT4	Transmit Channel 4 Frame Count Register B
0254 1130 - 0254 113C	-	Reserved
0254 1140	DXCH_ABASE5	Transmit Channel 5 Memory Base Address Register A
0254 1144	DXCH_AFALLOC5	Transmit Channel 5 Frame Allocation Register A
0254 1148	DXCH_AFSIZE5	Transmit Channel 5 Frame Size Register A
0254 114C	DXCH_AFCNT5	Transmit Channel 5 Frame Count Register A
0254 1150 - 0254 115C	-	Reserved
0254 1160	DXCH_BBASE5	Transmit Channel 5 Memory Base Address Register B
0254 1164	DXCH_BFALLOC5	Transmit Channel 5 Frame Allocation Register B
0254 1168	DXCH_BFSIZE5	Transmit Channel 5 Frame Size Register B
0254 116C	DXCH_BFCNT5	Transmit Channel 5 Frame Count Register B
0254 1170 - 0254 117C	-	Reserved

Table 7-81. DMATCU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 1800	DRCH_ABASE0	Receive Channel 0 Memory Base Address Register A
0254 1804	DRCH_AFALLOC0	Receive Channel 0 Frame Allocation Register A
0254 1808	DRCH_AFSIZE0	Receive Channel 0 Frame Size Register A
0254 180C	DRCH_AFCNT0	Receive Channel 0 Frame Count Register A
0254 1810 - 0254 181C	-	Reserved
0254 1820	DRCH_BBASE0	Receive Channel 0 Memory Base Address Register B
0254 1824	DRCH_BFALLOC0	Receive Channel 0 Frame Allocation Register B
0254 1828	DRCH _BFSIZE0	Receive Channel 0 Frame Size Register B
0254 182C	DRCH _BFCNT0	Receive Channel 0 Frame Count Register B
0254 1830 - 0254 183C	-	Reserved
0254 1840	DRCH_ABASE1	Receive Channel 1 Memory Base Address Register A

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Table 7-81. DMATCU Receive Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 1844	DRCH_AFALLOC1	Receive Channel 1 Frame Allocation Register A
0254 1848	DRCH_AFSIZE1	Receive Channel 1 Frame Size Register A
0254 184C	DRCH_AFCNT1	Receive Channel 1 Frame Count Register A
0254 1850 - 0254 185C	-	Reserved
0254 1860	DRCH_BBASE1	Receive Channel 1 Memory Base Address Register B
0254 1864	DRCH_BFALLOC1	Receive Channel 1 Frame Allocation Register B
0254 1868	DRCH _BFSIZE1	Receive Channel 1 Frame Size Register B
0254 186C	DRCH _BFCNT1	Receive Channel 1 Frame Count Register B
0254 1870 - 0254 187C	-	Reserved
0254 1880	DRCH_ABASE2	Receive Channel 2 Memory Base Address Register A
0254 1884	DRCH_AFALLOC2	Receive Channel 2 Frame Allocation Register A
0254 1888	DRCH_AFSIZE2	Receive Channel 2 Frame Size Register A
0254 188C	DRCH_AFCNT2	Receive Channel 2 Frame Count Register A
0254 1890 - 0254 189C	-	Reserved
0254 18A0	DRCH_BBASE2	Receive Channel 2 Memory Base Address Register B
0254 18A4	DRCH_BFALLOC2	Receive Channel 2 Frame Allocation Register B
0254 18A8	DRCH _BFSIZE2	Receive Channel 2 Frame Size Register B
0254 18AC	DRCH _BFCNT2	Receive Channel 2 Frame Count Register B
0254 18B0 - 0254 18BC	-	Reserved
0254 18C0	DRCH_ABASE3	Receive Channel 3 Memory Base Address Register A
0254 18C4	DRCH_AFALLOC3	Receive Channel 3 Frame Allocation Register A
0254 18C8	DRCH_AFSIZE3	Receive Channel 3 Frame Size Register A
0254 18CC	DRCH_AFCNT3	Receive Channel 3 Frame Count Register A
0254 18D0 - 0254 18DC	-	Reserved
0254 18E0	DRCH_BBASE3	Receive Channel 3 Memory Base Address Register B
0254 18E4	DRCH_BFALLOC3	Receive Channel 3 Frame Allocation Register B
0254 18E8	DRCH _BFSIZE3	Receive Channel 3 Frame Size Register B
0254 18EC	DRCH _BFCNT3	Receive Channel 3 Frame Count Register B
0254 18F0 - 0254 18FC	-	Reserved
0254 1900	DRCH_ABASE4	Receive Channel 4 Memory Base Address Register A
0254 1904	DRCH_AFALLOC4	Receive Channel 4 Frame Allocation Register A
0254 1908	DRCH_AFSIZE4	Receive Channel 4 Frame Size Register A
0254 190C	DRCH_AFCNT4	Receive Channel 4 Frame Count Register A
0254 1910 - 0254 191C	-	Reserved
0254 1920	DRCH_BBASE4	Receive Channel 4 Memory Base Address Register B
0254 1924	DRCH_BFALLOC4	Receive Channel 4 Frame Allocation Register B
0254 1928	DRCH _BFSIZE4	Receive Channel 4 Frame Size Register B
0254 192C	DRCH _BFCNT4	Receive Channel 4 Frame Count Register B
0254 1930 - 0254 193C	-	Reserved
0254 1940	DRCH_ABASE5	Receive Channel 5 Memory Base Address Register A
0254 1944	DRCH_AFALLOC5	Receive Channel 5 Frame Allocation Register A
0254 1948	DRCH_AFSIZE5	Receive Channel 5 Frame Size Register A
0254 194C	DRCH_AFCNT5	Receive Channel 5 Frame Count Register A
0254 1950 - 0254 195C	-	Reserved
0254 1960	DRCH_BBASE5	Receive Channel 5 Memory Base Address Register B
0254 1964	DRCH_BFALLOC5	Receive Channel 5 Frame Allocation Register B
0254 1968	DRCH _BFSIZE5	Receive Channel 5 Frame Size Register B

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Table 7-81. DMATCU Receive Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 196C	DRCH _BFCNT5	Receive Channel 5 Frame Count Register B
0254 1970 - 0254 197C	-	Reserved

Table 7-82. TDMU Channel Bitmaps

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0254 8000 - 0254 80FC	XBM_XBMA0	Transmit Channel 0 Bitmap A
0254 8100 - 0254 81FC	XBM_XBMB0	Transmit Channel 0 Bitmap B
0254 8200 - 0254 82FC	XBM_XBMA1	Transmit Channel 1 Bitmap A
0254 8300 - 0254 83FC	XBM_XBMB1	Transmit Channel 1 Bitmap B
0254 8400 - 0254 84FC	XBM_XBMA2	Transmit Channel 2 Bitmap A
0254 8500 - 0254 85FC	XBM_XBMB2	Transmit Channel 2 Bitmap B
0254 8600 - 0254 86FC	XBM_XBMA3	Transmit Channel 3 Bitmap A
0254 8700 - 0254 87FC	XBM_XBMB3	Transmit Channel 3 Bitmap B
0254 8800 - 0254 88FC	XBM_XBMA4	Transmit Channel 4 Bitmap A
0254 8900 - 0254 89FC	XBM_XBMB4	Transmit Channel 4 Bitmap B
0254 8A00 - 0254 8AFC	XBM_XBMA5	Transmit Channel 5 Bitmap A
0254 8B00 - 0254 8BFC	XBM_XBMB5	Transmit Channel 5 Bitmap B
0254 8C00 - 0254 BFFC	-	Reserved
0254 C000 - 0254 C0FC	RBM_RBMA0	Receive Channel 0 Bitmap A
0254 C100 - 0254 C1FC	RBM_RBMB0	Receive Channel 0 Bitmap B
0254 C200 - 0254 C2FC	RBM_RBMA1	Receive Channel 1 Bitmap A
0254 C300 - 0254 C3FC	RBM_RBMB1	Receive Channel 1 Bitmap B
0254 C400 - 0254 C4FC	RBM_RBMA2	Receive Channel 2 Bitmap A
0254 C500 - 0254 C5FC	RBM_RBMB2	Receive Channel 2 Bitmap B
0254 C600 - 0254 C6FC	RBM_RBMA3	Receive Channel 3 Bitmap A
0254 C700 - 0254 C7FC	RBM_RBMB3	Receive Channel 3 Bitmap B
0254 C800 - 0254 C8FC	RBM_RBMA4	Receive Channel 4 Bitmap A
0254 C900 - 0254 C9FC	RBM_RBMB4	Receive Channel 4 Bitmap B
0254 CA00 - 0254 CAFC	RBM_RBMA5	Receive Channel 5 Bitmap A
0254 CB00 - 0254 CBFC	RBM_RBMB5	Receive Channel 5 Bitmap B
0254 CC00 - 0254 FFFC	-	Reserved

Table 7-83. TDMU Channel Buffers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0255 0000 - 0255 0DFC	XPING0	Transmit Channel 0 PING Buffer
0255 0100 - 0255 03FC	-	Reserved
0255 0400 - 0255 04FC	XPONG0	Transmit Channel 0 PONG Buffer
0255 0500 - 0255 07FC	-	Reserved
0255 0800 - 0255 08FC	XPING1	Transmit Channel 1 PING Buffer
0255 0900 - 0255 0BFC	-	Reserved
0255 0C00 - 0255 0CFC	XPONG1	Transmit Channel 1 PONG Buffer
0255 0D00 - 0255 0FFC	-	Reserved
0255 1000 - 0255 1DFC	XPING2	Transmit Channel 2 PING Buffer
0255 1100 - 0255 13FC	-	Reserved
0255 1400 - 0255 14FC	XPONG2	Transmit Channel 2 PONG Buffer
0255 1500 - 0255 17FC	-	Reserved
0255 1800 - 0255 18FC	XPING3	Transmit Channel 3 PING Buffer

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Table 7-83. TDMU Channel Buffers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0255 1900 - 0255 1BFC	-	Reserved
0255 1C00 - 0255 1CFC	XPONG3	Transmit Channel 3 PONG Buffer
0255 1D00 - 0255 1FFC	-	Reserved
0255 2000 - 0255 2DFC	XPING4	Transmit Channel 4 PING Buffer
0255 2100 - 0255 23FC	-	Reserved
0255 2400 - 0255 24FC	XPONG4	Transmit Channel 4 PONG Buffer
0255 2500 - 0255 27FC	-	Reserved
0255 2800 - 0255 28FC	XPING5	Transmit Channel 5 PING Buffer
0255 2900 - 0255 2BFC	-	Reserved
0255 2C00 - 0255 2CFC	XPONG5	Transmit Channel 5 PONG Buffer
0255 2D00 - 0255 7FFC	-	Reserved
0255 8000 - 0255 8DFC	RPING0	Receive Channel 0 PING Buffer
0255 8100 - 0255 83FC	-	Reserved
0255 8400 - 0255 84FC	RPONG0	Receive Channel 0 PONG Buffer
0255 8500 - 0255 87FC	-	Reserved
0255 8800 - 0255 88FC	RPING1	Receive Channel 1 PING Buffer
0255 8900 - 0255 8BFC	-	Reserved
0255 8C00 - 0255 8CFC	RPONG1	Receive Channel 1 PONG Buffer
0255 8D00 - 0255 8FFC	-	Reserved
0255 9000 - 0255 9DFC	RPING2	Receive Channel 2 PING Buffer
0255 9100 - 0255 93FC	-	Reserved
0255 9400 - 0255 94FC	RPONG2	Receive Channel 2 PONG Buffer
0255 9500 - 0255 97FC	-	Reserved
0255 9800 - 0255 98FC	RPING3	Receive Channel 3 PING Buffer
0255 9900 - 0255 9BFC	-	Reserved
0255 9C00 - 0255 9CFC	RPONG3	Receive Channel 3 PONG Buffer
0255 9D00 - 0255 9FFC	-	Reserved
0255 A000 - 0255 ADFC	RPING4	Receive Channel 4 PING Buffer
0255 A100 - 0255 A3FC	-	Reserved
0255 A400 - 0255 A4FC	RPONG4	Receive Channel 4 PONG Buffer
0255 A500 - 0255 A7FC	-	Reserved
0255 A800 - 0255 A8FC	RPING5	Receive Channel 5 PING Buffer
0255 A900 - 0255 ABFC	-	Reserved
0255 AC00 - 0255 ACFC	RPONG5	Receive Channel 5 PONG Buffer
0255 AD00 - 0257 FFFC	-	Reserved

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7.14.3 TSIP2 Peripheral Register Descriptions

Table 7-84. TSIP Module Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0000	PID	PID Register
0258 0004	EMUTST	Emulation and Test Register
0258 0008	RST	Reset Register
0258 000C - 0258 007C	-	Reserved

Table 7-85. Serial Interface Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0080	SIUCTL	SIU Global Control Register
0258 0084 - 0258 009C	-	Reserved
0258 00A0	XCLK	Transmit Clock Source Register
0258 00A4	XCTL	Transmit Control Register
0258 00A8	XSIZ	Transmit Size Register
0258 00AC - 0258 00BC	-	Reserved
0258 00C0	RCLK	Receive Clock Source Register
0258 00C4	RCTL	Receive Control Register
0258 00C8	RSIZE	Receive Size Register
0258 00CC - 0258 00FC	-	Reserved

Table 7-86. TDMU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0100	TDMUCTL	TDMU Global Control Register
0258 0104	XFRFC	Transmit Free-Running Frame Counter
0258 0108	RFRFC	Receive Free-Running Frame Counter
0258 010C	TDMUCFG	TDMU Global Configuration Register
0258 0110	XBMST	Transmit Channel Active Status Register
0258 0114	RBMST	Receive Channel Active Status Register
0258 0118 - 0258 017C	-	Reserved

Table 7-87. DMATCU Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0180	DMACTL	DMATCU Global Control Register
0258 0184	XDLY	Transmit Timeslot Delay Counter
0258 0188	RDLY	Receive Timeslot Delay Counter
0258 018C	-	Reserved
0258 0190	XCHST	Transmit Channel Active Status Register
0258 0194	RCHST	Receive Channel Active Status Register
0258 019C - 0258 01FC	-	Reserved

Table 7-88. TDMU Channel Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0200 - 0258 020C	-	TX/RX Channel 0 Error Log Registers
0258 0210 - 0258 021C	-	TX/RX Channel 1 Error Log Registers
0258 0220 - 0258 022C	-	TX/RX Channel 2 Error Log Registers
0258 0230 - 0258 023C	-	TX/RX Channel 3 Error Log Registers

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Table 7-88. TDMU Channel Error Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0240 - 0258 024C	-	TX/RX Channel 4 Error Log Registers
0258 0250 - 0258 025C	-	TX/RX Channel 5 Error Log Registers
0258 0260 - 0258 03FC	-	Reserved

Table 7-89. TX/RX Channels 0-5 Error Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0200	ERRCTL0	TX/RX Channel 0 Error control Register
0258 0204	ERRCNT0	TX/RX Channel 0 Error Count Register
0258 0208	ERRQ0	TX/RX Channel 0 Error Queue Register
0258 020C	-	Reserved
0258 0210	ERRCTL1	TX/RX Channel 1 Error control Register
0258 0214	ERRCNT1	TX/RX Channel 1 Error Count Register
0258 0218	ERRQ1	TX/RX Channel 1 Error Queue Register
0258 021C	-	Reserved
0258 0220	ERRCTL2	TX/RX Channel 2 Error control Register
0258 0224	ERRCNT2	TX/RX Channel 2 Error Count Register
0258 0228	ERRQ2	TX/RX Channel 2 Error Queue Register
0258 022C	-	Reserved
0258 0230	ERRCTL3	TX/RX Channel 3 Error control Register
0258 0234	ERRCNT3	TX/RX Channel 3 Error Count Register
0258 0238	ERRQ3	TX/RX Channel 3 Error Queue Register
0258 023C	-	Reserved
0258 0240	ERRCTL4	TX/RX Channel 4 Error control Register
0258 0244	ERRCNT4	TX/RX Channel 4 Error Count Register
0258 0248	ERRQ4	TX/RX Channel 4 Error Queue Register
0258 024C	-	Reserved
0258 0250	ERRCTL5	TX/RX Channel 5 Error control Register
0258 0254	ERRCNT5	TX/RX Channel 5 Error Count Register
0258 0258	ERRQ5	TX/RX Channel 5 Error Queue Register
0258 025C	-	Reserved

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Table 7-90. TDMU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0800 - 0258 081C	-	Transmit Channel 0 Registers
0258 0820 - 0258 083C	-	Transmit Channel 1 Registers
0258 0840 - 0258 085C	-	Transmit Channel 2 Registers
0258 0860 - 0258 087C	-	Transmit Channel 3 Registers
0258 0880 - 0258 089C	-	Transmit Channel 4 Registers
0258 08A0 - 0258 08BC	-	Transmit Channel 5 Registers
0258 08C0 - 0258 0BFC	-	Reserved
0258 0C00 - 0258 0C1C	-	Receive Channel 0 Registers
0258 0C20 - 0258 0C3C	-	Receive Channel 1 Registers
0258 0C40 - 0258 0C5C	-	Receive Channel 2 Registers
0258 0C60 - 0258 0C7C	-	Receive Channel 3 Registers
0258 0C80 - 0258 0C9C	-	Receive Channel 4 Registers
0258 0CA0 - 0258 0CBC	-	Receive Channel 5 Registers
0258 0CC0 - 0258 0FFC	-	Reserved

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Table 7-91. TDMU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0800	XCHEN0	Transmit Channel 0 Enable Register
0258 0804 - 0258 081C	-	Reserved
0258 0820	XCHEN1	Transmit Channel 1 Enable Register
0258 0824 - 0258 083C	-	Reserved
0258 0840	XCHEN2	Transmit Channel 2 Enable Register
0258 0844 - 0258 085C	-	Reserved
0258 0860	XCHEN3	Transmit Channel 3 Enable Register
0258 0864 - 0258 087C	-	Reserved
0258 0880	XCHEN4	Transmit Channel 4 Enable Register
0258 0884 - 0258 089C	-	Reserved
0258 08A0	XCHEN5	Transmit Channel 5 Enable Register
0258 08A4 - 0258 08BC	-	Reserved

Table 7-92. TDMU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 0C00	RCHEN0	Receive Channel 0 Enable Register
0258 0C04 - 0258 0C1C	-	Reserved
0258 0C20	RCHEN1	Receive Channel 1 Enable Register
0258 0C24 - 0258 0C3C	-	Reserved
0258 0C40	RCHEN2	Receive Channel 2 Enable Register
0258 0C44 - 0258 0C5C	-	Reserved
0258 0C60	RCHEN3	Receive Channel 3 Enable Register
0258 0C64 - 0258 0C7C	-	Reserved
0258 0C80	RCHEN4	Receive Channel 4 Enable Register
0258 0C84 - 0258 0C9C	-	Reserved
0258 0CA0	RCHEN5	Receive Channel 5 Enable Register
0258 0CA4 - 0258 0CBC	-	Reserved

Table 7-93. DMATCU Channel Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 1000 - 0258 101C	-	Transmit Channel 0 Config A Registers
0258 1020 - 0258 103C	-	Transmit Channel 0 Config B Registers
0258 1040 - 0258 105C	-	Transmit Channel 1 Config A Registers
0258 1060 - 0258 107C	-	Transmit Channel 1 Config B Registers
0258 1080 - 0258 109C	-	Transmit Channel 2 Config A Registers
0258 10A0 - 0258 10BC	-	Transmit Channel 2 Config B Registers
0258 10C0 - 0258 10DC	-	Transmit Channel 3 Config A Registers
0258 10E0 - 0258 10FC	-	Transmit Channel 3 Config B Registers
0258 1100 - 0258 111C	-	Transmit Channel 4 Config A Registers
0258 1120 - 0258 113C	-	Transmit Channel 4 Config B Registers
0258 1140 - 0258 115C	-	Transmit Channel 5 Config A Registers
0258 1160 - 0258 117C	-	Transmit Channel 5 Config B Registers
0258 1180 - 0258 17FC	-	Reserved
0258 1800 - 0258 181C	-	Receive Channel 0 Config A Registers
0258 1820 - 0258 183C	-	Receive Channel 0 Config B Registers
0258 1840 - 0258 185C	-	Receive Channel 1 Config A Registers
0258 1860 - 0258 187C	-	Receive Channel 1 Config B Registers

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Table 7-93. DMATCU Channel Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 1880 - 0258 189C	-	Receive Channel 2 Config A Registers
0258 18A0 - 0258 18BC	-	Receive Channel 2 Config B Registers
0258 18C0 - 0258 18DC	-	Receive Channel 3 Config A Registers
0258 18E0 - 0258 18FC	-	Receive Channel 3 Config B Registers
0258 1900 - 0258 191C	-	Receive Channel 4 Config A Registers
0258 1920 - 0258 193C	-	Receive Channel 4 Config B Registers
0258 1940 - 0258 195C	-	Receive Channel 5 Config A Registers
0258 1960 - 0258 197C	-	Receive Channel 5 Config B Registers
0258 1980 - 0258 19FC	-	Reserved

Table 7-94. DMATCU Transmit Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 1000	DXCH_ABASE0	Transmit Channel 0 Memory Base Address Register A
0258 1004	DXCH_AFALLOC0	Transmit Channel 0 Frame Allocation Register A
0258 1008	DXCH_AFSIZE0	Transmit Channel 0 Frame Size Register A
0258 100C	DXCH_AFCNT0	Transmit Channel 0 Frame Count Register A
0258 1010 - 0258 101C	-	Reserved
0258 1020	DXCH_BBASE0	Transmit Channel 0 Memory Base Address Register B
0258 1024	DXCH_BFALLOC0	Transmit Channel 0 Frame Allocation Register B
0258 1028	DXCH_BFSIZE0	Transmit Channel 0 Frame Size Register B
0258 102C	DXCH_BFCNT0	Transmit Channel 0 Frame Count Register B
0258 1030 - 0258 103C	-	Reserved
0258 1040	DXCH_ABASE1	Transmit Channel 1 Memory Base Address Register A
0258 1044	DXCH_AFALLOC1	Transmit Channel 1 Frame Allocation Register A
0258 1048	DXCH_AFSIZE1	Transmit Channel 1 Frame Size Register A
0258 104C	DXCH_AFCNT1	Transmit Channel 1 Frame Count Register A
0258 1050 - 0258 105C	-	Reserved
0258 1060	DXCH_BBASE1	Transmit Channel 1 Memory Base Address Register B
0258 1064	DXCH_BFALLOC1	Transmit Channel 1 Frame Allocation Register B
0258 1068	DXCH_BFSIZE1	Transmit Channel 1 Frame Size Register B
0258 106C	DXCH_BFCNT1	Transmit Channel 1 Frame Count Register B
0258 1070 - 0258 107C	-	Reserved
0258 1080	DXCH_ABASE2	Transmit Channel 2 Memory Base Address Register A
0258 1084	DXCH_AFALLOC2	Transmit Channel 2 Frame Allocation Register A
0258 1088	DXCH_AFSIZE2	Transmit Channel 2 Frame Size Register A
0258 108C	DXCH_AFCNT2	Transmit Channel 2 Frame Count Register A
0258 1090 - 0258 109C	-	Reserved
0258 10A0	DXCH_BBASE2	Transmit Channel 2 Memory Base Address Register B
0258 10A4	DXCH_BFALLOC2	Transmit Channel 2 Frame Allocation Register B
0258 10A8	DXCH_BFSIZE2	Transmit Channel 2 Frame Size Register B
0258 10AC	DXCH_BFCNT2	Transmit Channel 2 Frame Count Register B
0258 10B0 - 0258 10BC	-	Reserved
0258 10C0	DXCH_ABASE3	Transmit Channel 3 Memory Base Address Register A
0258 10C4	DXCH_AFALLOC3	Transmit Channel 3 Frame Allocation Register A
0258 10C8	DXCH_AFSIZE3	Transmit Channel 3 Frame Size Register A
0258 10CC	DXCH_AFCNT3	Transmit Channel 3 Frame Count Register A
0258 10D0 - 0258 10DC	-	Reserved

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Table 7-94. DMATCU Transmit Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 10E0	DXCH_BBASE3	Transmit Channel 3 Memory Base Address Register B
0258 10E4	DXCH_BFALLOC3	Transmit Channel 3 Frame Allocation Register B
0258 10E8	DXCH_BFSIZE3	Transmit Channel 3 Frame Size Register B
0258 10EC	DXCH_BFCNT3	Transmit Channel 3 Frame Count Register B
0258 10F0 - 0258 10FC	-	Reserved
0258 1100	DXCH_ABASE4	Transmit Channel 4 Memory Base Address Register A
0258 1104	DXCH_AFALLOC4	Transmit Channel 4 Frame Allocation Register A
0258 1108	DXCH_AFSIZE4	Transmit Channel 4 Frame Size Register A
0258 110C	DXCH_AFCNT4	Transmit Channel 4 Frame Count Register A
0258 1110 - 0258 111C	-	Reserved
0258 1120	DXCH_BBASE4	Transmit Channel 4 Memory Base Address Register B
0258 1124	DXCH_BFALLOC4	Transmit Channel 4 Frame Allocation Register B
0258 1128	DXCH_BFSIZE4	Transmit Channel 4 Frame Size Register B
0258 112C	DXCH_BFCNT4	Transmit Channel 4 Frame Count Register B
0258 1130 - 0258 113C	-	Reserved
0258 1140	DXCH_ABASE5	Transmit Channel 5 Memory Base Address Register A
0258 1144	DXCH_AFALLOC5	Transmit Channel 5 Frame Allocation Register A
0258 1148	DXCH_AFSIZE5	Transmit Channel 5 Frame Size Register A
0258 114C	DXCH_AFCNT5	Transmit Channel 5 Frame Count Register A
0258 1150 - 0258 115C	-	Reserved
0258 1160	DXCH_BBASE5	Transmit Channel 5 Memory Base Address Register B
0258 1164	DXCH_BFALLOC5	Transmit Channel 5 Frame Allocation Register B
0258 1168	DXCH_BFSIZE5	Transmit Channel 5 Frame Size Register B
0258 116C	DXCH_BFCNT5	Transmit Channel 5 Frame Count Register B
0258 1170 - 0258 117C	-	Reserved

Table 7-95. DMATCU Receive Channels 0-5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 1800	DRCH_ABASE0	Receive Channel 0 Memory Base Address Register A
0258 1804	DRCH_AFALLOC0	Receive Channel 0 Frame Allocation Register A
0258 1808	DRCH_AFSIZE0	Receive Channel 0 Frame Size Register A
0258 180C	DRCH_AFCNT0	Receive Channel 0 Frame Count Register A
0258 1810 - 0258 181C	-	Reserved
0258 1820	DRCH_BBASE0	Receive Channel 0 Memory Base Address Register B
0258 1824	DRCH_BFALLOC0	Receive Channel 0 Frame Allocation Register B
0258 1828	DRCH _BFSIZE0	Receive Channel 0 Frame Size Register B
0258 182C	DRCH _BFCNT0	Receive Channel 0 Frame Count Register B
0258 1830 - 0258 183C	-	Reserved
0258 1840	DRCH_ABASE1	Receive Channel 1 Memory Base Address Register A
0258 1844	DRCH_AFALLOC1	Receive Channel 1 Frame Allocation Register A
0258 1848	DRCH_AFSIZE1	Receive Channel 1 Frame Size Register A
0258 184C	DRCH_AFCNT1	Receive Channel 1 Frame Count Register A
0258 1850 - 0258 185C	-	Reserved
0258 1860	DRCH_BBASE1	Receive Channel 1 Memory Base Address Register B
0258 1864	DRCH_BFALLOC1	Receive Channel 1 Frame Allocation Register B
0258 1868	DRCH _BFSIZE1	Receive Channel 1 Frame Size Register B
0258 186C	DRCH _BFCNT1	Receive Channel 1 Frame Count Register B

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Table 7-95. DMATCU Receive Channels 0-5 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 1870 - 0258 187C	-	Reserved
0258 1880	DRCH_ABASE2	Receive Channel 2 Memory Base Address Register A
0258 1884	DRCH_AFALLOC2	Receive Channel 2 Frame Allocation Register A
0258 1888	DRCH_AFSIZE2	Receive Channel 2 Frame Size Register A
0258 188C	DRCH_AFCNT2	Receive Channel 2 Frame Count Register A
0258 1890 - 0258 189C	-	Reserved
0258 18A0	DRCH_BBASE2	Receive Channel 2 Memory Base Address Register B
0258 18A4	DRCH_BFALLOC2	Receive Channel 2 Frame Allocation Register B
0258 18A8	DRCH _BFSIZE2	Receive Channel 2 Frame Size Register B
0258 18AC	DRCH _BFCNT2	Receive Channel 2 Frame Count Register B
0258 18B0 - 0258 18BC	-	Reserved
0258 18C0	DRCH_ABASE3	Receive Channel 3 Memory Base Address Register A
0258 18C4	DRCH_AFALLOC3	Receive Channel 3 Frame Allocation Register A
0258 18C8	DRCH_AFSIZE3	Receive Channel 3 Frame Size Register A
0258 18CC	DRCH_AFCNT3	Receive Channel 3 Frame Count Register A
0258 18D0 - 0258 18DC	-	Reserved
0258 18E0	DRCH_BBASE3	Receive Channel 3 Memory Base Address Register B
0258 18E4	DRCH_BFALLOC3	Receive Channel 3 Frame Allocation Register B
0258 18E8	DRCH _BFSIZE3	Receive Channel 3 Frame Size Register B
0258 18EC	DRCH _BFCNT3	Receive Channel 3 Frame Count Register B
0258 18F0 - 0258 18FC	-	Reserved
0258 1900	DRCH_ABASE4	Receive Channel 4 Memory Base Address Register A
0258 1904	DRCH_AFALLOC4	Receive Channel 4 Frame Allocation Register A
0258 1908	DRCH_AFSIZE4	Receive Channel 4 Frame Size Register A
0258 190C	DRCH_AFCNT4	Receive Channel 4 Frame Count Register A
0258 1910 - 0258 191C	-	Reserved
0258 1920	DRCH_BBASE4	Receive Channel 4 Memory Base Address Register B
0258 1924	DRCH_BFALLOC4	Receive Channel 4 Frame Allocation Register B
0258 1928	DRCH _BFSIZE4	Receive Channel 4 Frame Size Register B
0258 192C	DRCH _BFCNT4	Receive Channel 4 Frame Count Register B
0258 1930 - 0258 193C	-	Reserved
0258 1940	DRCH_ABASE5	Receive Channel 5 Memory Base Address Register A
0258 1944	DRCH_AFALLOC5	Receive Channel 5 Frame Allocation Register A
0258 1948	DRCH_AFSIZE5	Receive Channel 5 Frame Size Register A
0258 194C	DRCH_AFCNT5	Receive Channel 5 Frame Count Register A
0258 1950 - 0258 195C	-	Reserved
0258 1960	DRCH_BBASE5	Receive Channel 5 Memory Base Address Register B
0258 1964	DRCH_BFALLOC5	Receive Channel 5 Frame Allocation Register B
0258 1968	DRCH _BFSIZE5	Receive Channel 5 Frame Size Register B
0258 196C	DRCH _BFCNT5	Receive Channel 5 Frame Count Register B
0258 1970 - 0258 197C	-	Reserved

Table 7-96. TDMU Channel Bitmaps

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 8000 - 0258 80FC	XBM_XBMA0	Transmit Channel 0 Bitmap A
0258 8100 - 0258 81FC	XBM_XBMB0	Transmit Channel 0 Bitmap B
0258 8200 - 0258 82FC	XBM_XBMA1	Transmit Channel 1 Bitmap A

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Table 7-96. TDMU Channel Bitmaps (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0258 8300 - 0258 83FC	XBM_XBMB1	Transmit Channel 1 Bitmap B
0258 8400 - 0258 84FC	XBM_XBMA2	Transmit Channel 2 Bitmap A
0258 8500 - 0258 85FC	XBM_XBMB2	Transmit Channel 2 Bitmap B
0258 8600 - 0258 86FC	XBM_XBMA3	Transmit Channel 3 Bitmap A
0258 8700 - 0258 87FC	XBM_XBMB3	Transmit Channel 3 Bitmap B
0258 8800 - 0258 88FC	XBM_XBMA4	Transmit Channel 4 Bitmap A
0258 8900 - 0258 89FC	XBM_XBMB4	Transmit Channel 4 Bitmap B
0258 8A00 - 0258 8AFC	XBM_XBMA5	Transmit Channel 5 Bitmap A
0258 8B00 - 0258 8BFC	XBM_XBMB5	Transmit Channel 5 Bitmap B
0258 8C00 - 0258 BFFC	-	Reserved
0258 C000 - 0258 C0FC	RBM_RBMA0	Receive Channel 0 Bitmap A
0258 C100 - 0258 C1FC	RBM_RBMB0	Receive Channel 0 Bitmap B
0258 C200 - 0258 C2FC	RBM_RBMA1	Receive Channel 1 Bitmap A
0258 C300 - 0258 C3FC	RBM_RBMB1	Receive Channel 1 Bitmap B
0258 C400 - 0258 C4FC	RBM_RBMA2	Receive Channel 2 Bitmap A
0258 C500 - 0258 C5FC	RBM_RBMB2	Receive Channel 2 Bitmap B
0258 C600 - 0258 C6FC	RBM_RBMA3	Receive Channel 3 Bitmap A
0258 C700 - 0258 C7FC	RBM_RBMB3	Receive Channel 3 Bitmap B
0258 C800 - 0258 C8FC	RBM_RBMA4	Receive Channel 4 Bitmap A
0258 C900 - 0258 C9FC	RBM_RBMB4	Receive Channel 4 Bitmap B
0258 CA00 - 0258 CAFC	RBM_RBMA5	Receive Channel 5 Bitmap A
0258 CB00 - 0258 CBFC	RBM_RBMB5	Receive Channel 5 Bitmap B
0258 CC00 - 0258 FFFC	-	Reserved

Table 7-97. TDMU Channel Buffers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0259 0000 - 0259 0DFC	XPING0	Transmit Channel 0 PING Buffer
0259 0100 - 0259 03FC	-	Reserved
0259 0400 - 0259 04FC	XPONG0	Transmit Channel 0 PONG Buffer
0259 0500 - 0259 07FC	-	Reserved
0259 0800 - 0259 08FC	XPING1	Transmit Channel 1 PING Buffer
0259 0900 - 0259 0BFC	-	Reserved
0259 0C00 - 0259 0CFC	XPONG1	Transmit Channel 1 PONG Buffer
0259 0D00 - 0259 0FFC	-	Reserved
0259 1000 - 0259 1DFC	XPING2	Transmit Channel 2 PING Buffer
0259 1100 - 0259 13FC	-	Reserved
0259 1400 - 0259 14FC	XPONG2	Transmit Channel 2 PONG Buffer
0259 1500 - 0259 17FC	-	Reserved
0259 1800 - 0259 18FC	XPING3	Transmit Channel 3 PING Buffer
0259 1900 - 0259 1BFC	-	Reserved
0259 1C00 - 0259 1CFC	XPONG3	Transmit Channel 3 PONG Buffer
0259 1D00 - 0259 1FFC	-	Reserved
0259 2000 - 0259 2DFC	XPING4	Transmit Channel 4 PING Buffer
0259 2100 - 0259 23FC	-	Reserved
0259 2400 - 0259 24FC	XPONG4	Transmit Channel 4 PONG Buffer
0259 2500 - 0259 27FC	-	Reserved
0259 2800 - 0259 28FC	XPING5	Transmit Channel 5 PING Buffer

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Table 7-97. TDMU Channel Buffers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0259 2900 - 0259 2BFC	-	Reserved
0259 2C00 - 0259 2CFC	XPONG5	Transmit Channel 5 PONG Buffer
0259 2D00 - 0259 7FFC	-	Reserved
0259 8000 - 0259 8DFC	RPING0	Receive Channel 0 PING Buffer
0259 8100 - 0259 83FC	-	Reserved
0259 8400 - 0259 84FC	RPONG0	Receive Channel 0 PONG Buffer
0259 8500 - 0259 87FC	-	Reserved
0259 8800 - 0259 88FC	RPING1	Receive Channel 1 PING Buffer
0259 8900 - 0259 8BFC	-	Reserved
0259 8C00 - 0259 8CFC	RPONG1	Receive Channel 1 PONG Buffer
0259 8D00 - 0259 8FFC	-	Reserved
0259 9000 - 0259 9DFC	RPING2	Receive Channel 2 PING Buffer
0259 9100 - 0259 93FC	-	Reserved
0259 9400 - 0259 94FC	RPONG2	Receive Channel 2 PONG Buffer
0259 9500 - 0259 97FC	-	Reserved
0259 9800 - 0259 98FC	RPING3	Receive Channel 3 PING Buffer
0259 9900 - 0259 9BFC	-	Reserved
0259 9C00 - 0259 9CFC	RPONG3	Receive Channel 3 PONG Buffer
0259 9D00 - 0259 9FFC	-	Reserved
0259 A000 - 0259 ADFC	RPING4	Receive Channel 4 PING Buffer
0259 A100 - 0259 A3FC	-	Reserved
0259 A400 - 0259 A4FC	RPONG4	Receive Channel 4 PONG Buffer
0259 A500 - 0259 A7FC	-	Reserved
0259 A800 - 0259 A8FC	RPING5	Receive Channel 5 PING Buffer
0259 A900 - 0259 ABFC	-	Reserved
0259 AC00 - 0259 ACFC	RPONG5	Receive Channel 5 PONG Buffer
0259 AD00 - 025B FFFC	-	Reserved

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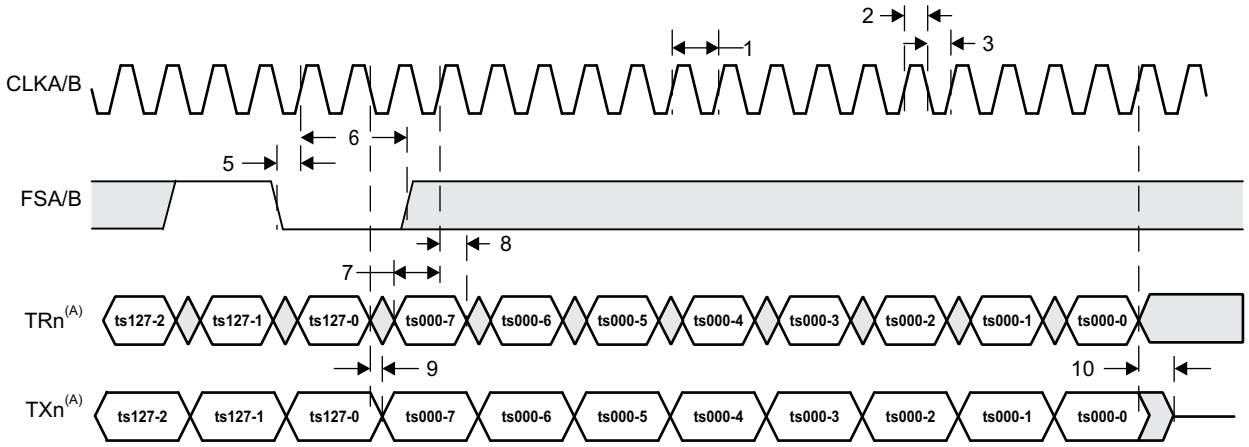
7.14.4 TSIP Electrical Data/Timing

Table 7-98. Timing Requirements for TSIP 2X Mode(1)

(see Figure 7-45)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, CLK rising edge to next CLK rising edge	61(2)		ns
2	$t_{w(CLKL)}$	Pulse duration, CLK low	0.4 $t_{c(clk)}$		ns
3	$t_{w(CLKH)}$	Pulse duration, CLK high	0.4 $t_{c(clk)}$		ns
4	$t_{t(CLK)}$	Transition time, CLK high to low or CLK low to high		2	ns
5	$t_{su(FS-CLK)}$	Setup time, f_s valid before rising CLK	5		ns
6	$t_{h(CLK-FS)}$	Hold time, f_s valid after rising CLK	5		ns
7	$t_{su(TR-CLK)}$	Setup time, t_r valid before rising CLK	5		ns
8	$t_{h(CLK-TR)}$	Hold time, t_r valid before rising CLK	5		ns
9	$t_{d(CLKL-TX)}$	Delay time, CLK low to TX valid	1	12	ns
10	$t_{dis(CLKH-TXZ)}$	Disable time, CLK low to TX tristate	2	10	ns

(1) Polarities of XMTFSYNCP = 0b, XMTFCLKP = 0, XMTDCLKP = 1b, RCVFSYNCP = 0, RCVFCLKP = 0, RCVDCLKP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Timing shown is for 8.192 Mbps links. Timing for 16.384 Mbps and 32.768 Mbps links is 30.5 ns and 15.2 ns, respectively.



A. Example timeslot numbering shown is for 8.192 Mbps links; 16.384 Mbps links have timeslots numbered 0 through 255 and 32.768 Mbps links have timeslots numbered 0 through 511. The data timing shown relative to the clock and frame sync signals would require a RCVDATD=1 and a XMTDATD=1.

Figure 7-45. TSIP 2x Timing Diagram

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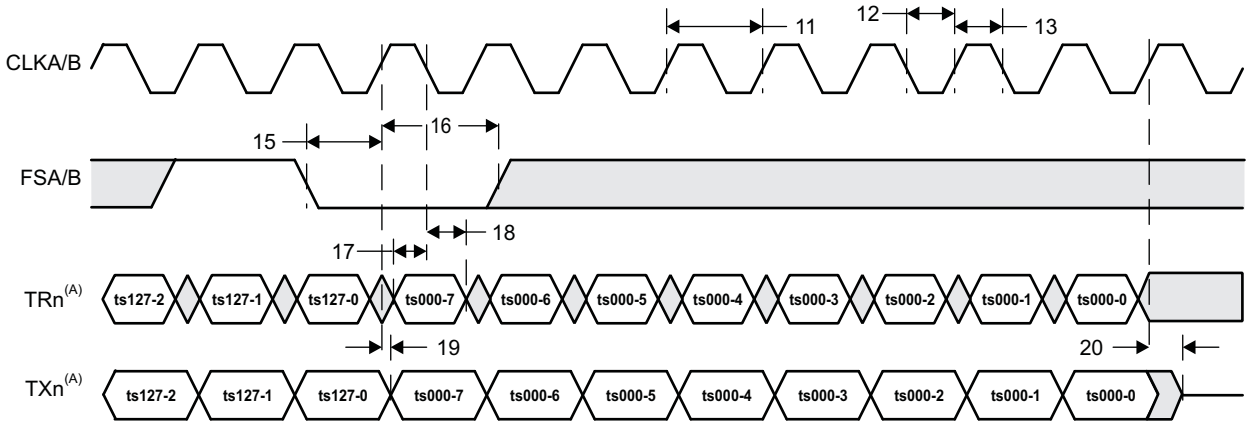
Table 7-99. Timing Requirements for TSIP 1X Mode(1)

(see Figure 7-46)

NO.			500/625/700		UNIT
			MIN	MAX	
11	$t_{c(CLK)}$	Cycle time, CLK rising edge to next CLK rising edge	122.1(2)		ns
12	$t_{w(CLKL)}$	Pulse duration, CLK low	0.4 $t_{c(clk)}$		ns
13	$t_{w(CLKH)}$	Pulse duration, CLK high	0.4 $t_{c(clk)}$		ns
14	$t_{t(CLK)}$	Transition time, CLK high to low or CLK low to high		2	ns
15	$t_{su(FS-CLK)}$	Setup time, f_s valid before rising CLK	5		ns
16	$t_{h(CLK-FS)}$	Hold time, f_s valid after rising CLK	5		ns
17	$t_{su(TR-CLK)}$	Setup time, t_r valid before falling CLK	5		ns
18	$t_{h(CLK-TR)}$	Hold time, t_r valid before falling CLK	5		ns
19	$t_{d(CLKH-TX)}$	Delay time, CLK high to TX valid (1024(2) clock cycles plus)	1	12	ns
20	$t_{dis(CLKH-TXZ)}$	Disable time, CLK high to TX tristate	1	12	ns

(1) Polarities of XMTFSYNCP = 0b, XMTFCLKP = 0, XMTDCLKP = 0b, RCVFSYNCP = 0, RCVFCLKP = 0, RCVDCLKP = 1. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Timing shown is for 8.192 Mbps links. Timing for 16.384 Mbps and 32.768 Mbps links is 61 ns and 30.5 ns, respectively.



A. Example timeslot numbering shown is for 8.192 Mbps links; 16.384 Mbps links have timeslots numbered 0 through 255 and 32.768 Mbps links have timeslots numbered 0 through 511. The data timing shown relative to the clock and frame sync signals would require a RCVDATD=1023 and a XMTDATD=1023.

Figure 7-46. TSIP 1x Timing Diagram

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7.15 Ethernet MAC (EMAC)

The C6472 device contains two Ethernet Media Access Controller (EMAC) interfaces. Each EMAC module provides an efficient interface between the C6472 DSP core processor and the networked community. The EMAC supports 10Base-T (10 Mbits/second [Mbps]), and 100BaseTX (100 Mbps), in either half- or full-duplex mode, and 1000BaseT (1000 Mbps) in full-duplex mode, with hardware flow control and quality-of-service (QOS) support.

The EMAC module conforms to the IEEE 802.3-2002 standard, describing the “Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer” specifications. The IEEE 802.3 standard has also been adopted by ISO/IEC and re-designated as ISO/IEC 8802-3:2000(E).

One deviation from this standard, the EMAC module does not use the Transmit Coding Error signal MTXER. Instead of driving the error pin when an underflow condition occurs on a transmitted frame, the EMAC will intentionally generate an incorrect checksum by inverting the frame CRC, so that the transmitted frame will be detected as an error by the network.

The EMAC control module is the main interface between the device core processor, the MDIO module, and the EMAC module. The relationship between these three components is shown in Figure 7-47. The EMAC control module contains the necessary components to allow the EMAC to make efficient use of device memory, plus it controls device interrupts. The EMAC control module incorporates 8K-bytes of internal RAM to hold EMAC buffer descriptors.

For more detailed information on the EMAC/MDIO, see the *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (literature number SPRUEF8).

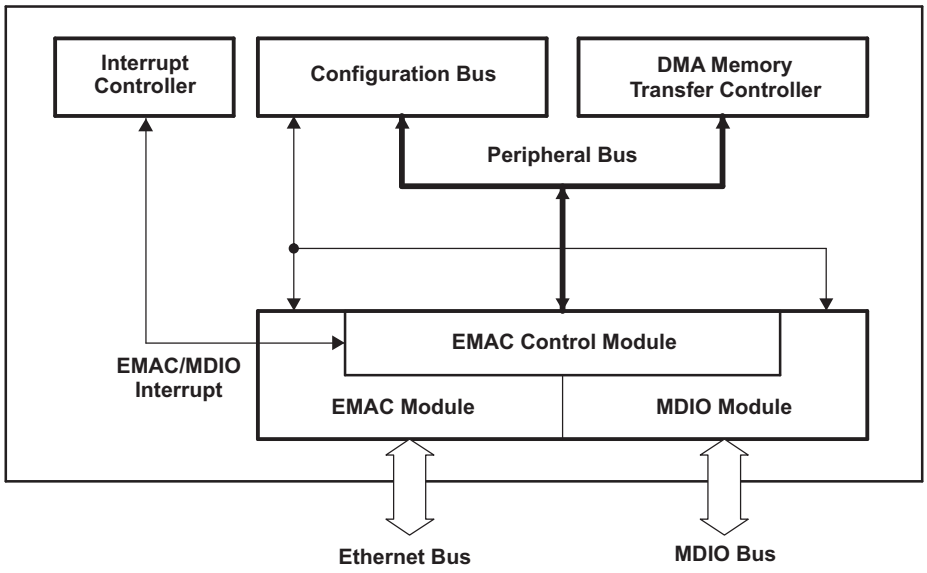

Figure 7-47. EMAC, MDIO, and EMAC Control Modules

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7.15.1 EMAC Device-Specific Information

Interface Modes

The EMAC module on the TMS320C6472 device supports five interface modes: Media Independent Interface (MII), Reduced Media Independent Interface (RMII), Source Synchronous Serial Media Independent Interface (S3MII), Gigabit Media Independent Interface (GMII), and Reduced Gigabit Media Independent Interface (RGMII). The MII and GMII interface modes are defined in the IEEE 802.3-2002 standard.

The RGMII mode of the EMAC conforms to the Reduced Gigabit Media Independent Interface (RGMII) Specification (version 2.0). The RGMII mode implements the same functionality as the GMII mode, but with a reduced number of pins. Data and control information is transmitted and received using both edges of the transmit and receive clocks (TXC and RXC).

Note: The EMAC internally delays the transmit clock (TXC) with respect to the transmit data and control pins. Therefore, the EMAC conforms to the RGMII-ID operation of the RGMII specification. However, the EMAC does not delay the receive clock (RXC); this signal must be delayed with respect to the receive data and control pins outside of the DSP.

The RMII mode of the EMAC conforms to the RMII Specification (revision 1.2), as written by the RMII Consortium, except for the half-duplex mode, which is not supported. As the name implies, the Reduced Media Independent Interface (RMII) mode is a reduced pin count version of the MII mode.

The S3MII mode of the EMAC conforms to the Serial-MII Specification (revision 2.1).

Interface Mode Select

The EMAC uses the same pins for the (G)MII, RMII, and S3MII modes. Standalone pins are included for the RGMII mode, due to specific voltage requirements. Only one mode can be used at a time for each EMAC port. The mode used is selected at device reset based on the MACSEL0[2:0] and MACSEL1[1:0] configuration pins (for more detailed information, see Section 3, *Device Configuration*, of this document). Table 7-100 shows all the multiplexed pins used in the (G)MII, RMII, and S3MII modes on EMAC. For a detailed description of these pin functions, see Section 2.7, *Terminal Functions*.

Table 7-100. EMAC/MDIO Multiplexed Pins (MII, GMII0, RMII, and S3MII Modes)

PIN NUMBER	SIGNAL NAME	MII0	GMII0	RMII0	RMII1	S3MII0	S3MII1
AH11	MRXD00/RMRXD00/SRXD0	MRXD00	MRXD00	RMRXD00		SRXD0	
AG12	MRXD01/RMRXD01/SRXSYNC0	MRXD01	MRXD01	RMRXD01		SRXSYNC0	
AJ11	MRXD02/SRXD1	MRXD02	MRXD02				SRXD1
AG10	MRCLK0/SRXCLK1	MRCLK0	MRCLK0				SRXCLK1
AJ10	MRXD03/SRXSYNC1	MRXD03	MRXD03				SRXSYNC1
AH9	MRXD04/RMRXD10		MRXD04		RMRXD10		
AG7	MRXD05/RMRXD11		MRXD05		RMRXD11		
AJ13	MRXD06/RMRXER1		MRXD06		RMRXER1		
AJ6	MRXD07		MRXD07				
AE12	MRXDV0/RMCRSDV1	MRXDV0	MRXDV0		RMCRSDV1		
AF12	MRXER0/RMRXER0/SRXCLK0	MRXER0	MRXER0	RMRXER0		SRXCLK0	
AF10	MCRS0/RMCRSDV0	MCRS0	MCRS0	RMCRSDV0			
AG6	GMTCLK0/REFCLK1/SREFCLK1		GMTCLK0		REFCLK1		SREFCLK1
AJ9	MTCLK0/REFCLK0/SREFCLK0	MTCLK0	MTCLK0	REFCLK0		SREFCLK0	
AF8	MTXD00/RMTXD00/STXD0	MTXD00	MTXD00	RMTXD00		STXD0	
AH7	MTXD01/RMTXD01/STXSYNC0	MTXD01	MTXD01	RMTXD01		STXSYNC0	
AG8	MTXD02/STXD1	MTXD02	MTXD02				STXD1
AF9	MTXD03/STXSYNC1	MTXD03	MTXD03				STXSYNC1

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Table 7-100. EMAC/MDIO Multiplexed Pins (MII, GMII0, RMII, and S3MII Modes) (continued)

PIN NUMBER	SIGNAL NAME	MII0	GMII0	RMII0	RMII1	S3MII0	S3MII1
AE7	MTXD04/RMTXD10/STXCLK1		MTXD04		RMTXD10		STXCLK1
AJ7	MTXD05/RMTXD11		MTXD05		RMTXD11		
AE11	MTXD06/RMTXEN1		MTXD06		RMTXEN1		
AG11	MTXD07/STXCLK0		MTXD07			STXCLK0	
AF11	MTXEN0/RMTXEN0	MTXEN0	MTXEN0	RMTXEN0			
AE8	MCOL0	MCOL0	MCOL0				
AH10	GMDIO	GMDIO	GMDIO				
AG9	GMDCLK	GMDCLK	GMDCLK				

The on-chip PLL2 and PLL2 Controller generate all the internal clocks to the EMAC module. When enabled, the input clock to the PLL2 Controller (CLKIN2) must have a 25-MHz frequency. For more information, see Section 7.9, *PLL2 and PLL2 Controller*, of this document.

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7.15.2 EMAC Peripheral Register Descriptions

Table 7-101. EMAC0 Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 0000	TXIDVER	Transmit Identification and Version Register
02C8 0004	TXCONTROL	Transmit Control Register
02C8 0008	TXTEARDOWN	Transmit Teardown Register
02C8 000F	-	Reserved
02C8 0010	RXIDVER	Receive Identification and Version Register
02C8 0014	RXCONTROL	Receive Control Register
02C8 0018	RXTEARDOWN	Receive Teardown Register
02C8 001C	-	Reserved
02C8 0020 - 02C8 007C	-	Reserved
02C8 0080	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
02C8 0084	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
02C8 0088	TXINTMASKSET	Transmit Interrupt Mask Set Register
02C8 008C	TXINTMASKCLEAR	Transmit Interrupt Mask Clear Register
02C8 0090	MACINVECTOR	MAC Input Vector Register
02C8 0094	MACEOIVECTOR	MAC End-of-Interrupt Vector Register
02C8 0098 - 02C8 009C	-	Reserved
02C8 00A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
02C8 00A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
02C8 00A8	RXINTMASKSET	Receive Interrupt Mask Set Register
02C8 00AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
02C8 00B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register
02C8 00B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
02C8 00B8	MACINTMASKSET	MAC Interrupt Mask Set Register
02C8 00BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
02C8 00C0 - 02C8 00FC	-	Reserved
02C8 0100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
02C8 0104	RXUNICASTSET	Receive Unicast Enable Set Register
02C8 0108	RXUNICASTCLEAR	Receive Unicast Clear Register
02C8 010C	RXMAXLEN	Receive Maximum Length Register
02C8 0110	RXBUFFEROFFSET	Receive Buffer Offset Register
02C8 0114	RXFILTERLOWTHRESH	Receive Filter Low Priority Frame Threshold Register
02C8 0118 - 02C8 011C	-	Reserved
02C8 0120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
02C8 0124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
02C8 0128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
02C8 012C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
02C8 0130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
02C8 0134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
02C8 0138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
02C8 013C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register
02C8 0140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
02C8 0144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
02C8 0148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
02C8 014C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
02C8 0150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register

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Table 7-101. EMAC0 Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 0154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
02C8 0158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register
02C8 015C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
02C8 0160	MACCONTROL	MAC Control Register
02C8 0164	MACSTATUS	MAC Status Register
02C8 0168	EMCONTROL	Emulation Control Register
02C8 016C	FIFOCONTROL	FIFO Control Register (Transmit and Receive)
02C8 0170	MACCONFIG	MAC Configuration Register
02C8 0174	SOFTRESET	Soft Reset Register
02C8 0178 - 02C8 01CC	-	Reserved
02C8 01D0	MACSRCADDRLO	MAC Source Address Low Bytes Register (Lower 16-bits)
02C8 01D4	MACSRCADDRHI	MAC Source Address High Bytes Register (Upper 16-bits)
02C8 01D8	MACHASH1	MAC Hash Address Register 1
02C8 01DC	MACHASH2	MAC Hash Address Register 2
02C8 01E0	BOFFTEST	Back Off Test Register
02C8 01E4	TPACETEST	Transmit Pacing Algorithm Test Register
02C8 01E8	RXPAUSE	Receive Pause Timer Register
02C8 01EC	TXPAUSE	Transmit Pause Timer Register
02C8 01F0 - 02C8 01FC	-	Reserved
02C8 0200 - 02C8 02FC	(see Table 7-102)	EMAC Statistics Registers
02C8 0300 - 02C8 04FC	-	Reserved
02C8 0500	MACADDRLO	MAC Address Low Bytes Register (Used in Receive Address Matching)
02C8 0504	MACADDRHI	MAC Address High Bytes Register (Used in Receive Address Matching)
02C8 0508	MACINDEX	MAC Index Register
02C8 050C - 02C8 05FC	-	Reserved
02C8 0600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
02C8 0604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
02C8 0608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
02C8 060C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
02C8 0610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
02C8 0614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
02C8 0618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
02C8 061C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register
02C8 0620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
02C8 0624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
02C8 0628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register
02C8 062C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
02C8 0630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
02C8 0634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
02C8 0638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
02C8 063C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
02C8 0640	TX0CP	Transmit Channel 0 Completion Pointer (Interrupt Acknowledge) Register
02C8 0644	TX1CP	Transmit Channel 1 Completion Pointer (Interrupt Acknowledge) Register
02C8 0648	TX2CP	Transmit Channel 2 Completion Pointer (Interrupt Acknowledge) Register

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Table 7-101. EMAC0 Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 064C	TX3CP	Transmit Channel 3 Completion Pointer (Interrupt Acknowledge) Register
02C8 0650	TX4CP	Transmit Channel 4 Completion Pointer (Interrupt Acknowledge) Register
02C8 0654	TX5CP	Transmit Channel 5 Completion Pointer (Interrupt Acknowledge) Register
02C8 0658	TX6CP	Transmit Channel 6 Completion Pointer (Interrupt Acknowledge) Register
02C8 065C	TX7CP	Transmit Channel 7 Completion Pointer (Interrupt Acknowledge) Register
02C8 0660	RX0CP	Receive Channel 0 Completion Pointer (Interrupt Acknowledge) Register
02C8 0664	RX1CP	Receive Channel 1 Completion Pointer (Interrupt Acknowledge) Register
02C8 0668	RX2CP	Receive Channel 2 Completion Pointer (Interrupt Acknowledge) Register
02C8 066C	RX3CP	Receive Channel 3 Completion Pointer (Interrupt Acknowledge) Register
02C8 0670	RX4CP	Receive Channel 4 Completion Pointer (Interrupt Acknowledge) Register
02C8 0674	RX5CP	Receive Channel 5 Completion Pointer (Interrupt Acknowledge) Register
02C8 0678	RX6CP	Receive Channel 6 Completion Pointer (Interrupt Acknowledge) Register
02C8 067C	RX7CP	Receive Channel 7 Completion Pointer (Interrupt Acknowledge) Register
02C8 0680 - 02C8 0FFC	-	Reserved

Table 7-102. EMAC0 Statistics Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 0200	RXGOODFRAMES	Good Receive Frames Register
02C8 0204	RXBCASTFRAMES	Broadcast Receive Frames Register (Total number of good broadcast frames received)
02C8 0208	RXMCASTFRAMES	Multicast Receive Frames Register (Total number of good multicast frames received)
02C8 020C	RXPAUSEFRAMES	Pause Receive Frames Register
02C8 0210	RXCRCERRORS	Receive CRC Errors Register (Total number of frames received with CRC errors)
02C8 0214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors)
02C8 0218	RXOVERSIZED	Receive Oversized Frames Register (Total number of oversized frames received)
02C8 021C	RXJABBER	Receive Jabber Frames Register (Total number of jabber frames received)
02C8 0220	RXUNDERSIZED	Receive Undersized Frames Register (Total number of undersized frames received)
02C8 0224	RXFRAGMENTS	Receive Frame Fragments Register
02C8 0228	RXFILTERED	Filtered Receive Frames Register
02C8 022C	RXQOSFILTERED	Received QOS Filtered Frames Register
02C8 0230	RXOCTETS	Receive Octet Frames Register (Total number of received bytes in good frames)
02C8 0234	TXGOODFRAMES	Good Transmit Frames Register (Total number of good frames transmitted)
02C8 0238	TXBCASTFRAMES	Broadcast Transmit Frames Register

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Table 7-102. EMAC0 Statistics Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 023C	TXMCASTFRAMES	Multicast Transmit Frames Register
02C8 0240	TXPAUSEFRAMES	Pause Transmit Frames Register
02C8 0244	TXDEFERRED	Deferred Transmit Frames Register
02C8 0248	TXCOLLISION	Transmit Collision Frames Register
02C8 024C	TXSINGLECOLL	Transmit Single Collision Frames Register
02C8 0250	TXMULTICOLL	Transmit Multiple Collision Frames Register
02C8 0254	TXEXCESSIVECOLL	Transmit Excessive Collision Frames Register
02C8 0258	TXLATECOLL	Transmit Late Collision Frames Register
02C8 025C	TXUNDERRUN	Transmit Underrun Error Register
02C8 0260	TXCARRIERSENSE	Transmit Carrier Sense Errors Register
02C8 0264	TXOCTETS	Transmit Octet Frames Register
02C8 0268	FRAME64	Transmit and Receive 64 Octet Frames Register
02C8 026C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
02C8 0270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
02C8 0274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
02C8 0278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
02C8 027C	FRAME1024TUP	Transmit and Receive 1024 to 1518 Octet Frames Register
02C8 0280	NETOCTETS	Network Octet Frames Register
02C8 0284	RXSOFOVERRUNS	Receive FIFO or DMA Start of Frame Overruns Register
02C8 0288	RXMOFOVERRUNS	Receive FIFO or DMA Middle of Frame Overruns Register
02C8 028C	RXDMAOVERRUNS	Receive DMA Start of Frame and Middle of Frame Overruns Register
02C8 0290 - 02C8 02FC	-	Reserved

Table 7-103. EMAC1 Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 0000	TXIDVER	Transmit Identification and Version Register
02CC 0004	TXCONTROL	Transmit Control Register
02CC 0008	TXTEARDOWN	Transmit Teardown Register
02CC 000F	-	Reserved
02CC 0010	RXIDVER	Receive Identification and Version Register
02CC 0014	RXCONTROL	Receive Control Register
02CC 0018	RXTEARDOWN	Receive Teardown Register
02CC 001C	-	Reserved
02CC 0020 - 02CC 007C	-	Reserved
02CC 0080	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
02CC 0084	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
02CC 0088	TXINTMASKSET	Transmit Interrupt Mask Set Register
02CC 008C	TXINTMASKCLEAR	Transmit Interrupt Mask Clear Register
02CC 0090	MACINVECTOR	MAC Input Vector Register
02CC 0094	MACEOIVECTOR	MAC End-of-Interrupt Vector Register
02CC 0098 - 02CC 009C	-	Reserved
02CC 00A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
02CC 00A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
02CC 00A8	RXINTMASKSET	Receive Interrupt Mask Set Register
02CC 00AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
02CC 00B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register

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Table 7-103. EMAC1 Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 00B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
02CC 00B8	MACINTMASKSET	MAC Interrupt Mask Set Register
02CC 00BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
02CC 00C0 - 02CC 00FC	-	Reserved
02CC 0100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
02CC 0104	RXUNICASTSET	Receive Unicast Enable Set Register
02CC 0108	RXUNICASTCLEAR	Receive Unicast Clear Register
02CC 010C	RXMAXLEN	Receive Maximum Length Register
02CC 0110	RXBUFFEROFFSET	Receive Buffer Offset Register
02CC 0114	RXFILTERLOWTHRESH	Receive Filter Low Priority Frame Threshold Register
02CC 0118 - 02CC 011C	-	Reserved
02CC 0120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
02CC 0124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
02CC 0128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
02CC 012C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
02CC 0130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
02CC 0134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
02CC 0138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
02CC 013C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register
02CC 0140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
02CC 0144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
02CC 0148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
02CC 014C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
02CC 0150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register
02CC 0154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
02CC 0158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register
02CC 015C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
02CC 0160	MACCONTROL	MAC Control Register
02CC 0164	MACSTATUS	MAC Status Register
02CC 0168	EMCONTROL	Emulation Control Register
02CC 016C	FIFOCONTROL	FIFO Control Register (Transmit and Receive)
02CC 0170	MACCONFIG	MAC Configuration Register
02CC 0174	SOFTRESET	Soft Reset Register
02CC 0178 - 02CC 01CC	-	Reserved
02CC 01D0	MACSRCADDRLO	MAC Source Address Low Bytes Register (Lower 16-bits)
02CC 01D4	MACSRCADDRHI	MAC Source Address High Bytes Register (Upper 16-bits)
02CC 01D8	MACHASH1	MAC Hash Address Register 1
02CC 01DC	MACHASH2	MAC Hash Address Register 2
02CC 01E0	BOFFTEST	Back Off Test Register
02CC 01E4	TPACETEST	Transmit Pacing Algorithm Test Register
02CC 01E8	RXPAUSE	Receive Pause Timer Register
02CC 01EC	TXPAUSE	Transmit Pause Timer Register
02CC 01F0 - 02CC 01FC	-	Reserved
02CC 0200 - 02CC 02FC	(see Table 7-102)	EMAC Statistics Registers
02CC 0300 - 02CC 04FC	-	Reserved
02CC 0500	MACADDRLO	MAC Address Low Bytes Register (Used in Receive Address Matching)

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Table 7-103. EMAC1 Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 0504	MACADDRHI	MAC Address High Bytes Register (Used in Receive Address Matching)
02CC 0508	MACINDEX	MAC Index Register
02CC 050C - 02CC 05FC	-	Reserved
02CC 0600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
02CC 0604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
02CC 0608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
02CC 060C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
02CC 0610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
02CC 0614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
02CC 0618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
02CC 061C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register
02CC 0620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
02CC 0624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
02CC 0628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register
02CC 062C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
02CC 0630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
02CC 0634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
02CC 0638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
02CC 063C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
02CC 0640	TX0CP	Transmit Channel 0 Completion Pointer (Interrupt Acknowledge) Register
02CC 0644	TX1CP	Transmit Channel 1 Completion Pointer (Interrupt Acknowledge) Register
02CC 0648	TX2CP	Transmit Channel 2 Completion Pointer (Interrupt Acknowledge) Register
02CC 064C	TX3CP	Transmit Channel 3 Completion Pointer (Interrupt Acknowledge) Register
02CC 0650	TX4CP	Transmit Channel 4 Completion Pointer (Interrupt Acknowledge) Register
02CC 0654	TX5CP	Transmit Channel 5 Completion Pointer (Interrupt Acknowledge) Register
02CC 0658	TX6CP	Transmit Channel 6 Completion Pointer (Interrupt Acknowledge) Register
02CC 065C	TX7CP	Transmit Channel 7 Completion Pointer (Interrupt Acknowledge) Register
02CC 0660	RX0CP	Receive Channel 0 Completion Pointer (Interrupt Acknowledge) Register
02CC 0664	RX1CP	Receive Channel 1 Completion Pointer (Interrupt Acknowledge) Register
02CC 0668	RX2CP	Receive Channel 2 Completion Pointer (Interrupt Acknowledge) Register
02CC 066C	RX3CP	Receive Channel 3 Completion Pointer (Interrupt Acknowledge) Register
02CC 0670	RX4CP	Receive Channel 4 Completion Pointer (Interrupt Acknowledge) Register
02CC 0674	RX5CP	Receive Channel 5 Completion Pointer (Interrupt Acknowledge) Register
02CC 0678	RX6CP	Receive Channel 6 Completion Pointer (Interrupt Acknowledge) Register
02CC 067C	RX7CP	Receive Channel 7 Completion Pointer (Interrupt Acknowledge) Register
02CC 0680 - 02CC 0FFC	-	Reserved

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Table 7-104. EMAC1 Statistics Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 0200	RXGOODFRAMES	Good Receive Frames Register
02CC 0204	RXBCASTFRAMES	Broadcast Receive Frames Register (Total number of good broadcast frames received)
02CC 0208	RXMCASTFRAMES	Multicast Receive Frames Register (Total number of good multicast frames received)
02CC 020C	RXPAUSEFRAMES	Pause Receive Frames Register
02CC 0210	RXCRCERRORS	Receive CRC Errors Register (Total number of frames received with CRC errors)
02CC 0214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors)
02CC 0218	RXOVERSIZED	Receive Oversized Frames Register (Total number of oversized frames received)
02CC 021C	RXJABBER	Receive Jabber Frames Register (Total number of jabber frames received)
02CC 0220	RXUNDERSIZED	Receive Undersized Frames Register (Total number of undersized frames received)
02CC 0224	RXFRAGMENTS	Receive Frame Fragments Register
02CC 0228	RXFILTERED	Filtered Receive Frames Register
02CC 022C	RXQOSFILTERED	Received QOS Filtered Frames Register
02CC 0230	RXOCTETS	Receive Octet Frames Register (Total number of received bytes in good frames)
02CC 0234	TXGOODFRAMES	Good Transmit Frames Register (Total number of good frames transmitted)
02CC 0238	TXBCASTFRAMES	Broadcast Transmit Frames Register
02CC 023C	TXMCASTFRAMES	Multicast Transmit Frames Register
02CC 0240	TXPAUSEFRAMES	Pause Transmit Frames Register
02CC 0244	TXDEFERRED	Deferred Transmit Frames Register
02CC 0248	TXCOLLISION	Transmit Collision Frames Register
02CC 024C	TXSINGLECOLL	Transmit Single Collision Frames Register
02CC 0250	TXMULTICOLL	Transmit Multiple Collision Frames Register
02CC 0254	TXEXCESSIVECOLL	Transmit Excessive Collision Frames Register
02CC 0258	TXLATECOLL	Transmit Late Collision Frames Register
02CC 025C	TXUNDERRUN	Transmit Underrun Error Register
02CC 0260	TXCARRIERSENSE	Transmit Carrier Sense Errors Register
02CC 0264	TXOCTETS	Transmit Octet Frames Register
02CC 0268	FRAME64	Transmit and Receive 64 Octet Frames Register
02CC 026C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
02CC 0270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
02CC 0274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
02CC 0278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
02CC 027C	FRAME1024TUP	Transmit and Receive 1024 to 1518 Octet Frames Register
02CC 0280	NETOCTETS	Network Octet Frames Register
02CC 0284	RXSOFOVERRUNS	Receive FIFO or DMA Start of Frame Overruns Register
02CC 0288	RXMOFOVERRUNS	Receive FIFO or DMA Middle of Frame Overruns Register
02CC 028C	RXDMAOVERRUNS	Receive DMA Start of Frame and Middle of Frame Overruns Register
02CC 0290 - 02CC 02FC	-	Reserved

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7.15.3 EMIC Peripheral Register Descriptions

Table 7-105. EMIC0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 1000	PID	Peripheral ID Register
02C8 1004	PSCFG	Prescalar Config Register
02C8 1008 - 02C8 101F	-	Reserved
02C8 1020	EW_INTCTL0 - EW_INTCTL5	EMAC Interrupt Control Register(1)
02C8 1038 - 02C8 10FC	-	Reserved
02C8 1100	RPCFG0 - RPCFG7	Receive Pacer Configuration Register(2)
02C8 1120	RPSTAT0 - RPSTAT7	Receive Pacer Statistics Register(2)
02C8 1140	TPCFG0 - TPCFG7	Transmit Pacer Configuration Register(3)
02C8 1160	TPSTAT0 - TPSTAT7	Transmit Pacer Statistics Register(3)

(1) 6 registers; one register per core.
(2) 8 registers; one register per receive event.
(3) 8 registers; one register per transmit event.

Table 7-106. EMIC1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 1000	PID	Peripheral ID Register
02CC 1004	PSCFG	Prescalar Config Register
02CC 1008 - 02CC 101F	-	Reserved
02CC 1020	EW_INTCTL0 - EW_INTCTL5	EMAC Interrupt Control Register(1)
02CC 1038 - 02CC 10FC	-	Reserved
02CC 1100	RPCFG0 - RPCFG7	Receive Pacer Configuration Register(2)
02CC 1120	RPSTAT0 - RPSTAT7	Receive Pacer Statistics Register(2)
02CC 1140	TPCFG0 - TPCFG7	Transmit Pacer Configuration Register(3)
02CC 1160	TPSTAT0 - TPSTAT7	Transmit Pacer Statistics Register(3)

(1) 6 registers; one register per core.
(2) 8 registers; one register per receive event.
(3) 8 registers; one register per transmit event.

Table 7-107. EMAC0 CPPI RAM

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 2000 - 02C8 3FFF	-	CPPI RAM (EMAC0 Buffer Descriptor Memory)

Table 7-108. EMAC1 CPPI RAM

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02CC 2000 - 02CC 3FFF	-	CPPI RAM (EMAC1 Buffer Descriptor Memory)

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7.15.4 EMAC Electrical Data/Timing (MII, GMII, RMII, RGMII, and SSMII)

7.15.4.1 EMAC MII and GMII Electrical Data/Timing

Table 7-109. Timing Requirements for MRCLK - MII and GMII Operation

(see Figure 7-48)

NO.			500/625/700						UNIT
			1000 Mbps		100 Mbps		10 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(MRCLK)}$	Cycle time, MRCLK	8		40		400		ns
2	$t_{w(MRCLKH)}$	Pulse duration, MRCLK high	2.8		14		140		ns
3	$t_{w(MRCLKL)}$	Pulse duration, MRCLK low	2.8		14		140		ns
4	$t_{t(MRCLK)}$	Transition time, MRCLK		1		3		3	ns

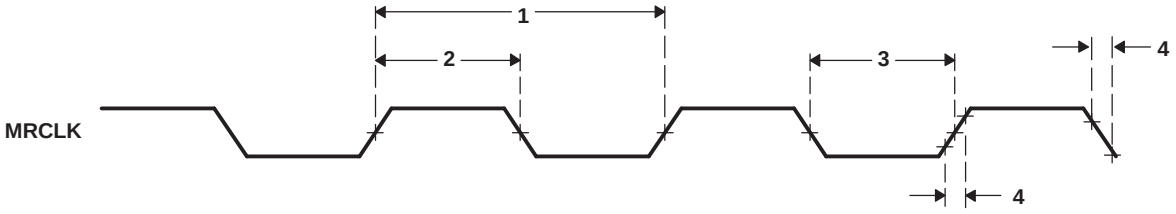

Figure 7-48. MRCLK Timing

Table 7-110. Switching Characteristics Over Recommended Operating Conditions for MTCLK - MII Operation

(see Figure 7-49)

NO.			500/625/700				UNIT
			100 Mbps		10 Mbps		
			MIN	MAX	MIN	MAX	
1	$t_{c(MTCLK)}$	Cycle time, MTCLK	40		400		ns
2	$t_{w(MTCLKH)}$	Pulse duration, MTCLK high	14		140		ns
3	$t_{w(MTCLKL)}$	Pulse duration, MTCLK low	14		140		ns
4	$t_{t(MTCLK)}$	Transition time, MTCLK		3		3	ns

Table 7-111. Switching Characteristics Over Recommended Operating Conditions for GMTCLK - GMII Operation

(see Figure 7-49)

NO.			500/625/700		UNIT
			1000 Mbps		
			MIN	MAX	
1	$t_{c(GMTCLK)}$	Cycle time, GMTCLK	8		ns
2	$t_{w(GMTCLKH)}$	Pulse duration, GMTCLK high	2.8		ns
3	$t_{w(GMTCLKL)}$	Pulse duration, GMTCLK low	2.8		ns
4	$t_{t(GMTCLK)}$	Transition time, GMTCLK		1	ns

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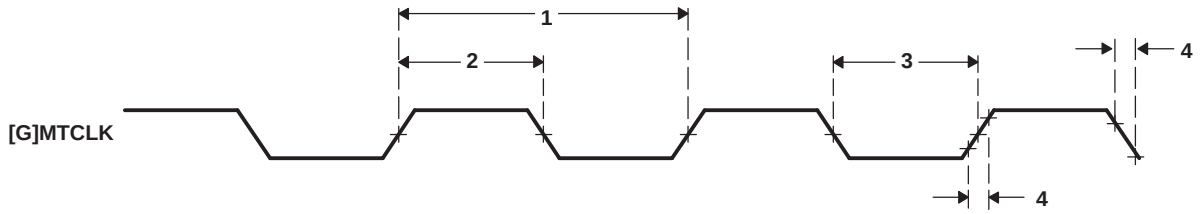

Figure 7-49. [G]MTCLK Timing

Table 7-112. Timing Requirements for EMAC MII and GMII Receive 10/100 Mbit/s

(see Figure 7-50)

NO.	PARAMETER		500/625/700 10/100 Mbps MIN	500/625/700 10/100 Mbps MAX	UNIT
1	$t_{su(GMII\_MRXD)}$	Setup time, GMII_MRXD to GMII_MRCLK rising edge	8		ns
	$t_{su(GMII\_MRXDV)}$	Setup time, GMII_MRXDV to GMII_MRCLK rising edge	8		
	$t_{su(GMII\_MRXER)}$	Setup time, GMII_MRXER to GMII_MRCLK rising edge	8		
2	$t_{h(GMII\_MRXD)}$	Hold time, GMII_MRXD valid after GMII_RCLK rising edge	8		ns
	$t_{h(GMII\_MRXDV)}$	Hold time, GMII_MRXDV valid after GMII_RCLK rising edge	8		
	$t_{h(GMII\_MRXER)}$	Hold time, GMII_MRXDV valid after GMII_RCLK rising edge	8		

Table 7-113. Timing Requirements for EMAC MII and GMII Receive 1000 Mbit/s

(see Figure 7-50)

NO.	PARAMETER		500/625/700 1000 Mbps MIN	500/625/700 1000 Mbps MAX	UNIT
1	$t_{su(GMII\_G\_MRXD)}$	Setup time, GMII_MRXD to GMII_MRCLK rising edge	2.5		ns
	$t_{su(GMII\_G\_MRXDV)}$	Setup time, GMII_MRXDV to GMII_MRCLK rising edge	2.5		
	$t_{su(GMII\_G\_MRXER)}$	Setup time, GMII_MRXER to GMII_MRCLK rising edge	2.5		
2	$t_{h(GMII\_G\_MRXD)}$	Hold time, GMII_MRXD valid after GMII_RCLK rising edge	0.2		ns
	$t_{h(GMII\_G\_MRXDV)}$	Hold time, GMII_MRXDV valid after GMII_RCLK rising edge	0.2		
	$t_{h(GMII\_G\_MRXER)}$	Hold time, GMII_MRXDV valid after GMII_RCLK rising edge	0.2		

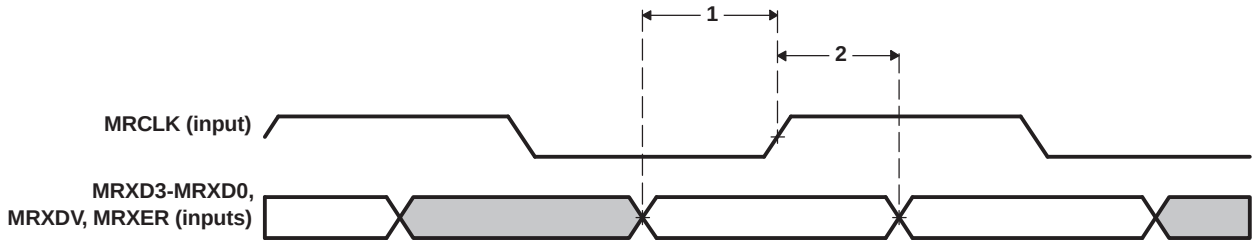

Figure 7-50. Input Timing

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Table 7-114. Switching Characteristics Over Recommended Operating Conditions for EMAC MII and GMII Transmit 10/100 Mbit/s

(see Figure 7-51)

NO.	PARAMETER		500/625/700 10/100 Mbps MIN	500/625/700 10/100 Mbps MAX	UNIT
1	$t_{d(GMII\_MTXD)}$	Delay time, GMII_MTCLK rising edge to GMII_MTXD	5	25	ns
	$t_{d(GMII\_MTXEN)}$	Delay time, GMII_MTCLK rising edge to GMII_MTXEN	5	25	

Table 7-115. Switching Characteristics Over Recommended Operating Conditions for EMAC MII and GMII Transmit 1000 Mbit/s

(see Figure 7-51)

NO.	PARAMETER		500/625/700 1000 Mbps MIN	500/625/700 1000 Mbps MAX	UNIT
1	$t_{s(GMII\_G\_MTXD)}$	Delay time, GMII_GMTCLK rising edge to GMII_MTXD	0.5	5	ns
	$t_{d(GMII\_G\_MTXEN)}$	Delay time, GMII_GMTCLK rising edge to GMII_MTXEN	0.5	5	

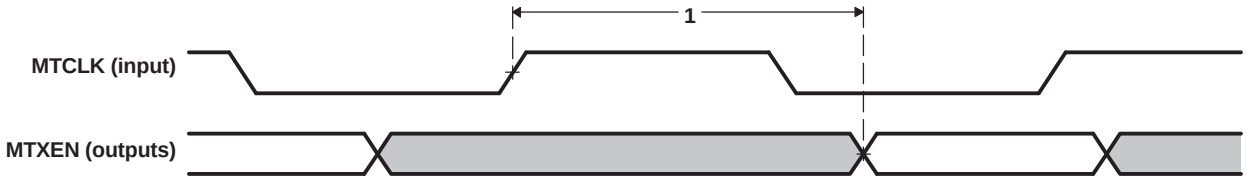

Figure 7-51. Output Timing

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7.15.4.2 EMAC RMII Electrical Data/Timing

The RMREFCLK pin is used to source a clock to the EMAC when it is configured for RMII operation. The RMREFCLK frequency should be 50 MHz ±50 PPM with a duty cycle between 35% and 65%, inclusive.

Table 7-116. Timing Requirements for RMREFCLK - RMII Operation

(see Figure 7-52)

NO.	PARAMETER		500/625/700			UNIT
			MIN	TYP	MAX	
1	$t_{c(RFCK)}$	Cycle time, REFCLK		20		ns
2	$t_{w(RFCKH)}$	Pulse duration, REFCLK high	7		13	ns
3	$t_{w(RFCKL)}$	Pulse duration, REFCLK low	7		13	ns
4	$t_{t(RFCK)}$	Transition time, REFCLK			2	ns

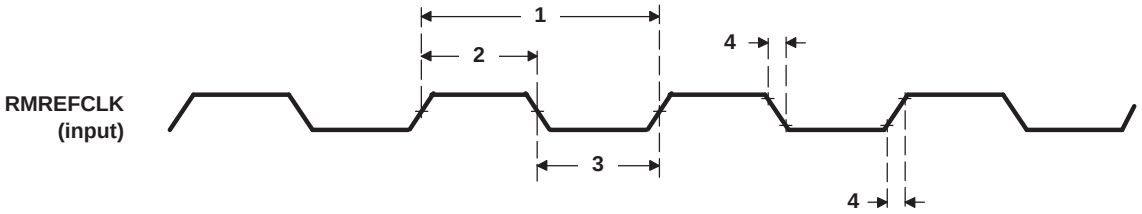

Figure 7-52. RMII Reference Clock (Input)

Table 7-117. Timing Requirements for EMAC RMII Receive

PARAMETER		500/625/700		UNIT
		MIN	MAX	
$t_{su(RXD-RFCK)}$	Setup time, RXD to REFCLK rising edge	4		ns
$t_{su(CDV-RFCK)}$	Setup time, CRSDV to REFCLK rising edge	4		ns
$t_{su(RXER-RFCK)}$	Setup time, RXER to REFCLK rising edge	4		ns
$t_{h(RFCK-RXD)}$	Hold time, RXD valid after REFCLK rising edge	2		ns
$t_{h(RFCK-CDV)}$	Hold time, CRSDV valid after REFCLK rising edge	2		ns
$t_{h(RFCK-RXER)}$	Hold time, RXER valid after REFCLK rising edge	2		ns

Table 7-118. Timing Requirements for EMAC RMII Transmit

PARAMETER		500/625/700		UNIT
		MIN	MAX	
$t_{d(RFCK-TXDV)}$	Delay time, REFCLK rising edge to TXD	2.5	13	ns
$t_{d(RFCK-TXENV)}$	Delay time, REFCLK rising edge to TXENV	2.5	13	ns

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7.15.4.3 EMAC RGMII Electrical Data/Timing

An extra clock signal, RGREFCLK, running at 125 MHz is included as a convenience to the user. Note that this reference clock is ***not*** a free-running clock. This should only be used by an external device if it does not expect a valid clock during device reset.

Table 7-119. Switching Characteristics Over Recommended Operating Conditions for EMAC RGREFCLK - RGMII Operation

(see Figure 7-53)

NO.	PARAMETER		500/625/700			UNIT
			MIN	TYP	MAX	
1	$t_{c(RGFCLK)}$	Cycle time, RGREFCLK		8		ns
2	$t_{w(RGFCLKH)}$	Pulse duration, RGREFCLK high	0.45 * $t_{c(RGFCLK)}$		0.55 * $t_{c(RGFCLK)}$	ns
3	$t_{w(RGFCLKL)}$	Pulse duration, RGREFCLK low	0.45 * $t_{c(RGFCLK)}$		0.55 * $t_{c(RGFCLK)}$	ns
4	$t_{t(RGFCLK)}$	Transition time, RGREFCLK			0.5	ns

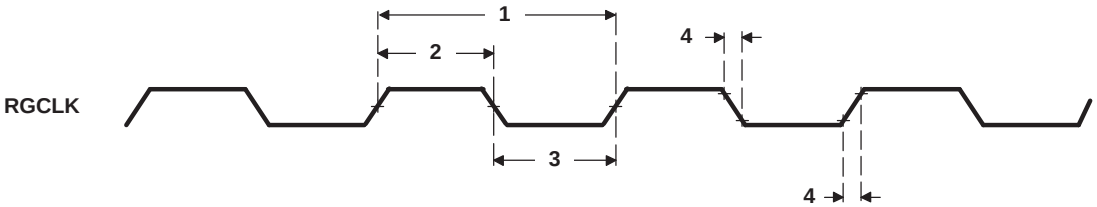

Figure 7-53. RGMII Reference Clock (Output)

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Table 7-120. Switching Characteristics Over Recommended Operating Conditions for EMAC RGMII Output Operation 10/100/1000 Mbit/s

(see Figure 7-54)

NO.	PARAMETER		SPEED	500/625/700		UNIT
				MIN	MAX	
1	$t_{c(RGTXC)}$	Cycle time, RGTXC	10 Mbps	360	440	ns
			100 Mbps	36	44	
			1000 Mbps	7.2	8.8	
2	$t_{w(RGTXCH)}$	Pulse duration, RGTXC high	10/100 Mbps	0.40*$t_{c(RGTXC)}$	0.60*$t_{c(RGTXC)}$	ns
			1000 Mbps	0.45*$t_{c(RGTXC)}$	0.55*$t_{c(RGTXC)}$	
3	$t_{w(RGTXCL)}$	Pulse duration, RGTXC low	10/100 Mbps	0.40*$t_{c(RGTXC)}$	0.60*$t_{c(RGTXC)}$	ns
			1000 Mbps	0.45*$t_{c(RGTXC)}$	0.55*$t_{c(RGTXC)}$	
4	$t_{t(RGTXC)}$	Transition time, RGTXC	10/100/1000 Mbps		0.75	ns
6	$t_{su(RGTDV-RGTXC)}$	Setup time, transmit selected signals (RGTD[3:0] and RGTXCTL) valid before RGTXC high/low	10/100/1000 Mbps	1.2		ns
7	$t_{h(RGTXC-RGTDV)}$	Hold time, transmit selected signals (RGTD[3:0] and RGTXCTL) valid after RGTXC high/low	10/100/1000 Mbps	1.2		ns

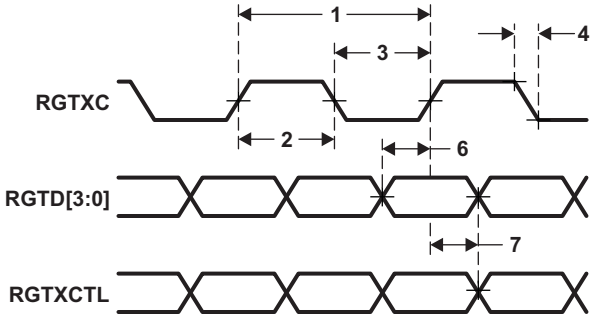

Figure 7-54. RGMII Output Timing

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Table 7-121. Timing Requirements for EMAC RGMII Input Operation 10/100/1000 Mbit/s

(see Figure 7-55)

NO.	PARAMETER		SPEED	500/625/700		UNIT
				MIN	MAX	
8	$t_{c(RGRXC)}$	Cycle time, RGRXC	10 Mbps	360	440	ns
			100 Mbps	36	44	
			1000 Mbps	7.2	8.8	
9	$t_{w(RGRXCH)}$	Pulse duration, RGRXC high	10/100 Mbps	0.40*$t_{c(RGRXC)}$	0.60*$t_{c(RGRXC)}$	ns
			1000 Mbps	0.45*$t_{c(RGRXC)}$	0.55*$t_{c(RGRXC)}$	
10	$t_{w(RGRXCL)}$	Pulse duration, RGRXC low	10/100 Mbps	0.40*$t_{c(RGRXC)}$	0.60*$t_{c(RGRXC)}$	ns
			1000 Mbps	0.45*$t_{c(RGRXC)}$	0.55*tc(RGRXC)	
11	$t_{t(RGRXC)}$	Transition time, RGRXC	10/100/1000 Mbps		0.75	ns
12	$t_{su(RGRDV-RGRXC)}$	Setup time, transmit selected signals (RGRD[3:0] and RGRXCTL) valid before RGRXC high/low	10/100/1000 Mbps	1.2		ns
13	$t_{h(RGRXC-RGRDV)}$	Hold time, transmit selected signals (RGRD[3:0] and RGRXCTL) valid after RGRXC high/low	10/100/1000 Mbps	1.2		ns

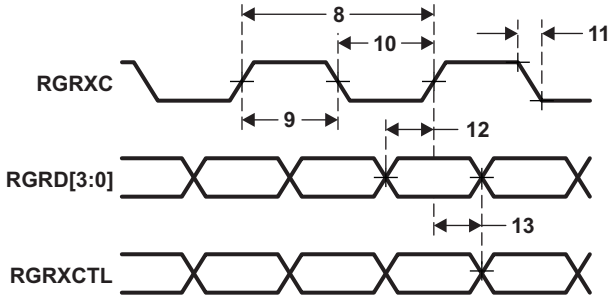

Figure 7-55. RGMII Input Timing

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7.15.4.4 EMAC SSMII Electrical Data/Timing

Table 7-122. Timing Requirements for EMAC SSMII Transmit

(see Figure 7-56)

NO.	PARAMETER		500/625/700			UNIT
			MIN	TYP	MAX	
1	$t_{c(TX\_CLK)}$	Cycle time, TX_CLK		8		ns
2	$t_{d(TX\_CLK-TX\_SYNC)}$	Delay time, TX_CLK high to TX_SYNC output valid	0.5		4.5	ns
3	$t_{d(TX\_CLK-TX\_DATA)}$	Delay time, TX_CLK high to TX_DATA output valid	0.5		4.5	ns

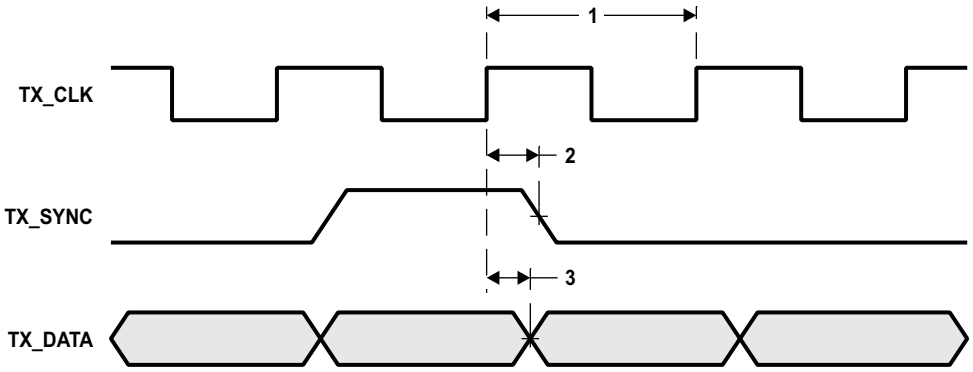

Figure 7-56. SSMII Transmit Timing

Table 7-123. Timing Requirements for EMAC SSMII Receive

(see Figure 7-57)

NO.	PARAMETER		500/625/700			UNIT
			MIN	TYP	MAX	
1	$t_{c(TR\_CLK)}$	Cycle time, TR_CLK		8		ns
2	$t_{su(RX\_SYNC)}$	Setup time, RX_SYNC setup time	1.5			ns
3	$t_{h(RX\_SYNC)}$	Hold time, RX_SYNC hold time	1			ns
4	$t_{su(RX\_DATA)}$	Setup time, RX_DATA setup time	1.5			ns
5	$t_{h(RX\_DATA)}$	Hold time, RX_DATA hold time	1			ns

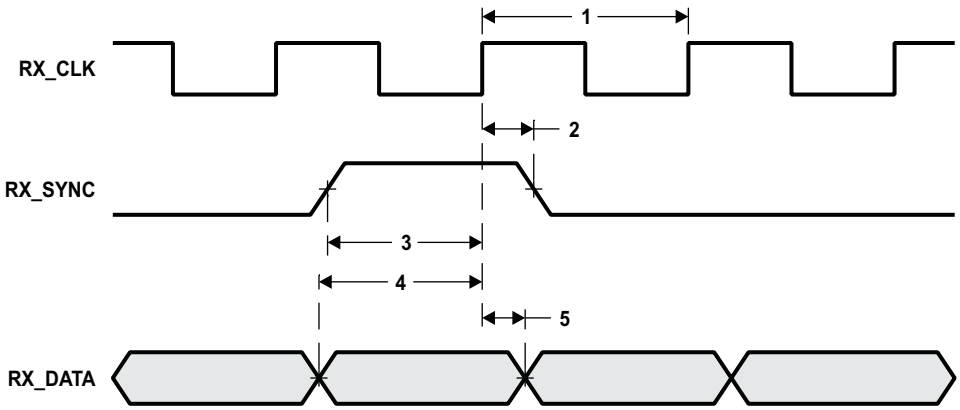

Figure 7-57. SSMII Receive Timing

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7.15.5 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and controls up to 32 Ethernet PHY(s) connected to the device, using a shared two-wire bus. Application software uses the MDIO module to configure the negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor.

The EMAC control module is the main interface between the device core processor, the MDIO module, and the EMAC module. The relationship between these three components is shown in Figure 7-47.

The MDIO uses the same pins for the MII, GMII, S3MII, and RMII modes. Standalone pins are included for the RGMII mode due to specific voltage requirements. Only one mode can be used at a time. The mode used is selected at device reset based on the MACSEL0[2:0] configuration pins (for more detailed information, see Section 3, *Device Configuration* section of this document).

For more detailed information on the EMAC/MDIO, see the *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (literature number SPRUEF8).

7.15.5.1 MDIO Device-Specific Information

Clocking Information

The on-chip PLL2 and PLL2 Controller generate all the clocks to the MDIO module. When enabled, the input clock to the PLL2 Controller (CLKIN2) must have a 25-MHz frequency. For more information, see Section 7.9, *PLL2 and PLL2 Controller* of this document.

7.15.5.2 MDIO Peripheral Register Descriptions

Table 7-124. MDIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 1800	VERSION	MDIO Version Register
02C8 1804	CONTROL	MDIO Control Register
02C8 1808	ALIVE	MDIO PHY Alive Status Register
02C8 180C	LINK	MDIO PHY Link Status Register
02C8 1810	LINKINTRAW	MDIO Link Status Change Interrupt (Unmasked) Register
02C8 1814	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register
02C8 1818 - 02C8 181C	-	Reserved
02C8 1820	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register
02C8 1824	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register
02C8 1828	USERINTMASKSET	MDIO User Command Complete Interrupt Mask Set Register
02C8 182C	USERINTMASKCLEAR	MDIO User Command Complete Interrupt Mask Clear Register
02C8 1830 - 02C8 187C	-	Reserved
02C8 1880	USERACCESS0	MDIO User Access Register 0
02C8 1884	USERPHYSEL0	MDIO User PHY Select Register 0
02C8 1888	USERACCESS1	MDIO User Access Register 1
02C8 188C	USERPHYSEL1	MDIO User PHY Select Register 1
02C8 1890 - 02C8 1FFC	-	Reserved

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7.15.5.3 MDIO Electrical Data/Timing

Table 7-125. Timing Requirements for MDIO Input

(see Figure 7-58)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{c(MDCLK)}$	Cycle time, MDCLK	400		ns
2	$t_{w(MDCLKH)}$	Pulse duration, MDCLK high	180		ns
	$t_{w(MDCLKL)}$	Pulse duration, MDCLK low	180		ns
3	$t_{t(MDCLK)}$	Transition time, MDCLK		5	ns
4	$t_{su(MDIO-MDCLKH)}$	Setup time, MDIO data input valid before MDCLK high	25		ns
5	$t_{h(MDCLKH-MDIO)}$	Hold time, MDIO data input valid after MDCLK high	10		ns

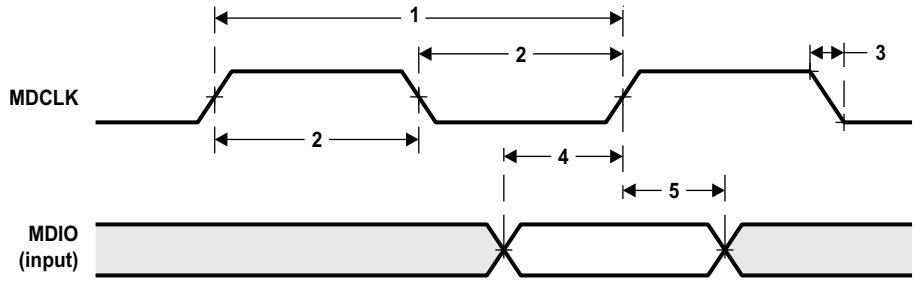

Figure 7-58. MDIO Input Timing

Table 7-126. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

(see Figure 7-59)

NO.	PARAMETER		500/625/700		UNIT
			MIN	MAX	
7	$t_{d(MDCLKL-MDIO)}$	Delay time, MDCLK low to MDIO data output valid		100	ns

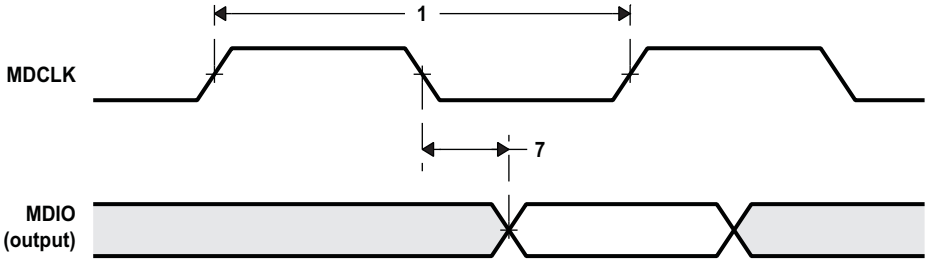

Figure 7-59. MDIO Output Timing

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7.16 Timers

The timers can be used to: time events, count events, generate pulses, interrupt the CPU, and send synchronization events to the EDMA. The localized timers (Timer 0 - Timer 5) can also be used as watchdog timers.

7.16.1 Timer Device-Specific Information

The C6472 device has six localized timers (Timer 0 - Timer 5) and six shared timers (Timer 6 - Timer 11). Each of the localized timers can be configured as a general-purpose timer or a watchdog timer. Each of the shared timers is a general-purpose timer. When configured as a general-purpose timer, each timer can be programmed as a 64-bit timer or as two separate 32-bit timers. The localized timers are clocked with an internal clock with a CPU/6 frequency. The shared timers can also be clocked with the same internal clock frequency or with an external signal provided on TIMI0 or TIMI1.

Each timer is made up of two 32-bit counters: a high counter and a low counter. The TIMI0 pin is connected to the low counter of each of the shared timers and the TIMI1 pin is connected to the high counter of each of the shared timers. The output of one of the shared timers, either the high counter or the low counter, can be selected to be output on the timer output pin (TIMO2).

When Timer 0 - Timer 5 are configured as watchdog timers, each core should maintain its own watchdog. Each core should also configure the corresponding RSTMUX0-5 register (see Section 3.8.2) to define the action that will be taken if a watchdog timeout occurs. In addition to the internally defined actions, a watchdog timeout results in the assertion of the WDOUT pin. WDOUT is a logically-combined signal from the six individual watchdog timers. A host can determine which of the six cores experienced the watchdog timeout by reading the RSTMUX registers or having the contents of those registers reported by one of the cores.

7.16.2 Timer Peripheral Register Descriptions

Table 7-127. Timer 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
025E 0000	-	Reserved
025E 0004	EMUMGT_CLKSPD0	Timer 0 Emulation Management/Clock Speed Register
025E 0008	-	Reserved
025E 000C	-	Reserved
025E 0010	CNTLO0	Timer 0 Counter Register Low
025E 0014	CNTHI0	Timer 0 Counter Register High
025E 0018	PRDLO0	Timer 0 Period Register Low
025E 001C	PRDHI0	Timer 0 Period Register High
025E 0020	TCR0	Timer 0 Control Register
025E 0024	TGCR0	Timer 0 Global Control Register
025E 0028	WDTCR0	Timer 0 Watchdog Timer Control Register
025E 002C - 025E FFFC	-	Reserved

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Table 7-128. Timer 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
025F 0000	-	Reserved
025F 0004	EMUMGT_CLKSPD1	Timer 1 Emulation Management/Clock Speed Register
025F 0008	-	Reserved
025F 000C	-	Reserved
025F 0010	CNTLO1	Timer 1 Counter Register Low
025F 0014	CNTHI1	Timer 1 Counter Register High
025F 0018	PRDLO1	Timer 1 Period Register Low
025F 001C	PRDHI1	Timer 1 Period Register High
025F 0020	TCR1	Timer 1 Control Register
025F 0024	TGCR1	Timer 1 Global Control Register
025F 0028	WDTCR1	Timer 1 Watchdog Timer Control Register
025F 002C - 025F FFFC	-	Reserved

Table 7-129. Timer 2 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0260 0000	-	Reserved
0260 0004	EMUMGT_CLKSPD2	Timer 2 Emulation Management/Clock Speed Register
0260 0008	-	Reserved
0260 000C	-	Reserved
0260 0010	CNTLO2	Timer 2 Counter Register Low
0260 0014	CNTHI2	Timer 2 Counter Register High
0260 0018	PRDLO2	Timer 2 Period Register Low
0260 001C	PRDHI2	Timer 2 Period Register High
0260 0020	TCR2	Timer 2 Control Register
0260 0024	TGCR2	Timer 2 Global Control Register
0260 0028	WDTCR2	Timer 2 Watchdog Timer Control Register
0260 002C - 0260 FFFC	-	Reserved

Table 7-130. Timer 3 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0261 0000	-	Reserved
0261 0004	EMUMGT_CLKSPD3	Timer 3 Emulation Management/Clock Speed Register
0261 0008	-	Reserved
0261 000C	-	Reserved
0261 0010	CNTLO3	Timer 3 Counter Register Low
0261 0014	CNTHI3	Timer 3 Counter Register High
0261 0018	PRDLO3	Timer 3 Period Register Low
0261 001C	PRDHI3	Timer 3 Period Register High
0261 0020	TCR3	Timer 3 Control Register
0261 0024	TGCR3	Timer 3 Global Control Register
0261 0028	WDTCR3	Timer 3 Watchdog Timer Control Register
0261 002C - 0261 FFFC	-	Reserved

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Table 7-131. Timer 4 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0262 0000	-	Reserved
0262 0004	EMUMGT_CLKSPD4	Timer 4 Emulation Management/Clock Speed Register
0262 0008	-	Reserved
0262 000C	-	Reserved
0262 0010	CNTLO4	Timer 4 Counter Register Low
0262 0014	CNTHI4	Timer 4 Counter Register High
0262 0018	PRDLO4	Timer 4 Period Register Low
0262 001C	PRDHI4	Timer 4 Period Register High
0262 0020	TCR4	Timer 4 Control Register
0262 0024	TGCR4	Timer 4 Global Control Register
0262 0028	WDTCR4	Timer 4 Watchdog Timer Control Register
0262 002C - 0262 FFFC	-	Reserved

Table 7-132. Timer 5 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0263 0000	-	Reserved
0263 0004	EMUMGT_CLKSPD5	Timer 5 Emulation Management/Clock Speed Register
0263 0008	-	Reserved
0263 000C	-	Reserved
0263 0010	CNTLO5	Timer 5 Counter Register Low
0263 0014	CNTHI5	Timer 5 Counter Register High
0263 0018	PRDLO5	Timer 5 Period Register Low
0263 001C	PRDHI5	Timer 5 Period Register High
0263 0020	TCR5	Timer 5 Control Register
0263 0024	TGCR5	Timer 5 Global Control Register
0263 0028	WDTCR5	Timer 5 Watchdog Timer Control Register
0263 002C - 0263 FFFC	-	Reserved

Table 7-133. Timer 6 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0264 0000	-	Reserved
0264 0004	EMUMGT_CLKSPD6	Timer 6 Emulation Management/Clock Speed Register
0264 0008	-	Reserved
0264 000C	-	Reserved
0264 0010	CNTLO6	Timer 6 Counter Register Low
0264 0014	CNTHI6	Timer 6 Counter Register High
0264 0018	PRDLO6	Timer 6 Period Register Low
0264 001C	PRDHI6	Timer 6 Period Register High
0264 0020	TCR6	Timer 6 Control Register
0264 0024	TGCR6	Timer 6 Global Control Register
0264 0028 - 0264 FFFC	-	Reserved

Table 7-134. Timer 7 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0265 0000	-	Reserved
0265 0004	EMUMGT_CLKSPD7	Timer 7 Emulation Management/Clock Speed Register

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Table 7-134. Timer 7 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0265 0008	-	Reserved
0265 000C	-	Reserved
0265 0010	CNTLO7	Timer 7 Counter Register Low
0265 0014	CNTHI7	Timer 7 Counter Register High
0265 0018	PRDLO7	Timer 7 Period Register Low
0265 001C	PRDHI7	Timer 7 Period Register High
0265 0020	TCR7	Timer 7 Control Register
0265 0024	TGCR7	Timer 7 Global Control Register
0265 0028 - 0265 FFFC	-	Reserved

Table 7-135. Timer 8 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0266 0000	-	Reserved
0266 0004	EMUMGT_CLKSPD8	Timer 8 Emulation Management/Clock Speed Register
0266 0008	-	Reserved
0266 000C	-	Reserved
0266 0010	CNTLO8	Timer 8 Counter Register Low
0266 0014	CNTHI8	Timer 8 Counter Register High
0266 0018	PRDLO8	Timer 8 Period Register Low
0266 001C	PRDHI8	Timer 8 Period Register High
0266 0020	TCR8	Timer 8 Control Register
0266 0024	TGCR8	Timer 8 Global Control Register
0266 0028 - 0266 FFFC	-	Reserved

Table 7-136. Timer 9 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0267 0000	-	Reserved
0267 0004	EMUMGT_CLKSPD9	Timer 9 Emulation Management/Clock Speed Register
0267 0008	-	Reserved
0267 000C	-	Reserved
0267 0010	CNTLO9	Timer 9 Counter Register Low
0267 0014	CNTHI9	Timer 9 Counter Register High
0267 0018	PRDLO9	Timer 9 Period Register Low
0267 001C	PRDHI9	Timer 9 Period Register High
0267 0020	TCR9	Timer 9 Control Register
0267 0024	TGCR9	Timer 9 Global Control Register
0267 0028 - 0267 FFFC	-	Reserved

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Table 7-137. Timer 10 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0268 0000	-	Reserved
0268 0004	EMUMGT_CLKSPD10	Timer 10 Emulation Management/Clock Speed Register
0268 0008	-	Reserved
0268 000C	-	Reserved
0268 0010	CNTLO10	Timer 10 Counter Register Low
0268 0014	CNTHI10	Timer 10 Counter Register High
0268 0018	PRDLO10	Timer 10 Period Register Low
0268 001C	PRDHI10	Timer 10 Period Register High
0268 0020	TCR10	Timer 10 Control Register
0268 0024	TGCR10	Timer 10 Global Control Register
0268 0028 - 0268 FFFC	-	Reserved

Table 7-138. Timer 11 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0269 0000	-	Reserved
0269 0004	EMUMGT_CLKSPD11	Timer 11 Emulation Management/Clock Speed Register
0269 0008	-	Reserved
0269 000C	-	Reserved
0269 0010	CNTLO11	Timer 11 Counter Register Low
0269 0014	CNTHI11	Timer 11 Counter Register High
0269 0018	PRDLO11	Timer 11 Period Register Low
0269 001C	PRDHI11	Timer 11 Period Register High
0269 0020	TCR11	Timer 11 Control Register
0269 0024	TGCR11	Timer 11 Global Control Register
0269 0028 - 0269 FFFC	-	Reserved

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7.16.3 Timer Electrical Data/Timing

Table 7-139. Timing Requirements for Timer Input(1)

(see Figure 7-60)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(TIMIxH)}$	Pulse duration, TIMIxH high	12P		ns
2	$t_{w(TIMIxL)}$	Pulse duration, TIMIxL low	12P		ns

(1) P = 1/CPU clock frequency in ns.

Table 7-140. Switching Characteristics Over Recommended Operating Conditions for Timer Output(1)

(see Figure 7-60)

NO.			500/625/700		UNIT
			MIN	MAX	
3	$t_{w(TIMOxH)}$	Pulse duration, TIMOxH high	12P		ns
4	$t_{w(TIMOxL)}$	Pulse duration, TIMOxL low	12P		ns

(1) P = 1/CPU clock frequency in ns.

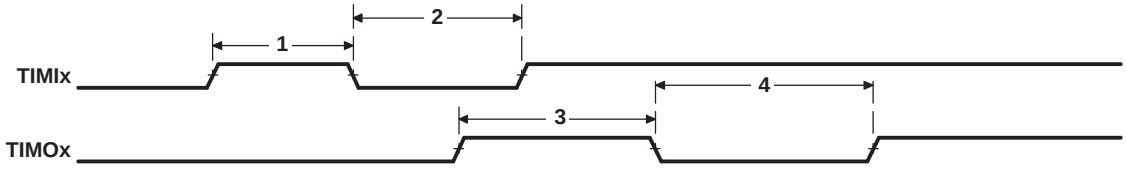

Figure 7-60. Timer Timing

Table 7-141. Switching Characteristics Over Recommended Operating Conditions for Watchdog Timer Output(1)

(see Figure 7-61)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(WDOUTH)}$	Pulse duration, $\overline{\text{WDOUT}}$ high (minimum time between adjacent WDOUT indications)	12P		ns
2	$t_{w(WDOUTL)}$	Pulse duration, $\overline{\text{WDOUT}}$ low (active output pulse)	12P		ns

(1) P = 1/CPU clock frequency in ns.

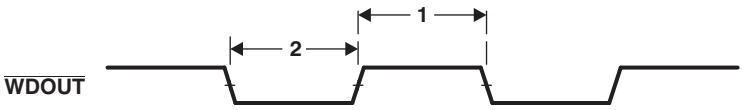

Figure 7-61. $\overline{\text{WDOUT}}$ Timing

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7.17 UTOPIA

7.17.1 UTOPIA Device-Specific Information

The Universal Test and Operations PHY Interface for ATM (UTOPIA) peripheral is a 50 MHz, 8-/16-Bit Slave-only interface. The UTOPIA peripheral contains two, two-cell FIFOs, one for transmit and one for receive, to buffer data sent/received at the interface. There is a transmit and a receive indication to the PDMA to enable servicing.

For more detailed information on the UTOPIA peripheral, see the *TMS320C6472/TMS320TCI6486 DSP Universal Test & Operations PHY Interface for ATM 2 (UTOPIA2) User's Guide* (literature number SPRUEG2).

7.17.2 UTOPIA Peripheral Register Descriptions

Table 7-142. UTOPIA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B4 0000	UCR	UTOPIA Control Register
02B4 0004 - 02B4 0010	-	Reserved
02B4 0014	CDR	Clock Detect Register
02B4 0018	EIER	Error Interrupt Enable Register
02B4 001C	EIPR	Error Interrupt Pending Register
02B4 0020	RRMR0	Receive Routing Unit Mask and Match Register 0
02B4 0024	RRMR1	Receive Routing Unit Mask and Match Register 1
02B4 0028	RRMR2	Receive Routing Unit Mask and Match Register 2
02B4 002C	RRMR3	Receive Routing Unit Mask and Match Register 3
02B4 0030	RRMR4	Receive Routing Unit Mask and Match Register 4
02B4 0034	RRMR5	Receive Routing Unit Mask and Match Register 5
02B4 0038 - 02B4 003C	-	Reserved
02B4 0040	RRSR	Receive Routing Select Register
02B4 0044 - 02B7 00FC	-	Reserved
02B40100	UPIDR	UTOPIA Peripheral ID Register
02B4 0104	UPWREMU	UTOPIA Power Management and Emulation Register
02B4 0108 - 02B7 FFFC	-	Reserved

Table 7-143. PDMA Global Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02BC 0000	PIR	Peripheral Identification Register
02BC 0004	GCSR	Global Control Status Register
02BC 0020	SR0	Statistics Register 0
02BC 0024	SR1	Statistics Register 1
02BC 0028 - 02BC 005C	-	Reserved
02BC 0060	PCR0	Peripheral Control Register 0
02BC 0064	PCR1	Peripheral Control Register 1
02BC 0068 - 02BC 00FC	-	Reserved
02BC 0100 - 02BC 010C	TXC0	TX0 Channel Proxy Registers (see Table 7-144)
02BC 0110 - 02BC 011C	TXC1	TX1 Channel Proxy Registers (see Table 7-144)
02BC 0120 - 02BC 012C	TXC2	TX2 Channel Proxy Registers (see Table 7-144)
02BC 0130 - 02BC 013C	TXC3	TX3 Channel Proxy Registers (see Table 7-144)
02BC 0140 - 02BC 014C	TXC4	TX4 Channel Proxy Registers (see Table 7-144)
02BC 0150 - 02BC 015C	TXC5	TX5 Channel Proxy Registers (see Table 7-144)

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Table 7-143. PDMA Global Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02BC 0180 - 02BC 018C	RXC0	RX0 Channel Proxy Registers (see Table 7-144)
02BC 0190 - 02BC 019C	RXC1	RX1 Channel Proxy Registers (see Table 7-144)
02BC 01A0 - 02BC 01AC	RXC2	RX2 Channel Proxy Registers (see Table 7-144)
02BC 01B0 - 02BC 01BC	RXC3	RX3 Channel Proxy Registers (see Table 7-144)
02BC 01C0 - 02BC 01CC	RXC4	RX4 Channel Proxy Registers (see Table 7-144)
02BC 01D0 - 02BC 01DC	RXC5	RX5 Channel Proxy Registers (see Table 7-144)

Table 7-144. PDMA Channel Proxy Registers

HEX ADDRESS OFFSET	ACRONYM	REGISTER NAME
00h	SAR	PDMA switch address register
04h	PAR	PDMA peripheral address register
08h	BSR	PDMA buffer size register Section
0Ch	TCR	PDMA transfer control register Section

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7.17.3 UTOPIA Electrical Data/Timing

Table 7-145. Timing Requirements for UTOPIA Receive/Transmit Clock (UCLK)(1)

(see Figure 7-62)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{c(UCLK)}$	UXCLK or URCLK cycle time	20		ns
2	$t_{w(UCLKL)}$	UXCLK or URCLK pulse duration low	$0.4t_{c(URCLK)}$	$0.6t_{c(URCLK)}$	ns
3	$t_{w(UCLKH)}$	UXCLK or URCLK pulse duration high	$0.4t_{c(URCLK)}$	$0.6t_{c(URCLK)}$	ns
4	$t_{t(UCLK)}$	Transition time, UXCLK or URCLK (high to low or low to high)		2	ns

(1) UCLK = UXCLK or URCLK.

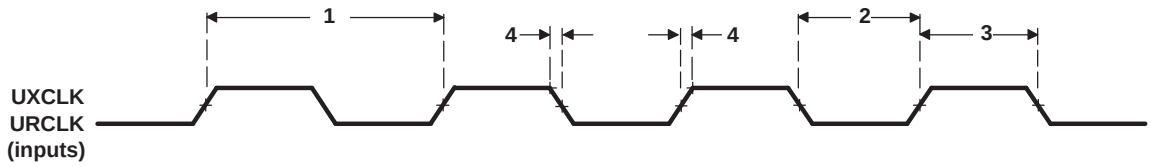

Figure 7-62. UTOPIA Clock

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Table 7-146. Timing Requirements for UTOPIA Slave Receive Cycles

(see Figure 7-63)

NO.			500/625/700		UNIT
			MIN	MAX	
5	$t_{su(URDATA-URCLKH)}$	Setup time, URDATA valid before URCLK high	4		ns
6	$t_{h(URCLKH-URDATA)}$	Hold time, URDATA valid after URCLK high	1		ns
7	$t_{su(URADDR-URCLKH)}$	Setup time, URADDR valid before URCLK high	4		ns
8	$t_{h(URCLKH-URADDR)}$	Hold time, URADDR valid after URCLK high	1		ns
9	$t_{su(URENB-URCLKH)}$	Setup time, $\overline{URENB}$ valid before URCLK high	4		ns
10	$t_{h(URCLKH-URENB)}$	Hold time, $\overline{URENB}$ valid after URCLK high	1		ns
11	$t_{su(URSOC-URCLKH)}$	Setup time, URSOC valid before URCLK high	4		ns
12	$t_{h(URCLKH-URSOC)}$	Hold time, URSOC valid after URCLK high	1		ns

Table 7-147. Switching Characteristics Over Recommended Operating Conditions for UTOPIA Slave Receive Cycles

(see Figure 7-63)

NO.	PARAMETER		500/625/700		UNIT
			MIN	MAX	
13[1]	$t_{d(URCLKH-URCLAV)}$	Delay time, URCLK high to URCLAV valid	2	10	ns
14[1]	$t_{en(URCLKH-URCLAV)}$	Enable time, URCLK high to URCLAV driven	2	10	ns
15[2] [3]	$t_{dis(URCLKL-URCLAVZ)}$	Disable time, URCLK low to URCLAV high-impedance state	2	10	ns

(1) MAX delay time and enable time increases to 12.5 ns at 20 pF and 14 ns at 30 pF, specified by design.
(2) Specifed by design for MIN values.
(3) Specifed by design for MAX values.

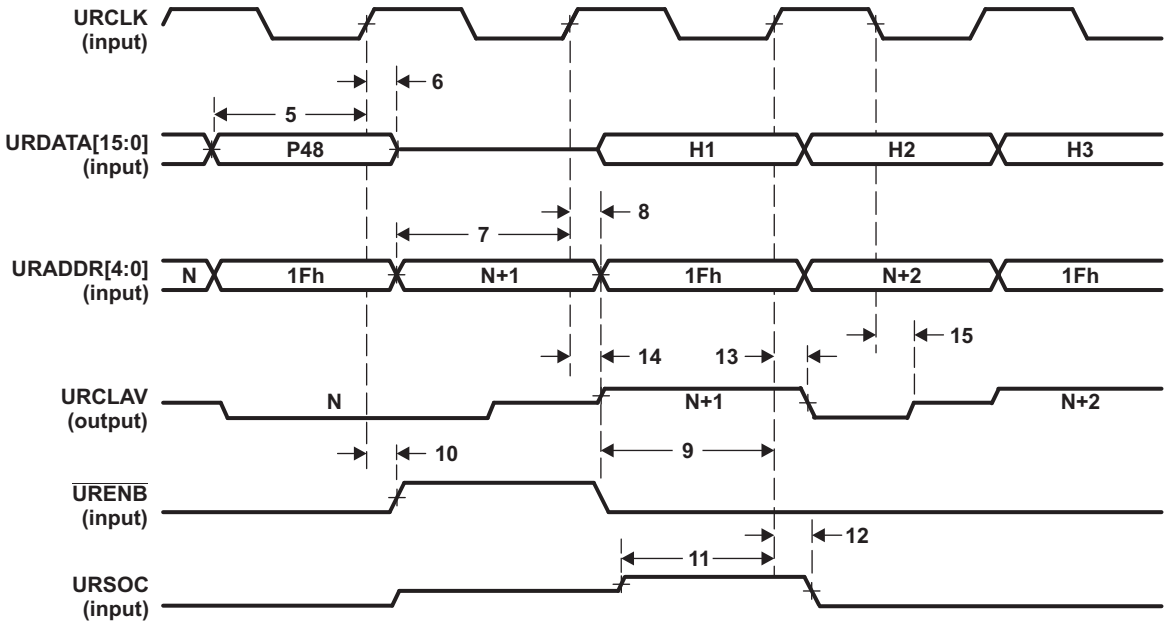

Figure 7-63. UTOPIA Slave Receive

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Table 7-148. Timing Requirements for UTOPIA Slave Transmit Cycles

(see Figure 7-64)

NO.			500/625/700		UNIT
			MIN	MAX	
16	$t_{su(UXADDR-UXCLKH)}$	Setup time, UXADDR valid before UXCLK high	4		ns
17	$t_{h(UXCLKH-UXADDR)}$	Hold time, UXADDR valid after UXCLK high	1		ns
18	$t_{su(UXENB-UXCLKH)}$	Setup time, $\overline{\text{UXENB}}$ valid before UXCLK high	4		ns
19	$t_{h(UXCLKH-UXENB)}$	Hold time, $\overline{\text{UXENB}}$ valid after UXCLK high	1		ns

Table 7-149. Switching Characteristics Over Recommended Operating Conditions for UTOPIA Slave Transmit Cycles

(see Figure 7-64)

NO.	PARAMETER		500/625/700		UNIT
			MIN	MAX	
20[1]	$t_{d(UXCLKH-UXDATAV)}$	Delay time, UXCLK high to UXDATA valid	2	10	ns
21[1]	$t_{en(UXCLKH-UXDATA)}$	Enable time, UXCLK high to UXDATA driven	2	10	ns
22[2] [3]	$t_{dis(UXCLKH-UXDATAZ)}$	Disable time, UXCLK high to UXDATA high-impedance state	2	10	ns
23[1]	$t_{d(UXCLKH-UXCLAV)}$	Delay time, UXCLK high to UXCLAV driven low	2	10	ns
24[1]	$t_{en(UXCLKH-UXCLAV)}$	Enable time, UXCLK high to UXCLAV driven high	2	10	ns
25[2] [3]	$t_{dis(UXCLKL-UXCLAVZ)}$	Disable time, UXCLK low to UXCLAV high-impedance state	2	10	ns
26[1]	$t_{d(UXCLKH-UXSOCV)}$	Delay time, UXCLK high to UXSOC valid	2	10	ns
27[1]	$t_{en(UXCLKH-UXSOC)}$	Enable time, UXCLK high to UXSOC driven	2	10	ns
28[2] [3]	$t_{dis(UXCLKH-UXSOCZ)}$	Disable time, UXCLK high to UXSOC high-impedance state	2	10	ns

(1) MAX delay time and enable time increases to 12.5 ns at 20 pF and 14 ns at 30 pF, specified by design.
(2) Specifed by design for MIN values.
(3) Specifed by design for MAX values.

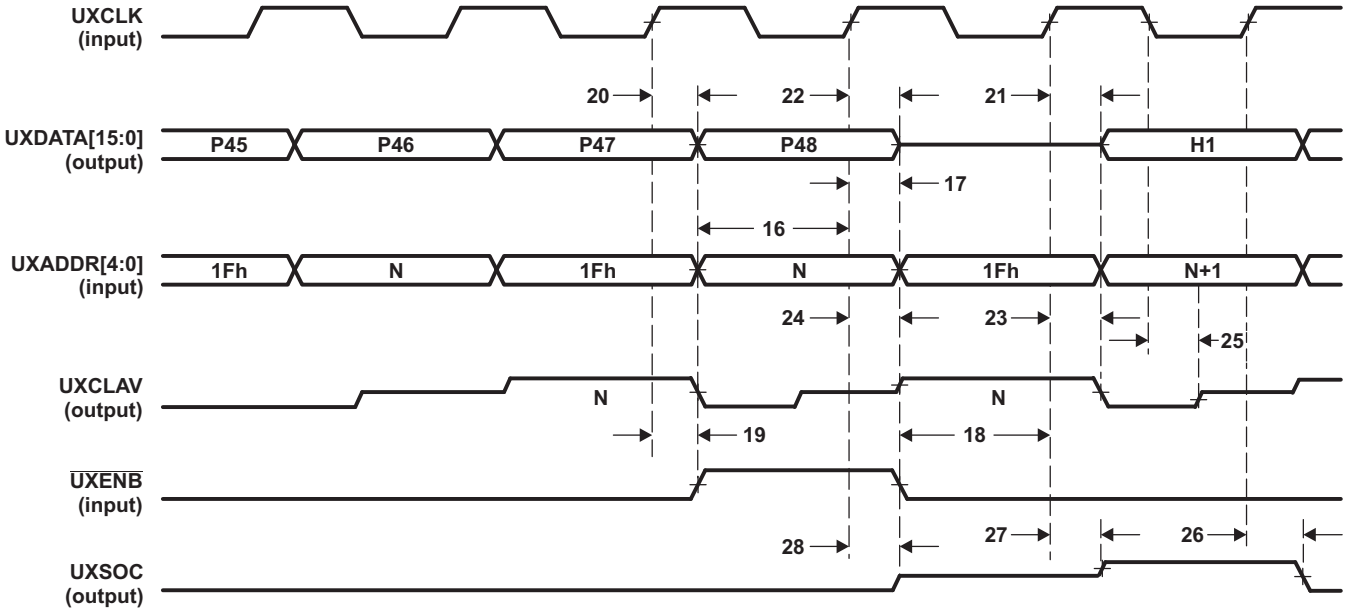

Figure 7-64. UTOPIA Slave Transmit

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7.18 Serial RapidIO (SRIO) Port

The SRIO ports on the C6472 device are high-performance, low-pin-count interconnects aimed for embedded markets. The use of the RapidIO interconnect in a system board design can create a homogeneous interconnect environment providing simple, high-throughput connectivity and control among the devices. RapidIO is based on the memory and device addressing concepts of processor buses where the transaction processing is managed completely by hardware. This enables the RapidIO interconnect to lower the system cost by providing low latency, reduced overhead, packet data processing and high system bandwidth. The RapidIO interconnect offers very-low-pin count interfaces with scalable system bandwidth. The C6472 device contains two independent 1x lanes. The lanes can operate at 1.25, 2.5, or 3.135 Gbps.

The PHY part of the SRIO consists of the physical layer and includes the input and output buffers (each serial link consists of a differential pair), the 8-bit/10-bit encoder/decoder, the PLL clock recovery, and the parallel-to-serial/serial-to-parallel converters (SERDES).

The transmitter supports programmable output levels and de-emphasis settings. The receiver has equalization that can be converged automatically or programmed statically.

7.18.1 Serial RapidIO Device-Specific Information

The approach to specifying interface timing for the SRIO Port is different than on other interfaces such as HPI. For these other interfaces the device timing was specified in terms of data manual specifications and I/O buffer information specification (IBIS) models.

For the C6472 SRIO Port, Texas Instruments (TI) provides a printed circuit board (PCB) solution showing two DSPs connected via a 1x SRIO link directly to the user. TI has performed the simulation and system characterization to ensure all SRIO interface timings in this solution are met. The complete SRIO system solution is documented in the *TMS320C6472/TMS320TCI6486 Serial RapidIO Implementation Guidelines* application report (literature number SPRAAT9).

TI *only* supports designs that follow the board design guidelines outlined in the SPRAAT9 application report.

The Serial RapidIO peripheral is a master peripheral in the C6472 DSP. It conforms to the *RapidIO™ Interconnect Specification, Part VI: Physical Layer 1x/4x LP-Serial Specification, Revision 1.2*. For more information from an application perspective, see the *TMS320C6472/TMS320TCI648x Serial RapidIO (SRIO) User's Guide* (literature number SPRUE13).

7.18.2 SRIO Peripheral Register Descriptions

Table 7-150. RapidIO Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0000	PID	Peripheral Identification Register
02D0 0004	PCR	Peripheral Control Register
02D0 0008 - 02D0 001C	-	Reserved
02D0 0020	PER_SET_CNTL	Peripheral Settings Control Register
02D0 0024 - 02D0 002C	-	Reserved
02D0 0030	GBL_EN	Peripheral Global Enable Register
02D0 0034	GBL_EN_STAT	Peripheral Global Enable Status
02D0 0038	BLK0_EN	Block Enable 0
02D0 003C	BLK0_EN_STAT	Block Enable Status 0
02D0 0040	BLK1_EN	Block Enable 1
02D0 0044	BLK1_EN_STAT	Block Enable Status 1
02D0 0048	BLK2_EN	Block Enable 2
02D0 004C	BLK2_EN_STAT	Block Enable Status 2

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0050	BLK3_EN	Block Enable 3
02D0 0054	BLK3_EN_STAT	Block Enable Status 3
02D0 0058	BLK4_EN	Block Enable 4
02D0 005C	BLK4_EN_STAT	Block Enable Status 4
02D0 0060	BLK5_EN	Block Enable 5
02D0 0064	BLK5_EN_STAT	Block Enable Status 5
02D0 0068	BLK6_EN	Block Enable 6
02D0 006C	BLK6_EN_STAT	Block Enable Status 6
02D0 0070	BLK7_EN	Block Enable 7
02D0 0074	BLK7_EN_STAT	Block Enable Status 7
02D0 0078	BLK8_EN	Block Enable 8
02D0 007C	BLK8_EN_STAT	Block Enable Status 8
02D0 0080	DEVICEID_REG1	RapidIO DEVICEID1 Register
02D0 0084	DEVICEID_REG2	RapidIO DEVICEID2 Register
02D0 0088	DEVICEID_REG3	RapidIO DEVICEID3 Register
02D0 008C	DEVICEID_REG4	RapidIO DEVICEID4 Register
02D0 0090	PF_16B_CNTL0	Packet Forwarding Register 0 for 16-bit DeviceIDs
02D0 0094	PF_8B_CNTL0	Packet Forwarding Register 0 for 8-bit DeviceIDs
02D0 0098	PF_16B_CNTL1	Packet Forwarding Register 1 for 16-bit DeviceIDs
02D0 009C	PF_8B_CNTL1	Packet Forwarding Register 1 for 8-bit DeviceIDs
02D0 00A0	PF_16B_CNTL2	Packet Forwarding Register 2 for 16-bit DeviceIDs
02D0 00A4	PF_8B_CNTL2	Packet Forwarding Register 2 for 8-bit DeviceIDs
02D0 00A8	PF_16B_CNTL3	Packet Forwarding Register 3 for 16-bit DeviceIDs
02D0 00AC	PF_8B_CNTL3	Packet Forwarding Register 3 for 8-bit DeviceIDs
02D0 00B0 - 02D0 00FC	-	Reserved
02D0 0100	SERDES_CFGRX0_CNTL	SERDES Receive Channel Configuration Register 0
02D0 0104	SERDES_CFGRX1_CNTL	SERDES Receive Channel Configuration Register 1
02D0 0108	SERDES_CFGRX2_CNTL	SERDES Receive Channel Configuration Register 2
02D0 010C	SERDES_CFGRX3_CNTL	SERDES Receive Channel Configuration Register 3
02D0 0110	SERDES_CFGTX0_CNTL	SERDES Transmit Channel Configuration Register 0
02D0 0114	SERDES_CFGTX1_CNTL	SERDES Transmit Channel Configuration Register 1
02D0 0118	SERDES_CFGTX2_CNTL	SERDES Transmit Channel Configuration Register 2
02D0 011C	SERDES_CFGTX3_CNTL	SERDES Transmit Channel Configuration Register 3
02D0 0120	SERDES_CFG0_CNTL	SERDES Macro Configuration Register 0
02D0 0124	SERDES_CFG1_CNTL	SERDES Macro Configuration Register 1
02D0 0128	SERDES_CFG2_CNTL	SERDES Macro Configuration Register 2
02D0 012C	SERDES_CFG3_CNTL	SERDES Macro Configuration Register 3
02D0 0130 - 02D0 01FC	-	Reserved
02D0 0200	Doorbell0_ICSR	Doorbell Interrupt Condition Status Register 0
02D0 0204	-	Reserved
02D0 0208	Doorbell0_ICCR	Doorbell Interrupt Condition Clear Register 0
02D0 020C	-	Reserved
02D0 0210	Doorbell1_ICSR	Doorbell Interrupt Condition Status Register 1
02D0 0214	-	Reserved
02D0 0218	Doorbell1_ICCR	Doorbell Interrupt Condition Clear Register 1
02D0 021C	-	Reserved
02D0 0220	Doorbell2_ICSR	Doorbell Interrupt Condition Status Register 2

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0224	-	Reserved
02D0 0228	Doorbell2_ICCR	Doorbell Interrupt Condition Clear Register 2
02D0 022C	-	Reserved
02D0 0230	Doorbell3_ICSR	Doorbell Interrupt Condition Status Register 3
02D0 0234	-	Reserved
02D0 0238	Doorbell3_ICCR	Doorbell Interrupt Condition Clear Register 3
02D0 023C	-	Reserved
02D0 0240	RX_CPPI_ICSR	RX CPPI Interrupt Condition Status Register
02D0 0244	-	Reserved
02D0 0248	RX_CPPI_ICCR	RX CPPI Interrupt Condition Clear Register
02D0 024c	-	Reserved
02D0 0250	TX_CPPI_ICSR	TX CPPI Interrupt Condition Status Register
02D0 0254	-	Reserved
02D0 0258	TX_CPPI_ICCR	TX CPPI Interrupt Condition Clear Register
02D0 025C	-	Reserved
02D0 0260	LSU_ICSR	LSU Interrupt Condition Status Register
02D0 0264	-	Reserved
02D0 0268	LSU_ICCR	LSU Interrupt Condition Clear Register
02D0 026C	-	Reserved
02D0 0270	ERR_RST_EVNT_ICSR	Error, Reset, and Special Event Interrupt Condition Status Register
02D0 0274	-	Reserved
02D0 0278	ERR_RST_EVNT_ICCR	Error, Reset, and Special Event Interrupt Condition Clear Register
02D0 027C	-	Reserved
02D0 0280	Doorbell0_ICRR	Doorbell0 Interrupt Condition Routing Register
02D0 0284	Doorbell0_ICRR2	Doorbell 0 Interrupt Condition Routing Register 2
02D0 0288 - 02D0 028C	-	Reserved
02D0 0290	Doorbell1_ICRR	Doorbell1 Interrupt Condition Routing Register
02D0 0294	Doorbell1_ICRR2	Doorbell 1 Interrupt Condition Routing Register 2
02D0 0298 - 02D0 029C	-	Reserved
02D0 02A0	Doorbell2_ICRR	Doorbell2 Interrupt Condition Routing Register
02D0 02A4	Doorbell2_ICRR2	Doorbell 2 Interrupt Condition Routing Register 2
02D0 02A8 - 02D0 02AC	-	Reserved
02D0 02B0	Doorbell3_ICRR	Doorbell3 Interrupt Condition Routing Register
02D0 02B4	Doorbell3_ICRR2	Doorbell 3 Interrupt Condition Routing Register 2
02D0 02B8 - 02D0 02BC	-	Reserved
02D0 02C0	RX_CPPI_ICRR	Receive CPPI Interrupt Condition Routing Register
02D0 02C4	RX_CPPI_ICRR2	Receive CPPI Interrupt Condition Routing Register 2
02D0 02C8 - 02D0 02CC	-	Reserved
02D0 02D0	TX_CPPI_ICRR	Transmit CPPI Interrupt Condition Routing Register
02D0 02D4	TX_CPPI_ICRR2	Transmit CPPI Interrupt Condition Routing Register 2
02D0 02D8 - 02D0 02DC	-	Reserved
02D0 02E0	LSU_ICRR0	LSU Interrupt Condition Routing Register 0
02D0 02E4	LSU_ICRR1	LSU Interrupt Condition Routing Register 1
02D0 02E8	LSU_ICRR2	LSU Interrupt Condition Routing Register 2
02D0 02EC	LSU_ICRR3	LSU Interrupt Condition Routing Register 3

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 02F0	ERR_RST_EVNT_ICRR	Error, Reset, and Special Event Interrupt Condition Routing Register
02D0 02F4	ERR_RST_EVNT_ICRR2	Error, Reset, and Special Event Interrupt Condition Routing Register 2
02D0 02F8	ERR_RST_EVNT_ICRR3	Error, Reset, and Special Event Interrupt Condition Routing Register 3
02D0 02FC	-	Reserved
02D0 0300	INTDST0_DECODE	INTDST Interrupt Status Decode Register 0
02D0 0304	INTDST1_DECODE	INTDST Interrupt Status Decode Register 1
02D0 0308	INTDST2_DECODE	INTDST Interrupt Status Decode Register 2
02D0 030C	INTDST3_DECODE	INTDST Interrupt Status Decode Register 3
02D0 0310	INTDST4_DECODE	INTDST Interrupt Status Decode Register 4
02D0 0314	INTDST5_DECODE	INTDST Interrupt Status Decode Register 5
02D0 0318	INTDST6_DECODE	INTDST Interrupt Status Decode Register 6
02D0 031C	INTDST7_DECODE	INTDST Interrupt Status Decode Register 7
02D0 0320	INTDST0_RATE_CNTL	INTDST Interrupt Rate Control Register 0
02D0 0324	INTDST1_RATE_CNTL	INTDST Interrupt Rate Control Register 1
02D0 0328	INTDST2_RATE_CNTL	INTDST Interrupt Rate Control Register 2
02D0 032C	INTDST3_RATE_CNTL	INTDST Interrupt Rate Control Register 3
02D0 0330	INTDST4_RATE_CNTL	INTDST Interrupt Rate Control Register 4
02D0 0334	INTDST5_RATE_CNTL	INTDST Interrupt Rate Control Register 5
02D0 0338	INTDST6_RATE_CNTL	INTDST Interrupt Rate Control Register 6
02D0 033C	INTDST7_RATE_CNTL	INTDST Interrupt Rate Control Register 7
02D0 0340 - 02D0 03FC	-	Reserved
02D0 0400	LSU1_REG0	LSU1 Control Register 0
02D0 0404	LSU1_REG1	LSU1 Control Register 1
02D0 0408	LSU1_REG2	LSU1 Control Register 2
02D0 040C	LSU1_REG3	LSU1 Control Register 3
02D0 0410	LSU1_REG4	LSU1 Control Register 4
02D0 0414	LSU1_REG5	LSU1 Control Register 5
02D0 0418	LSU1_REG6	LSU1 Control Register 6
02D0 041C	LSU1_FLOW_MASKS	LSU1 Congestion Control Flow Mask Register
02D0 0420	LSU2_REG0	LSU2 Control Register 0
02D0 0424	LSU2_REG1	LSU2 Control Register 1
02D0 0428	LSU2_REG2	LSU2 Control Register 2
02D0 042C	LSU2_REG3	LSU2 Control Register 3
02D0 0430	LSU2_REG4	LSU2 Control Register 4
02D0 0434	LSU2_REG5	LSU2 Control Register 5
02D0 0438	LSU2_REG6	LSU2 Control Register 6
02D0 043C	LSU2_FLOW_MASKS1	LSU2 Congestion Control Flow Mask Register
02D0 0440	LSU3_REG0	LSU3 Control Register 0
02D0 0444	LSU3_REG1	LSU3 Control Register 1
02D0 0448	LSU3_REG2	LSU3 Control Register 2
02D0 044C	LSU3_REG3	LSU3 Control Register 3
02D0 0450	LSU3_REG4	LSU3 Control Register 4
02D0 0454	LSU3_REG5	LSU3 Control Register 5
02D0 0458	LSU3_REG6	LSU3 Control Register 6
02D0 045C	LSU3_FLOW_MASKS2	LSU3 Congestion Control Flow Mask Register

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0460	LSU4_REG0	LSU4 Control Register 0
02D0 0464	LSU4_REG1	LSU4 Control Register 1
02D0 0468	LSU4_REG2	LSU4 Control Register 2
02D0 046C	LSU4_REG3	LSU4 Control Register 3
02D0 0470	LSU4_REG4	LSU4 Control Register 4
02D0 0474	LSU4_REG5	LSU4 Control Register 5
02D0 0478	LSU4_REG6	LSU4 Control Register 6
02D0 047C	LSU4_FLOW_MASKS3	LSU4 Congestion Control Flow Mask Register
02D0 0480 - 02D0 04FC	-	Reserved
02D0 0500	QUEUE0_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 0
02D0 0504	QUEUE1_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 1
02D0 0508	QUEUE2_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 2
02D0 050C	QUEUE3_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 3
02D0 0510	QUEUE4_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 4
02D0 0514	QUEUE5_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 5
02D0 0518	QUEUE6_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 6
02D0 051C	QUEUE7_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 7
02D0 0520	QUEUE8_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 8
02D0 0524	QUEUE9_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 9
02D0 0528	QUEUE10_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 10
02D0 052C	QUEUE11_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 11
02D0 0530	QUEUE12_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 12
02D0 0534	QUEUE13_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 13
02D0 0538	QUEUE14_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 14
02D0 053C	QUEUE15_TXDMA_HDP	Queue Transmit DMA Head Descriptor Pointer Register 15
02D0 0540 - 02D0 057C	-	Reserved
02D0 0580	QUEUE0_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 0
02D0 0584	QUEUE1_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 1
02D0 0588	QUEUE2_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 2
02D0 058C	QUEUE3_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 3
02D0 0590	QUEUE4_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 4
02D0 0594	QUEUE5_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 5
02D0 0598	QUEUE6_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 6
02D0 059C	QUEUE7_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 7
02D0 05A0	QUEUE8_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 8
02D0 05A4	QUEUE9_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 9
02D0 05A8	QUEUE10_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 10
02D0 05AC	QUEUE11_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 11
02D0 05B0	QUEUE12_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 12
02D0 05B4	QUEUE13_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 13
02D0 05B8	QUEUE14_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 14
02D0 05BC	QUEUE15_TXDMA_CP	Queue Transmit DMA Completion Pointer Register 15
02D0 05D0 - 02D0 05FC	-	Reserved

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0600	QUEUE0_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 0
02D0 0604	QUEUE1_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 1
02D0 0608	QUEUE2_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 2
02D0 060C	QUEUE3_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 3
02D0 0610	QUEUE4_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 4
02D0 0614	QUEUE5_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 5
02D0 0618	QUEUE6_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 6
02D0 061C	QUEUE7_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 7
02D0 0620	QUEUE8_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 8
02D0 0624	QUEUE9_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 9
02D0 0628	QUEUE10_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 10
02D0 062C	QUEUE11_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 11
02D0 0630	QUEUE12_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 12
02D0 0634	QUEUE13_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 13
02D0 0638	QUEUE14_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 14
02D0 063C	QUEUE15_RXDMA_HDP	Queue Receive DMA Head Descriptor Pointer Register 15
02D0 0640 - 02D0 067C	-	Reserved
02D0 0680	QUEUE0_RXDMA_CP	Queue Receive DMA Completion Pointer Register 0
02D0 0684	QUEUE1_RXDMA_CP	Queue Receive DMA Completion Pointer Register 1
02D0 0688	QUEUE2_RXDMA_CP	Queue Receive DMA Completion Pointer Register 2
02D0 068C	QUEUE3_RXDMA_CP	Queue Receive DMA Completion Pointer Register 3
02D0 0690	QUEUE4_RXDMA_CP	Queue Receive DMA Completion Pointer Register 4
02D0 0694	QUEUE5_RXDMA_CP	Queue Receive DMA Completion Pointer Register 5
02D0 0698	QUEUE6_RXDMA_CP	Queue Receive DMA Completion Pointer Register 6
02D0 069C	QUEUE7_RXDMA_CP	Queue Receive DMA Completion Pointer Register 7
02D0 06A0	QUEUE8_RXDMA_CP	Queue Receive DMA Completion Pointer Register 8
02D0 06A4	QUEUE9_RXDMA_CP	Queue Receive DMA Completion Pointer Register 9
02D0 06A8	QUEUE10_RXDMA_CP	Queue Receive DMA Completion Pointer Register 10
02D0 06AC	QUEUE11_RXDMA_CP	Queue Receive DMA Completion Pointer Register 11
02D0 06B0	QUEUE12_RXDMA_CP	Queue Receive DMA Completion Pointer Register 12
02D0 06B4	QUEUE13_RXDMA_CP	Queue Receive DMA Completion Pointer Register 13
02D0 06B8	QUEUE14_RXDMA_CP	Queue Receive DMA Completion Pointer Register 14
02D0 06BC	QUEUE15_RXDMA_CP	Queue Receive DMA Completion Pointer Register 15
02D0 06C0 - 02D0 006FC	-	Reserved
02D0 0700	TX_QUEUE_TEAR_DOWN	Transmit Queue Teardown Register
02D0 0704	TX_CPPI_FLOW_MASKS0	Transmit CPPI Supported Flow Mask Register 0
02D0 0708	TX_CPPI_FLOW_MASKS1	Transmit CPPI Supported Flow Mask Register 1
02D0 070C	TX_CPPI_FLOW_MASKS2	Transmit CPPI Supported Flow Mask Register 2
02D0 0710	TX_CPPI_FLOW_MASKS3	Transmit CPPI Supported Flow Mask Register 3
02D0 0714	TX_CPPI_FLOW_MASKS4	Transmit CPPI Supported Flow Mask Register 4
02D0 0718	TX_CPPI_FLOW_MASKS5	Transmit CPPI Supported Flow Mask Register 5
02D0 071C	TX_CPPI_FLOW_MASKS6	Transmit CPPI Supported Flow Mask Register 6
02D0 0720	TX_CPPI_FLOW_MASKS7	Transmit CPPI Supported Flow Mask Register 7
02D0 0724 - 02D0 073C	-	Reserved
02D0 0740	RX_QUEUE_TEAR_DOWN	Receive Queue Teardown Register
02D0 0744	RX_CPPI_CNTL	Receive CPPI Control Register
02D0 0748 - 02D0 07DC	-	Reserved

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 07E0	TX_QUEUE_CNTL0	Transmit CPPI Weighted Round Robin Control Register 0
02D0 07E4	TX_QUEUE_CNTL1	Transmit CPPI Weighted Round Robin Control Register 1
02D0 07E8	TX_QUEUE_CNTL2	Transmit CPPI Weighted Round Robin Control Register 2
02D0 07EC	TX_QUEUE_CNTL3	Transmit CPPI Weighted Round Robin Control Register 3
02D0 07F0 - 02D0 07FC	-	Reserved
02D0 0800	RXU_MAP_L0	Mailbox-to-Queue Mapping Register L0
02D0 0804	RXU_MAP_H0	Mailbox-to-Queue Mapping Register H0
02D0 0808	RXU_MAP_L1	Mailbox-to-Queue Mapping Register L1
02D0 080C	RXU_MAP_H1	Mailbox-to-Queue Mapping Register H1
02D0 0810	RXU_MAP_L2	Mailbox-to-Queue Mapping Register L2
02D0 0814	RXU_MAP_H2	Mailbox-to-Queue Mapping Register H2
02D0 0818	RXU_MAP_L3	Mailbox-to-Queue Mapping Register L3
02D0 081C	RXU_MAP_H3	Mailbox-to-Queue Mapping Register H3
02D0 0820	RXU_MAP_L4	Mailbox-to-Queue Mapping Register L4
02D0 0824	RXU_MAP_H4	Mailbox-to-Queue Mapping Register H4
02D0 0828	RXU_MAP_L5	Mailbox-to-Queue Mapping Register L5
02D0 082C	RXU_MAP_H5	Mailbox-to-Queue Mapping Register H5
02D0 0830	RXU_MAP_L6	Mailbox-to-Queue Mapping Register L6
02D0 0834	RXU_MAP_H6	Mailbox-to-Queue Mapping Register H6
02D0 0838	RXU_MAP_L7	Mailbox-to-Queue Mapping Register L7
02D0 083C	RXU_MAP_H7	Mailbox-to-Queue Mapping Register H7
02D0 0840	RXU_MAP_L8	Mailbox-to-Queue Mapping Register L8
02D0 0844	RXU_MAP_H8	Mailbox-to-Queue Mapping Register H8
02D0 0848	RXU_MAP_L9	Mailbox-to-Queue Mapping Register L9
02D0 084C	RXU_MAP_H9	Mailbox-to-Queue Mapping Register H9
02D0 0850	RXU_MAP_L10	Mailbox-to-Queue Mapping Register L10
02D0 0854	RXU_MAP_H10	Mailbox-to-Queue Mapping Register H10
02D0 0858	RXU_MAP_L11	Mailbox-to-Queue Mapping Register L11
02D0 085C	RXU_MAP_H11	Mailbox-to-Queue Mapping Register H11
02D0 0860	RXU_MAP_L12	Mailbox-to-Queue Mapping Register L12
02D0 0864	RXU_MAP_H12	Mailbox-to-Queue Mapping Register H12
02D0 0868	RXU_MAP_L13	Mailbox-to-Queue Mapping Register L13
02D0 086C	RXU_MAP_H13	Mailbox-to-Queue Mapping Register H13
02D0 0870	RXU_MAP_L14	Mailbox-to-Queue Mapping Register L14
02D0 0874	RXU_MAP_H14	Mailbox-to-Queue Mapping Register H14
02D0 0878	RXU_MAP_L15	Mailbox-to-Queue Mapping Register L15
02D0 087C	RXU_MAP_H15	Mailbox-to-Queue Mapping Register H15
02D0 0880	RXU_MAP_L16	Mailbox-to-Queue Mapping Register L16
02D0 0884	RXU_MAP_H16	Mailbox-to-Queue Mapping Register H16
02D0 0888	RXU_MAP_L17	Mailbox-to-Queue Mapping Register L17
02D0 088C	RXU_MAP_H17	Mailbox-to-Queue Mapping Register H17
02D0 0890	RXU_MAP_L18	Mailbox-to-Queue Mapping Register L18
02D0 0894	RXU_MAP_H18	Mailbox-to-Queue Mapping Register H18
02D0 0898	RXU_MAP_L19	Mailbox-to-Queue Mapping Register L19
02D0 089C	RXU_MAP_H19	Mailbox-to-Queue Mapping Register H19
02D0 08A0	RXU_MAP_L20	Mailbox-to-Queue Mapping Register L20
02D0 08A4	RXU_MAP_H20	Mailbox-to-Queue Mapping Register H20

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 08A8	RXU_MAP_L21	Mailbox-to-Queue Mapping Register L21
02D0 08AC	RXU_MAP_H21	Mailbox-to-Queue Mapping Register H21
02D0 08B0	RXU_MAP_L22	Mailbox-to-Queue Mapping Register L22
02D0 08B4	RXU_MAP_H22	Mailbox-to-Queue Mapping Register H22
02D0 08B8	RXU_MAP_L23	Mailbox-to-Queue Mapping Register L23
02D0 08BC	RXU_MAP_H23	Mailbox-to-Queue Mapping Register H23
02D0 08C0	RXU_MAP_L24	Mailbox-to-Queue Mapping Register L24
02D0 08C4	RXU_MAP_H24	Mailbox-to-Queue Mapping Register H24
02D0 08C8	RXU_MAP_L25	Mailbox-to-Queue Mapping Register L25
02D0 08CC	RXU_MAP_H25	Mailbox-to-Queue Mapping Register H25
02D0 08D0	RXU_MAP_L26	Mailbox-to-Queue Mapping Register L26
02D0 08D4	RXU_MAP_H26	Mailbox-to-Queue Mapping Register H26
02D0 08D8	RXU_MAP_L27	Mailbox-to-Queue Mapping Register L27
02D0 08DC	RXU_MAP_H27	Mailbox-to-Queue Mapping Register H27
02D0 08E0	RXU_MAP_L28	Mailbox-to-Queue Mapping Register L28
02D0 08E4	RXU_MAP_H28	Mailbox-to-Queue Mapping Register H28
02D0 08E8	RXU_MAP_L29	Mailbox-to-Queue Mapping Register L29
02D0 08EC	RXU_MAP_H29	Mailbox-to-Queue Mapping Register H29
02D0 08F0	RXU_MAP_L30	Mailbox-to-Queue Mapping Register L30
02D0 08F4	RXU_MAP_H30	Mailbox-to-Queue Mapping Register H30
02D0 08F8	RXU_MAP_L31	Mailbox-to-Queue Mapping Register L31
02D0 08FC	RXU_MAP_H31	Mailbox-to-Queue Mapping Register H31
02D0 0900	FLOW_CNTL0	Flow Control Table Entry Register 0
02D0 0904	FLOW_CNTL1	Flow Control Table Entry Register 1
02D0 0908	FLOW_CNTL2	Flow Control Table Entry Register 2
02D0 090C	FLOW_CNTL3	Flow Control Table Entry Register 3
02D0 0910	FLOW_CNTL4	Flow Control Table Entry Register 4
02D0 0914	FLOW_CNTL5	Flow Control Table Entry Register 5
02D0 0918	FLOW_CNTL6	Flow Control Table Entry Register 6
02D0 091C	FLOW_CNTL7	Flow Control Table Entry Register 7
02D0 0920	FLOW_CNTL8	Flow Control Table Entry Register 8
02D0 0924	FLOW_CNTL9	Flow Control Table Entry Register 9
02D0 0928	FLOW_CNTL10	Flow Control Table Entry Register 10
02D0 092C	FLOW_CNTL11	Flow Control Table Entry Register 11
02D0 0930	FLOW_CNTL12	Flow Control Table Entry Register 12
02D0 0934	FLOW_CNTL13	Flow Control Table Entry Register 13
02D0 0938	FLOW_CNTL14	Flow Control Table Entry Register 14
02D0 093C	FLOW_CNTL15	Flow Control Table Entry Register 15
02D0 0940 - 02D0 09FC	-	Reserved
RapidIO Peripheral-Specific Registers		
02D0 1000	DEV_ID	Device Identity CAR
02D0 1004	DEV_INFO	Device Information CAR
02D0 1008	ASBLY_ID	Assembly Identity CAR
02D0 100C	ASBLY_INFO	Assembly Information CAR
02D0 1010	PE_FEAT	Processing Element Features CAR
02D0 1014	-	Reserved
02D0 1018	SRC_OP	Source Operations CAR

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 101C	DEST_OP	Destination Operations CAR
02D0 1020 - 02D0 1048	-	Reserved
02D0 104C	PE_LL_CTL	Processing Element Logical Layer Control CSR
02D0 1050 - 02D0 1054	-	Reserved
02D0 1058	LCL_CFG_HBAR	Local Configuration Space Base Address 0 CSR
02D0 105C	LCL_CFG_BAR	Local Configuration Space Base Address 1 CSR
02D0 1060	BASE_ID	Base Device ID CSR
02D0 1064	-	Reserved
02D0 1068	HOST_BASE_ID_LOCK	Host Base Device ID Lock CSR
02D0 106C	COMP_TAG	Component Tag CSR
02D0 1070 - 02D0 10FC	-	Reserved
RapidIO Extended Features - LP Serial Registers		
02D0 1100	SP_MB_HEAD	1x/4x LP_Serial Port Maintenance Block Header
02D0 1104 - 02D0 1118		
02D0 1120	SP_LT_CTL	Port Link Time-Out Control CSR
02D0 1124	SP_RT_CTL	Port Response Time-Out Control CSR
02D0 1128 - 02D0 1138	-	Reserved
02D0 113C	SP_GEN_CTL	Port General Control CSR
02D0 1140	SP0_LM_REQ	Port 0 Link Maintenance Request CSR
02D0 1144	SP0_LM_RESP	Port 0 Link Maintenance Response CSR
02D0 1148	SP0_ACKID_STAT	Port 0 Local AckID Status CSR
02D0 114C - 02D0 1154	-	Reserved
02D0 1158	SP0_ERR_STAT	Port 0 Error and Status CSR
02D0 115C	SP0_CTL	Port 0 Control CSR
02D0 1160	SP1_LM_REQ	Port 1 Link Maintenance Request CSR
02D0 1164	SP1_LM_RESP	Port 1 Link Maintenance Response CSR
02D0 1168	SP1_ACKID_STAT	Port 1 Local AckID Status CSR
02D0 116C - 02D0 1174	-	Reserved
02D0 1178	SP1_ERR_STAT	Port 1 Error and Status CSR
02D0 117C	SP1_CTL	Port 1 Control CSR
02D0 1180	SP2_LM_REQ	Port 2 Link Maintenance Request CSR
02D0 1184	SP2_LM_RESP	Port 2 Link Maintenance Response CSR
02D0 1188	SP2_ACKID_STAT	Port 2 Local AckID Status CSR
02D0 118C - 02D0 1194	-	Reserved
02D0 1198	SP2_ERR_STAT	Port 2 Error and Status CSR
02D0 119C	SP2_CTL	Port 2 Control CSR
02D0 11A0	SP3_LM_REQ	Port 3 Link Maintenance Request CSR
02D0 11A4	SP3_LM_RESP	Port 3 Link Maintenance Response CSR
02D0 11A8	SP3_ACKID_STAT	Port 3 Local AckID Status CSR
02D0 11AC - 02D0 11B4	-	Reserved
02D0 11B8	SP3_ERR_STAT	Port 3 Error and Status CSR
02D0 11BC	SP3_CTL	Port 3 Control CSR
02D0 11C0 - 02D0 1FFC	-	Reserved
RapidIO Extended Feature - Error Management Registers		
02D0 2000	ERR_RPT_BH	Error Reporting Block Header
02D0 2004	-	Reserved
02D0 2008	ERR_DET	Logical/Transport Layer Error Detect CSR

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 200C	ERR_EN	Logical/Transport Layer Error Enable CSR
02D0 2010	H_ADDR_CAPT	Logical/Transport Layer High Address Capture CSR
02D0 2014	ADDR_CAPT	Logical/Transport Layer Address Capture CSR
02D0 2018	ID_CAPT	Logical/Transport Layer Device ID Capture CSR
02D0 201C	CTRL_CAPT	Logical/Transport Layer Control Capture CSR
02D0 2020 - 02D0 2024	-	Reserved
02D0 2028	PW_TGT_ID	Port-Write Target Device ID CSR
02D0 202C - 02D0 203C	-	Reserved
02D0 2040	SP0_ERR_DET	Port 0 Error Detect CSR
02D0 2044	SP0_RATE_EN	Port 0 Error Enable CSR
02D0 2048	SP0_ERR_ATTR_CAPT_DBG0	Port 0 Attributes Error Capture CSR 0
02D0 204C	SP0_ERR_CAPT_DBG1	Port 0 Packet/Control Symbol Error Capture CSR 1
02D0 2050	SP0_ERR_CAPT_DBG2	Port 0 Packet/Control Symbol Error Capture CSR 2
02D0 2054	SP0_ERR_CAPT_DBG3	Port 0 Packet/Control Symbol Error Capture CSR 3
02D0 2058	SP0_ERR_CAPT_DBG4	Port 0 Packet/Control Symbol Error Capture CSR 4
02D0 205C - 02D0 2064	-	Reserved
02D0 2068	SP0_ERR_RATE	Port 0 Error Rate CSR 0
02D0 206C	SP0_ERR_THRESH	Port 0 Error Rate Threshold CSR
02D0 2070 - 02D0 207C	-	Reserved
02D0 2080	SP1_ERR_DET	Port 1 Error Detect CSR
02D0 2084	SP1_RATE_EN	Port 1 Error Enable CSR
02D0 2088	SP1_ERR_ATTR_CAPT_DBG0	Port 1 Attributes Error Capture CSR 0
02D0 208C	SP1_ERR_CAPT_DBG1	Port 1 Packet/Control Symbol Error Capture CSR 1
02D0 2090	SP1_ERR_CAPT_DBG2	Port 1 Packet/Control Symbol Error Capture CSR 2
02D0 2094	SP1_ERR_CAPT_DBG3	Port 1 Packet/Control Symbol Error Capture CSR 3
02D0 2098	SP1_ERR_CAPT_DBG4	Port 1 Packet/Control Symbol Error Capture CSR 4
02D0 209C - 02D0 20A4	-	Reserved
02D0 20A8	SP1_ERR_RATE	Port 1 Error Rate CSR
02D0 20AC	SP1_ERR_THRESH	Port 1 Error Rate Threshold CSR
02D0 20B0 - 02D0 20BC	-	Reserved
02D0 20C0	SP2_ERR_DET	Port 2 Error Detect CSR
02D0 20C4	SP2_RATE_EN	Port 2 Error Enable CSR
02D0 20C8	SP2_ERR_ATTR_CAPT_DBG0	Port 2 Attributes Error Capture CSR 0
02D0 20CC	SP2_ERR_CAPT_DBG1	Port 2 Packet/Control Symbol Error Capture CSR 1
02D0 20D0	SP2_ERR_CAPT_DBG2	Port 2 Packet/Control Symbol Error Capture CSR 2
02D0 20D4	SP2_ERR_CAPT_DBG3	Port 2 Packet/Control Symbol Error Capture CSR 3
02D0 20D8	SP2_ERR_CAPT_DBG4	Port 2 Packet/Control Symbol Error Capture CSR 4
02D0 20DC - 02D0 20E4	-	Reserved
02D0 20E8	SP2_ERR_RATE	Port 2 Error Rate CSR
02D0 20EC	SP2_ERR_THRESH	Port 2 Error Rate Threshold CSR
02D0 20F0 - 02D0 20FC	-	Reserved
02D0 2100	SP3_ERR_DET	Port 3 Error Detect CSR
02D0 2104	SP3_RATE_EN	Port 3 Error Enable CSR
02D0 2108	SP3_ERR_ATTR_CAPT_DBG0	Port 3 Attributes Error Capture CSR 0
02D0 210C	SP3_ERR_CAPT_DBG1	Port 3 Packet/Control Symbol Error Capture CSR 1
02D0 2110	SP3_ERR_CAPT_DBG2	Port 3 Packet/Control Symbol Error Capture CSR 2
02D0 2114	SP3_ERR_CAPT_DBG3	Port 3 Packet/Control Symbol Error Capture CSR 3

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Table 7-150. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 2118	SP3_ERR_CAPT_DBG4	Port 3 Packet/Control Symbol Error Capture CSR 4
02D0 211C - 02D0 2124	-	Reserved
02D0 2128	SP3_ERR_RATE	Port 3 Error Rate CSR
02D0 212C	SP3_ERR_THRESH	Port 3 Error Rate Threshold CSR
02D0 2130 - 02D1 0FFC	-	Reserved
Implementation Registers		
02D1 1000 - 02D1 1FFC	-	Reserved
02D1 2000	SP_IP_DISCOVERY_TIMER	Port IP Discovery Timer in 4x mode
02D1 2004	SP_IP_MODE	Port IP Mode CSR
02D1 2008	IP_PRESCAL	Port IP Prescaler Register
02D1 200C	-	Reserved
02D1 2010	SP_IP_PW_IN_CAPT0	Port-Write-In Capture CSR Register 0
02D1 2014	SP_IP_PW_IN_CAPT1	Port-Write-In Capture CSR Register 1
02D1 2018	SP_IP_PW_IN_CAPT2	Port-Write-In Capture CSR Register 2
02D1 201C	SP_IP_PW_IN_CAPT3	Port-Write-In Capture CSR Register 3
02D1 2020 - 02D1 3FFC	-	Reserved
02D1 4000	SP0_RST_OPT	Port 0 Reset Option CSR
02D1 4004	SP0_CTL_INDEP	Port 0 Control Independent Register
02D1 4008	SP0_SILENCE_TIMER	Port 0 Silence Timer Register
02D1 400C	SP0_MULT_EVNT_CS	Port 0 Multicast-Event Control Symbol Request Register
02D1 4010	-	Reserved
02D1 4014	RIO_SP0_CS_TX	Port 0 Control Symbol Transmit Register
02D1 4018 - 02D1 40FC	-	Reserved
02D1 4100	RIO_SP1_RST_OPT	Port 1 Reset Option CSR
02D1 4104	RIO_SP1_CTL_INDEP	Port 1 Control Independent Register
02D1 4108	RIO_SP1_SILENCE_TIMER	Port 1 Silence Timer Register
02D1 410C	RIO_SP1_MULT_EVNT_CS	Port 1 Multicast-Event Control Symbol Request Register
02D1 4110	-	Reserved
02D1 4114	RIO_SP1_CS_TX	Port 1 Control Symbol Transmit Register
02D1 4118 - 02D1 41FC	-	Reserved
02D1 4200	RIO_SP2_RST_OPT	Port 2 Reset Option CSR
02D1 4204	RIO_SP2_CTL_INDEP	Port 2 Control Independent Register
02D1 4208	RIO_SP2_SILENCE_TIMER	Port 2 Silence Timer Register
02D1 420C	RIO_SP2_MULT_EVNT_CS	Port 2 Multicast-Event Control Symbol Request Register
02D1 4214	RIO_SP2_CS_TX	Port 2 Control Symbol Transmit Register
02D1 4218 - 02D1 42FC	-	Reserved
02D1 4300	RIO_SP3_RST_OPT	Port 3 Reset Option CSR
02D1 4304	RIO_SP3_CTL_INDEP	Port 3 Control Independent Register
02D1 4308	RIO_SP3_SILENCE_TIMER	Port 3 Silence Timer Register
02D1 430C	RIO_SP3_MULT_EVNT_CS	Port 3 Multicast-Event Control Symbol Request Register
02D1 4310	-	Reserved
02D1 4314	RIO_SP3_CS_TX	Port 3 Control Symbol Transmit Register
02D1 4318 - 02DF FFFC	-	Reserved

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7.19 General-Purpose Input/Output (GPIO)

7.19.1 GPIO Device-Specific Information

On the C6472 device, the GPIO peripheral pins are muxed with configuration inputs that are captured at device reset. For more detailed information on device/peripheral configuration and the C6472 device pin muxing, see Section 3, *Device Configuration*.

7.19.2 GPIO Peripheral Register Descriptions

Table 7-151. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B0 0000	GPIOPID	GPIO Peripheral ID Register
02B0 0004	GPIOEMU	GPIO Emulation Control Register
02B0 0008	BINTEN	GPIO Interrupt Per Bank Enable Register
02B0 000C	-	Reserved
02B0 0010	DIR	GPIO Direction Register
02B0 0014	OUT_DATA	GPIO Output Data register
02B0 0018	SET_DATA	GPIO Set Data register
02B0 001C	CLR_DATA	GPIO Clear Data Register
02B0 0020	IN_DATA	GPIO Input Data Register
02B0 0024	SET_RIS_TRIG	GPIO Set Rising Edge Interrupt Register
02B0 0028	CLR_RIS_TRIG	GPIO Clear Rising Edge Interrupt Register
02B0 002C	SET_FAL_TRIG	GPIO Set Falling Edge Interrupt Register
02B0 0030	CLR_FAL_TRIG	GPIO Clear Falling Edge Interrupt Register
02B0 008C - 02B0 3FFC	-	Reserved

7.19.3 GPIO Electrical Data/Timing

Table 7-152. Timing Requirements for General-Purpose Input(1)

(see Figure 7-65)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	12P		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	12P		ns

(1) P = 1/CPU clock frequency in ns.



Figure 7-65. General-Purpose Input Port Timing

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Table 7-153. Switching Characteristics Over Recommended Operating Conditions for General-Purpose Output(1)

(see Figure 7-66)

NO.			500/625/700		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	6P		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	6P		ns

(1) P = 1/CPU clock frequency in ns.

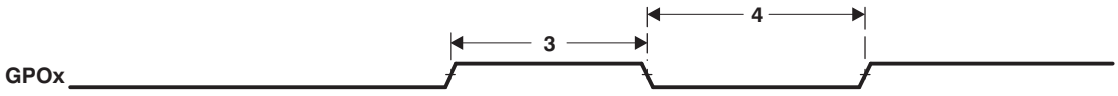

Figure 7-66. General-Purpose Output Port Timing

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7.20 Emulation Features and Capability

7.20.1 Advanced Event Triggering (AET)

The C6472 device supports Advanced Event Triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware Program Breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data Watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State Sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on AET, see the following documents:

Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs application report (literature number SPRA753)

Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems application report (literature number SPRA387)

7.20.2 Trace

The C6472 device supports Trace. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for Trace Advanced Emulation, see the *Emulation and Trace Headers Technical Reference Manual* (literature number SPRU655).

Table 7-154. Timing Requirements for Trace

(see Figure 7-67)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{w(EMUnH)}$	Pulse duration, EMUn high	3 - 0.6(1)		ns
	$t_{w(EMUnH)}$ 90%	Pulse duration, EMUn high detected at 90% V_{OH}	1.5		
2	$t_{w(EMUnL)}$	Pulse duration, EMUn low	3 - 0.6(1)		
	$t_{w(EMUnL)}$ 10%	Pulse duration, EMUn low detected at 10% V_{OH}	1.5		
3	$t_{sko(EMUn)}$	Output Skew time, time delay difference between EMU pins configured as trace.	390 ps	1.8 ns	

(1) This parameter applies to the maximum trace export frequency operating in a 40/60 duty cycle.

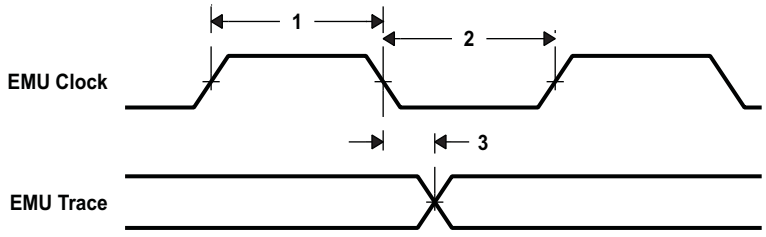

Figure 7-67. Trace Timing

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7.20.3 IEEE 1149.1 JTAG

The JTAG interface is used to support boundary scan testing and emulation of the C6472 device. The JTAG interface provides an asynchronous TRST and only the four primary JTAG signals (TCK, TDI, TMS, and TDO) are required for boundary scan. The pins EMU0 and EMU1 have no effect on the operation of the JTAG interface on the C6472 device. Most interfaces on the device follow the Boundary Scan Test Specification (IEEE1149.1), while the SerDes (RapidIO) supports the AC coupled net test defined in AC Coupled Net Test Specification (IEEE1149.6).

It is expected that all compliant devices are connected through the same JTAG interface, in daisy-chain fashion, as per the specification.

7.20.3.1 IEEE 1149.1 JTAG Compatibility Statement

For maximum reliability, the C6472 DSP includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of an external pullup resistor on TRST. When using this type of JTAG controller, assert TRST to initialize the DSP after powerup and externally drive TRST high before attempting any emulation or boundary scan operations.

7.20.3.2 Boundary Scan Operation

The C6472 device supports boundary scan testing through the IEEE 1149.1 JTAG interface. The *TMS320C6472 BSDL Model* (literature number SPRM384) is available to support boundary scan test vector development. The BSDL model files list POR and RESET as *compliance pins* and define their required state to be a 1. These pins must be pulled high prior to any boundary scan test sequence initialization and they must remain steady at a high level throughout the boundary scan testing to attain valid results. POR and RESET are the only pins (other than power and ground pins) that must remain at a fixed state during the boundary scan testing.

The JTAG ID is commonly read by boundary scan test tools. Note that the VARIANT field in the JTAG ID (see Section 3.10) may not be valid during boundary scan testing unless sufficient CLKIN1 clock cycles have been received (see Section 7.7 and Figure 7-9).

In an ideal system designed for boundary scan test, all of the ICs would have their own JTAG interface and all of the input and output pins would be controlled through the internal boundary scan cells. Since many of the devices on boards, like clock buffers, do not contain boundary scan cells or a JTAG interface, the outputs from these devices should be tristated during boundary scan testing. This allows all of the nets attached to the C6472 device to be tested. Additionally, if testing is desired for SRIO, DDR, or RGMII pins that may be powered down in some configurations, see the notes in Section 7.3.3. Additional BSDL files are available for designs that have one or more of these three interfaces disabled.

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7.20.3.3 JTAG Electrical Data/Timing

Table 7-155. Timing Requirements for JTAG

(see Figure 7-68)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{c(TCLK)}$	Cycle time, TCLK	23.255	(1)	ns
3	$t_{su(TDIV-TCLKH)}$	Setup time, TDI/TMS/$\overline{TRST}$ valid before TCLK high	3		ns
4	$t_{h(TCLKH-TDIV)}$	Hold time, TDI/TMS/$\overline{TRST}$ valid after TCLK high	6 (2)		ns

(1) Fully-synchronous design removes maximum clock period limitations.
(2) Hold time measured from rising edge.

Table 7-156. Switching Characteristics Over Recommended Operating Conditions for JTAG

(see Figure 7-68)

NO.			500/625/700		UNIT
			MIN	MAX	
2	$t_{d(TCLKL-TDOV)}$	Delay time, TCLK low to TDO valid	0	12	ns

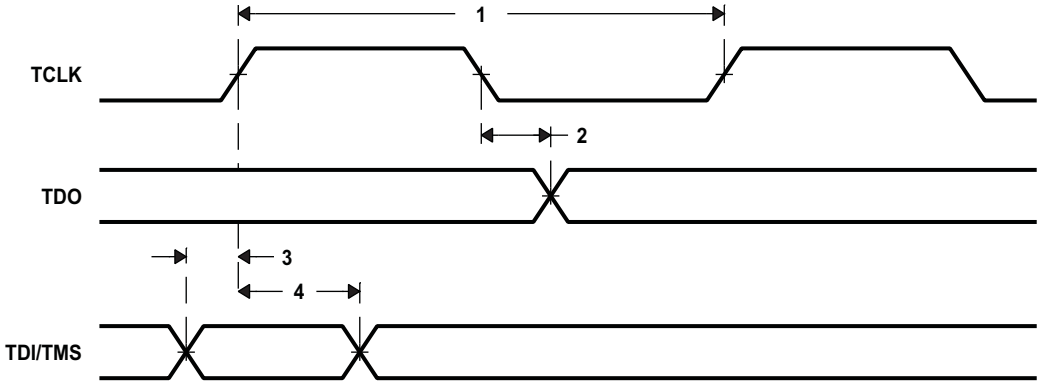

Figure 7-68. JTAG Timing

Table 7-157. Timing Requirements for HS-RTDX

(see Figure 7-69)

NO.			500/625/700		UNIT
			MIN	MAX	
1	$t_{c(TCLK)}$	Cycle time, TCLK	10	20	ns
2	$t_{su(TCLKH-EMUn)}$	Setup time, EMUn input valid before TCLK high	1.5		ns
3	$t_{h(TCLKH-EMUn)}$	Hold time, EMUn input valid after TCLK high	3.0		ns
4	$t_{d(TCLKH-EMUn)}$	Delay time, TCLK high to EMUn output valid	3.0	$t_{c(TCLK)}$ - 3.5	ns

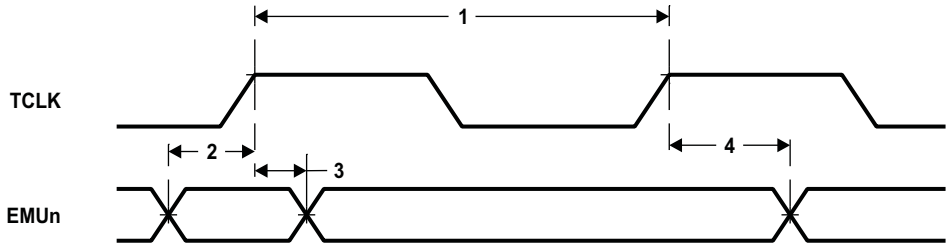

Figure 7-69. HS-RTDX Timing

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8 Mechanical Data

8.1 Thermal Data

Table 8-1 shows the thermal resistance characteristics for the PBGA - CTZ/ZTZ mechanical package.

Table 8-1. Thermal Resistance Characteristics (S-PBGA Package) [CTZ/ZTZ]

NO.			°C/W	AIR FLOW (lfm)(1)
1	$R\Theta_{JC}$	Junction-to-case	0.56	N/A
2	$R\Theta_{JB}$	Junction-to-board	5.1	N/A
3	$R\Theta_{JA}$	Junction-to-free air	12.9	0
4			9.9	150
5			8.5	250
6			7.3	500
7	Psi_{JT}	Junction-to-package top	0.027	0
			0.028	150
			0.028	250
			0.029	500

(1) lfm = linear feet per minute.

8.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device. This data is subject to change without notice and without revision of this document.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320C6472ECTZ	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	-40 to 100	@2007 TI TMS320C6472CTZ
TMS320C6472ECTZ.B	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	-40 to 100	@2007 TI TMS320C6472CTZ
TMS320C6472ECTZ7	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	0 to 0	@2007 TI TMS320C6472CTZ 700
TMS320C6472ECTZ7.B	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	-40 to 100	@2007 TI TMS320C6472CTZ 700
TMS320C6472ECTZA6	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	0 to 0	@2007 TI TMS320C6472CTZA 625
TMS320C6472ECTZA6.B	Active	Production	FCBGA (CTZ) | 737	44 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-245C-72HR	-40 to 100	@2007 TI TMS320C6472CTZA 625

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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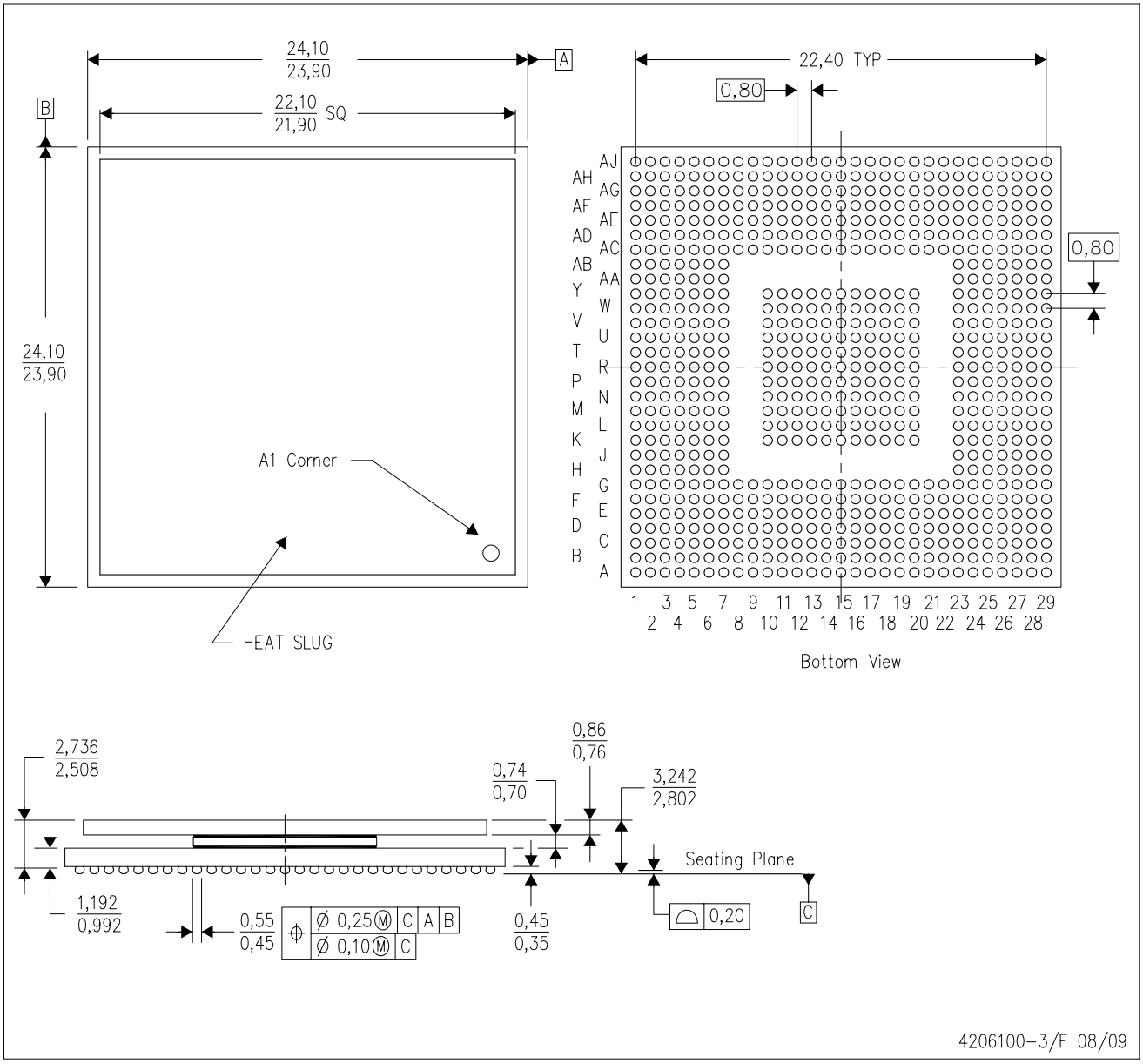
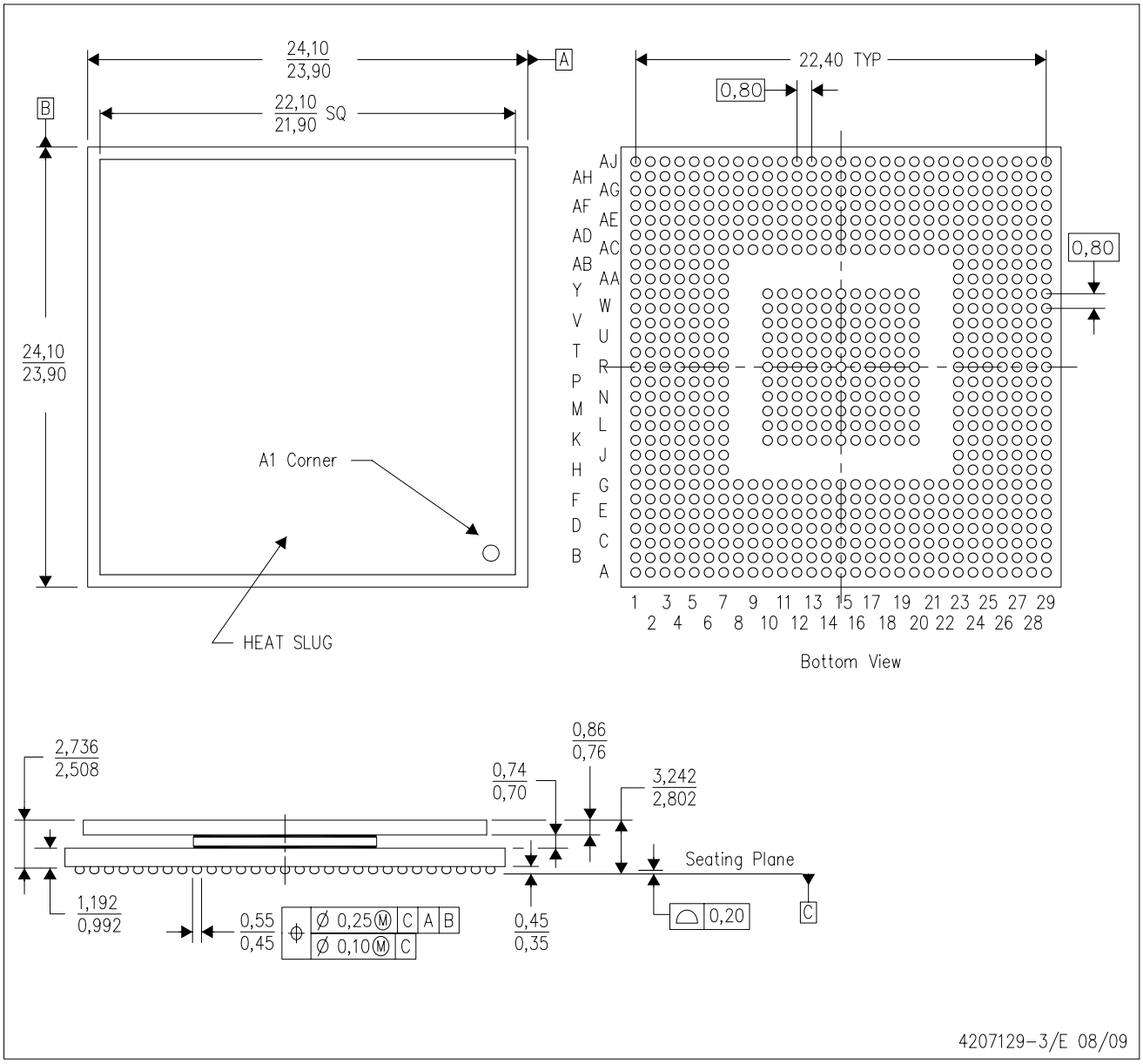
ZTZ (S–PBGA–N737) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. Flip chip application only.
E. This is a Pb–free solder ball design.

CTZ (S–PBGA–N737) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. Flip chip application only.
E. Pb–free die bump and solder ball.

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