# THE DATASHEET OF

TMS320C5545AZQW06

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# TMS320C5545
# Fixed-Point Digital Signal Processor
# Silicon Revision 2.4

# Silicon Errata

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# TMS320C5545 Silicon Revision 2.4

## 1 Introduction

This document describes the known exceptions to the functional specifications for the TMS320C5545 device. For more detailed information on this device, see the device-specific data manual (SPRS853).

The advisory numbers in this document are not sequential. Some advisory numbers have been moved to the next revision and others have been removed and documented in the user's guide. When items are moved or deleted, the remaining numbers remain the same and are not resequenced.

### 1.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C5545AZQW10). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**TMX —** Experimental device that is not necessarily representative of the final device's electrical specifications.

**TMP —** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**TMS —** Fully-qualified production device.

Support tool development evolutionary flow:

**TMDX —** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS —** Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZQW), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "10" is the default 100 MHz device).


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## 1.2 Revision Identification

Figure 1 provides an example of the device markings. The device revision can be determined by the symbols marked on the top of the package.

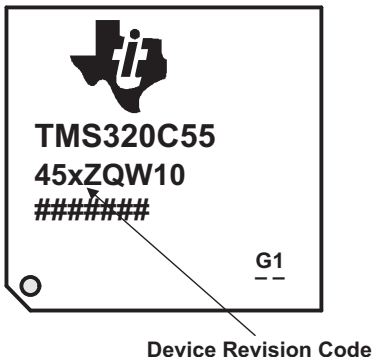


**Figure 1. Example and Device Revision Codes**

Silicon revision is identified by a device revision code marked on the package. The code on the package is of the format C5545x, where "x" denotes the silicon revision. Table 1 lists the information associated with each silicon revision.

**Table 1. Device Revision Codes**

| DEVICE PART NUMBER DEVICE REVISION CODE (x) | SILICON REVISION | PART NUMBERS/COMMENTS |
|---|---|---|
| A | 2.4 | This silicon revision is available as TMS *only*. **TMS**320C5545AZQW |


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# 2 Silicon Revision 2.4 Usage Notes and Known Design Exceptions to Functional Specifications

This section describes the usage notes and advisories that apply to silicon Revision 2.4 of the device.

## *2.1 Usage Notes for Silicon Revision 2.4*

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

### 2.1.1 Master Clock Gating With $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ Asserted

On silicon Revision 2.4, the DSP can disable the Master Clock by setting bit 15 of the PCGCR register (0x1C02). Once the master clock is disabled, it can only be re-enabled by one of the following events:

- Hardware reset being asserted ($\overline{\text{RESET}}$ = low)
- An enabled RTC alarm or periodic interrupt occurring
- The $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ pins being asserted (low) (level-sensitive)

When the master clock is disabled, there are no clocks for edge detection and therefore the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ pins are level-sensitive. This means that a low on either the $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ pin will force bit 15 of the PCGCR register to "0", enabling the master clock. Attempting to write a "1" to bit 15 of the PCGCR register while $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ are asserted will be unsuccessful since re-enabling the clocks has a higher priority than disabling them.

### 2.1.2 Serial Boot Modes Only Support 16-bit Address Mode

On silicon Revision 2.4, the DSP supports the following boot modes: SPI EEPROM, SPI Serial Flash or I2C EEPROM, eMMC/SD/SDHC, UART, and USB. The SPI EEPROM boot supports both 16-bit and 24-bit address modes, while the I2C EEPROM boot mode *only* supports 16-bit address mode.

### 2.1.3 Reserved Bits in the RTC Oscillator Register (RTCOSC) [0x192C]

For proper device operation on silicon Revision 2.4, the "RESERVED" bits in the RTCOSC register (0x192C) should always be set to "zero".


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### 2.1.4 Two 1149.1 JTAG Tap Controllers for JTAG Pins ($\overline{TRST}$, TCK, TMS, TDI, TDO)

The silicon Revision 2.4 device has two internal 1149.1 JTAG Tap controllers but only one set of corresponding JTAG pins ($\overline{TRST}$, TCK, TMS, TDI, TDO).

One TAP controller supports emulation and the other supports JTAG 1149.1 Boundary Scan. Only one of the two TAPs is internally connected to the pins at a time and it is the latched state of the EMU0 pin that determines which TAP is connected. The EMU0 pin is latched on the rising edge of $\overline{TRST}$ and from that time forward the selected tap is connected to the pins. If the latched state of EMU0 is "0", the boundary scan tap is selected and customers may perform boundary scan testing. If the latched state of EMU0 is "1", the DSP's emulation tap is selected and customers may perform emulation with TI's Code Composer Studio™ IDE Emulation Debugger.

**Note:** Because of the device's internal (and recommended external) pullup on the EMU0 pin and the fact that the emulation pods (e.g., XDS560) do not drive the EMU0 pin while $\overline{TRST}$ is driven low-to-high, the emulation tap will normally be the one selected. However, customers who wish to do boundary scan testing will need to have an external pulldown (2 kΩ is recommended), with sufficient strength to overcome the internal pullup, so that the boundary scan tap is connected to the JTAG pins.

### 2.1.5 Bootloader Disables Peripheral Clocks

After hardware reset, on silicon Revision 2.4 of the device, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from the peripheral. At that time, the required peripheral's clock will be enabled for the query and then disabled when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR, except the CPU domain, will be idled. After the boot process is complete, the user is responsible for enabling and programming the required clock configuration for the DSP.

For example, the bootloader disables both the MPORT and FFTHWA. To enable the MPORT and FFT HWA, write 0x000E to the ICR registers and issue an "idle" command.

*Assembly Code Example:*

```
*port(#0x0001) = #(0x000E)
idle
```

*C Code Example:*

```
*(ioport volatile unsigned *)0x0001 = 0x000E;
asm("    idle");    // must add at least one blank before idle in " ".
```

### 2.1.6 SPI Booting Does Not Support 24-Bit Encrypted Reauthoring and Bound to Device

On silicon revision 2.4, the device does not support 24-bit SPI encrypted boot mode. The user must use 16-bit SPI Boot. See Table 2 for the supported boot modes for 16- and 24-bit SPI.

**Table 2. Supported Boot Modes for SPI**

| Boot Mode | Unencrypted | Encrypted | Encrypted and Bound to Device | Encrypted Reauthoring and Bound to Device |
|---|---|---|---|---|
| 16-Bit SPI | Supported | Supported | Supported | Supported |
| 24-Bit SPI | Supported | Not Supported | Not Supported | Not Supported |


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### 2.1.7 eMMC Card of 4GB or Greater Without Valid Boot Image on eMMC/SD0 Slot is Inaccessible After Bootloader Checks for Boot Image

On silicon revision 2.4, the bootloader has a fixed order in which it checks for a valid boot image on each supported boot device: 16-bit SPI EEPROM, 24-bit SPI serial flash, I2C EEPROM, SD/SDHC/eMMC/moviNAND (only Serial Port 0 is checked), UART or USB.

If an eMMC card of 4GB or greater is present on the eMMC/SD0 slot, and the eMMC card does not contain a valid boot image when the bootloader checks for a valid boot image on the eMMC/SD0 slot, then the eMMC card becomes inaccessible until it is power-cycled. When booting from UART or USB, the bootloader checks eMMC before checking UART or USB and therefore the eMMC card becomes inaccessible until power-cycled.

The user is responsible for one of the following:

- Ensure that an eMMC card of 4GB or greater is not checked by the bootloader unless it contains a valid boot image.
- Ensure that the eMMC card without a valid boot image is power-cycled after being checked by the bootloader.

This usage note applies only to the eMMC/SD0 slot. The eMMC/SD1 slot is not affected because booting is not supported using the eMMC/SD1 slot.

### 2.1.8 eMMC Card of 2GB or Less Cannot Boot from Boot Partition Area

On silicon revision 2.4, the bootloader for the device cannot boot from the boot partition area of an eMMC card that is 2GB or less. However, the device can boot from the first data partition formatted in FAT16 or FAT32.

The user must use an eMMC card greater than 2GB to boot from the boot partition area, or the user must boot from the first data partition formatted in FAT16 or FAT32.


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### 2.1.9 SPI Enters a Reset State When Writing to the SPICDR Register

On silicon revision 2.4, the SPI enters a reset state when writing to the SPICDR register. When software writes to the SPICDR register at 0x3000, the software also evaluates and applies the content of the SPICCR register at 0x3001. Thus, if the RST bit (bit 14) of SPICCR is set to a "1" inadvertently, a SPI reset will occur.

Before writing to the SPICDR register, the user must read the SPICCR register and mask out the RST bit with the rest of the bits preserved and write back to SPICCR. Next, write to the SPICDR register.

Following is an example sequence:

- Read SPICCR.
- Mask with 0xBFFF.
- Write back to SPICCR.
- Write to SPICDR.

*C Code Example:*

```
#define SPICDR     *(volatile ioport Uint16*)     (0x3000)
#define SPICCR     *(volatile ioport Uint16*)     (0x3001)
Uint16 temp;
temp = SPICCR;
SPICCR = temp & 0xBFFF;
SPICDR = 0x18;
```

### 2.1.10 SPI Clock State Is Changed When Writing to the SPICDR Register

On silicon revision 2.4, software writes to the SPICCR register (0x3001) when writing to the SPICDR register (0x3000). As a result, the CLKEN bit (bit 15) of SPICCR is set when writing to SPICDR.

The user is responsible for reading the SPICCR register, writing the appropriate value of CLKEN, and preserving the remaining bits back to SPICCR **before** writing to the SPICDR register.


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### 2.1.11 HWAFFT Data and Scratch Pointers Copied as 16-Bit Instead of 23-Bit

On silicon revision 2.4, the HWAFFT uses two data buffers, data and scratch, to pass data to the FFT coprocessor, to store intermediate results, and to store the FFT output. The hwafft_Npts routines available in ROM use pointers to access the data and scratch buffers. These pointers are copied as 16-bit addresses instead of 23-bit addresses when copying from AR0 to AR3 and from AR1 to AR2. The upper bits are not copied which can lead to incorrect FFT results and potential corruption of data incorrectly addressed by the hwafft_Npts routine.

The user is responsible for following one of the following workarounds:

- Execute hwafft_Npts from RAM using the updated hwafft.asm with bug fixes. The hwafft.asm file included with SPRABB6.zip incorporates bug fixes for this errata. The HWAFFT routines stored in ROM cannot be updated and do not incorporate these bug fixes. For reference, hwafft_rom.asm is included in SPRABB6.zip and contains the HWAFFT routines exactly as they exist in the ROM of the affected revisions.
- Execute hwafft_Npts from RAM or from ROM while passing duplicate pointers to the scratch and data buffers to correctly initialize the upper bits of AR0, AR1, AR2, and AR3. The data and scratch buffers can be located in word addresses greater than 0x10000, but the buffers must not cross 16-bit address boundaries (that is, address bits 22–16 must not change). Additionally, if hwafft_512pts is used, data and scratch must not reside at the beginning of a page boundary (that is, word address 0x10000 or 0x20000). This workaround initializes the most significant bits of internal registers AR2 and AR3 such that when the 16-bit address is copied from AR0 and AR1, and provided the assumptions above are satisfied, the full 23-bit address remains correct throughout HWAFFT execution.

  In the user program wherever hwafft_Npts is called, replace:

```
out_sel = hwafft_Npts(data, scratch, fft_flag, scale_flag);
```

  With:

```
out_sel = hwafft_Npts(data, scratch, scratch, data, fft_flag, scale_flag);
```

  In hwafft.h, replace:

```
Uint16 hwafft_Npts(
    Int32 *data,
    Int32 *scratch,
    Uint16 fft_flag,
    Uint16 scale_flag
);
```

  With:

```
Uint16 hwafft_Npts(
    Int32 *data,
    Int32 *scratch,
    Int32 *duplicate_scratch,
    Int32 * duplicate_data,
    Uint16 fft_flag,
    Uint16 scale_flag
);
```

### 2.1.12 USB Oscillator Consumes Power When Core Voltage Is Removed

On silicon revision 2.4, the USB oscillator is disabled by writing a '1' to the USBOSCDIS bit of the USBSCR register. Whenever voltage to the core is removed (for example, during RTC-only mode), the value written to the USBOSCDIS register is lost. If the USB I/O supplies are supplied, the USB oscillator reactivates and consumes power.

To disable the USB oscillator when core voltage is removed, the user must power down all USB I/O supplies (USB_$V_{DDOSC}$, USB_$V_{DDA3P3}$, and USB_$V_{DDPLL}$).


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## 2.2 Silicon Revision 2.4 Known Design Exceptions to Functional Specifications

**Table 3. Silicon Revision 2.4 Advisory List**


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| **Advisory 2.0.1** —USB: Endianess Incompatibility | 12 |
| **Advisory 2.0.4** —I2S: I2S Internal Data Delay | 14 |
| **Advisory 2.0.5** —USB: USB Queue Manager Reads Only 16-bit Address of USB Descriptors | 15 |
| **Advisory 2.0.8** —DMA: DMA Transfer Length Must be a Multiple of 4 x $2^{(\text{Burst Mode})}$ | 16 |
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## Advisory 2.0.1 *USB: Endianess Incompatibility*

**Revision(s) Affected** 2.4

**Details**

The CPU is a word addressable and big endian architecture. The CPU interfaces to the rest of the system through several ports: MPORT, XPORT, DPORT, and IPORT. The DMA transfers data from peripherals to on-chip memory through the MPORT in 32-bit packets. The CPU accesses the peripherals through the XPORT in 8- or 16-bit packets. The CPU accesses external memory in 8-bit (configured through a system register setting), 16-bit (through CPU single word access), or 32-bit (through CPU double-word access). External data accesses occur through the DPORT.

Some peripherals (e.g., USB, LCD, and eMMC/SD) have sensitivity to the data endianess. LCD: Endianess is controlled through software. Default is little endian. MMC/SD: Endianess is controlled through software. Default is big endian. USB: DMA transfer to/from USB buffer is big endian. CPU XPORT access to USB buffer is little endian. USB endianess is not software controllable. The two endianesses of the USB could result in inter byte swap.

Figure 2 shows data paths that could create byte/word swaps.

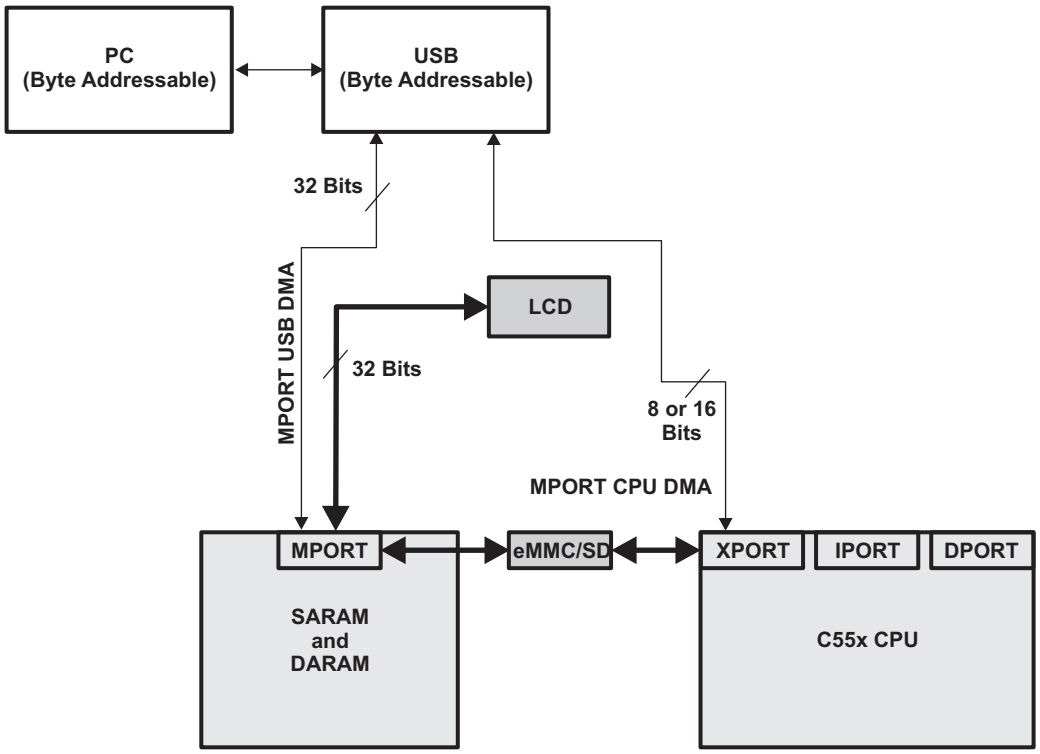


**Figure 2. CPU, USB, LCD, and eMMC/SD Data Paths**


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**Example Case:** Data transfer between the USB and CPU (see Figure 3 and Figure 4).

Data can be read from the USB by the USB DMA or CPU. The USB DMA accesses on-chip memory through the MPORT and only performs a 32-bit read while the CPU can perform a 16-bit read via the XPORT. When USB DMA transfers data from the USB buffers to on-chip memory, the data transfer is 32-bits and is handled in big endian fashion, so no data swap occurs (see Figure 3). However, when the CPU, through the XPORT, accesses the USB buffers, the data is accessed 16-bits at a time in little endian fashion resulting in an inter byte swap (see the Figure 4).

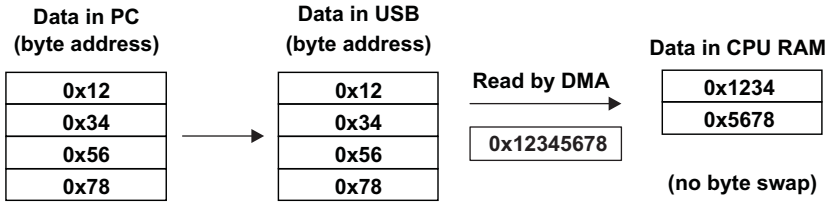


**Figure 3. USB DMA Read**

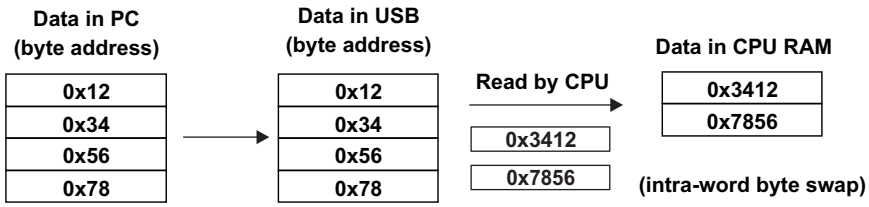


**Figure 4. CPU Read From USB**

**Workaround(s)**

To correct this issue, software is required to fix the intra-word byte swap on the data prior to processing on the device CPU.


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## Advisory 2.0.4 *I2S: I2S Internal Data Delay*

**Revision(s) Affected** 2.4

**Details**

The I2S module has an internal delay for the data transmit/receive path that varies depending on the settings of the Pack bit and Word Length in the I2S Control Register and the FSDIV in the Sample Rate Generator Register.

Table 4 shows the transmit path internal data delays. Feedback path refers to an I2S transmit pin that is externally connected to the I2S receive pin.

**Table 4. Transmit Path Internal Data Delays**

| PACK | DATA DELAY |
|---|---|
| 1 | The first five transmit frames will be zero data. On the sixth transmit frame, the data written to the transmit register will be shifted out on the DX pin. |
| 0 | The first three transmit frames will be zero data. On the fourth transmit frame, the data written to the transmit register will be shifted out on the DX pin. |

Table 5 shows the receive path internal data delays:

**Table 5. Receive Path Internal Data Delays**

| WORD LENGTH | DATA DELAY |
|---|---|
| 8-bit | The RX data registers will contain zero data for the first two frames. |
| 10, 12, 14, and 16-bit | The RX data registers will contain zero data for the first three frames. |
| 18, 20, 24, and 32-bit | The RX data registers will contain zero data for the first two frames. |

Table 6 shows the feedback path internal data delays:

**Table 6. Feedback Path Internal Data Delays**

| PACK | WORD LENGTH | FSDIV BITS I2SSRATE.[5:3] | DATA DELAY |
|---|---|---|---|
| 1 | 8-bit | 000 | Data received on the 7th sample |
| | 8-bit | 001 – 101 | Data received on the 6th sample |
| | 10-, 12-, 14-, and 16-bit | 001 | Data received on the 5th sample |
| | 10-, 12-, 14-, and 16-bit | 010 – 101 | Data received on the 4th sample |
| 0 | 8-, 10-, 12-, 14-, 16-, 18-, 20-, 24-, and 32-bit | 000 – 101 | Data received on the 3rd interrupt |

**Workaround(s)** Zero data should be Ignored.



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## Advisory 2.0.5 *USB: USB Queue Manager Reads Only 16-bit Address of USB Descriptors*

**Revision(s) Affected** 2.4

**Details** The device has 23-bit address space but the USB Queue Manager (QMGR) is a 32-bit register that holds the address of the USB descriptors. A descriptor itself is a structure with information about the addresses of the source/destination data buffers and their sizes. The address of a particular descriptor is written to the QMGR register for a particular DMA endpoint. The CPU writes the address of a descriptor to the QMGR register for a for a DMA endpoint. The QMGR fires the USB DMA to read the descriptor at the address pointed to in the QMGR register and sets up the DMA endpoints for future transfers. When a USB host connects and performs a transfer, the QMGR copies the address of the descriptor to a completed queue. Upon receiving the USB interrupt, the USB driver should read the 32-bit descriptor address in the QMGR completion queue to determine which DMA endpoint has completed transferring data. Even though the CPU can write a 32-bit value into the QMGR register, it can only read the lower 16-bits of this register. Thus, the descriptor can only be allocated in the CPU memory map to the same lower 16-bit address and all descriptors must be placed in one contiguous block of 64K words in SARAM.

For example:

- USB descriptor A is located at 0x008000
- USB descriptor B is located at 0x018000

The descriptor A and B will be considered the same descriptor.

**Workaround(s)** The USB descriptors should be placed in ONE CONTIGUOUS BLOCK of 64K words ($2^{16}$) in memory.


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## Advisory 2.0.8 *DMA: DMA Transfer Length Must be a Multiple of 4 x 2(Burst Mode)*

**Revision(s) Affected**

2.4

**Details**

If the transfer length register has a value that is zero or *not* a multiple of 4 x 2(Burst Mode) when the DMA transfer begins, it will cause an unexpected operation of DMA.

While the DMA transfers 32-bit words from a source address to a destination address, the value in the DMA transfer length register is the length in bytes. For example, if the total DMA transfer length is 4 32-bit words and the burst size = 1, 4 x 4 = 16 should be written to the DMA transfer length register. The burst size should also be considered. Burst size is the minimum data transfer size; therefore, the total DMA Transfer Length should be 4 x 2(Burst Mode). For more details, see Table 7.

**Table 7. DMA Transfer Lengths**

| BURST MODE | BURST SIZE (32-BIT WORD) | DMA TRANSFER LENGTH (BYTES) |
|---|---|---|
| 0 | 1 | Multiple of 4 (minimum 4) |
| 1 | 2 | Multiple of 8 (minimum 8) |
| 2 | 4 | Multiple of 16 (minimum 16) |
| 3 | 8 | Multiple of 32 (minimum 32) |
| 4 | 16 | Multiple of 64 (minimum 64) |

**Workaround(s)**

Write only a multiple of 4 x 2(Burst Mode) to the DMA transfer register before the DMA starts.



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## Advisory 2.0.10 *USB: CPPI Receive Starvation Interrupt*

**Revision(s) Affected** 2.4

**Details** When an endpoint is enabled for receive transfer(s) that will be serviced via CPPI DMA and data has been received prior to allocating the DMA resource, the DMA will generate a starvation interrupt to notify the application a lack of resource (starvation) in anticipation that the application will furnish the required resource. Once the starvation occurs, the CPPI DMA continues generating interrupts periodically whenever the host tries to send data. It does not stop until the application furnishes a resource.

The USB starvation interrupt is always enabled and cannot be masked off at the USB controller level. Since the DMA continues to generate the starvation interrupt periodically and there exists no capability to mask the starvation interrupt at the USB controller level, the CPU is forced either to fully service the DMA interrupt as it is received or disable all USB interrupts at the CPU level. Disabling the entire USB interrupt might not be the desired option since the CPU needs to be aware of other USB interrupts that are more critical.

**Workaround(s)** Dedicated data receiving buffers are recommended. The data buffers should be allocated and available to the CPPI DMA during USB initialization. The required data buffer size is highly dependent on USB host applications. For Windows XP USB Mass Storage device driver, it is recommended to allocate at least 64 KB (128 descriptors; 128*512 = 64 KB) of data buffer space.


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## Advisory 2.0.13 *USB Controller in TI's C55xx Device Responds Abnormally to Certain Control Out Transfers*

**Revision(s) Affected** 2.4

**Details**

USB is in device mode and connected to a standard PC (host) and is operating in full speed mode. The problem has been observed when using Control-OUT transfers with odd byte payload. USB engine occasionally provides abnormal response in the status phase of Control-OUT transfers with data payload. The abnormal response seen is, the status phase should contain 0-length IN packet, but occasionally 1-byte IN packets are sent by the device.

**Issues:**

Whenever host sends an odd byte control OUT transfer to device, the out packet gets written into FIFO and then, FIFO contents will be read by the device CPU (through bridge responsible for bus and protocol conversion, etc.). Since this is an odd byte transfer, the last byte needs to be read by switching to byte mode access, but in the C55xx device topology the read byte enable signal which is supposed to generate the byte enables for performing odd byte read is tied off (10'h2) in design. This will force all reads and writes to be half words (2 bytes). The writes are still okay, as their byte enables come from the byte enable signal directly through software configurations, but for reads considering byte enable signal is tied-off this will always result in 2 bytes read, even if there is only 1 byte of data that needs to be read. This results in non-clearing of FIFO pointers.

Since FIFO pointers were not cleared, and gets cleared only when the DATAEND and RXPKTRDY bit is set, there exists a race condition when DATAEND & RXPKYRDY is set, FIFO pointers are getting cleared and at the same time IN packet is received. Due to this race condition, where IN packet is received while FIFO pointers getting cleared, the data in the FIFO is sent out during the status phase.

The above mentioned issue will not exist with even bytes OUT transfers. For even byte OUT packets, as the need doesn't exist to perform a byte mode switch to accomplish byte read, and device needs to perform half-word read, this in turn will clear the FIFO pointers. Hence, the device will respond with the correct status information.

**Workaround(s)**

With the following workaround solution the issue will recede.

1. Once the control OUT packet is received, perform read of all the odd bytes from the FIFO, considering read is always half word (16 bits) the FIFO pointers will not get cleared to zero, but instead will move to 'h7F (negative one). This can be observed in the count register (COUNT_INDEX0) register.
2. After the first read sequence, instead of setting ServiceRxPktRdy and DataEnd bit, set FIFO_Access bit in TestMode Register (Addr = 840Eh).
3. Setting the FIFO Access bit will readjust the FIFO pointers. That is, USB host side FIFO pointer will set to previous odd bytes transfer plus one and CPU side FIFO pointer will be set to zero. To illustrate further, say if the odd bytes transfer is 63 bytes then the host side FIFO pointer will be set to 64 whereas CPU side FIFO pointer will reset to zero.
4. Configuring the FIFO access bit to '1' will generate an interrupt and RxPktRdy will be set.
5. The generated interrupt (from FIFO Access bit) needs to be disabled and the corresponding interrupt flag needs to be cleared.
6. As next step software needs to again perform dummy read from the FIFO, this will clear the FIFO pointers.
7. After the dummy reads, set ServiceRxPktRdy and DataEnd bit.
8. Device will respond with the correct status packet.


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The below Pseudo code provides workaround implementation details.

```
// Read endpoint-0 Buffer Function
void USB_readEP0Buf( .. )
{
// Declarations
    .
    .
    .

    /* select EP0 registers */
    usbRegisters->INDEX_TESTMODE &= ~(CSL_USB_INDEX_TESTMODE_EPSEL_MASK);

    /* get Receive packet size */
    packetSize = ((usbRegisters->COUNT0_INDX) &
                  CSL_USB_COUNT0_INDX_EP0RXCOUNT_MASK);

    // perform 1st read sequence
    for(count = 0; count < (packetSize)/2; count++)
    {
        *pBuf = usbRegisters->FIFO0R1;
        pBuf++;
    }

    // this will perform last half word read in first read sequence.

    if (packetSize & 0x1)
    {
        *pBuf = usbRegisters->FIFO0R1 & 0xFF;
    }
    // Check if the packet size is odd bytes or even bytes.
    // for odd bytes the second read operations are performed.
    // If it's even bytes then do not perform 2nd read sequence.

    if(packetSize & 0x1) //if True then its odd bytes transfer
    {
        // following operations are atomic
        value = IRQ_globalDisable();

        // Set FIFO access bit in Test mode register

        usbRegisters->INDEX_TESTMODE |=
                CSL_USB_INDEX_TESTMODE_FIFO_ACCESS_MASK;

        // perform the second sequence of read operations.

        for(count = 0; count < (packetSize)/2; count++)
        {
            *TempBuf = usbRegisters->FIFO0R1;
            TempBuf++;
        }

        if (packetSize & 0x1)
        {
            *TempBuf = usbRegisters->FIFOR1;
        }

        // Clear USB interrupt flags

        // enable the hardware interrupt
        IRQ_globalRestore(value);
        }
}
```

The above procedure will result in the device sending the correct status information that is zero length packet to the USB host.


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# Revision History

**Changes from A Revision (July 2015) to B Revision** **Page**

- Updated/Changed PART NUMBERS in Table 1 ..... 5
- Updated/Changed intro paragraph of Section 2.1.6 ..... 7
- Updated/Changed 24-Bit SPI Encrypted and Encrypted and Bound to Device from "Supported" to "*Not Supported*" in Table 2 ..... 7


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