WINSOURCE ELECTRONICS

THE DATASHEET OF

TMS320C54V90BPGE

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- **Provides Two-Chip Modem Solution**
- **Data Rates from 300 bps to 56 Kbps**
- **Data Modulation Standards**
  V.90, V.34, V.32bis, V.32, V.22bis, V.22, V.23, V.21 and V.23 Reversible (Minitel), Bell 212, Bell 103
- **FAX Capabilities**
  - **ITU−T V.17, V.29, V.27ter Modulations**
  - **TIA/EIA 578 Class 1 Interface**
- **V.42 or MNP Class 3 and 4 Error Control and V.42bis Compression**
- **Caller ID**
- **Field-Proven Modem Algorithms Give Highest Performance, Reliability, and Compatibility**
- **Non-Volatile EEPROM Configuration Storage**
- **Worldwide Telecom Approvals**
- **Parallel Phone Support Including Parallel Phone Detection**
- **Parallel Phone Exclusion Relay Control**
- **Protected Against Surge and Overvoltage on the Telephone Line**
- **Parallel Host Port Interface Supports a Variety of Industry Standard Busses**
- **Integral Serial Interface (UART)**
- **Autobaud on Serial DTE Interface**
- **State-of-the-Art Integrated Transformerless Silicon DAA for Phone Line Interconnection**
- **40K x 16-Bit Dual-Access On-Chip RAM**
- **128K x 16-Bit On-Chip ROM**
- **Applications**
  - **Embedded Systems**
  - **Set-Top Boxes**
  - **Gaming Consoles**
  - **Internet Appliances**
  - **Portable Devices (PDAs, Digital Cameras)**
  - **Remote Data Collection, Point-of-Sale**
  - **Meter Reading, Utility Monitoring**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank Switching**
  - **On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Enhanced 8-Bit Parallel Host-Port Interface (HPI8)**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **8.5-ns Single-Cycle Fixed-Point Instruction Execution Time (117.96 MIPS) or 17-ns Instruction Execution Time (58.98 MIPS) for 3.3-V Power Supply (1.5-V Core)**
- **Available in a 144-Pin Plastic Low-Profile Quad Flatpack (LQFP) (PGE Suffix) and a 144-Pin Ball Grid Array (BGA) (GGU Suffix)**

description

The TMS320C54V90 is used to implement a full-featured, high-performance modem technology, intended for use in embedded systems and similar applications. This highly integrated solution implements a complete modem using only two chips: the TMS320C54V90 DSP with on-chip RAM and ROM, and the Si3016 line-side DAA.

The modem can connect to a host system serially (RS-232 functionality), or as an 8-bit peripheral to the processor in a host system. The TMS320C54V90 uses a standard Digital Signal Processor (DSP) and proprietary firmware to perform all the modem signal processing, the V.42/V.42bis compression, and AT commands interpretation for modem control functions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Note: Human Body Model ESD test performance for this product was demonstrated to be ±1.5 kV during product qualification. Industry standard test method used was IEA/JESD22-A114. Adherence to ESD handling precautionary procedures is advised at all times.

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

The TMS320C54V90 also uses the latest silicon DAA technology. This technology does not require a transformer and results in lower cost, lower power, and a smaller area for the DAA function.

For serial interface applications, an integrated UART implements the serial interface with no additional hardware.

part numbers

The following orderable part numbers apply to the TMS320C54V90 device:

- TMS320C54V90BPGE − Selects QFP-packaged DSP
- TMS320C54V90BGGU − Selects BGA-packaged DSP
- Si3016−KS − Selects DAA shipped in tubes
- Si3016−KSR − Selects DAA shipped in tape and reel

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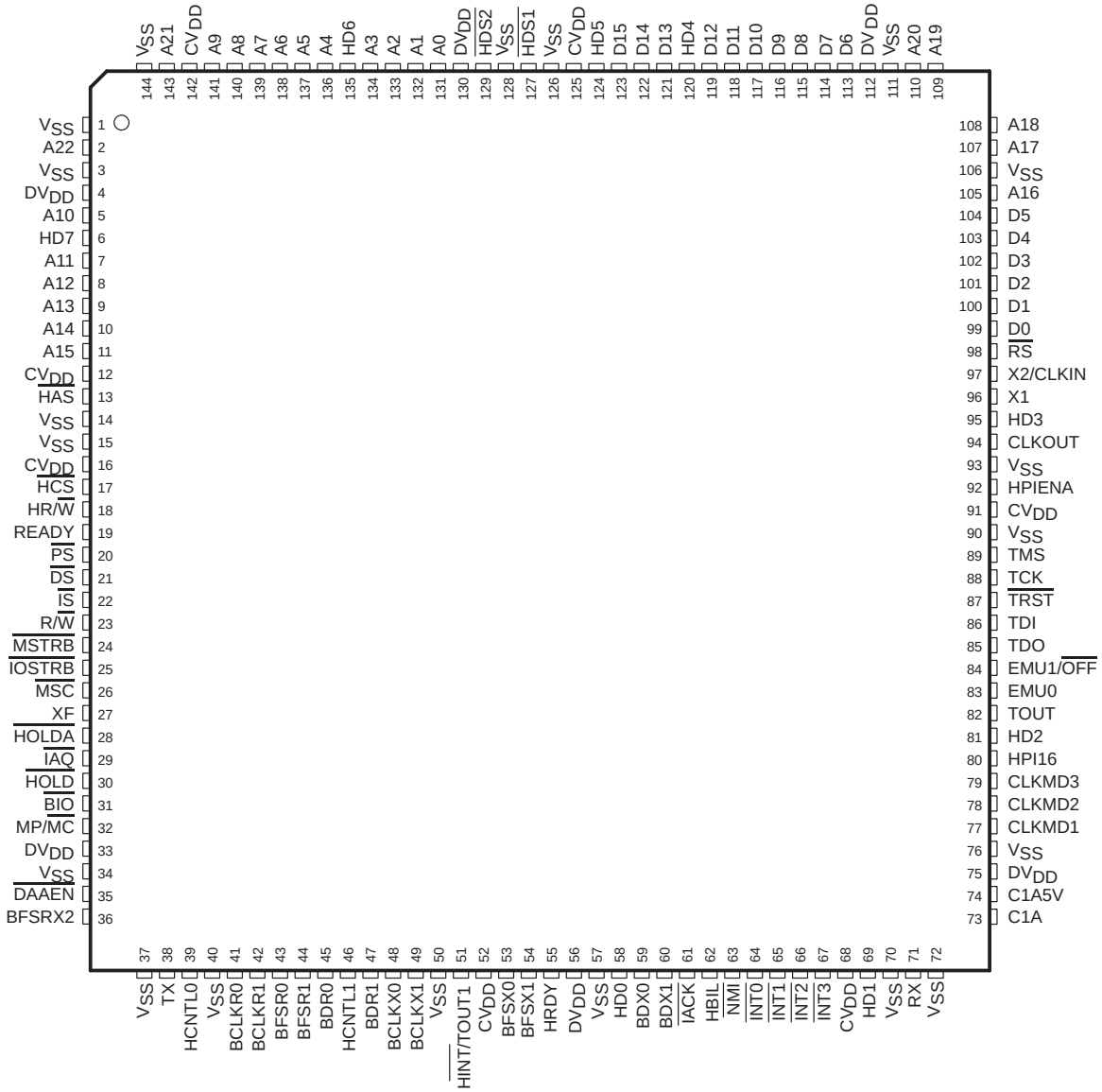
REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
*	July 2001	Advance Information	Original
A	September 2001	Advance Information	Changed the DAAEN signal to a true low, $\overline{\text{DAAEN}}$. Added Schottky diode (D6) schematic diagram and BOM. Changed name of core and I/O power supplies. Added DAA power supply description.
B	October 2002	Advance Information	Updated schematic diagrams, electrical characteristics, and recommended operating conditions.
C	March 2003	Production Data	Updated AT command tables, schematic diagrams, electrical characteristics, and recommended operating conditions.
D	April 2003	Production Data	Updated AT command tables.
E	June 2003	Production Data	Revised orderable part numbers on page 2. Revised Table 2 and Figure 22.

REVISION HISTORY (Continued)

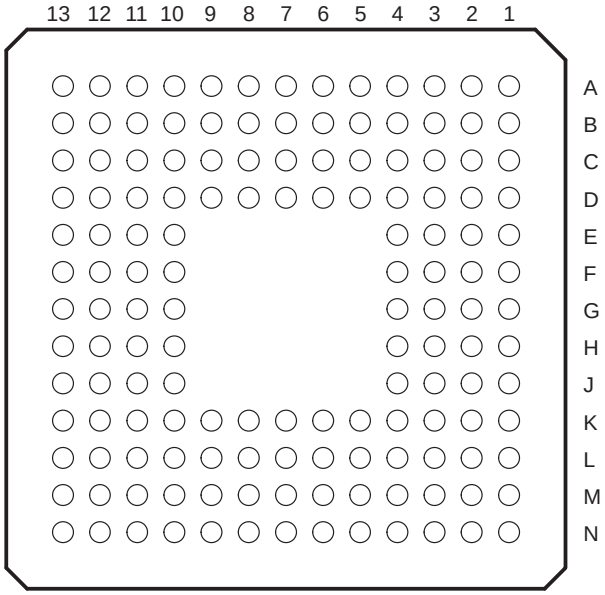
REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
F	October 2003	Production Data	Revised orderable part numbers on page 2. Revised Table 2, Table 14, Table 15, Table 19, Table 23, and Table 24. Revised “country code setting” section on page 45. Revised schematic diagrams on page 56 and page 57. Updated Figure 22. Changed “operating case temperature range” from “−40°C to 100°C” to “0°C to 100°C” in “absolute maximum ratings” section. Updated T_C, V_{IH}, and V_{IL} in “recommended operating conditions” table.

PGE PACKAGE†
(TOP VIEW)



† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

GGU PACKAGE
(BOTTOM VIEW)



The pin assignments table to follow lists each signal name and BGA ball number for the TMS320C54V90 (144-pin BGA) package which is footprint compatible with the TMS320VC5402.

Pin Assignments for the TMS320C54V90GGU (144-Pin BGA) Package†

SIGNAL QUADRANT 1	BGA BALL #	SIGNAL QUADRANT 2	BGA BALL #	SIGNAL QUADRANT 3	BGA BALL #	SIGNAL QUADRANT 4	BGA BALL #
V_{SS}	A1	C1A	N13	V_{SS}	N1	A19	A13
A22	B1	C1A5V	M13	TX	N2	A20	A12
V_{SS}	C2	DV_{DD}	L12	HCNTL0	M3	V_{SS}	B11
DV_{DD}	C1	V_{SS}	L13	V_{SS}	N3	DV_{DD}	A11
A10	D4	CLKMD1	K10	BCLKR0	K4	D6	D10
HD7	D3	CLKMD2	K11	BCLKR1	L4	D7	C10
A11	D2	CLKMD3	K12	BFSR0	M4	D8	B10
A12	D1	HPI16	K13	BFSR1	N4	D9	A10
A13	E4	HD2	J10	BDR0	K5	D10	D9
A14	E3	TOUT	J11	HCNTL1	L5	D11	C9
A15	E2	EMU0	J12	BDR1	M5	D12	B9
CV_{DD}	E1	$\overline{EMU1/OFF}$	J13	BCLKX0	N5	HD4	A9
$\overline{HAS}$	F4	TDO	H10	BCLKX1	K6	D13	D8
V_{SS}	F3	TDI	H11	V_{SS}	L6	D14	C8
V_{SS}	F2	$\overline{TRST}$	H12	$\overline{HINT/TOUT1}$	M6	D15	B8
CV_{DD}	F1	TCK	H13	CV_{DD}	N6	HD5	A8
$\overline{HCS}$	G2	TMS	G12	BFSX0	M7	CV_{DD}	B7
$HR/\overline{W}$	G1	V_{SS}	G13	BFSX1	N7	V_{SS}	A7
READY	G3	CV_{DD}	G11	HRDY	L7	$\overline{HDS1}$	C7
$\overline{PS}$	G4	HPIENA	G10	DV_{DD}	K7	V_{SS}	D7
$\overline{DS}$	H1	V_{SS}	F13	V_{SS}	N8	$\overline{HDS2}$	A6
$\overline{IS}$	H2	CLKOUT	F12	HD0	M8	DV_{DD}	B6
$R/\overline{W}$	H3	HD3	F11	BDX0	L8	A0	C6
$\overline{MSTRB}$	H4	X1	F10	BDX1	K8	A1	D6
$\overline{IOSTRB}$	J1	X2/CLKIN	E13	$\overline{IACK}$	N9	A2	A5
$\overline{MSC}$	J2	$\overline{RS}$	E12	HBIL	M9	A3	B5
XF	J3	D0	E11	$\overline{NMI}$	L9	HD6	C5
$\overline{HOLDA}$	J4	D1	E10	$\overline{INT0}$	K9	A4	D5
$\overline{IAQ}$	K1	D2	D13	$\overline{INT1}$	N10	A5	A4
$\overline{HOLD}$	K2	D3	D12	$\overline{INT2}$	M10	A6	B4
$\overline{BIO}$	K3	D4	D11	$\overline{INT3}$	L10	A7	C4
$MP/\overline{MC}$	L1	D5	C13	CV_{DD}	N11	A8	A3
DV_{DD}	L2	A16	C12	HD1	M11	A9	B3
V_{SS}	L3	V_{SS}	C11	V_{SS}	L11	CV_{DD}	C3
$\overline{DAAEN}$	M1	A17	B13	RX	N12	A21	A2
BFSRX2	M2	A18	B12	V_{SS}	M12	V_{SS}	B2

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

TMS320C54V90 Terminal Functions

TERMINAL NAME	I/O†	DESCRIPTION
EXTERNAL MEMORY INTERFACE PINS		
A22 (MSB) A21 A20 A19 A18 A17 A16	O/Z	Parallel address bus A22 (MSB) through A0 (LSB). The lower sixteen address pins—A0 to A15—are multiplexed to address all external memory (program, data) or I/O, while the upper seven address pins—A22 to A16—are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when $\overline{OFF}$ is low.
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)		A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB) — I — These pins can be used to address internal memory via the HPI when the HPI16 pin is high.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB) — I/O — Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. The data bus also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
INITIALIZATION, INTERRUPT, AND RESET PINS		
$\overline{IACK}$	O/Z	Interrupt acknowledge signal. $\overline{IACK}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–0. $\overline{IACK}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{INT3}$	I	External user interrupt inputs. $\overline{INT0}$−$\overline{3}$ are prioritized and maskable via the interrupt mask register and interrupt mode bit. The status of these pins can be polled by way of the interrupt flag register.
$\overline{NMI}$	I	Nonmaskable interrupt. $\overline{NMI}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.

† I = Input, O = Output, Z = High-impedance, S = Supply

TMS320C54V90 Terminal Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET PINS (CONTINUED)		
RS	I	Reset input. RS causes the DSP to terminate execution and causes a re-initialization of the CPU and peripherals. When RS is brought to a high level, execution begins at location 0FF80h of program memory. RS affects various registers and status bits.
MP/MC	I	Microprocessor/microcomputer mode select pin. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 16K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/MC bit of the PMST register can override the mode that is selected at reset.
MULTIPROCESSING AND GENERAL-PURPOSE PINS		
BIO	I	Branch control input. A branch can be conditionally executed when BIO is active. If low, the processor executes the conditional instruction. The BIO condition is sampled during the decode phase of the pipeline for XC instruction, and all other instructions sample BIO during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or as a general-purpose output pin. XF goes into the high-impedance state when OFF is low, and is set high at reset.
MEMORY CONTROL PINS		
DS PS IS	O/Z	Data, program, and I/O space select signals. DS, PS, and IS are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. Placed into a high-impedance state in hold mode. DS, PS, and IS also go into the high-impedance state when OFF is low.
MSTRB	O/Z	Memory strobe signal. MSTRB is always high unless low-level asserted to indicate an external bus access to data or program memory. Placed in high-impedance state in hold mode. MSTRB also goes into the high-impedance state when OFF is low.
READY	I	Data ready input. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/W	O/Z	Read/write signal. R/W indicates transfer direction during communication to an external device. Normally in read mode (high), unless asserted low when the DSP performs a write operation. Placed in high-impedance state in hold mode. R/W also goes into the high-impedance state when OFF is low.
IOSTRB	O/Z	I/O strobe signal. IOSTRB is always high unless low level asserted to indicate an external bus access to an I/O device. Placed in high-impedance state in hold mode. IOSTRB also goes into the high-impedance state when OFF is low.
HOLD	I	Hold input. HOLD is asserted to request control of the address, data, and control lines. When acknowledged by the C54x, these lines go into high-impedance state.
HOLDA	O/Z	Hold acknowledge signal. HOLDA indicates that the DSP is in a hold state and that the address, data, and control lines are in a high-impedance state, allowing the external memory interface to be accessed by other devices. HOLDA also goes into the high-impedance state when is OFF low.
MSC	O/Z	Microstate complete. MSC indicates completion of all software wait states. When two or more software wait states are enabled, the MSC pin goes active at the beginning of the first software wait state, and goes inactive (high) at the beginning of the last software wait state. If connected to the ready input, MSC forces one external wait state after the last internal wait state is completed. MSC also goes into the high impedance state when OFF is low.
IAQ	O/Z	Instruction acquisition signal. IAQ is asserted (active low) when there is an instruction address on the address bus and goes into the high-impedance state when OFF is low.

† I = Input, O = Output, Z = High-impedance, S = Supply

TMS320C54V90 Terminal Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
OSCILLATOR/TIMER PINS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. CLKOUT also goes into the high-impedance state when OFF is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode external/internal input signals. CLKMD1−CLKMD3 allows you to select and configure different clock modes such as crystal, external clock, various PLL factors.
X2/CLKIN	I	Input pin to internal oscillator from the crystal. If the internal oscillator is not being used, an external clock source can be applied to this pin. The internal machine cycle time is determined by the clock operating mode pins (CLKMD1, CLKMD2 and CLKMD3).
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when OFF is low.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT cycle wide. TOUT also goes into the high-impedance state when OFF is low.
TOUT1	I/O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer1 counts down past zero. The pulse is a CLKOUT cycle wide. The TOUT1 output is multiplexed with the HINT pin of the HPI, and TOUT1 is only available when the HPI is disabled.
MULTICHANNEL BUFFERED SERIAL PORT PINS		
BCLKR0 BCLKR1	I/O/Z	Receive clock input. CLKR serves as the serial shift clock for the buffered serial port receiver. BCLKRX2 is McBSP2 transmit AND receive clock. This pin is optionally bondable as C1A (see DAA section).
BDR0 BDR1	I	Serial data receive input.
BFSR0 BFSR1 BFSRX2	I/O/Z	Frame synchronization pulse for receive input. The FSR pulse initiates the receive data process over DR. BFSRX2 is McBSP2 transit AND receive frame sync
BCLKX0 BCLKX1	I/O/Z	Transmit clock. CLKX serves as the serial shift clock for the buffered serial port transmitter. The CLKX pins are configured as inputs after reset. CLKX goes into the high-impedance state when OFF is low.
BDX0 BDX1	O/Z	Serial data transmit output. DX is placed in the high-impedance state when not transmitting, when RS is asserted or when OFF is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit output. The FSX pulse initiates the transmit data process over DX. The FSX pins are configured as inputs after reset. FSX goes into the high-impedance state when OFF is low.
INTEGRATED DAA		
C1A	I/O	DAA I/O connection.
C1A5V	S	Dedicated 5.0-V power supply for I/O pin C1A.
DAAEN	I	DAA Enable Input. Enables the DAA when low.
UART		
TX	O	UART asynchronous serial transmit data output.
RX	I	UART asynchronous serial receive data input.

† I = Input, O = Output, Z = High-impedance, S = Supply

TMS320C54V90 Terminal Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
HOST PORT INTERFACE PINS		
A0−A15	I	These pins can be used to address internal memory via the HPI when the HPI16 pin is HIGH.
D0−D15	I/O	These pins can be used to read/write internal memory via the HPI when the HPI16 pin is high. The sixteen data pins, D0 to D15, are multiplexed to transfer data between the core CPU and external data/program memory, I/O devices, or HPI in 16-bit mode. The data bus is placed in the high-impedance state when not outputting or when $\overline{RS}$ or $\overline{HOLD}$ is asserted. The data bus also goes into the high-impedance state when $\overline{OFF}$ is low. The data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The data bus holders of the DSP are disabled at reset, and can be enabled/disabled via the BH bit of the BSCR.
HD0−HD7	I/O/Z	Parallel bidirectional data bus. These pins can also be used as general-purpose I/O pins when the HPI16 pin is high. HD0−HD7 is placed in the high-impedance state when not outputting data or when $\overline{OFF}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the DSP, the bus holders keep the pins at the logic level that was most recently driven. The HPI data bus holders are disabled at reset, and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control inputs. These inputs select a host access to one of the three HPI registers. (Pullup only enabled when HPIENA=0, HPI16=1)
HBIL	I	Byte identification input. Identifies first or second byte of transfer. (Pullup only enabled when HPIENA=0, invalid when HPI16=1)
$\overline{HCS}$	I	Chip select input. This pin is the select input for the HPI, and must be driven low during accesses. (Pullup only enabled when HPIENA=0, or HPI16=1)
$\overline{HDS1}$ $\overline{HDS2}$	I	Data strobe inputs. These pins are driven by the host read and write strobes to control transfers. (Pullup only enabled when HPIENA=0)
$\overline{HAS}$	I	Address strobe input. Address strobe input. Hosts with multiplexed address and data pins require this input, to latch the address in the HPIA register. (Pullup only enabled when HPIENA=0)
HR/$\overline{W}$	I	Read/write input. This input controls the direction of an HPI transfer. (Pullup only enabled when HPIENA=0)
HRDY	O/Z	Ready output. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{HINT}$	O/Z	Interrupt output. This output is used to interrupt the host. When the DSP is in reset, this signal is driven high. $\overline{HINT}$ can also be used for timer 1 output (TOUT1), when the HPI is disabled. The signal goes into the high-impedance state when $\overline{OFF}$ is low. (invalid when HPI16=1)
HPIENA	I	HPI enable input. This pin must be driven high during reset to enable the HPI. An internal pulldown resistor is always active and the HPIENA pin is sampled on the rising edge of $\overline{RS}$. If HPIENA is left open or driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the DSP is reset.
HPI16	I	HPI 16-bit Select Pin. HPI16=1 selects the non-multiplexed mode. The non-multiplexed mode allows hosts with separate address/data buses to access the HPI address range via the 16 address pins A0–A15. 16-bit Data is also accessible through pins D0–D15. HOST-to-DSP and DSP-to-HOST interrupts are not supported. There are no HPIC and HPIA registers in the non-multiplexed mode since there are HCNTRL0,1 signals available. Internally pulled low.

† I = Input, O = Output, Z = High-impedance, S = Supply

TMS320C54V90 Terminal Functions (Continued)

TERMINAL NAME	I/O†	DESCRIPTION
SUPPLY PINS		
CV_{DD}	S	$+V_{DD}$. Dedicated 1.5-V power supply for the core CPU.
DV_{DD}	S	$+V_{DD}$. Dedicated 3.3-V power supply for I/O pins.
V_{SS}	S	Ground.
TCK	I	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input, pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{OFF}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{TRST}$	I	IEEE standard 1149.1 test reset. $\overline{TRST}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{TRST}$ is not connected or driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator 0 pin. When $\overline{TRST}$ is driven low, EMU0 must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of IEEE standard 1149.1 scan system.
EMU1/$\overline{OFF}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output via IEEE standard 1149.1 scan system. When $\overline{TRST}$ is driven low, EMU1/$\overline{OFF}$ is configured as $\overline{OFF}$. The EMU1/$\overline{OFF}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). Thus, for the $\overline{OFF}$ feature, the following conditions apply: $\overline{TRST}$=low, EMU0=high, EMU1/$\overline{OFF}$ = low

† I = Input, O = Output, Z = High-impedance, S = Supply

pin descriptions: Si3016

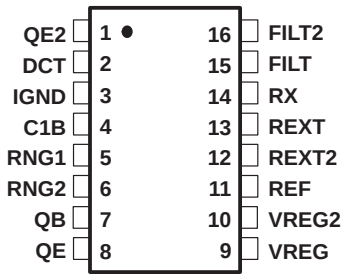


Table 1. Si3016 Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	QE2	**TRANSISTOR EMITTER 2.** Connects to the emitter of Q4.
2	DCT	**DC TERMINATION.** Provides DC termination to the telephone network.
3	IGND	**ISOLATED GROUND.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**ISOLATION CAPACITOR 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side module.
5	RNG1	**RING 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3016.
6	RNG2	**RING 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3016.
7	QB	**TRANSISTOR BASE.** Connects to the base of transistor Q3. Used to go on/off-hook.
8	QE	**TRANSISTOR EMITTER.** Connects to the emitter of transistor Q3. Used to go on/off-hook.
9	VREG	Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**REFERENCE.** Connects to an external resistor to provide a high accuracy reference current.
12	REXT2	**EXTERNAL RESISTOR 2.** Sets the complex AC termination impedance.
13	REXT	**EXTERNAL RESISTOR.** Sets the real AC termination impedance.
14	RX	**RECEIVE INPUT.** Serves as the receive side input from the telephone network.
15	FILT	**FILTER.** Provides filtering for the DC termination circuits.
16	FILT2	**FILTER 2.** Provides filtering for the bias circuits.

functional description

TMS320C54V90 DSP and memory

The DSP is a 16-bit processor operating at up to 117 MIPS. It has 40K x 16 RAM and 128K x 16 program ROM on-chip. This provides complete “controller-based” modem functionality with no external memory.

The DSP firmware implements all the modem signal processing, V.42 error correction, V.42bis compression, AT command parser, and modem controller functions.

block diagram

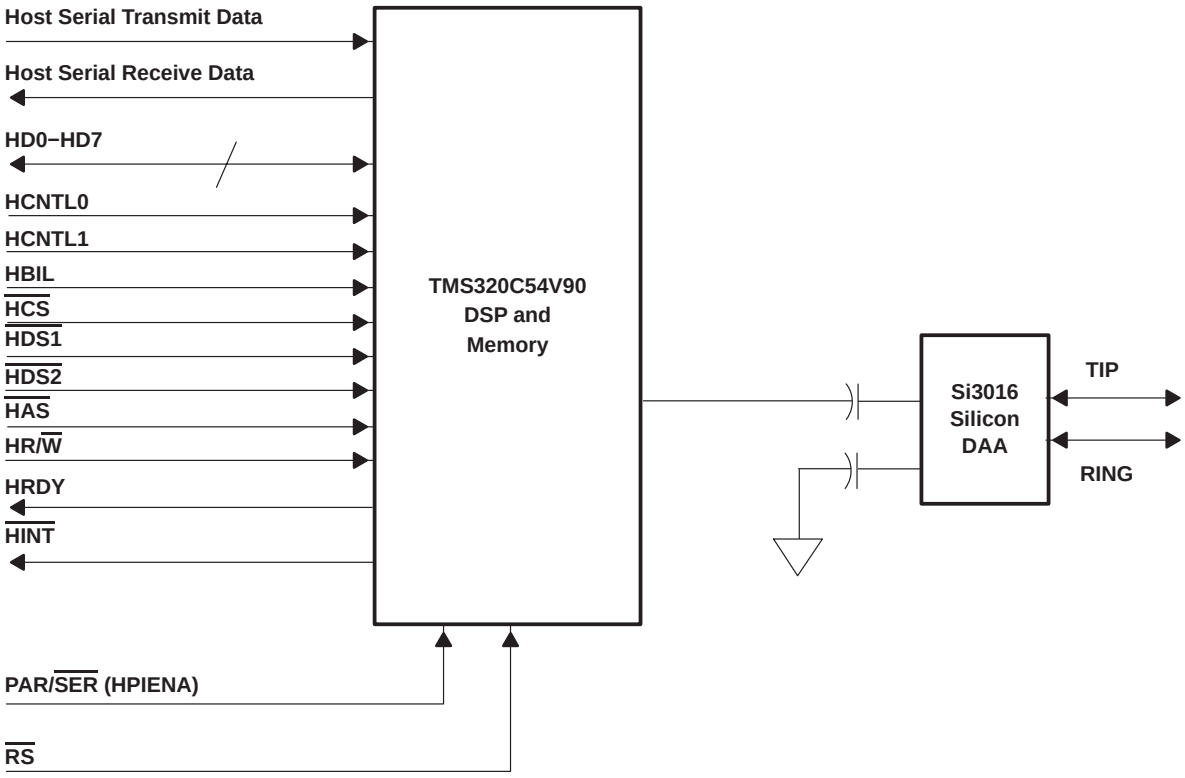


Figure 1. TMS320C54V90 Modem Block Diagram

Si3016 silicon DAA

The DAA block provides all the functions associated with the telephone line interface and the analog front end, including:

- On-hook/off-hook control
- DC termination
- AC termination
- Ring detect
- Dielectric isolation
- Surge protection
- Loop current monitor
- 2-wire/4-wire hybrid
- Receive and Transmit filters
- D/A and A/D converters
- On-hook loop voltage sensing (optional)

Si3016 silicon DAA (continued)

Certain characteristics of the DAA, such as DC and AC termination, are programmable to meet the requirements of different countries/administrations. Normally, these details are invisible to the user, and the proper characteristics are selected using an AT command and a country code.

Likewise, call origination, dialing, automatic answering, etc. are controlled by AT commands, and the TMS320C54V90 firmware controls the details of DAA functions.

The interface between the DSP and the DAA carries both Transmit and Receive line signals as digitized samples, as well as control information for the DAA.

mode selection

The CLKMD inputs select various initial conditions for the clocking system and PLLs at power-up. The TMS320C54V90 also uses these inputs to select various operating modes. Use of any of the “reserved” combinations may prevent proper operation of the modem (for example, by disabling the crystal oscillator).

Table 2. Mode Selection with CLKMD pins

MODE	CLKMD1	CLKMD2	CLKMD3	CONFIGURATION	UART MODE
0	0	0	0	reserved	−
1	0	0	1	reserved	−
2	0	1	0	Normal Mode, 58 MIPS	115.2 Kbps
3	0	1	1	reserved	−
4	1	0	0	reserved	−
5	1	0	1	Normal mode, 117 MIPS	Autobaud
6	1	1	0	reserved	−
7	1	1	1	Normal mode, 58 MIPS	Autobaud

clock considerations

The modem reference design includes a crystal from which clocks are derived for the DSP and the DAA. In the standard configuration, the oscillator frequency (or optionally the CLKIN input frequency) is 14.7456 MHz ± 50 ppm. The DSP’s internal PLL multiplies this either by four or by eight (depending on the CLKMD input selection) yielding either 58.9824 MHz or 117.9648 MHz clocking internal to the DSP. The DSP’s external clock output, CLKOUT, is preset to one quarter of the internal DSP clock, and therefore will either be 14.7456 MHz or 29.4912 MHz depending on which internal clock frequency is selected.

power requirements

The TMS320C54V90 requires 3.3V for the DSP I/Os and the DAA, 1.5 V for the DSP core, and 5 V for the capacitively-coupled interface between the DSP and DAA. The method of deriving these different voltages will depend on what power is available in the host system, cost, and efficiency considerations.

The reference design assumes that an active low power-on reset signal at 3.3-V logic levels is available from the host system.

serial and parallel interface modes

The TMS320C54V90 modem can interface with the host system either serially, via an RS-232 connection, or in parallel, via the HPI.

The selection between these two types of interfaces is made using the PAR/$\overline{\text{SER}}$ (HPIENA) input pin.

For either interface, the same set of pins are used, but with different functionality.

Table 3 shows the functionality of the modem host interface pins in both the serial and parallel interface modes.

Details of the operation of both these types of host interface are presented in the following sections of this document.

Table 3. I/O Definition for Serial and Parallel Modes

SIGNAL NAME	FUNCTION IN PARALLEL MODE (HPIENA=3.3 V)	FUNCTION IN SERIAL MODE (HPIENA=0 V)
UARTRX	Not Used	TXD (Serial Transmit Data)
UARTTX	Not Used	RXD (Serial Receive Data)
HD0	Host Port Data Bus bit 0	$\overline{\text{DTR}}$ (Data Terminal Ready)
HD1	Host Port Data Bus bit 1	$\overline{\text{RTS}}$ (Request to Send)
HD2	Host Port Data Bus bit 2	$\overline{\text{CTS}}$ (Clear to Send)
HD3	Host Port Data Bus bit 3	$\overline{\text{DSR}}$ (Data Set Ready)
HD4	Host Port Data Bus bit 4	$\overline{\text{DCD}}$ (Data Carrier Detect)
HD5	Host Port Data Bus bit 5	$\overline{\text{RI}}$ (Ring Indication)
HD6	Host Port Data Bus bit 6	$\overline{\text{MUTE}}$† (Speaker Mute)
HD7	Host Port Data Bus bit 7	$\overline{\text{OH}}$ (Off-Hook)
HCNTL0	Host Port Control 0	Not Used
HCNTL1	Host Port Control 1	Not Used
HBIL	Byte Order Identifier	Not Used
$\overline{\text{HCS}}$	Chip Select	Not Used
$\overline{\text{HDS1}}$	Data Strobe 1	Not Used
$\overline{\text{HDS2}}$	Data Strobe 2	Not Used
$\overline{\text{HAS}}$	Address Strobe	Not Used
HR/$\overline{\text{W}}$	Read/Write	Not Used
HRDY	Host Port Ready	Not Used
HINT	Host Port Interrupt	Not Used

† Functional, but included for expansion only since speaker interface not provided.

serial interface

If the PAR/$\overline{\text{SER}}$ input is held low when $\overline{\text{RS}}$ is released, the modem will operate with a serial interface instead of a parallel interface. The HD0-7 pins become general purpose I/O pins and are used for EIA-232 control signals as shown in Table 3. The serial data is carried on SERIAL TRANSMIT DATA and SERIAL RECEIVE DATA. These signals are at 3.3V logic levels, and the polarity is correct for inverting EIA-232 drivers and receivers.

serial interface (continued)

The serial interfaced is implemented with an on-chip UART. By default at power-up, the serial interface is ilitialized to automatically detect and configure itself to the data rate used by the host (autobaud). Data rates from 300 bits per second to 230400 bits per second are supported. The character format is 10 bit, i.e., 1 start, 8 data, and 1 stop bit. Both RTS/CTS and XON/XOFF flow control are supported.

host port interface (HPI)

The host port interface (HPI) is an 8-bit parallel port used to interface a host processor to the DSP. Information is exchanged between the DSP and the host processor through a 2K-word block of on-chip memory that is accessible by both the host and the DSP. The DSP has access to the HPI control register (HPIC) and the host can address the HPI memory through the HPI address register (HPIA).

Both the host and the DSP have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one HPI cycle.

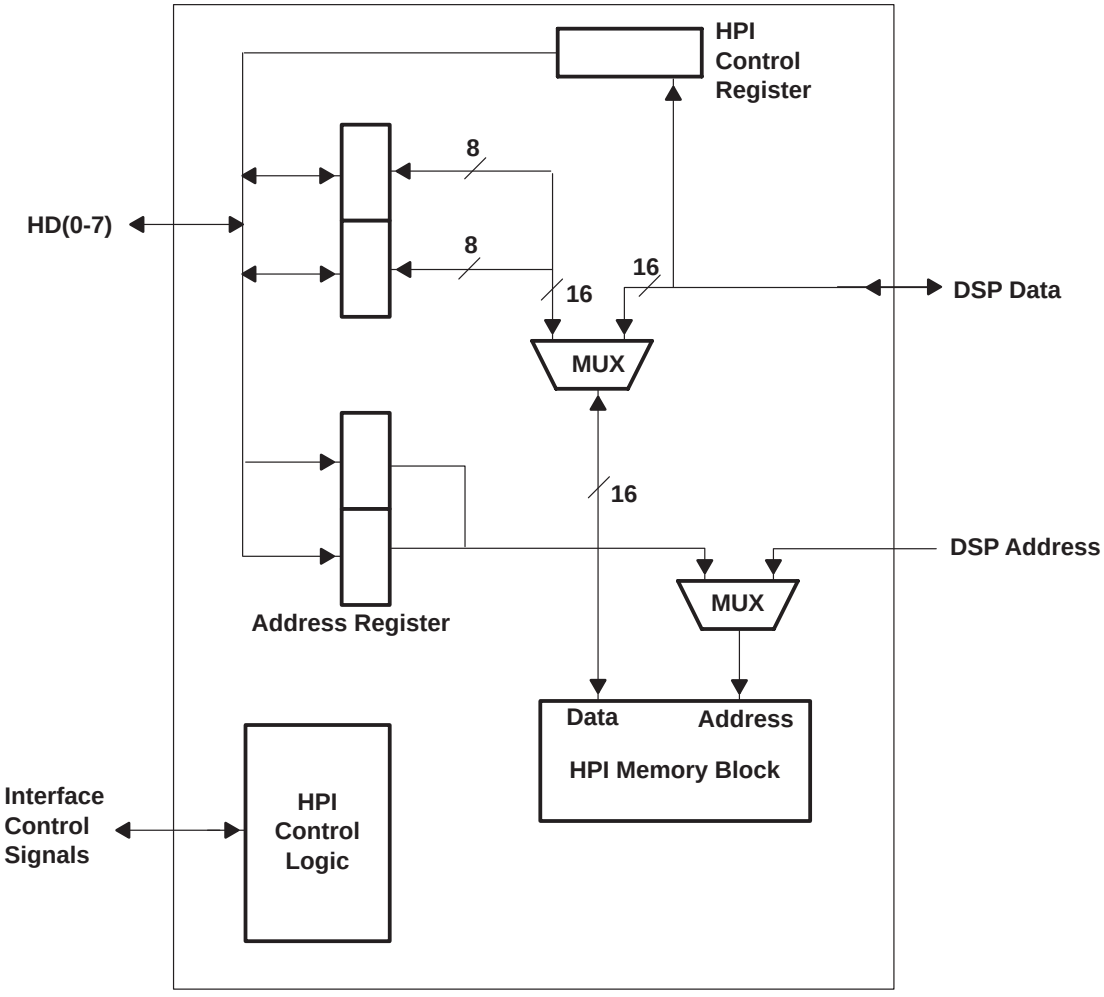


Figure 2. Host Processor Interface Block Diagram

host port interface (HPI) (continued)

The HPI interface consists of an 8-bit bidirectional data bus and various control signals. Data transfers of 16-bit words occur as two consecutive bytes with a dedicated pin (HBIL) indicating whether the high or low byte is being transmitted. Two control pins, HCNTL1 and HCNTL0, control host access to the HPIA, HPI data (with an optional automatic address increment), or the HPIC. The host can interrupt the DSP device by writing to HPIC. The DSP device can interrupt the host with a dedicated $\overline{\text{HINT}}$ pin that the host can acknowledge and clear.

The HPI control logic has two data strobes, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, a read/write strobe HR/W, and an address strobe $\overline{\text{HAS}}$, to enable a glueless interface to a variety of industry-standard host devices. The HPI is interfaced easily to hosts with multiplexed address/data bus, separate address and data buses, one data strobe and a read/write strobe, or two separate strobes for read and write. The HPI supports high-speed back-to-back accesses.

The HPI can handle one byte every five DSP device periods-that is, 64 Mbps with a 40-MIPS DSP, or 160 Mbps with a 100-MIPS DSP. The HPI is designed so that the host can take advantage of this high bandwidth and run at frequencies up to (f * n)/5, where *n* is the number of host cycles for an external access and *f* is the DSP device frequency.

basic host port interface functional description

The external HPI consists of the 8-bit HPI data bus and control signals that configure and control the interface. The interface can connect to a variety of host devices with little or no additional logic. Figure 3 shows a simplified diagram of a connection between the HPI and a host device. The 8-bit data bus (HD0-HD7) exchanges information with the host. Because of the 16-bit word structure of the DSP, all transfers with a host must consist of two consecutive bytes. The dedicated HBIL pin indicates whether the first or second byte is being transferred. An internal control register bit determines whether the first or second byte is placed into the most significant byte of a 16-bit word. The host must not break the first byte/second byte (HBIL low/high) sequence of an ongoing HPI access. If this sequence is broken, data can be lost, and unpredictable operation can result.

The two control inputs (HCNTL0 and HCNTL1) indicate which internal HPI register is being accessed and the type of access to the register. These inputs, along with HBIL, are commonly driven by host address bus bits or a function of these bits. Using the HCNTL0/1 inputs, the host can specify an access to the HPI control (HPIC) register, the HPI address (HPIA) register (which serves as the pointer into HPI memory), or HPI data (HPID) register. The HPID register can also be accessed with an optional automatic address increment.

The autoincrement feature provides a convenient way of reading or writing to subsequent word locations. In autoincrement mode, a data read causes a postincrement of the HPIA, and a data write causes a preincrement of the HPIA. By writing to the HPIC, the host can interrupt the DSP CPU, and the $\overline{\text{HINT}}$ output can be used by the DSP to interrupt the host. The host can also acknowledge and clear $\overline{\text{HINT}}$ by writing to the HPIC.

basic host port interface functional description (continued)

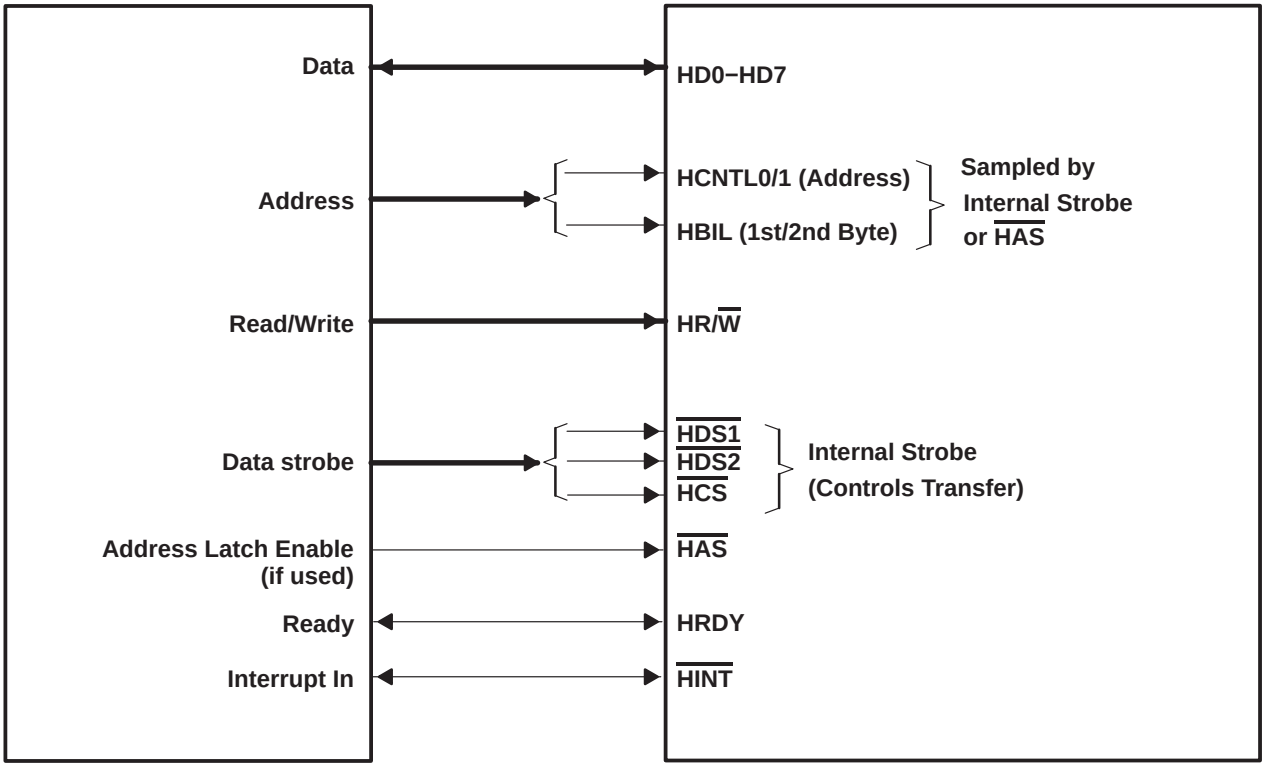


Figure 3. Generic System Block Diagram

Table 4 summarizes the three registers that the HPI utilizes for communication between the host device and the DSP CPU and their functions.

Table 4. HPI Registers Description

NAME	DESCRIPTION
HPIA	Directly accessible only by the host. Contains the address in the HPI memory at which the current access occurs.
HPIC	HPI control register. Directly accessible by either the host or by the DSP. Contains control and status bits for HPI operations.
HPID	HPI data register. Directly accessible only by the host. Contains the data that was read from the HPI memory if the current access is a read, or the data that will be written to HPI memory if the current access is a write.

The HPI ready pin (HRDY) allows insertion of wait states for hosts that support a ready input to allow deferred completion of access cycles and have faster cycle times than the HPI can accept due to DSP operating clock rates. If HRDY, when used directly from the DSP, does not meet host timing requirements, the signal can be resynchronized using external logic if necessary. HRDY is useful when the DSP operating frequency is variable, or when the host is capable of accessing at a faster rate than the maximum shared-access mode access rate. In both cases, the HRDY pin provides a convenient way to automatically (no software handshake needed) adjust the host access rate to a faster DSP clock rate.

All of these features combined allow the HPI to provide a flexible and efficient interface to a wide variety of industry-standard host devices. Also, the simplicity of the HPI interface greatly simplifies data transfers both from the host and the DSP sides of the interface. Once the interface is configured, data transfers are made with a minimum of overhead at a maximum speed.

details of host port interface operation

This subsection includes a detailed description of each HPI external interface pin function, as well as descriptions of the register and control bit functions. Logical interface timings and initialization and read/write sequences are discussed in the Host Read/Write Access to HPI section.

The external HPI interface signals implement a flexible interface to a variety of types of host devices. Devices with single or multiple data strobes and with or without address latch enable (ALE) signals can easily be connected to the HPI.

HPI signal names and functions

Table 5 describes the function HPI external interface pins in detail.

Table 5. HPI Signal Names and Functions

HPI PIN	HOST PIN	STATE†	SIGNAL FUNCTION
$\overline{\text{HAS}}$	Address latch enable (ALE) or Address strobe or unused (tied high)	I	Address strobe input. Hosts with a multiplexed address and data bus connect $\overline{\text{HAS}}$ to their ALE pin or equivalent. HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ are then latched on $\overline{\text{HAS}}$ falling edge. When used, $\overline{\text{HAS}}$ must precede the later of $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, or $\overline{\text{HDS2}}$ (see detailed HPI timing specifications on page 80). Hosts with separate address and data bus can connect $\overline{\text{HAS}}$ to a logic-1 level. In this case, HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ are latched by the later of $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, or $\overline{\text{HCS}}$ falling edge while $\overline{\text{HAS}}$ stays inactive (high).
HBIL	Address or control lines	I	Byte identification input. Identifies first or second byte of transfer (but not most significant or least significant - this is specified by the BOB bit in the HPIC register, described later in this section). HBIL is low for the first byte and high for the second byte.
HCNTL0 HCNTL1	Address or control lines	I	Host control inputs. Selects a host access to the HPIA register, the HPI data latches (with optional address increment), or the HPIC register.
$\overline{\text{HCS}}$	Address or control lines	I	Chip select. Serves as the enable input for the HPI and must be low during an access but may stay low between accesses. $\overline{\text{HCS}}$ normally precedes $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$, but this signal also samples HCNTL0/1, HR/$\overline{\text{W}}$, and HBIL if $\overline{\text{HAS}}$ is not used and $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$ are already low (this is explained in further detail later in this subsection). Figure 4 shows the equivalent circuit of the $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ inputs.
HD0-HD7	Data bus	I/O/Z	Parallel bidirectional 3-state data bus. HD7 (MSB) through HD0 (LSB) are placed in the high-impedance state when not outputting ($\overline{\text{HDS}}$ | $\overline{\text{HCS}}$ = 1).
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	Read strobe and write strobe or data strobe	I	Data strobe inputs. Control transfer of data during host access cycles. Also, when $\overline{\text{HAS}}$ is not used, used to sample HBIL, HCNTL0/1, and HR/$\overline{\text{W}}$ when $\overline{\text{HCS}}$ is already low (which is the case in normal operation). Hosts with separate read and write strobes connect those strobes to either $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$. Hosts with a single data strobe connect it to either $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$, connecting the unused pin high. Regardless of HDS connections, HR/$\overline{\text{W}}$ is still required to determine direction of transfer. Because $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are internally exclusive-NORed, hosts with a high true data strobe can connect this to one of the HDS inputs with the other HDS input connected low. Figure 4 shows the equivalent circuit of the $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, and $\overline{\text{HCS}}$ inputs.
$\overline{\text{HINT}}$	Host interrupt input	O/Z	Host interrupt output. Controlled by the HINT bit in the HPIC. Driven high when the DSP is being reset.

† I = Input, O = Output, Z = High Impedance

HPI signal names and functions (continued)

Table 5. HPI Signal Names and Functions (Continued)

HPI PIN	HOST PIN	STATE†	SIGNAL FUNCTION
HRDY	Asynchronous ready	O/Z	HPI ready output. When high, indicates that the HPI is ready for a transfer to be performed. When low, indicates that the HPI is busy completing the internal portion of the previous transaction. $\overline{HCS}$ enables HRDY; that is, HRDY is always high when $\overline{HCS}$ is high.
HR/$\overline{W}$	Read/Write strobe, address line, or multiplexed address/data	I	Read/write input. Hosts must drive HR/$\overline{W}$ high to read HPI and low to write HPI. Hosts without a read/write strobe can use an address line for this function.

† I = Input, O = Output, Z = High Impedance

The $\overline{HCS}$ input serves primarily as the enable input for the HPI, and the $\overline{HDS1}$ and $\overline{HDS2}$ signals control the HPI data transfer; however, the logic with which these inputs are implemented allows their functions to be interchanged if desired. If $\overline{HCS}$ is used in place of $\overline{HDS1}$ and $\overline{HDS2}$ to control HPI access cycles, HRDY operation is affected (since $\overline{HCS}$ enables HRDY and HRDY is always high when $\overline{HCS}$ is high). The equivalent circuit for these inputs is shown in Figure 4. The figure shows that the internal strobe signal that samples the HCNTL0/1, HBIL, and HR/$\overline{W}$ inputs (when $\overline{HAS}$ is not used) is derived from all three of the input signals, as the logic illustrates. Therefore, the latest of $\overline{HDS1}$, $\overline{HDS2}$, or $\overline{HCS}$ is the one which actually controls sampling of the HCNTL0/1, HBIL, and HR/$\overline{W}$ inputs. Because $\overline{HDS1}$ and $\overline{HDS2}$ are exclusive-NORed, both these inputs being low does not constitute an enabled condition.

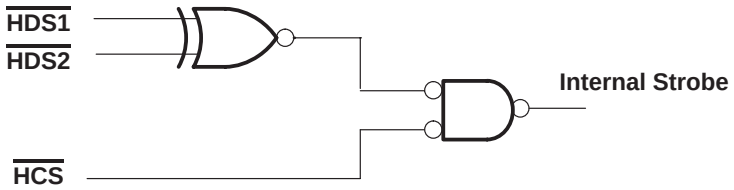


Figure 4. Select Input Logic

When using the $\overline{HAS}$ input to sample HCNTL0/1, HBIL, and HR/$\overline{W}$, this allows these signals to be removed earlier in an access cycle, therefore allowing more time to switch bus states from address to data information, facilitating interface to multiplexed address and data type buses. In this type of system, an ALE signal is often provided and would normally be the signal connected to $\overline{HAS}$.

HPI signal names and functions (continued)

The two control pins (HCNTL0 and HCNTL1) indicate which internal HPI register is being accessed and the type of access to the register. The states of these two pins select access to the HPI address (HPIA), HPI data (HPID), or HPI control (HPIC) registers. The HPIA register serves as the pointer into HPI memory, the HPIC contains control and status bits for the transfers, and the HPID contains the actual data transferred. Additionally, the HPID register can be accessed with an optional automatic address increment. Table 6 describes the HCNTL0/1 bit functions.

On the DSP, HPI memory is a 2K 16-bit word block of dual-access RAM. From the host interface, the 2K-word block of HPI memory can conveniently be accessed at addresses 0 through 7FFh; however, the memory can also be accessed by the host starting with any HPIA values with the 11 LSBs equal to 0. For example, the first word of the HPI memory block can be accessed by the host with any of the following HPIA values: 0000h, 0800h,1000h,1800h, ... F800h.

Table 6. HPI Input Control Signals Function Selection Descriptions

HCNTL1	HCNTL0	
0	0	Host can read or write the HPI control register, HPIC.
0	1	Host can read or write the HPI data latches. HPIA is automatically postincremented each time a read is performed and preincremented each time a write is performed.
1	0	Host can read or write the address register, HPIA. This register points to the HPI memory.
1	1	Host can read or write the HPI data latches. HPIA is not affected.

The HPI autoincrement feature provides a convenient way of accessing consecutive word locations in HPI memory. In the autoincrement mode, a data read causes a postincrement of the HPIA, and a data write causes a preincrement of the HPIA. Therefore, if a write is to be made to the first word of HPI memory with the increment option, due to the preincrement nature of the write operation, the HPIA should first be loaded with any of the following values: 07FFh, 0FFFh, 17FFh, ... FFFFh. The HPIA is a 16-bit register and all 16 bits can be written to or read from, although with a 2K-word HPI memory implementation, only the 11 LSBs of the HPIA are required to address the HPI memory. The HPIA increment and decrement affect all 16 bits of this register.

HPI control register bits and function

Four bits control HPI operation. These bits are BOB (which selects first or second byte as most significant), SMOD (which selects host or shared-access mode), and DSPINT and HINT (which can be used to generate DSP and host interrupts, respectively) and are located in the HPI control register (HPIC). A detailed description of the HPIC bit functions is presented in Table 7.

Because the host interface always performs transfers with 8-bit bytes and the control register is normally the first register accessed to set configuration bits and initialize the interface, the HPIC is organized on the host side as a 16-bit register with the same high and low byte contents (although access to certain bits is limited, as described previously) and with the upper bits unused on the DSP side. The control/status bits are located in the least significant four bits. The host accesses the HPIC register with the appropriate selection of HCNTL0/1, as described previously, and two consecutive byte accesses to the 8-bit HPI data bus. When the host writes to HPIC, both the first and second byte written **must** be the same value.

The layout of the HPIC bits is shown in Figure 5 through Figure 8. In the tables for read operations, if 0 is specified, this value is always read; if X is specified, an unknown value is read. For write operations, if X is specified, any value can be written. On a host write, both bytes must be identical. Note that bits 4−7 and 12−15 on the host side and bits 4−15 on the DSP side are reserved for future expansion.

HPI control register bits and function (continued)

Table 7. HPI Control Register (HPIC) Bit Descriptions

BIT	HOST ACCESS	DSP ACCESS	DESCRIPTION
BOB	Read/Write	--	If BOB = 1, first byte is least significant. If BOB = 0, first byte is most significant. BOB affects both data and address transfers. Only the host can modify this bit and it is not visible to the DSP. BOB must be initialized before the first data or address register access.
SMOD	Read	Read/Write	If SMOD = 1, shared-access mode (SAM) is enabled: the HPI memory can be accessed by the DSP. (This is the only mode used in the TM-100 application. SMOD = 0 during reset; SMOD = 1 after reset. SMOD can be modified only by the DSP but can be read by both the DSP and the host.
DSPINT	Write	--	The host processor-to-DSP interrupt. This bit can be written only by the host and is not readable by the host or the DSP. When the host writes a 1 to this bit, an interrupt is generated to the DSP. Writing a 0 to this bit has no effect. Always read as 0. When the host writes to HPIC, both bytes must write the same value.
$\overline{\text{HINT}}$	Read/Write	Read/Write	This bit determines the state of the DSP $\overline{\text{HINT}}$ output, which can be used to generate an interrupt to the host. HINT = 0 upon reset, which causes the external $\overline{\text{HINT}}$ output to be inactive (high). The HINT bit can be set only by the DSP and can be cleared only by the host. The DSP writes a 1 to HINT, causing the $\overline{\text{HINT}}$ pin to go low. The HINT bit is read by the host or the DSP as a 0 when the external $\overline{\text{HINT}}$ pin is inactive (high) and as a 1 when the $\overline{\text{HINT}}$ pin is active (low). For the host to clear the interrupt, however, it must write a 1 to HINT. Writing a 0 to the HINT bit by either the host or the DSP has no effect.

15–12	11	10	9	8	7–4	3	2	1	0
X	HINT	0	SMOD	BOB	X	HINT	0	SMOD	BOB

LEGEND: X = Unknown value is read.

Figure 5. HPIC Diagram - Host Reads from HPIC

15–12	11	10	9	8	7–4	3	2	1	0
X	HINT	DSPINT	X	BOB	X	HINT	DSPINT	X	BOB

LEGEND: X = Any value can be written.

Figure 6. HPIC Diagram - Host Writes to HPIC

HPI control register bits and function (continued)

15–4	3	2	1	0
X	HINT	0	SMOD	0

LEGEND: X = Unknown value is read.

Figure 7. HPIC Diagram - DSP Reads from HPIC

15–4	3	2	1	0
X	HINT	X	SMOD	X

LEGEND: X = Any value can be written.

Figure 8. HPIC Diagram - DSP Writes to HPIC

Because the DSP can write to the SMOD and HINT bits, and these bits are read twice on the host interface side, the first and second byte reads by the host may yield different data if the DSP changes the state of one or both of these bits in between the two read operations. The characteristics of host and DSP HPIC read/write cycles are summarized in Table 8.

Table 8. DSP HPIC Read/Write Cycles

DEVICE	READ	WRITE
Host	2 bytes	2 bytes (Both bytes must be equal)
DSP	16 bits	16 bits

host read/write access to HPI

The host begins HPI accesses by performing the external interface portion of the cycle; that is, initializing first the HPIC register, then the HPIA register, and then writing data to or reading data from the HPID register. Writing to HPIA or HPID initiates an internal cycle that transfers the desired data between the HPID and the dedicated internal HPI memory. Because this process requires several DSP cycles, each time an HPI access is made, data written to the HPID is not written to the HPI memory until after the host access cycle, and the data read from the HPID is the data from the previous cycle. Therefore, when reading, the data obtained is the data from the location specified in the previous access, and the current access serves as the initiation of the next cycle. A similar sequence occurs for a write operation: the data written to HPID is not written to HPI memory until after the external cycle is completed. If an HPID read operation immediately follows an HPID write operation, the same data (the data written) is read.

The autoincrement feature available for HPIA results in sequential accesses to HPI memory by the host being extremely efficient. During random (nonsequential) transfers or sequential accesses with a significant amount of time between them, it is possible that the DSP may have changed the contents of the location being accessed between a host read and the previous host data read/write or HPIA write access, because of the prefetch nature of internal HPI operation. If this occurs, data different from the current memory contents may be read. Therefore, in cases where this is of concern in a system, two reads from the same address or an address write prior to the read access can be made to ensure that the most recent data is read.

When the host performs an external access to the HPI, there are two distinctly different types of cycles that can occur: those for which wait states are generated (the HRDY signal is active) and those without wait states.

host read/write access to HPI (continued)

For accesses utilizing the HRDY signal, during the time when the internal portion of the transfer is being performed (either for a read or a write), HRDY is low, indicating that another transfer cannot yet be initiated. Once the internal cycle is completed and another external cycle can begin, HRDY is driven high by the HPI. This occurs after a fixed delay following a cycle initiation (refer to the DSP data sheet for detailed timing information for HPI external interface timings). Therefore, unless back-to-back cycles are being performed, HRDY is normally high when the first byte of a cycle is transferred. The external HPI cycle using HRDY is shown in the timing diagram in Figure 9.

In a typical external access, as shown in Figure 9, the cycle begins with the host driving HCNTL0/1, HR/$\overline{W}$, HBIL, and $\overline{HCS}$, indicating specifically what type of transfer is to occur and whether the cycle is to be read or a write. Then the host asserts the $\overline{HAS}$ signal (if used) followed by one of the data strobe signals. If HRDY is not already high, it goes high when the previous internal cycle is complete, allowing data to be transferred, and the control signals are deasserted. Following the external HPI cycle, HRDY goes low and stays low for a period of approximately five CLKOUT cycles (refer to the DSP data sheet for HPI timing information) while the DSP completes the internal HPI memory access, and then HRDY is driven high again. Note, however, HRDY is always high when $\overline{HCS}$ is high.

As mentioned previously, SAM accesses generally utilize the HRDY signal. The exception to the HRDY-based interface timings when in SAM occurs when reading HPIC or HPIA or writing to HPIC (except when writing 1 to either DSPINT or HINT). In these cases, HRDY stays high; for all other SAM accesses, HRDY is active.

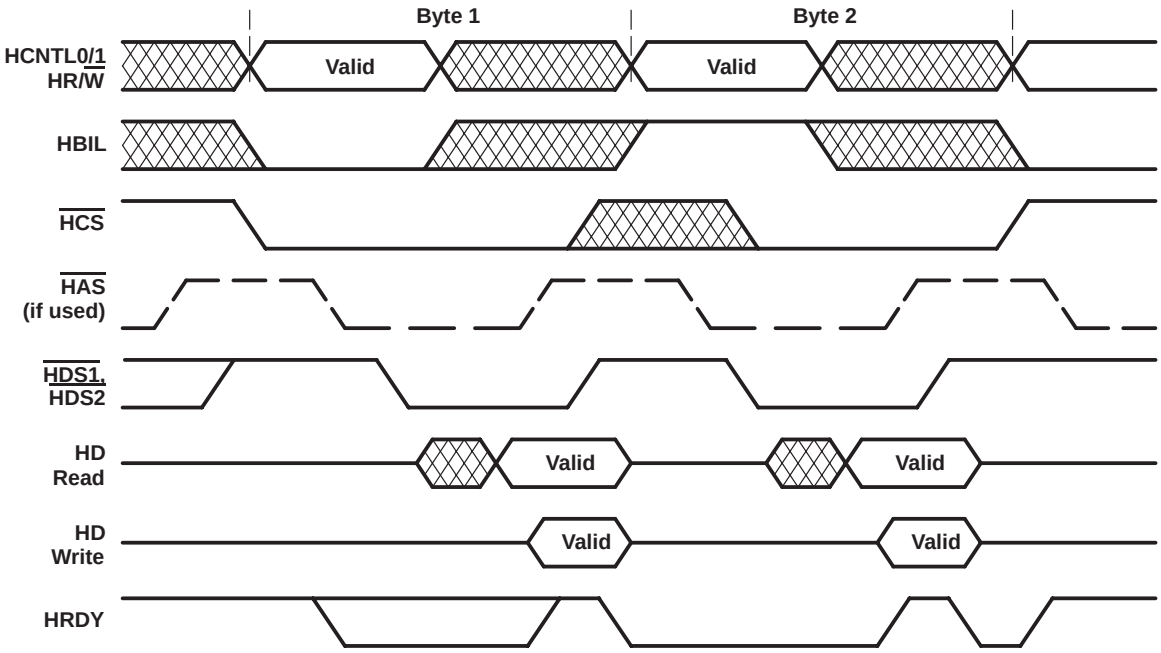


Figure 9. HPI Timing Diagram

host read/write access to HPI (continued)

Table 9. Wait-State Generation Conditions

REGISTER	WAIT STATE GENERATED	
	READS	WRITES
HPIC	No	1 to DSPINT/HINT - Yes All other cycles - No
HPIA	No	Yes
HPID	Yes	Yes

example access sequences

A complete host access cycle always involves two bytes, the first with HBIL low, and the second with HBIL high. This 2-byte sequence must be followed regardless of the type of host access (HPIA, HPIC, or data access) and the host must not break the first byte/second byte (HBIL low/high) sequence of an ongoing HPI access. If this sequence is broken, data may be lost, and unpredictable operation may result.

Before accessing data, the host must first initialize HPIC, in particular the BOB bit, and then HPIA (in this order, because BOB affects the HPIA access). After initializing BOB, the host can then write to HPIA with the correct byte alignment. On an HPI memory read operation, after completion of the HPIA write, the HPI memory is read and the contents at the given address are transferred to the two 8-bit data latches, the first byte data latch and the second byte data latch. Table 10 illustrates the sequence involved in initializing BOB and HPIA for an HPI memory read. In this example, BOB is set to 0 and a read is requested of the first HPI memory location (in this case 1000h), which contains FFFEh.

Table 10. Initialization of BOB and FPIA

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host writes HPIC, 1st byte	00	0	00	0	00xx	xxxx	xxxx	xxxx
Host writes HPIC, 2nd byte	00	0	00	1	0000	xxxx	xxxx	xxxx
Host writes HPIA, 1st byte	10	0	10	0	0000	10xx	xxxx	xxxx
Host writes HPIA, 2nd byte	00	0	10	1		1000	xxxx	
Internal HPI RAM read complete						1000	FF	FE

In the cycle shown in Table 10, BOB and HPIA are initialized, and by loading HPIA, an internal HPI memory access is initiated. The last line of Table 10 shows the condition of the HPI after the internal RAM read is complete; that is, after some delay following the end of the host write of the second byte to HPIA, the read is completed and the data has been placed in the upper and lower byte data latches. For the host to actually retrieve this data, it must perform an additional read of HPID. During this HPID read access, the contents of the first byte data latch appears on the HD pins when HBIL is low and the content of the second byte data latch appears on the HD pins when HBIL is high. Then the address is incremented if autoincrement is selected and the memory is read again into the data latches. The sequence involved in this access is shown in Table 11.

example access sequences (continued)

Table 11. Read Access to HPI with Autoincrement

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host reads data, 1st byte	FF	1	01	0	0000	1000	FF	FE
Host reads data, 2nd byte	FE	1	01	1	0000	1000	FF	FE
Internal HPI RAM read complete						1001	6A	BC

In the access shown in Table 11, the data obtained from reading HPID is the data from the read initiated in the previous cycle (the one shown in Table 10) and the access performed as shown in Table 11 also initiates a further read, this time at location 1001h (because autoincrement was specified in this access by setting HCNTL1/0 to 01). Also, when autoincrement is selected, the increment occurs with each 16-bit word transferred (not with each byte); therefore, as shown in Table 11, the HPIA is incremented by only 1. The last line of Table 11 indicates that after the second internal RAM read is complete, the contents of location 1001h (6ABCh) has been read and placed into the upper and lower byte data latches.

During a write access to the HPI, the first byte data latch is overwritten by the data coming from the host while the HBIL pin is low, and the second byte data latch is overwritten by the data coming from the host while the HBIL pin is high. At the end of this write access, the data in both data latches is transferred as a 16-bit word to the HPI memory at the address specified by the HPIA register. The address is incremented prior to the memory write because autoincrement is selected.

An HPI write access is illustrated in Table 12. In this example, after the internal portion of the write is completed, location 1002h of HPI RAM contains 1234h. If a read of the same address follows this write, the same data just written in the data latches (1234h) is read back.

Table 12. Write Access to HPI with Autoincrement

EVENT	HD	HR/$\overline{W}$	HCNTL1/0	HBIL	HPIC	HPIA	LATCH1	LATCH2
Host writes data, 1st byte	12	0	01	0	0000	1002	12	FE
Host writes data, 2nd byte	34	0	01	1	0000	1002	12	34
Internal HPI RAM write complete						1002	12	34

host device using DSPINT to interrupt the DSP

A DSP interrupt is generated when the host writes a 1 to the DSPINT bit in HPIC. The host and the DSP always read this bit as 0. A DSP write has no effect. Once a 1 is written to DSPINT by the host, a 0 need not be written before another interrupt can be generated, and writing a 0 to this bit has no effect. The host should not write a 1 to the DSPINT bit while writing to BOB or HINT, or an unwanted DSP interrupt is generated.

host port interface (DSP) using HINT to interrupt the host device

When the DSP writes a 1 to the HINT bit in HPIC, the $\overline{\text{HINT}}$ output is driven low; the HINT bit is read as a 1 by the DSP or the host. The HINT signal can be used to interrupt the host device. The host device, after detecting the $\overline{\text{HINT}}$ interrupt line, can acknowledge and clear the DSP interrupt and the HINT bit by writing a 1 to the HINT bit. The HINT bit is cleared and then read as a 0 by the DSP or the host, and the $\overline{\text{HINT}}$ pin is driven high. If the DSP or the host writes a 0, the HINT bit remains unchanged.

using the HPI in the TMS320C54V90 application

The previous section has described the operation of the generic HPI. This section will describe the specific memory map and protocol used in the TMS320C54V90 application.

This section uses the standard modem convention for referring to transmit and receive data:

- “Transmit data” is data to be transmitted on the phone line. Thus, transmit data passes from the host processor to the TMS320C54V90 DSP and is a write to the HPI.
- “Receive data” is data received from the phone line. Thus, receive data passes from the TMS320C54V90 DSP to the host processor and is a read from the HPI.

The data structure in the shared HPI memory consists of circular buffers for transmit and receive data, and control/status registers. Two mechanisms are provided to facilitate control and access of data in the transmit and receive circular buffers: transmit and receive circular buffer address pointers for the two circular buffers, and a data valid flag in the upper data byte of each word in the two buffers. The transmit and receive buffer pointers point to the current location in the buffer for data transfer. Circular buffer locations are accessed in an ascending (numerically increasing) address order.

The data valid flag for each word in the two buffers indicates whether the data in the lower byte of the word is valid or invalid/empty. Proper buffer management must be used to prevent both underflow and overflow, since the data source could be faster or slower than the data sink (in either direction). This is discussed in detail later in this section.

Control registers for the transmit and receive directions contain control and status bits, including bits corresponding to the EIA-RS232 control signals. The control register bits are positive-true, i.e., a 1 = EIA-RS232 “on”.

The embedded valid data flags allow for flow control locally across the HPI interface, while the RTS and CTS control bits implement higher-level flow control in the same fashion as the corresponding signals on a serial RS232 interface. On the host interface side, the state of RTS must be driven, and the state of CTS must be monitored by the host, and the host must respond appropriately

Table 13 shows the HPI memory map, and Figure 10 and Figure 11 show the bit functions in the control registers. As shown in Table 13, some registers have different functions during initialization vs. normal mode. The HPI interface is usually in normal mode, unless a unique sequence is performed to place the interface into initialization mode (see Initialization section).

using the HPI in the TMS320C54V90 application (continued)

Table 13. HPI Memory Map†

ADDRESS	HOST ACCESS	DSP ACCESS	FUNCTION	
			NORMAL MODE	INITIALIZATION MODE
1000–1001h			Not used	
1002h	W	R	Host Command Register	Revision Word 1
1003h	W	R	Host Acknowledge/Parameter Register	Host Acknowledge/Parameter Register
1004h	W	R	Transmit Control Register	Revision Word 2
1005h	W	R		Revision Word 3
1006h	W	R		Revision Month/Day
1007h	W	R		Revision Year
1008h	W	R		Host Type Identifier (0001)
1009h	W	R		Revision Word 4
100A–100Fh			Not used	
1010h	R	W	DSP Receive Buffer Pointer	
1011h	R	W	DSP Transmit Buffer Pointer	
1012h	R	W	DSP Command Register	DSP Command Register
1013h	R	W	DSP Acknowledge/Parameter Register	DSP Acknowledge/Parameter Register
1015h	R	W	Receive Control Register	
1016–101F			Not used	
1020h–102Fh	R/W	R/W	16-word Transmit Data Buffer	
1030–105Fh			Not used	
1060h–106Fh	R/W	R/W	16-word Receive Data Buffer	
1070h–17FFh			Not used for HPI. Should not be accessed by Host. May be used for other functions (general purpose memory) by DSP.	

† The Read and Write access indicated in the table must be enforced by the software.

using the HPI in the TMS320C54V90 application (continued)

15	1	0
X	DTR	RTS

LEGEND: X = Any value can be written.

Figure 10. Transmit Control Register

15	14	13	12	11	10	9	8
X	X	OFF_HOOK	X	RI	DCD	DSR	CTS

7	0
X	

LEGEND: X = Unknown value is read.

Figure 11. Receive Control Register

data format

The transmit and receive circular buffers each consist of 16 16-bit words. (As described previously, each word transfer requires two 8-bit transfers across the HPI interface.)

Only the lower byte of each word is used for data. The entire lower byte is treated as data. If the data format is less than 8 bits, the data should be right-justified. For example, with 7-bit ASCII data, the MSB can be a parity bit or can be forced to 1 or 0.

The upper byte of each word is used as a flag to indicate whether this word has valid data to transfer. Before writing new data into the transmit data buffer, the host system must first read the current location of the buffer to ensure that the previous data content has been read by the DSP. When the upper byte is 00h, the current location is available for writing new data. When new data is written, the upper byte should be set to a non-zero value such as 3Fh. For example, if the new data is the ASCII character “A”, 3F41h should be written into the buffer. When that location is later read, both the upper and lower bytes will be set to 00h by the DSP.

Similarly, when the host system is reading the receive data buffer for new data, it should interpret the upper byte as a “valid data” indicator. After reading the new data, the host system must write back 00h to both the upper and lower bytes of the current receive data buffer location to clear it as an acknowledgement to the DSP that the data has been read before advancing to the next buffer location.

As mentioned previously, both the transmit and receive buffer pointers and the valid data flags can be used to control data transfers. The pointers used by the DSP to read and write the buffers can be accessed at locations 1011h and 1010h respectively, and circular buffer locations are accessed in an ascending (numerically increasing) address order. However, because all access to the shared memory must be addressed indirectly through the HPIA register, the valid data flag method is generally a more efficient way to control data transfers than having read and write pointers that reside in the shared memory. Although the transmit and receive buffer pointers will be updated by the DSP and will always contain the address of the current location in the buffer for data transfer by the DSP, if the host simply reads these pointers once during initialization and then maintains its own version of the pointers internally, significant overhead in HPI data transfers can be saved.

data format (continued)

Note that when the host maintains its own version of the pointers internally, these versions of the circular buffer pointers will often not be pointing to the same address as the DSP transmit and receive buffer pointers, since the rate at which the host and the DSP transfer data to and from the transmit and receive buffers is often different. For this reason, the valid data flag mechanism is extremely efficient, and even crucial in managing buffer data transfers.

initialization

The following steps should be performed following a power-on Reset to initialize the HPI and resynchronize the host with the DSP:

1. Write the value 0005h into HPI address 1002h (Host Command Register). This requests that the DSP place the HPI interface in initialization mode.
2. Wait for the DSP to respond with the value of 1234h at HPI address 1012h (DSP Command Register). This indicates that the DSP has placed the HPI interface in initialization mode.
3. Once the DSP has responded with 1234h, initialize the host's internal copy of the data buffer pointers to the values at addresses 1010h (DSP Current Receive Data Buffer Pointer) and 1011h (DSP Current Transmit Data Buffer Pointer).
4. Write the following responses in the appropriate HPI addresses **in the order as shown** in Table 14.
5. Wait for the DSP to respond with the value of 0000h at HPI address 1012h (DSP Command Register).
6. Write the value 0000h at HPI addresses 1002h and 1003h to acknowledge a successful resynchronization.
7. Initialization and resynchronization are complete. The HPI interface now reenters normal mode. Although it can be assumed that the DSP pointers are set to the first address of their respective buffers, it is suggested that the host HPI driver use the values that were read from addresses 1010h (DSP Current Receive Data Buffer Pointer) and 1011h (DSP Current Transmit Data Buffer Pointer).

NOTE: This sequence of operations can also be initiated at any time to resynchronize the interface.

Table 14. Initial Writes to HPI

ADDRESS	VALUE	FORMAT
1002h	Revision word 1	(BCD, decimal) range 0–9
1003h	Acknowledge response	Must be 5678h
1004h	Revision word 2	(BCD, decimal) range 0–9
1005h	Revision word 3	(BCD, decimal) range 0–9
1006h	Revision Month/Day	(BCD, decimal) High/Low bytes MM/DD
1007h	Revision Century/Year	(BCD, decimal) High/ Low bytes YYYY
1008h	Driver Identifier	Must be 0001h
1009h	Revision word 4	Must be 0002h

Revision Words 1–4, Month/Day, and Year, are provided so that the host can load information about its driver. This information will be reported by the ATI4 command.

initialization (continued)

After a power-on reset, the upper bytes of the circular buffers will be cleared to indicate that there is no data in the buffers. The EIA-RS232 signals will be set to default values based on the default AT Commands (see AT Commands section). The modem will be in the AT command mode. The EIA-RS232 signal status after power-on reset is as follows:

CTS = on

DSR = off

DCD = off

RI = off

OFF_HOOK = off

RTS = ignored

DTR = ignored

data transfer protocol — transmit

It is recommended that the host maintain an internal pointer that represents the next buffer location that will become available for an HPI write to ensure most efficient data transfers. Initially, this would be the beginning of the buffer.

For a transmit operation, the current buffer location is read and the upper-byte flag is tested until it becomes 00h indicating that the location is available. Then the new data is written into the low byte and a non-zero value such as 3Fh is written into the upper byte. The pointer is incremented and the process is repeated until all new data are sent or a location is found where the upper-byte flag has not yet been cleared by the DSP. Encountering an asserted upper-byte flag would indicate that the buffer has been filled up, and further data transfers must wait until one or more buffer locations become empty.

Note that the host version of the buffer pointer will often not be pointing to the same address as the DSP buffer pointers, since the rate at which the host and the DSP transfer data to and from the transmit and receive buffers is often different.

The auto increment feature of the HPIA can be used to reduce the number of accesses to the HPIA. However, the pointer in the host must be updated and kept consistent with the HPIA. Also, the HPIA needs to be restored when switching between the Transmit Data Buffer and the Receive Data buffer.

data transfer protocol — receive

The receive data transfer is similar to the transmit data transfer with the roles reversed between the host and the DSP.

When the DSP places data in a buffer location, it will set the upper byte flag to a non-zero value. It will test the flag before writing to ensure that the location has been emptied by the host.

As with the transmit operation, it is recommended that the host maintain its own internal pointer indicating the next empty buffer location. It reads that location and tests the upper byte until it detects the flag set. It will then read the location and write back to that location with the upper and lower bytes cleared. This will repeat until the host tests a location where the upper byte is cleared. Encountering a location with its upper byte cleared would indicate that the end of valid data in the receive data buffer has been reached, and the host must wait for additional data to be received. Note again that the host version of the buffer pointer will often not be pointing to the same address as the DSP buffer pointers, since the rate at which the host and the DSP transfer data to and from buffers is often different.

HPI interrupt

Since the flag bits and control registers reflect the last operation completed by the DSP, and since the HPIA can only be written by the host, it is possible for the host data transfers to be accomplished entirely asynchronously on a polled basis. For greater efficiency however, an interrupt-driven mode is also provided as follows:

The DSP generates an interrupt by setting the HINT bit, which also asserts the $\overline{\text{HINT}}$ output signal. This can be used either to generate a hardware interrupt on the host, or the host can poll the bit or $\overline{\text{HINT}}$ output signal to determine when to service the HPI data transfers.

Three conditions can cause an interrupt:

1. More than eight locations in the receive data buffer have been filled by the DSP since the last interrupt.
2. More than eight locations in the transmit data buffer have been read by the DSP since the last interrupt.
3. The Buffer Flush timer (defined by S−Register 71) expires (default = 10 ms). This is to ensure that both buffers are flushed in the case of low data activities (see S−Register description for additional information).

There are two modes of operation for the Buffer Flush timer:

- Free-running Mode – Selected by default, or by the AT command AT*Y254:W618A,0. In this mode, a HINT interrupt is generated when a free-running periodic timer expires before condition 1) or 2) above occurs. The period is programmable from 2 to 254 ms through S−Register 71. The default value is 10 ms.
- Data Triggered Mode – Selected by the AT command AT*Y254:W618A,1. In this mode, a HINT interrupt is generated when neither condition 1) or 2) above is met, but at least one data character has been written to or read from the buffers by the DSP within the defined timeout period. The period is programmable from 2 to 254 ms through S−Register 71. The default value is 10 ms. Note that the timer does not run when there is no data in either buffer, and an interrupt will not be generated until at least one piece of data is transferred and then the full timer period expires.

In either mode, the Buffer Flush timer is disabled when S−Register 71 is set to 255.

When using the HPI interrupt function to control data transfers, as with any other data transfer control mechanism, it is the responsibility of the data source (the host processor in the case of transmit, and the DSP in the case of receive) to prevent overflow by detecting that there are no more buffer locations with flags cleared, and stopping the flow of data.

With flow control and compression, data rate across the HPI can be higher than the modem line rate and can also be variable. The buffer management schemes discussed above will allow handling of the following data transfer scenarios:

- The recipient takes all data currently in the buffer
- The recipient takes part of the data currently in the buffer
- The source writes multiple blocks (up to the capacity of the buffer) before some or all is read
- The buffer is full, cannot write any more
- The buffer is empty, no new data for recipient

AT commands

This section describes the modem AT (ATtention) command set, which is the primary mechanism through which a host interacts with the modem.

The AT command protocol permits you to:

- Obtain information from the modem
- Configure the modem
- Establish or terminate data communications
- Test the modem

The tables presented later in this section describe the available AT commands and their format and function.

Later sections describe the modem's response to these AT commands in detail to more easily facilitate host interface to the modem.

In addition to the AT commands described in this section, several other mechanisms in the modem software affect certain aspects of modem and AT command operation. In particular, operation of some AT commands is affected by the contents of a group of registers called the S-Registers. The S-Register description section should be consulted for an explanation of the available S-Registers, and their contents and access.

After Reset, the TMS320C54V90 is in AT command mode, and accepts commands from the serial port or from the HPI Transmit Data buffer, depending on which interface is selected. Each command string (except A/) must be preceded by the letters AT and followed by a carriage return or Enter. The A/ command, which doesn't require a carriage return or the AT-prefix, instructs the modem to repeat the last command string it received. Also, note that the command prefix can be entered either as AT or at, but not At or aT.

The modem responds with an "OK" acknowledgement when commands are accepted. Otherwise, an "ERROR" response is returned to the DTE when an invalid command or illegal parameters are detected. Some commands such as ATA, ATD and ATO, are exceptions to this, and do not return an "OK" response. Instead the modem either responds with a "CONNECT" message when a successful connection is made or a "NO CARRIER", "NO DIALTONE", or "BUSY" message if the attempt failed.

Multiple commands can be assembled together into a single command string with the restriction that certain "action" commands, such as ATA, ATD, ATO or ATH, must be placed at the end of a concatenated string, otherwise the commands following them will be discarded. The AT command buffer can hold up to 50 characters.

New commands cannot be issued until a response to the previous command is received. In the case of no response, wait a minimum of five seconds before entering another command.

Once the modem has successfully completed a handshake procedure and entered data mode, the AT command parser is disabled. All subsequent characters flowing in from the DTE interface are assumed to be "payload" data. If necessary, the DTE can re-invoke the AT command parser while online by sending a special "escape" sequence. This escape sequence consists of three consecutive identical characters, which are normally (the default value) defined to be the "+" character (so the escape sequence is "+++"). To be accepted by the modem, the escape sequence must be sent with the proper guard time (as specified by the contents of S-Register 12) before, during and after the 3-character sequence transmission. A valid escape sequence must meet all of the following three conditions:

1. A period of no TXD activity equal to or greater than S12 (S-Register 12) before the first of the escape code characters is received.
2. The time elapsed between reception of the first and the third escape code characters must be equal to or less than S12.
3. A period of no TXD activity equal to or greater than S12 after the third escape code character is received.

AT commands (continued)

Note that the specific character used for the escape sequence is defined by the contents of S2, and therefore, if system requirements dictate, this character can be changed. This is, in fact, necessary sometimes if the remote modem being used considers the +++ sequence to be a control sequence of its own. In this case, the +++ sequence may cause the remote modem to disconnect. In order to facilitate a proper escape sequence, the 54V90 modem escape sequence character can be changed, for example, to a minus sign (decimal 45) by modifying the S2 contents. The escape sequence guard time specification may also be modified in the same fashion by changing the contents of S12.

additional host interface considerations

The modem firmware supports X-ON/X-OFF and RTS-CTS flow control on both the serial and parallel HPI interfaces. Additionally, because the HPI interface uses circular buffers, proper management of the read and write data flags will inherently result in flow control.

Also, optionally, the TMS320C54V90 modem can use an external serial EEPROM to store various types of initialized configuration and other information. Refer to the Non-volatile EEPROM Initialized Configuration Storage description section for further information regarding the EEPROM feature.

If use of the external EEPROM feature is not desired, enhanced features such as stored configurations and stored numbers may still be implemented directly by software on the host processor, with appropriate AT commands sent on a per-call basis.

Table 15 through Table 21 describe the available AT commands. The tables are grouped as follows:

- The basic AT commands
- The extended AT& commands
- The extended AT% commands
- The extended AT\ commands
- The extended AT+ commands
- The extended AT* commands
- The extended AT! commands

The default values indicated in Table 15 through Table 21 will be present after reset.

Table 15. Basic AT Command Set

COMMAND	ACTION
$	Help screen- AT$ will list all basic AT commands.
A/	Repeat command. Repeat last command.
A	Answer call. Answer incoming call.
C1	Included for compatibility only, responds with “OK”.
Dn	Dial. The dial command, followed by one or more dial command modifiers, manually dials a phone number: ! Flash hook switch for 1/2 second. , Pause before continuing. Time is in S-Register 8. ; Return to AT command mode. Leaves modem off-hook. @ Wait for quiet answer before continuing. Time is in S-Register 7. P Pulse (rotary) dialing. T Tone (DTMF) dialing. W Wait for dial tone before continuing. Time is in S-Register 6. *,#,A,B,C,D,0,1,2,3,4,5,6,7,8,9 (DTMF digits). 0,1,2,3,4,5,6,7,8,9 (pulse digits).
En E0 E1 ◊	Local DTE echo. Disable. Enable.
Hn H0 H1	Hook switch. Go on-hook (hang up modem). Go off-hook.
In I0 I1 I3 I4 I5 I6 I7 I8 I9	Identification and checksum. Report product code. Report calculated checksum. Report firmware revision level. Report DTE interface type. Report country code. Report basic connection information. (See ATI6 Command Response section.) Report DAA type. Report processor and clock frequency. Report Solsis generation.
On O0 O1 O2	Go On-line (and enter data mode) from command mode. All but O0 from idle assume call already established. Responds with a CONNECT message (as appropriate for optioning) immediately or once handshake is completed. Mainly used for testing purposes. Go on-line. Returns directly to data mode (without any handshaking or rate renegotiation), OR, from idle, without a call already established, goes off-hook in originate mode, attempts to handshake, and enters data mode if connection is established. This is typically used in direct line modem applications. In the idle case, no response is given if connection cannot be established, and the host must be prepared to initiate an appropriate recovery in this situation. Go on-line and retrain, with a complete handshake, and then enter data mode. Responds NO CARRIER if handshake fails. Go on-line and perform a basic rate renegotiation (a subset of a complete handshake) and then enter data mode. Responds NO CARRIER if connection cannot be established.
P	Dialing type, Pulse (rotary) dial [vs. Tone dial]. See also T command.
Qn Q0 ◊ Q1	Response mode. Enable. Disable (enable quiet mode).

NOTE: ◊ = Indicates the default value

Table 15. Basic AT Command Set (Continued)

COMMAND	ACTION
Sn Sn? Sn=x S$	S-Registers. Output contents of S-Register n. Set S-Register n to value x. Help screen for S-registers.
T ◊	Dialing type, Tone (DTMF) dial [vs. Pulse dial]. See also P command.
Vn V0 V1 ◊	Select numeric or text response types to AT commands. Also see AT!Cn commands. Select decimal ASCII numeric responses to AT commands. Only valid when used with AT!C1 (alternate command response mode). Indeterminate otherwise. See Table 26 for values. Select ASCII text responses to AT commands (default).
Xn X0 X1 X2 X3 X4 ◊ X5	Call Progress Monitor (CPM). Basic results; disable CPM. Extended results; disable CPM. Extended results and detect dial tone only. Extended results and detect busy only. Extended results, full CPM. Extended results, full CPM and detect ringback.
Yn Y0 ◊ Y1	Long space disconnect. Disable. Enable.
Z	Retrieve/restore AT command settings previously stored in EEPROM with AT&W.

NOTE: ◊ = Indicates the default value

Table 16. Extended AT& Command Set

COMMAND	ACTION
&$	Help screen lists all AT& commands.
&Cn &C0 &C1 &C2 &C3 ◊	Carrier operation. Force Carrier On. Real mode (follows modem energy detection). Force Carrier On; toggle Carrier on disconnect. Carrier On after link established.
&Dn &D0 ◊ &D1 &D2 &D3	Select modem response to DTR (Data Terminal Ready) on-to-off transition. Note that valid DTR on-to-off transition time (valid loss of DTR) determined by S25 setting. Ignore transition. Modem considers DTR always on (default). Enter AT command mode from data mode. Responds OK. Go on-hook (hang up). Responds NO CARRIER. Same as &D2, but also recalls stored configuration from EEPROM if installed. This allows special setup for one call with easy recovery to previous setup.
&F	Load factory defaults
&Gn &G4 &G5 &G6 &G7 &G8 &G9 &G10 &G11 &G12 &G13 &G14 &G15 &G16 &G17 ◊	Maximum Line Connection Rate in V.34 mode. Maximum DCE data rate is 2.4 Kbps. Maximum DCE data rate is 4.8 Kbps. Maximum DCE data rate is 7.2 Kbps. Maximum DCE data rate is 9.6 Kbps. Maximum DCE data rate is 12 Kbps. Maximum DCE data rate is 14.4 Kbps. Maximum DCE data rate is 16.8 Kbps. Maximum DCE data rate is 19.2 Kbps. Maximum DCE data rate is 21.6 Kbps. Maximum DCE data rate is 24 Kbps. Maximum DCE data rate is 26.4 Kbps. Maximum DCE data rate is 28.8 Kbps. Maximum DCE data rate is 31.2 Kbps. Maximum DCE data rate is 33.6 Kbps.
&Hn &H0 ◊ &H1 &H2 &H3 &H4 &H5 &H6 &H7 &H8 &H9 &H10 &H12	Switched network handshake mode. V.90 multimode. V.90/V.34. V.34 multimode. V.34 only. V.32bis multimode. V.32bis only. V.22bis. V.22. Bell 212. Bell 103. V.21. V.23.
&K &K0 &K1 &K2 ◊ &K3 &K4	Modem-to-DTE flow control. Disable in both directions. Use XON/XOFF from modem to DTE only. Use CTS. Use RTS/CTS. Use XON/XOFF in both directions.

NOTE: ◊ = Indicates the default value

Table 16. Extended AT& Command Set (Continued)

COMMAND	ACTION
&L	Maximum PCM rate (V.90)
&L1	28000
&L2	29333
&L3	30666
&L4	32000
&L5	33333
&L6	34666
&L7	36000
&L8	37333
&L9	38666
&L10	40000
&L11	41333
&L12	42666
&L13	44000
&L14	45333
&L15	46666
&L16	48000
&L17	49333
&L18	50666
&L19	52000
&L20	53333
&L21	54666
&L22 ◊	56000
&M0 ◊	Async mode. Included for compatibility only, responds with “OK”.
&P	Pulse Dialing Rate
&P0 ◊	10 pps
&P1	20 pps (only allowed for Japan country code).
&Sn	DSR operation (Data Set Ready).
&S0	Force DSR On; toggle Off on disconnect.
&S1 ◊	Normal DSR operation.
&S2	DSR follows carrier detect.
&S3	Force DSR On.
&Tn	Test mode. (See also the %Dn command).
&T0	Cancel (terminate) test mode (after you have done +++ and wait for OK).
&T1	Initiate analog loopback test. AT&G11 should always be issued before AT&T1 to limit DCE data rate to 19.2Kbps for test result consistency.
&W	Stores the AT command configuration settings of key AT commands in serial EEPROM, if installed. Responds OK if EEPROM installed and working correctly, or ERROR if not. Allows custom configuration (other than defaults) to be defined, and returned to after specialized modifications are made for exception conditions. Stored information is retrieved automatically after power-up, or with ATZ. See Non-Volatile EEPROM Initialized Configuration Storage section for list of which command settings are stored.

NOTE: ◊ = Indicates the default value

Table 17. Extended AT% Command Set

COMMAND	ACTION
%$	Help screen lists all AT% commands.
%Cn %C0 %C1 ◊	Data Compression. Disable. Enable in transmit and receive paths
%Dn %D0 %D1 ◊	DSR operation in test mode. (See also the &Tn command). Force DSR On during test mode Force DSR Off during test mode.
%In %I0 ◊ %I1	Loop current monitor. Loop current is monitored in the off-hook state. If there is a significant change in loop current, it is presumed that another device has gone off hook, and the modem will immediately disconnect, and respond NO CARRIER. See also %V command. Disable. Enable.
%Kn %K0 ◊ %K1	Character abort. 2-second delay to character abort. Disable.
%On %O0 ◊ %O1 %O2	Answer mode. Answer mode if ringing. Force to answer mode. Automatic answer in originate mode.
%Vn %V0 ◊ %V1 %V2	Check loop voltage before dialing. See also %I command. Disable (default) Enable using a preset threshold. The loop voltage is compared to a threshold stored in S100. If the voltage is below the threshold, it is presumed that another device is off-hook on the same line, dialing will not be attempted, and the response is LINE UNAVAILABLE. Enable using a measured threshold. The loop voltage is compared to a measured threshold stored in S101. This threshold is continuously monitored and is initialized by the modem automatically each time the modem is powered up or when a phone line is plugged in. S101 is set to (S102)% of the measured loop voltage. The default value of S102 is 85(%). A re-calibration of the threshold can also be initiated manually with the ATS101=0 command. After initialization, if the line voltage is below the threshold, it is presumed that another device is off-hook on the same line, dialing will not be attempted, and the response is LINE UNAVAILABLE.
%Z	Enter power down mode. Hardware reset is required to return to normal operation.

NOTE: ◊ = Indicates the default value

Table 18. Extended AT\ Command Set

COMMAND	ACTION
\$	Help screen lists all AT\ commands.
\Cn	Fallback selection and pre-link data buffer.
\C0 ◊	Time-out and fallback; speed buffer; no data buffer.
\C1	Time-out and fallback; speed buffer; buffer receive data.
\Gn	Modem-to-modem flow control (Only in Speed Buffer Mode).
\G0 ◊	Disable.
\G1	Enable XON/XOFF in transmit and receive paths.
\G2	Enable in transmit path only.
\G3	Enable in transmit and receive paths, with pass-through.
\Nn	Asynchronous protocol.
\N0	Wire mode (only in Speed Buffer Mode).
\N1	Wire mode (only in Speed Buffer Mode).
\N2	MNP reliable mode (or drop call if failed to negotiate MNP link)
\N3 ◊	V.42 or MNP auto-reliable mode (fallback to Speed Buffer mode if failed to negotiate either link)
\N4	V.42 reliable mode (or drop call if failed to negotiate V.42 link)
\N5	V.42 reliable mode (or drop call).
\Tn	Select serial DTE interface speed. Note that when using the parallel HPI interface, this command causes no effect on operation. The only action that is taken is to load this parameter selection into a register that can be accessed via the HPI.
\T1 ◊	Autobaud
\T2	300
\T3	1200
\T4	2400
\T5	4800
\T6	7200
\T7	9600
\T8	14.4 K
\T9	19.2 K
\T10	38.4 K
\T11	57.6 K
\T12	115.2 K
\T13	230.4 K
\Vn	Connect message type.
\V0 ◊	Reports line rate upon data mode, link message after link negotiation.
\V1	Connect and protocol message sent after link negotiation, connect reported as DTE rate.
\V2	Connect and protocol message sent after link negotiation (Microcom compatible), connect reported as line rate.
\V3	Connect message only after protocol negotiation, connect reported as DTE rate.
\V4	Connect message reports asymmetrical connect speeds.

NOTE: ◊ = Indicates the default value

Table 19. Extended AT+ Commands (FAX and Caller ID)

COMMAND	ACTION
+FCLASS +FCLASS=0 ◊ +FCLASS=1 +FCLASS=? +FCLASS?	Selects between FAX and Data Mode operation. Select Data Mode. Select facsimile Class 1 mode. Report service classes supported. Report current selection.
+FTS=n	Stop transmission and pause for n x 10 msec before execution of next command.
+FRS=n	Wait for silence (loss of energy) for n = 0−255 x 10 msec increments. This command is included for compatibility, but is totally ignored.
+FTM=? +FTM=n	Reports Class 1 FAX transmitter capabilities (24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146). Selects Class 1 FAX transmitter speed (n = any of those listed in capabilities).
+FRM=? +FRM=n	Reports Class 1 FAX receiver capabilities (24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146). Selects Class 1 FAX receiver speed (n = any of those listed in capabilities).
+FTH=n	Where n = 3. Selects transmitter mode for FAX control channel.
+FRH=n	Where n = 3. Selects receiver mode for FAX control channel.
+PHF	Hook flash.
+VCDT=n +VCDT=0 ◊ +VCDT=1 +VCDT=2 +VCDT=3 +VCDT=4	Configure CID response format for various countries. CID message sent after first ring (USA type). CID message preceded by DTAS dual-tone alert signal (European type). CID message preceded by an abbreviated (non-ringing) ring pulse (France, Spain type). CID message preceded by polarity reversal plus DTAS signal (United Kingdom type). CID message preceded by polarity reversal plus seizing signal (Japan).
+VCID +VCID=? +VCID? +VCID=0 ◊ +VCID=1 +VCID=2	Caller ID functionality. Report the available range of selections. Report the current selection. Disable Caller ID reporting. Enable Caller ID reporting with formatted presentation. When received, basic Caller ID information (time, number, etc.) is presented to the DTE interface formatted as ASCII text. Compatible with either single-line or multi-line Caller ID data. See also the +VCID=2 option. Enable Caller ID with unformatted presentation. When received, complete Caller ID data is presented to the DTE interface as the received data represented in hex ASCII, i.e., if the hex byte of 41 is received, the hex value of 34 (ASCII "4") followed by the value 31 (ASCII "1") is sent. Compatible with either single-line or multi-line Caller ID data. See also the +VCID=1 option.

NOTE: ◊ = Indicates the default value

Table 20. Extended AT* Command Set

COMMAND	ACTION
*Y254:Aaaaa,bbbb	AND address aaaa with bit pattern bbbb. Note that aaaa must be exactly four digit hex and must reflect any leading zeros.
*Y254:Oaaaa,bbbb	OR address aaaa with bit pattern bbbb.
*Y254:Qaaaa	Reads selected data memory location address aaaa (hex).
*Y254:Qaaaa,n,m	Display memory from address aaaa (hex). For n=0–3, display program memory from page n. For n=4, display data memory. The parameter m specifies the number of lines to be displayed in hex. Each line displays 12 locations. If m is omitted, 23 lines of 12 values are displayed. If m and n are both omitted, one data memory location is displayed.
*Y254:Waaaa,vvvv	Writes vvvv (Hex) to data memory location aaaa (hex). Used to modify user adjustable PTT parameters (see Table 22 for User Adjustable PTT parameter definitions).
*Y254:W618A,n	Select free running or data triggered Buffer Flush timer mode. If n = 0, free running mode is selected. If n = 1, data triggered mode is selected. Default is 0. Refer to the HPI interface section for a description of the Buffer Flush timer function.
*Y254:W6189,n	Select BSkyB compatibility mode. If n = 0, compatibility is not selected. If n = 1, compatibility is selected. Default is 0.

Table 21. Extended AT! Command Set

COMMAND	ACTION
!Cn !C0 ◊ !C1	Configures AT command response mode. Also see ATVn commands. Configure AT command responses in standard response mode (default). Configure AT command response in alternate response mode. Must be selected to receive numeric response types as selected by ATV0.
!Xn	Phone exclusion relay driver control enable. Enables XF output as a relay driver control to isolate a local external parallel phone handset from the phone line (the modem is always connected to the phone line). It is assumed that the relay is normally closed. The implemented polarity for XF is such that when XF is high (or power is off), the relay is deactivated (and the phone is connected), and when XF is low, the relay is activated (and the phone is disconnected). Appropriate circuitry must be used to implement relay driver for this function to operate correctly. See also Parallel Phone Handset Exclusion Relay Driver Control description in the Parallel Phone Exclusion Relay Control section.
!X0 ◊	Disabled. XF is always high, to keep relay always deactivated, with external handset always connected to the phone line (default).
!X1	Modem disconnects immediately from online state and goes back on hook whenever a parallel phone is detected going off-hook. XF then goes low for a period given by S-register 231 (default is 500msec) and then high again. This action ensures that the current call will get disconnected properly and the parallel phone will receive a dial tone to place a new call. Should only be used if AT%I1 also selected.
!X2	XF goes low to activate the relay to isolate handset whenever modem is off-hook. With this selection, the external parallel handset will not be able to acquire the phone line any time the modem is off-hook, and if the phone is off-hook when the modem goes off-hook, the phone will be immediately disconnected from the line.

NOTE: ◊ = Indicates the default value

user adjustable PTT parameters definitions

The adjustable PTT parameters are initialized according to the selected country code setting, or by other specific AT commands, and therefore normally do not require modification by the user. The information in this section is provided for those exceptionable situations that might require these parameters to be further modified.

The PTT parameters may be modified using the following AT command.

AT*Y254:Wpppp,vvvv

where, pppp = parameter #, vvvv = parameter value – both in 4-digit hexadecimal format.

Table 22. User-Adjustable PTT Parameters Definitions

PARAMETER #	PULSE DIALING	UNIT	DEFAULTS
0100	Reserved		
0101	Break Time	msec	
0102	Make Time	msec	
0103	Inter-digit Time, Part 1 (total = 1 + 2, See #104)	msec	
0104	Inter-digit Time, Part 2 (total = 1 + 2, See #103)	msec	
	Number of pulses generated for…		
0105	Digit 0		
0106	Digit 1		
0107	Digit 2		
0108	Digit 3		
0109	Digit 4		
010A	Digit 5		
010B	Digit 6		
010C	Digit 7		
010D	Digit 8		
010E	Digit 9		
	DTMF Dialing		
010F	Hi/Lo tone attenuation expressed as a 4-digit hexadecimal ”0XY0” where, X = high group tone attenuation in dB Y = low group tone attenuation in dB	dB	
0110	Tone ON Time	msec	
0111	Tone OFF Time (inter−digit)	msec	
	Off−Hook Delay		
0112		msec	
	Incoming Ring Detection		
0113	Maximum Ring Signal Frequency, F_{max} (Hz)	Enter 2400 x ($1/F_{max}$)	
0114	Minimum Ring Signal Frequency, Delta, $F_{min} - F_{max}$ (Hz)	Enter 2400 x ($1/F_{min}$) − 2400 x ($1/F_{max}$)	
0115	Minimum Ring ON Duration, T_{on} (seconds)	Enter T_{on} x 2400	
0116	Maximum Ring Cadence, T_{ring} (seconds)	Enter T_{ring} x 2400	

Table 22. User-Adjustable PTT Parameters Definitions (Continued)

PARAMETER #	PULSE DIALING	UNIT	DEFAULTS
	Pre−CPM Tone Detector Filters		
0117	Band−pass Filter Coefficients (0117 to 012B)		
	Post−CPM Tone Detector Filters		
012C	Band−pass Filter Coefficients (012C to 0140)		
	Pre−CPM Tone (Dial Tone) Detect		
0141	Dial Tone ON Threshold Level	Arbitrary	
0142	Dial Tone OFF Threshold Level	Arbitrary	
	Post−CPM Tone Detect		
0143	ON Threshold	Arbitrary	
0144	OFF Threshold	Arbitrary	
0145	**Blacklisting System**	16-bit Address	
	Blacklisting Parameter Table		
0146			
	Country Specific Bit Mapped Options		
014E			
	Loop Current Detection		
014F	ON Timer	msec	
0150	OFF Debounce Timer	msec	
	Busy Tone Cadence		
0151	Minimum Cadence, T_{min} (seconds)	Enter 2400 x T_{min}	
0152	Maximum Cadence Delta, $T_{max} - T_{min}$ (seconds)	Enter 2400 x T_{max} − 2400 x T_{min}	
0153	Minimum Tone ON Time, T_{on} (seconds)	Enter 2400 x T_{on}	
	Ringback Tone Cadence		
0154			
	Dialtone Detection		
0157	Detection Window	msec	
0158	Minimum Tone ON Time, T_{on} (seconds)	Enter 2400 x T_{on}	
0159	‘W’ Dial Modifier Wait Time	seconds	
	Country−dependent Restricted Options		
015A	Variable, up to six parameters		
	Nominal Transmit Level		
0178	Gain Multiplier (16-bits)	Q12 format (S3.12)	3F00h

special test commands

summary

To facilitate the process of testing, the modem supports a number of special test commands where the user can put the modem into a non-standard mode of operation.

special 'AT' commands

continuous DTMF transmission

AT*Y1Dn

where, n = digit to be dialed

The modem goes off−hook and transmits a continuous DTMF digit. This facilitates adjustment and measurement of level and twist.

This mode is terminated by a character abort (hitting any keys).

sustaining the transmitter at any modulation

AT*Y113

This command disables the Poor Signal Quality Retrain feature. It is useful for examination of the modem's transmit spectrum in the following way.

Procedure:

1. Disable V.42, i.e. AT\N0, to avoid protocol requesting a disconnect.
2. Disable loss-of-carrier disconnect by executing ATS10=255.
3. AT*Y113
4. After modem is connected escape into command mode, i.e. +++, to avoid garbage characters flooding the terminal screen when you remove the remote modem's signal.
5. Remove remote modem's signal.

Also note that AT*Y113 must be re-executed each time a call is made.

country code setting

The modem can be configured to operate in any of the countries shown below by an AT command as follows,

AT*Y162K = CC, *where* CC *is the corresponding numeric code*

The selected country code is saved automatically in EEPROM if installed.

Also the country code setting should be initialized before any other initialization is performed. This is because the country code setting initializes many parameters which, if modified separately, will simply be changed back by the country code setting if it is initialized later.

Table 23. Country Code Setting

COUNTRY	CODE	COUNTRY	CODE	COUNTRY	CODE
Algeria	213	Hungary	36	Qatar	974
Argentina	54	India	91	Reset‡	911
Australia	61	Indonesia	62	Russia	7
Austria	43	Ireland	353	Saudi_Arabia	966
Bahrain	973	Israel	972	Singapore	65
Belgium	32	Italy†	21	Slovakia	428
Bolivia	591	Japan	81	Slovenia	386
Brazil	55	Jordan	962	South_Africa	27
Chile	56	Korea	82	Spain	34
China	86	Kuwait	965	Sweden	46
Colombia	57	Lebanon	961	Switzerland	41
Costa_Rica	506	Malaysia	60	Syria	963
CTR21/TBR21	21	Mexico	52	Taiwan	886
Cyprus	357	Morocco	212	Thailand	66
Czechoslovakia	42	Netherlands	31	Trinidad	888
Denmark	45	New_Zealand	64	Turkey	90
Ecuador	593	Norway	47	Tunisia	216
Egypt	20	Oman	968	UAE	971
Finland	358	Panama	507	UK	44
France	33	Peru	51	Uruguay	598
Germany	49	Philippines	63	USA/Canada	1
Greece	30	Poland	48	Venezuela	58
Guatemala	502	Portugal	351	Yemen	967
Hong_Kong	852	Puerto_Rico	999		

† In most cases, the country code of 21 for Italy as indicated is appropriate, however, some circumstances may require a different configuration. In cases where a user desires to comply with the traditional homologation requirements of Italy, for example NET4 compliance, a special AT command sequence is required as follows:

AT*Y162K=386
AT*Y254:W101,3C,28,28,348
AT*Y254:W14E,169
AT*Y254:W158,2D0
AT*Y254:W17D,100C,1110

‡ After a power−on reset, country code is 911, indicating that no country code has been programmed. Operation is the same as USA/Canada.

s-registers/commands

The S command allows you to view (Sn?) or change (Sn=x) the S-Registers. The S-Registers store values for functions that typically are rarely changed, such as timers or counters, and the ASCII values of control characters, such as Carriage Return. S−Register values are entered and displayed in decimal ASCII form. Table 24 summarizes the S-Register set.

Table 24. S-Register Commands

S-REG.	FUNCTION	DECIMAL (DEFAULT)	ASCII	UNITS
0	Automatic answer.	0		
1	Ring Count (reset after 10 seconds).	0		
2	Escape code character.	43	+	
3	Carriage return character.	13	CR	
4	Line feed character.	10	LF	
5	Backspace character.	08	BS	
6	Dial tone wait timer	02		seconds
7	Carrier wait timer; @ dial command modifier wait timer; ringback wait timer.	80		seconds
8	Dial pause timer for, dial command modifiers.	02		seconds
9	Carrier presence timer.	06		0.1 second
10	Carrier loss timer.	14		0.1 second
12	Escape code guard timer.	50		0.02 second
25	DTR delay timer.	05		0.01 seconds
30	Activity Timer	0		minutes
38	Hang-up delay timer.	20		seconds
71	Buffer flush timer for HPI interrupt	10		0.001 seconds
72	V.23 Reversible Mode	0		1=enable 0=disable
100	Static on-hook line sensing voltage threshold	9		n x 2.75
101	Measured on-hook line sensing voltage threshold	−		n x 2.75
102	Measured on-hook line sensing voltage threshold percentage of actual line voltage	85		percent
231	Phone exclusion relay driver hook flash duration time	50		0.01 seconds

result codes

Table 25 and Table 26 show the AT command response result codes in standard and alternate command response modes. In alternate command response mode, both text (verbose) and numeric response types are available. Note that the AT!C command is used to select between the standard and alternate command response modes, and the ATV command is used to select between text and numeric response types. The AT\V command selects the format of the connect message.

result codes (continued)

Table 25. Standard Result Code Definitions (!C0)

VERBOSE	DESCRIPTION
OK	Command has been accepted
ERROR	Modem detected an error in an AT command.
CONNECT	A connection established (300 bps, fax, or V.21).
RING	Modem detected an incoming call.
RINGING	Modem detected ring−back tone from far end. (If ATX5 is selected.)
NO CARRIER	Call disconnected.
NO DIALTONE	Modem cannot detect Dial Tone
BUSY	Busy response from network is detected
LINE UNAVAILABLE	Low loop voltage before modem goes off hook to dial (Indicates another device is using the line).
NO ANSWER	Remote modem did not answer. Modem did not detect period of silence set by S7 when using the @ dial modifier in the dial command.
FORBIDDEN NUMBER	The number to be dialed has been blacklisted. Further attempt to dial is prohibited until either delay timeout is reached or until modem is reset.
BLACK LIST FULL	The list of forbidden number is full. (Only for countries that require blacklisting).
DELAY LIST FULL	The ten delay records are active. No resources to handle more numbers. (Only for countries that require redialing delay).
DELAYED xx HOURS xx MINUTES xx SECONDS	The number is blocked from further dialing for the length of time displayed because of past failed attempts.
CONNECT 75	Line Speed. Connect Message format for \V0
CONNECT 300	Line Speed. Connect Message format for \V0
CONNECT 1200	Line Speed. Connect Message format for \V0
CONNECT 2400	Line Speed. Connect Message format for \V0
CONNECT 4800	Line Speed. Connect Message format for \V0
CONNECT 9600	Line Speed. Connect Message format for \V0
CONNECT 7200	Line Speed. Connect Message format for \V0
CONNECT 12000	Line Speed. Connect Message format for \V0
CONNECT 16800	Line Speed. Connect Message format for \V0
CONNECT 14400	Line Speed. Connect Message format for \V0
CONNECT 19200	Line Speed. Connect Message format for \V0
CONNECT 21600	Line Speed. Connect Message format for \V0
CONNECT 24000	Line Speed. Connect Message format for \V0
CONNECT 26400	Line Speed. Connect Message format for \V0
CONNECT 28800	Line Speed. Connect Message format for \V0
CONNECT 31200	Line Speed. Connect Message format for \V0
CONNECT 33600	Line Speed. Connect Message format for \V0
CONNECT 28000	Line Speed. Connect Message format for \V0
CONNECT 29333	Line Speed. Connect Message format for \V0
CONNECT 30666	Line Speed. Connect Message format for \V0
CONNECT 32000	Line Speed. Connect Message format for \V0
CONNECT 33333	Line Speed. Connect Message format for \V0
CONNECT 34666	Line Speed. Connect Message format for \V0
CONNECT 36000	Line Speed. Connect Message format for \V0
CONNECT 37333	Line Speed. Connect Message format for \V0

result codes (continued)

Table 25. Standard Result Code Definitions (!C0) (Continued)

VERBOSE	DESCRIPTION
CONNECT 38666	Line Speed. Connect Message format for \V0
CONNECT 40000	Line Speed. Connect Message format for \V0
CONNECT 41333	Line Speed. Connect Message format for \V0
CONNECT 42666	Line Speed. Connect Message format for \V0
CONNECT 44000	Line Speed. Connect Message format for \V0
CONNECT 45333	Line Speed. Connect Message format for \V0
CONNECT 46666	Line Speed. Connect Message format for \V0
CONNECT 48000	Line Speed. Connect Message format for \V0
CONNECT 49333	Line Speed. Connect Message format for \V0
CONNECT 50666	Line Speed. Connect Message format for \V0
CONNECT 52000	Line Speed. Connect Message format for \V0
CONNECT 53333	Line Speed. Connect Message format for \V0
CONNECT 54666	Line Speed. Connect Message format for \V0
CONNECT 56000	Line Speed. Connect Message format for \V0
CONNECT *line speed* /REL	Line Speed\Protocol. Connect message for \V2
CONNECT 300	Connect DTE speed. \V1 and \V3 format
CONNECT 1200	Connect DTE speed. \V1 and \V3 format
CONNECT 2400	Connect DTE speed. \V1 and \V3 format
CONNECT 4800	Connect DTE speed. \V1 and \V3 format
CONNECT 7200	Connect DTE speed. \V1 and \V3 format
CONNECT 9600	Connect DTE speed. \V1 and \V3 format
CONNECT 14400	Connect DTE speed. \V1 and \V3 format
CONNECT 19200	Connect DTE speed. \V1 and \V3 format
CONNECT 38400	Connect DTE speed. \V1 and \V3 format
CONNECT 57600	Connect DTE speed. \V1 and \V3 format
CONNECT 115200	Connect DTE speed. \V1 and \V3 format
CONNECT 230400	Connect DTE speed. \V1 and \V3 format
CONNECT Rx Tx	Connect Rx line speed Tx line speed. \V4 format
PROTOCOL: NONE	Connection established without Error Correction
PROTOCOL: V42	V.42 Error Correction established
PROTOCOL: V42bis	V.42bis Data Compression established
PROTOCOL: ALTERNATE, CLASS 3+ CLASS 4	MNP Error Correction established

result codes (continued)

Table 26. Alternate Mode (!C1) Result Code Definitions

NUMERIC	VERBOSE	DESCRIPTION
0	OK	Command has been accepted
1	CONNECT	Short form connect message or 300bps FSK connection
2	RING	Incoming ring detected
3	NO CARRIER	Modem has been disconnected from line
4	ERROR	Invalid command has been rejected
5	CONNECT 1200	Successful 1200 bps connection at DCE rate
6	NO DIALTONE	Modem cannot detect Dial Tone
7	BUSY	Busy response from network is detected
8	NO ANSWER	S7 timed out while ringback after executing dial modifier @
10	CONNECT 2400	Successful 2400 bps connection at DCE rate
11	CONNECT 4800	Successful 4800 bps connection at DCE rate
12	CONNECT 9600	Successful 9600 bps connection at DCE rate
13	CONNECT 7200	Successful 7200 bps connection at DCE rate
14	CONNECT 12000	Successful 12000 bps connection at DCE rate
15	CONNECT 14400	Successful 14400 bps connection at DCE rate
16	CONNECT 19200	Successful 19200 bps connection at DCE rate
17	CONNECT 38400	Successful 38400 bps connection at DTE rate
18	CONNECT 57600	Successful 57600 bps connection at DTE rate
19	CONNECT 115200	Successful 11500 bps connection at DTE rate
22	CONNECT 75	Successful 75 bps connection at DCE rate.
24	DELAYED *time*	Re−dial attempt aborted. Delayed re−dial in progress
32	FORBIDDEN NUMBER	Re−dial attempt aborted. Number is blacklisted
40	+MRR: 300,300	DCE carrier at 300 bps
44	+MRR: 1200,75	V.23 TX=1200 bps, RX=75 bps
45	+MRR: 75,1200	V.23 TX=75 bps, RX=1200 bps
46	+MRR: 1200	DCE carrier at 1200 bps
47	+MRR: 2400	DCE carrier at 2400 bps
48	+MRR: 4800	DCE carrier at 4800 bps
49	+MRR: 7200	DCE carrier at 7200 bps
50	+MRR: 9600	DCE carrier at 9600 bps
51	+MRR: 12000	DCE carrier at 12000 bps
52	+MRR: 14400	DCE carrier at 14400 bps
53	+MRR: 16800	DCE carrier at 16800 bps
54	+MRR: 19200	DCE carrier at 19200 bps
55	+MRR: 21600	DCE carrier at 21600 bps
56	+MRR: 24000	DCE carrier at 24000 bps
57	+MRR: 26400	DCE carrier at 26400 bps
58	+MRR: 28800	DCE carrier at 28800 bps
59	CONNECT 16800	Successful 16800 bps connection at DCE rate
61	CONNECT 21600	Successful 21600 bps connection at DCE rate
62	CONNECT 24000	Successful 24000 bps connection at DCE rate
63	CONNECT 26400	Successful 26400 bps connection at DCE rate
64	CONNECT 28800	Successful 28800 bps connection at DCE rate

result codes (continued)

Table 26. Alternate Mode (!C1) Result Code Definitions (Continued)

NUMERIC	VERBOSE	DESCRIPTION
70	+ER: NONE	Modem connected without error correction
77	+ER: LAPM	Modem connected with V.42 error correction
78	+MRR: 31200	DCE carrier at 31200 bps
79	+MRR: 33600	DCE carrier at 33600 bps
80	+ER: ALT	Modem connected with MNP error correction
83	LINE UNAVAILABLE	Line already occupied by another device (i.e. phone)
84	CONNECT 33600	Successful 33600 bps connection at DCE rate
91	CONNECT 31200	Successful 31200 bps connection at DCE rate
134	+MCR: 103B	Modem connected in Bell 103 mode
135	+MCR: 212B	Modem connected in Bell 212 mode
136	+MCR: V21	Modem connected in V.21 mode
137	+MCR: V22	Modem connected in V.22mode
138	+MCR: V22B	Modem connected in V.22bis mode
139	+MCR: V23	Modem connected in V.23 mode
140	+MCR: V32	Modem connected in V.32 or V.32bis mode
142	+MCR: V34	Modem connected in V.34 mode
145	+MCR: V90	Modem connected in V.90 mode
150	+MRR: 32000	DCE carrier at 32000 bps
152	+MRR: 36000	DCE carrier at 36000 bps
154	+MRR: 40000	DCE carrier at 40000 bps
156	+MRR: 44000	DCE carrier at 44000 bps
158	+MRR: 48000	DCE carrier at 48000 bps
160	+MRR: 52000	DCE carrier at 52000 bps
162	+MRR: 56000	DCE carrier at 56000 bps
165	CONNECT 32000	Successful 32000 bps connection at DCE rate
167	CONNECT 36000	Successful 36000 bps connection at DCE rate
169	CONNECT 40000	Successful 40000 bps connection at DCE rate
171	CONNECT 44000	Successful 44000 bps connection at DCE rate
173	CONNECT 48000	Successful 48000 bps connection at DCE rate
175	CONNECT 52000	Successful 52000 bps connection at DCE rate
177	CONNECT 56000	Successful 56000 bps connection at DCE rate
180	CONNECT 28000	Successful 28000 bps connection at DCE rate
181	CONNECT 29333	Successful 29333 bps connection at DCE rate
182	CONNECT 30666	Successful 30666 bps connection at DCE rate
183	CONNECT 33333	Successful 33333 bps connection at DCE rate
184	CONNECT 34666	Successful 34666 bps connection at DCE rate
185	CONNECT 37333	Successful 37333 bps connection at DCE rate
186	CONNECT 38666	Successful 38666 bps connection at DCE rate
187	CONNECT 41333	Successful 41333 bps connection at DCE rate
188	CONNECT 42666	Successful 42666 bps connection at DCE rate
189	CONNECT 45333	Successful 45333 bps connection at DCE rate
190	CONNECT 46666	Successful 46666 bps connection at DCE rate
191	CONNECT 49333	Successful 49333 bps connection at DCE rate

result codes (continued)

Table 26. Alternate Mode (!C1) Result Code Definitions (Continued)

NUMERIC	VERBOSE	DESCRIPTION
192	CONNECT 50666	Successful 50666 bps connection at DCE rate
193	CONNECT 53333	Successful 53333 bps connection at DCE rate
194	CONNECT 54666	Successful 54666 bps connection at DCE rate
195	+MRR: 28000	DCE carrier at 28000 bps
196	+MRR: 29333	DCE carrier at 29333 bps
197	+MRR: 30666	DCE carrier at 30666 bps
198	+MRR: 33333	DCE carrier at 33333 bps
199	+MRR: 34666	DCE carrier at 34666 bps
200	+MRR: 37333	DCE carrier at 37333 bps
201	+MRR: 38666	DCE carrier at 38666 bps
202	+MRR: 41333	DCE carrier at 41333 bps
203	+MRR: 42666	DCE carrier at 42666 bps
204	+MRR: 45333	DCE carrier at 46666 bps
205	+MRR: 46666	DCE carrier at 46666 bps
206	+MRR: 49333	DCE carrier at 49333 bps
207	+MRR: 50666	DCE carrier at 50666 bps
208	+MRR: 53333	DCE carrier at 53333 bps
209	+MRR: 54666	DCE carrier at 54666 bps

ATI6 command response

The ATI6 command can be used to provide detailed and useful information regarding characteristics of a modem connection. This command provides detailed information regarding an ongoing call, or summarized information regarding the most recent (but completed) call.

To provide information regarding an ongoing call, the host must reenter command mode on the modem, normally accomplished by entering +++. Note however, that some modems will drop an ongoing call if this sequence is entered, because the sequence serves some control function for the remote modem. In order to avoid this, the escape sequence character to reenter command mode can be changed to a different value (for example, ”−”) by changing the value in S−Register 2, using the ATS2= command.

The detailed ATI6 command response consists of eight lines of information. The summarized ATI6 command response consists only of the first three lines of the detailed response. The figure below shows the detailed ATI6 command response, as it would be sent to the host.

Detailed ATI6 command response:

Time in Data (Sec.): 00000023
Local Retrain/RR: 00/00
Remote Retrain/RR: 00/00
Clock Offset (ppm): 08.8
Round Trip Delay (msec): 0006
RX Level −11.0 dB
TX Level −17 dB
SNR 52.4 dB

ATI6 command response (continued)

The following describes in detail the information provided in this command response:

Line 1 − Time in Data Mode: The time in seconds that the modem has been connected. This value is latched so that it can be read after the call is completed.

Line 2 − Local Retrain/RR: Two pieces of information are presented on this line. The first parameter indicates the number of retrains requested by the local modem. The second parameter indicates the number of rate renegotiations requested by the local modem. Higher values indicate an unstable connection. These values are latched so that they can be read after the call is completed.

Line 3 − Remote Retrain/RR: Same as 2 but as requested by the remote modem.

Line 4 − Clock offset (ppm = parts per million): Represents a measure of the difference in clock frequency between the local and the remote modems. The larger this number, the more difficult it is for the modem to maintain reliable data transfers. A large value for clock offset may indicate a clock frequency problem on the local or remote modem.

LIne 5 − Round trip (or “bulk”) delay: This value represents a measure in milliseconds of the propagation delay present in the telephone network. This delay consists of the total round trip time delay for a signal to propagate from the modem transmitter, through the network to the remote connection, and back. Although this parameter may not be significant to a user, it is critical for certain aspects of internal modem operation. For the modern digital telephone network, coast to coast delays in the US are generally between 30 − 100 msec. Local calls will have a smaller delay, while calls to various international locations may exhibit a significantly larger value.

Line 6,7 − RX/TX Levels: Measure in dB of the level of the signal present at the modem’s receiver and transmitter, respectively. For V.90 connections, nominal levels for these parameters are generally in the range of −10 to −20 dB. For other modulations, these values may vary widely.

Line 8 − SNR: Signal to Noise Ratio in dB. A measure of the relative amount of undesirable signal qualities present in the modem’s received signal. Higher values indicate less noise compared to the desired signal. A high−speed data connection (50 Kbps or higher) requires an SNR of 50 dB or greater.

non-volatile EEPROM initialized configuration storage

The 54V90 modem provides for the capability to store several types of initialized information in an external serial EEPROM, to be saved in a non-volatile form for recall at a later time, even after the modem has been powered off. The information storable in EEPROM includes numerous AT command configurations set up by the user, many S-Register settings, and various other operating parameters.

EEPROM functionality is supported by two AT commands — ATZ and AT&W. The AT&W command stores information to the EEPROM. The information stored by the AT&W command is retrieved either on power-up or with the ATZ command.

To allow use of the software support for information storage in the external serial EEPROM, the EEPROM should be connected as shown in the reference design schematics in this document. If the AT&W command is invoked and the EEPROM is not installed, the command response is ERROR.

non-volatile EEPROM initialized configuration storage (continued)

The information stored in the EEPROM is shown below. Note that the selected country code is saved in EEPROM automatically without the use of AT&W. Configuration parameters saved by AT&W:

- E,L,M,T,P,Q,V,X,Y
- &C,&D,&G,&H,&K,&L,&R,&S,&P
- %C,%K,%O,%I,%V
- \C,\G,\K,\N,\T,\V
- +VCDT,+VCID
- BskyB Enable (when selected with *Y254:W6189,1)
- !X, !C
- S0,6,7,8,10,25,30,38,71,72,100,102,231
- In alternate response mode (AT!C1 mode): B, W, &Q, N

parallel phone exclusion relay control

The 54V90 modem provides the capability to use the DSP XF output to control an external relay, which can be used to isolate an external telephone handset from the phone line when system conditions require this.

Control of the XF output state to support a variety of system configurations is provided. Software control of the XF output for exclusion relay control is implemented through the AT!X commands (see AT command set description for additional information).

The functionality of the exclusion relay control is implemented assuming the relay used is of a normally closed (when not energized/not activated) configuration. The polarity of the XF output is defined to be that XF is a one when the relay is to be deactivated (closed) and zero when the relay is to be activated (opened). When the system is powered off, the relay will also be deactivated (since no power is available to open the relay) and the phone is connected to the line.

The particular circuitry used to control the relay may vary depending on the specific relay used, however, the functionality described above must be implemented for proper operation.

A functional diagram of the exclusion relay connection is shown in Figure 12.

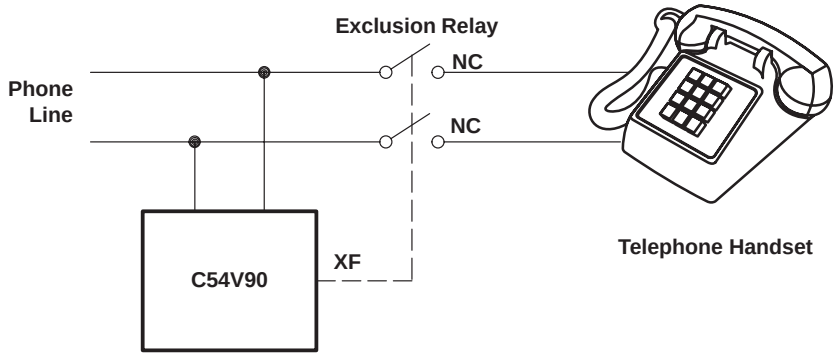


Figure 12. Exclusion Relay Connection Functional Dlagram

connecting HPI interface to ISA bus

The HPI data, control and address lines can be mapped to the ISA bus as shown below. The I/O driver must indirectly address the data memory through the HPIA register, and must also insure that each 16-bit data access is implemented as two 8-bit accesses.

The DSP I/O pins are not 5-V tolerant, so a level translation is required in a 5-V system.

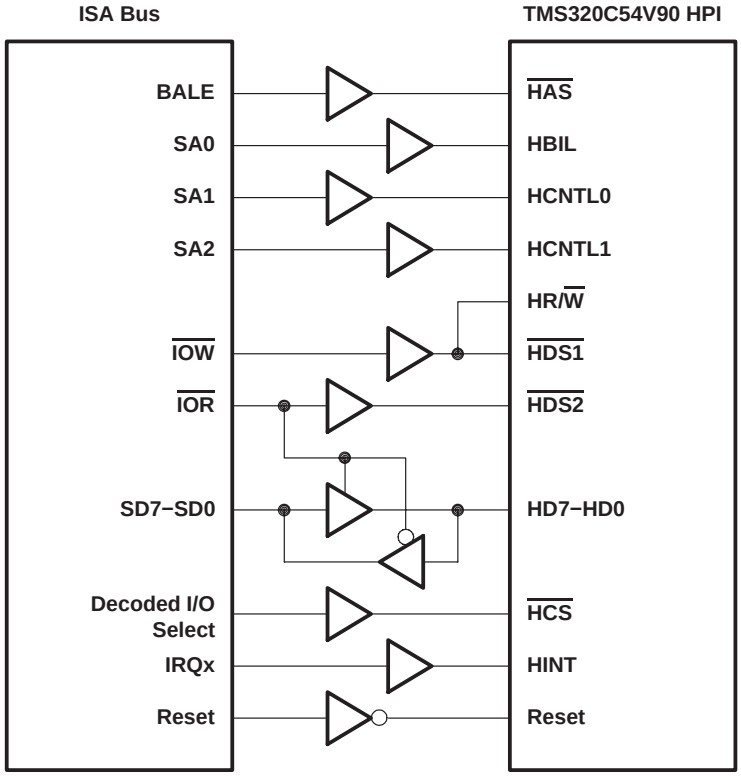


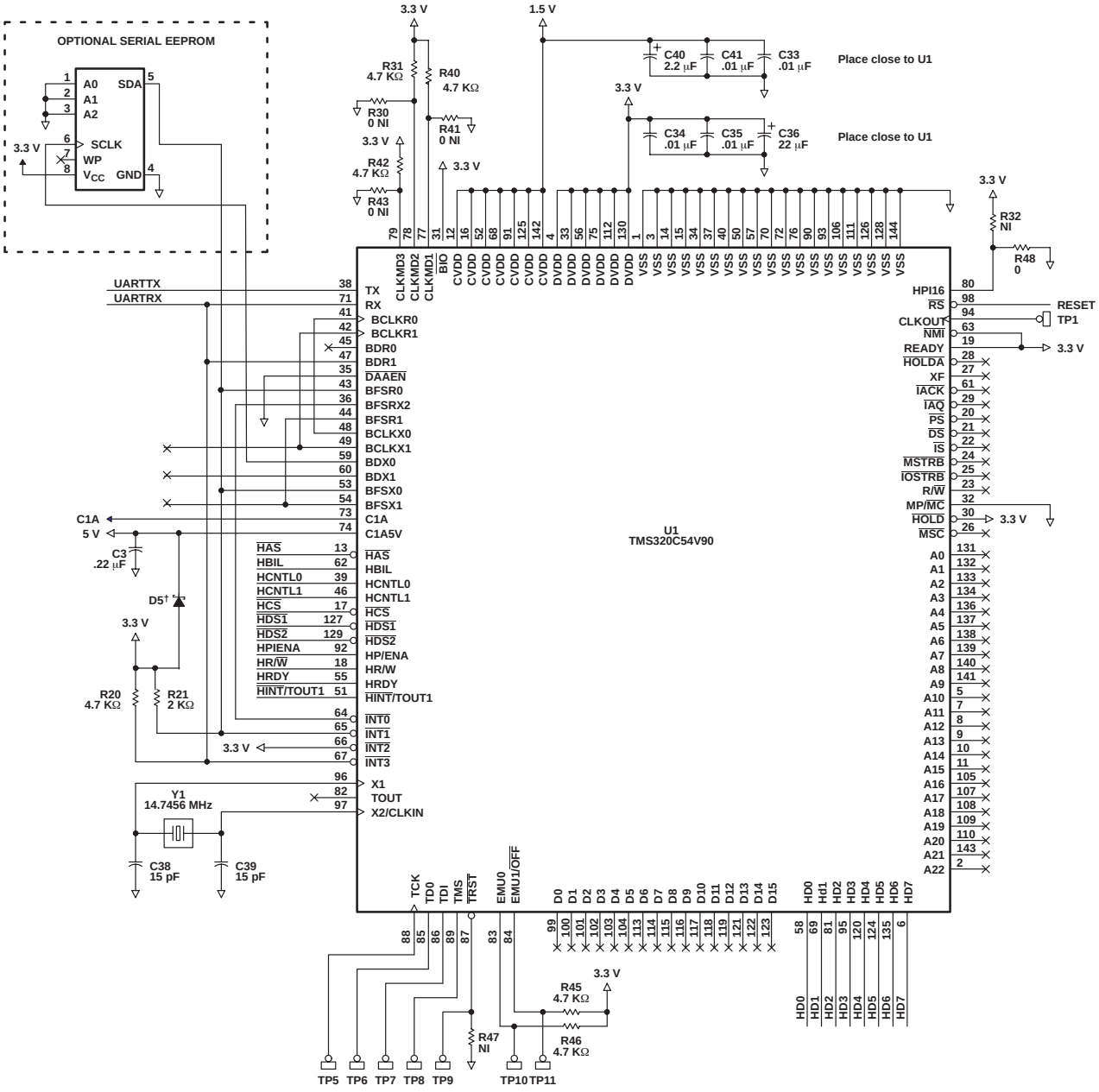
Figure 13. Connecting HPI Interface to ISA Bus

connecting HPI interface to ISA bus (continued)

Table 27. Mapping of I/O Space to HPI Registers

/IOW	SA2	SA1	SA0	FUNCTION
0	0	0	0	Write HPI Control Register Low Byte
0	0	0	1	Write HPI Control Register High Byte
0	0	1	0	Write HPI Data Register Low Byte (with address pre-increment)
0	0	1	1	Write HPI Data Register High Byte (with address pre-increment)
0	1	0	0	Write HPI Address Register Low Byte
0	1	0	1	Write HPI Address Register High Byte
0	1	1	0	Write HPI Data Register Low Byte (without address pre-increment)
0	1	1	1	Write HPI Data Register High Byte (without address pre-increment)
1	0	0	0	Read HPI Control Register Low Byte
1	0	0	1	Read HPI Control Register High Byte
1	0	1	0	Read HPI Data Register Low Byte (with address post-increment)
1	0	1	1	Read HPI Data Register High Byte (with address post-increment)
1	1	0	0	Read HPI Address Register Low Byte
1	1	0	1	Read HPI Address Register High Byte
1	1	1	0	Read HPI Data Register Low Byte (without address post-increment)
1	1	1	1	Read HPI Data Register High Byte (without address post-increment)

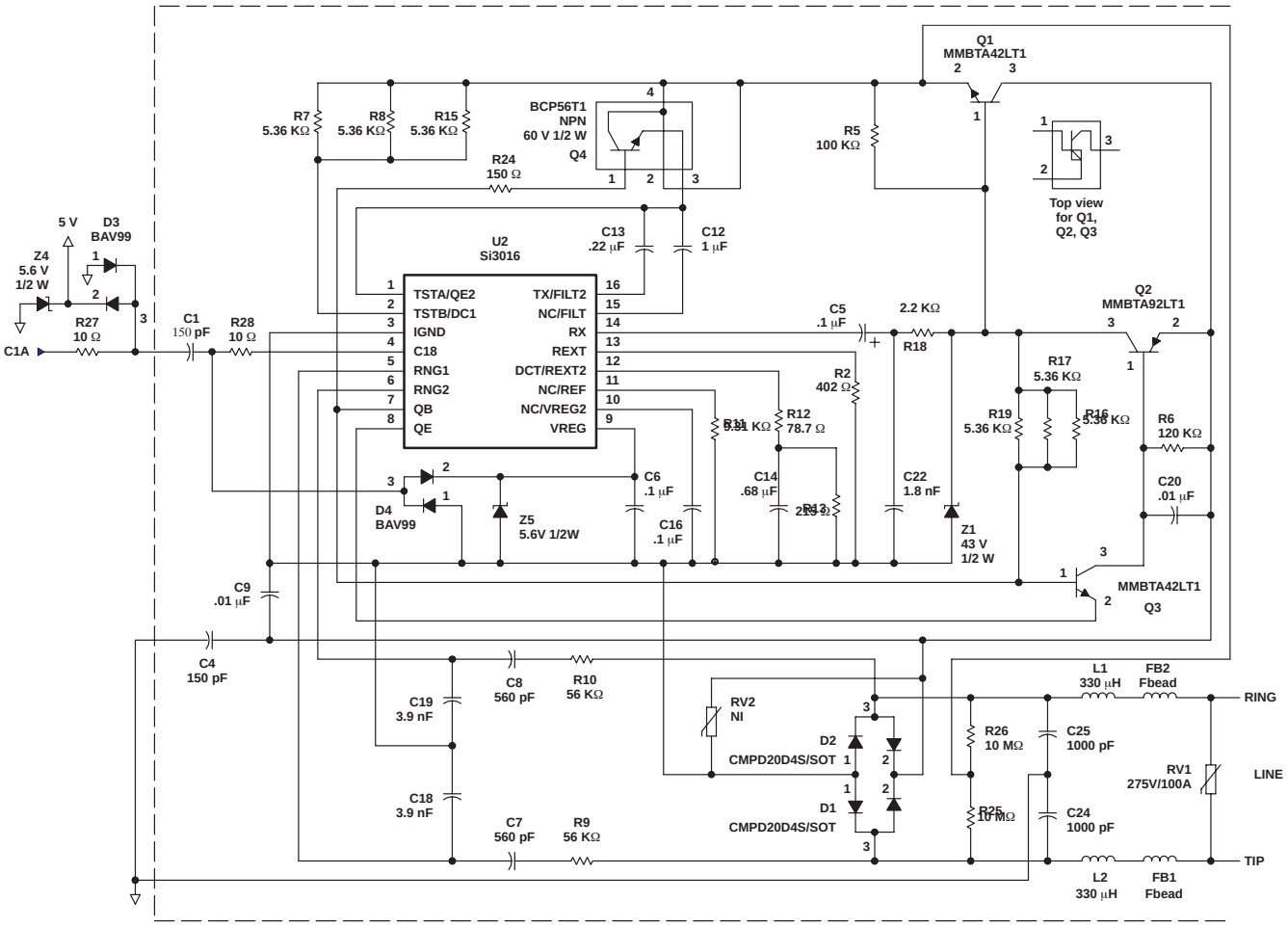
TMS320C54V90 SCHEMATIC



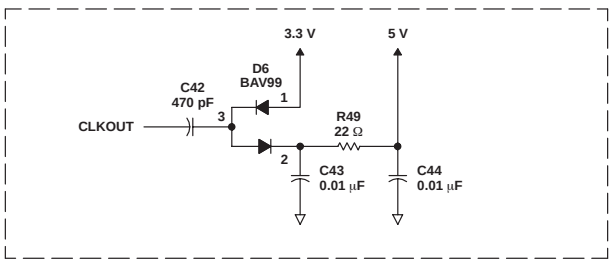
† D5 only required if C1A5V is not > DV_{DD} − 0.5 V during power up, see the Recommended Operating Conditions table.

TMS320C54V90 SCHEMATIC (CONTINUED)

Q4 needs a 100-mm square pad area on top of board. Place same area on bottom of PCB. Connect top and bottom areas areas with feed through holes for heat conduction. Q4 will dissipate 0.5W max. under worst case condition.



Optional 5 V Charge Pump†



†This circuit can be used, if desired, to provide 5 V supply for the TMS320C54V90

TMS320C54V90 SCHEMATIC (CONTINUED)

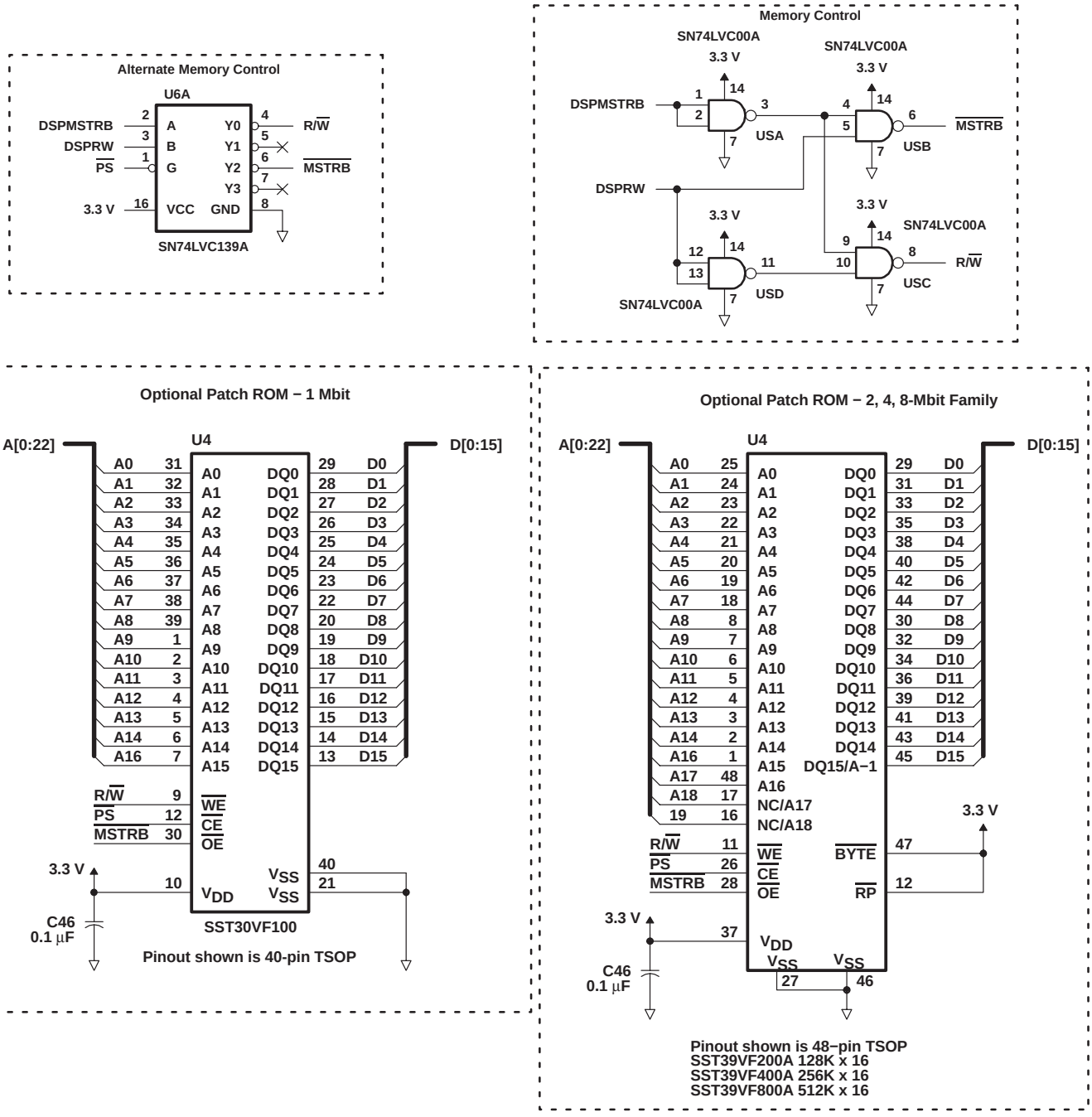


Table 28. Bill of Materials

ITEM	QUANTITY	REFERENCE	VALUE	PCB FOOTPRINT	MFR PART NUMBER
1	2	C4, C1	150pF	1808 20% 3KV X7R	Required to be Y2-compliant capacitors
2	1	C5	.1µF	10% 50v Case A TANT	
3	2	C6, C16	.1µF	0603 10% 16v X7R	
4	2	C7, C8	560pF	0805 20% 250V X7R	
5	1	C9	.01µF	0805 20% 250V X7R	
6	5	C20, C33, C34, C35, C41	.01µF	0603 20% 16V X7R	
7	1	C12	1µF	20% 16v TANT Case A	
8	2	C3, C13	.22µF	0603 10% 16V X7R	
9	1	C14	.68µF	20% 16V TANT Case A	
10	2	C18, C19	3.9nF	0603 20% 16v X7R	
11	1	C22	1.8nF	0603 20% 50V X7R	
12	2	C24, C25	1000pF	1812 3KV X7R	Required to be Y2-compliant capacitors
13	1	C36	22µF	A case 6.3v	
14	2	C39, C38	15pF	0603 5% 50v NPO	
15	1	C40	2.2µF	A case 6.3v	
16	2	D2, D1	CMPD2004S	SOT−23	Central Semi
17	2	D4, D3	BAV99	SOT−23	Diodes Inc BAV99−7 On Semi Fairchild Zetex BAV99TA
18	2	FB2, FB1	Fbead	0805	Murata BLM21B102S
19	2	L1, L2	330µH		Sporton RCP0408−301K01
20	2	Q3, Q1	MMBTA42LT1	SOT−23	
21	1	Q2	MMBTA92LT1	SOT−23	
22	1	Q4	BCP56T1 NPN 60v 1/2W	SOT−223	
23	1	RV1	275V/100A	DO−214AA	ST SMP100−270LC Teccor P3100SB
24	1	R2	402	1206 1% 1/8W 1210 (SMTPCB pads)	
25	1	R5	100k	0603 1% 1/16W	
26	1	R6	120k	0603 5% 1/16W	
27	6	R7, R8, R15, R16, R17, R19	5.36k	1210 1% 1/4W	
28	2	R9, R10	56K	0805 5% 1/10W	
29	1	R11	9.31K	0603 1% 1/16W	
30	1	R12	78.7	0603 1% 1/16W	

† D5 only required if C1A5V is not > DV_{DD} − 0.5 V during power up, see the Recommended Operating Conditions table.
NOTE: Contact Texas Instruments to obtain an Excel spreadsheet version of this Bill of Materials, if desired.

Table 28. Bill of Materials (Continued)

ITEM	QUANTITY	REFERENCE	VALUE	PCB FOOTPRINT	MFR PART NUMBER
31	1	R13	215	0603 1% 1/16W	
32	1	R18	2.2k	0805 5% 1/10W	
33	7	R20, R21, R31, R40, R42, R45, R46	4.7k	0603 5% 1/16W	
34	1	R24	150	0603 5% 1/16W	
35	2	R25, R26	10M	0805 5% 1/10W	
36	3	R30, R41, R43	0 NI	0603 5% 1/16W	(NI = not installed)
37	2	R32, R47	NI	0603 5% 1/16W	(NI = not installed)
38	1	R48	0	0603 5% 1/16W	
39	2	R27, R28	10	0805 5% 1/10W	
40	11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	TEST POINT	(not a part)	
41	1	U1	TMS320C54V90		
42	1	U2	Si3016	SOIC−16 (0.05 pitch, 0.153 body width)	
43	1	Y1	14.7456 MHz	HC−49/US	Fundamental Mode, parallel resonant, 30Ω ESR max, 10 pF Cload.
44	1	Z1	43V 1/2W	SOD−123	Diodes Inc BZT52C43 General Semi MMSZ5260B
45	2	Z4, Z5	5.6V 1/2W	SOD−123	Diodes Inc BZT52C5V6−13 General Semi MMSZ5232B
46	1	D5†	Schottky	2.5 x 5 mm	Panasonic MA2Q735 Toshiba CRS03 Rohm RB160L−40
OPTIONAL COMPONENTS					
1	1	C42	470pF	0603 10% 50V NPO	
2	2	C43, C44	.01µF	0603 20% 16V X7R	
3	1	D6	BAV99	SOT−23	Diodes Inc. BAV99-7 On Semi Fairchild Zetex BAV99TA
4	1	R49	22	0603 5% 1/16W	

† D5 only required if C1A5V is not > DV_{DD} − 0.5 V during power up, see the Recommended Operating Conditions table.
NOTE: Contact Texas Instruments to obtain an Excel spreadsheet version of this Bill of Materials, if desired.

general DAA layout guidelines

description

The integrated DAA provides a very high level of integration for modem designs. Integration of the analog front end (AFE) and hybrid, and the removal of the transformer, relays, and opto-couplers reduces the layout effort considerably. The DAA consists of two parts—the DSP-side and the line-side. When designing with the DAA, there are several layout guidelines that will assist the designer in attaining telecom, safety, and EMC approvals.

This document is divided into six main sections: operational items, analog performance related items, EMC items, safety items, assembly items, and thermal considerations. Operational items are defined as those items that must be followed to ensure functionality of the solution. Analog performance related items are layout recommendations that are pertinent to the analog performance of the solution. EMC items are those items that will affect the emissions/immunity performance of the solution. Safety items are layout issues that could impact safety requirements of a particular modem solution. Assembly items are items that should be noted to assist in assembly of the solution. Thermal considerations are those items that may affect operational performance due to extreme temperatures.

operational guidelines

Figure 14 depicts the placement of the chipset, some of the major discrete components, and the RJ11 connector. Note the placement of the DSP and the Si3016. Aligning these devices so that pins 73/74 of the DSP face pins 1–8 of the Si3016 will aid in following some of the more specific layout guidelines. Utilizing this placement will also allow the design to closely resemble the example layout, enabling the designer to directly follow these guidelines.

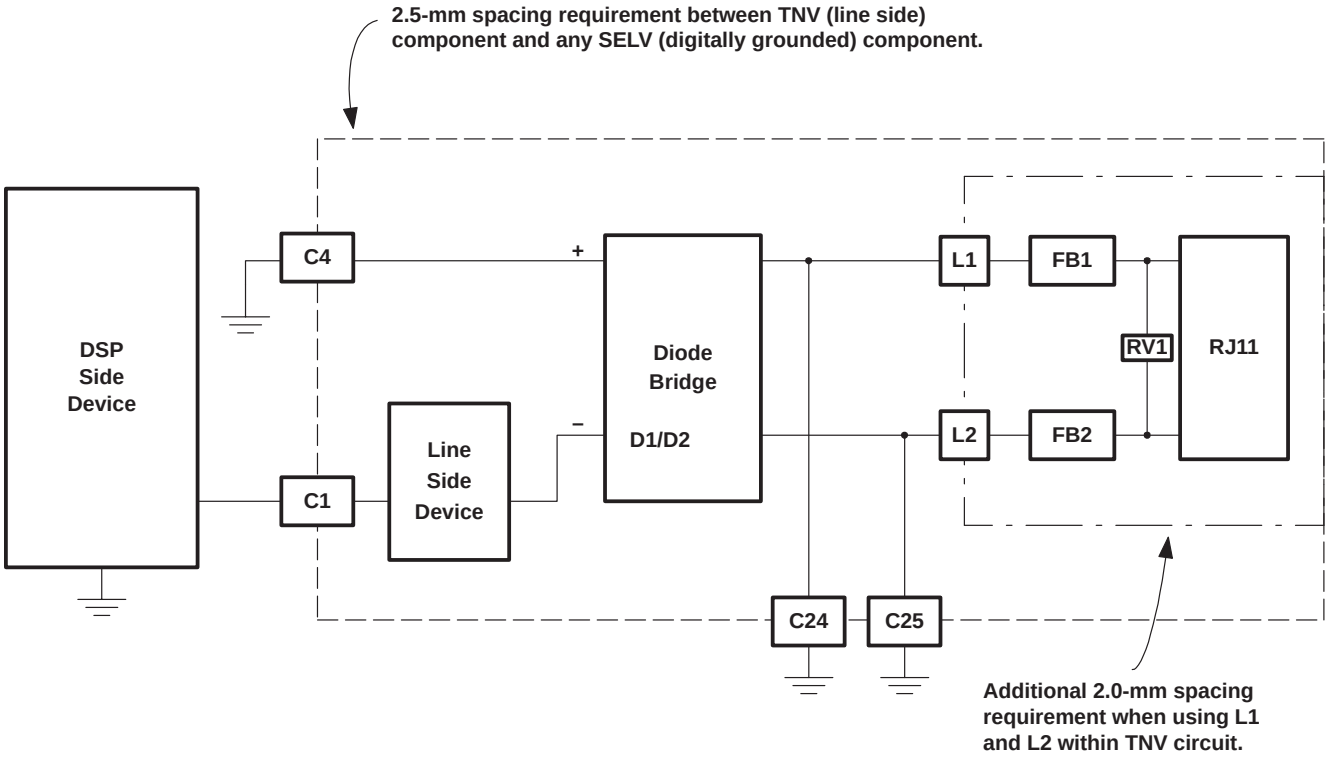


Figure 14. Chipset Diagram

layout requirements

For the line-side chip (U2), the primary layout considerations are the placement and routing of C6, C9, C16, D1, D2, and RV2.

Capacitors C6 and C16 provide regulation of the supplies powering U2. The loop formed by C6 to pins 3 and 9 and the loop formed by C16 to pins 3 and 10 should be made as small as possible. Figure 15 shows an example of how to minimize these loops. The trace back to pin 3 is thicker because multiple loops use this path. The thicker trace has a lower impedance, which lessens the effect of multiple currents in that trace.

Capacitor C9, dual diodes D1 and D2, and the MOV RV2 form a loop that should be minimized. C9 performs a low pass filter function on the transmit and receive signals. The inductance in the loop from C9 to the diode bridge (D1 and D2) can affect the ability of C9 to suppress out-of-band energy. See Figure 16 for a layout example.

The placement of capacitors C12 and C13 is also important because these components are in high gain loops. Noise in these loops may affect the signals at TIP and RING. The loop formed from pin 15 through C12 to pin 1 (QE2) and the loop formed from pin 16 though C13 to pin 1 should be routed as short as possible. Figure 15 illustrates an example of these loops. Also, the trace from Q4 pin 3 (emitter) should connect directly to the QE2 pin and should not share the same route as the C12 and C13 capacitors to QE2.

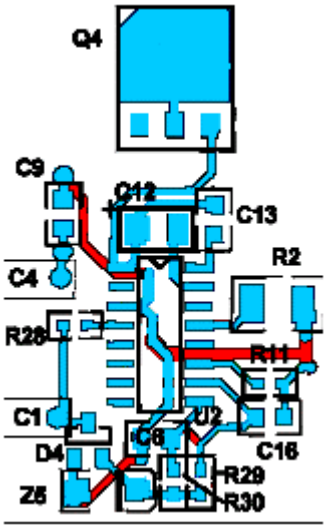


Figure 15. Routing for C6, C16, C12, C13, Q4, R2, and R11

analog performance

The components on the line side of the DAA are composed of a small digital interface section (capacitor barrier interface, converters, and control logic), and the remaining components are used for either analog circuits (hybrid, dc impedance, ac impedance, ringer impedance, etc.) or safety and EMC (surge protector, ferrite beads, EMC capacitors, etc.).

Routing all traces in the DAA section with 15 mil or greater traces when possible will ensure high overall analog performance of the silicon DAA. Furthermore, the DAA section should not use a ground plane for the IGND signal; instead the IGND signal should be routed using a 20-mil trace. Thermal considerations may also be affected by the size of the IGND trace. See the Thermal Considerations section.

After placing C6, C12, C13, and C16, the designer should focus on placing R11 and routing the trace from Q4 pin 3 to U2 pin 1 using as small a loop as possible to ensure good analog performance. Due to the relatively high current that can flow in the trace from Q4 pin 3 to U2 pin 1, this trace should be routed separately from the trace coming from C12 and C13 to pin 1. This will ensure that the current from Q4 will not affect the sensitive C12 and C13 loops. Figure 15 illustrates an example of the placement and routing of R11, Q4, and U2.

EMC

Several sources conduct or radiate EMC from/to electronic apparatus. Among these are the following:

- Antenna loops formed by ICs and their decoupling capacitors
- PC-board traces carrying driving and driven-chip currents
- Common impedance coupling and crosstalk

To minimize EMC-related problems, all extraneous system noise and the effects of parasitic PC-board trace antennas must be reduced. Employment of an effective system shielding may also be necessary. The following section discusses how to minimize the EMC problems that can occur on the DAA design.

Capacitors C1, C2, C4, and C9 provide the path for the isolation currents. The typical application schematic recommends that C2 not be installed. If C2 is not installed, the isolation current flows in the following manner:

1. From the DSP C1A pin
2. Across C1 to pin 4 of the Si3016 (U2)
3. From pin 4 to pin 3 of U2
4. To C9
5. Across C9 to C4
6. And finally, across C4 to ground

Because the isolation signal operates around 2 MHz, it is important to keep the path of the signal as small as possible (see Figure 16).

EMC (continued)

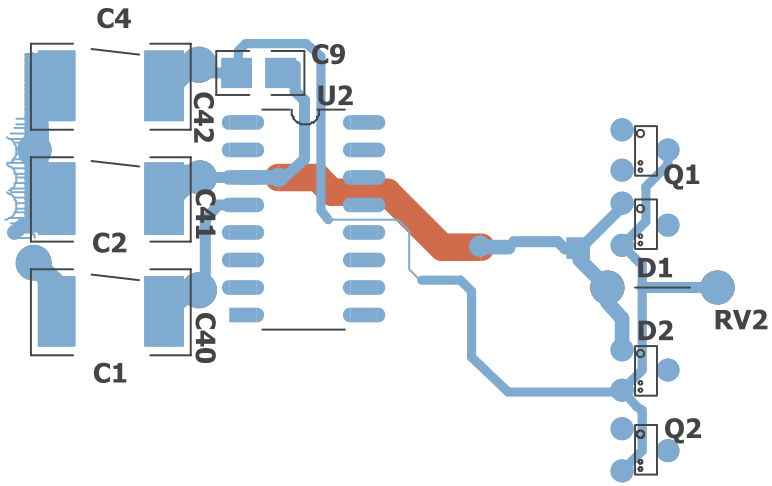


Figure 16. Isolation Interface and Diode Bridge

Short, direct routes using thick 20 mil minimum traces, should be used to connect the isolation capacitors to their respective pins. The GND side of these caps should be connected directly to ground, as close to the DSP as possible. The IGND side of C2 should connect directly to the IGND pin of the Si3016. It is acceptable to use a long trace to connect C4 to the Q1 pin 3 node, as long as there is an IGND trace that follows the C4 to Q1 trace.

For those designs that exhibit emission problems related to the isolation interface, the C30 capacitor may be installed. C30 will shunt some of the high frequency energy and reduce emissions due to the harmonics of the isolation link.

FB1, FB2, RV1, C24, C25, C31, and C32, and if implemented, a fuse should be placed as close as possible to the RJ11 as shown in Figure 17. It is important for the routing from the RJ11 connector through the ferrite beads FB1 and FB2 to be well matched. The routing to C24 and C25 should also be well matched. The distance from the TIP and RING connections on the RJ11 through the EMC capacitors C24 and C25 to chassis ground should be kept as short as possible. If possible, the routing through the ringer network to the line-side device pin 5 and pin 6 should also be well matched as shown in Figure 18.

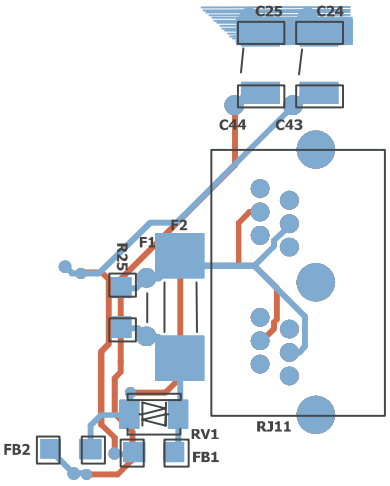


Figure 17. RJ11

EMC (continued)

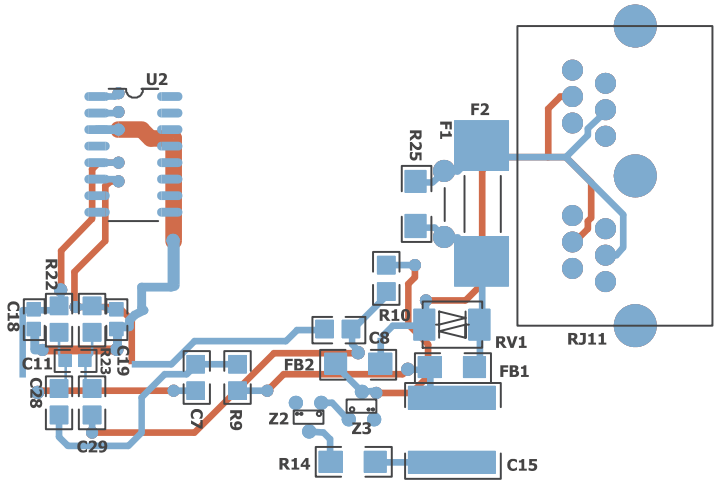


Figure 18. Ringer Network

Routing all the connections from RJ11 to FB1, FB2, RV1, C24, C25, C31, C32, and F1 using a 20-mil trace will improve the EMC performance of the solution.

Good general design practices should be followed to improve the EMC performance of the solution. This includes laying out the digital ground plane as small as possible and rounding off the corners. Placing series resistors on the clock signals near their source and ensuring that the traces from oscillators or crystals are made as short as possible will contribute to the overall emissions performance of the solution.

When using the DAA in unearthed systems, the designer should consider making some modifications to prevent common mode 50/60 Hz signals from entering the signal path. In an unearthed system, a large 50/60 Hz signal can be present between IGND (line-side pin 3) and digital ground. This signal is often as large as 50 V_{RMS}.

The primary consideration is to use well-matched capacitors which bridge the telephone network voltage (TNV) to the safety extra-low voltage (SELV). C1 should match C4, and C24 should match C25. Matching should be within 10%. To the extent that C1 and C24 does not equal C4 and C25, there will be a common mode to differential conversion of the 50/60 Hz signal. Typical common mode rejection of the 50/60 Hz signal is better than 95 dB.

A secondary consideration is capacitive coupling from DGND (SELV) to nodes on the line-side (TNV) circuitry. The most prevalent system design where capacitive coupling occurs is in mini PCI and MDC designs. However, this coupling always exists and can have a noticeable effect on analog performance when SELV is physically close to TNV.

EMC (continued)

For safety considerations, 3-mm spacing is recommended between TNV and SELV (international minimum is 2.5 mm). However, there are three nodes on the line side which require special consideration to insure robust analog performance in unearthed systems:

- RX pin on Si3016
- FILT pin on Si3016
- FILT2 pin on Si3016

For these pins and the traces that connect to these pins, the following guidelines should be followed:

- Whenever possible, keep at least a 5 mm distance between these nodes and SELV.
- An IGND guard ring can be used on the board level. This IGND guard ring should be inserted between SELV and the nodes listed above. For FR4 board material, the IGND guard can be placed on any layer. Optimal placement would be for the IGND guard ring to be on the same layer as the nodes listed above. This guard ring allows SELV to couple into IGND rather than the nodes listed above.
- For designs (e.g., MDC, mini PCI designs) which have TNV circuitry in close proximity (< 5 mm) to a SELV plane, a ay shield can be used to protect against coupling. This coupling occurs through air between the SELV plane and the TNV nodes described above. A small IGND shield can be placed between the TNV nodes and the SELV plane. This plane allows the SELV to couple into IGND rather than the TNV nodes.

safety

The layout of the modem circuitry, in particular the area of the circuit that is exposed to telephone network voltages (TNV), is subject to many safety compliance issues. It is recommended that all customers consult with their safety expert or consultant on the various regulations that could impact their designs. One of the most critical layout issues that relates to safety is to ensure that a minimum 2.5-mm (3-mm preferable) or 100-mil space is provided between safety extra low voltage (SELV) and TNV circuitry. Designs requiring 5 kV isolation between TNV and SELV should use 5 mm minimum spacing.

When L1 and L2 are included in the DAA, the spacing requirements between the TNV circuit and SELV needs to be increased from 2.5 mm to 3.5 mm. This increased spacing requirement compensates for the secondary peaking effects during longitudinal surges resulting from the addition of L1 and L2.

In addition to the increased spacing requirement between TNV and SELV, there is a second spacing requirement within the TNV circuit. During surge events, the voltage across the L1 and L2 inductors can be sufficient to create arcing to nearby TNV nodes. To prevent arcing, it is recommended the opposing terminals of the L1 and L2 inductors be isolated from each other by 2.0 mm. Thus, the nodes corresponding to RV1, FB1, FB2, RJ11, and one terminal of L1/L2, should be isolated by 2.0 mm from nodes that connect to the other terminal of L1/L2.

assembly

There are several steps that can be taken in layout to ensure that the assembly process goes smoothly. For example, an assembly-related error is to install the polarized capacitors with the polarity backwards. This can be prevented by stenciling the board with a plus sign on the correct side of C12, C14, and C5 to indicate the proper orientation for the polarized capacitors. Also, indicating pin 1 on the board with a stencil marking improves the chances that the integrated circuits will be installed correctly. Thought should also be given to using several footprints for a given component to allow for multiple vendor choices. Popular components using multiple footprints are C1, C2, C4, C12, C24, C25, C31, C32, F1, and Z1. Taking these basic steps will assist in the assembly process and ease future troubleshooting.

thermal considerations

When using the DAA in common applications, there are several thermal considerations that should be taken into account. These thermal considerations will ensure that the device is not operating outside of the recommended operating conditions, thus protecting the device from possible degradation.

On small form factor printed circuit board (PCB) designs, the ability of the PCB to dissipate heat becomes a very important design consideration. These small designs will require additional mechanisms to remove the heat from the DAA. For applications with a PCB area of less than approximately 3000 mm^2, thermal design rules should be applied.

check list

Table 29 is a check list that the designer can use during layout. The items marked as required should be taken into consideration first.

Table 29. Layout Check List

✓	#	LAYOUT ITEMS	REQUIRED
		OPERATIONAL ITEMS	
	1	Small loop from C6 to U2 pin 9 and pin 3	Yes
	2	Small loop from C16 to U2 pin 10 and pin 3	Yes
	3	Small loop from C12 to U2 pin 15 and pin 1	Yes
	4	Small loop from C13 to U2 pin 16 and pin 1	Yes
	22	Copper pad heat sink is at least 0.08 sq. in. for Q4.	Yes
		ANALOG PERFORMANCE	
	5	Small loop from R11 to U2 pin 11 and pin 3	Yes
	6	Separate trace from Q4 pin 3 to U2 pin 1 than the trace from C12 and C13 to U2 pin 1	Yes
	7	Minimum of 15 mil traces in DAA section	
	8	Minimum of 20 mil trace for IGND	
	9	No ground plane in DAA section	Yes
	n/a	> 5-mm spacing between SELV and TNV nodes (RX, FILT, FILT2)	Yes
	n/a	IGND guard ring to protect TNV nodes (RX, FILT, FILT2)	Yes
	n/a	IGND Faraday shield to protect TNV nodes (RX, FILT, FILT2)	Yes
		EMC ITEMS	
	10	Small loop formed between U2, C1, C9, and C4.	Yes
	11	Minimum of 20 mil trace from DSP to C1, C9, and C4 and from U2 to C1 and C9	
	12	FB1, FB2, and RV1 placed as close as possible to the RJ11	Yes
	n/a	Routing from TIP and RING of the RJ11 through F1 to the ferrite beads is well matched	Yes
	16	Distance from TIP and RING through EMC capacitors C24 and C25 to Chassis Ground is short	Yes
	17	C9 is located near C4	
	n/a	C4 is located with C2 between DSP and U2	
	18	Minimum of 20 mil trace from RJ11 to FB1, FB2, RV1, C24, C25, C31, C32, and F1	
	19	Routing of TIP and RING signals from the RJ11 through the ringer networks to U2 pin 5 and pin 6 is well matched	
	20	Trace from D1 & D2 to IGND and to C4–C9 node is well matched and forms a small loop.	
	21	DGND return paths for C10 and C3 should be on component side.	
	n/a	Digital Ground plane is made as small as possible	
	n/a	Ground plane has rounded corners	
	n/a	Series resistors on clock signals are placed near source	

check list (continued)

Table 29. Layout Check List (Continued)

✓	#	LAYOUT ITEMS	REQUIRED
		SAFETY ITEMS	
	23	Additional 2 mm spacing for inductors (if necessary)	
	24	Minimum 2.5-mm (100 mils) between SELV and TNV (3.0-mm or higher recommended, see Safety section)	Yes
	n/a	Space for fire enclosure	
		ASSEMBLY ITEMS	
	26	Polarity for C5 is negative side connects with U2 pin 14	
	27	Polarity for C12 is negative side connects with U2 pin 15	
	n/a	Polarity for C14 is negative side connects with U2 pin 3 (IGND)	

check list (continued)

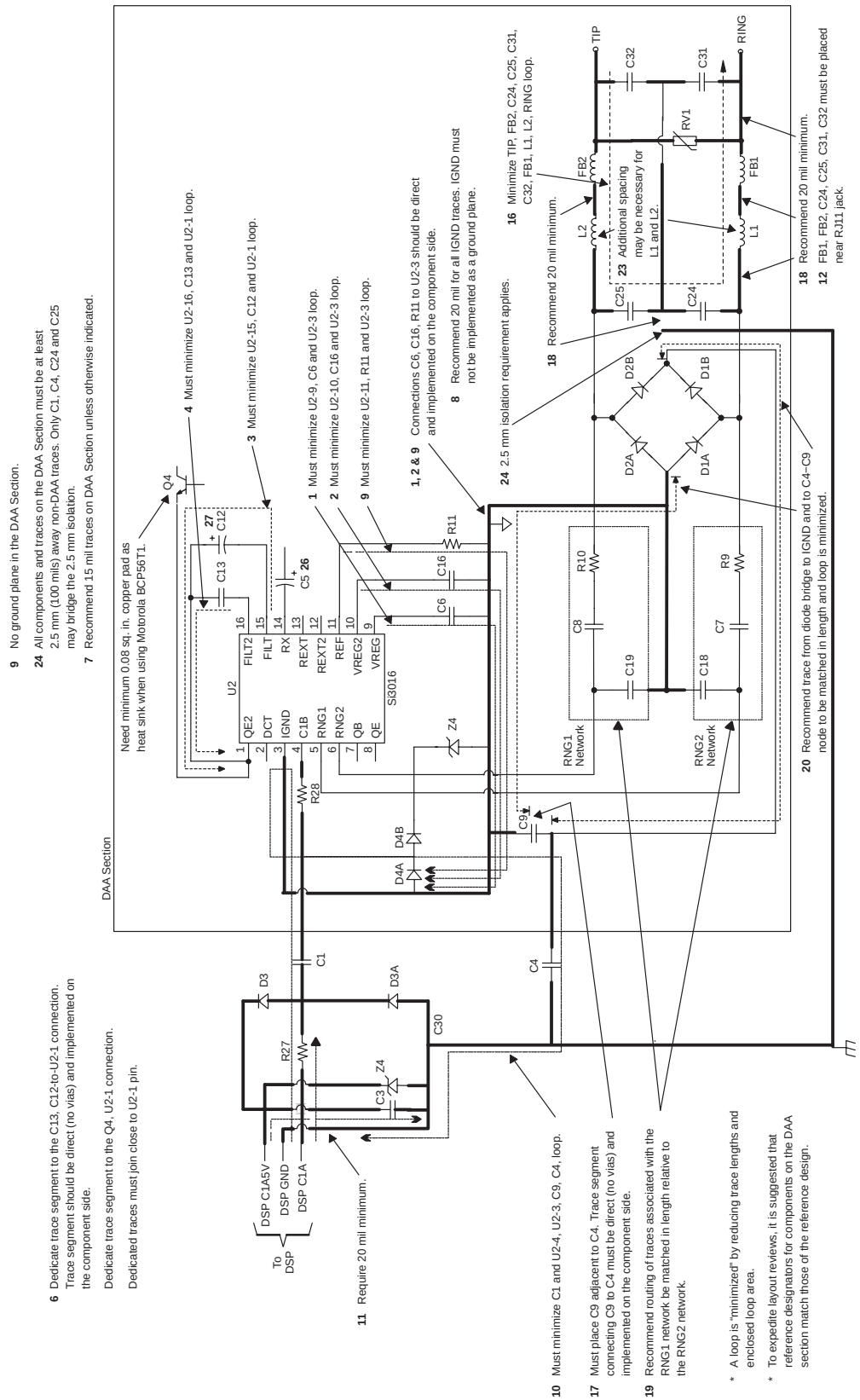


Figure 19. TMS320C54V90 Modem Layout Guidelines

additional TMS320C54V90-to-Si3016 layout guidelines

purpose

This section discusses layout issues specific to the TMS320C54V90. The layout guidelines in the previous section discuss the generic layout issues associated with the DAA circuit, especially the IC and components on the line side of the isolation barrier.

In TMS320C54V90, the line side device is the Si3016. The digital portion of the DAA is not a separate chip, but has been integrated into the TMS320C54V90 DSP.

capacitively coupled data link

A digital data link carries samples of the modem signal and control information between the two parts of the DAA. The link is bidirectional and capacitively coupled for isolation. The link runs between C1A (pin 73) of the DSP and C1B (pin 4) of the Si3016.

The load capacitance on the C1A pin is critical. The driver is designed for a maximum load capacitance of 10 pF. Excessive capacitive load will degrade the link signal and may cause erratic operation or increased sensitivity to external noise sources.

DAA 5V

The DSP has an input pin, C1A5V (pin74), which is an input for a 5V supply used only by the C1A driver. This pin needs to be bypassed for low noise. There are also some surge protection components that connect to 5 V. These connections should be short and direct.

layout guidelines

The following layout guidelines are intended to:

- minimize the capacitive load on C1A
- bypass the 5-V supply
- provide effective surge protection

The component reference designators refer to the TMS320C54V90 reference design.

1. The DSP and the Si3016 should be located close together and oriented so that there is a short direct path from C1A to C1B. This path should be no longer than 25 mm.
2. The connection from C1A to C1B, through R27, C1, and R28 should be made with all components and circuit traces on the same side of the board (no vias).
3. There shall be no ground or power planes under C1, or R28. The planes may be removed under the trace from C1A to R27, and under R27, but it is not essential.
4. A 0.22-uF bypass capacitor should be connected to the C1A5V pin as close as possible to the pin, and the other side connected to a ground plane.
5. The connections from Z4 and D3 to the C1A5V pin should be as short and direct as possible. Avoid vias.
6. Some early versions of the Reference Design had a 10 pF cap from C1A to ground or from the junction of R27/C1 to ground. This was optional and intended for EMI suppression if needed. This cap should not be installed under any circumstances.

layout guidelines (continued)

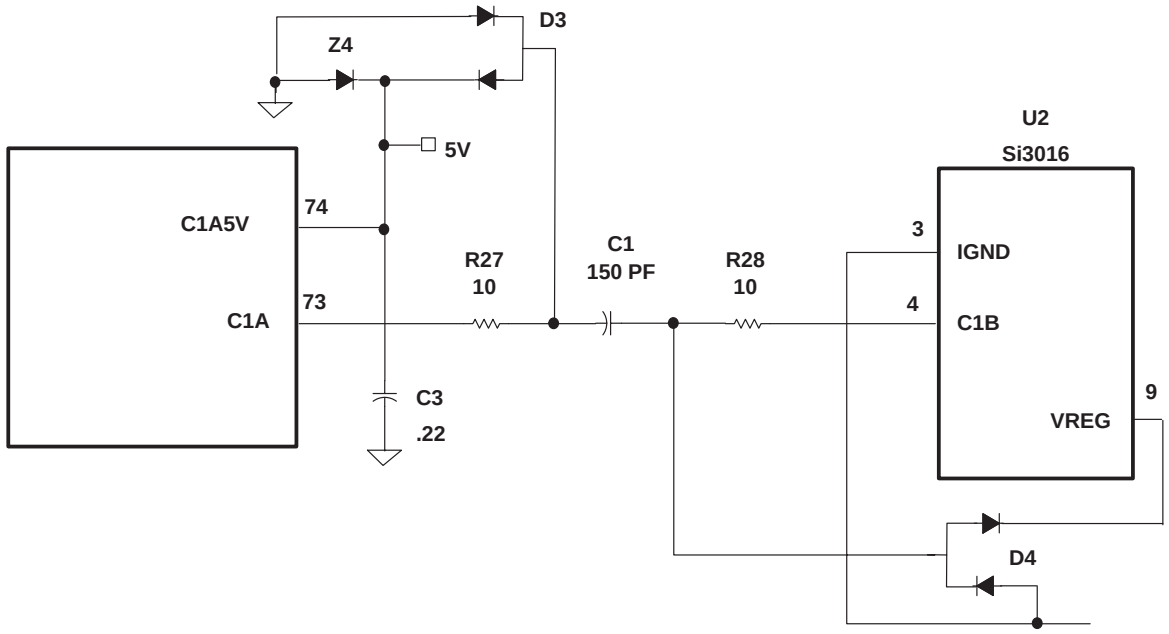


Figure 20. Partial Schematic

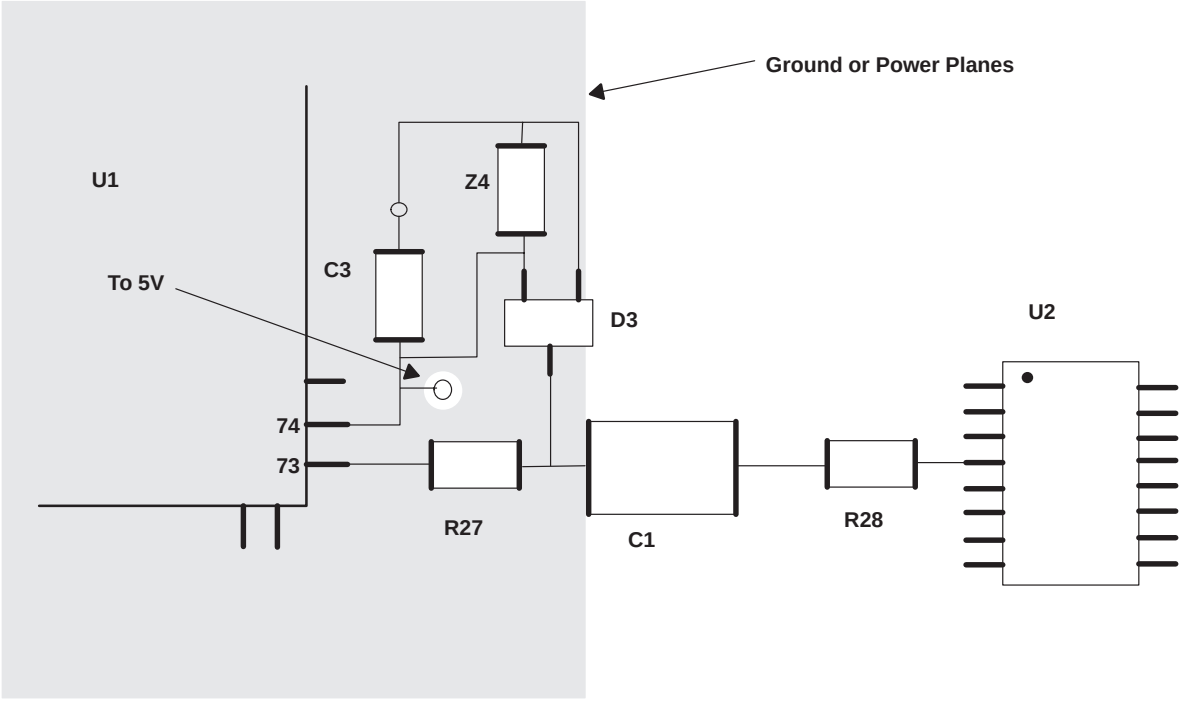


Figure 21. Example Layout

enhanced overvoltage protection

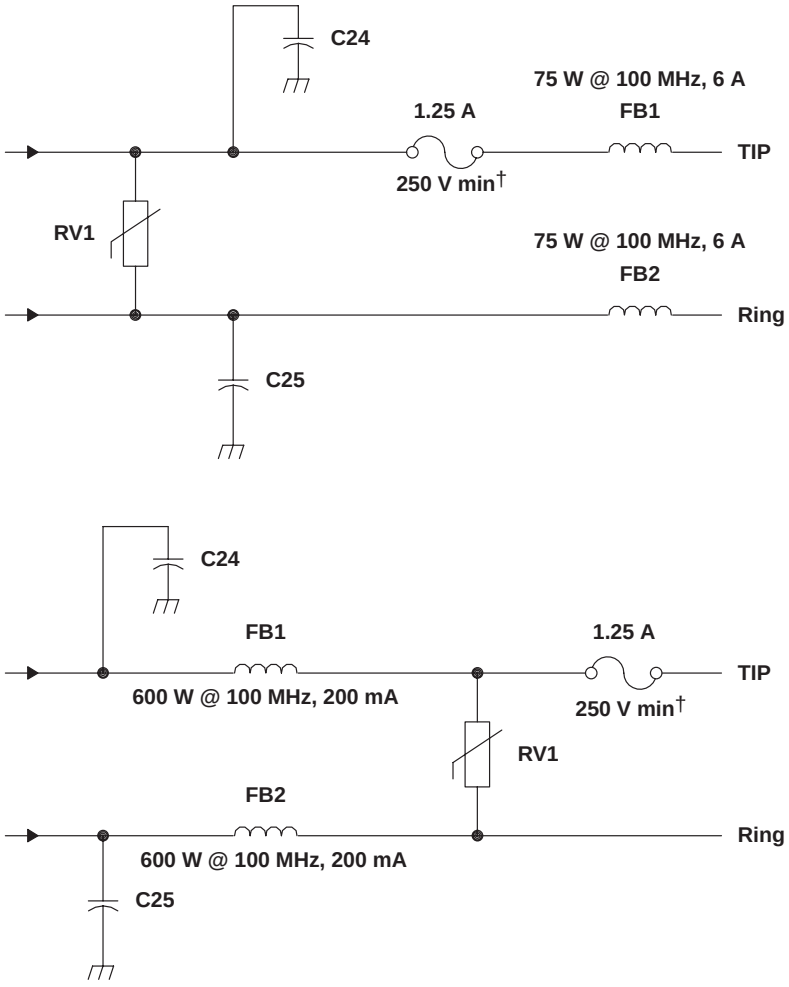
Although designs using the Si3016 comply with UL1950 3rd Edition and pass all over-current and over-voltage tests, there are still several issues to consider.

Figure 22 shows two designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 22 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 22 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests will apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your professional testing agency during the design of the product to determine which tests apply to your system.

enhanced overvoltage protection (continued)



† Teccor FI250T or equivalent.

Figure 22. Circuits that Pass All UL1950 Overvoltage Tests

special telephone interface considerations

ringer impedance

The ring detector in a typical DAA is AC coupled to the line with a large, 1 uF, 250 V decoupling capacitor. The ring detector on the Si3016 is also capacitively coupled to the line, but it is designed to use smaller, less expensive 1.8 nF capacitors. Inherently, this network produces a very high ringer impedance to the line on the order of 800 to 900 kW. This value is acceptable for the majority of countries, including FCC and CTR21.

Several countries including the Czech Republic, Poland, South Africa and South Korea, require a maximum ringer impedance. For Poland, South Africa, and South Korea, the maximum ringer impedance specification can be met with an internally synthesized impedance by setting the RZ bit in Register 16.

ringer impedance (continued)

For Czech Republic designs, an additional network comprised of C15, R14, Z2, and Z3 is required. (See Figure 23 and Table 30.) This network is not required for any other country. However, if this network is installed, the RZ bit should not be set for any country.

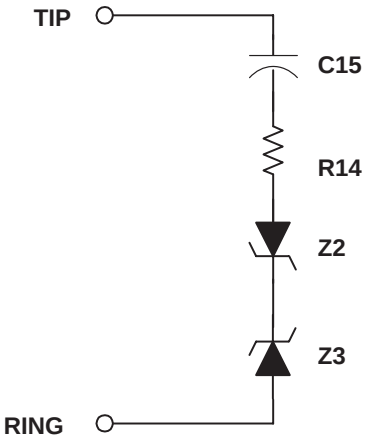


Figure 23. Ringer Impedance Network

Table 30. Component Values—Optional Ringer Impedance Network

SYMBOL	VALUE
C15	1 µF, 250 V
R14	7.5 kW, 1/4 W
Z2,Z3	5.6 V

billing tone detection

“Billing tones” or “metering pulses” generated by the central office can cause modem connection difficulties. The billing tone is typically either a 12-kHz or 16-kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors related to the modem data. The Si3016 has a feature which allows the device to provide feedback as to whether a billing tone has occurred and when it ends.

Billing tone detection is enabled by setting the BTE bit (Register 17, bit 2). Billing tones less than 1.1 Vpk on the line will be filtered out by the low pass digital filter on the Si3016. The ROV bit is set when a line signal is greater than 1.1 Vpk, indicating a receive overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the line-derived power supply of the line-side device (Si3016). When the BTD bit is set, the DC termination is changed to an 800 W DC impedance. This ensures minimum line voltage levels even in the presence of billing tones.

billing tone detection (continued)

The OVL bit (Register 19) should be polled following a billing tone detection. When the OVL bit returns to zero, indicating that the billing tone has passed, the BTE bit should be written to zero to return the DC termination to its original state. It will take approximately one second to return to normal DC operating conditions. The BTD and ROV bits are sticky, and they must be written to zero to be reset. After the BTE, ROV, and BTD bits are all cleared, the BTE bit can be set to reenable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA will remain off-hook during a billing tone event, the received data from the line will be corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries/customers.

Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

billing tone filter (optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. (The Si3016 can remain off-hook during a billing tone event, but modem data will be lost in the presence of large billing tone signals.) The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 24 shows an example billing tone filter. Figure 25 shows the billing tone filter and the ringer impedance network for the Czech Republic. Both of these circuits may be combined into a single external dongle.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

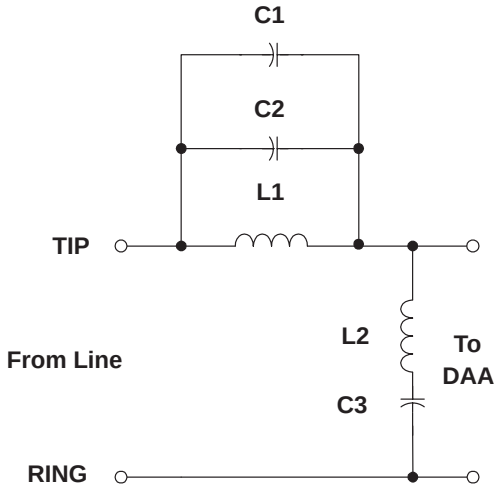


Figure 24. Billing Tone Filter

billing tone filter (optional) (continued)

Table 31. Component Values—Optional Billing Tone Filters

SYMBOL	VALUE
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 W, ±10%
L2	10 mH, >40 mA, <10 W, ±10%

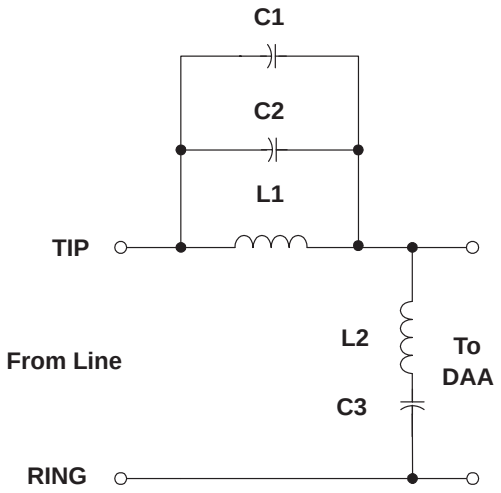


Figure 25. Dongle Applications Circuit

The billing tone filter affects the AC termination and return loss. The current complex AC termination will pass worldwide return loss specifications both with and without the billing tone filter by at least 3 dB. The AC termination is optimized for frequency response and hybrid cancellation, while having greater than 4 dB of margin with or without the dongle for South Africa, Australia, CTR21, German, and Swiss country-specific specifications.

absolute maximum ratings

Differential Voltage Tip to Ring (steady-state, excluding surges) . . . . . 275 V
Voltage Tip-to-Ground or Ring-to-Ground . . . . . 2000 V
Supply voltage I/O range, DV_{DD} . . . . . −0.3 to 4.0 V
Supply voltage core range, CV_{DD} . . . . . −0.3 to 2.0 V
Input Voltage- Logic inputs . . . . . −0.3 to 4.5 V
Output Voltage . . . . . −0.3 to 4.5 V
Operating case temperature range . . . . . 0°C to 100°C
Storage temperature . . . . . −40°C to 150°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
T_C	Operating case temperature		0		100	°C
DV_{DD}	Supply voltage, I/O†		2.7	3.3	3.6	V
CV_{DD}	Supply voltage, DSP core		1.42	1.5	1.65	V
C1A5V	Supply voltage, DAA‡		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{RS}$, $\overline{INTn}$, $\overline{NMI}$, X2/CLKIN, $\overline{BIO}$, BCLKR0, BCLKR1, BCLKR2, BCLKX0, $\overline{BCLKX1}$, $\overline{BCLKX2}$, $\overline{HCS}$, $\overline{HDS1}$, $\overline{HDS2}$, TCK, CLKMDn	2.4		V_{CC} + 0.3	V
		All other inputs	2		V_{CC} + 0.3	
V_{IL}	Low-level input voltage		−0.3		0.8	V
I_{OH}	High-level output current				−300	µA
I_{OL}	Low-level output current				1.5	mA

† DV_{DD} must be > C1A5V − 3.3 V during power up.
‡ C1A5V must be > DV_{DD} − 0.5 V during power up.

electrical characteristics over recommended operating case temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		DV_{DD} = 3.3 ±0.3 V, I_{OH} = Max	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.4	V
I_{IZ}	Input current for outputs in high impedance	D0−D15, HD0−HD7	Bus holders enabled, DV_{DD} = MAX, V_I = V_{SS} to DV_{DD}	−50		50	µA
		All other inputs	CV_{DD} = MAX, V_I = V_{SS} to DV_{DD}	−5		5	
I_I	Input current	X2/CLKIN	V_I = V_{SS} to DV_{DD}	−40		40	µA
		$\overline{TRST}$		−5		300	
		HPIENA		−5		300	
		TMS, TCK, TDI, HPI†		−300		5	
		All other input-only pins		−5		5	
I_{cc}	Supply current, 3.3 V		DV_{DD} = 3.3 V, 59 MIPS, T_C = 25°C		2.5		mA
I_{core}	Supply current, 1.5 V		DV_{DD} = 1.5 V, 59 MIPS, T_C = 25°C		28		mA
I	Supply current, standby		IDLE3 (AT%Z)		3.5		mA
I_{C1}	Supply current, C1A5V		internal DAA active		0.5		mA
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

† HPI input signals except for HPIENA

switching characteristics

In the following sections, many timing parameters are defined in terms of the parameter H which is 0.5 $t_{c(CO)}$. For 58 MIPS operation, H=33.9 ns and for 117 MIPS operation, H=16.9 ns. See Clocking Considerations and Mode Selection sections for additional information on clock options.

The HPI interface, reset, and interrupt can be completely asynchronous to CLKOUT.

reset and interrupt timings over recommended operating conditions (see Figure 26 and Figure 27)†

PARAMETER		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, $\overline{RS}$ after CLKOUT low	0		ns
$t_{h(INT)}$	Hold time, $\overline{INTn}$ after CLKOUT low‡	0		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low§	4H+5		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{INTn}$ high (synchronous)	2H+7		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{INTn}$ high (asynchronous)	4H		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{INTn}$ low (synchronous)	2H+7		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{INTn}$ low (asynchronous)	4H		ns
$t_{su(INT)}$	Setup time, $\overline{INTn}$, $\overline{RS}$ before CLKOUT low	8	10	ns

† Note that reset ($\overline{RS}$) may cause a change in clock frequency, therefore changing the value of H.
‡ The external interrupt $\overline{INTn}$ is synchronized to the core CPU by way of a two-flip-flop synchronizer which samples the input with consecutive falling edges of CLKOUT. The input to the interrupt pin is required to represent a 1-0-0 sequence at the timing that is corresponding to three CLKOUT sampling sequences.
§ If the PLL mode is selected, then at power-on sequence, $\overline{RS}$ must be held low for at least 50 ms to ensure synchronization and lock-in of the PLL.

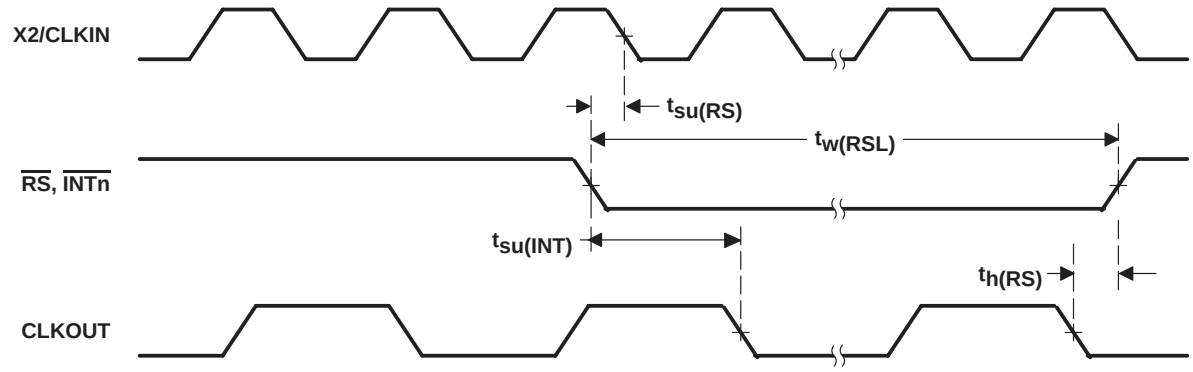


Figure 26. Reset and Interrupt Timing

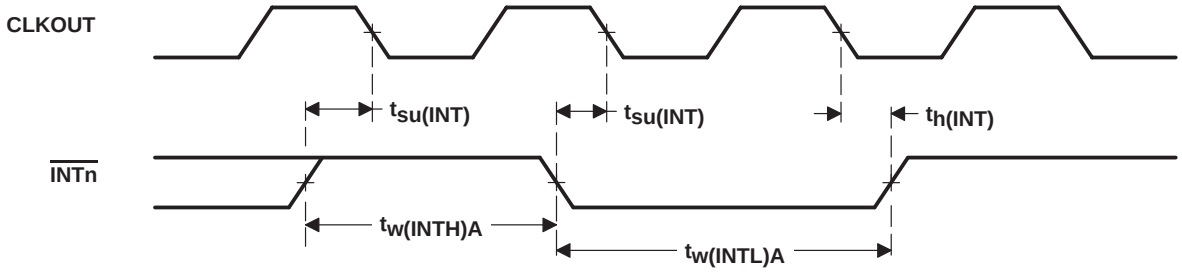


Figure 27. Interrupt Timing

HPI timing

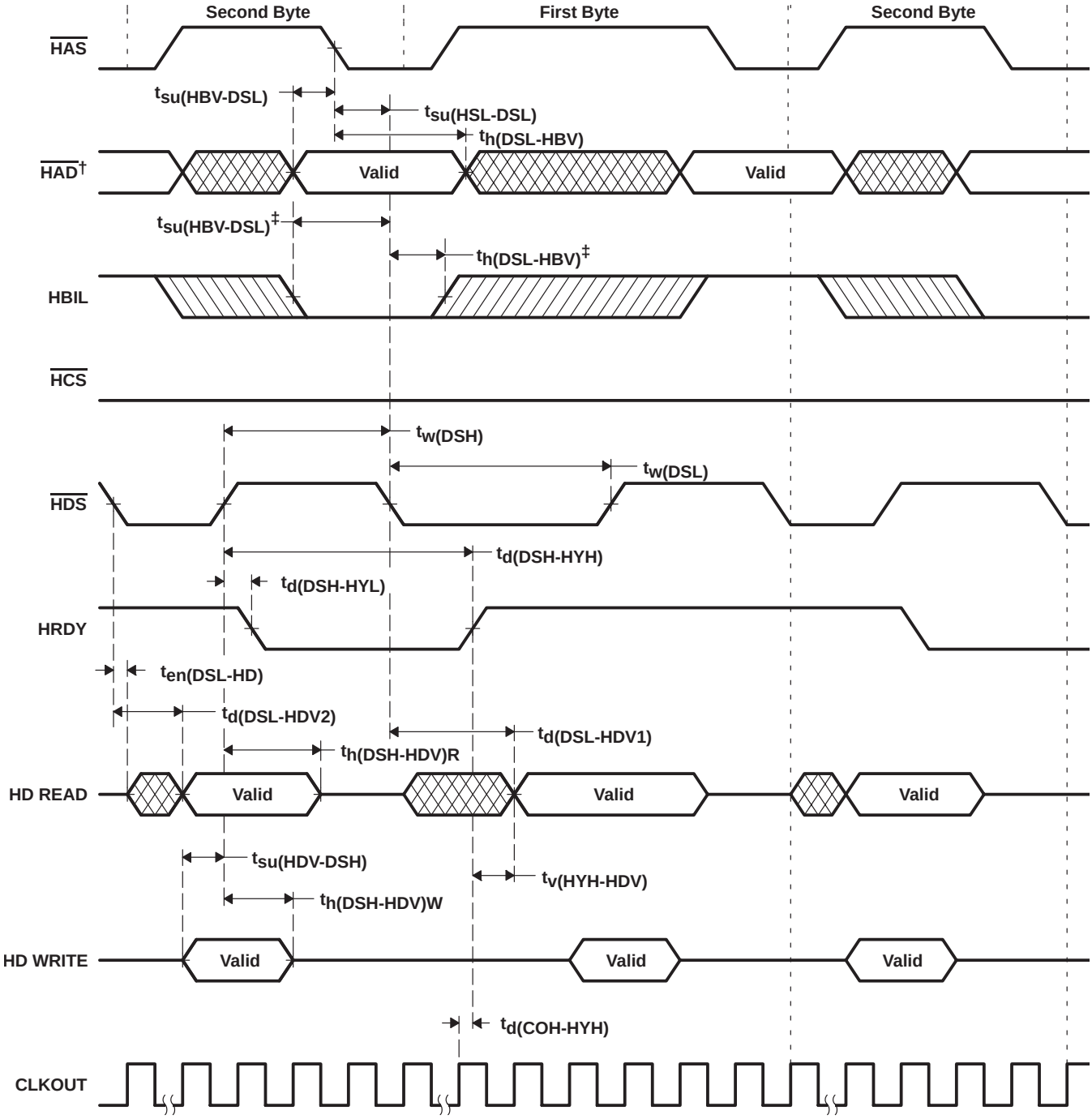
HPI switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 28 through Figure 30 and Notes A, B, and C)

PARAMETER			MIN	MAX	UNIT
$t_{en(DSL-HD)}$	Enable time, HD driven from DS low		2	15	ns
$t_{d(DSL-HDV1)}$	Delay time, DS low to HDx valid for first byte of an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)}$ < 18H		18H+15−$t_{w(DSH)}$	ns
		Case 1b: Memory accesses when DMAC is active in 16-bit mode and $t_{w(DSH)}$ ≥ 18H		15	
		Case 2a: Memory accesses when DMAC is inactive and $t_{w(DSH)}$ < 10H		10H+15−$t_{w(DSH)}$	
		Case 2b: Memory accesses when DMAC is inactive and $t_{w(DSH)}$ ≥ 10H		15	
		Case 3: Register accesses		15	
$t_{d(DSL-HDV2)}$	Delay time, DS low to HDx valid for second byte of an HPI read			15	ns
$t_{h(DSH-HDV)R}$	Hold time, HDx valid after DS high, for a HPI read		3	5	ns
$t_{v(HYH-HDV)}$	Valid time, HDx valid after HRDY high			4	ns
$t_{d(DSH-HYL)}$	Delay time, DS high to HRDY low†			9	ns
$t_{d(DSH-HYH)}$	Delay time, DS high to HRDY high	Case 1: Memory accesses when DMAC is active		18H+10	ns
		Case 2: Memory accesses when DMAC is inactive		10H+10	
		Case 3: Write accesses to HPIC register‡		6H+10	
$t_{d(HCS-HRDY)}$	Delay time, $\overline{HCS}$ low/high to HRDY low/high			8	ns
$t_{d(COH-HYH)}$	Delay time, CLKOUT high to HRDY high			10	ns
$t_{d(COH-HTX)}$	Delay time, CLKOUT high to HINT change			10	ns
$t_{su(HBV-DSL)}$	Setup time, HBIL valid before DS low		10		ns
$t_{h(DSL-HBV)}$	Hold time, HBIL valid after DS low		5		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before DS low		5		ns
$t_{w(DSL)}$	Pulse duration, DS low		20		ns
$t_{w(DSH)}$	Pulse duration, DS high		10		ns
$t_{su(HDV-DSH)}$	Setup time, HDx valid before DS high, HPI write		5		ns
$t_{h(DSH-HDV)W}$	Hold time, HDx valid after DS high, HPI write		3		ns

† The HRDY output is always high when the $\overline{HCS}$ input is high, regardless of DS timings.
‡ This timing applies when writing a one to the DSPINT bit or HINT bit of the HPIC register. All other writes to the HPIC occur asynchronously, and do not cause HRDY to be deasserted.

NOTES: A. DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$ and $\overline{HDS2}$.
B. HDx refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.)
C. DMAC stands for direct memory access (DMA) controller. The HPI shares the internal DMA bus with the DMAC, thus HPI access times are affected by DMAC activity.

HPI timing (continued)



† HAD refers to HCNTL0, HCNTL1, and HR/W
‡ When HAS not used (HAS always high.)

Figure 28. Using HDS to Control Accesses (HCS Always Low)

HPI timing (continued)

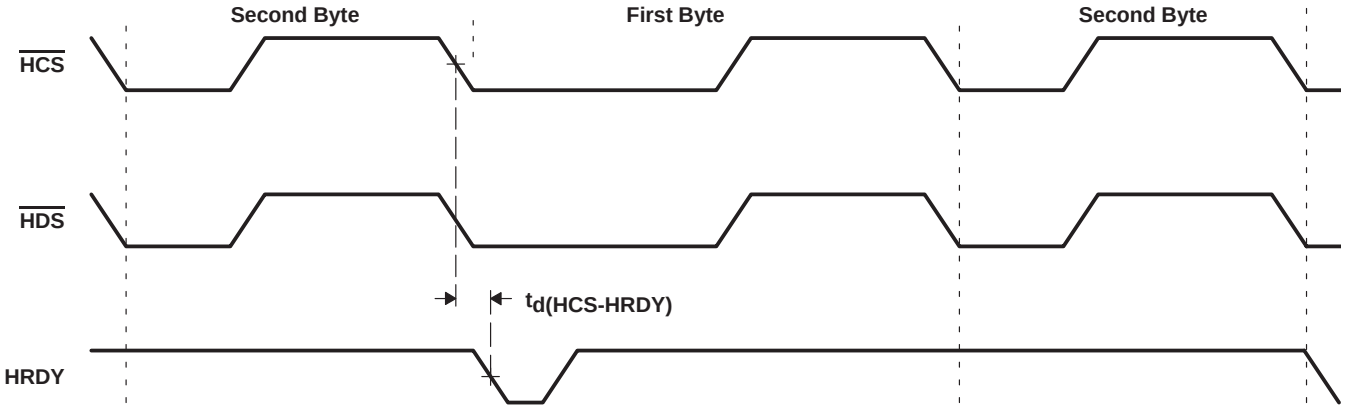


Figure 29. Using $\overline{\text{HCS}}$ to Control Accesses

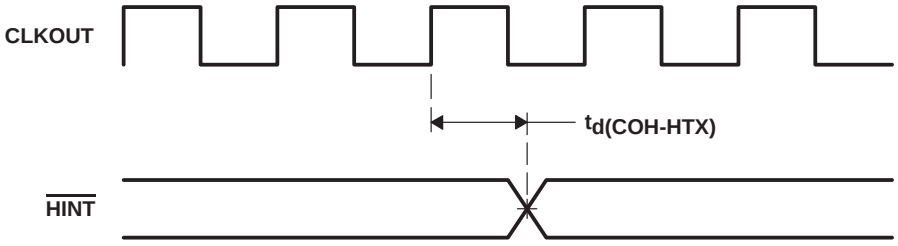
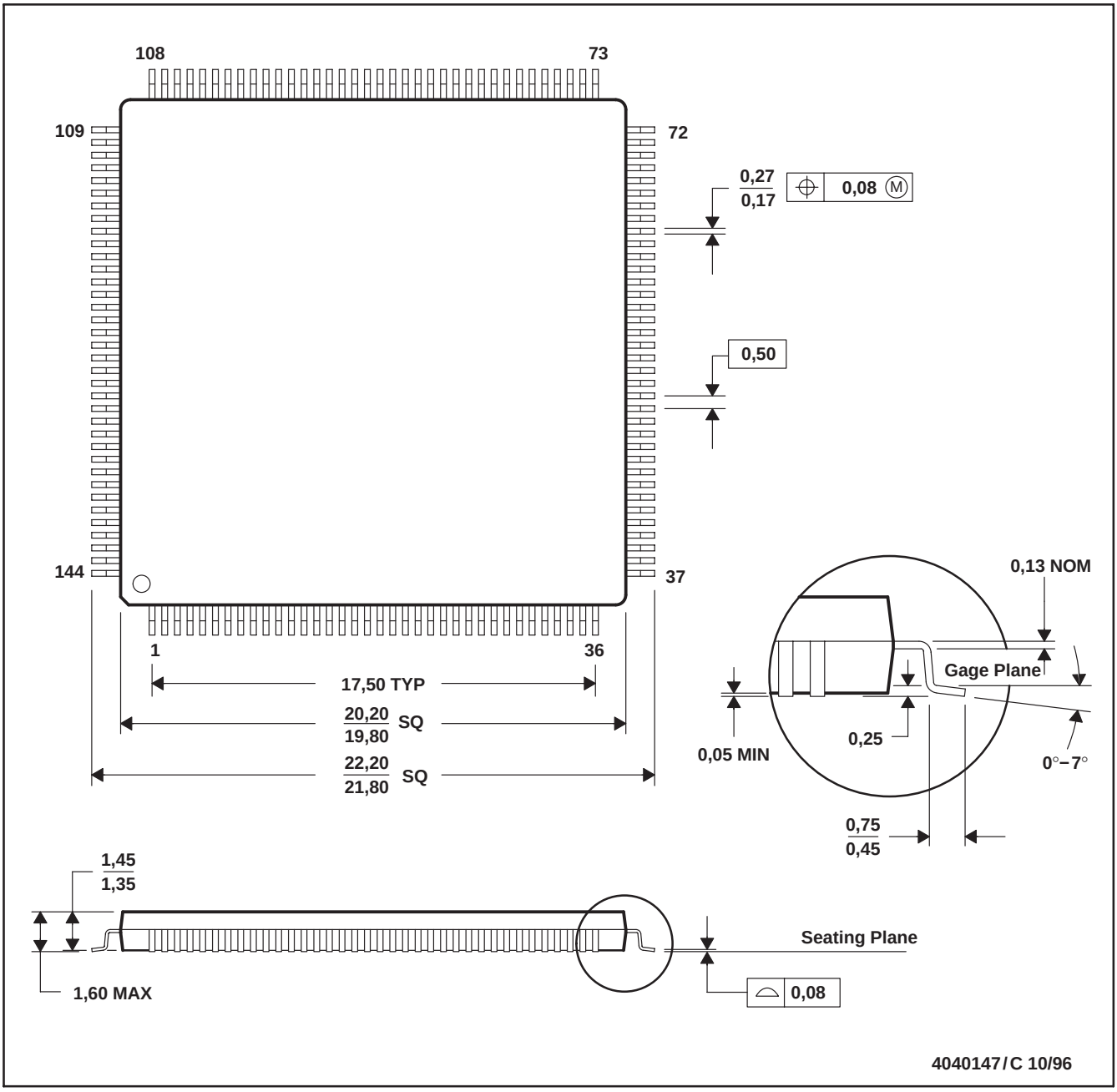


Figure 30. $\overline{\text{HINT}}$ Timing

MECHANICAL DATA

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



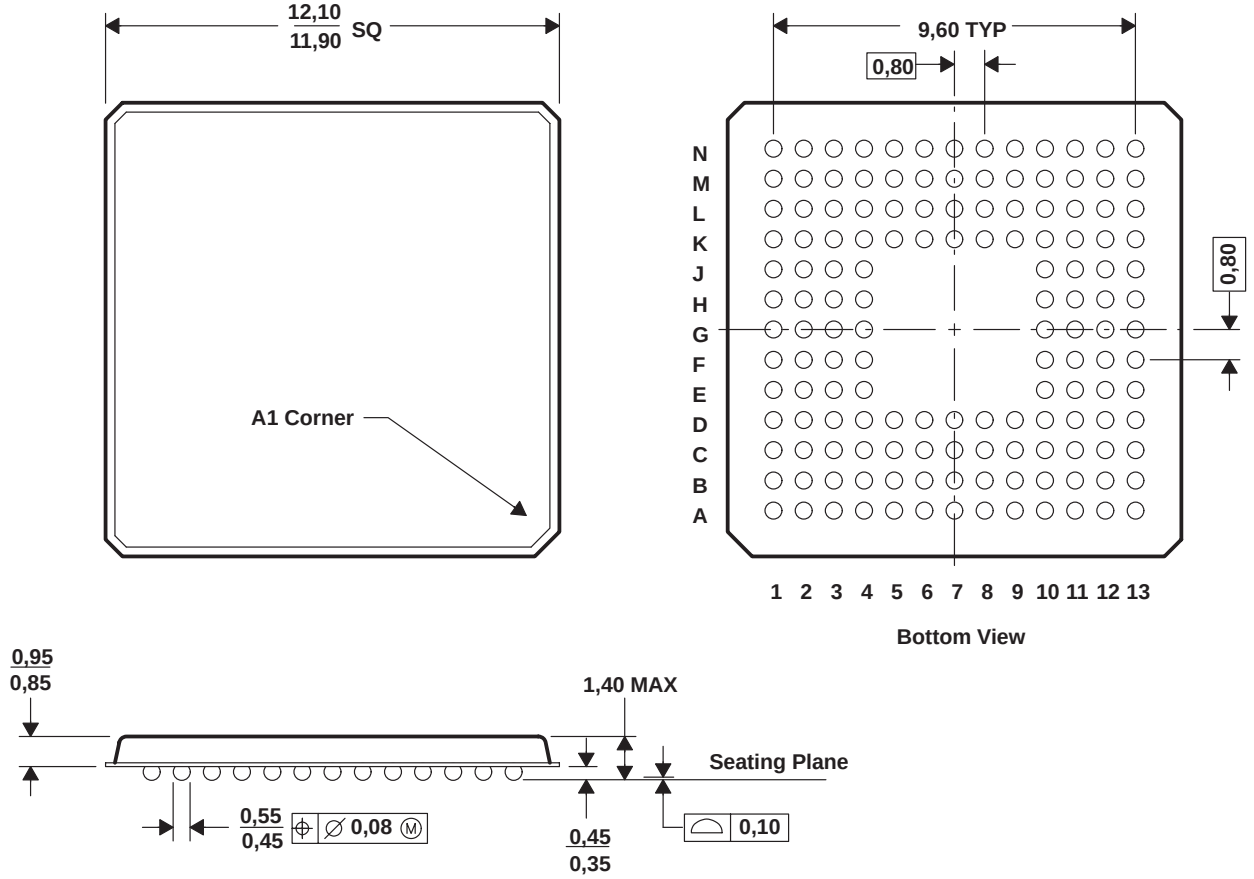
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	56
$R_{\Theta JC}$	5

MECHANICAL DATA

GGU (S-PBGA-N144) **PLASTIC BALL GRID ARRAY PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA™ configuration

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	38
$R_{\Theta JC}$	5

MicroStar BGA is a trademark of Texas Instruments.

MECHANICAL DATA

Si3016 **16-PIN SMALL OUTLINE PLASTIC PACKAGE (SOIC)**

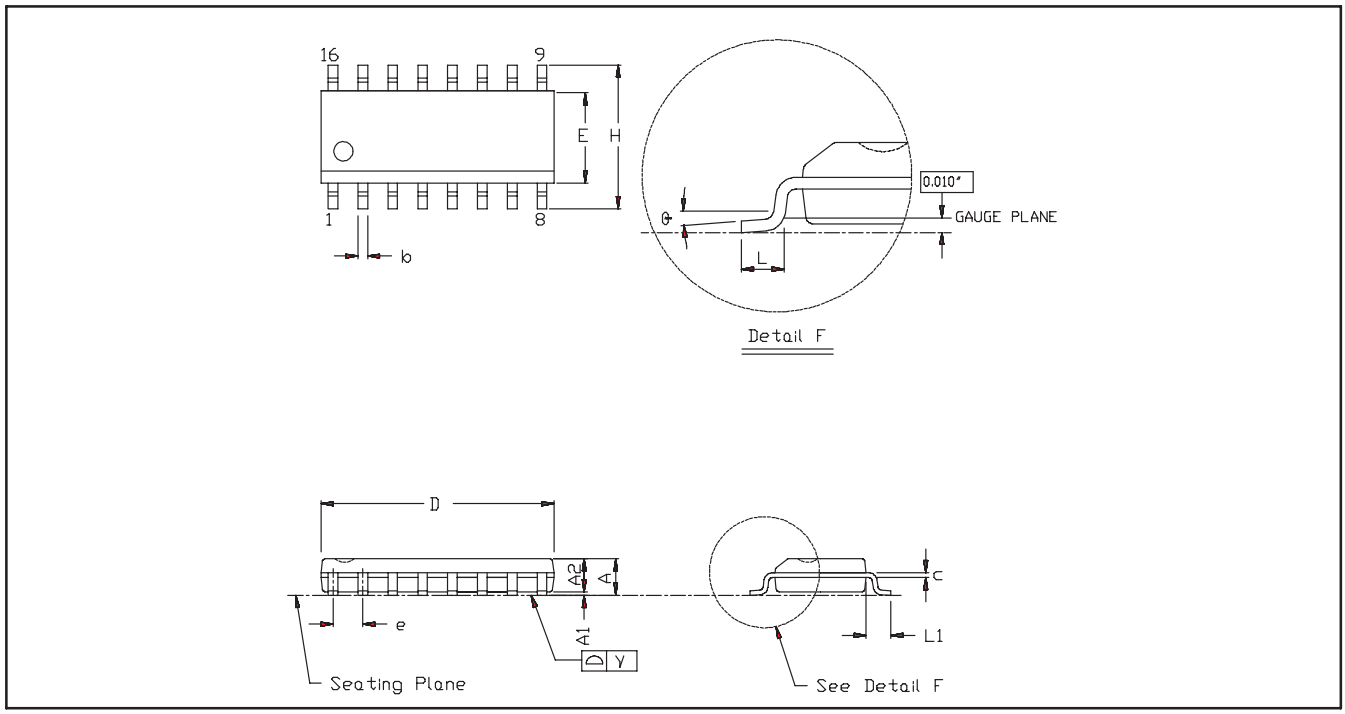


Table 32. Package Diagram Dimensions

CONTROLLING DIMENSION: MM				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.051	0.059	1.30	1.50
b	0.013	0.020	0.330	0.51
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC	—	1.27 BSC	—
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
L1	0.042 BSC	—	1.07 BSC	—
γ	—	0.004	—	0.10
θ	0°	8°	0°	8°

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320C54V90BPGE	Obsolete	Production	LQFP (PGE) | 144	-	-	Call TI	Call TI	-	320C54V90B PGE TMS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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