WINSOURCE ELECTRONICS

THE DATASHEET OF

TS8729N

TS8729N - 550W 20% Duty Cycle 2.0ms Pulse Width Peak GaN RF Switch

1.0 Features

- Low TX insertion loss: 0.19dB @ 800MHz
- High isolation: 40dB @ 800MHz
- 550W 20% Duty Cycle 2.0ms Pulse Width
- Versatile 2.6-5.5V power supply
- Operating frequency: 500MHz to 2.0GHz

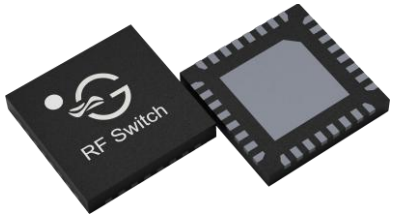


Figure 1 Device Image
(32 Pin 5×5×1.25mm QFN Package)

2.0 Applications

- L-Band Radar
- High Power Tx/Rx transceivers / tactical radios

RoHS10/REACH/Halogen Free Compliance

3.0 Description

The TS8729N is an asymmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. The TS8729N can cover 500MHz to 2.0GHz bandwidth and provide low insertion loss, high isolation and high linearity within a small package size.

The TS8729N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

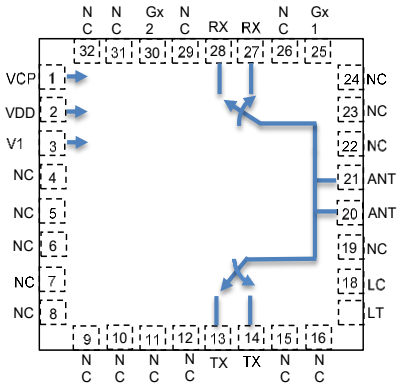


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS8729N	32 Pin 5×5×1.25mm QFN	Tape and Reel	1000	13" (330mm)	18mm	TS8729NMTRPBF
Evaluation Board						TS8729N-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 100nF capacitor to GND on this pin.
2	VDD	DC power supply
3	V1	Switch control input 1
4,5,6,7,8,9,10,11,16,23,24,31,32	NC	No internal connection, can be grounded
12,15,19,22,25,30,26,29	NC	No internal connection. Must be left Open
13,14	TX	TX Port
17,18	LT, LC	Tuning Inductor
20,21	ANT	Antenna Port
27,28	RX	RX Port

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, Tcase=+85°C, 915MHz	TX, ANT	200	W
RF Input Power Peak, Tcase=+85°C, 915MHz, 1% duty cycle, 10usec pulse width	TX, ANT	600	W
RF Input Power CW, Tcase=+85°C, 915MHz	RX, ANT	10	W
RF Input Power Peak, Tcase=+85°C, 915MHz, 1% duty cycle, 10usec pulse width	RX, ANT	15	W
RF Input Power Peak, Tcase=+85°C, 915MHz, 20% duty cycle, 2ms pulse width	RX, ANT	12	W
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	3.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		500		2000	MHz
Insertion loss, TX	915MHz		0.25		dB
	1300MHz (matched)		0.22		
Insertion loss, RX	915MHz		0.8		dB
	1300MHz (matched)		0.65		
Isolation ANT-TX	915MHz		15		dB
	1300MHz (matched)		39		
Isolation ANT-RX	915MHz		52		dB
	1300MHz (matched)		47		
Return Loss RX	915MHz		19		dB
	1300MHz (matched)		20		
Return Loss TX	915MHz		17		dB
	1300MHz (matched)		32		
P0.1dB CW, TX	0.1dB compression point, 915MHz		>300		W
P0.1dB Peak, TX	Duty Cycle 20% with 2.0msec pulse width, 915MHz		>550		W
P0.1dB CW, Rx	0.1dB compression point, 915MHz		5		W
P0.1dB Peak, Rx	1% DC, 10 us Pulse Width, 915MHz		10		W
P0.1dB Peak, Rx	20% DC, 2 ms Pulse Width, 915MHz		8		W
Switching time (RX/TX)	50% ctrl to 90% of RF value.		1.1 / 1.4		µs
	50% ctrl to 10% of RF value.		0.4 / 1.6		µs
Rise and Fall time (RX/TX)	10% to 90% of RF value.		0.74 / 0.25		µs
	90% to 10% of RF value.		0.38 / 1.51		µs
Control voltage	Power Supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins low, I_{il}		0		µA
	All control pins high, I_{ih}			7.5	µA
Current consumption, IDD	Active mode (VDD on)		160	200	µA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	Active RF Path
0	ANT-RX
1	ANT-TX

Attention:
[1] VDD should be applied first before V1, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V1 control pin, the state at start-up without any control voltage applied will be ANT-RX.

9.0 Evaluation Board

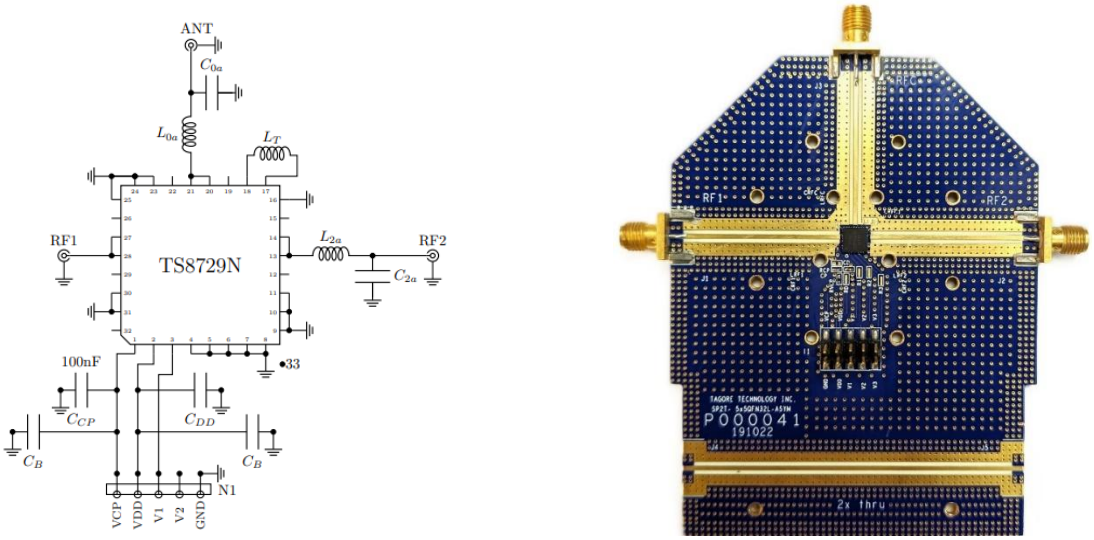


Figure 3 Evaluation Board and Schematic

Attention:
[1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be added.
[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

10.0 Typical Characteristics – Unmatched (<500 MHz)

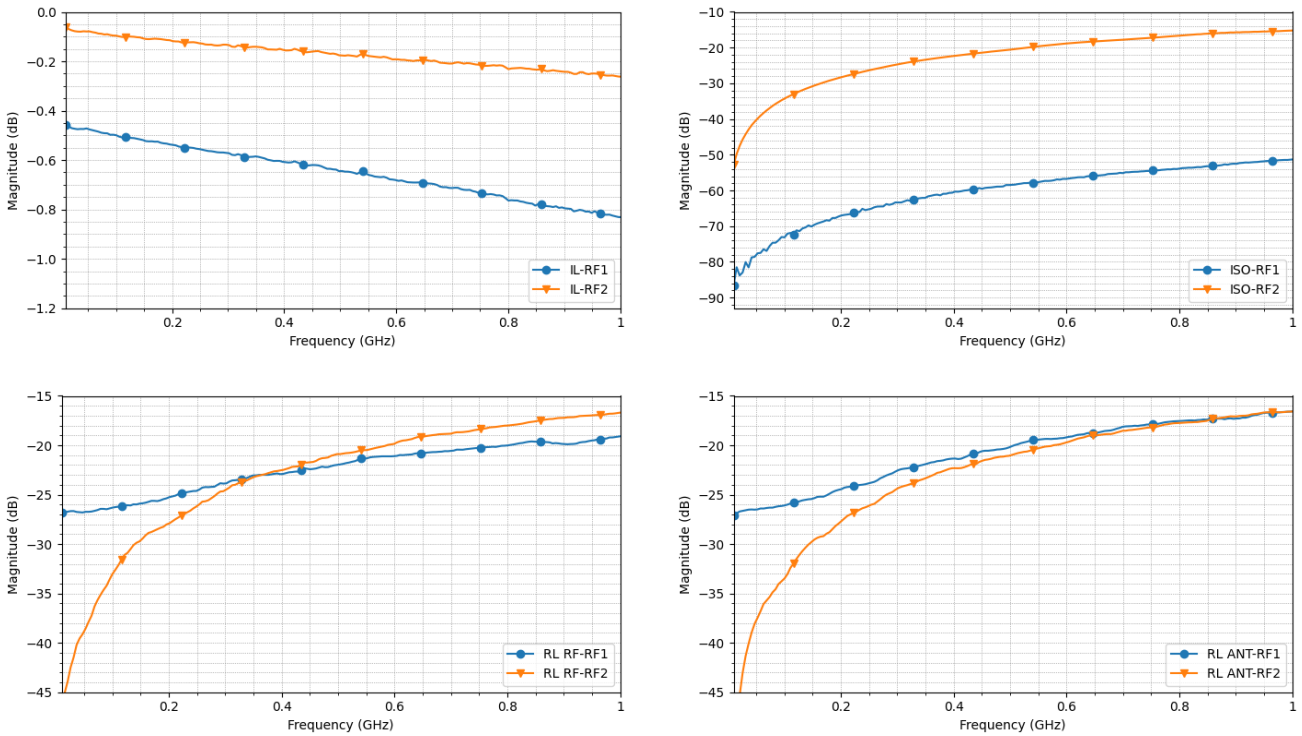


Figure 4 Typical characteristics

10.1 Typical Characteristics – Matched (1000 MHz – 1600 MHz)

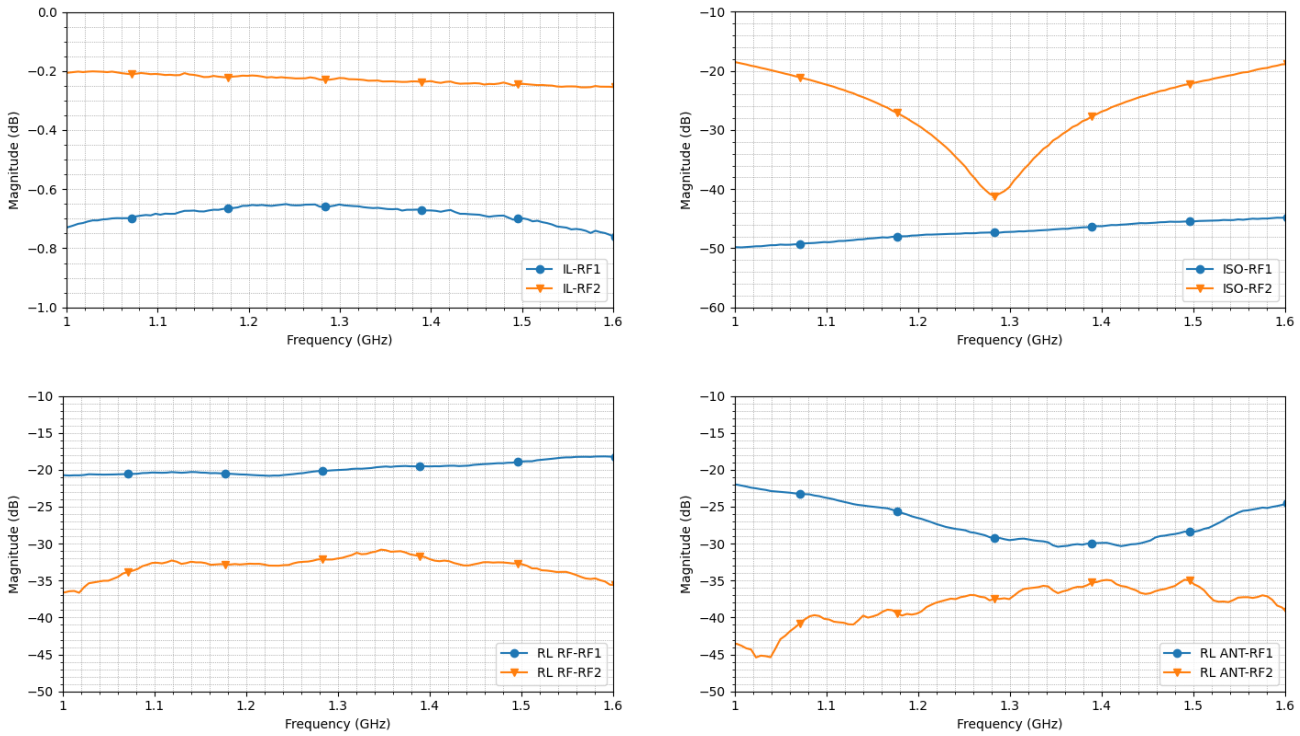


Figure 5 Typical characteristics (1000 MHz – 1600 MHz)

11.0 Typical Characteristics – Switching Time



Figure 6 Switching Time

Table 6 Bill of Materials – Matching* (<500 MHz)

Component	Part Number	Description	Notes
C_{CP}	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_{DD}	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
C_B	UQCL2A270GAT2A	Ceramic capacitor, 27 pF, 200 V, ±2%.	Optional
L_T			DNP
L_{0a}			DNP
C_{0a}			DNP
L_{2a}			DNP
C_{2a}			DNP

Table 7 Bill of Materials – Matching* (1000 MHz – 1600 MHz)

Component	Part Number	Description	Notes
C_{CP}	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_{DD}	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
C_B	UQCL2A270GAT2A	Ceramic capacitor, 27 pF, 200 V, ±2%.	Optional
L_T	0402DC-22NX_R_	Ceramic core chip inductor, 22 nH, ± 5%.	
L_{0a}	0603DC-5N6X_RW	Ceramic core chip inductor, 5.6 nH, ± 5%.	Two in parallel.
C_{0a}	0603N0R3BW251	Ceramic capacitor, 0.3 pF, 250V, ± 0.1pF.	
L_{2a}	0603DC-5N6X_RW	Ceramic core chip inductor, 5.6 nH, ± 5%.	Two in parallel.
C_{2a}	0603N0R3BW251	Ceramic capacitor, 0.3 pF, 250V, ± 0.1pF.	

* For additional details, please contact the Tagore Technology support team.

12.0 Device Package Information

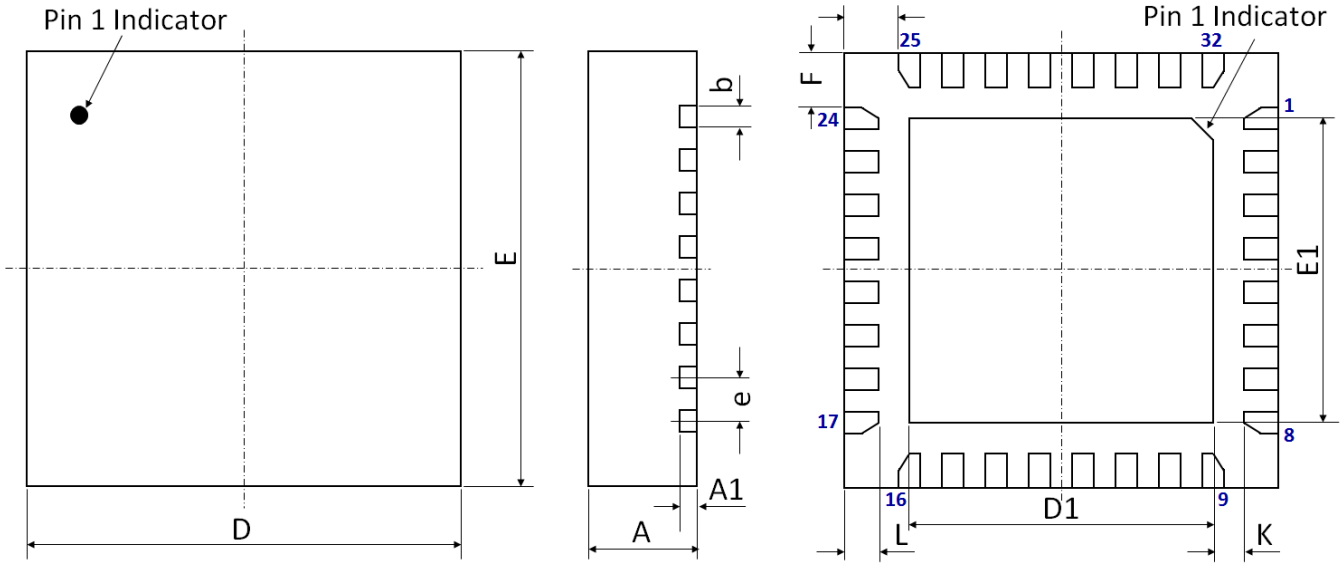


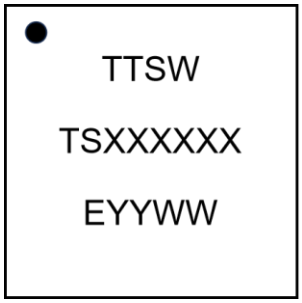
Figure 12 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	1.25	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)
Attention: Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

13.0 PCB Land Design

Guidelines:

[1] 4 layer PCB is recommended.

[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.

[3] Thermal vias shall only be placed on the center pad.

[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

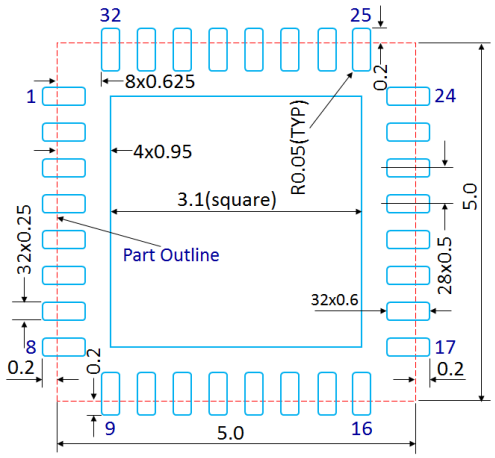


Figure 13 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 14 Solder Mask Pattern
(Dimensions are in mm)

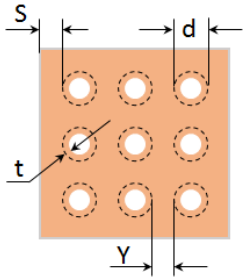


Figure 15 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

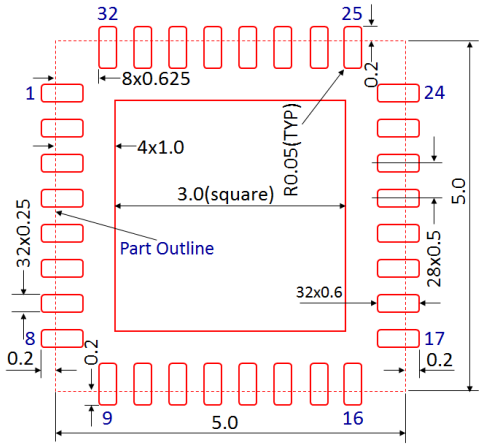


Figure 16 Stencil Openings
(Dimensions are in mm)

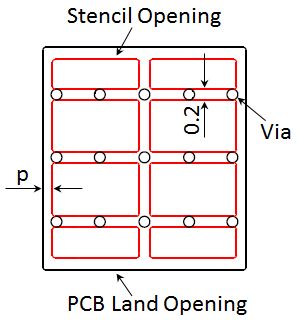


Figure 17 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

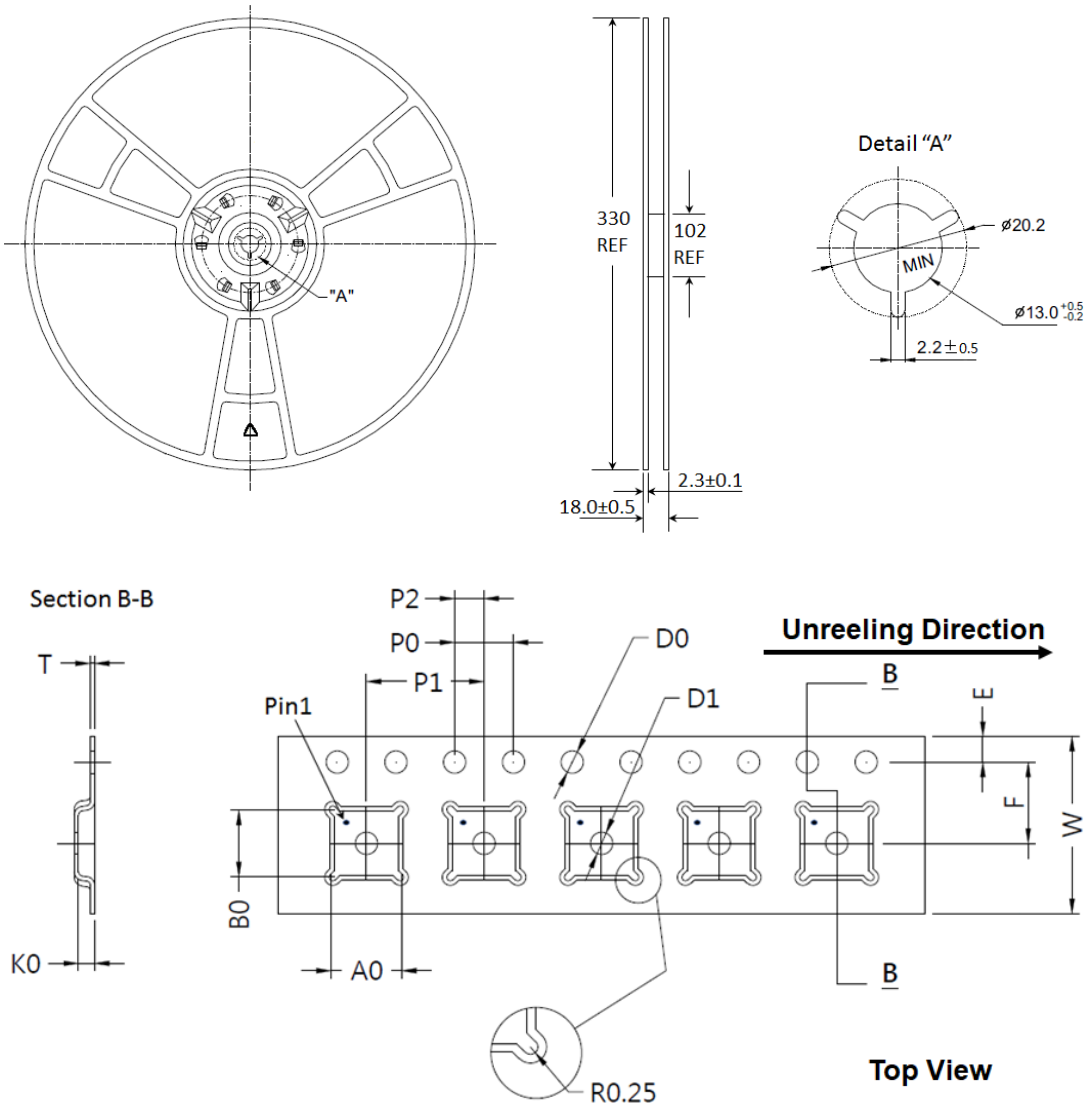


Figure 18 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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