WINSOURCE ELECTRONICS

THE DATASHEET OF

TS7421L

TS7421L - 30W CW GaN Broadband RF Switch SPDT

1.0 Features

- Low insertion loss: 0.30dB @ 800MHz
- High isolation: 44dB @ 800MHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.5V power supply

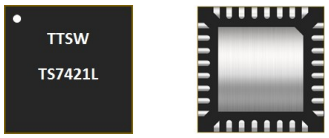


Figure 1 Device Image
(32 Pin 4×4×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS7421L is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500MHz to 5GHz makes the TS7421L an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7421L is packaged into a compact Quad Flat No lead (QFN) 4x4mm 32 leads plastic package.

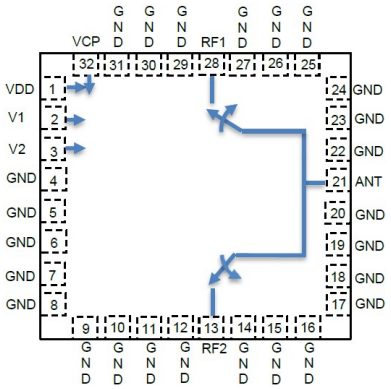


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS7421L	32 Pin 4×4×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS7421LMTRPBF
Evaluation Board						TS7421L-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VDD	DC power supply
2	V1	Switch control input 1
3	V2	Switch control input 2
4,5,6,7,8,9,10,11,12,14,15,16,17, 18,19,20,22,23,24,25,26,27,29,30,31	NC	No internal connection, Can be grounded
13	RF2	RF port 2
21	ANT	Antenna port
28	RF1	RF port 1
32	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management. Adequate heatsinking required

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 500-3000MHz, T_C=+85°C	RFx	45	dBm
RF Input Power CW, 500-3000MHz, (VSWR 10:1), 1 minute	RFx	44	dBm
RF Input Power CW, >3GHz – 5GHz, T_C=+85°C	RFx	42.5	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	10	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 37	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		500		5000	MHz
Insertion Loss, RFx	500MHz		0.30		dB
	800MHz		0.30	0.4	
	1.95GHz		0.35	0.5	
	2.6GHz		0.40	0.55	
	5.0GHz		0.75		
Isolation, ANT-RFx	500MHz		48		dB
	800MHz	40	44		
	1.95GHz	32	35		
	2.6GHz	28	32		
	5.0GHz		22		
Return Loss, ANT-RFx	500MHz		35		dB
	800MHz		35		
	1.95GHz		30		
	2.6GHz		27		
	5.0GHz		17		
H2	800MHz, Pin=38dBm		-83		dBc
H3	800MHz, Pin=38dBm		-80		dBc
IIP3	800MHz		74		dBm
P0.1dB[1]	0.1dB compression point, 500MHz - 4GHz		46		dBm
P0.1dB[1]	0.1dB compression point, >4GHz		45		dBm
Switching Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		0.8		μs
Control Voltage	Power supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		160	200	μA

Note: [1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

[3] Insertion loss goes up by 0.1dB at 85degC base plate temp.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1
1	0	ANT-RF2

Attention: [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V2 control pin, which can be left floating when the all OFF state is used.
[3] If all OFF state is not used, the switch can be operated with single control pin V1.
[4] There is also an internal pull-down to ground on V1 control pin, the state at start-up without any control voltage applied will be ANT-RF1 on by default.

9.0 Evaluation Board Schematic

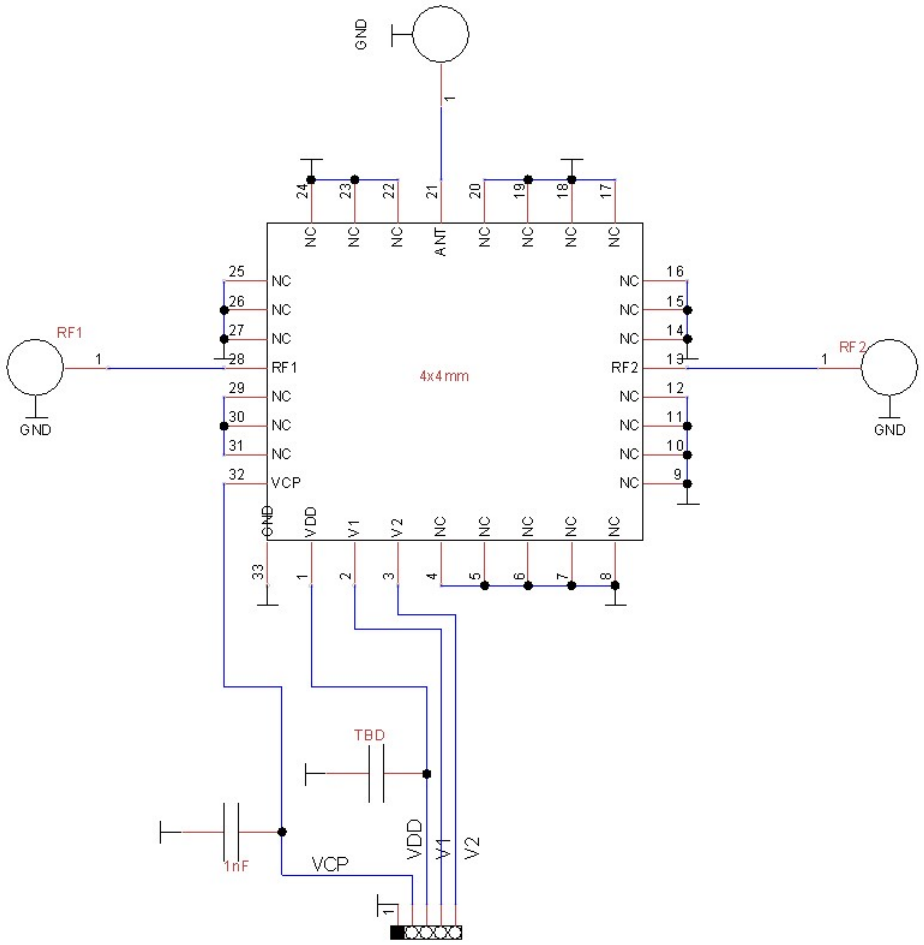


Figure 3 Evaluation Board Schematic

10.0 Typical Characteristics

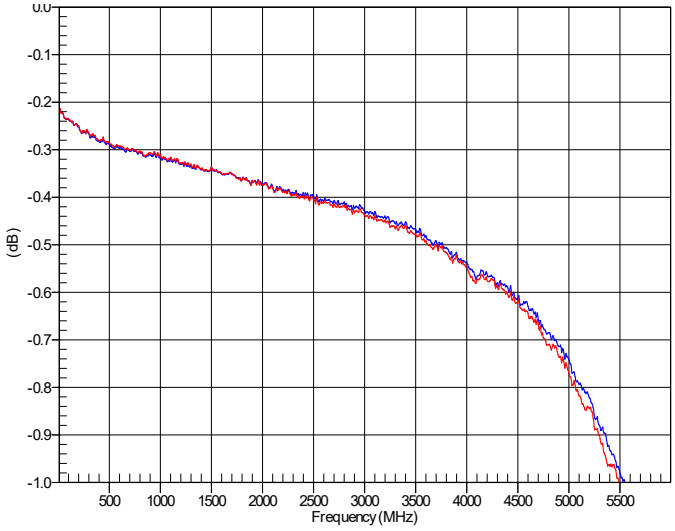


Figure 4 RF1, RF2 Insertion Loss

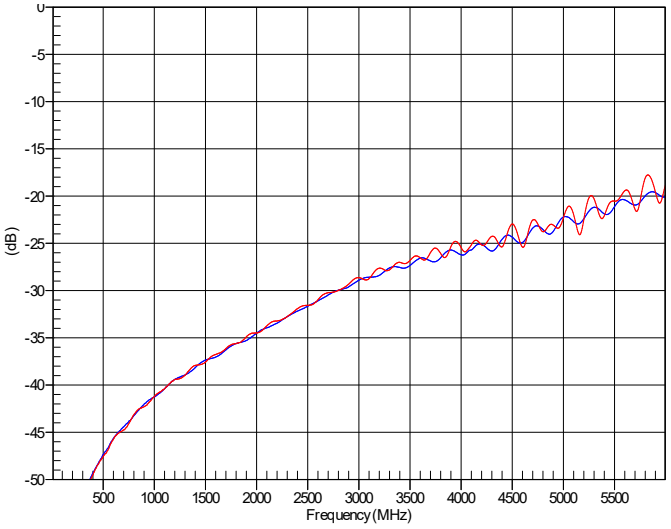


Figure 5 RF1, RF2 Isolation

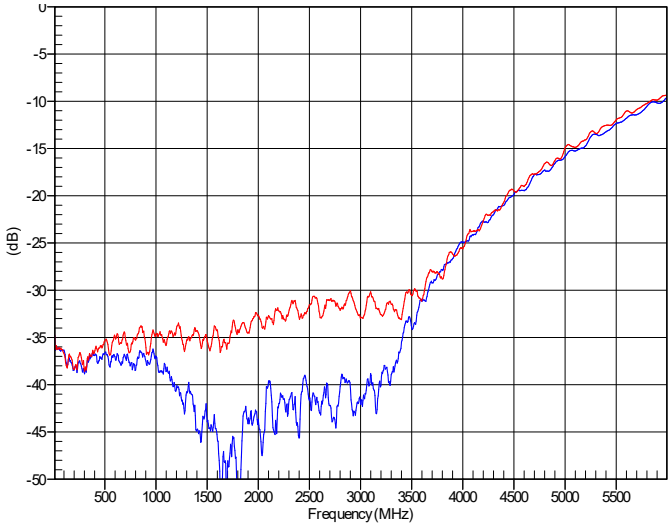


Figure 6 RF1, RF2 Return Loss

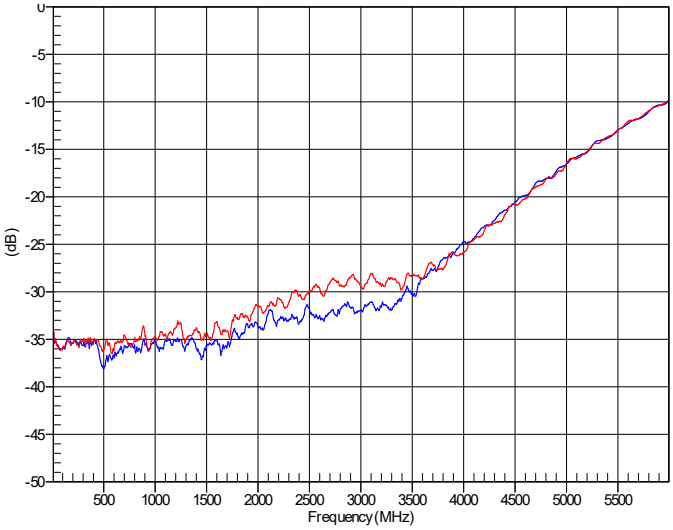


Figure 7 ANT Return Loss

11.0 Device Package Information

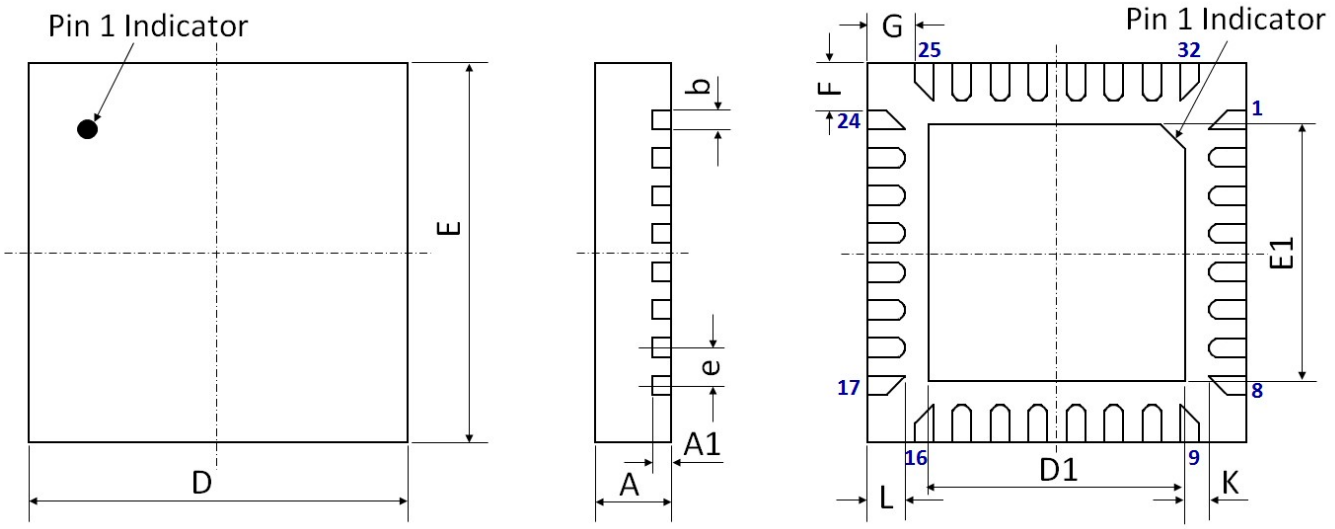


Figure 8 Device Package Drawing
(All dimensions are in mm)

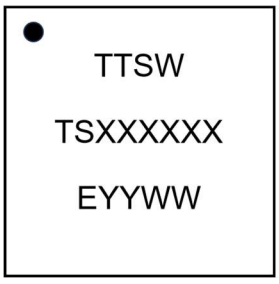
Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering-related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

12.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 4(X)×4(Y)=16.

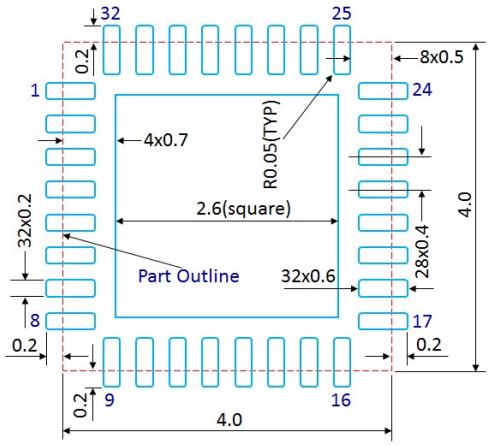


Figure 9 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 10 Solder Mask Pattern
(Dimensions are in mm)

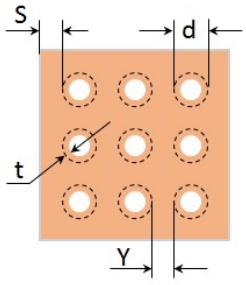


Figure 11 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

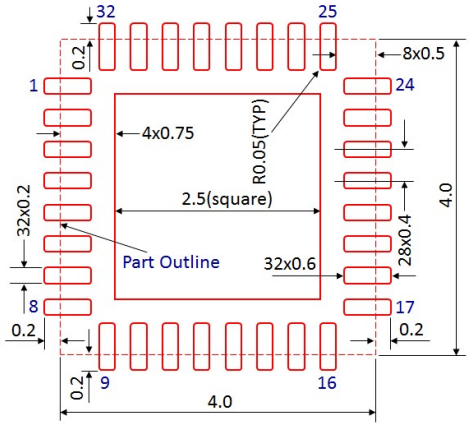


Figure 12 Stencil Openings
(Dimensions are in mm)

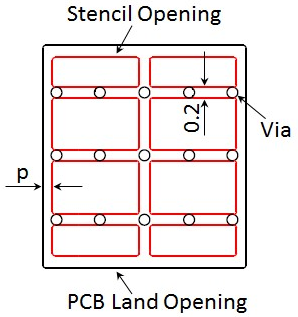


Figure 13 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

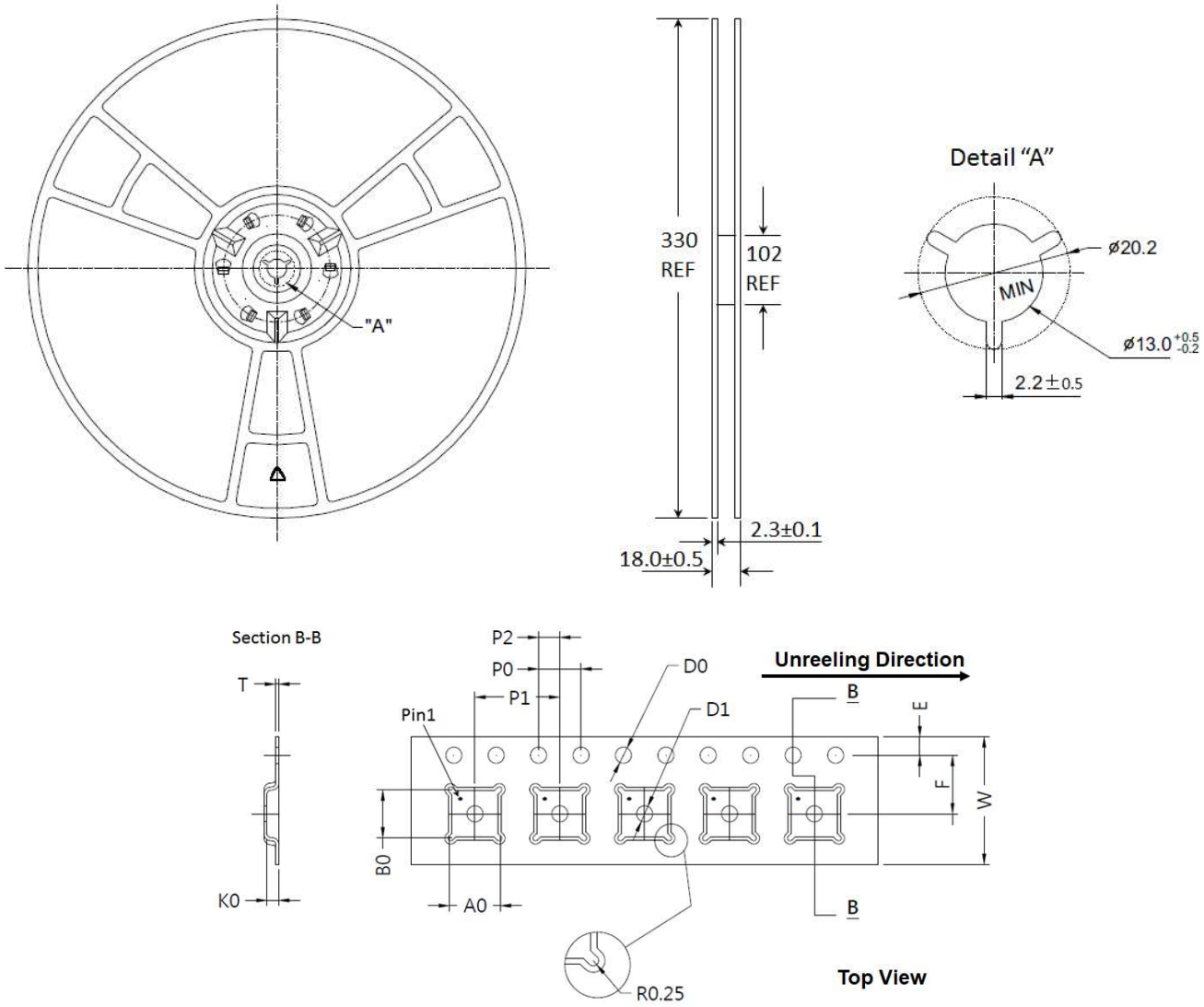


Figure 14 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	4.35	±0.10	K0	1.10	±0.10
B0	4.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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