WINSOURCE ELECTRONICS

# THE DATASHEET OF

TS7226K

# TS7226K - 10W CW, 50W Peak Power GaN Broadband RF Switch SPDT

## 1.0 Features

- Low insertion loss: 0.5dB @ 2.6GHz
- High isolation: 35dB @ 2.6GHz
- High peak power handling capability
- No external DC blocking capacitors on RF lines
- 40dBm CW hot switching capability
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 500MHz to 7GHz

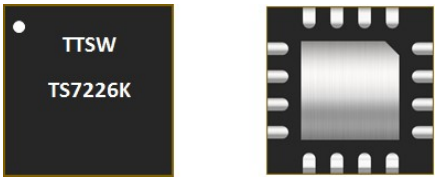



**Figure 1 Device Image**
(16 Pin 3×3×0.8mm QFN Package)

## 2.0 Applications

- Mobile radio handsets
- Massive MIMO
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

**RoHS/REACH/Halogen Free Compliance**

## 3.0 Description

The TS7226K is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500MHz to 7GHz frequencies makes the TS7226K an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7226K is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

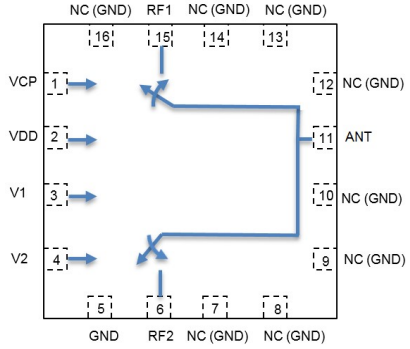



**Figure 2 Function Block Diagram**
(Top View)

## 4.0 Ordering Information

**Table 1 Ordering Information**

| Base Part Number | Package Type | Form | Qty | Reel Diameter | Reel Width | Orderable Part Number |
|---|---|---|---|---|---|---|
| TS7226K | 16 Pin 3×3×0.8mm QFN | Tape and Reel | 3000 | 13” (330mm) | 18mm | TS7226KMTRPBF |
| Evaluation Board | | | | | | TS7226K-EVB |

## 5.0 Pin Description

**Table 2 Pin Definition**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | VCP | Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time. |
| 2 | VDD | DC power supply |
| 3 | V1 | Switch control input 1 |
| 4 | V2 | Switch control input 2 |
| 6 | RF2 | RF port 2 |
| 5,7,8,9,10,12,13,14,16 | NC | No internal connection, can be grounded |
| 11 | ANT | Antenna port |
| 15 | RF1 | RF port 1 |

**Note:** The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

## 6.0 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings** @$T_A$=+25°C Unless Otherwise Specified

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| **Electrical Ratings** | | | |
| Power Supply Voltage | VDD | 2.6 to 5.5 | V |
| Storage Temperature Range | $T_{st}$ | -55 to +125 | °C |
| Operating Temperature Range | $T_{op}$ | -40 to +85 | °C |
| Maximum Junction Temperature | $T_J$ | +140 | °C |
| RF Input Power CW, 2600MHz, $T_J$=+85°C | RFx | 41.5 | dBm |
| **Thermal Ratings** | | | |
| Thermal Resistance (junction-to-case) – Bottom side | $R_{\theta JC}$ | 25 | °C/W |
| Thermal Resistance (junction-to-top) | $R_{\theta JT}$ | ≤ 39 | °C/W |
| Soldering Temperature | $T_{SOLD}$ | 260 | °C |
| **ESD Ratings** | | | |
| Human Body Model (HBM) | Level 1B | 500 to <1000 | V |
| Charged Device Model (CDM) | Level C3 | ≥1000 | V |
| **Moisture Rating** | | | |
| Moisture Sensitivity Level | MSL | 1 | - |

**Attention:**
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 Electrical Specifications

**Table 4 Electrical Specifications** @$T_A$=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Operating Frequency | | 500 | | 7000 | MHz |
| Insertion Loss, RFx | 800MHz | | 0.40 | 0.50 | dB |
| | 1.95GHz | | 0.45 | 0.55 | |
| | 2.6GHz | | 0.50 | 0.65 | |
| | 3.8GHz | | 0.60 | | |
| | 7.0GHz | | 0.90 | | |
| Isolation ANT-RFx | 800MHz | 45 | 48 | | dB |
| | 1.95GHz | 37 | 40 | | |
| | 2.6GHz | 32 | 35 | | |
| | 3.8GHz | | 30 | | |
| | 7.0GHz | | 20 | | |
| Return Loss ANT-RFx | 800MHz | | 25 | | dB |
| | 1.95GHz | | 23 | | |
| | 2.6GHz | | 18 | | |
| | 3.8GHz | | 15 | | |
| | 7.0GHz | | 13 | | |
| H2 | 800MHz, Pin=38dBm | | -78 | | dBc |
| H3 | 800MHz, Pin=38dBm | | -73 | | dBc |
| IIP3 | 2.6GHz | | 72 | | dBm |
| P0.1dB[1] | 2.6GHz | 40 | 42.5 | | dBm |
| P0.1dB[1] | >5GHz | | 39 | | dBm |
| Peak P0.1dB[2] | 1% duty cycle, 2.6GHz | | 47 | | dBm |
| Switching Time | 50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3) | | 0.50 | | μs |
| Control Voltage | Power supply VDD | 2.6 | 3.3 | 5.5 | V |
| | All control pins high, $V_{ih}$ | 1.0 | 3.3 | 5.25 | V |
| | All control pins low, $V_{il}$ | -0.3 | | 0.5 | V |
| Control Current | All control pins low, $I_{il}$ | | 0 | | μA |
| | All control pins high, $I_{ih}$ | | | 7.5 | μA |
| Current Consumption, IDD | Active mode | | 160 | 200 | μA |

**Note:**

[1] P0.1dB is a figure of merit.

[2] 1% duty cycle and 10μs frame width. Peak P0.1dB.

[3] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

## 8.0 Switch Truth Table

**Table 5 Switch Truth Table**

| V1 | V2 | Active RF Path |
|---|---|---|
| 0 | 1 | All OFF |
| 0 | 0 | ANT-RF1 |
| 1 | 0 | ANT-RF2 |

**Attention:**
[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.
[3] If all OFF state is not used, the switch can be operated with single control pin V1.

## 9.0 Evaluation Board

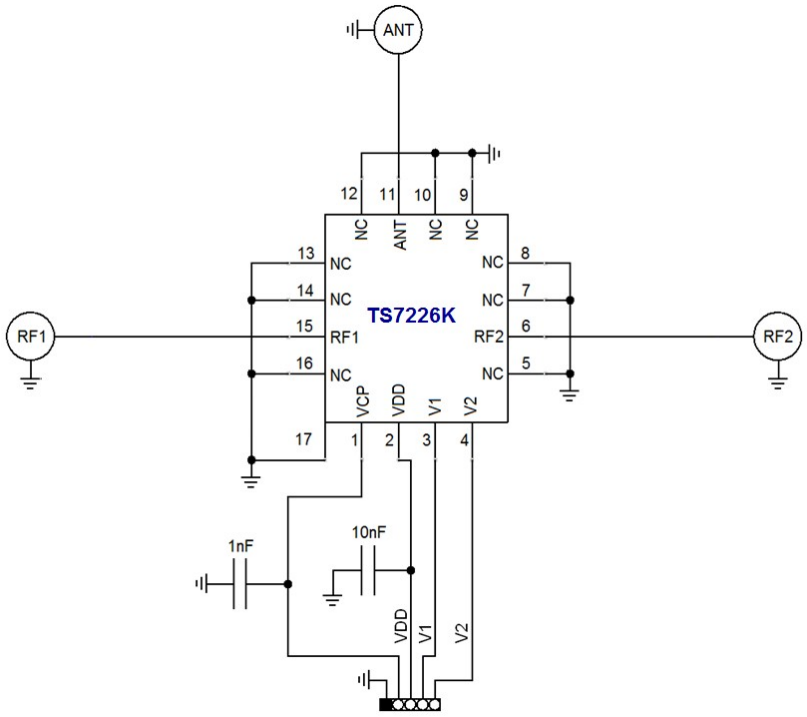



**Figure 3 Evaluation Board Schematic**

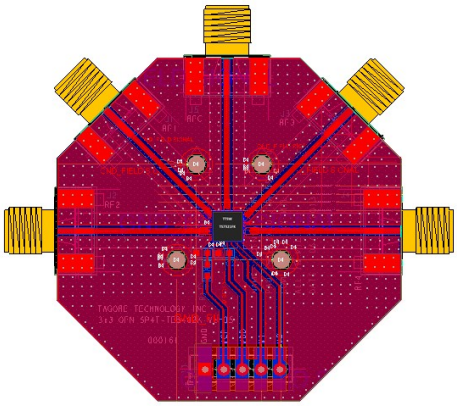


**Figure 4 Evaluation Board Image**

**Attention:**
[1] 17 refers to the center pad of the device.
[2] The purpose of connection between VCP and connector C1 is to monitor VCP, do not apply external voltage to VCP.

## 10.0 Typical Characteristics

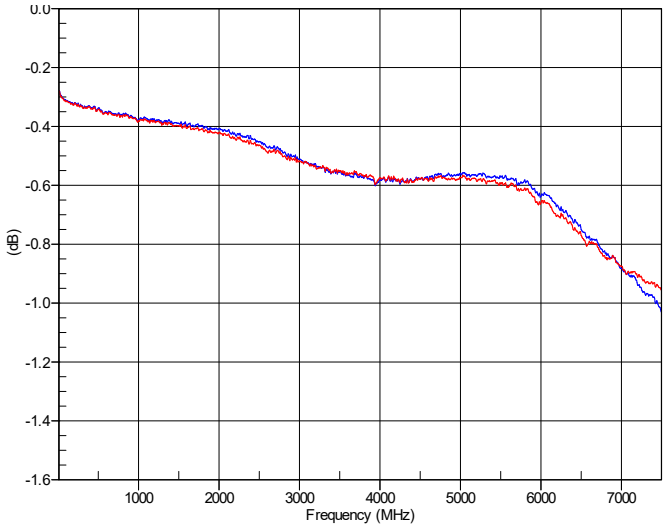



**Figure 5 RF1, RF2 Insertion Loss**

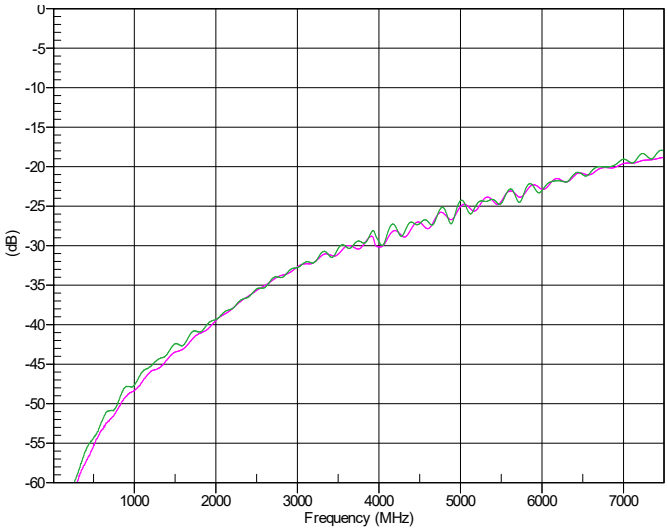



**Figure 6 RF1, RF2 Isolation**

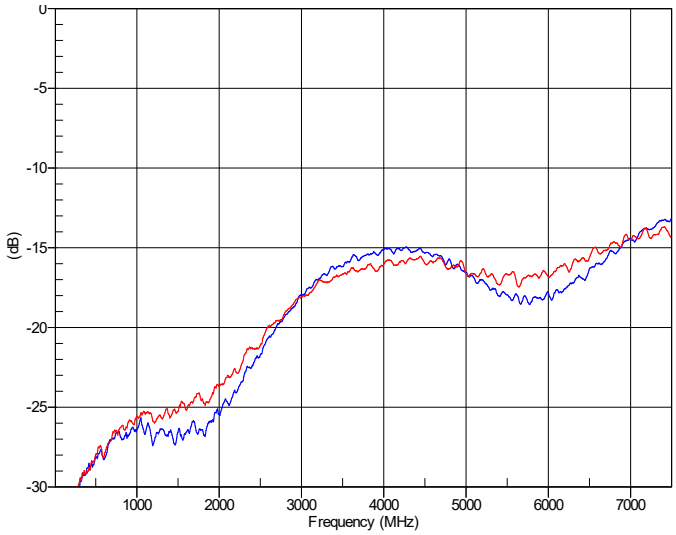



**Figure 7 RF1, RF2 Return Loss**

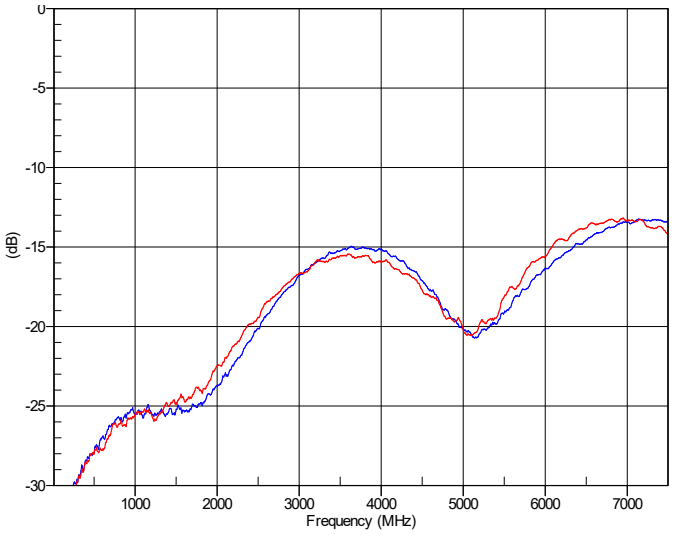



**Figure 8 ANT Return Loss**

## 11.0 Device Package Information

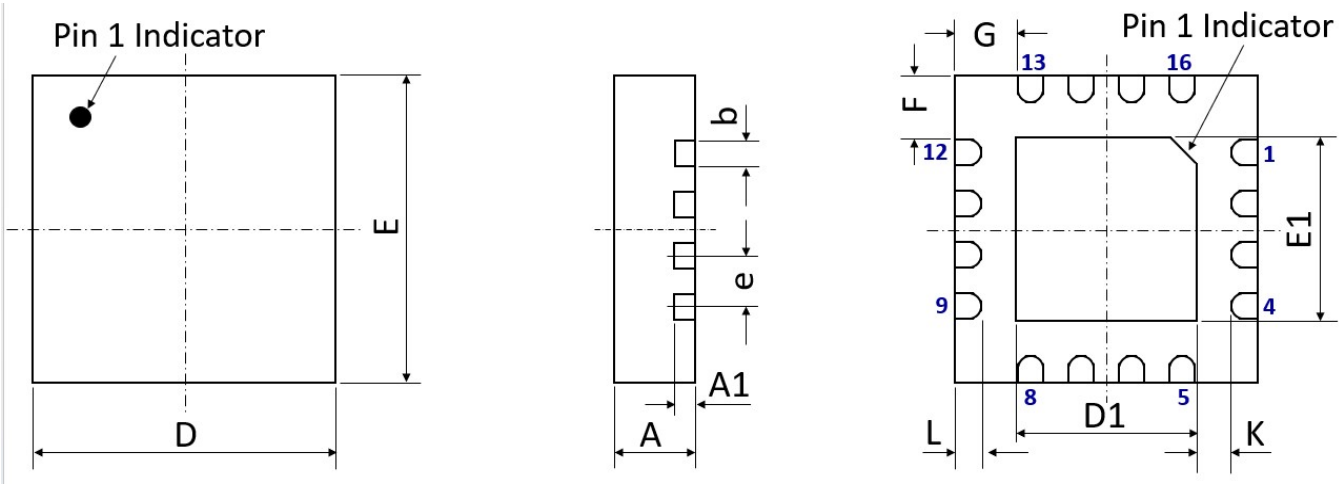



**Figure 9 Device Package Drawing**
(All dimensions are in mm)

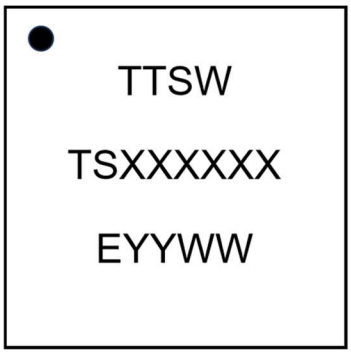
**Table 6 Device Package Dimensions**

| **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) | **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) |
|---|---|---|---|---|---|
| A | 0.80 | ±0.05 | E | 3.00 BSC | ±0.05 |
| A1 | 0.203 | ±0.02 | E1 | 1.70 | ±0.05 |
| b | 0.25 | +0.05/-0.07 | F | 0.625 | ±0.05 |
| D | 3.00 BSC | ±0.05 | G | 0.625 | ±0.05 |
| D1 | 1.70 | ±0.05 | L | 0.25 | ±0.05 |
| e | 0.50 BSC | ±0.05 | K | 0.40 | ±0.05 |

**Note:** Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

**Attention:**
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

**Top-marking specification:**




● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

## 12.0 PCB Land Design

**Guidelines:**
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9.

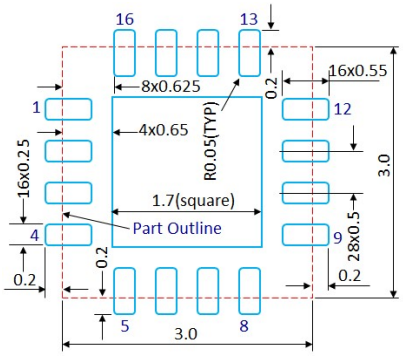



**Figure 10 PCB Land Pattern**
(Dimensions are in mm)




Non-Solder Mask Defined (Preferred)

Solder Mask Defined

**Figure 11 Solder Mask Pattern**
(Dimensions are in mm)

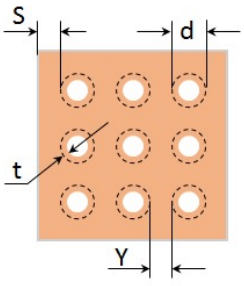



**Figure 12 Thermal Via Pattern**
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

## 13.0 PCB Stencil Design

**Guidelines:**

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

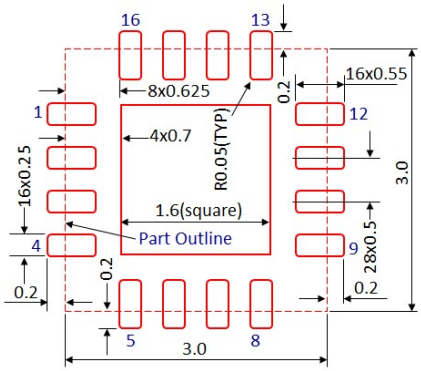



**Figure 13 Stencil Openings**
(Dimensions are in mm)

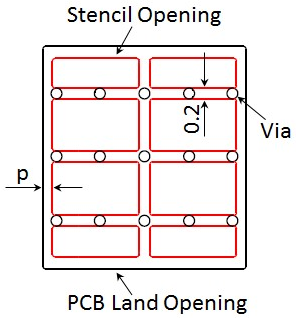



**Figure 14 Stencil Openings Shall not Cover Via Areas If Possible**
(Dimensions are in mm)

## 14.0 Tape and Reel Information

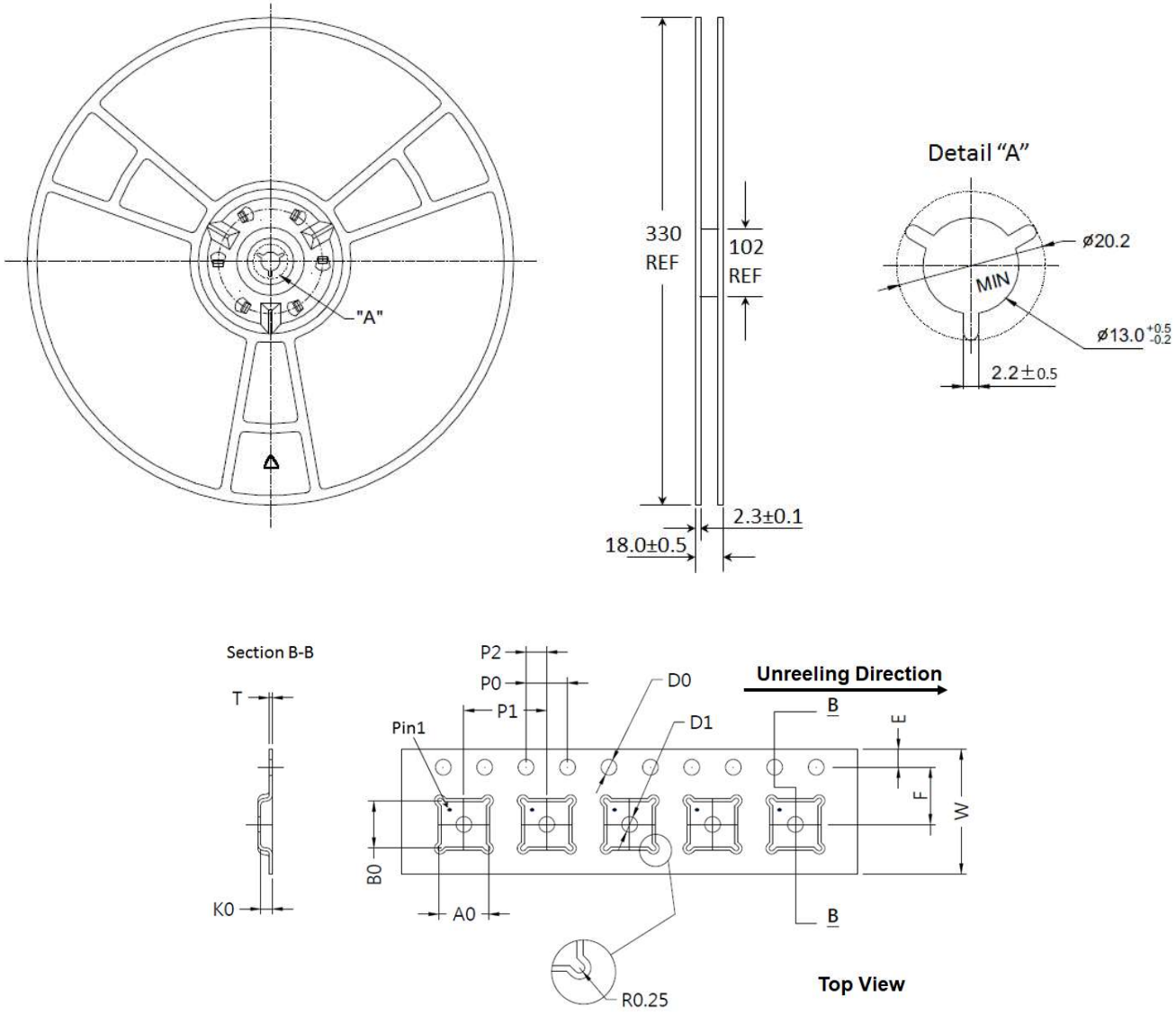



**Figure 15 Tape and Reel Drawing**

**Table 7 Tape and Reel Dimensions**

| **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) | **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) |
|---|---|---|---|---|---|
| A0 | 3.35 | ±0.10 | K0 | 1.10 | ±0.10 |
| B0 | 3.35 | ±0.10 | P0 | 4.00 | ±0.10 |
| D0 | 1.50 | +0.10/-0.00 | P1 | 8.00 | ±0.10 |
| D1 | 1.50 | +0.10/-0.00 | P2 | 2.00 | ±0.05 |
| E | 1.75 | ±0.10 | T | 0.30 | ±0.05 |
| F | 5.50 | ±0.05 | W | 12.00 | ±0.30 |

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