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# LNBH221PD-TR

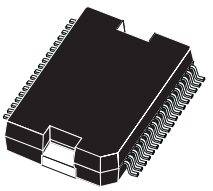
www.win-source.net 0086-755-83957316

# LNBH221

## Dual LNB supply and control IC with step-up converter and I²C interface

## Features

- All the features are the same for both section
- Complete and independent interface between LNBS and relevant I²C bus
- Built-in DC-DC controller for single 12 V supply operation and high efficiency (typ. 93 % @ 500 mA)
- LNB output current guaranteed up to 500 mA
- Both compliant with EUTELSAT and direct output voltage specification accurate built-in 22 kHz tone oscillator suits widely accepted standards
- Fast oscillator start-up facilitates DiSEqC™ encoding
- Built-in 22 kHz tone detector supports bi-directional DiSEqC™ 2.0
- Semi low-drop post regulator and high efficiency step-up PWM for low power loss: Typ. 0.56 W @ 125 mA
- Two output pins suitable to by-pass the output R-L filter and avoid any tone distortion (R-L filter as per DiSEqC 2.0 specs, see *Figure 4 on page 8*)
- Overload and over-temperature internal protections
- Overload and over-temperature I²C diagnostic bits
- LNB short circuit SOA protection with I²C diagnostic bit
- +/- 4 kV ESD tolerant on input/output power pins



**PowerSO-36**

## Description

Intended for analog and digital dual satellite STB receivers/sat-TV, sets/PC cards, the LNBH221 is a voltage regulator and interface IC, assembled in PowerSO-36, specifically designed to provide the power 13/18 V, and the 22 kHz tone signalling for two independent LNB down converters or to a multiswitch box that could be independently powered and set. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

Obsolete Product(s) - Obsolete Product(s)

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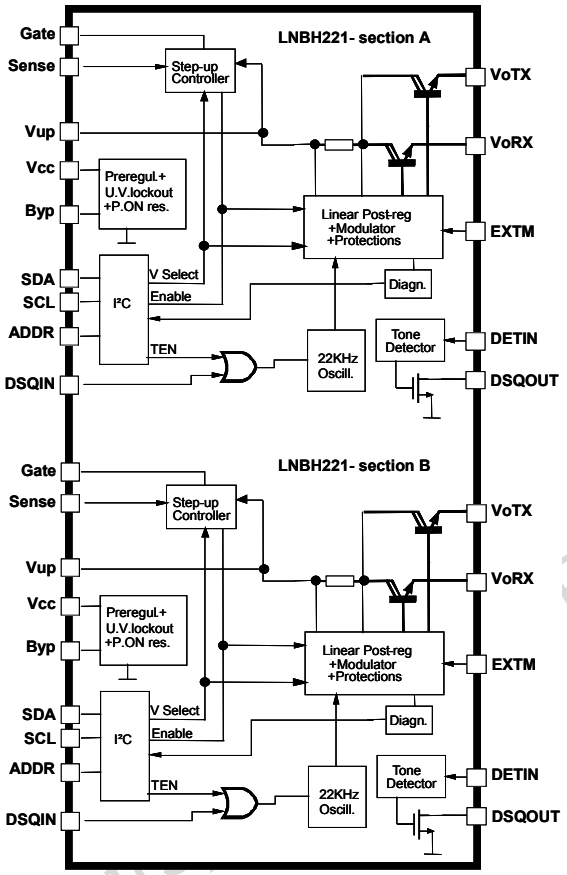
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# 1 Diagram

**Figure 1. Block diagram**




Obsolete Product(s)

# 2 Maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC input voltage | -0.3 to 16 | V |
| $V_{UP}$ | DC input voltage | -0.3 to 25 | V |
| $V_O$TX/RX | DC output pin voltage | -0.3 to 25 | V |
| $I_O$ | Output current | Internally limited | mA |
| $V_I$ | Logic input voltage (SDA, SCL, DSQIN) | -0.3 to 7 | V |
| $V_{DETIN}$ | Detector input signal amplitude | -0.3 to 2 | $V_{PP}$ |
| $V_{OH}$ | Logic high output voltage (DSQOUT) | -0.3 to 7 | V |
| $I_{GATE}$ | Gate current | ± 400 | mA |
| $V_{SENSE}$ | Current sense voltage | -0.3 to 1 | V |
| $V_{ADDRESS}$ | Address pin voltage | -0.3 to 7 | V |
| $T_{STG}$ | Storage temperature range | -40 to 150 | °C |
| $T_J$ | Operating junction temperature range | -40 to 125 | °C |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance junction-case | 2 | °C/W |

Obsolete Product(s) - Obsolete Product(s)

# 3 Pin configuration

**Figure 2. Pin configurations (top view)**

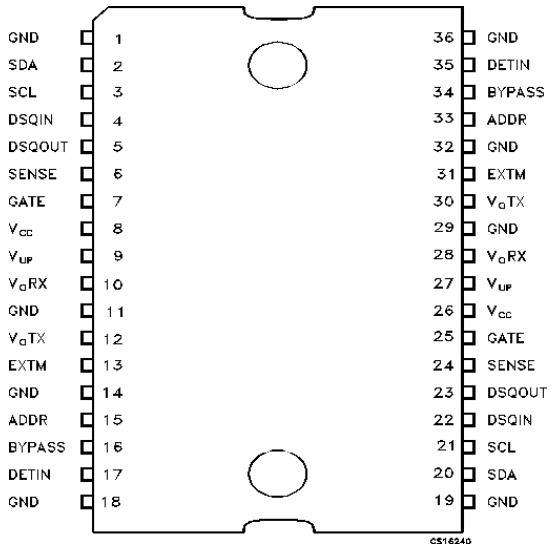



**Table 3. Pin description**

| Symbol | Name | Function | Pin number Sect: | |
|---|---|---|---|---|
| | | | A | B |
| $V_{CC}$ | Supply input | 8 V to 15 V supply. A 220 µF bypass capacitor to GND with a 470 nF (ceramic) in parallel is recommended. | 8 | 26 |
| GATE | External switch gate | External MOS switch gate connection of the step-up converter. | 7 | 25 |
| SENSE | Current sense (input) | Current Sense comparator input. Connected to current sensing resistor. | 6 | 24 |
| $V_{UP}$ | Step-up voltage | Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor. | 9 | 27 |
| $V_O$RX | Output port during 22 kHz Tone RX | RX Output to the LNB in DiSEqC 2.0 application. See truth table for voltage selections and description on page 4. | 28 | 10 |
| SDA | Serial data | Bidirectional data from/to I²C bus. | 2 | 20 |
| SCL | Serial clock | Clock from I²C bus. | 3 | 21 |
| DSQIN | DiSEqC input | When the TEN bit of the system register is LOW, this pin will accept the DiSEqC code from the main µcontroller. Each section of the LNBH221 will use this code to modulate the internally generated 22 kHz carrier. Set to GND this pin if not used. | 4 | 22 |
| DETIN | Detector in | 22 kHz tone detector input. Must be AC coupled to the DiSEqC bus. | 35 | 17 |

Obsolete Product(s) - Obsolete Product(s)

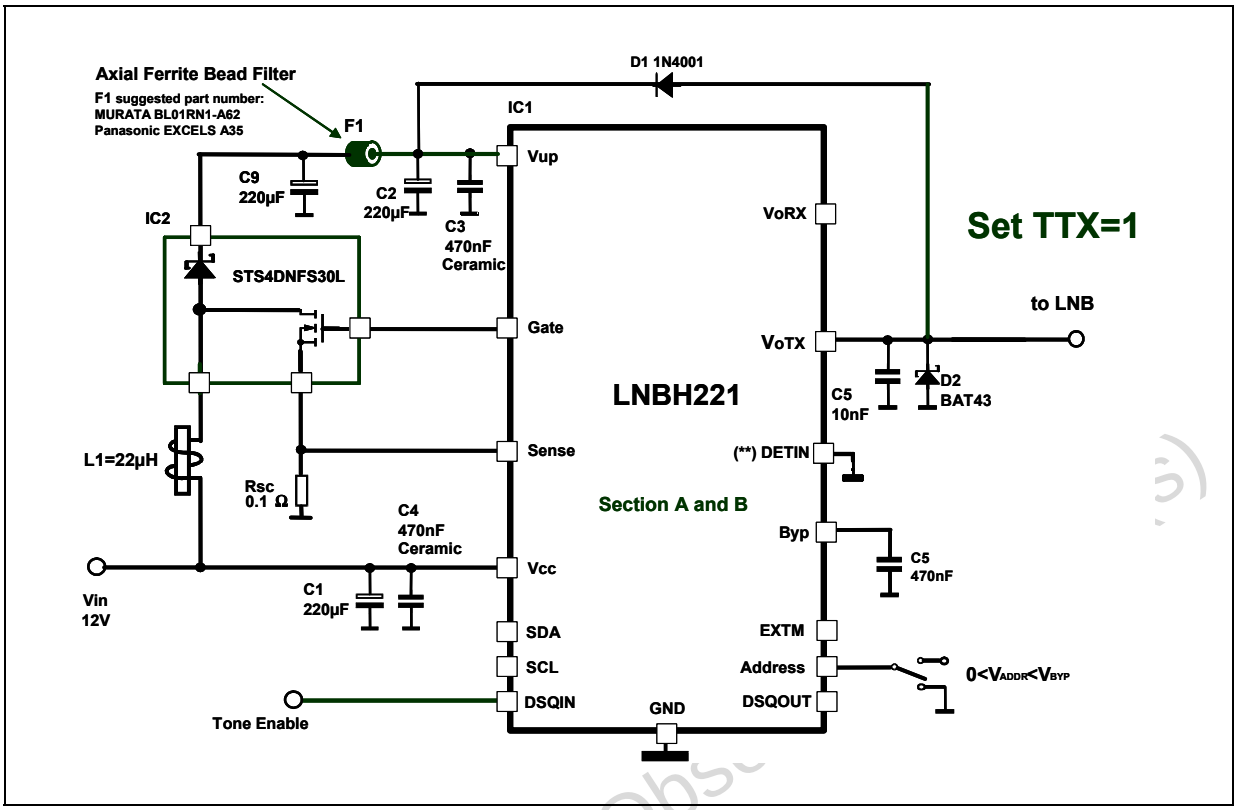
**Table 3. Pin description**

| Symbol | Name | Function | Pin number Sect: | |
|---|---|---|---|---|
| | | | A | B |
| DSQOUT | DiSEqC output | Open drain output of the tone detector to the main microcontroller for DiSEqC data decoding. It is LOW when tone is detected on the DETIN. | 5 | 23 |
| EXTM | External modulation | External modulation input. Needs DC decoupling to the AC source. If not used, can be left open. | 31 | 13 |
| GND | Ground | Circuit ground. It is internally connected to the die frame for heat dissipation. | 1, 14, 18, 19, 32, 36 | 1, 14, 18, 19, 32, 36 |
| BYP | Bypass capacitor pin | Needed for internal pre regulator filtering. | 34 | 16 |
| $V_O$TX | Output port during 22 kHz tone TX | Output of the linear post regulator/modulator to the LNB. See truth table for voltage selections. | 30 | 12 |
| GND | Ground | To be connected to ground. | 29 | 11 |
| ADDR | Address setting | Four I²C bus addresses available by setting the address pin level voltage. | 33 | 15 |

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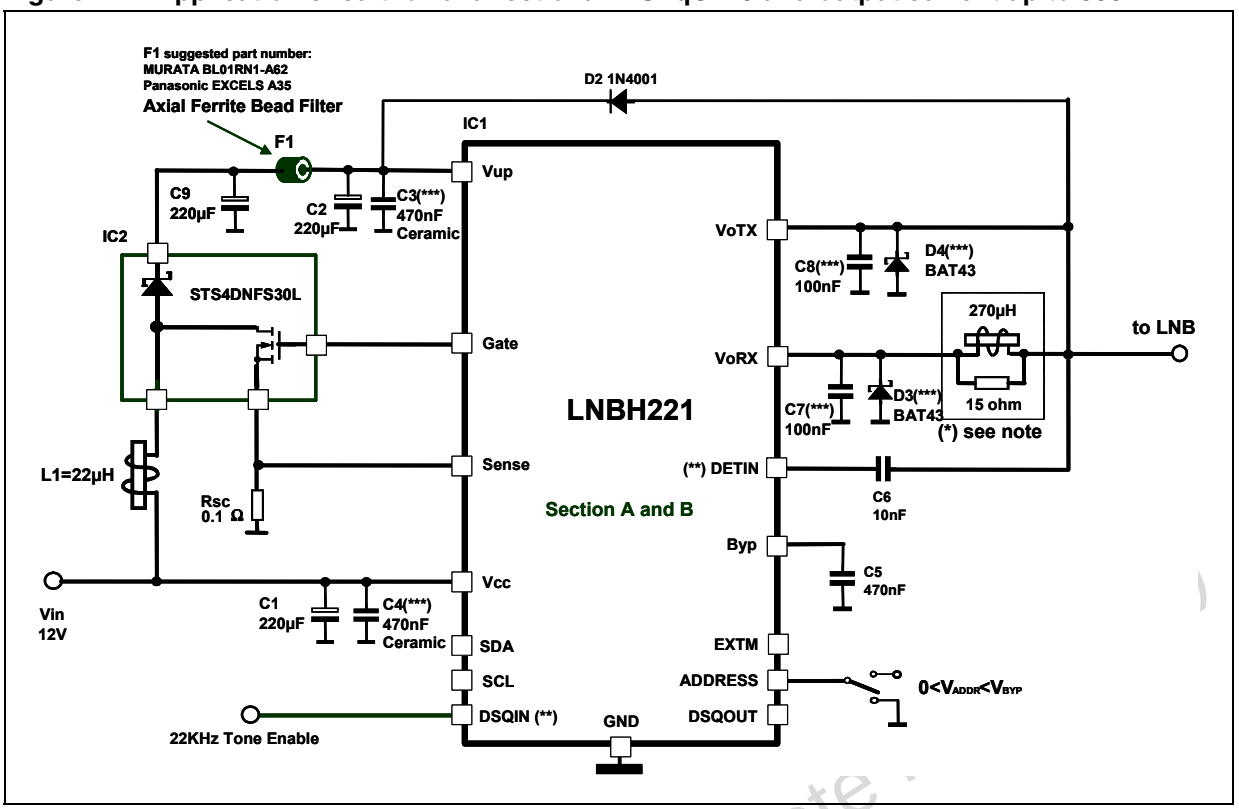
# 4 Typical application circuits for each section: A and B

**Figure 3. Application circuit for DiSEqC 1.x and output current up to 500 mA**




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**Figure 4. Application circuit for bi-directional DiSEqC 2.0 and output current up to 500 mA**




C8, D3 and D4 are needed to protect the output pins from any negative voltage spikes during high speed voltage transitions.

(*) R-L filter to be used according to EUTELSAT recommendation to implement the DiSEqC™ 2.0, (see DiSEqC™ implementation on page 8). If bidirectional DiSEqC™ 2.0 is not implemented it can be removed both with C8 and D4.

(**) Do not leave these pins floating if not used.

(***) To be soldered as close as possible to relative pins.

Obsolete Product(s) - Obsolete

# 5 Application information

Basically, the LNBH221 includes two circuits that are completely independent. Each circuit can be separately controlled and must have its independent external components. All the below specification must be considered equal for each section.

This IC has a built in DC-DC step-up controller that, from a single supply source ranging from 8 to 15 V, generates the voltages ($V_{UP}$) that let the linear post-regulator to work at a minimum dissipated power of 1 W typ. @ 500 mA load (the linear regulator drop voltage is internally kept at: $V_{UP}$ - $V_{OUT}$ = 2 V typ.). An under voltage lockout circuit will disable the whole circuit when the supplied $V_{CC}$ drops below a fixed threshold (6.7 V typically). The internal 22 kHz tone generator is factory trimmed in accordance to the standards, and can be controlled either by the I²C interface or by a dedicated pin (DSQIN) that allows immediate DiSEqC™ data encoding *Note 1*. When the TEN (Tone ENable) I²C bit it is set to HIGH, a continuous 22 kHz tone is generated on the output regardless of the DSQIN pin logic status.

The TEN bit must be set LOW when the DSQIN pin is used for DiSEqC™ encoding. The fully bi-directional DiSEqC™ 2.0 interfacing is completed by the built-in 22 kHz tone detector. Its input pin (DETIN) must be AC coupled to the DiSEqC™ bus, and the extracted PWK data are available on the DSQOUT pin *Note 1*. To comply to the bi-directional DiSEqC™ 2.0 bus hardware requirements an output R-L filter is needed. The LNBH221 is provided with two output pins: the $V_O$TX to be used during the tone transmission and the $V_O$RX to be used when the tone is received. This allows the 22 kHz Tone to pass without any losses due to the R-L filter impedance (see DiSeqC 2.0 application circuit on page 4). In DiSeqC 2.0 applications during the 22 kHz transmission activated by DSQIN pin (or TEN I²C bit), the $V_O$TX pin must be preventively set ON by the TTX I²C bit and, both the 13/18 V power supply and the 22 kHz tone, are provided by mean of $V_O$TX output. As soon as the tone transmission is expired, the $V_O$TX must be set to OFF by setting the TTX I²C bit to zero and the 13/18 V power supply is provided to the LNB by the $V_O$RX pin through the R-L filter. When the LNBH221 is used in DiSeqC 1.x applications the R-L filter is not required (see DiSeqC 1.x *Figure 4 on page 8*), the TTX I²C bit must be kept always to HIGH so that, the $V_O$TX output pin can provide both the 13/18 V power supply and the 22 kHz tone, enabled by DSQIN pin or by TEN I²C bit. All the functions of this IC are controlled via I²C bus by writing 6 bits on the system register (SR, 8 bits). The same register can be read back, and two bits will report the diagnostic status. When the IC is put in stand-by (EN bit LOW), the power blocks are disabled.

When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18 V by mean of the VSEL bit (Voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, the LNBH221 is provided with the LLC I²C bit that increase the selected voltage value (+1 V when VSEL = 0 and +1.5 V when VSEL = 1) to compensate for the excess voltage drop along the coaxial cable (LLC bit HIGH). By mean of the LLC bit, the LNBH221 is also compliant to the American LNB power supply standards that require the higher output voltage level to 19.5 V (typ.) (instead of 18 V), by simply setting the LLC=1 when VSEL = 1. In order to improve design flexibility and to allow implementation of new coming LNB remote control standards, an analogic modulation input pin is available (EXTM).

An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. Also in this case, the $V_O$TX output must be set ON during the tone transmission by setting the TTX bit high. When external modulation is not used, the relevant pin can be left open. The current limitation block is SOA type: if the output port is shorted to ground, the SOA current limitation block limits the short circuit current ($I_{SC}$) at typically 300 mA or 200 mA respectively for $V_{OUT}$ 13 V or 18 V, to reduce the power dissipation.

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Moreover, it is possible to set the short circuit current protection either statically (simple current clamp) or dynamically by the PCL bit of the I²C SR; when the PCL (pulsed current limiting) bit is set to LOW, the overcurrent protection circuit works dynamically, as soon as an overload is detected, the output is shut-down for a time $T_{OFF}$, typically 900 ms. Simultaneously the OLF bit of the system register is set to HIGH. After this time has elapsed, the output is resumed for a time $T_{ON}$ = 1/10 $T_{OFF}$ (typ.). At the end of $T_{ON}$, if the overload is still detected, the protection circuit will cycle again through $T_{OFF}$ and $T_{ON}$. At the end of a full $T_{ON}$ in which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical $T_{ON}$ + $T_{OFF}$ time is 990 ms and it is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up in most conditions. However, there could be some cases in which an highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL = HIGH) and then switching to the dynamic mode (PCL = LOW) after a chosen amount of time. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared. This IC is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the linear regulator are shut off, and the OTF SR bit is set to HIGH. Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 140 °C (typ.).

*Note: 1 External components are needed to comply to bi-directional DiSEqC™ bus hardware requirements. Full compliance of the whole application to DiSEqC™ specifications is not implied by the use of this IC.*

*2 NOTICE: DiSEqC is a trademark of EUTELSAT. I²C is a trademark of Philips Semiconductors.*

## 5.1 I²C bus interface (one for each section)

Data transmission from main micropower to the LNBH221 and viceversa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

## 5.2 Data validity

As shown in *Figure 5*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

## 5.3 Start and stop conditions

As shown in *Figure 6* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

Obsolete Product(s) - Obsolete Product(s)

## 5.4 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

## 5.5 Acknowledge

The master (micropower) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 7*). The peripheral (LNBH221) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH221 won't generate the acknowledge if the $V_{CC}$ supply is below the under voltage lockout threshold (6.7 V typ.).

## 5.6 Transmission without acknowledgement

Avoiding to detect the acknowledge of the LNBH221, the micropower can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

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**Figure 5. Data validity on the I²C bus**

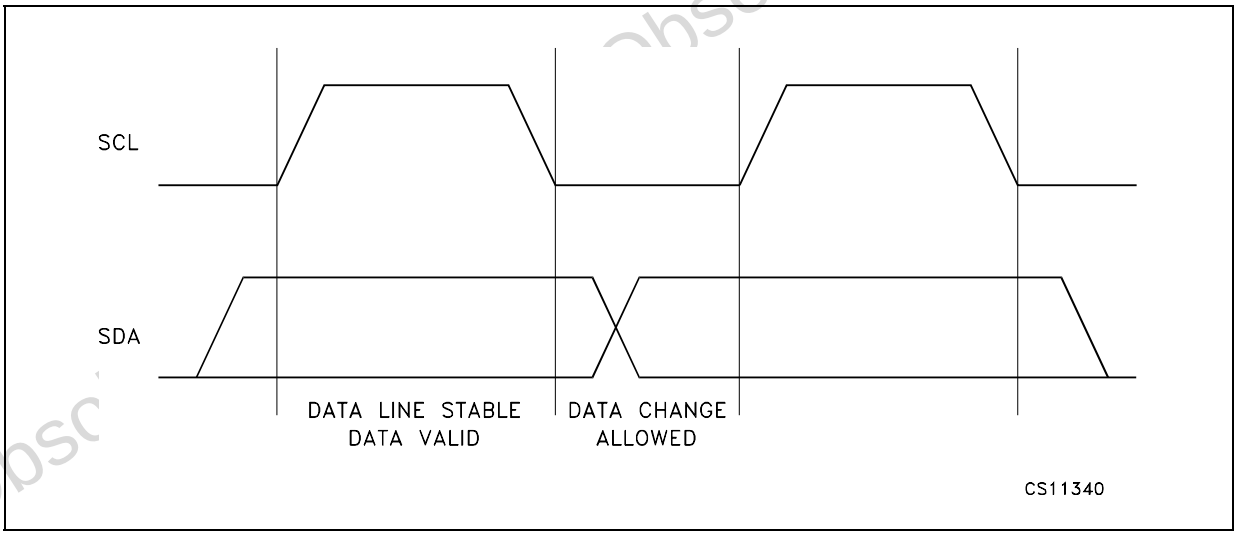


**Figure 6. Timing diagram on I²C bus**

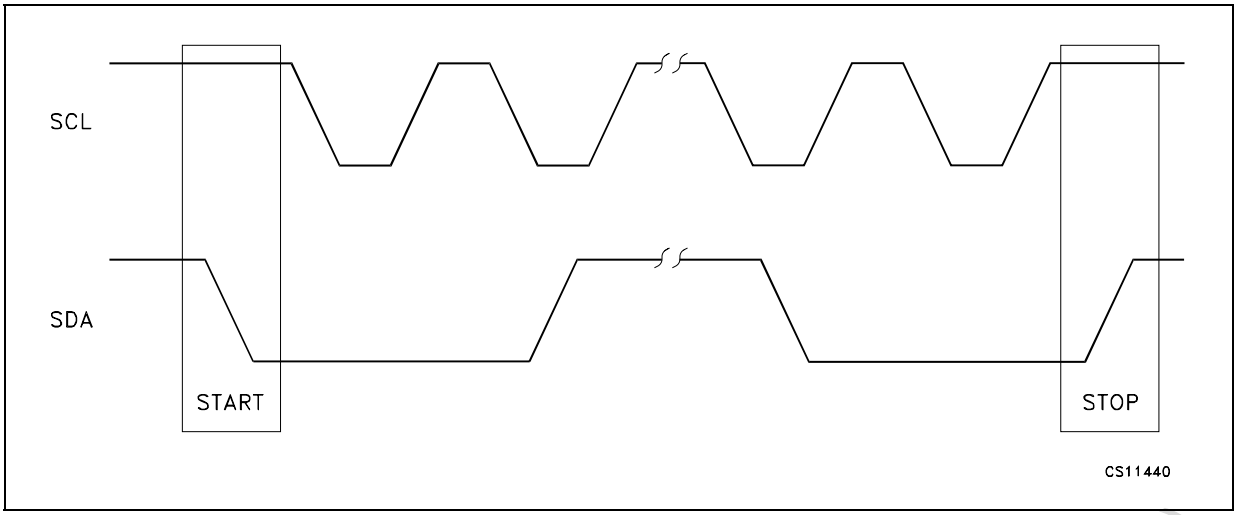
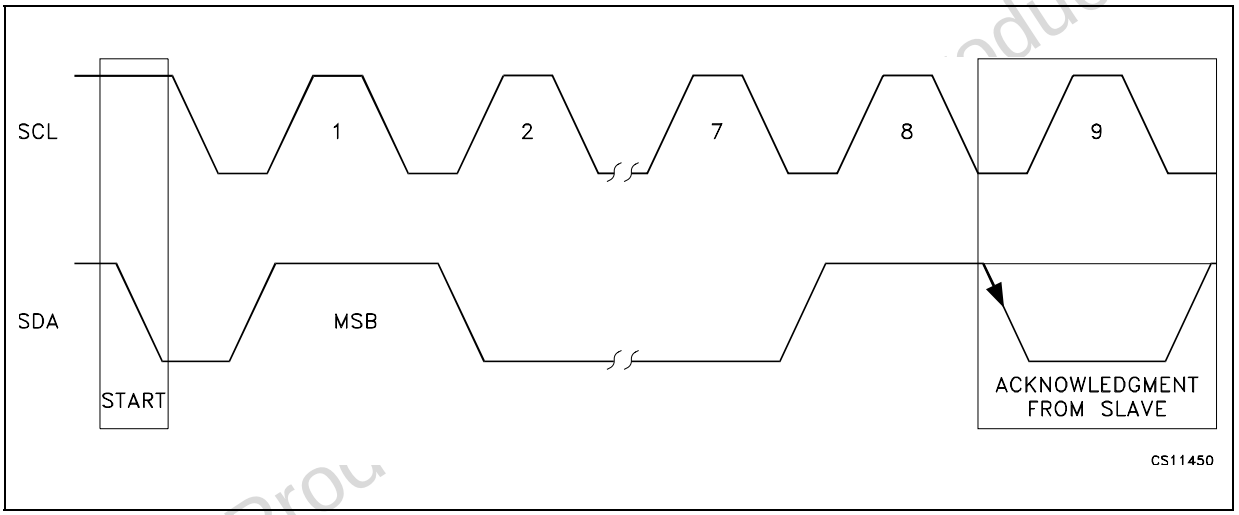



**Figure 7. Acknowledge on I²C bus**



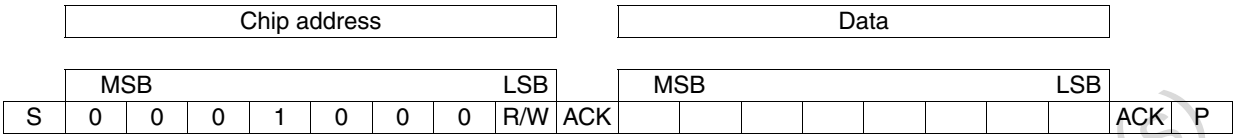

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# 6 LNBH221 software description (same for both section)

## 6.1 Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte = hex 10 / 11 (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)




ACK= Acknowledge

S= Start

P= Stop

R/W= Read/Write

## 6.2 System register (SR, 1 byte)

| **MSB** | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|
| R, W | R, W | R, W | R, W | R, W | R, W | R | R |
| PCL | TTX | TEN | LLC | VSEL | EN | OTF | OLF |

R,W= read and write bit

R= Read-only bit

All bits reset to 0 at power-on

## 6.3 Transmitted data (I²C bus write mode)

When the R/W bit in the chip address is set to 0, the main micropower can write on the system register (SR) of the LNBH221 via I²C bus. Only 6 bits out of the 8 available can be written by the micropower, since the remaining 2 are left to the diagnostic flags, and are read-only.

Obsolete Product(s) - Obsolete Product(s)

**Table 4. Truth table**

| PCL | TTX | TEN | LLC | VSEL | EN | OTF | OLF | Function |
|---|---|---|---|---|---|---|---|---|
| | | | 0 | 0 | 1 | X | X | $V_{OUT}$=13.25V, $V_{UP}$=15.25V |
| | | | 0 | 1 | 1 | X | X | $V_{OUT}$=18V, $V_{UP}$=20V |
| | | | 1 | 0 | 1 | X | X | $V_{OUT}$=14.25V, $V_{UP}$=16.25V |
| | | | 1 | 1 | 1 | X | X | $V_{OUT}$=19.5V, $V_{UP}$=21.5V |
| | | 0 | | | 1 | X | X | 22 kHz tone is controlled by DSQIN pin |
| | | 1 | | | 1 | X | X | 22 kHz tone is ON, DSQIN pin disabled |
| | 0 | | | | 1 | X | X | $V_O$RX output is ON, output voltage controlled by VSEL and LLC |
| | 1 | X | | | 1 | X | X | $V_O$TX output is ON, 22 kHz controlled by DSQIN or TEN, output voltage level controlled by VSEL and LLC |
| 0 | | | | | 1 | X | X | Pulsed (dynamic) current limiting is selected |
| 1 | | | | | 1 | X | X | Static current limiting is selected |
| X | X | X | X | X | 0 | X | X | Power blocks disabled |

X= don't care.

Values are typical unless otherwise specified.

## 6.4 Received data (I²C bus read mode)

The LNBH221 can provide to the master a copy of the system register information via I²C bus in read mode. The read mode is master activated by sending the chip address with R/W bit set to 1.

At the following master generated clocks bits, the LNBH221 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- acknowledge the reception, starting in this way the transmission of another byte from the LNBH221;

- no acknowledge, stopping the read mode communication.

While the whole register is read back by the micropower, only the two read-only bits OLF and OTF convey diagnostic informations about the LNBH221.

**Table 5. Register**

| PCL | ISEL | TEN | LLC | VSEL | EN | OTF | OLF | Function |
|---|---|---|---|---|---|---|---|---|
| These bits are read exactly the same as they were left after last write operation | | | | | | 0 | | $T_J$<140°C, normal operation |
| | | | | | | 1 | | $T_J$>150°C, power block disabled |
| | | | | | | | 0 | $I_{OUT}$<$I_{OMAX}$, normal operation |
| | | | | | | | 1 | $I_{OUT}$>$I_{OMAX}$, overload protection triggered |

Values are typical unless otherwise specified.

Obsolete Product(s) - Obsolete Product(s)

## 6.5 Power-on I²C interface reset

The I²C interface built in the LNBH221 is automatically reset at power on. As long as the $V_{CC}$ stays below the under voltage lockout threshold (6.7 V typ.), the interface will not respond to any I²C command and the system register (SR) is initialized to all zeroes, thus keeping the power blocks disabled. Once the $V_{CC}$ rises above 7.3 V typ, the I²C interface becomes operative and the SR can be configured by the main micropower. This is due to 500 mV of hysteresis provided in the UVL threshold to avoid false retriggering of the power-on reset circuit.

## 6.6 Address pin

Connecting this pin to GND the chip I²C interface address is 0001000, but, it is possible to choice among 4 different addresses simply setting this pin at 4 fixed voltage levels (see *Table 9 on page 17*).

## 6.7 DiSEqC™ implementation

The LNBH221 helps the system designer to implement the bi-directional DiSEqC 2.0 protocol by allowing an easy PWK modulation/demodulation of the 22 kHz carrier. The PWK data are exchanged between the LNBH221 and the main micropower using logic levels that are compatible with both 3.3 and 5 V microcontrollers. This data exchange is made through two dedicated pins, DSQIN and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the micropower, thus leaving to the resident firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC protocol. Full compliance of the system to the specification is thus not implied by the bare use of the LNBH221. The system designer should also take in consideration the bus hardware requirements; that can be simply accomplished by the R-L termination connected on the $V_{OUT}$ pins of the LNBH221, as shown in the *Figure 4 on page 8*. To avoid any losses due to the R-L impedance during the tone transmission, the LNBH221 has dedicated output ($V_O$TX) that, in a DiSEqC 2.0 application, is connected after the filter and must be enabled by setting the TTX SR bit HIGH only during the tone transmission (see DiSEqC 2.0 *Application information on page 9*). Unidirectional (1.x) DiSEqC and non-DiSEqC systems normally don't need this termination, and the $V_O$TX pin can be directly connected to the LNB supply port of the tuner (see *Figure 3: Application circuit for DiSEqC 1.x and output current up to 500 mA on page 7*). There is also no need of tone decoding, thus DETIN and DSQOUT pins can be left unconnected and the tone is provided by the $V_O$TX.

Obsolete Product(s) - Obsolete Product(s)

# 7 Electrical characteristics

$T_J$ = 0 to 85 °C, EN = 1, TTX = 0/1, LLC=VSEL=TEN=PCL=0, DSQIN=LOW, $V_{IN}$ = 12 V, $I_{OUT}$ = 50 mA, unless otherwise specified. See software description section for I²C access to the system register.

**Table 6. Electrical characteristics of each section (A and B)**

| Symbol | Parameter | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage | $I_{OUT}$ = 500 mA TEN=VSEL=LLC=1 | | 8 | | 15 | V |
| $I_{IN}$ | Supply current | EN=TEN=VSEL=LLC=1, No Load | | | 20 | 40 | mA |
| | | EN=0 | | | 3.5 | 7 | |
| $V_{OUT}$ | Output voltage | $I_{OUT}$ = 500 mA VSEL=1 | LLC=0 | 17.3 | 18 | 18.7 | V |
| | | | LLC=1 | 18.7 | 19.5 | 20.3 | |
| $V_{OUT}$ | Output voltage | $I_O$ = 500 mA VSEL=0 | LLC=0 | 12.75 | 13.25 | 13.75 | V |
| | | | LLC=1 | 13.75 | 14.25 | 14.75 | |
| $\Delta V_{OUT}$ | Line regulation | $V_{IN}$ =8 to 15V | VSEL=0 | | 5 | 40 | mV |
| | | | VSEL=1 | | 5 | 60 | |
| $\Delta V_{OUT}$ | Load regulation | VSEL = 0 or 1 $I_{OUT}$ = 50 to 500mA | | | | 200 | mV |
| $I_{MAX}$ | Output current limiting | | | 500 | | 750 | mA |
| $I_{SC}$ | Output short circuit current | VSEL = 0 | | | 300 | | mA |
| | | VSEL = 1 | | | 200 | | |
| $t_{OFF}$ | Dynamic overload protection OFF time | PCL=0, output shorted | | | 900 | | ms |
| $t_{ON}$ | Dynamic overload protection ON time | PCL=0, output shorted | | | $t_{OFF}$/10 | | ms |
| $f_{TONE}$ | Tone frequency | TEN=1 | | 20 | 22 | 24 | kHz |
| $A_{TONE}$ | Tone amplitude | TEN=1 | | 0.55 | 0.72 | 0.9 | $V_{PP}$ |
| $D_{TONE}$ | Tone duty cycle | TEN=1 | | 40 | 50 | 60 | % |
| $t_r$, $t_f$ | Tone rise and fall time | TEN=1 | | 5 | 8 | 15 | µs |
| $G_{EXTM}$ | External modulation gain | $\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 50kHz, TTX=1 | | | 6 | | |
| $V_{EXTM}$ | External modulation input voltage | AC Coupling, TTX=1 | | | | 400 | $mV_{PP}$ |
| $Z_{EXTM}$ | External modulation impedance | f = 10Hz to 50kHz | | | 260 | | W |
| $f_{SW}$ | DC-DC converter switch frequency | | | | 220 | | kHz |
| $f_{DETIN}$ | Tone detector frequency capture range | 0.4$V_{PP}$ sinewave | | 18 | | 24 | kHz |

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**Table 6. Electrical characteristics of each section (A and B) (continued)**

| Symbol | Parameter | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DETIN}$ | Tone detector input amplitude | $f_{IN}$=22 kHz sinewave | 0.2 | | 1.5 | $V_{PP}$ |
| $Z_{DETIN}$ | Tone detector input impedance | | | 150 | | kΩ |
| $V_{OL}$ | DSQOUT pin logic LOW | Tone present, $I_{OL}$=2mA | | 0.3 | 0.5 | V |
| $I_{OZ}$ | DSQOUT pin leakage current | Tone absent, $V_{OH}$ = 6V | | | 10 | µA |
| $V_{IL}$ | DSQIN input pin logic LOW | | | | 0.8 | V |
| $V_{IH}$ | DSQIN input pin logic HIGH | | 2 | | | V |
| $I_{IH}$ | DSQIN pin input current | $V_{IH}$ = 5V | | 15 | | µA |
| $I_{OBK}$ | Output backward current | EN=0, $V_{OBK}$ = 18V | | -6 | -15 | mA |
| $T_{SHDN}$ | Thermal shutdown threshold | | | 150 | | °C |
| $\Delta T_{SHDN}$ | Thermal shutdown hysteresis | | | 15 | | °C |

**Table 7. Gate and sense electrical characteristics** ($T_J$ = 0 to 85 °C, $V_{IN}$ = 12 V)

| Symbol | Parameter | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{DSON-L}$ | Gate LOW $R_{DSON}$ | $I_{GATE}$=-100mA | | 4.5 | | Ω |
| $R_{DSON-H}$ | Gate LOW $R_{DSON}$ | $I_{GATE}$=100mA | | 4.5 | | Ω |
| $V_{SENSE}$ | Current limit sense voltage | | | 200 | | mV |

**Table 8. I²C electrical characteristics** ($T_J$ = 0 to 85 °C, $V_{IN}$ = 12 V)

| Symbol | Parameter | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | LOW level input voltage | SDA, SCL | | | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | SDA, SCL | 2 | | | V |
| $I_{IN}$ | Input current | SDA, SCL, $V_{IN}$= 0.4 to 4.5V | -10 | | 10 | µA |
| $V_{OL}$ | Low level output voltage | SDA (open drain), $I_{OL}$ = 6mA | | | 0.6 | V |
| $f_{MAX}$ | Maximum clock frequency | SCL | 500 | | | kHz |

**Table 9. Address pin characteristics** ($T_J$ = 0 to 85 °C, $V_{IN}$ = 12 V)

| Symbol | Parameter | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ADDR-1}$ | "0001000" addr pin voltage | | 0 | | 0.7 | V |
| $V_{ADDR-2}$ | "0001001" addr pin voltage | | 1.3 | | 1.7 | V |
| $V_{ADDR-3}$ | "0001010" addr pin voltage | | 2.3 | | 2.7 | V |
| $V_{ADDR-4}$ | "0001011" addr pin voltage | | 3.3 | | 5 | V |
| $V_{ADDR-1}$ | "0001000" addr pin voltage | | 0 | | 0.7 | V |

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# 8 Thermal design notes

During normal operation, the LNBH221 device dissipates some power. At rated output current of 500 mA on each section output, the voltage drop on both linear regulators lead to a total dissipated power that is typically 2 W. The heat generated requires a suitable heatsink to keep the junction temperature below the over-temperature protection threshold. Assuming a 45 °C temperature inside the set-top-box case, the total $R_{thJC}$ has to be less than 40 °C/W.

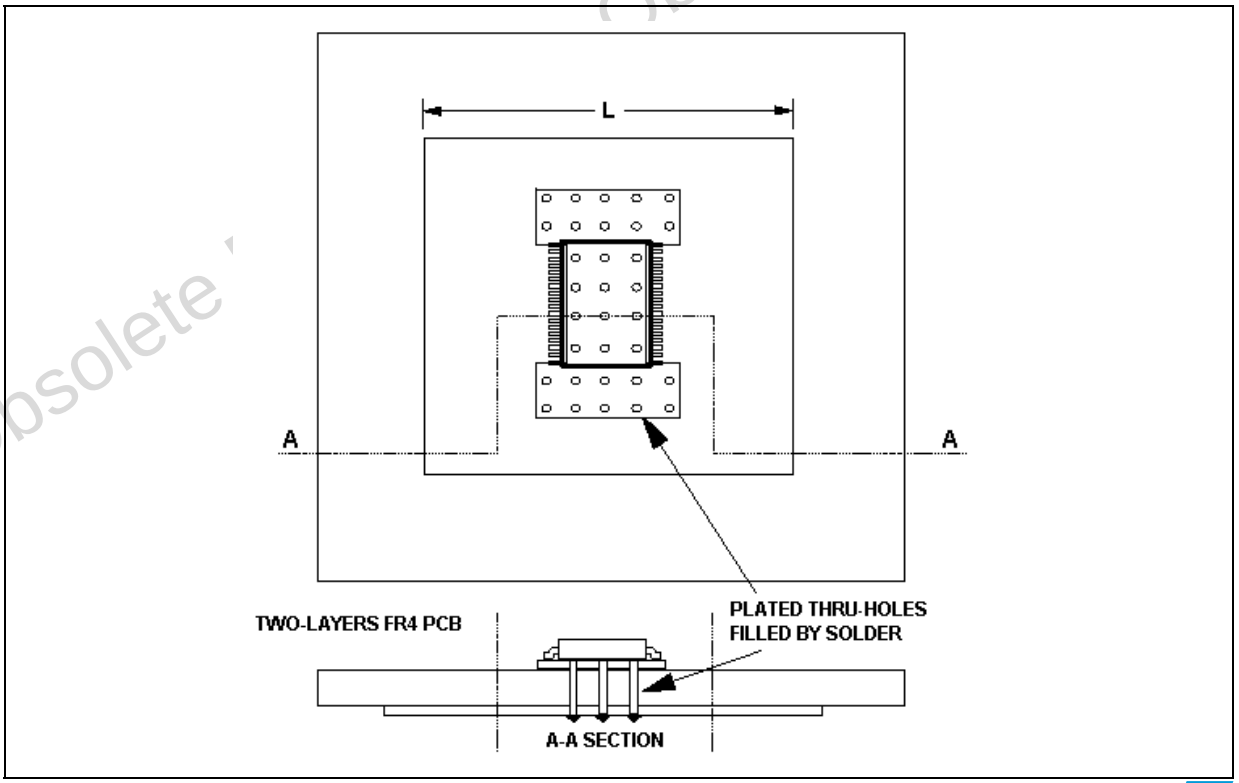
While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

Given for the PSO-36 package an $R_{thJC}$ equal to 2 °C/W, a maximum of 38 °C/W are left to the PCB heatsink. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In figure 8, it is shown a suggested layout for the PSO-36 package with a dual layer PCB, where the IC exposed pad connected to GND and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when L = 40 mm, achieves an $R_{thJA}$ of about 28 °C/W.

Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground exposed pad approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

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**Figure 8. PowerSO-36 suggested PCB heatsink layout**



# 9 Typical performance characteristics (of each section)

$T_J$ = 25 °C, unless otherwise specification.

**Figure 9. Output voltage vs. temperature**

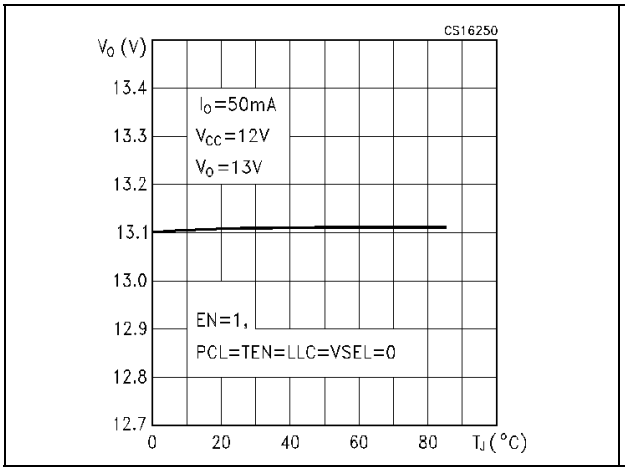



**Figure 10. Output voltage vs. temperature**

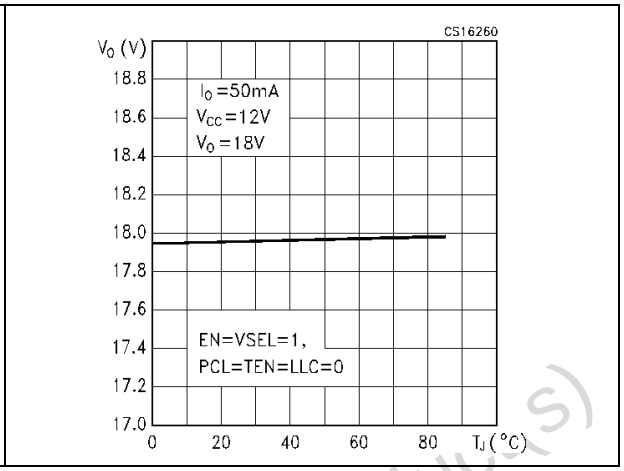



**Figure 11. Output voltage vs. temperature**

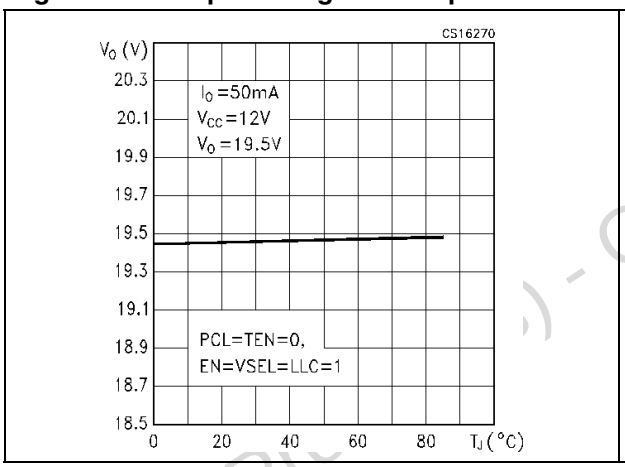



**Figure 12. Load regulation vs. temperature**

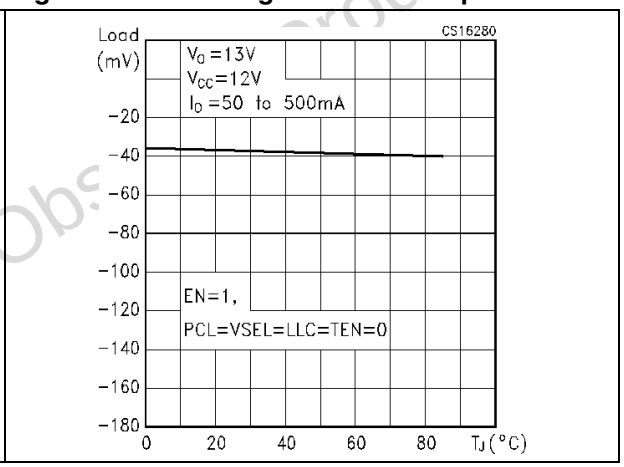



**Figure 13. Load regulation vs. temperature**

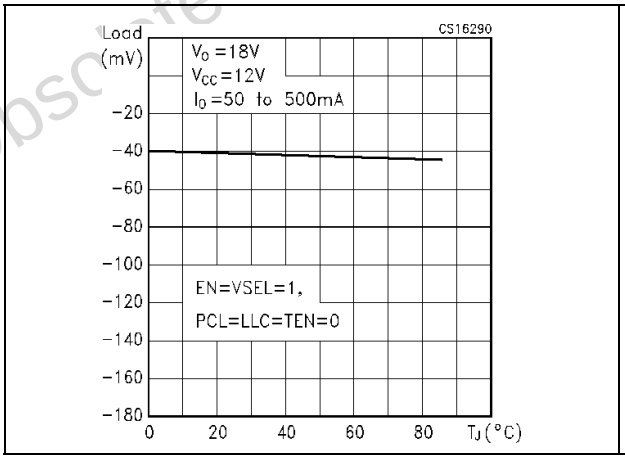
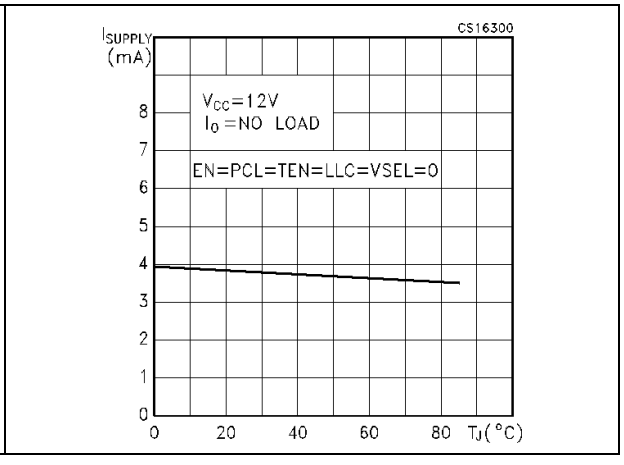



**Figure 14. Supply current vs. temperature**




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**Figure 15. Supply current vs. temperature**

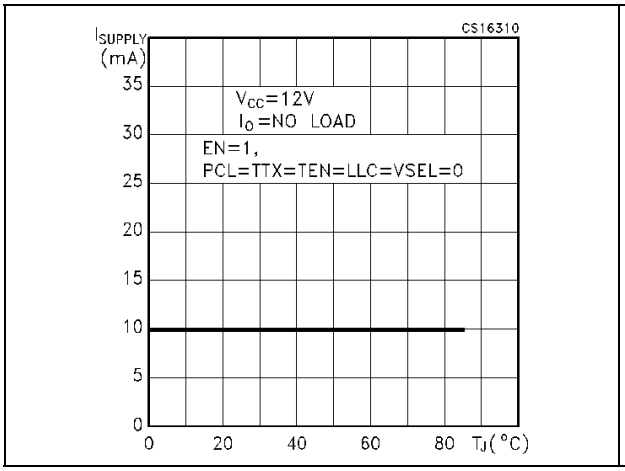



**Figure 16. Supply current vs. temperature**

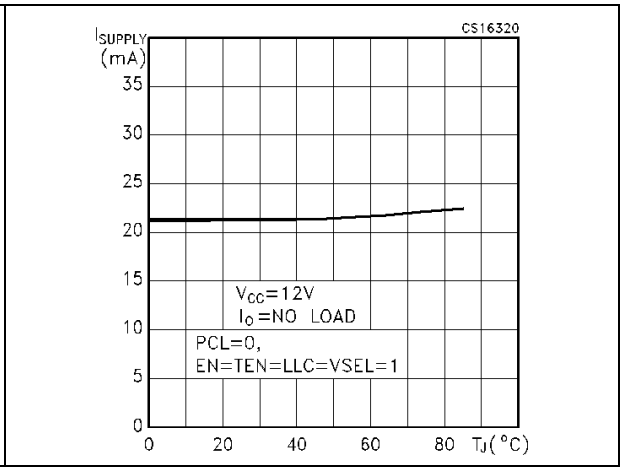



**Figure 17. Dynamic overload protection ON time vs. temperature**

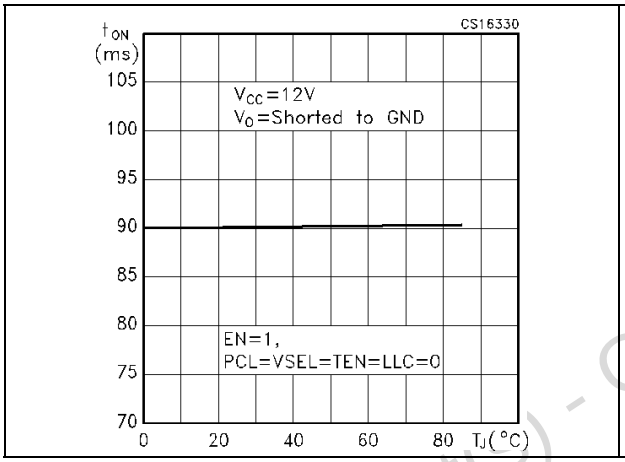



**Figure 18. Dynamic overload protection OFF time vs. temperature**

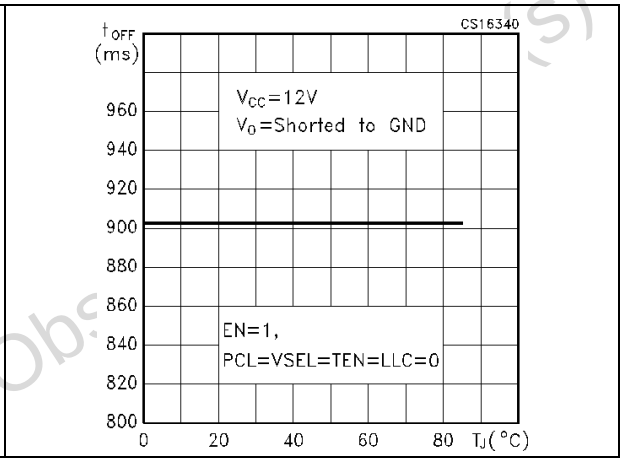



**Figure 19. Output current limiting vs. temperature**

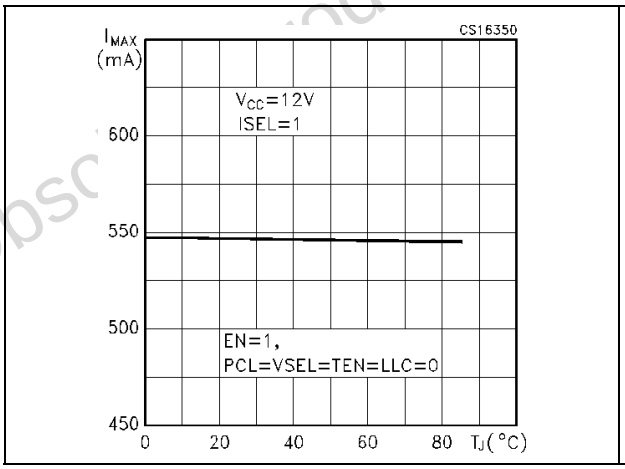
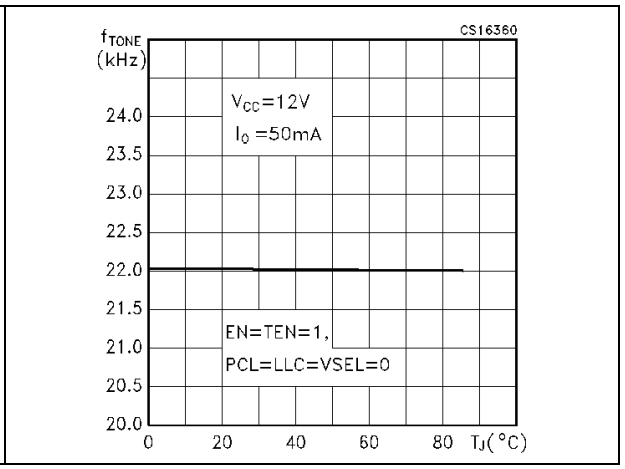



**Figure 20. Tone frequency vs. temperature**




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**Figure 21. Tone amplitude vs. temperature**

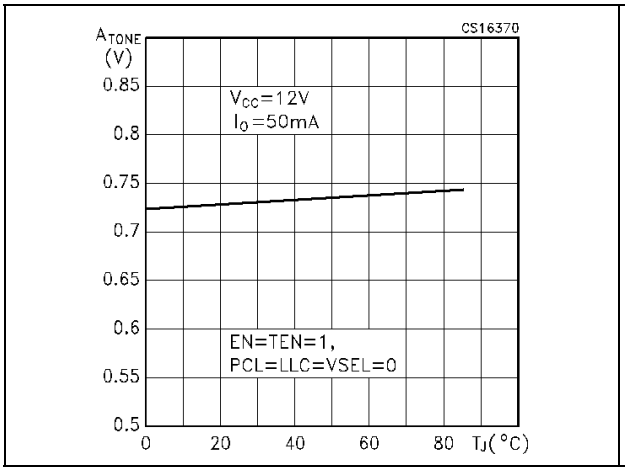



**Figure 22. Tone duty cycle vs. temperature**

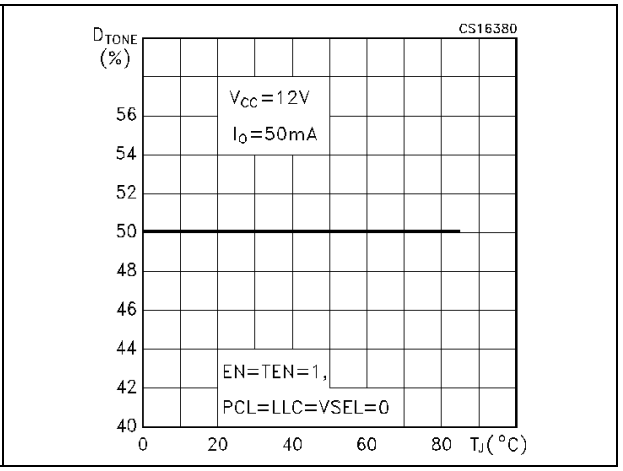



**Figure 23. Tone rise time vs. temperature**

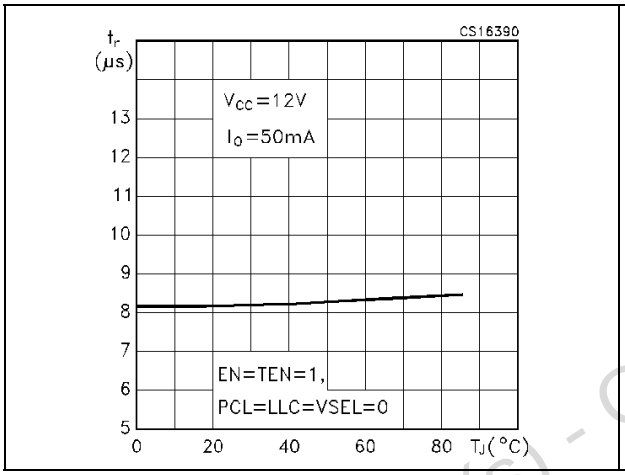



**Figure 24. Tone fall time vs. temperature**

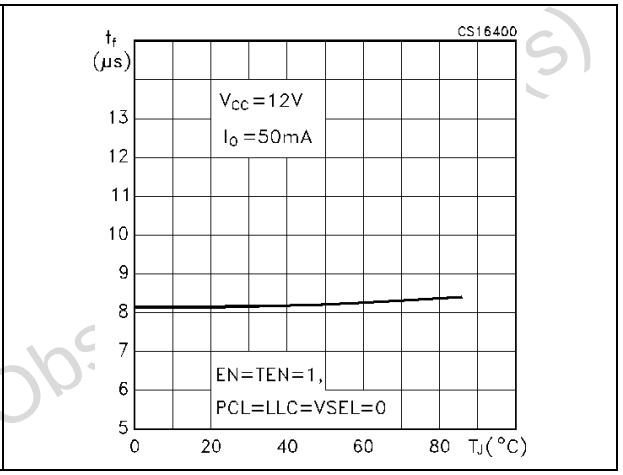



**Figure 25. Under voltage lockout threshold vs. temperature**

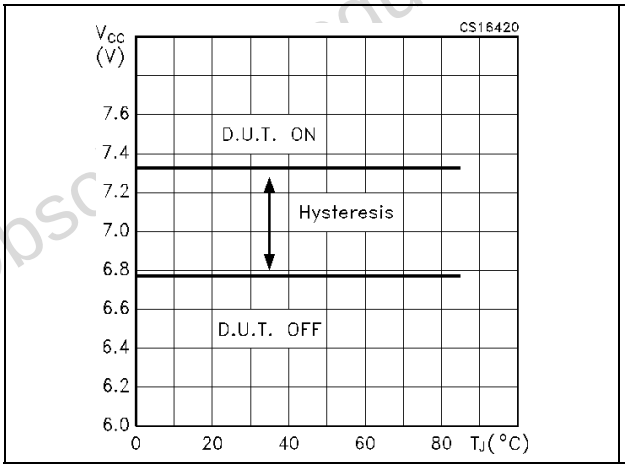



**Figure 26. Output backward current vs. temperature**

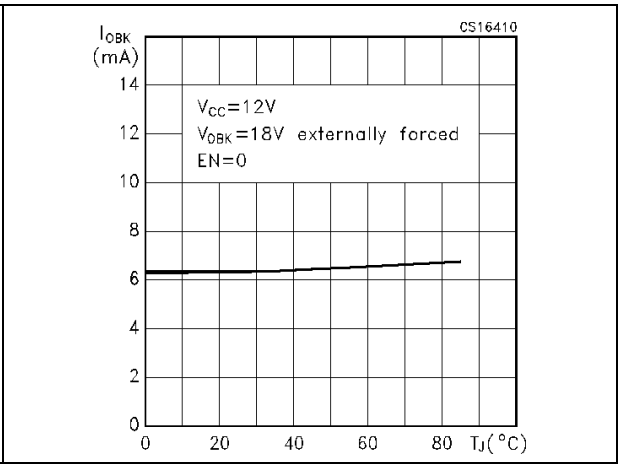


**Figure 27. DC-DC converter efficiency vs. temperature**

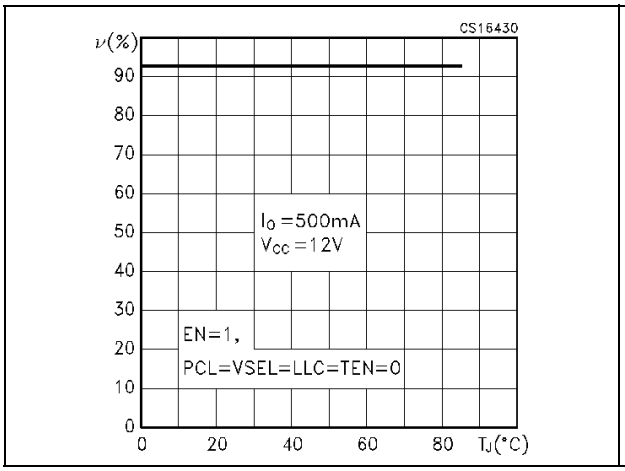



**Figure 28. Current limit sense voltage vs. temperature**

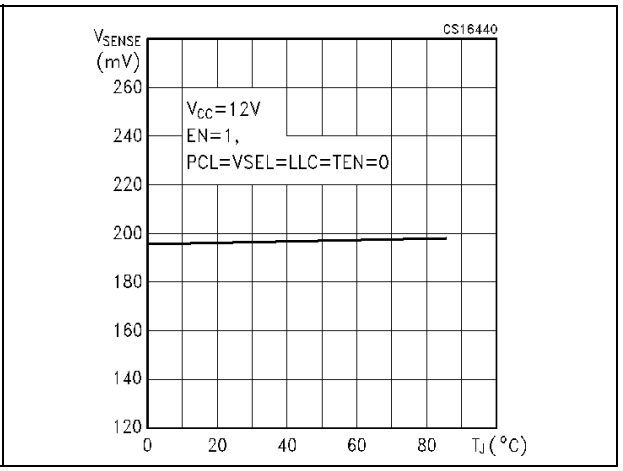
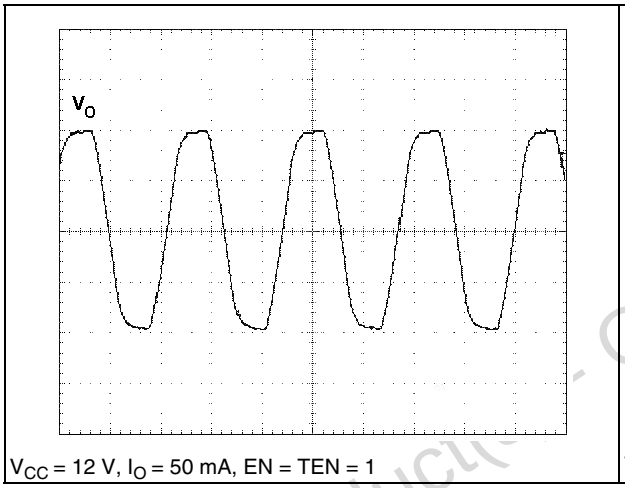
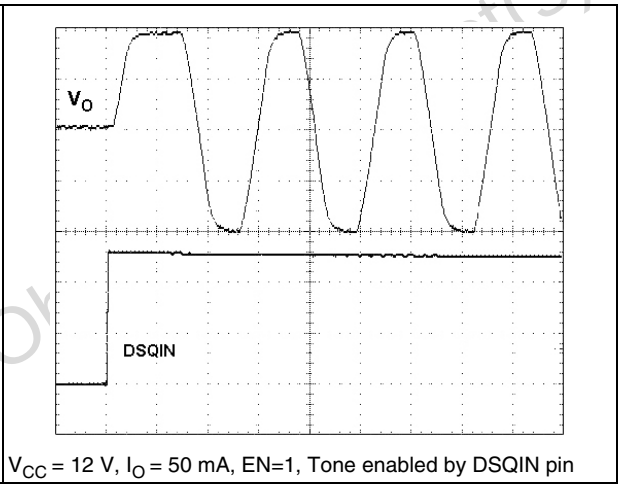



**Figure 29. 22 kHz tone waveform**



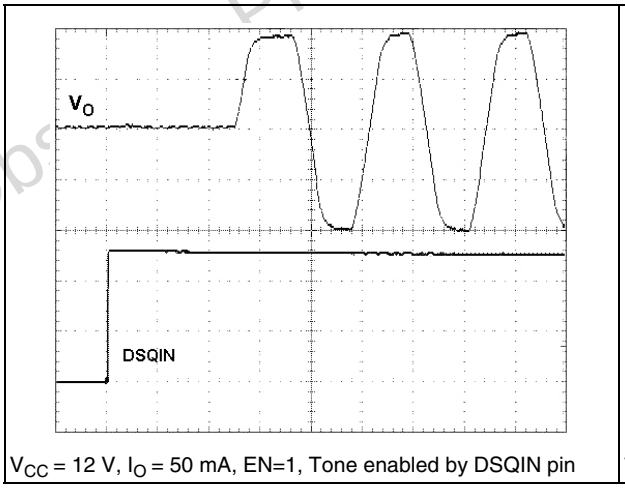

$V_{CC}$ = 12 V, $I_O$ = 50 mA, EN = TEN = 1

**Figure 30. DSQIN tone enable transient response**



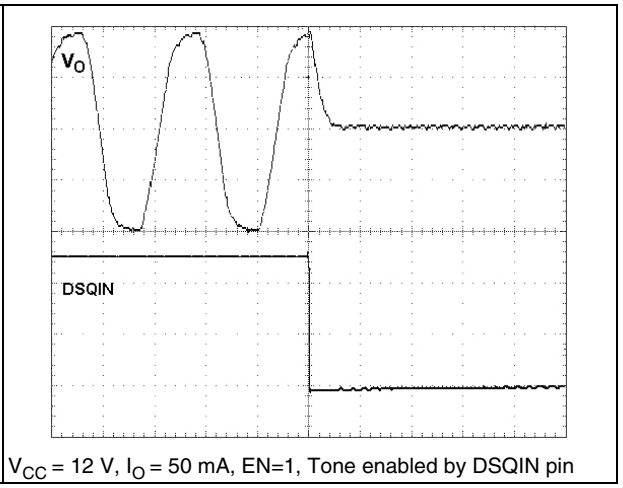

$V_{CC}$ = 12 V, $I_O$ = 50 mA, EN=1, Tone enabled by DSQIN pin

**Figure 31. DSQIN tone enable transient response**




$V_{CC}$ = 12 V, $I_O$ = 50 mA, EN=1, Tone enabled by DSQIN pin

**Figure 32. DSQIN tone disable transient response**




$V_{CC}$ = 12 V, $I_O$ = 50 mA, EN=1, Tone enabled by DSQIN pin

# 10 Package mechanical data

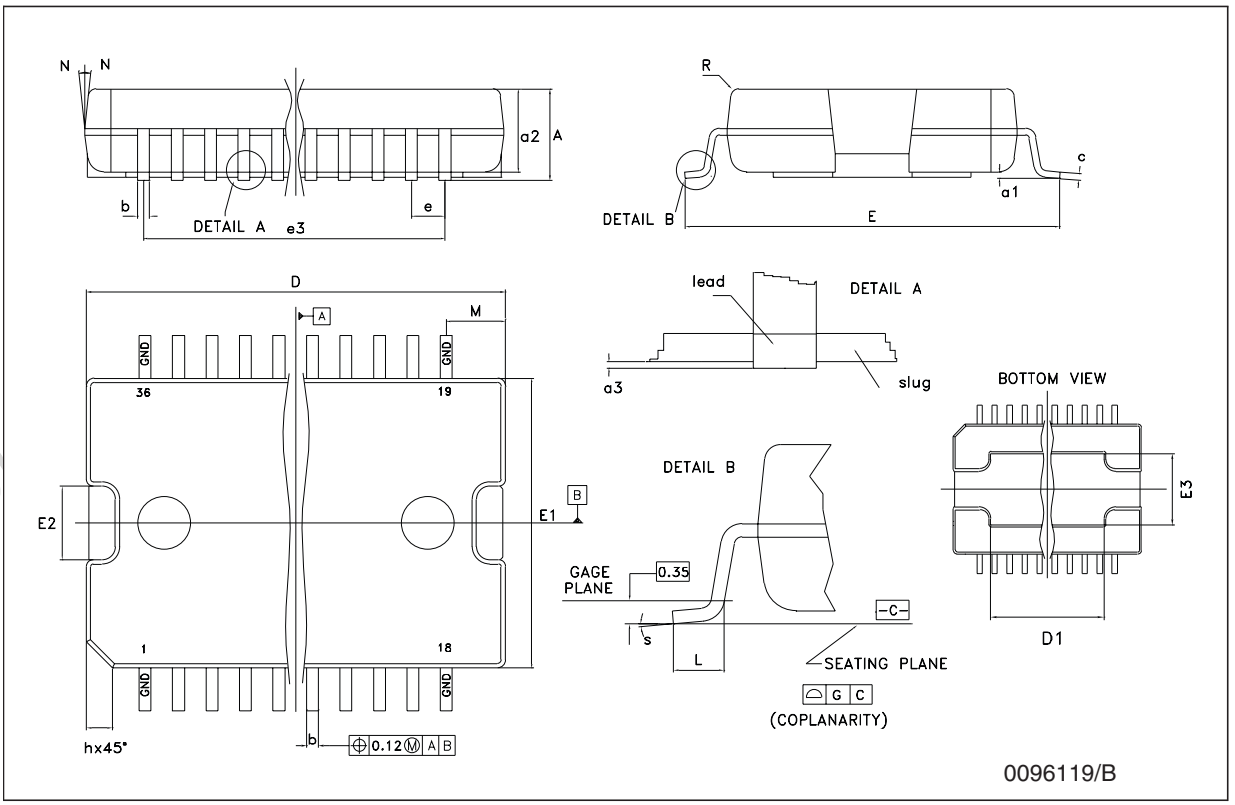
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## PowerSO-36 mechanical data

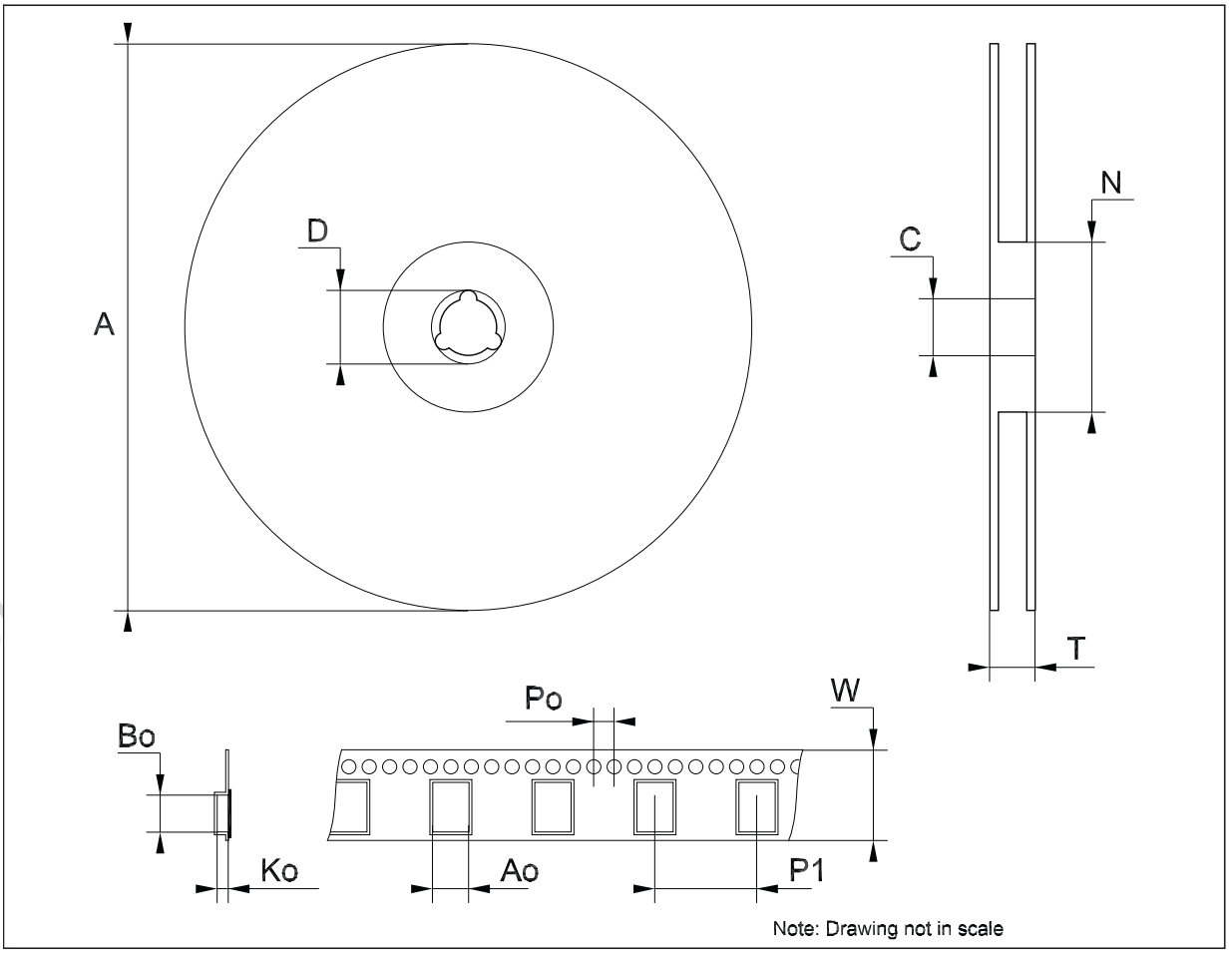
| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 3.60 | | | 0.1417 |
| a1 | 0.10 | | 0.30 | 0.0039 | | 0.0118 |
| a2 | | | 3.30 | | | 0.1299 |
| a3 | 0 | | 0.10 | 0 | | 0.0039 |
| b | 0.22 | | 0.38 | 0.0087 | | 0.0150 |
| c | 0.23 | | 0.32 | 0.0091 | | 0.0126 |
| D (1) | 15.80 | | 16.00 | 0.6220 | | 0.6299 |
| D1 | 9.40 | | 9.80 | 0.3701 | | 0.3858 |
| E | 13.90 | | 14.50 | 0.5472 | | 0.5709 |
| E1 (1) | 10.90 | | 11.10 | 0.4291 | | 0.4370 |
| E2 | | | 2.90 | | | 0.1142 |
| E3 | 5.8 | | 6.2 | 0.2283 | | 0.2441 |
| e | | 0.65 | | | 0.0256 | |
| e3 | | 11.05 | | | 0.4350 | |
| G | 0 | | 0.10 | 0.0000 | | 0.0039 |
| H | 15.50 | | 15.90 | 0.6102 | | 0.6260 |
| h | | | 1.10 | | | 0.0433 |
| L | 0.80 | | 1.10 | 0.0315 | | 0.0433 |
| N | | | 10° | | | 10° |
| S | 0° | | 8° | 0° | | 8° |

(1) “D and E1” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15 mm (0.006”)



## Tape and reel PowerSO-36 mechanical data

| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.197 |
| Ao | 15.1 | | 15.3 | 0.594 | | 0.602 |
| Bo | 16.5 | | 16.7 | 0.650 | | 0.658 |
| Ko | 3.8 | | 4.0 | 0.149 | | 0.157 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 23.9 | | 24.1 | 0.941 | | 0.949 |
| W | 23.7 | | 24.3 | 0.933 | | 0.957 |




Note: Drawing not in scale

# 11 Revision history

**Table 10. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 08-Apr-2005 | 4 | Maturity changed. |
| 01-Mar-2006 | 5 | The *Figure 3* and *Figure 4* updated. |
| 17-Apr-2009 | 6 | Updated statement ECOPACK®. |

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