THE DATASHEET OF

F2910NBGP8

Description

The F2910 is a high reliability, low insertion loss, 50Ω absorptive SPST RF switch designed for a multitude of wireless and RF applications. This device covers a broad frequency range from 30MHz to 8000MHz. In addition to providing low insertion loss, the F2910 also delivers excellent linearity and isolation performance while providing a 50Ω termination on RF2 in the isolation mode. The F2910 includes a patent pending constant impedance $K_{|Z|}$ feature for the RF2 port. $K_{|Z|}$ maintains near constant impedance when switching RF ports and improves hot switching ruggedness. $K_{|Z|}$ minimizes VSWR transients and reduces phase and amplitude variations when switching.

The F2910 uses a single positive supply voltage supporting either 3.3V or 1.8V control logic.

Competitive Advantage

The F2910 provides constant impedance for one RF port during transitions, improving a system's hot-switching ruggedness. The device also supports high power handling and high isolation.

- Constant impedance $K_{|Z|}$ during switching transition
- Low insertion loss
- High isolation
- Excellent linearity
- Extended temperature range: -55°C to +105°C

Typical Applications

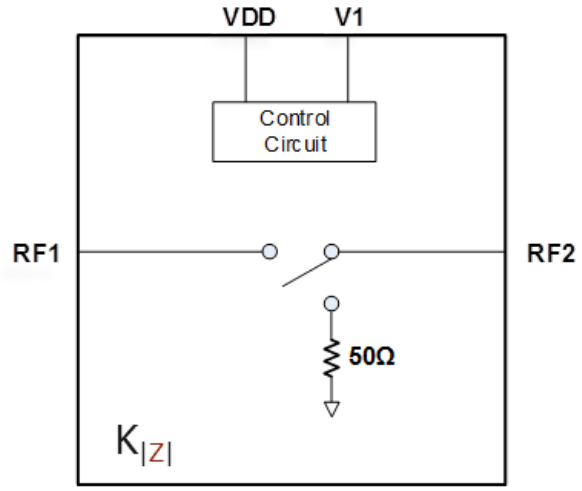
- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

Features

- Insertion Loss
  - ✓ 0.55dB at 2GHz
- High Isolation
  - ✓ 51dB at 2GHz
- High Linearity
  - ✓ IIP3 of 65dBm
- Wide Single Positive Supply Voltage Range
- 3.3V and 1.8V compatible control logic
- Operating temperature -55°C to +105°C
- 2 x 2 mm 8-DFN package

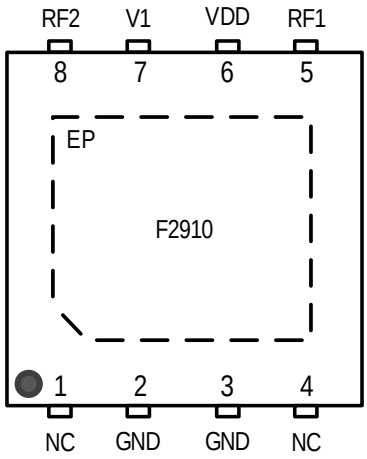
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2 mm x 2 mm x 0.9 mm 8-VFQFP-N – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 4	NC	This pin may be connected to the paddle and can be grounded.
2, 3	GND	Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible.
5	RF1	RF1 Port. Matched to 50 Ω in the insertion loss state only. If this pin is not 0 V DC, then an external coupling capacitor must be used.
6	V_{DD}	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
7	V1	Logic control pin. See Table 6 for proper logic setting.
8	RF2	RF2 Port. Matched to 50 Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

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Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{DD} to GND	V_{DD}	-0.3	+6.0	V
V1 to GND	V_{Logic}	-0.3	Lower of (V_{DD} + 0.3V, 3.6V)	V
RF1, RF2 to GND	V_{RF}	-0.3	+0.3	V
RF Input Power Port 1 or 2. Other port terminated into 50 Ω [a]	P_{RF12}		33	dBm
RF Input Power Port 1 in isolation. Port 2 terminated into 50 Ω [a]	P_{RF1_ISO}		23	
RF Input Power Port 2 in isolation. Port 1 terminated into 50 Ω [a]	P_{RF2_ISO}		30	
Maximum Junction Temperature	T_{jmax}		+140	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		1000 (Class C3)	V

a. V_{DD} = 2.7 V to 5.5 V, 30 MHz ≤ F_{RF} ≤ 8000 MHz, T_c = 105°C, Z_S = Z_L = 50 ohms.

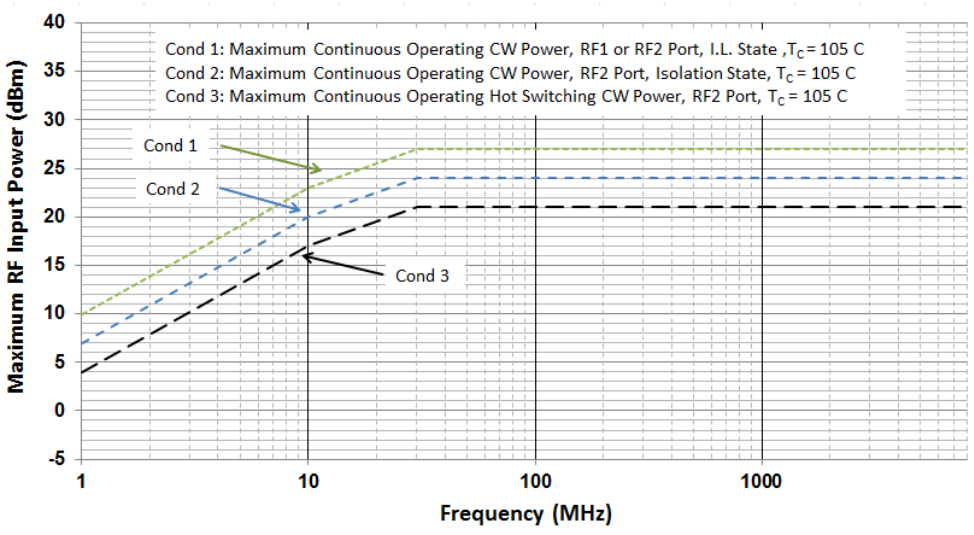
Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Power supply voltage	V_{DD}			2.7		5.5	V
Logic Input High Threshold	V_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		***1.1*** [a]		Lower of (V_{DD}, 3.6)	V
Logic Input Low Threshold	V_{IL}			-0.3 [b]		0.6	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature		-55		+105	°C
RF Frequency Range	F_{RF}			30		8000 [c]	MHz
RF Continuous Input CW Power (Non-Switched) [d]	P_{RF}	RF1 or RF2 as the input (Insertion loss state)	T_c = 85 ºC			30	dBm
			T_c = 105 ºC			27	
		RF1 as the input (Isolation state)	T_c = 85 ºC			20	
			T_c = 105 ºC			17	
		RF2 as the input (Isolation state)	T_c = 85 ºC			27	
			T_c = 105 ºC			24	
RF Continuous Input Power (RF Hot Switching CW) [d]	P_{RFSW}	Applied to RF2 input switching between Insertion loss to Isolation states	T_c = 85 ºC			24	dBm
			T_c = 105 ºC			21	
RF1/2 Port Impedance	Z_{RFx}	Insertion loss state			50		Ω
RF2 Port Impedance	Z_{RFx}	Isolation state			50		Ω

a. Items in min/max columns in ***bold italics*** are Guaranteed by Test.
b. Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
c. To achieve best performance from 5 – 8 GHz, the use of bypass capacitors as described in the Applications Circuit section is required.tee
d. Levels based on: V_{DD} = 2.7 V to 5.5 V, 30 MHz ≤ F_{RF} ≤ 8000 MHz, Z_S = Z_L = 50 ohms. See Figure 3 for power handling derating vs RF frequency.

Figure 3. Maximum RF Input Operating Power vs. RF Frequency



Electrical Characteristics

Table 4. Electrical Characteristics

Typical Application Circuit: V_{DD} = 3.3 V, T_{CASE} = +25 °C, F_{RF} = 2 GHz, Driven Port = RF2, Input power = 0 dBm, Z_S = Z_L = 50 Ω. PCB board trace and connector losses are de-embedded unless otherwise noted. IIP2 / IIP3: P_{IN} = 13 dBm / tone, 50 MHz spacing. Performance beyond 5 GHz based on application circuit (Figure 20) using best RF PCB design practices. See note c for details.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Current	I_{IH}, I_{IL}		*-1*		*+1*	µA
DC Current	I_{DD}	V_{DD} =3.3 V		190	*304* [a]	µA
		V_{DD} =5.0 V		220	*374*	
Insertion Loss	IL	0.03 GHz		0.38		dB
		0.35 GHz		0.44		
		1.0 GHz		0.50	0.70 [b]	
		2.0 GHz		0.55	*0.80*	
		3.0 GHz		0.60	0.85	
		4.0 GHz		0.67	0.90	
		5.0 GHz		0.75	1.00	
		6.0 GHz		0.80 [c]		
		7.0 GHz		1.00 [c]		
		8.0 GHz		1.55 [c]		
Isolation	ISO	0.03 GHz		85		dB
		0.35 GHz	66	73		
		1.0 GHz	55	61		
		2.0 GHz	45	51		
		3.0 GHz	40	46		
		4.0 GHz	35	41		
		5.0 GHz	30	37		
		6.0 GHz		33 [c]		
		7.0 GHz		29 [c]		
		8.0 GHz		26 [c]		
Max RF2 Port VSWR During Switching	VSWR	Insertion Loss to Isolation		3.3:1		
		Isolation to Insertion Loss		2.0:1		
RF1, RF2 Return Loss (Insertion Loss State)	RF_{RL}	2.0 GHz		27		dB
		3.0 GHz		25		
		4.0 GHz		20		
		5.0 GHz		18		
		6.0 GHz		20 [c]		
		7.0 GHz		25 [c]		
		8.0 GHz		13 [c]		

a. Items in min/max columns in ***bold italics*** are Guaranteed by Test.
b. Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
c. To achieve performance beyond 5 GHz, the use of bypass capacitors (BOM C2, C3, and C5) installed close to the device as embodied in the evaluation board per the application circuit (Figure 20) is required. See the appropriate Typical Operating Conditions graphs.

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Electrical Characteristics (Cont.)

Typical Application Circuit: V_{DD} = 3.3 V, T_{CASE} = +25 °C, F_{RF} = 2 GHz, Driven Port = RF2, Input power = 0 dBm, Z_S = Z_L = 50 Ω. PCB board trace and connector losses are de-embedded unless otherwise noted. IIP2 / IIP3: P_{IN} = 13 dBm / tone, 50 MHz spacing. Performance beyond 5 GHz based on application circuit (Figure 20) using best RF PCB design practices. See note c for details.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
RF2 Return Loss (Isolation State)	RF_{RLT}	2.0 GHz			27		dB
		3.0 GHz			27		
		4.0 GHz			25		
		5.0 GHz			20		
		6.0 GHz			15 [c]		
		7.0 GHz			12 [c]		
		8.0 GHz			10 [c]		
Input 1dB Compression [d]	ICP_{1dB}	0.03 GHz			34		dBm
		3.0 GHz			35		
		4.0 GHz			35		
Input 0.1dB Compression [d]	$ICP_{0.1dB}$	0.03 GHz			33		dBm
		3.0 GHz			34		
		4.0 GHz			34		
Input IP2 [e]	IIP2	F1 = 0.35 GHz, F2 = 0.40 GHz			123		dBm
		F1 = 0.95 GHz, F2 = 1.00 GHz			124		
		F1 = 2.40 GHz, F2 = 2.45 GHz			118		
Input IP3 [e]	IIP3	0.03 GHz			65		dBm
		0.35 GHz			65		
		1.00 GHz			68		
		2.40 GHz			67		
Non-RF Driven Spurious [f]	$Spur_{MAX}$	Any port when externally terminated into 50 Ω			-102		dBm
Switching Time [g]	T_{SW}	50% control to 90% RF			265	500	ns
		50% control to 10% RF			225	500	
		50% control to RF settled to within +/- 0.1 dB of insertion loss value			280		
Maximum Switching Rate	SW_{RATE}				25		kHz
Maximum Video Feed-through on RF Ports	VID_{FT}	Peak transients during switching. Measured with 20 ns rise-time, 0 to 3.3 V control pulse	Rise Time		25		mVpp
			Fall Time		45		

a. Items in min/max columns in ***bold italics*** are Guaranteed by Test.
b. Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
c. To achieve performance beyond 5 GHz, the use of bypass capacitors (BOM C2, C3, and C5) installed close to the device as embodied in the evaluation board per the application circuit (Figure 20) is required. See the appropriate Typical Operating Conditions graphs.
d. The input 0.1 and 1 dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
e. RF1 or RF2 driven IIP2 / IIP3 results when in insertion loss state. IP2 Frequency = F1 + F2.
f. Spurious due to on-chip negative voltage generator. Spurious fundamental is approximately 5.7 MHz.
g. F_{RF} = 1 GHz.

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Thermal Characteristics

Table 5. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	159.5	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC}	15.1	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted:

- V_{DD} = 3.3 V.
- $Z_L = Z_S$ = 50 Ohms Single Ended.
- F_{RF} = 2 GHz.
- P_{IN} = 13 dBm / tone applied to RF2 port for two tone linearity tests.
- Two tone frequency spacing = 50 MHz.
- All temperatures are referenced to the exposed paddle.
- Evaluation Kit traces and connector losses are de-embedded.
- Performance beyond 5 GHz as listed in the Electrical Characteristics is based on the application circuit (Figure 20) with bypass capacitors (BOM C2, C3, and C5) installed. The capacitors must be installed in close proximity to the device as embodied in the evaluation board with best practices followed for PCB design. Performance above 5 GHz de-rated as shown in Typical Performance Characteristics plots Figure 10 to Figure 13 when application circuit with bypass capacitors is not utilized.
- Unless otherwise noted, C2, C3 and C5 are installed in following plots.

Typical Performance Characteristics

Figure 4. Insertion Loss vs. Frequency over Temperature

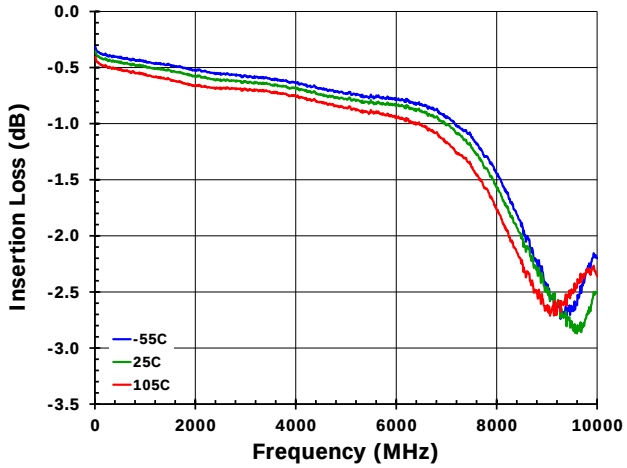


Figure 5. Isolation vs. Frequency over Temperature

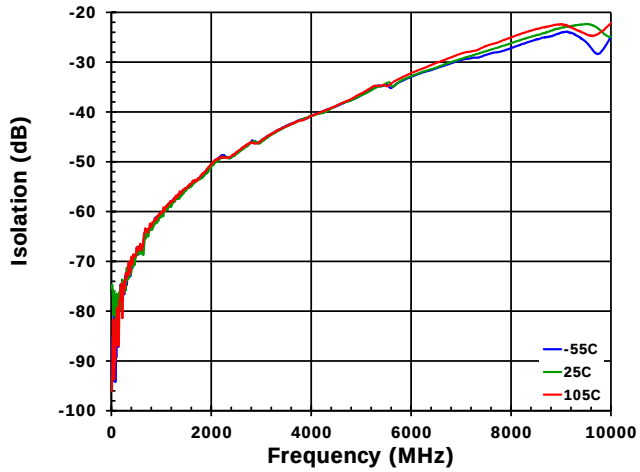


Figure 6. Return Loss vs. Frequency over Temp [RF1 Insertion Loss State]

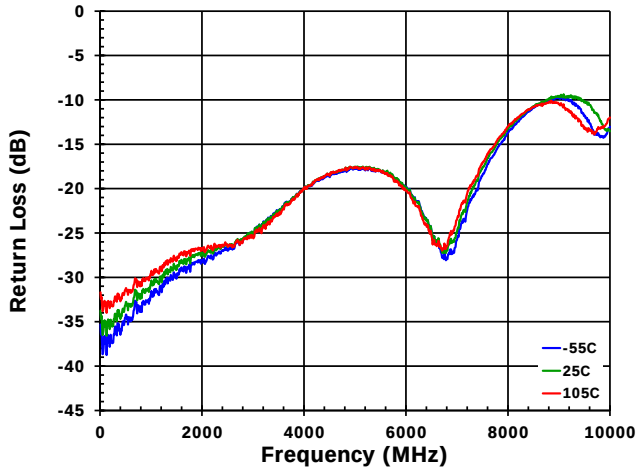


Figure 7. Return Loss vs. Frequency over Temp [RF2 Insertion Loss State]

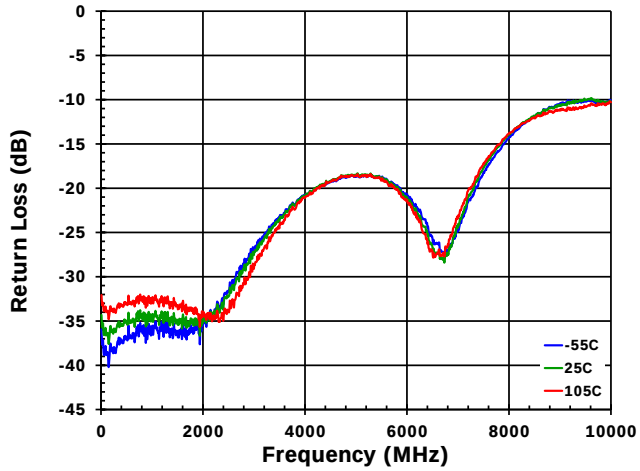


Figure 8. Return Loss vs. Frequency over Temperature [RF2 Terminated State]

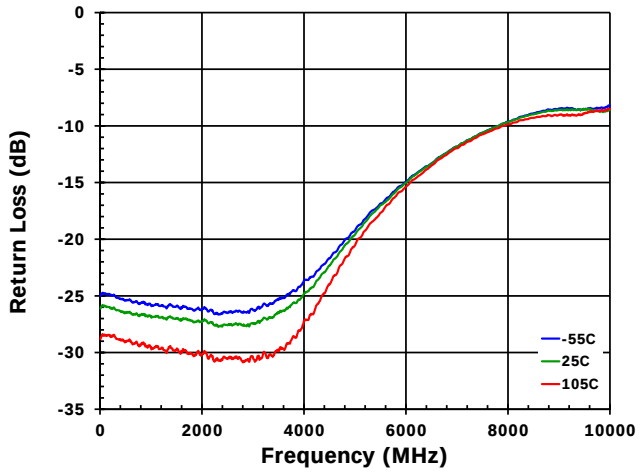


Figure 9. Evaluation Board Loss vs. Frequency

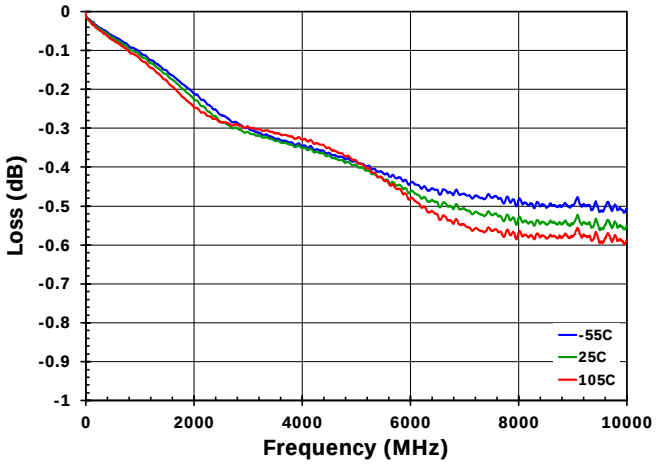


Figure 10. Insertion Loss vs. Frequency With and Without Capacitors

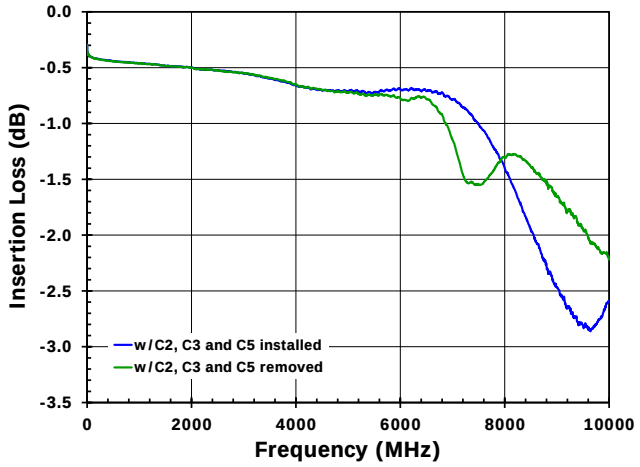


Figure 11. Isolation vs. Frequency With and Without Capacitors

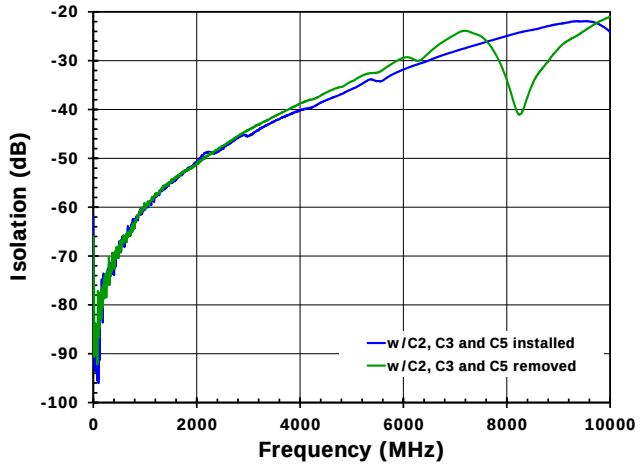


Figure 12. Return Loss vs. Frequency With and Without Capacitors

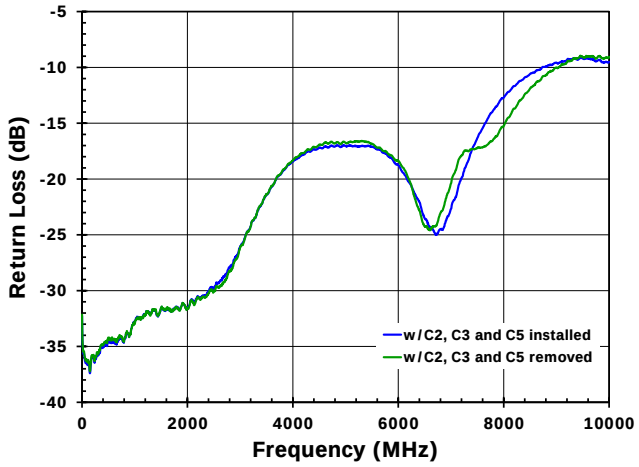


Figure 13. Return Loss vs. Frequency With and Without Capacitors [State 0]

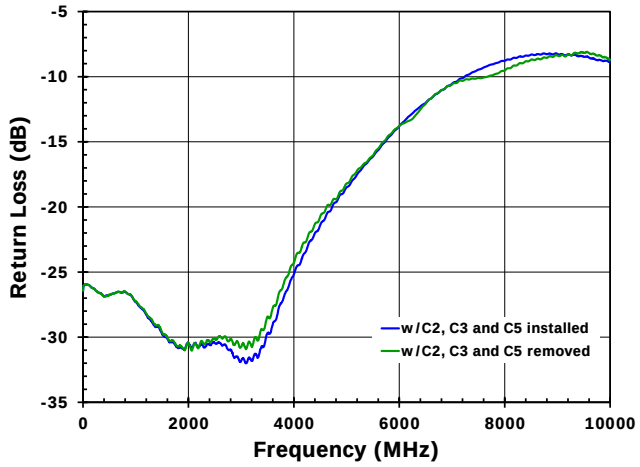


Figure 14. Input IP3 vs. Frequency

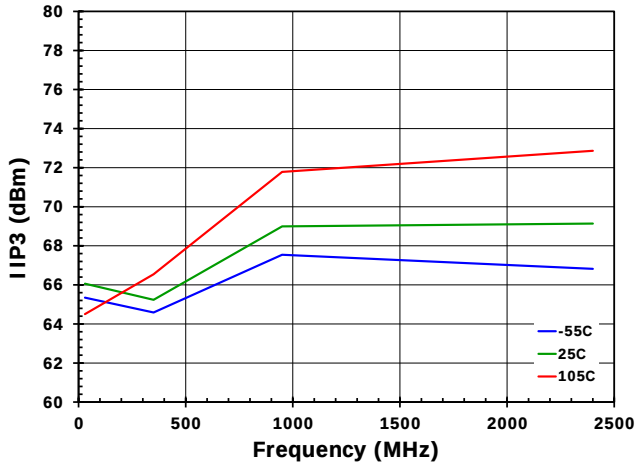


Figure 15. 1 dB Compression at 3 GHz

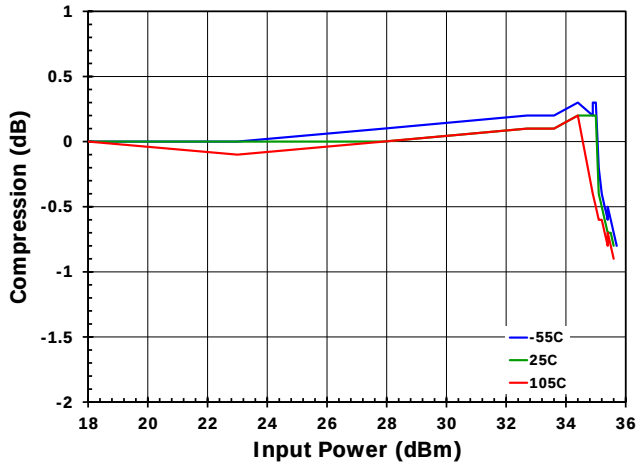


Figure 16. Switching Time Isolation to Insertion loss

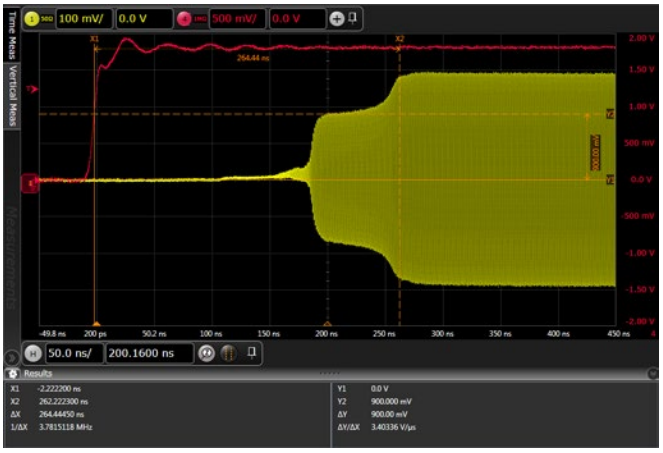


Figure 17. Switching Time Insertion Loss to Isolation



Evaluation Kit Picture

Figure 18. Top View

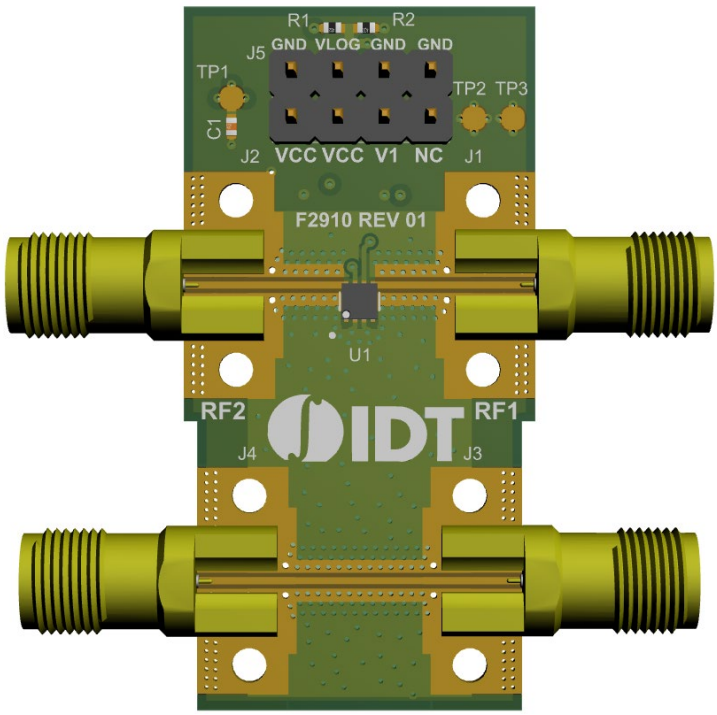
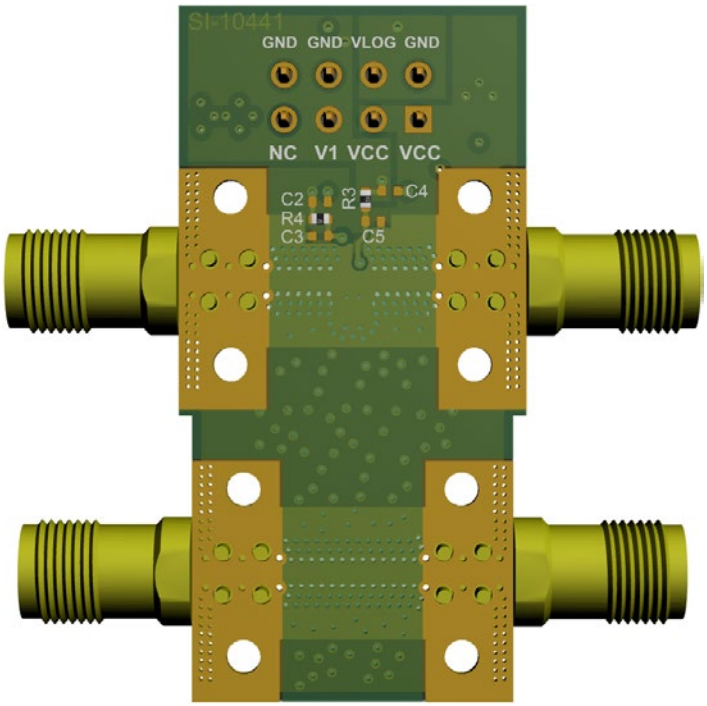


Figure 19. Bottom View



Control Mode

Table 6. Switch Control Truth Table

V1 (Logic)	State	Port Match
0	Isolation	RF1 port reflective, RF2 port terminated into 50 ohms
1	Insertion Loss	RF1 and RF2 port matched to 50 ohm

Evaluation Kit / Applications Circuit

Figure 20. Electrical Schematic

Note: The use of bypass capacitors C2, C3, and C5 as listed in the BOM (Table 7) is required to achieve performance as listed in the Electrical Characteristics for frequencies beyond 5 GHz. The capacitors must be installed in close proximity to the device as embodied in the evaluation board with best practices followed for PCB design.

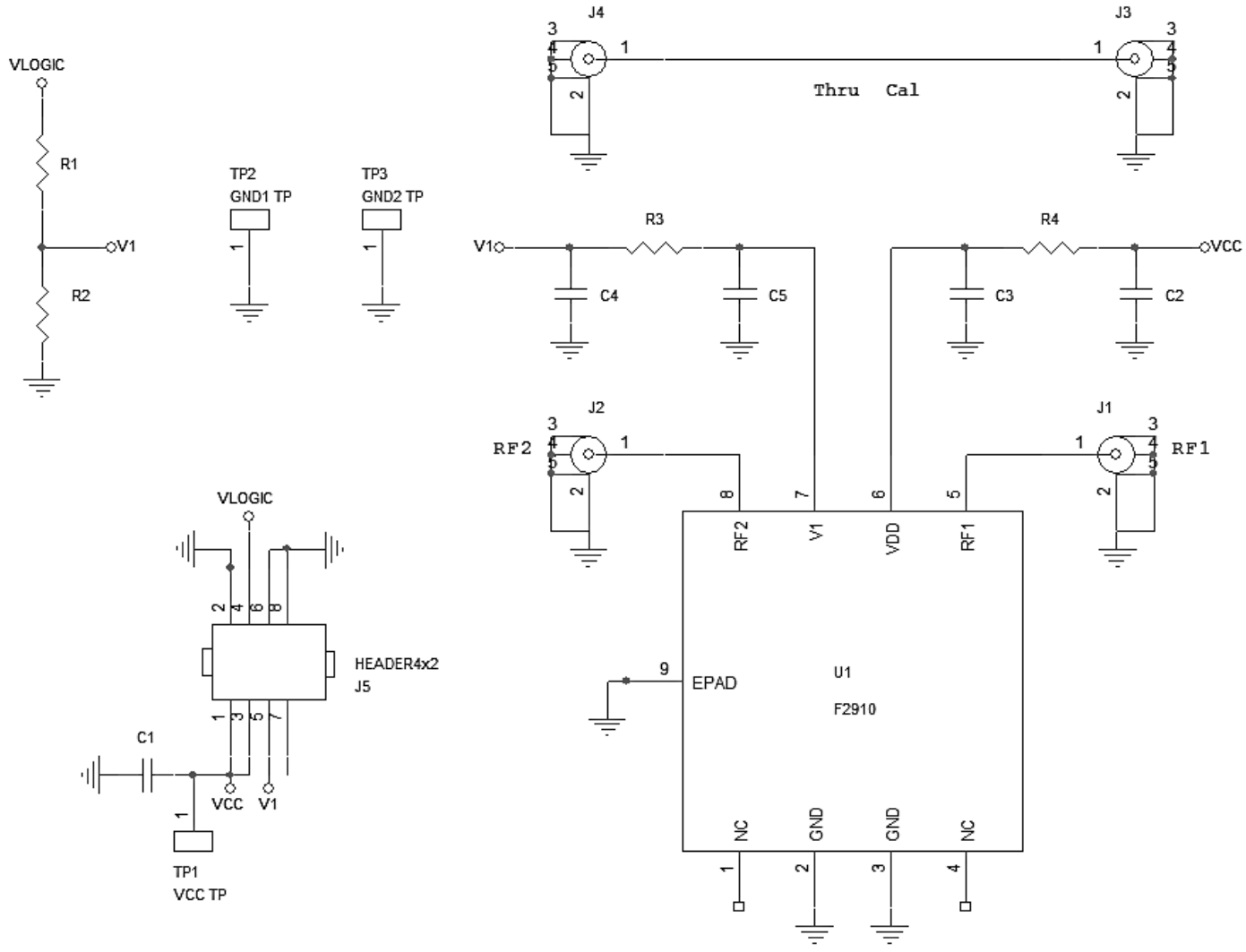


Table 7. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1 µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2	1	0.5 pF ±0.1 pF, 50V, C0G, Ceramic Capacitor (0402)	GJM1555C1HR50BB01	Murata
C3	1	4.5 pF ±0.1 pF, 50V, C0G, Ceramic Capacitor (0402)	GJM1555C1H4R5BB01D	Murata
C4	0	Not Installed (0402)		
C5	1	4.9 pF ±0.1 pF, 50V, C0G, Ceramic Capacitor (0402)	GJM1555C1H4R9BB01	Murata
R1	1	15k Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R2	1	18k Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1802X	Panasonic
R3, R4	2	0 Ω 1/10W, Jumper (0402)	ERJ-2GE0R00X	Panasonic
J1 – J4	4	SMA Edge Mount	142-0761-881	Cinch Connectivity
J5	1	CONN HEADER VERT 4x2 POS GOLD	67997-108HLF	Amphenol FCI
TP1	0	Not Installed (Red Test Point Loop)		
TP2, TP3	0	Not Installed (Black Test Point Loop)		
U1	1	SPST Switch 2 mm x 2 mm 8 pin DFN	F2910NBGP/W	IDT
	1	Printed Circuit Board	F2910 EVKIT REV 01	IDT

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Evaluation Kit Operation

Default Start-up

Control pins include no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

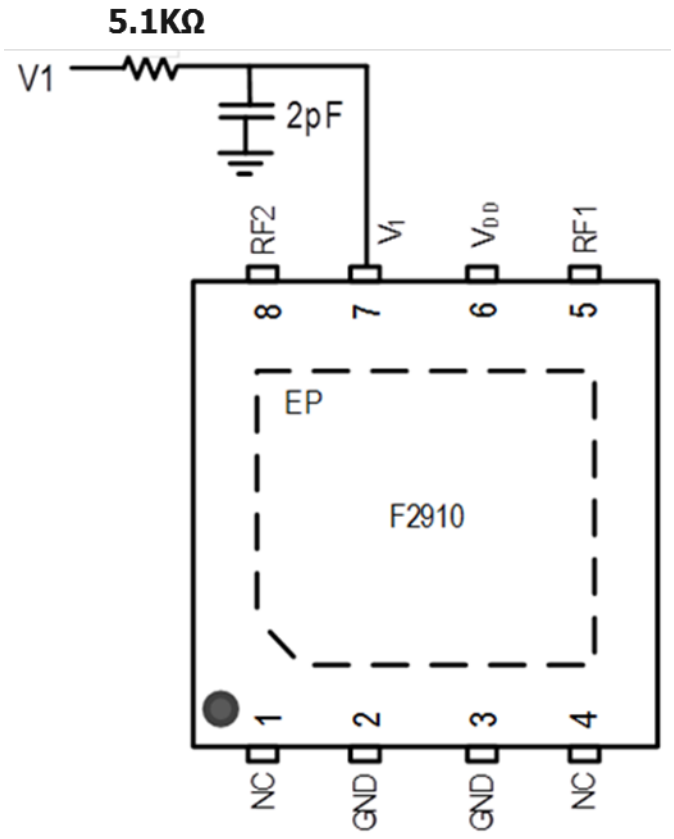
Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µs. In addition, all control pins should remain at 0 V (± 0.3 V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pin 7 as shown in Figure 21. If bypass capacitor C5 as described in the application circuit (Figure 20) is used to achieve high frequency performance optimization, the use of an additional 2 pF capacitor as shown in Figure 21 is not necessary.

Figure 21. Control Pin signal integrity improvement circuit



External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.7 V to 5.5 V with the power supply output disabled.

Logic Control Setup

Using the EVKIT to manually set the control logic:

On connector J5, connect a 2-pin shunt from V_{CC} (pin 3) to V_{LOGIC} (pin 4). This connection provides the V_{CC} voltage supply to the Eval Board logic control pull-up network. Resistors R1 and R2 form a voltage divider to set the V_{IH} level over the 2.7 V to 5.5 V V_{CC} range for manual logic control.

Connector J5 has one logic input pin: V1 (pin 5). See Table 6 for Logic Truth Table. With the pull-up network enabled (as noted above) this pin can be left open to provide a logic high through pull-up resistor R1. To set a logic low for V1, connect a 2-pin shunt on J5 from V_{CTL} (pin 5) to GND (pin 6).

Note that when using the on board R1/R2 voltage divider, the current draw from the V_{CC} supply will be higher by approximately V_{CC} / 33 kΩ.

Using external control logic:

Pins 3, 4, 6, 7, and 8 of J5 should have no external connections. External logic control is applied to J5 V1 (pin 5). See Table 5 for the Logic Truth Table.

Turn On Procedure

Setup the supplies and EVKIT as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V_{CC} Supply

Set the desired logic setting to achieve the desired Table 5 configuration. Note that external control logic should not be applied without V_{CC} being present.

Turn Off Procedure

Set the logic control to a logic low.
Disable the V_{CC} supply.

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Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/8-dfn-package-outline-drawing-20-x-20-x-09-mm-body-epad-08-x-16-mm-05mm-pitch-nbnbg8p3?language=en

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Orientation	Temperature
F2910NBGP	2 x 2 x 0.9 mm 8-VFQFP-N	MSL1	Bulk		-55° to +105°C
F2910NBGP8	2 x 2 x 0.9 mm 8-VFQFP-N	MSL1	Tape and Reel	EIA-481-C[a]	-55° to +105°C
F2910EVBI	Evaluation Board				

a. Contact IDT for additional information on tape and reel orientation

Marking Diagram



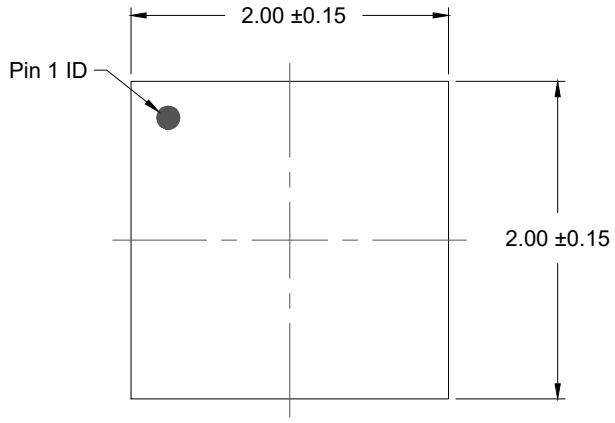
1. Line 1 is the part number.
2. Line 2 – “6” is last digit of the year.
3. Line 2 – “U” is the workweek code
4. Line 2 – AG is the sequential code

Revision History

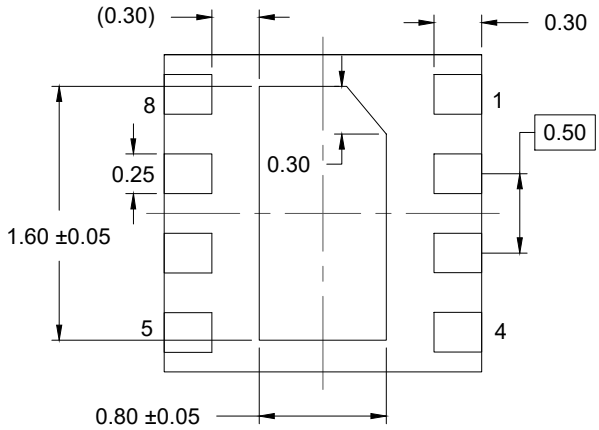
Revision Date	Description of Change
August 31, 2020	• Updated the package outline drawings; however, no mechanical changes
October 25, 2020	• Added orientation information and F2910NBGP/W part number.
August 29, 2016	Initial release.

Package Outline Drawing

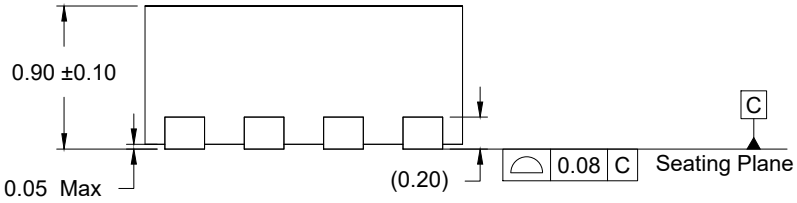
Package Code: NBG8P3
8-DFN 2.0 x 2.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4178-03, Revision: 02, Date Created: Aug 25, 2023



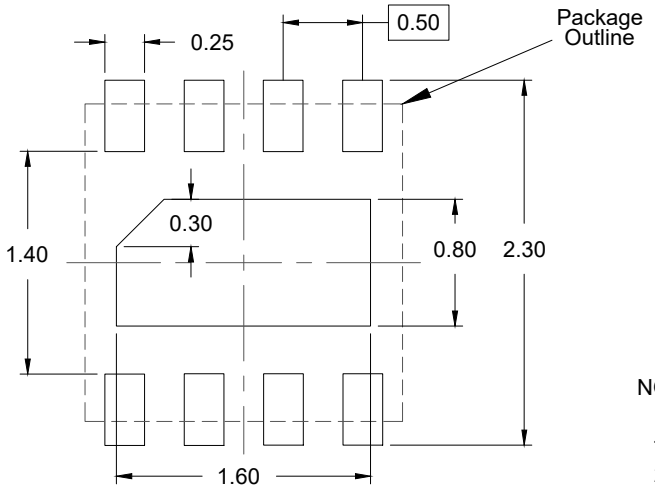
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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