THE DATASHEET OF

PE42447A-Z

www.win-source.net 0086-755-83957316

PE42447

Document Category: Product Specification

UltraCMOS© SP4T RF Switch, 10 MHz–8 GHz

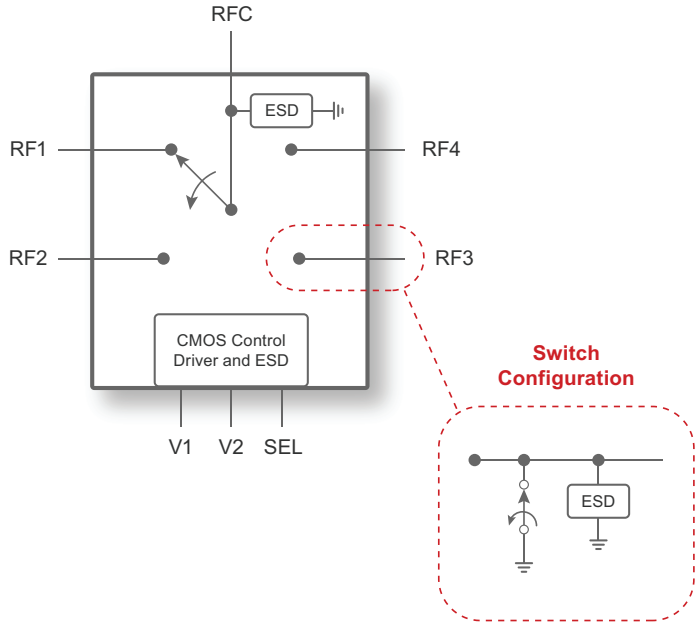
Features

- Low insertion loss:
  - 0.4 dB at 2.7 GHz typical
  - 0.48 dB at 3.8 GHz typical
- High linearity IIP3: 85 dBm
- High power handling: 40-dBm RMS, 50-dBm peak
- Operating temperature: +125 °C
- Packaging: 20-lead 4 × 4 mm LGA

Applications

- 5G massive MIMO active antenna system (AAS)
- 4G/4.5G TD-LTE macro/micro cell
- Automated test equipment (ATE)
- Land mobile radio (LMR)
- Genera-purpose switching

Figure 1 • PE42447 Functional Diagram



Product Description

The PE42447 is a HaRP™ technology-enhanced SP4T RF switch that supports a frequency range from 10 MHz to 8 GHz. It delivers extremely low insertion loss and high linearity with high input power handling capability making this device ideal for hybrid analog beamforming and in 5G massive MIMO (multi-input multi-output) applications. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42447 is manufactured on pSemi's UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology.

©2024–2025, pSemi Corporation. All rights reserved. • Headquarters: 9369 Carroll Park Drive, San Diego, CA, 92121

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** could cause permanent damage. Restrict operation to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • PE42447 Absolute Maximum Ratings

Parameter or Condition	Min	Max	Unit
Positive supply voltage, V_{DD}	-0.3	5.5	V
Digital input voltage	-0.3	3.6	V
RF input power, RMS	–	40	dBm
RF input power peak (LTE 10-MHz ETM1.1 carrier with 10-dB PAR)	–	50	dBm
RF input power, RMS (10s survivability)(1)	–	43.5	dBm
Storage temperature	-65	150	°C
ESD voltage HBM, all pins(2)	–	1000	V
ESD voltages, CDM, all pins(3)	–	1000	V

Notes:

1) The part was tested at 43.5-dBm average power/50.5-dBm peak power for two seconds with 100 exposures with a cool down period of five seconds between each exposure. This test was conducted at 115 °C T_{CASE}. Signal type: LTE TDD, ETM1.1 test model, 10-ms frame duration, 70% duty cycle.
2) Human body model (MIL-STD 883 Method 3015).
3) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the PE42447 recommending operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2 • PE42447 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Positive supply voltage, V_{DD}	4.5	5	5.50	V
Positive supply current, I_{DD}, at typical control voltage = 1.8V	–	65	200	µA
Control voltage high	1.17	–	3.6	V
Control voltage low	-0.30	–	0.6	V
Digital input leakage current	–	–	10	µA
Temperature range	-40	25	125	°C

Electrical Specifications

Table 3 lists the PE42447 key electrical specifications at +25 °C T_{CASE} and VDD = 5V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3 • PE42447 Electrical Specifications

Name	Description	Min	Typ	Max	Unit
Insertion loss	1800 MHz	–	0.32	0.36	dB
	2700 MHz	–	0.38	0.41	dB
	3800 MHz	–	0.48	0.53	dB
	4200 MHz	–	0.53	0.61	dB
	5000 MHz	–	0.62	0.68	dB
	6000 MHz	–	0.83	1.00	dB
	7000 MHz	–	1.02	1.27	dB
	8000 MHz	–	1.38	2.15	dB
Isolation	1800 MHz	37.6	38.0	–	dB
	2700 MHz	33.2	33.6	–	dB
	3800 MHz	29.1	29.7	–	dB
	4200 MHz	27.7	28.5	–	dB
	5000 MHz	25.3	25.9	–	dB
	6000 MHz	22.5	23.1	–	dB
	7000 MHz	19.0	20.0	–	dB
	8000 MHz	17.6	18.4	–	dB
IMD3 (CW)	Measured using two pulsed CW (3.5 GHz, 2.5% duty cycle for 4.616 ms period), each 34 dBm. Measurement bandwidth: 100 kHz for carriers and intermodulation products. Spec. limit valid within theoretical IMD3 center frequency ±10 MHz. Carrier spacings: 50 MHz, 100 MHz.	–	-103	-96	dBc
IMD3 (LTE)	LTE signal EMT1.1 34 dBm, 8-dB Par at 3500 MHz	–	-100	-91	dBc
Input IP3 (LTE)	LTE signal EMT1.1 34 dBm, 8-dB Par at 3500 MHz	82	85	–	dBm
Input IP3 (CW)	Measured using 2x 34-dBm CW signals, tone spacings: 50 MHz, 100 MHz.	82	85	–	dBm
Input IP2 (CW)		143	144	–	dBm
Input power handling (RMS)[1]	During static operation, no hot switching. Input signal is LTE 10-MHz ETM1.1 carrier with 10-dB PAR. No compression expected at peak power.	–	–	40	dBm
Input power handling (Peak)		–	–	50	dBm
Input power handling (RMS)	During transition phase. Input signal is LTE 10-MHz ETM1.1 carrier with 10-dB PAR.	–	–	25	dBm
Input power handling (Peak)		–	–	35	dBm

Table 3 • PE42447 Electrical Specifications (Cont.)

Name	Description	Min	Typ	Max	Unit
Reflected power handling (RMS)	Max 10s time duration. Input signal is 37-dBm LTE 10-MHz ETM1.1 carrier with 8-dB PAR on 3.5:1 VSWR. Simultaneous presence of forward and reflected signal. To be tested with different phases of the reflected signal at the output of DUT. Reflected power.	–	–	32	dBm
Reflected power handling (Peak)		–	–	40	dBm
Reflected power handling (RMS)	Indefinite time duration. Input signal is 37-dBm LTE 10-MHz ETM1.1carrier with 8-dB PAR on 2:1 VSWR. Simultaneous presence of forward and reflected signal. To be tested with different phases of the reflected signal at the output of DUT.	–	–	27	dBm
Reflected power handling (Peak)		–	–	35	dBm
Settling time[2]	Insertion loss settled to final value +- 0.1dB. Small signal test.	–	1.27	1.4	µs
Switching time	50% Vctrl to gain settled to IL +/- 0.5 dB. Small signal test.	–	0.9	1	µs
Switching Interval	Time allowed between switching events.	–	16	–	µs
Input P0.1dB[3]	P0.1dB peak using LTE_TDD_10M at 3400 MHz with 10-dB PAR.	–	50.3	–	dBm
Second harmonic	34-dBm input signal CW signal. 3300 to 3800 MHz	–	-111	-104	dBc
Third harmonic	34-dBm input signal CW signal. 3300 to 3800 MHz	–	-105	-98.5	dBc
Return loss input/output	≥1800 MHz	–	33.6	–	dB
	2300 to 2700 MHz	–	31.5	–	dB
	3300 to 3800 MHz	–	23.2	–	dB
	3700 to 4200 MHz	–	21.9	–	dB
	4400 to 5000 MHz	–	21.6	–	dB
	5000 to 6000 MHz	–	15.4	–	dB
	6000 to 7000 MHz	–	13.7	–	dB
	7000 to 8000 MHz	–	10.5	–	dB
Relative phase error	Relative phase error due to temperature variation and part-to-part variation. [phaseDelta(RF1-RF2), phaseDelta(RF1-RF3) and phaseDelta(RF1-RF4)], 2300 to 2700 MHz	–	–	0.65	degree
	Relative phase error due to temperature variation and part-to-part variation. [phaseDelta(RF1-RF2), phaseDelta(RF1-RF3) and phaseDelta(RF1-RF4)], 3300 to 3800 MHz	–	–	0.58	degree
	Relative phase error due to temperature variation and part-to-part variation. [phaseDelta(RF1-RF2), phaseDelta(RF1-RF3) and phaseDelta(RF1-RF4)], 3800 to 5000 MHz	–	–	1.02	degree
Relative phase variation between paths[4]	Relative phase variation between the two phase shifter paths (Path1/2: RF1 - RF4 and Path3/4: RF2 - RF3), 2300 to 2700 MHz	–	–	0.2	degree
	Relative phase variation between the two phase shifter paths (Path1/2: RF1 - RF4 and Path3/4: RF2 - RF3), 3300 to 3800 MHz	–	–	0.25	degree
	Relative phase variation between the two phase shifter paths (Path1/2: RF1 - RF4 and Path3/4: RF2 - RF3), 3800 to 5000 MHz	–	–	0.33	degree

Table 3 • PE42447 Electrical Specifications (Cont.)

Name	Description	Min	Typ	Max	Unit

Notes:

1) The input power handling (RMS) needs to be de-rated to 39 dBm for 105 °C T_{CASE} operation to maintain safe operation over the lifetime of the part.
2) At 1.1 µs after an switching event, the third harmonic on the selected port should settle to -70 dBc for an input signal with peak power of 43 dBm or less.
3) The P0.1 dB is measured under steady state condition and not 1.1 µs after a switching event.
4) The phase shifter paths are shown in **Figure 13**. The 'relative phase variation' is calculated with between Path1 and Path3 (or Path2 and Path4). The reason for choosing this combination is because RF1 and RF4 are symmetric ports (and so are RF2 and RF3), so the phase error between Path1 and Path2 (or Path3 and Path4) should be negligible.

SP4T Control Logic

Table 4 list the PE42447 control logic truth table.

Table 4 • PE42447 Truth Table

ON Port	V2	V1	SEL
RF1	0	0	0
RF2	0	1	0
RF3	1	0	0
RF4	1	1	0
Transpose			
RF1	1	1	1 or no-connect
RF2	1	0	1 or no-connect
RF3	0	1	1 or no-connect
RF4	0	0	1 or no-connect

Typical Performance Data

Figure 2–Figure 10 show the typical performance data at +25 °C T_{CASE} and VDD = 5V (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 2 • Insertion Loss RFc to RFx vs. Frequency

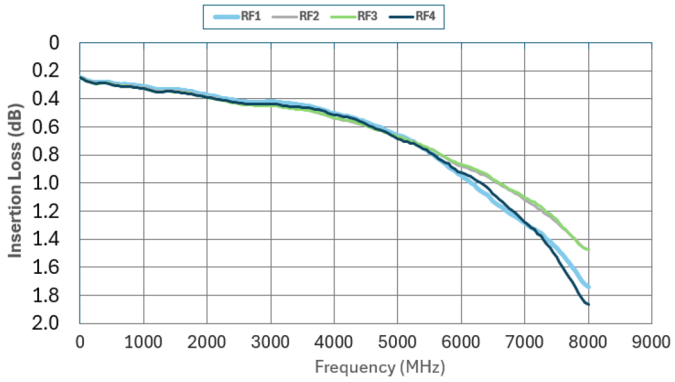


Figure 3 • Insertion Loss Over Temperature RF1

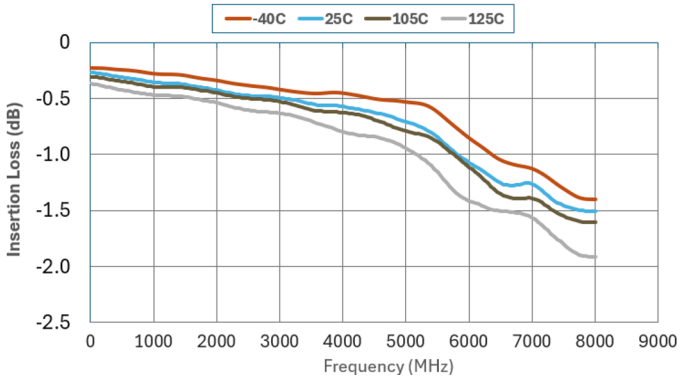


Figure 4 • Input Return Loss When RFx is Selected

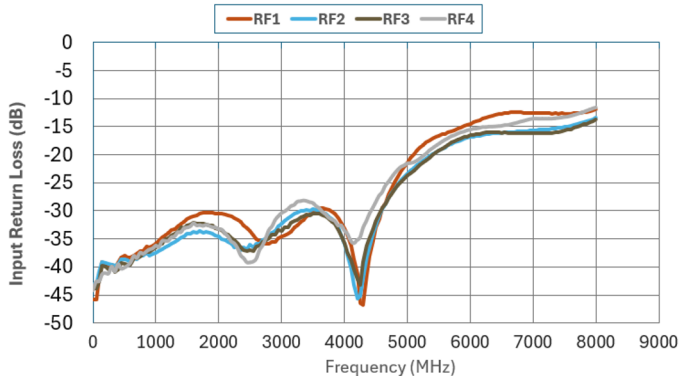


Figure 5 • Output Return Loss When RFx is Selected

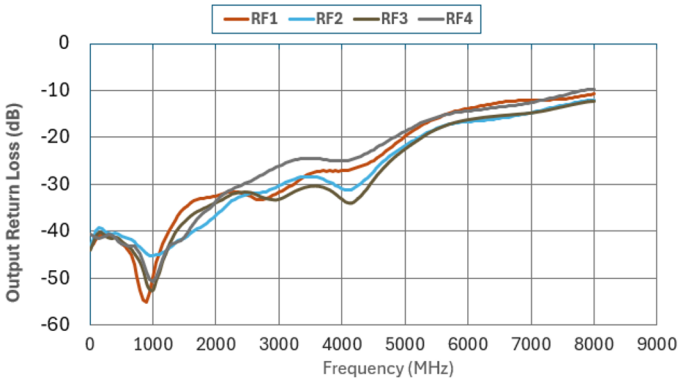


Figure 6 • Output Return Loss When RFx is Not Selected

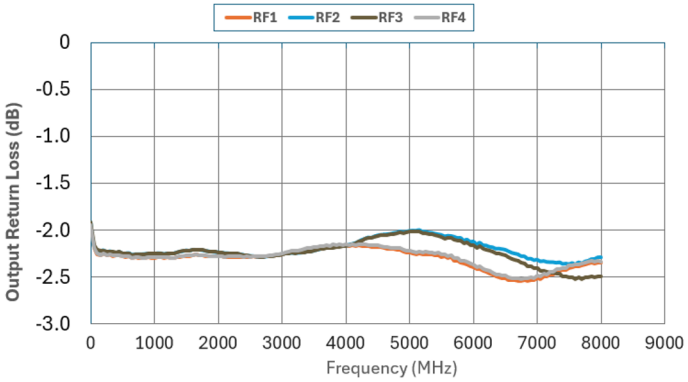


Figure 7 • Isolation When RF1 is On

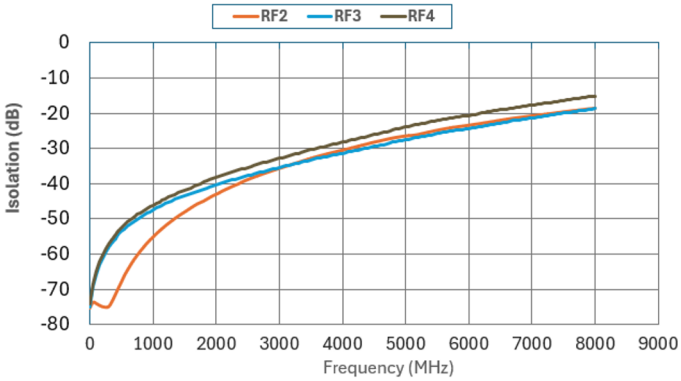


Figure 8 • Isolation When RF2 is On

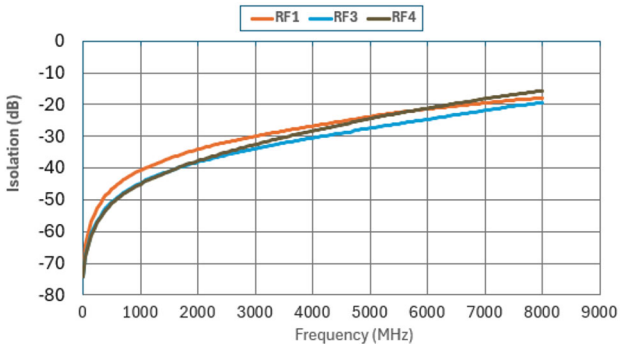


Figure 9 • Isolation When RF3 is On

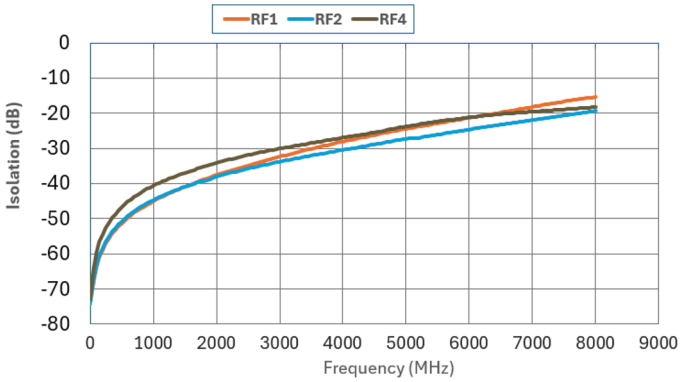
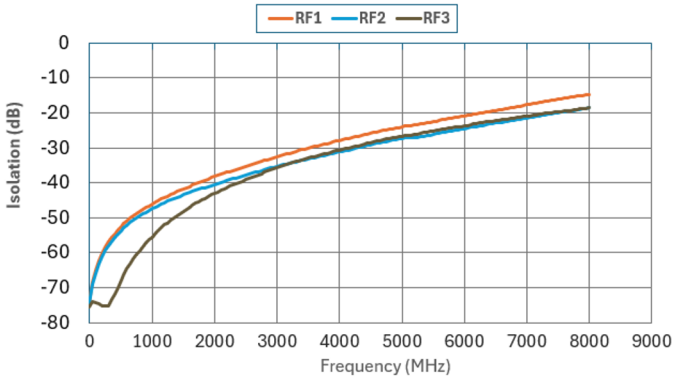


Figure 10 • Isolation When RF4 is On



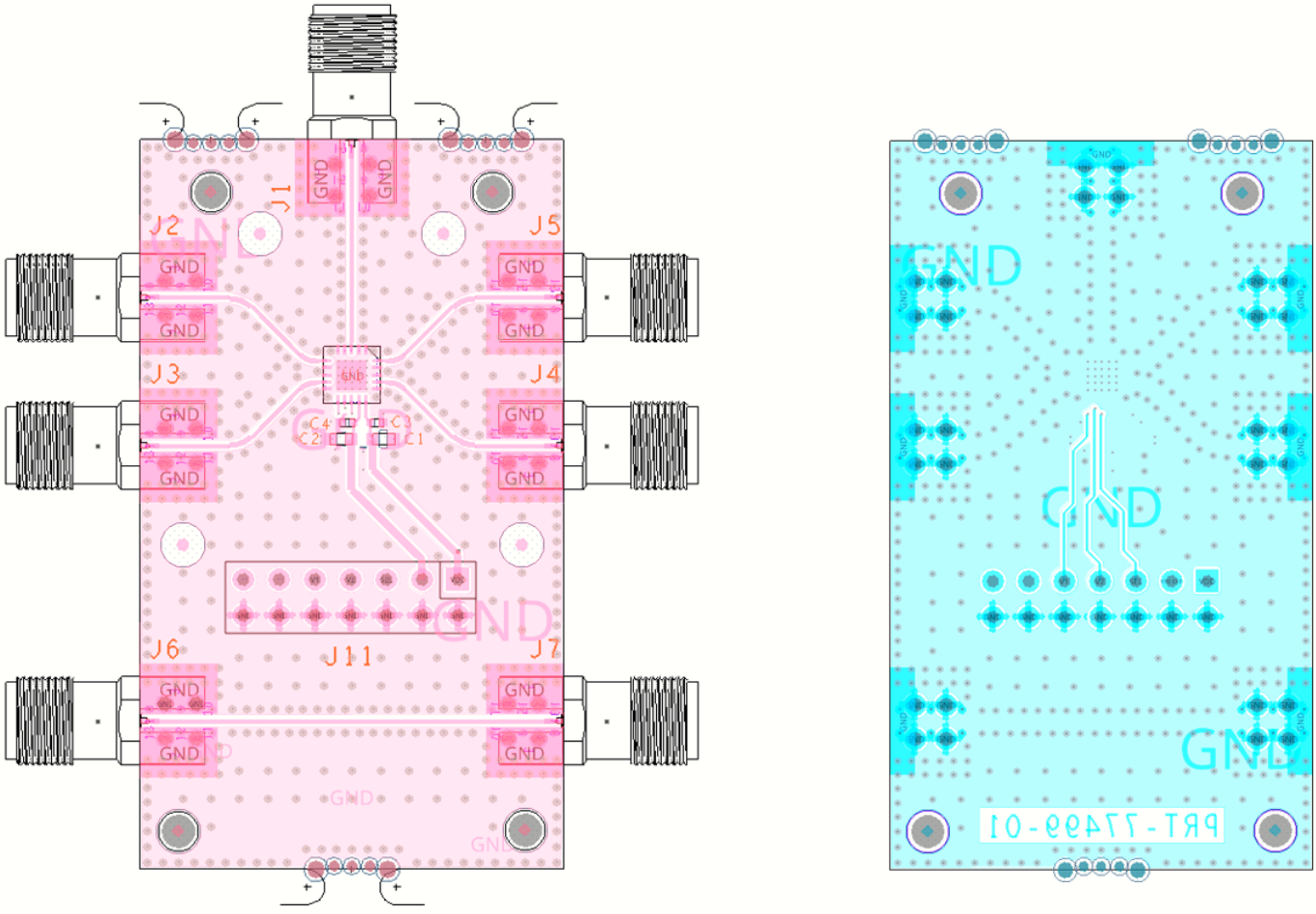
Evaluation Kit

pSemi designed the SPDT switch evaluation board (PRT-77499) to ease your evaluation of the pSemi PE42447. The RF common port is connected through a 50Ω transmission line via the top SMA connector J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via side SMA connectors J2, J3, J4 and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C™ and FR406 with a total thickness of 62 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 1 and use a coplanar waveguide design with a trace width of 15.8 mils, signal-to-ground spacing of 8 mils, and trace metal thickness of 1.7 mils. The board stackup for 50Ω transmission lines has 8-mil thickness of Rogers 4003C between layer 1 and layer 2, and 42-mil thickness of FR406 between layer 2 and layer 3.

Please consult the manufacturers' guidelines for proper board material properties in your application. The PCB must be designed in such a way that RF transmission lines and sensitive DC I/O traces such as VSS_EXT are heavily isolated from one another; otherwise, the true performance of the PE42447 could be hindered.

Figure 11 • Evaluation Board Layout, PE42447 Top/Bottom Layer



Top Layer *Bottom Layer*

Evaluation Board Schematic and BOM

Figure 12 shows the evaluation board schematic, and **Table 5** lists the evaluation board bill of materials.

Figure 12 • PE42447 Evaluation Board Schematic

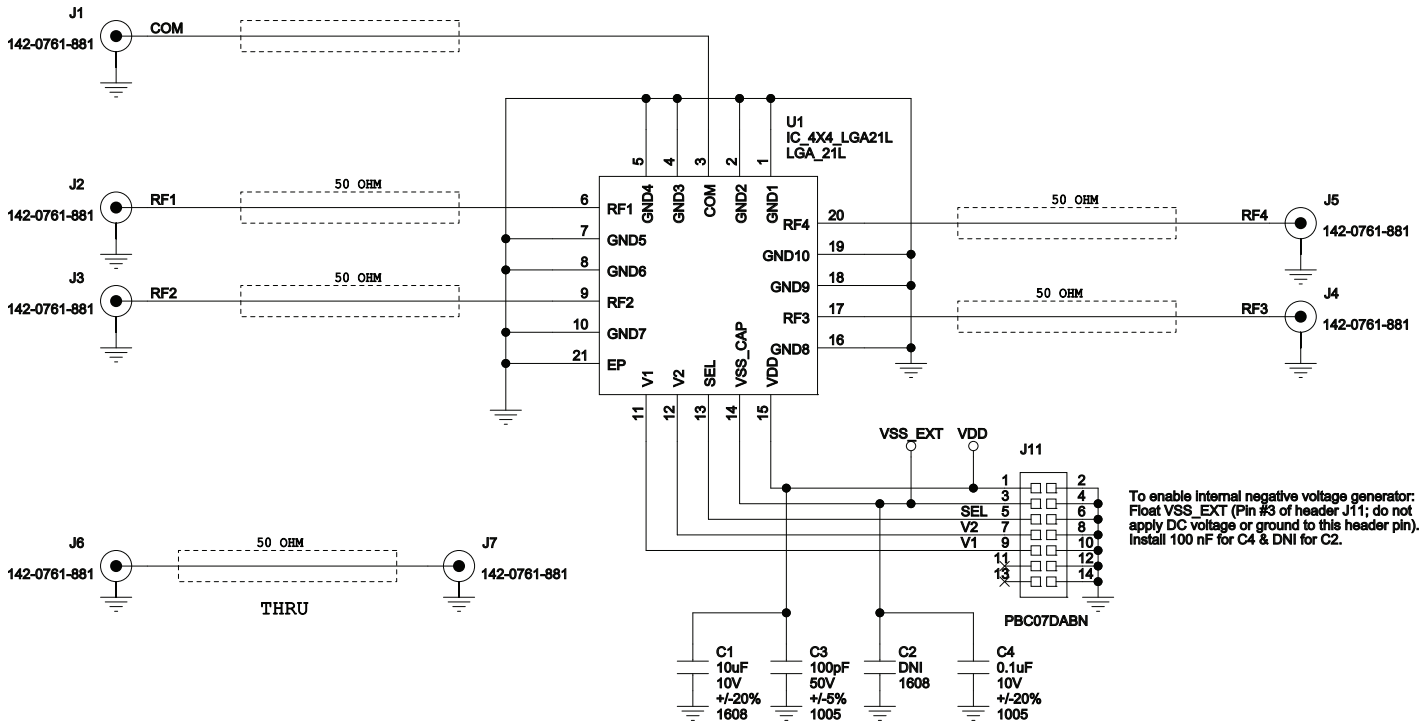


Table 5 • PE42447 Evaluation Board BOM Components

Reference	Value	Description	Manufacturer	Mfg. Part Number
C1	10 µF	CAP, SMD, CER, 10 µF, 10V, +/-20%, X7T, 0603 (1608 Metric)	Murata Electronics North America	GRM188D71A106-MA73D
C2	DNI	CAP, SMD, CER, DNI, n/a, n/a, n/a, 0603 (1608 Metric)	Murata Electronics North America	–
C3	100 pF	CAP, SMD, CER, 100 pF, 50V, +/-5%, C0G, NP0, 0402 (1005 Metric)	Murata Electronics North America	GRM1555C1H101-JA01D
C4	0.1 µF	CAP, SMD, CER, 0.1 µF, 10V, +/-20%, X5R, 0402 (1005 Metric)	Murata Electronics North America	GRM155R61A104-MA01D
J1,J2,J3,J4,J5, J6,J7	142-0761-881	CONN, Coaxial Connectors (RF), SMA, SMD, Jack, Female Socket, 50 Ohm	Cinch Connectivity Solutions Johnson	142-0761-881
J11	PBC07DABN	CONN, Rectangular Connectors - Headers, Male Pins, Header Unshrouded Breakaway, TH, Male	Sullins Connector Solutions	PBC07DABN
PCB1	PCB	PCB,PE42447 SP4T EVK	pSemi Corporation	PRT-77499
U1	IC-4X4_ LGA21L	20-lead 4 × 4 mm LGA	pSemi Corporation	PE42447

Application Diagram

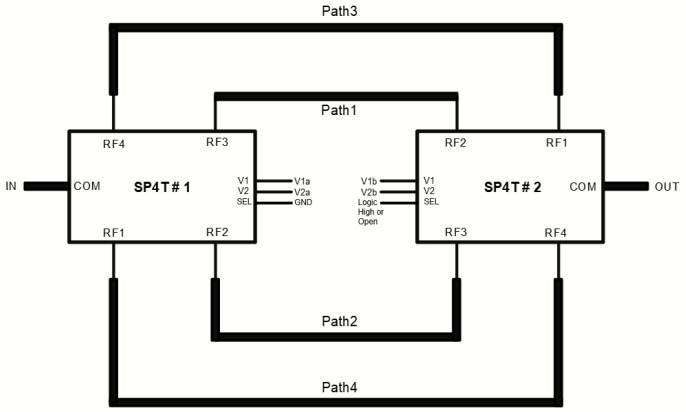
Table 6 • Application Diagram Lookup Table

Phase State	ON Ports		Path
	SP4T #1	SP4T #2	
State 1	RF3	RF2	Path 1
State 2	RF2	RF3	Path 2
State 3	RF4	RF1	Path 3
State 4	RF1	RF4	Path 4

Figure 13 shows an application diagram for a phase shifter application implemented using two SP4T switches.

Note: To characterize the parameters Relative Phase, Relative Phase Error, and Relative Phase Variation between Paths, all four paths had exactly the same delay line lengths.

Figure 13 • PE42447 Application Diagram Used in a Phase Shifter



Pin Information

Figure 14 shows the PE42447 pin map for the 20-lead 4 × 4 mm LGA package, and **Table 7** lists the description for each pin.

Figure 14 • Pin Configuration (Top View)

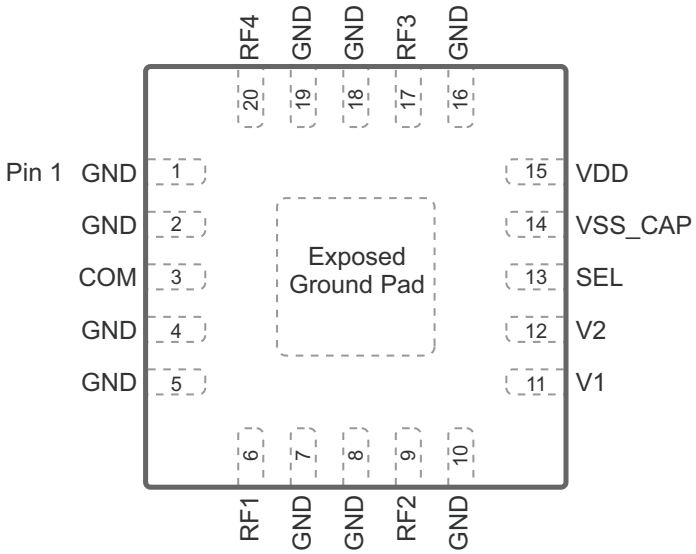


Table 7 • PE42447 Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	COM[1]	RF common port
4	GND	Ground
5	GND	Ground
6	RF1[1]	RF port 1
7	GND	Ground
8	GND	Ground
9	RF2[1]	RF port 2
10	GND	Ground
11	V1	Digital control logic input 1
12	V2	Digital control logic input 2
13	SEL[2]	Logic select—used to determine definition for V1 and V2 pins
14	VSS_CAP[3]	Bypass capacitor for VSS
15	VDD	Supply voltage
16	GND	Ground
17	RF3[1]	RF port 3
18	GND	Ground
19	GND	Ground
20	RF4[1]	RF port 4
Pad	GND	Exposed pad: ground for proper operation.

1) RF pins 3, 6, 9, 17 and 20 must be at 0 V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0 V DC requirement is met.
2) Internal pull-up resistor will set pin to logic high if pin is floating. Ground pin to set to logic low.
3) Install capacitor on VSS_CAP (pin 14) to GND. Do not apply DC or ground this pin. Either leave the pin open or connect a supply capacitor on this pin on the application board. The capacitor can be 100 nF or above. The larger the capacitor value, the longer will be the circuit startup time.

Packaging Information

This section provides the following packaging data:

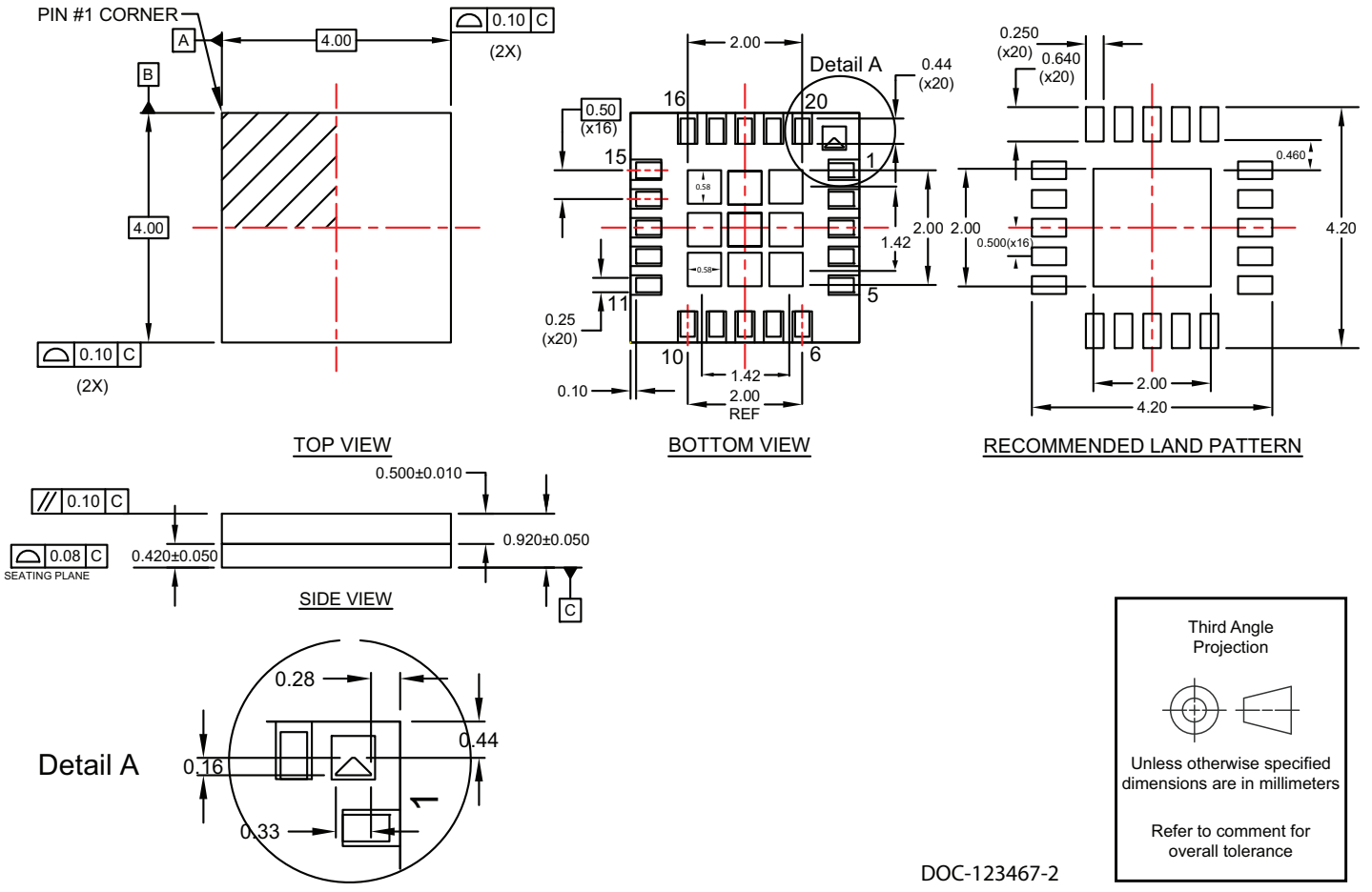
- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The PE42447 moisture sensitivity level rating for the 20-lead 4 × 4 mm LGA package is MSL3.

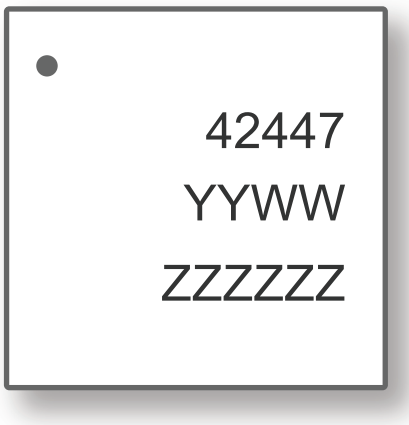
Package Drawing

Figure 15 • Package Mechanical Drawing for the 20-lead 4 × 4 mm LGA Package



Top-Marking Specification

Figure 16 • PE42447 Package Marking Specification

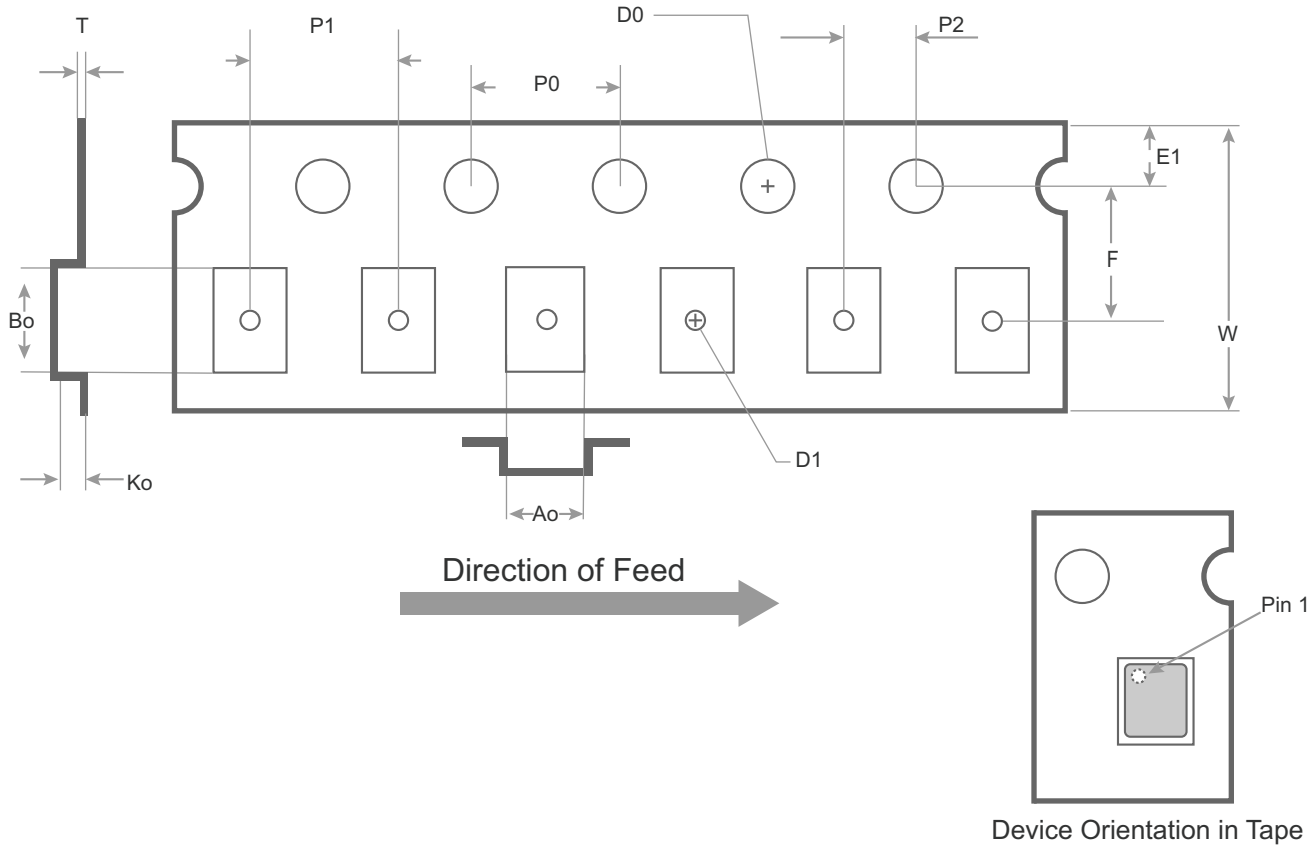


● = Pin 1 indicator
42447 = Product part number
YY = Last two digits of assembly year (2022 = 22)
WW = Work week of assembly lot start date (01, ..., 52)
ZZZZZZ = Assembly lot code (max six characters)

DOC-100702-1

Tape and Reel Specification

Figure 17 • Tape and Reel Specification for the 20-lead 4 × 4 mm LGA Package



Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 8 • Tape and Reel Dimensions

Carrier Tape Dimensions					
Pocket	**Nominal**	**Tolerance**	**Pocket**	**Nominal**	**Tolerance**
Ao	4.30	±0.10	**D1**	1.50	+0.20/-0
Bo	4.30	±0.10	**D0**	1.50	+0.10/-0
Ko	1.25	±0.10	**E1**	1.75	±0.10
P1	8.00	±0.10	**P0**	4.00	±0.10
W	12.00	+0.30/-0.10	**P2**	2.00	±0.05
F	5.50	±0.05	**T**	0.30	±0.03

Ordering Information

Table 9 • PE42447 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE42447A-Z	PE42447 SP4T switch	Green 20-lead 4 × 4 mm LGA	3000 units/T&R
EK42447-01	PE42447 evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark

©2024–2025, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View PE42447A-Z on WIN SOURCE
- pSemi Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management