THE DATASHEET OF

PE424201A-Z

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PE42420

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 20–6000 MHz

Features

- HaRP™ technology enhanced:
  - No gate or phase lag
  - No drift in insertion loss and phase
- High linearity: IIP3 of 65 dBm
- High isolation:
  - 69 dB @ 1 GHz
  - 62 dB @ 3 GHz
  - 50 dB @ 6 GHz
- Supports +1.8V control logic
- +125 °C operating temperature
- High ESD tolerance:
  - 4 kV HBM on RFC
  - 2 kV HBM on all other pins
- Packaging: 20-lead 4 × 4 mm LGA

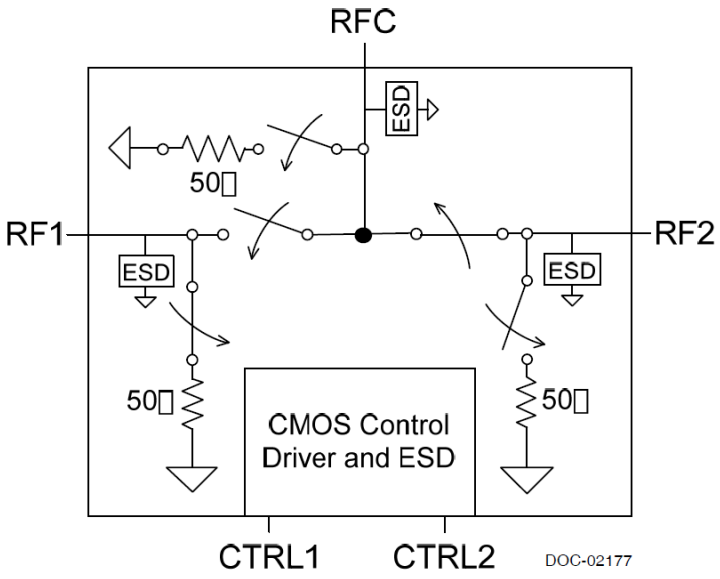


Figure 1. PE42420 functional diagram

Applications

- Transmit path switching
- RF and IF signal routing
- AGC loops
- Filter bank switching

Product description

The PE42420 is a HaRP™ technology-enhanced absorptive SPDT RF switch designed for use in 3G/4G wireless infrastructure and other high-performance RF applications.

This general-purpose switch consists of two symmetric RF ports with exceptional port-to-port isolation up to 6 GHz. An integrated CMOS decoder provides an easy two-pin, low-voltage CMOS control interface. No external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42420 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42420 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage, CTRL1 and CTRL2	V_{CTRL}	-0.3	3.6	V
Operating power, 20 MHz[1]	P_{IN}	–	28	dBm
Maximum peak power into termination (RFx)[2]	P_{MAX}	–	23	dBm
Storage temperature range	T_{ST}	-65	+150	°C
Maximum die junction temperature	T_{JMAX}	–	+150	°C
ESD voltage HBM:[3] - RFC - All other pins	$V_{ESD,HBM}$	–	 4000 2000	V
ESD voltage MM, all pins[4]	$V_{ESD,MM}$	–	100	V

1. 100% duty cycle, all bands, 50Ω.
2. 10-dB PAR, all bands, 50Ω.
3. Human Body Model (MIL-STD 883 Method 3015).
4. Machine Model (JEDEC JESD22-A115).

Recommended operating conditions

Table 2 lists the PE42420 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42420 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	–	5.5	V
Supply current, V_{DD} = 2.7–5.5V	I_{DD}	–	120	200	µA
Digital input high, CTRL1 and CTRL2	V_{IH}	1.17	–	3.6	V
Digital input low, CTRL1 and CTRL2	V_{IL}	-0.3	–	0.6	V
Digital input current	I_{CTRL}	–	9	12	µA
Maximum operating power, RFC–RFx(1)	P_{IN}	–	–	25	dBm
Maximum peak power into termination (RFx) at +125 °C(2)	$P_{MAX,CW}$	–	–	20	dBm
Operating temperature range	T_{OP}	-40	–	+125	°C

1. 100% duty cycle, all bands, 50Ω.
2. 10-dB PAR, all bands, 50Ω.

Electrical specifications

Table 3 lists the PE42420 key electrical specifications at +25 °C and V_{DD} = 3.0V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42420 electrical specifications at +25 °C

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	20	–	6000	MHz
Insertion loss	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz(1) 3000–4000 MHz(1) 4000–5000 MHz(1) 5000–6000 MHz(1)	–	0.95 0.95 1.00 1.15 1.25 1.60	1.15 1.15 1.20 1.35 1.55 1.90	dB
Isolation	RFx–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	67 63 59 60 54 44	69 64 62 64 60 50	–	dB
Isolation	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	69 65 63 62 52 44	71 67 68 67 57 48	–	dB
Return loss, all ports,	–	20–4000 MHz 4000–5000 MHz(1) 5000–6000 MHz(1)	–	20 15 13	–	dB
Input 1-dB compression point(2)	RFC–RFx	20–100 MHz 100–6000 MHz	31 33	–	–	dBm
Input IP2	RFC–RFx	20–100 MHz 100–6000 MHz	–	80 110	–	dBm
Input IP3	RFC–RFx	20–100 MHz 100–6000 MHz	 60	65 65	–	dBm
Switching time(3)	–	50% CTRL to 90% or 10% RF	–	300	400	ns

1. To improve the insertion loss and return loss, use external matching.
2. The input 1-dB compression point is a linearity figure of merit. For the maximum operating power, P_{IN} (50Ω), see Table 2.
3. The PE42420 has a maximum 25 kHz switching frequency. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 4 lists the PE42420 key electrical specifications at +105 °C and V_{DD} = 3.0V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 4. PE42420 electrical specifications at +105 °C

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	20	–	6000	MHz
Insertion loss	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz(1) 3000–4000 MHz(1) 4000–5000 MHz(1) 5000–6000 MHz(1)	–	1.05 1.10 1.25 1.35 1.50 1.60	1.25 1.35 1.45 1.75 2.00 2.00	dB
Isolation	RFx–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	66 63 59 60 54 44	68 64 62 64 60 50	–	dB
Isolation	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	68 65 62 62 51 44	70 67 67 67 55 48	–	dB
Return loss, all ports,	–	20–4000 MHz 4000–5000 MHz(1) 5000–6000 MHz(1)	–	19 15 13	–	dB
Input 1-dB compression point(2)	RFC–RFx	20–100 MHz 100–6000 MHz	 33	31	–	dBm
Input IP2	RFC–RFx	20–100 MHz 100–6000 MHz	–	80 110	–	dBm
Input IP3	RFC–RFx	20–100 MHz 100–6000 MHz	 60	65 65	–	dBm
Switching time(3)	–	50% CTRL to 90% or 10% RF	–	300	400	ns

1. To improve the insertion loss and return loss, use external matching.
2. The input 1-dB compression point is a linearity figure of merit. For the maximum operating power, P_{IN} (50Ω), see Table 2.
3. The PE42420 has a maximum 25 kHz switching frequency. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 5 lists the PE42420 key electrical specifications at +125 °C and V_{DD} = 3.0V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 5. PE42420 electrical specifications at +125 °C

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	20	–	6000	MHz
Insertion loss	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz(1) 3000–4000 MHz(1) 4000–5000 MHz(1) 5000–6000 MHz(1)	–	1.14 1.23 1.35 1.54 1.71 1.75	1.52 1.57 1.67 2.39 2.97 3.01	dB
Isolation	RFx–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	65 61 49 57 52 42	68 64 64 71 61 49	–	dB
Isolation	RFC–RFx	20–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	64 64 62 60 40 39	69 67 67 66 54 47	–	dB
Return loss, all ports,	–	20–4000 MHz 4000–5000 MHz(1) 5000–6000 MHz(1)	–	16 13 13	–	dB
Input 1-dB compression point(2)	RFC–RFx	20–100 MHz 100–6000 MHz	 33	–	–	dBm
Input IP2	RFC–RFx	20–100 MHz 100–6000 MHz	–	 107	–	dBm
Input IP3	RFC–RFx	20–100 MHz 100–6000 MHz	 60	 65	–	dBm
Switching time(3)	–	50% CTRL to 90% or 10% RF	–	300	400	ns

1. To improve the insertion loss and return loss, use external matching.
2. The input 1-dB compression point is a linearity figure of merit. For the maximum operating power, P_{IN} (50Ω), see Table 2.
3. The PE42420 has a maximum 25 kHz switching frequency. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42420 typical spurious performance is –155 dBm.

The PE42420 uses a negative voltage generator with a fundamental frequency of ~11 MHz. This can result in harmonics spurious in the 20–100 MHz band at -110 dBm or lower. Consider the effect of these on your system noise figure or receiver sensitivity.

SPDT control logic

Table 6. PE42420 truth table

CTRL1	CTRL2	RFC–RF1	RFC–RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A(*)	N/A(*)

* CTRL1 = high and CTRL2 = high are not supported.

Typical performance data

Figure 2–Figure 16 show the typical performance data at +25 °C and V_{DD} = 3.0V, unless otherwise specified.

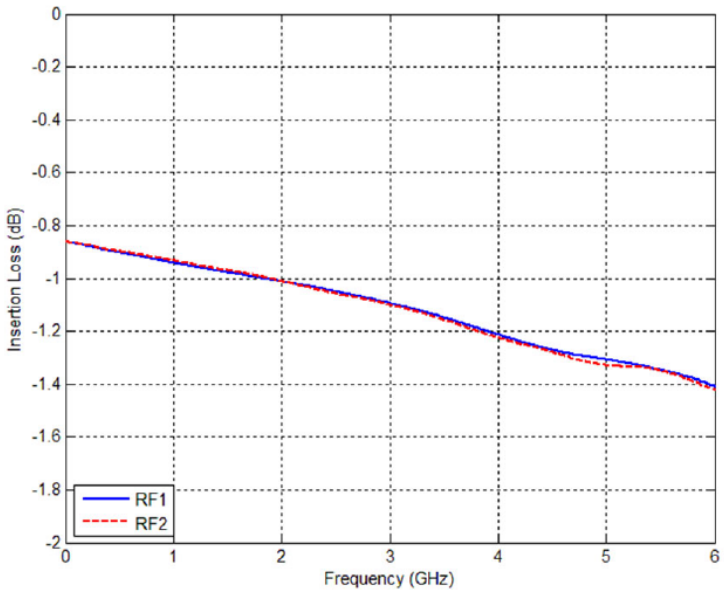


Figure 2. Insertion loss (RFC–RFx)

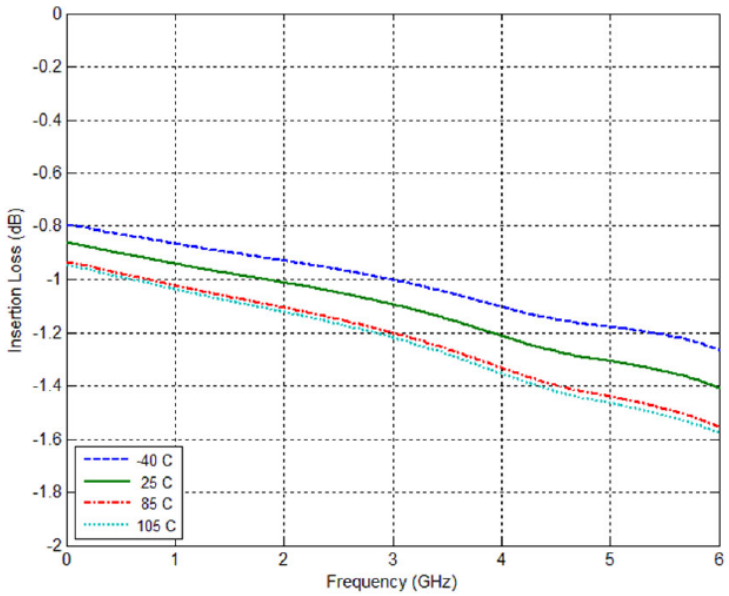


Figure 3. Insertion loss vs. temperature (RFx–RFC)

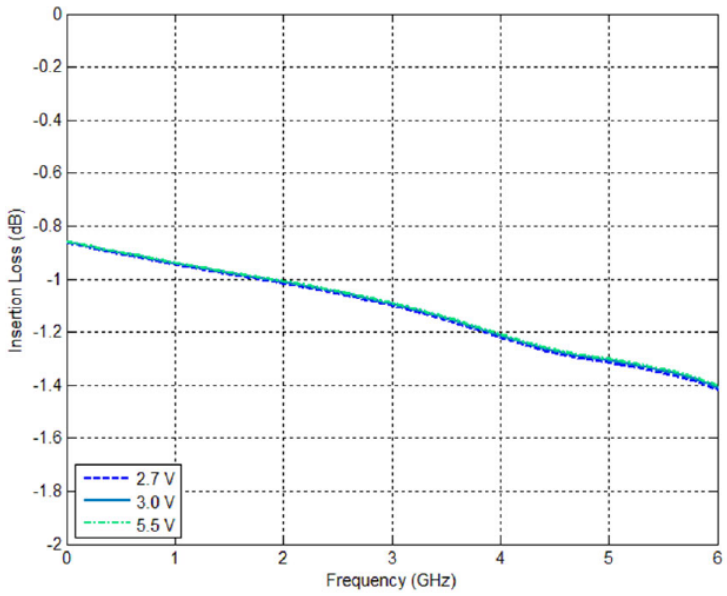


Figure 4. Insertion loss vs. V_{DD} (RFx–RFC)

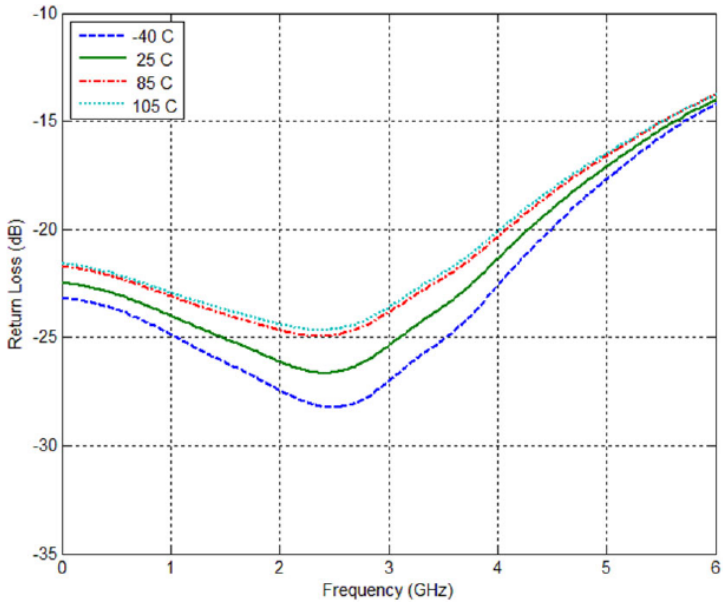


Figure 5. RFC port return loss vs. temperature (RF1 active)

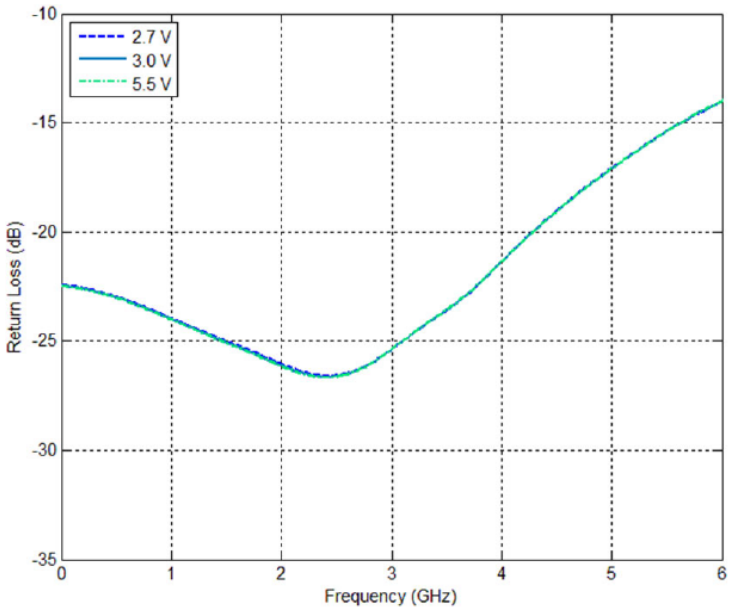


Figure 6. RFC port return loss vs. V_{DD} (RF1 active)

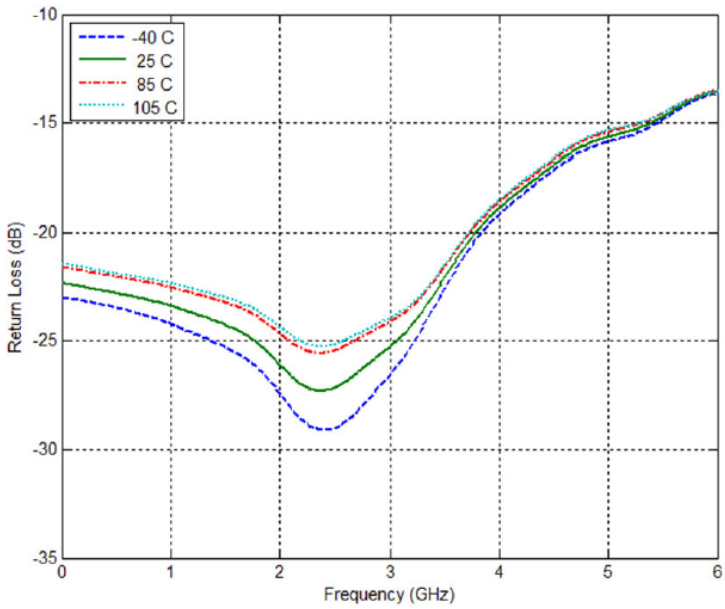


Figure 7. RFC port return loss vs. temperature (RF2 active)

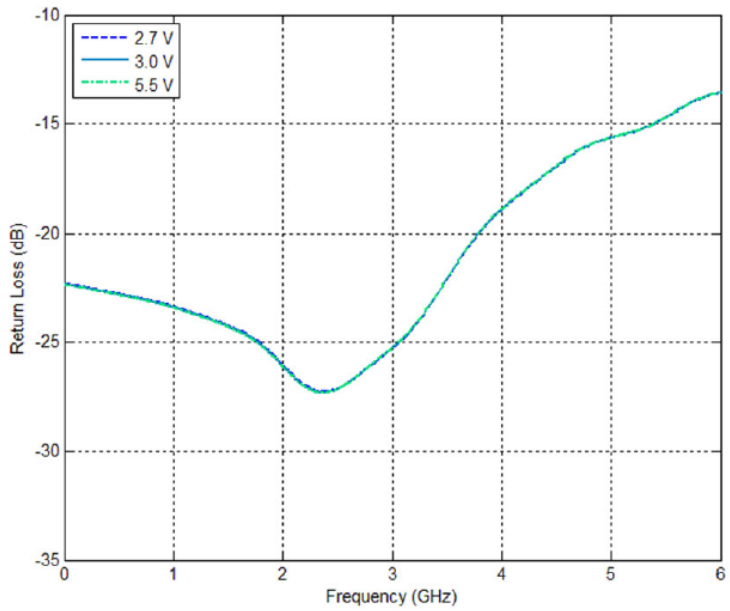


Figure 8. RFC port return loss vs. V_{DD} (RF2 active)

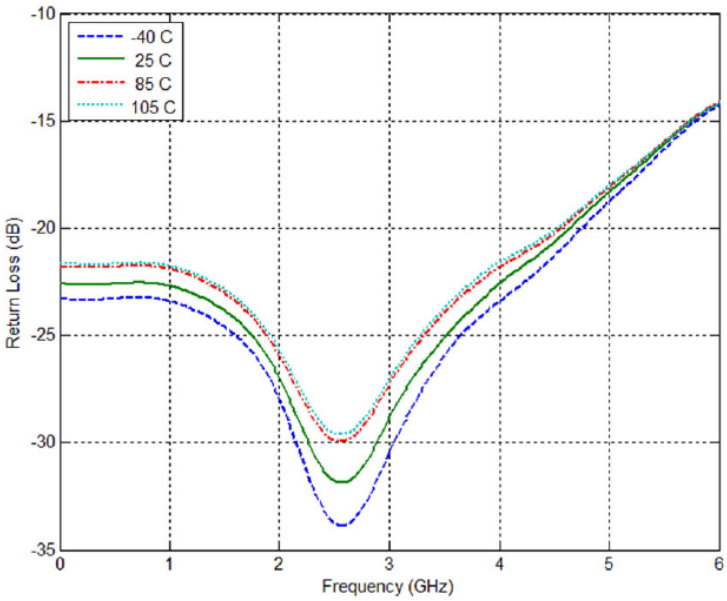


Figure 9. Active port return loss vs. temperature (RF1 active)

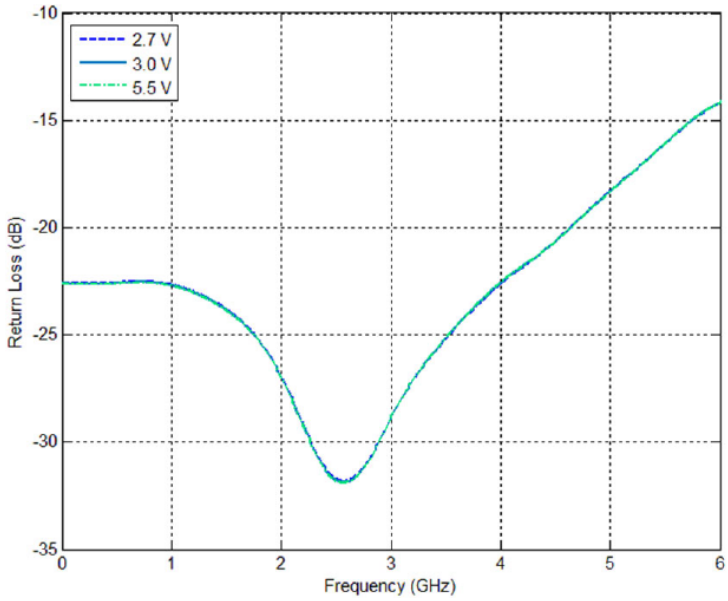


Figure 10. Active port return loss vs. V_{DD} (RF1 active)

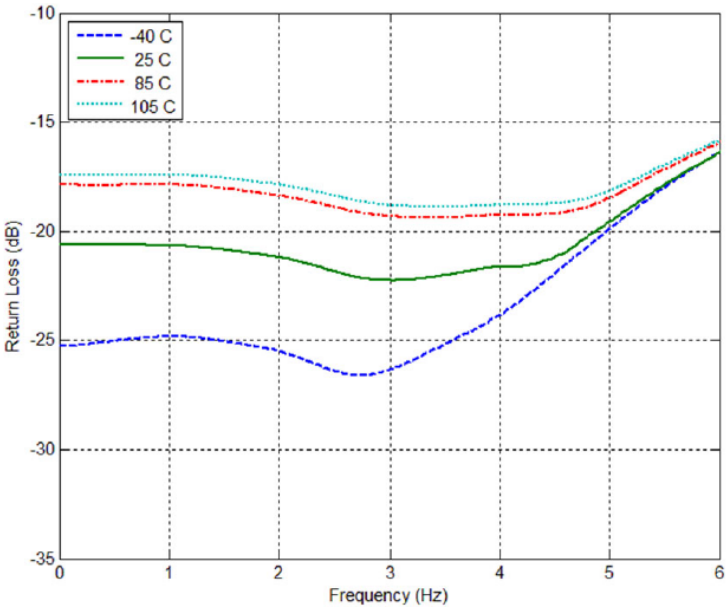


Figure 11. Terminated port return loss vs. temperature (RF1 active)

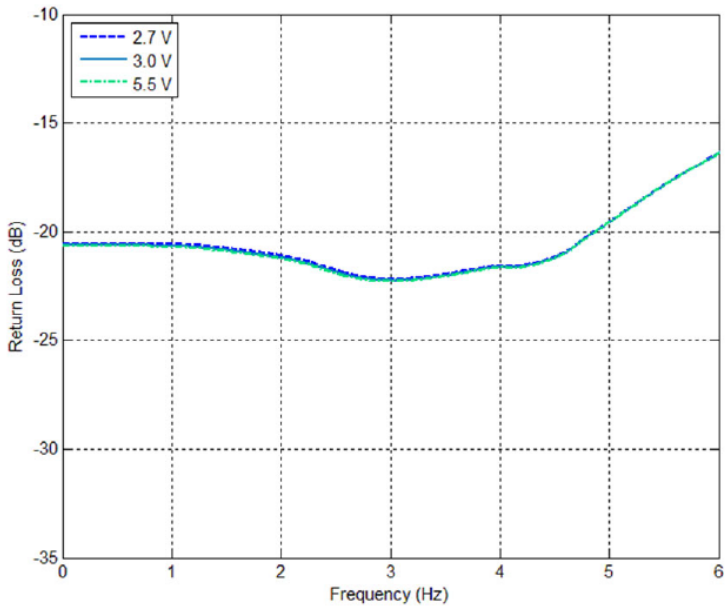


Figure 12. Terminated port return loss vs. V_{DD} (RF1 active)

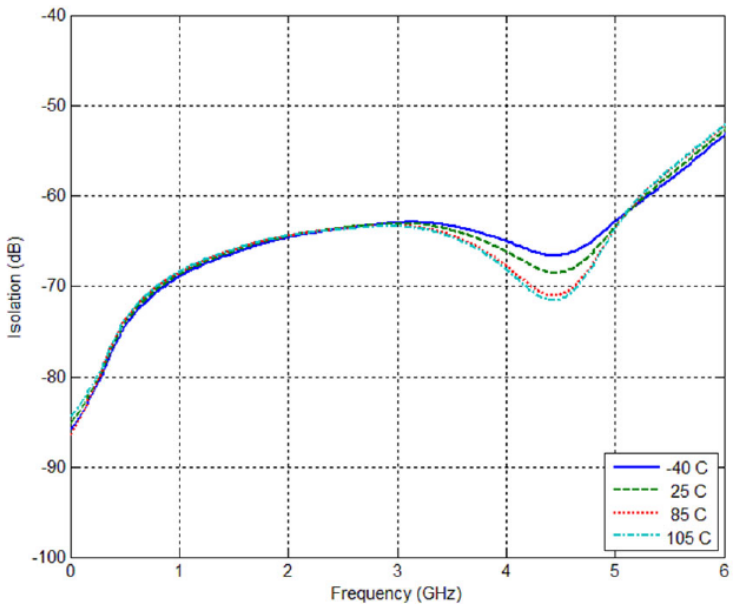


Figure 13. Isolation vs. temperature (RFx–RFx)

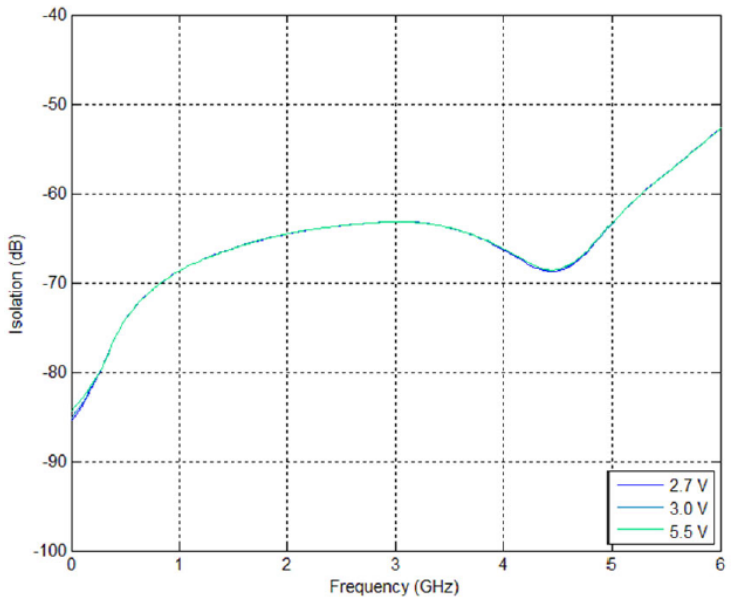


Figure 14. Isolation vs. V_{DD} (RFx–RFx)

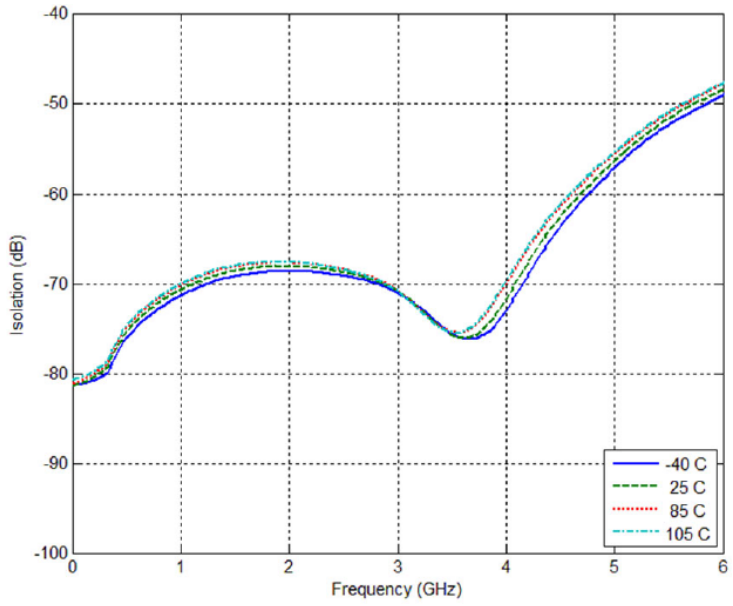


Figure 15. Isolation vs. temperature (RFC–RFx)

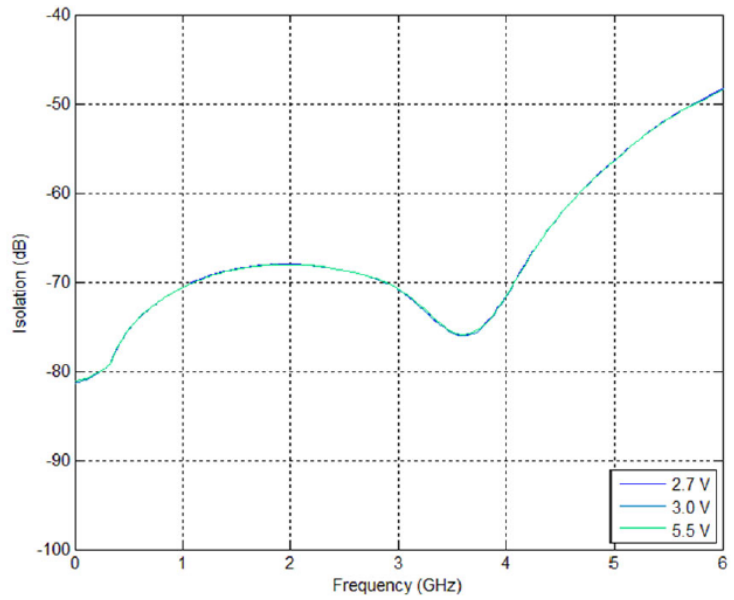


Figure 16. Isolation vs. V_{DD} (RFC–RFx)

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the pSemi PE42420. The RF common port connects through a 50Ω transmission line via the top SMA connector, J2. The RF1 and RF2 ports connect through 50Ω transmission lines via SMA connectors J1 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J4 and J5, which you can use to calculate the loss of the PCB. J6 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 36 mils. To achieve high isolation, the 50Ω transmission lines are designed in layer 2 using a stripline waveguide design. The board stack up for 50Ω transmission lines has 10 mil thickness of Rogers 4350 between layer 1 and layer 2, and 10 mil thickness of Rogers 4350 between layer 2 and layer 3.

To realize the true performance of the PE42420, design the PCB so that the RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

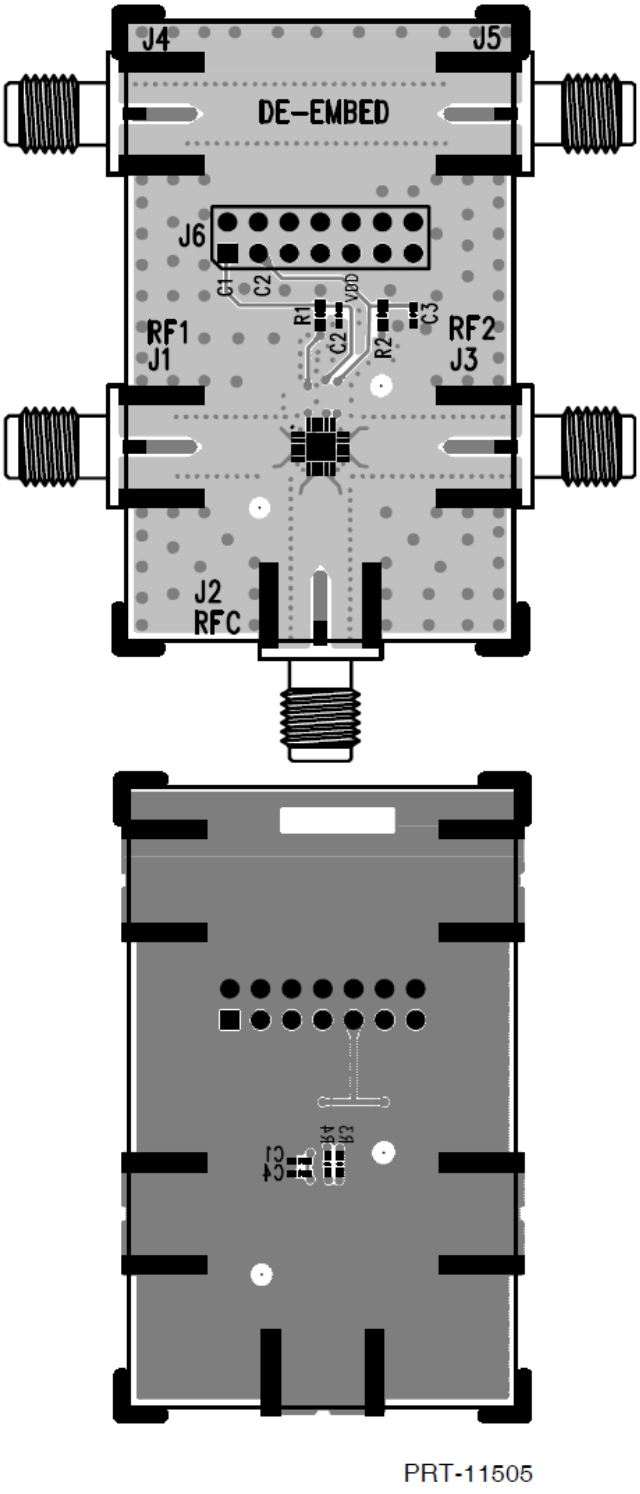


Figure 17. Evaluation board layout

Evaluation board schematic

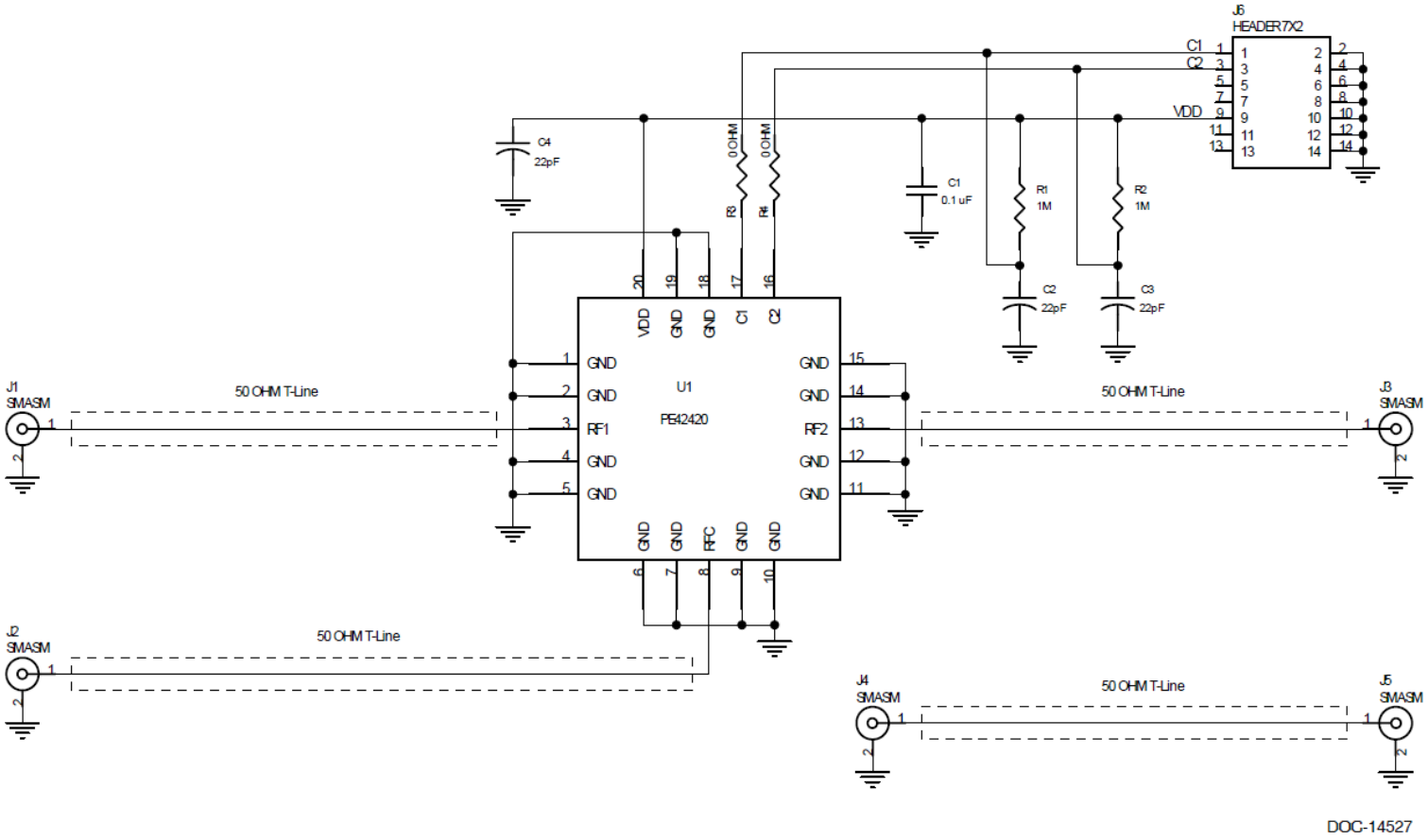


Figure 18. Evaluation board schematic

Pin information

Figure 19 shows the PE42420 pin map for the 20-lead 4 × 4 mm LGA package, and Table 7 lists the description for each pin.

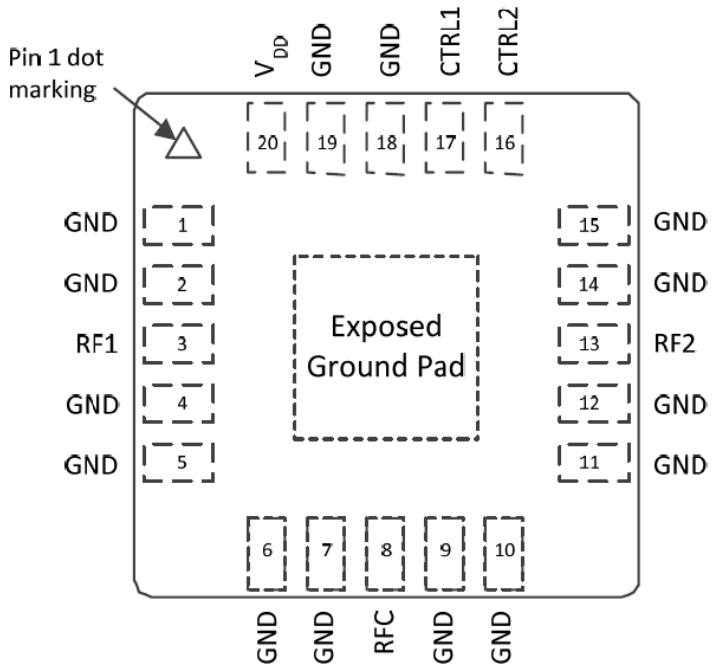


Figure 19. Pin configuration (top view)

Table 7. PE42420 pin descriptions

Pin no.	Pin name	Description
1, 2, 4–7, 9, 10–12, 14, 15, 18, 19	GND	Ground
3(*)	RF1	RF port 1
8(*)	RFC	RF common
13(*)	RF2	RF port 2
16	CTRL2	Digital control logic input 2
17	CTRL1	Digital control logic input 1
20	V_{DD}	Supply voltage
Pad	GND	Exposed pad. Ground for proper operation.

* RF pins 3, 8, and 13 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42420 moisture sensitivity level rating for the 20-lead 4 × 4 mm LGA package is MSL3.

Package drawing

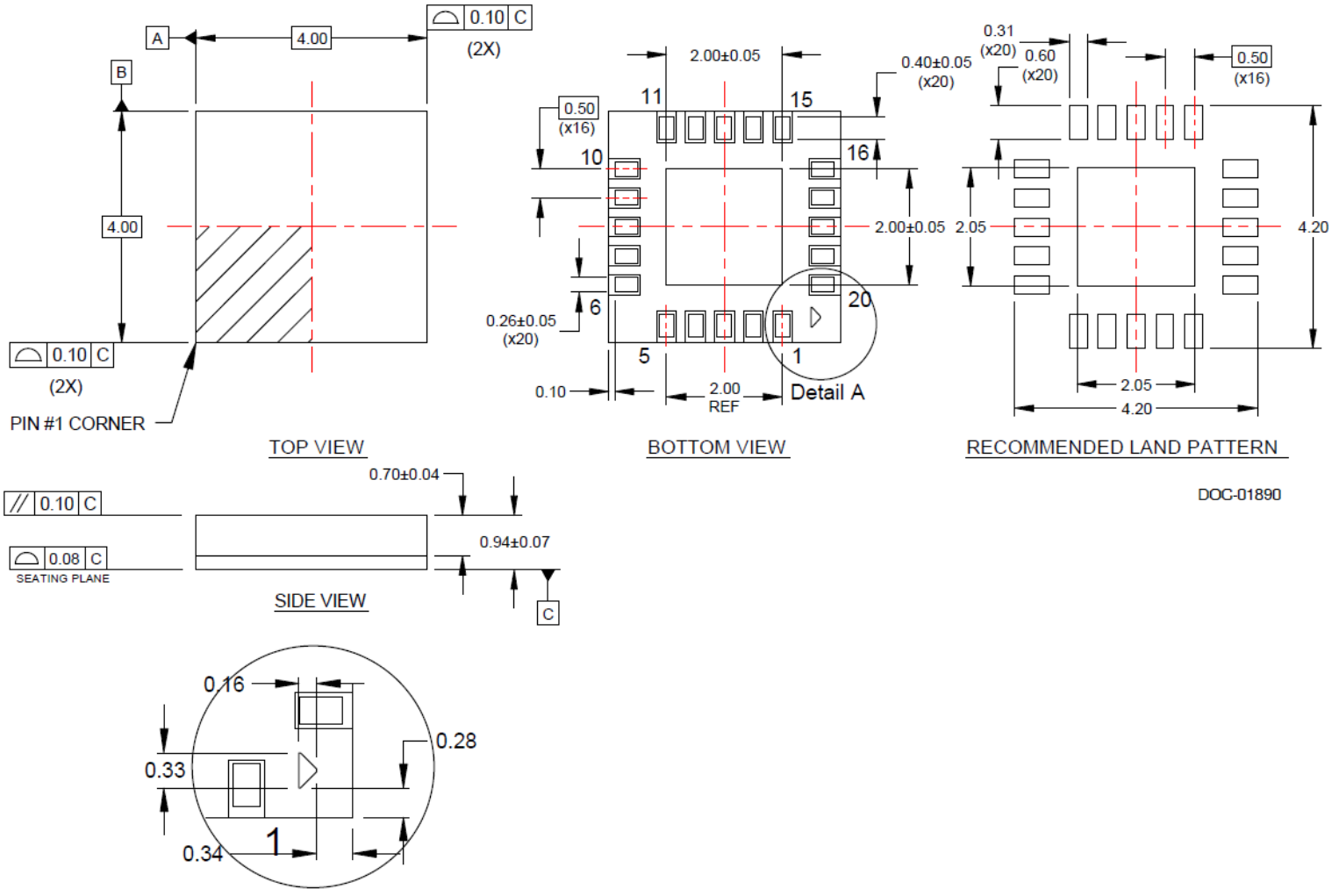


Figure 20. Package mechanical drawing for the 20-lead 4 × 4 mm LGA package

Top-marking specification

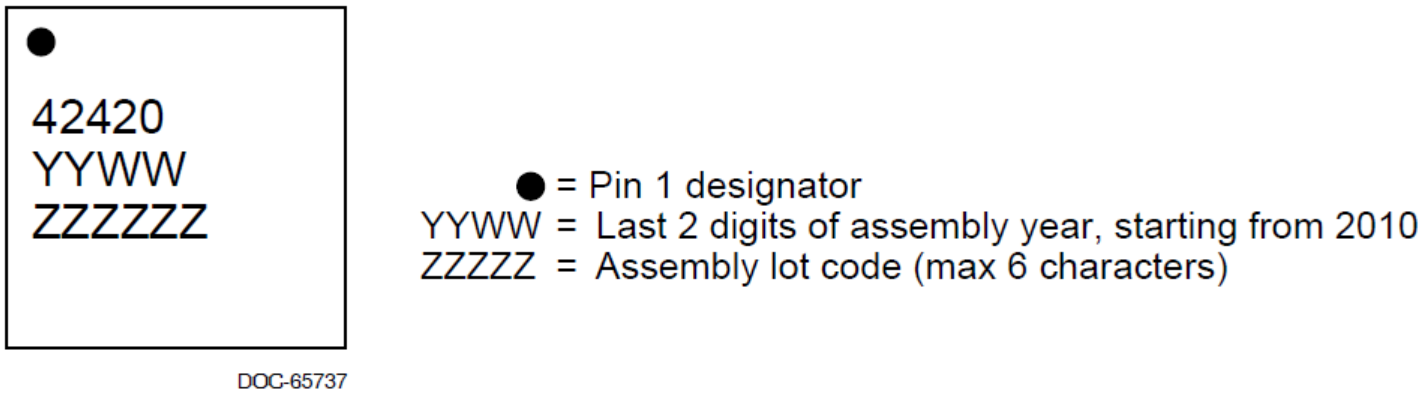
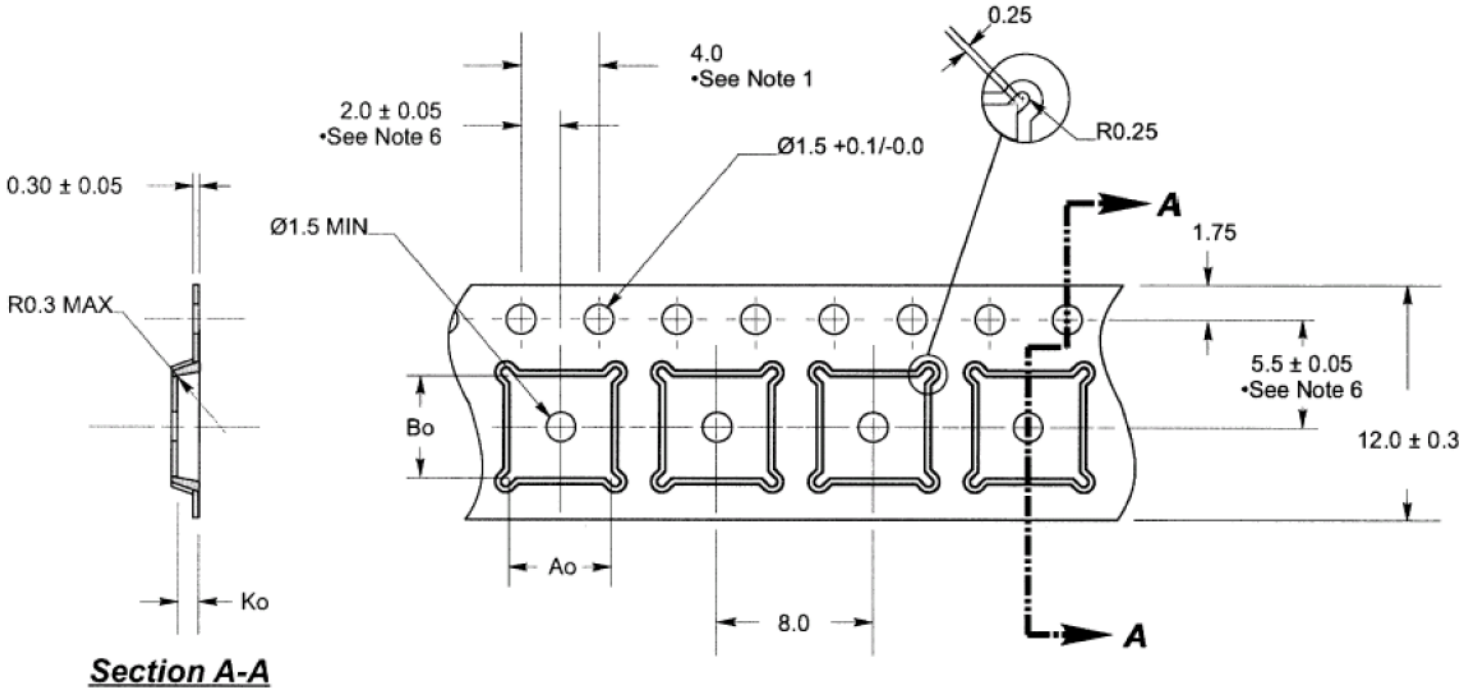


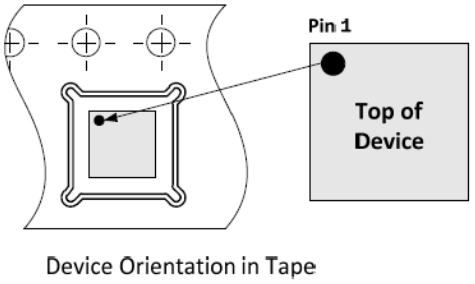
Figure 21. PE42420 package marking specification

Tape and reel specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.02.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm



Device Orientation in Tape

Figure 22. Tape and reel specification for the 20-lead 4 × 4 mm LGA package

Ordering information

Order code	Description	Packaging	Shipping method
PE42420F-Z	PE42420 SPDT RF switch	Green 20-lead 4 × 4 mm LGA	3000 units/T&R
EK42420-05	PE42420 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
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