**Freescale Semiconductor**
**Technical Data**

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# MPC850 PowerQUICC™ Integrated Communications Processor Hardware Specifications

This document contains detailed information on power considerations, AC/DC electrical characteristics, and AC timing specifications for revision A,B, and C of the MPC850 Family.

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## 1 Overview

The MPC850 is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. The MPC850, which includes support for Ethernet, is specifically designed for cost-sensitive, remote-access, and telecommunications applications. It is provides functions similar to the MPC860, with system enhancements such as universal serial bus (USB) support and a larger (8-Kbyte) dual-port RAM.

In addition to a high-performance embedded MPC8xx core, the MPC850 integrates system functions, such as a versatile memory controller and a communications processor module (CPM) that incorporates a specialized, independent RISC communications processor (referred to as the CP). This separate processor off-loads peripheral tasks from the embedded MPC8xx core.

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The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One $I^2C$ port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

**Table 1. MPC850 Functionality Matrix**

| Part | Number of SCCs Supported | Ethernet Support | ATM Support | USB Support | Multi-channel HDLC Support | Number of PCMCIA Slots Supported |
|---|---|---|---|---|---|---|
| MPC850 | 1 | Yes | - | Yes | - | 1 |
| MPC850DE | 2 | Yes | - | Yes | - | 1 |
| MPC850SR | 2 | Yes | Yes | Yes | Yes | 1 |
| MPC850DSL | 2 | Yes | Yes | Yes | No | 1 |

Additional documentation may be provided for parts listed in Table 1.

# 2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

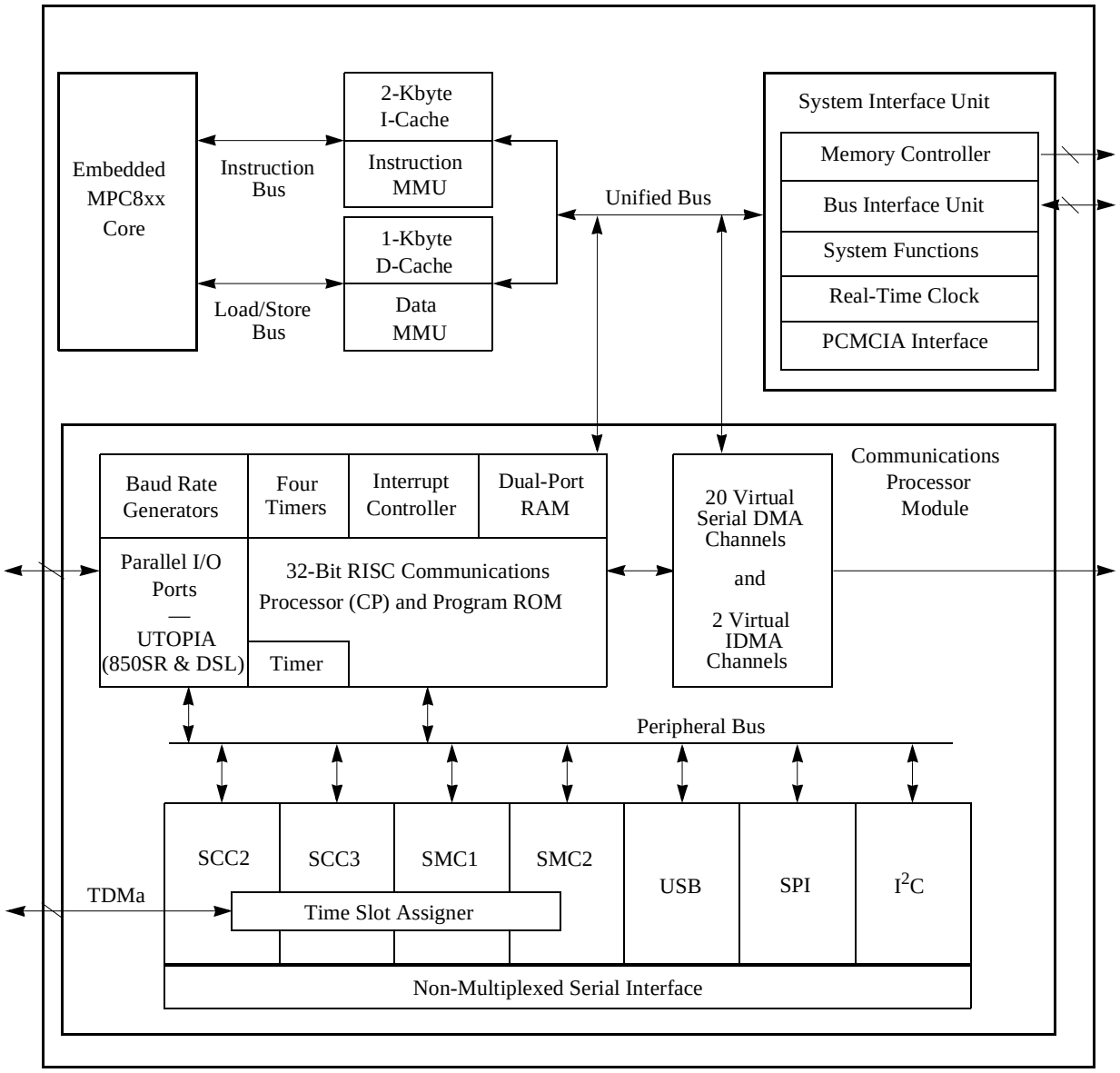



**Figure 1. MPC850 Microprocessor Block Diagram**

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

  - 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
    - Caches are two-way, set-associative
    - Physically addressed
    - Cache blocks can be updated with a 4-word line burst
    - Least-recently used (LRU) replacement algorithm
    - Lockable one-line granularity
  - Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
  - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
  - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
  - Memory controller programmable to support most size and speed memory interfaces
  - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
  - Variable block sizes, 32 Kbytes to 256 Mbytes
  - Selectable write protection
  - On-chip bus arbiter supports one external bus master
  - Special features for burst mode support
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One $I^2C^{®}$ (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

# 3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

**Table 2. Maximum Ratings**

(GND = 0V)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | VDDH | -0.3 to 4.0 | V |
| | VDDL | -0.3 to 4.0 | V |
| | KAPWR | -0.3 to 4.0 | V |
| | VDDSYN | -0.3 to 4.0 | V |
| Input voltage [1] | $V_{in}$ | GND-0.3 to VDDH + 2.5 V | V |
| Junction temperature [2] | $T_j$ | 0 to 95 (standard)<br>-40 to 95 (extended) | °C |
| Storage temperature range | $T_{stg}$ | -55 to +150 | °C |

1 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

2 The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$). Table 3 provides the package thermal characteristics for the MPC850.

# 4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

**Table 3. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal resistance for BGA [1] | $\theta_{JA}$ | 40 [2] | °C/W |
| | $\theta_{JA}$ | 31 [3] | °C/W |
| | $\theta_{JA}$ | 24 [4] | °C/W |
| Thermal Resistance for BGA (junction-to-case) | $\theta_{JC}$ | 8 | °C/W |

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

**Table 4. Power Dissipation ($P_D$)**

| Characteristic | Frequency (MHz) | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|
| Power Dissipation All Revisions (1:1) Mode | 33 | TBD | 515 | mW |
| | 40 | TBD | 590 | mW |
| | 50 | TBD | 725 | mW |

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

**Table 5. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage at 40 MHz or less | VDDH, VDDL, KAPWR, VDDSYN | 3.0 | 3.6 | V |
| Operating voltage at 40 MHz or higher | VDDH, VDDL, KAPWR, VDDSYN | 3.135 | 3.465 | V |
| Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals) | VIH | 2.0 | 3.6 | V |
| Input high voltage (all general purpose I/O and peripheral pins) | VIH | 2.0 | 5.5 | V |

**Table 5. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input low voltage | VIL | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | VIHC | 0.7*(VCC) | VCC+0.3 | V |
| Input leakage current, Vin = 5.5 V (Except TMS, TRST, DSCK and DSDI pins) | $I_{in}$ | — | 100 | µA |
| Input leakage current, Vin = 3.6V (Except TMS, TRST, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input leakage current, Vin = 0V (Except TMS, TRST, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance | $C_{in}$ | — | 20 | pF |
| Output high voltage, IOH = -2.0 mA, VDDH = 3.0V<br>except XTAL, XFC, and open-drain pins | VOH | 2.4 | — | V |
| Output low voltage<br>CLKOUT [3]<br>IOL = 3.2 mA [1]<br>IOL = 5.3 mA [2]<br>IOL = 7.0 mA PA[14]/USBOE, PA[12]/TXD2<br>IOL = 8.9 mA TS, TA, TEA, BI, BB, HRESET, SRESET | VOL | — | 0.5 | V |

1 A[6:31], TSIZ0/REG, TSIZ1, D[0:31], DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, PA[15]/USBRXD, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/USBRXP, PC[10]/TGATE1/USBRXN, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/USBTXP, PC[6]/USBTXN, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

2 BDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO

3 The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

# 5 Power Considerations

The average chip-junction temperature, $T_J$, in °C can be obtained from the equation:

$T_J = T_A + (P_D \bullet \theta_{JA})(1)$

where

$T_A$ = Ambient temperature, °C

$\theta_{JA}$ = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between $P_D$ and $T_J$ is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 5.1 Layout Practices

Each $V_{CC}$ pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

## Table 6. Bus Operation Timing [1]

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B1 | CLKOUT period | 20 | — | 30.30 | — | 25 | — | — | — | ns |
| B1a | EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2) | -0.90 | 0.90 | -0.90 | 0.90 | -0.90 | 0.90 | — | 50.00 | ns |
| B1b | EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10) | -2.30 | 2.30 | -2.30 | 2.30 | -2.30 | 2.30 | — | 50.00 | ns |
| B1c | CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [2] | -0.60 | 0.60 | -0.60 | 0.60 | -0.60 | 0.60 | — | 50.00 | ns |
| B1d | CLKOUT phase jitter [2] | -2.00 | 2.00 | -2.00 | 2.00 | -2.00 | 2.00 | — | 50.00 | ns |
| B1e | CLKOUT frequency jitter (MF < 10) [2] | — | 0.50 | — | 0.50 | — | 0.50 | — | 50.00 | % |
| B1f | CLKOUT frequency jitter (10 < MF < 500) [2] | — | 2.00 | — | 2.00 | — | 2.00 | — | 50.00 | % |
| B1g | CLKOUT frequency jitter (MF > 500) [2] | — | 3.00 | — | 3.00 | — | 3.00 | — | 50.00 | % |
| B1h | Frequency jitter on EXTCLK [3] | — | 0.50 | — | 0.50 | — | 0.50 | — | 50.00 | % |
| B2 | CLKOUT pulse width low | 8.00 | — | 12.12 | — | 10.00 | — | — | 50.00 | ns |
| B3 | CLKOUT width high | 8.00 | — | 12.12 | — | 10.00 | — | — | 50.00 | ns |
| B4 | CLKOUT rise time | — | 4.00 | — | 4.00 | — | 4.00 | — | 50.00 | ns |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 50.00 | ns |
| B7 | CLKOUT to A[6–31], RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3] invalid | 5.00 | — | 7.58 | — | 6.25 | — | 0.250 | 50.00 | ns |
| B7a | CLKOUT to TSIZ[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3], $\overline{BDIP}$, $\overline{PTR}$ invalid | 5.00 | — | 7.58 | — | 6.25 | — | 0.250 | 50.00 | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], $\overline{STS}$ invalid [4] | 5.00 | — | 7.58 | — | 6.25 | — | 0.250 | 50.00 | ns |
| B8 | CLKOUT to A[6–31], RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3] valid | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B8a | CLKOUT to TSIZ[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3] $\overline{BDIP}$, $\overline{PTR}$ valid | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B8b | CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], $\overline{STS}$ valid [4] | 5.00 | 11.74 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B9 | CLKOUT to A[6–31] RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3], $\overline{TSIZ}$[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3], $\overline{PTR}$ high-Z | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B11 | CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion | 5.00 | 11.00 | 7.58 | 13.58 | 6.25 | 12.25 | 0.250 | 50.00 | ns |
| B11a | CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion, (When driven by the memory controller or PCMCIA interface) | 2.50 | 9.25 | 2.50 | 9.25 | 2.50 | 9.25 | — | 50.00 | ns |
| B12 | CLKOUT to $\overline{TS}$, $\overline{BB}$ negation | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B12a | CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) | 2.50 | 11.00 | 2.50 | 11.00 | 2.50 | 11.00 | — | 50.00 | ns |
| B13 | CLKOUT to $\overline{TS}$, $\overline{BB}$ high-Z | 5.00 | 19.00 | 7.58 | 21.58 | 6.25 | 20.25 | 0.250 | 50.00 | ns |
| B13a | CLKOUT to $\overline{TA}$, $\overline{BI}$ high-Z, (when driven by the memory controller or PCMCIA interface) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | — | 50.00 | ns |
| B14 | CLKOUT to $\overline{TEA}$ assertion | 2.50 | 10.00 | 2.50 | 10.00 | 2.50 | 10.00 | — | 50.00 | ns |
| B15 | CLKOUT to $\overline{TEA}$ high-Z | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | — | 50.00 | ns |
| B16 | $\overline{TA}$, $\overline{BI}$ valid to CLKOUT(setup time) [5] | 9.75 | — | 9.75 | — | 9.75 | — | — | 50.00 | ns |
| B16a | $\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, valid to CLKOUT (setup time) [5] | 10.00 | — | 10.00 | — | 10.00 | — | — | 50.00 | ns |
| B16b | $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid to CLKOUT (setup time) [6] | 8.50 | — | 8.50 | — | 8.50 | — | — | 50.00 | ns |
| B17 | CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (Hold time).[5] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B17a | CLKOUT to $\overline{KR}$, $\overline{RETRY}$, except $\overline{TEA}$ valid (hold time) | 2.00 | — | 2.00 | — | 2.00 | — | — | 50.00 | ns |
| B18 | D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) [7] | 6.00 | — | 6.00 | — | 6.00 | — | — | 50.00 | ns |
| B19 | CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) [7] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B20 | D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) [8] | 4.00 | — | 4.00 | — | 4.00 | — | — | 50.00 | ns |
| B21 | CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) [8] | 2.00 | — | 2.00 | — | 2.00 | — | — | — | — |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B22 | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0,1 | — | 8.00 | — | 8.00 | — | 8.00 | — | 50.00 | ns |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 | 7.00 | 14.00 | 11.00 | 18.00 | 9.00 | 16.00 | 0.375 | 50.00 | ns |
| B23 | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | — | 50.00 | ns |
| B24 | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0. | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B24a | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B25 | CLKOUT rising edge to $\overline{OE}$, $\overline{WE[0–3]}$ asserted | — | 9.00 | — | 9.00 | — | 9.00 | — | 50.00 | ns |
| B26 | CLKOUT rising edge to $\overline{OE}$ negated | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | — | 50.00 | ns |
| B27 | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 | 23.00 | — | 36.00 | — | 29.00 | — | 1.250 | 50.00 | ns |
| B27a | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B28 | CLKOUT rising edge to $\overline{WE[0–3]}$ negated GPCM write access CSNT = 0 | — | 9.00 | — | 9.00 | — | 9.00 | — | 50.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE[0–3]}$ negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | — | 12.00 | — | 14.00 | — | 13.00 | 0.250 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B28c | CLKOUT falling edge to $\overline{\text{WE[0–3]}}$ negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 | 7.00 | 14.00 | 11.00 | 18.00 | 9.00 | 16.00 | 0.375 | 50.00 | ns |
| B28d | CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | — | 14.00 | — | 18.00 | — | 16.00 | 0.375 | 50.00 | ns |
| B29 | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, CSNT = 0 | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B29a | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B29b | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B29c | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B29d | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B29e | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B29f | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1 | 5.00 | — | 9.00 | — | 7.00 | — | 0.375 | 50.00 | ns |
| B29g | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 5.00 | — | 9.00 | — | 7.00 | — | 0.375 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B29h | $\overline{WE}$[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |
| B29i | $\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |
| B30 | $\overline{CS}$, $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access [9] | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B30a | $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B30b | $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B30c | $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 5.00 | — | 8.00 | — | 6.00 | — | 0.375 | 50.00 | ns |
| B30d | $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B31 | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B32 | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B33 | CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B33a | CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B34 | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B34a | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B34b | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B35 | A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B35a | A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B35b | A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B36 | A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B37 | UPWAIT valid to CLKOUT falling edge [10] | 6.00 | — | 6.00 | — | 6.00 | — | — | 50.00 | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [10] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge [11] | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B40 | A[6–31], TSIZ[0–1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge. | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) | 2.00 | — | 2.00 | — | 2.00 | — | — | 50.00 | ns |
| B43 | $\overline{AS}$ negation to memory controller signals negation | — | TBD | — | TBD | TBD | — | — | 50.00 | ns |

1 The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR) + 1ns(CAP\ LOAD - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

$D_{50}$ is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

2 Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

3 If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

4 The timing for $\overline{BR}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

5 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

6 The timing required for $\overline{BR}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

7 The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

8 The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

9 The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.

10 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

11 The $\overline{AS}$ signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.

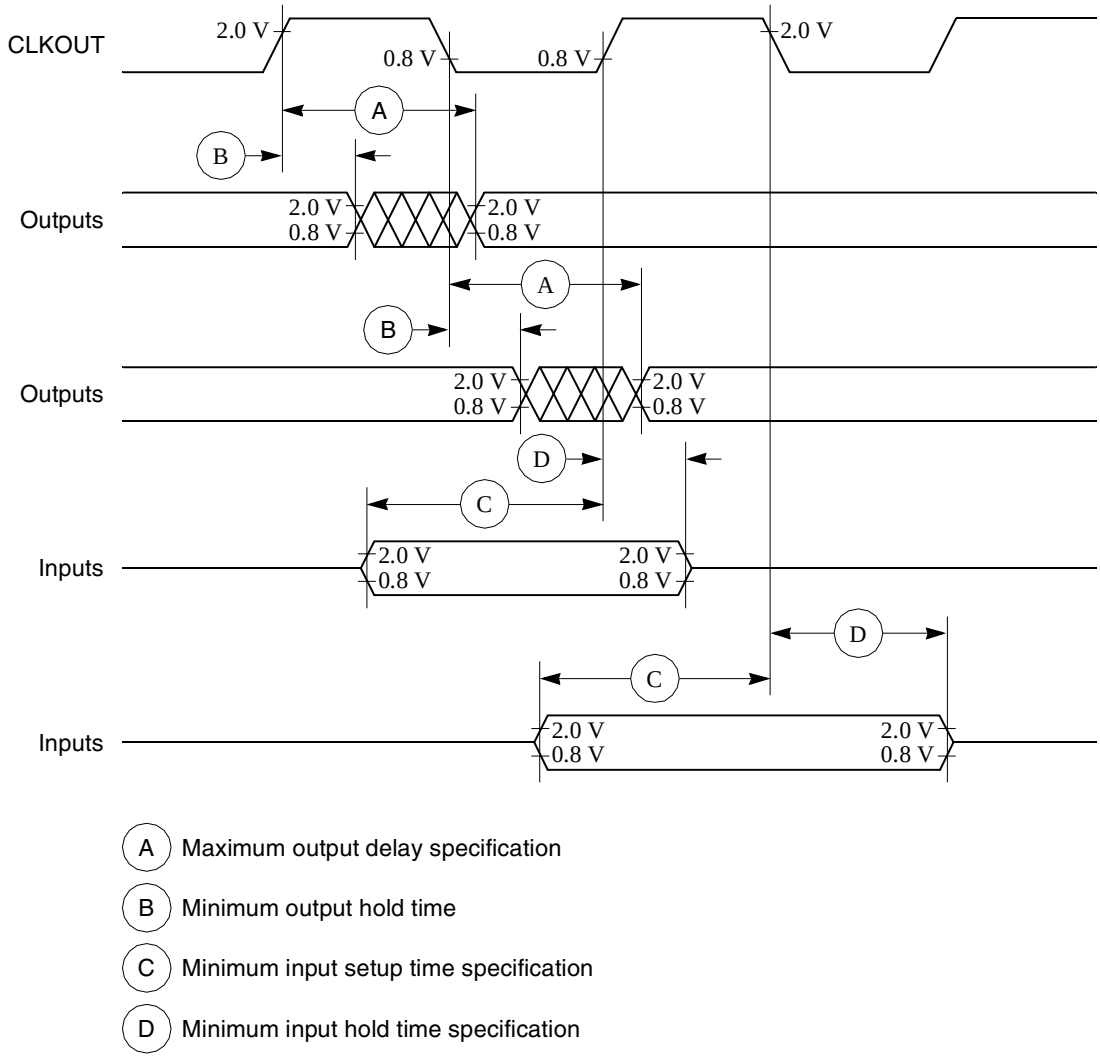



**Figure 2. Control Timing**

Figure 3 provides the timing for the external clock.

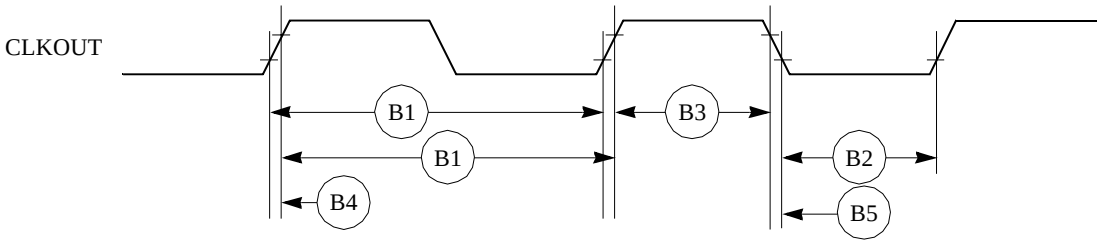



**Figure 3. External Clock Timing**

Figure 4 provides the timing for the synchronous output signals.

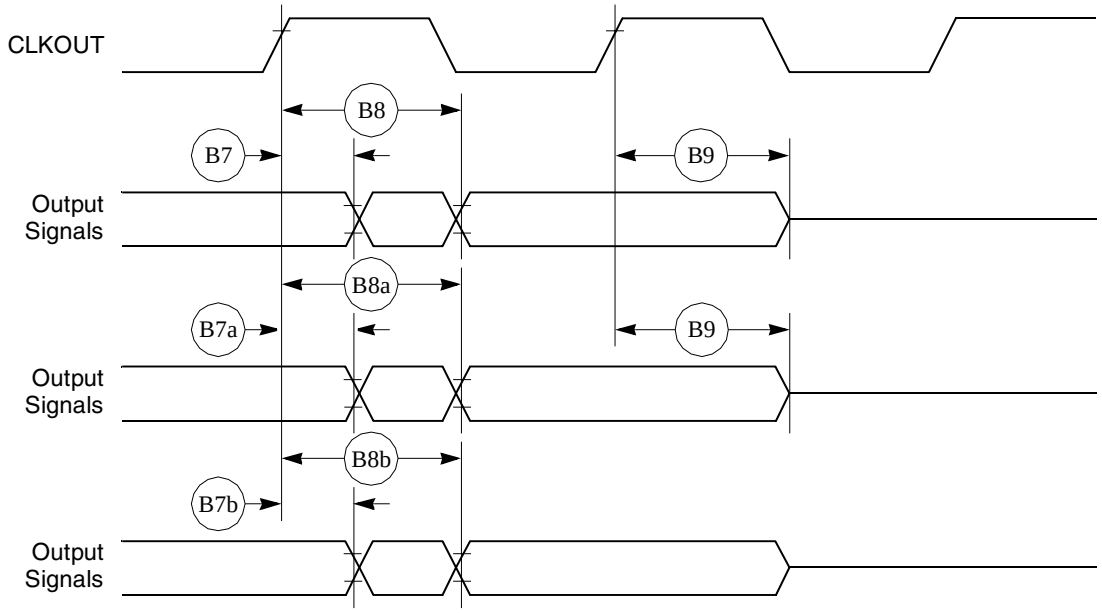



**Figure 4. Synchronous Output Signals Timing**

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

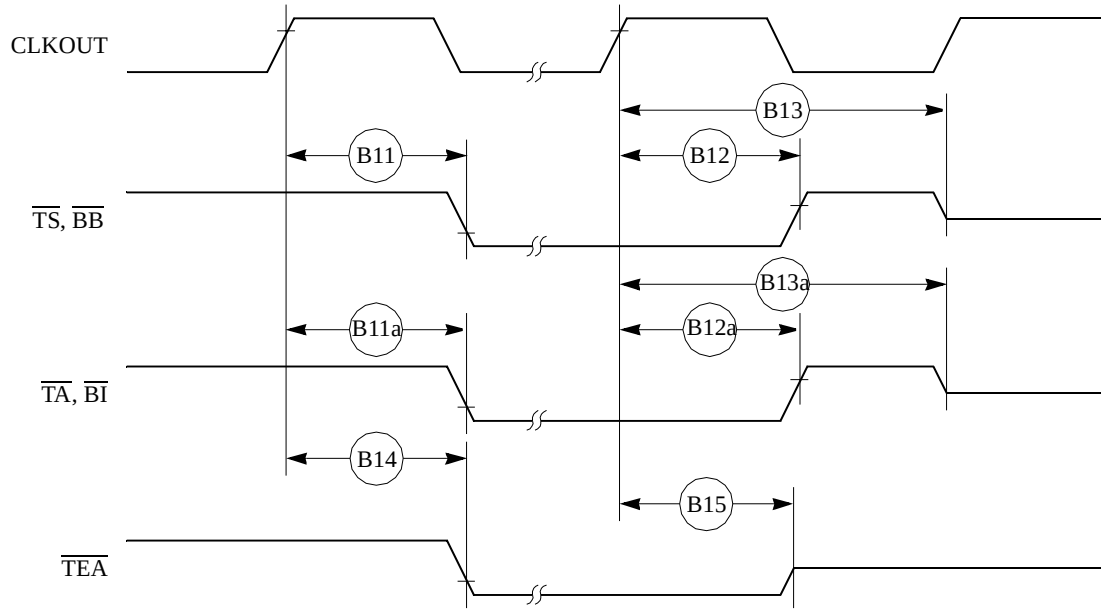



**Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing**

Figure 6 provides the timing for the synchronous input signals.

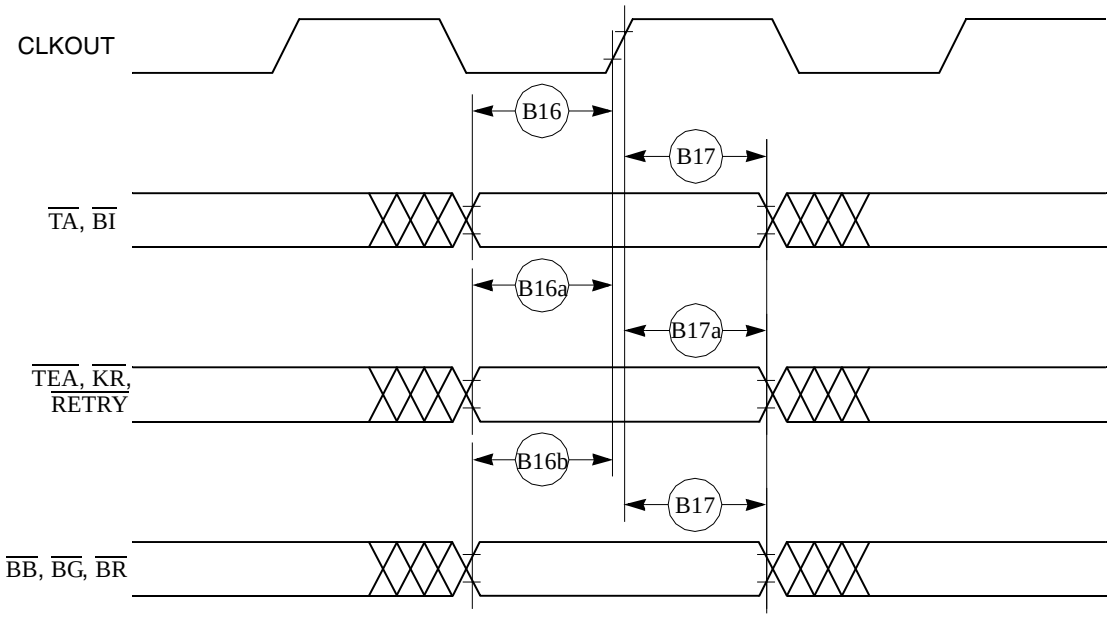



**Figure 6. Synchronous Input Signals Timing**

Figure 7 provides normal case timing for input data.

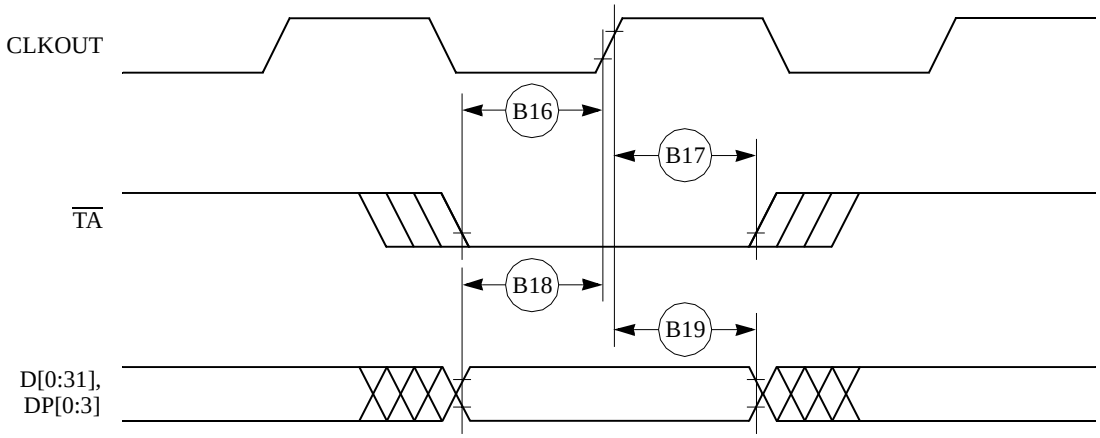



**Figure 7. Input Data Timing in Normal Case**

Figure 8 provides the timing for the input data controlled by the UPM in the memory controller.

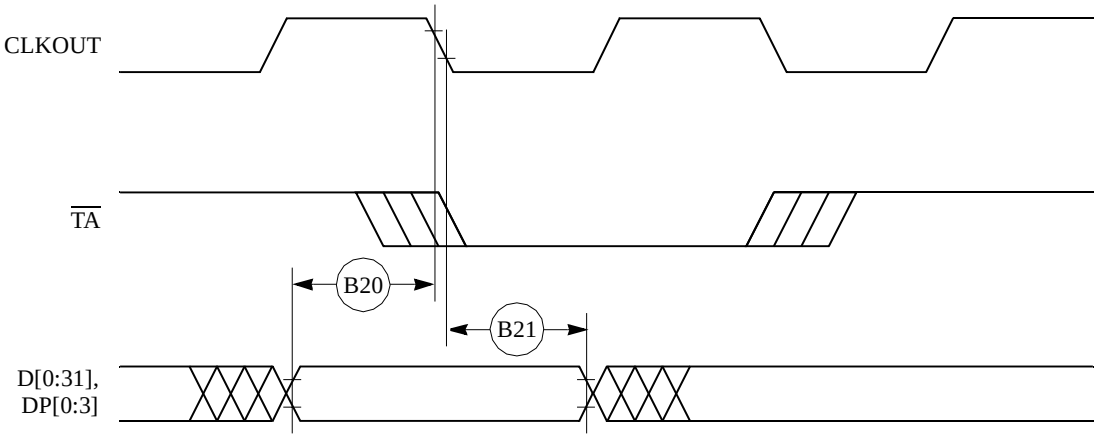



**Figure 8. Input Data Timing when Controlled by UPM in the Memory Controller**

Figure 9 through Figure 12 provide the timing for the external bus read controlled by various GPCM factors.

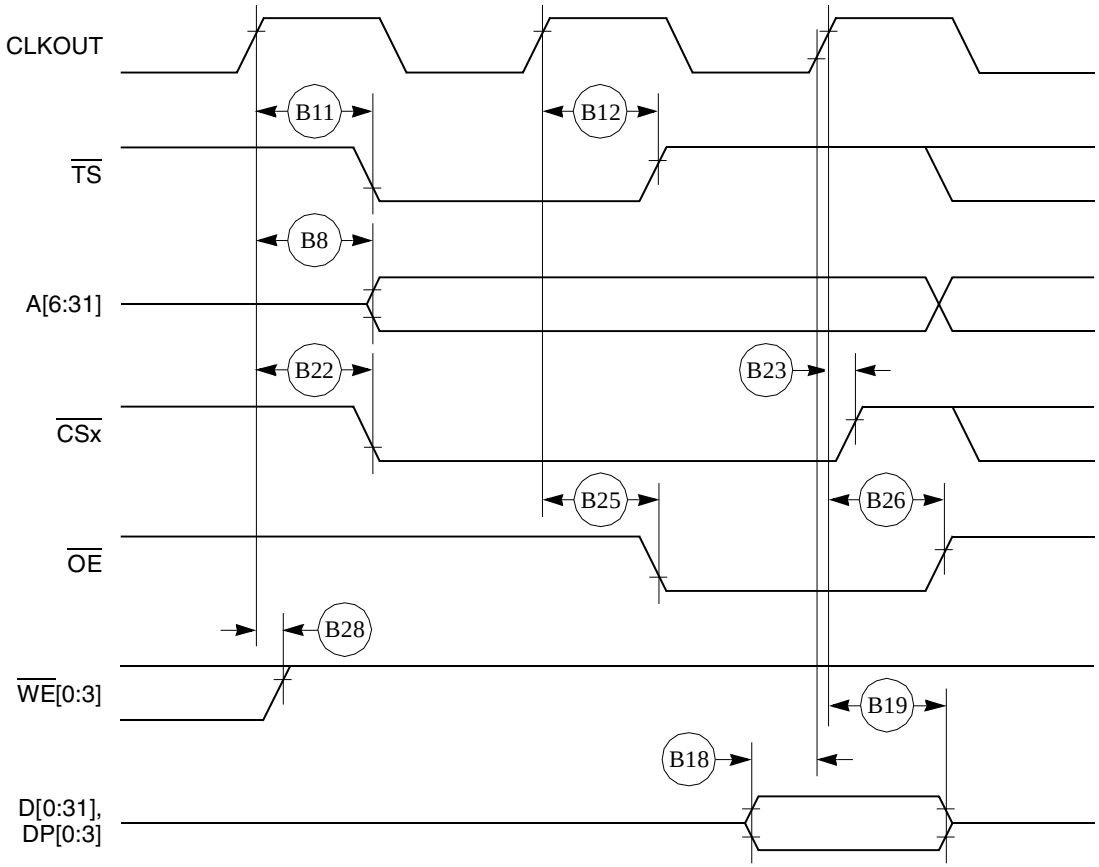



**Figure 9. External Bus Read Timing (GPCM Controlled—ACS = 00)**

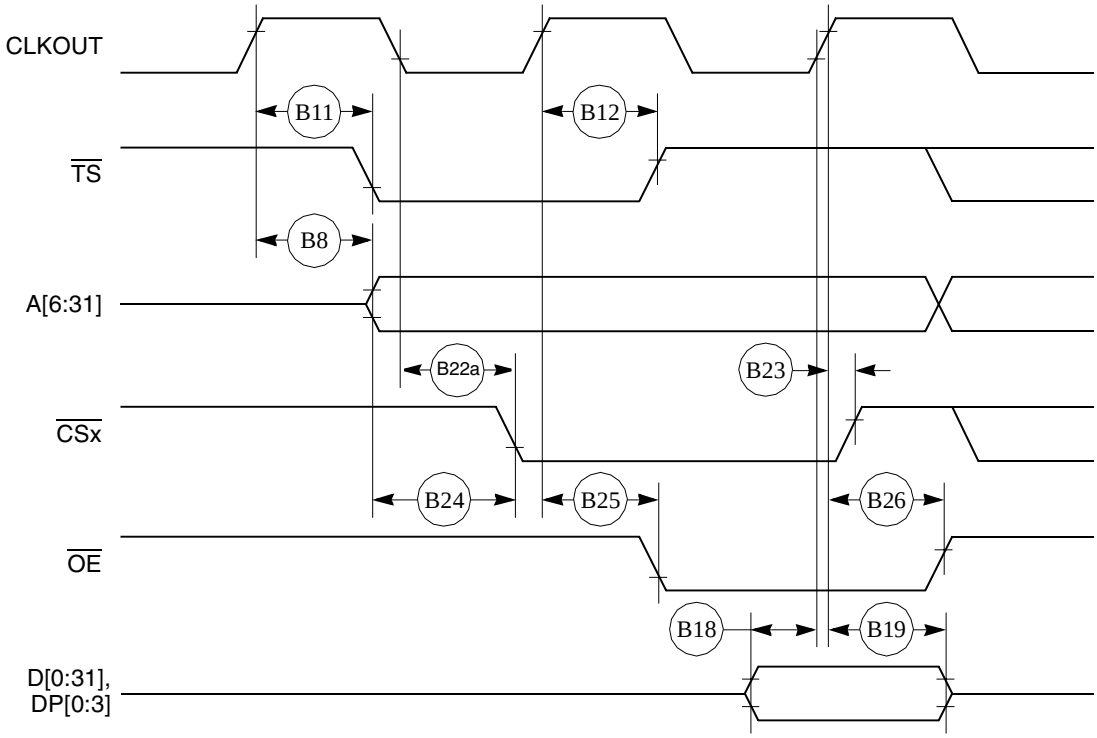



**Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)**

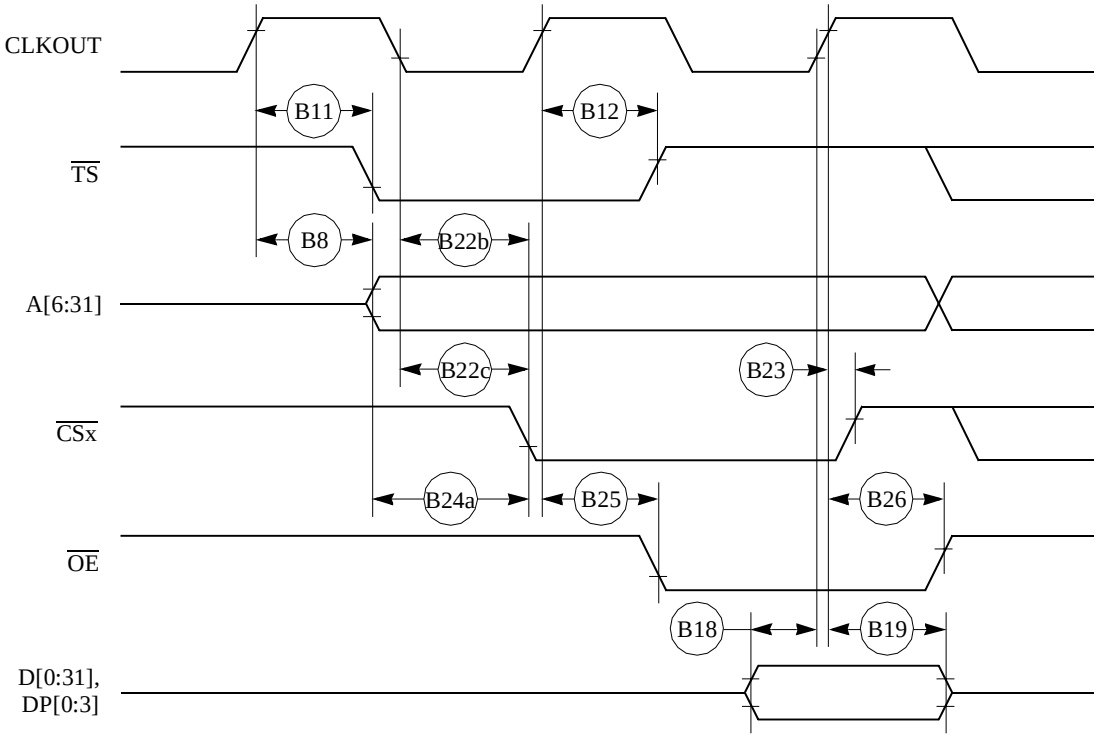



**Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

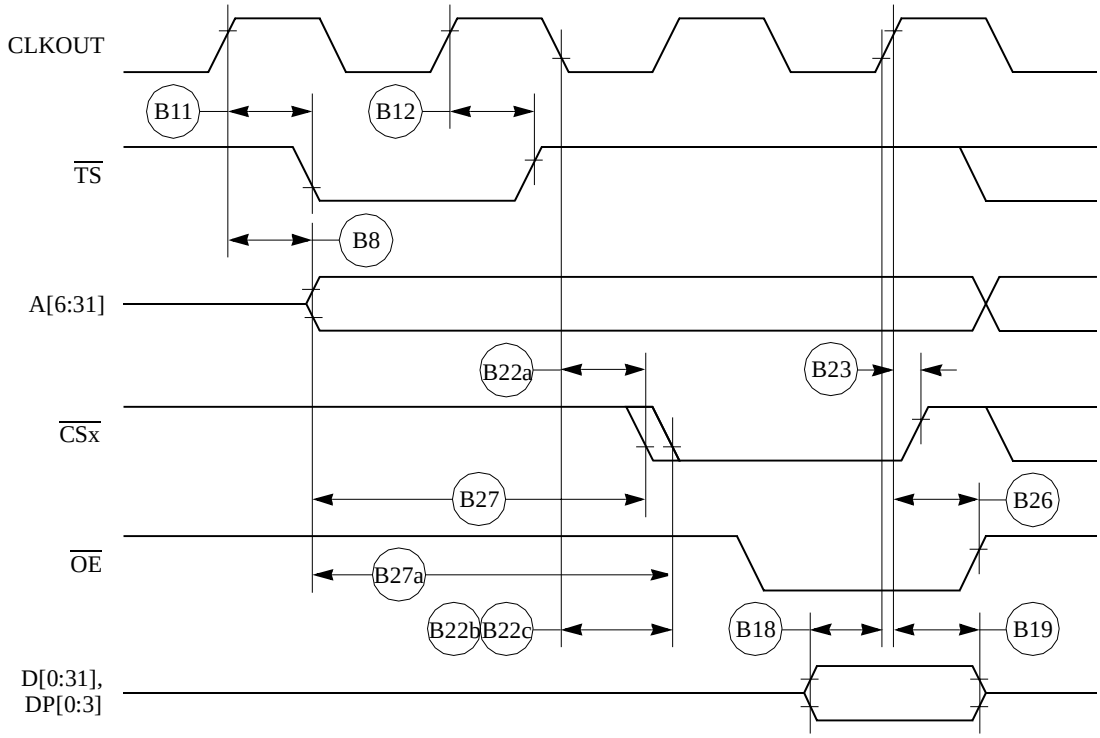



**Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)**

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

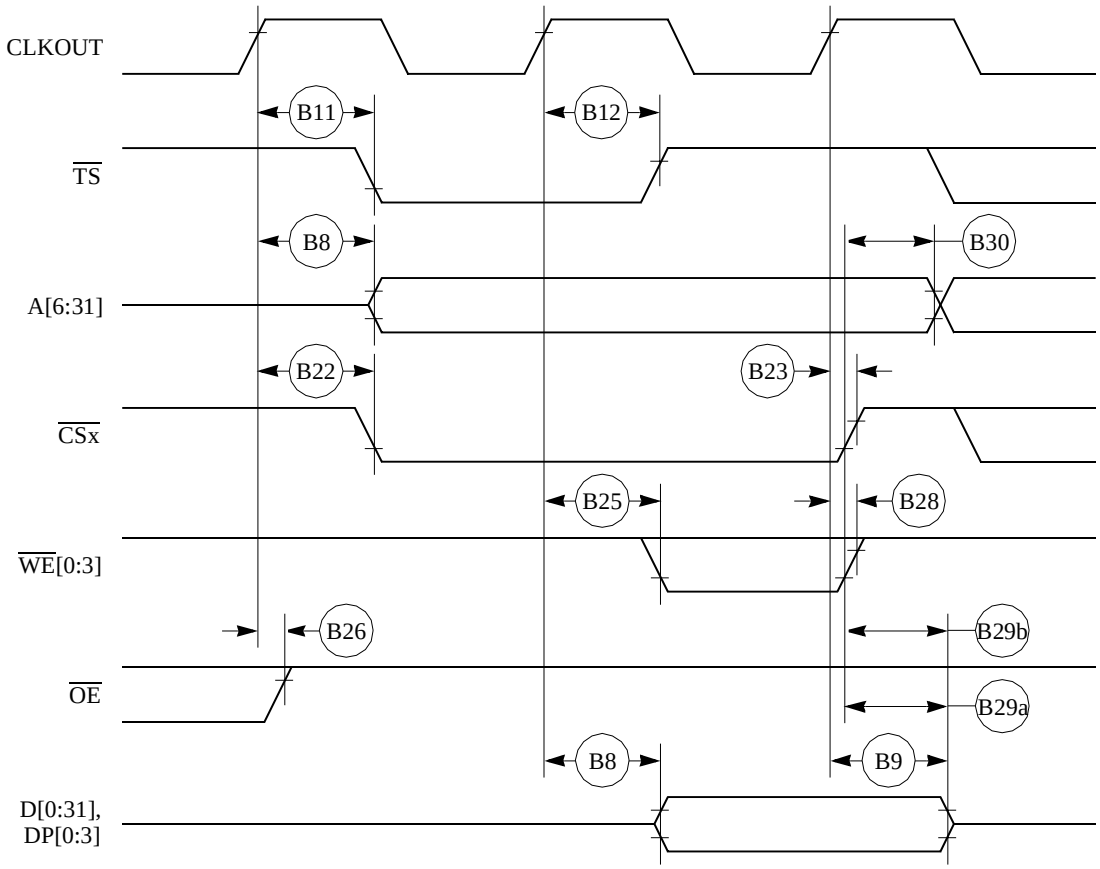



**Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)**

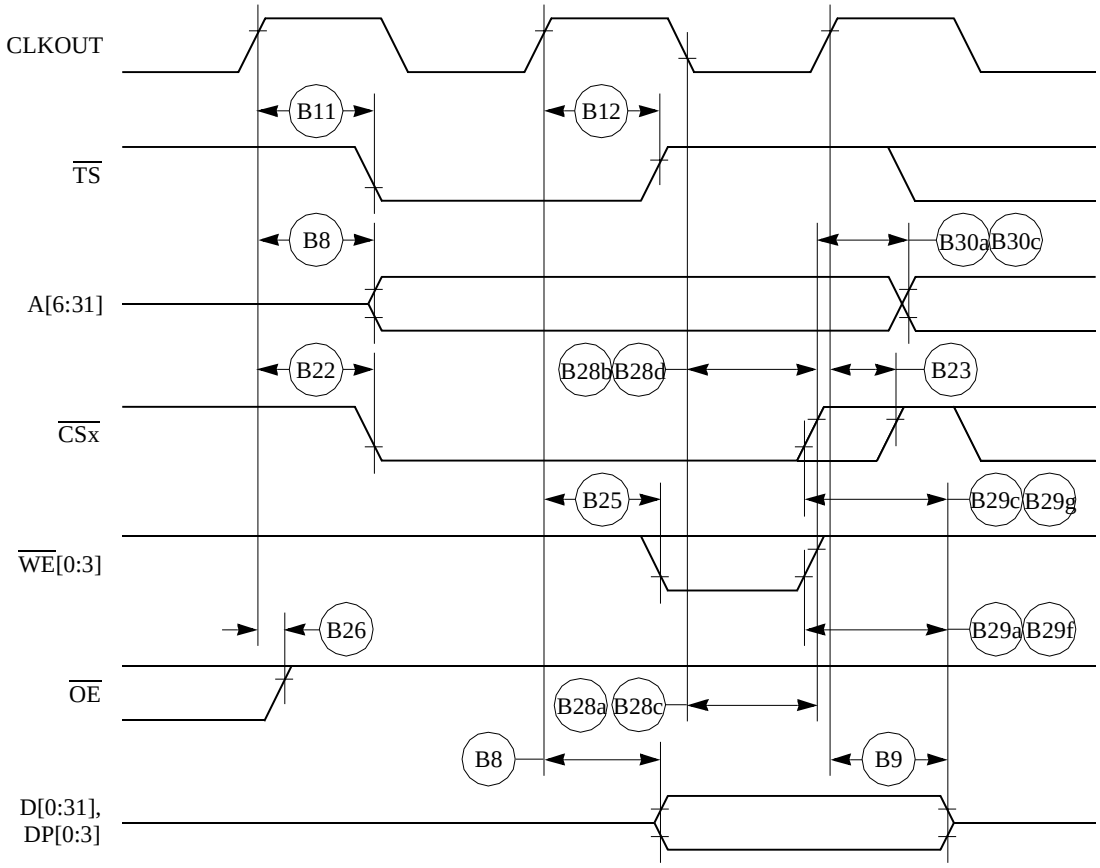



**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

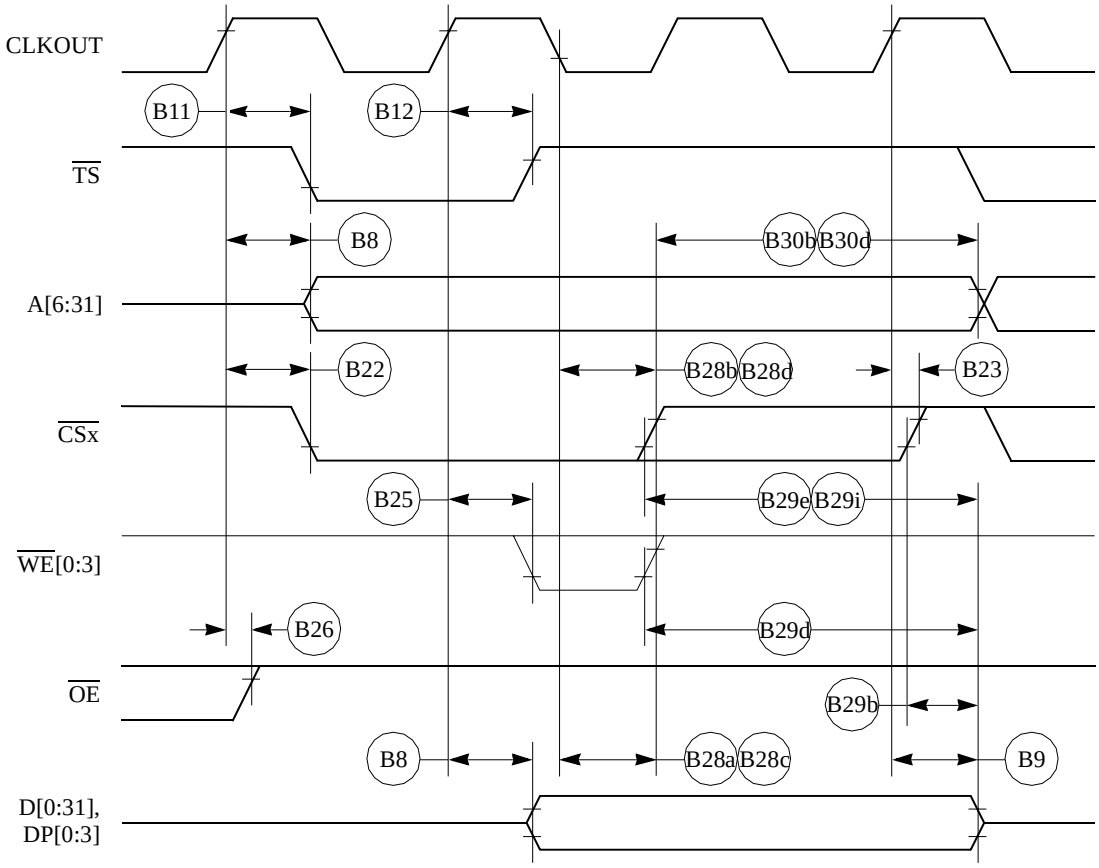



**Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)**

Figure 16 provides the timing for the external bus controlled by the UPM.

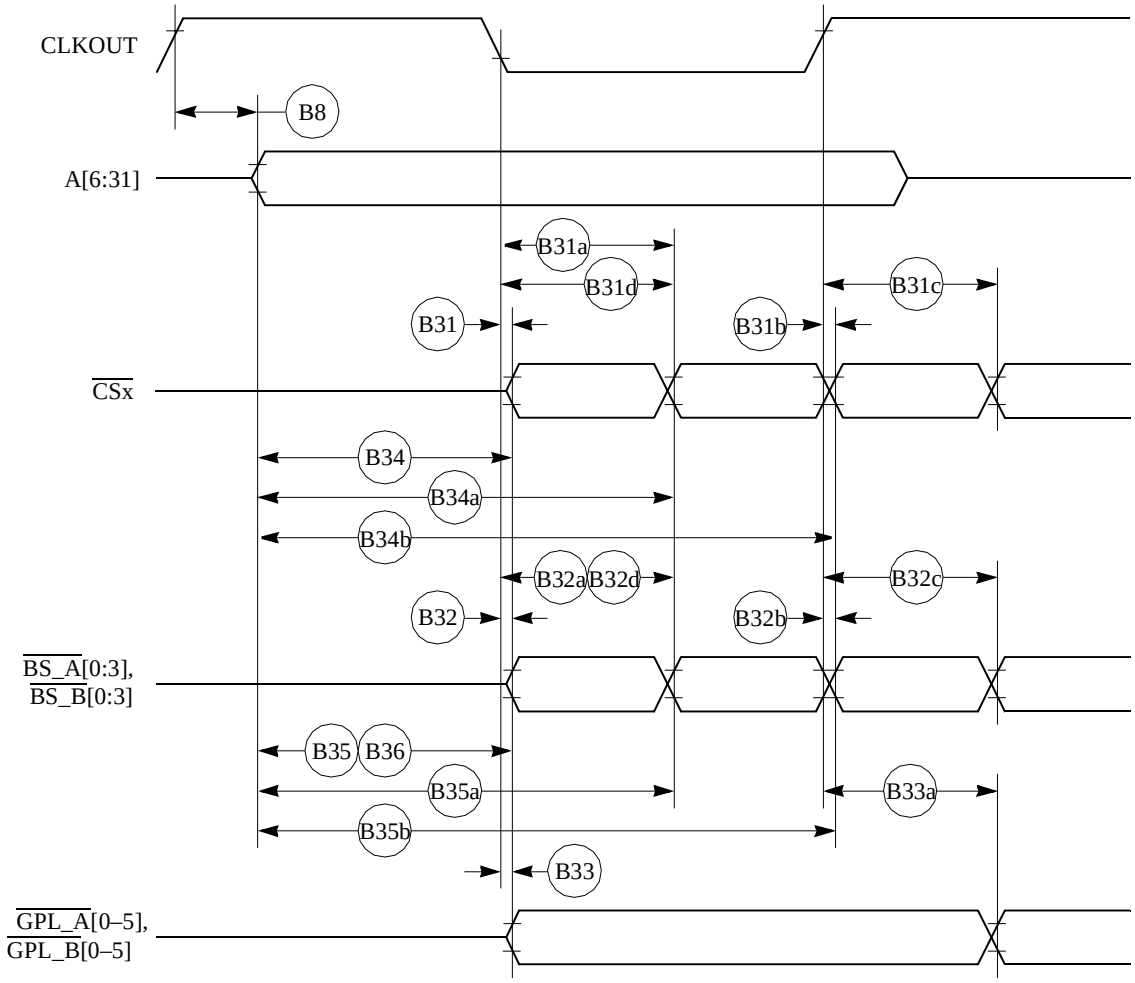



**Figure 16. External Bus Timing (UPM Controlled Signals)**

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

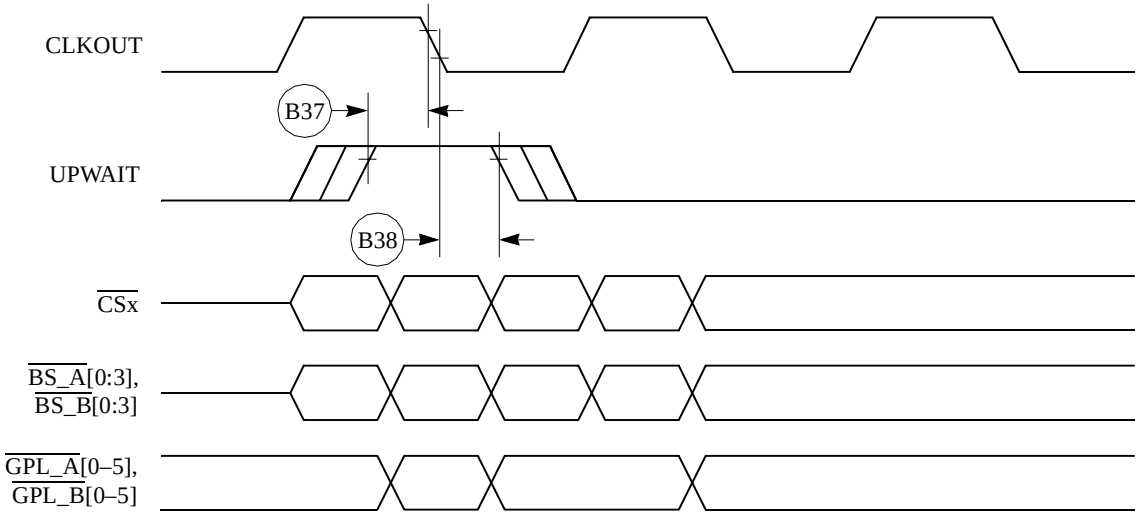



**Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

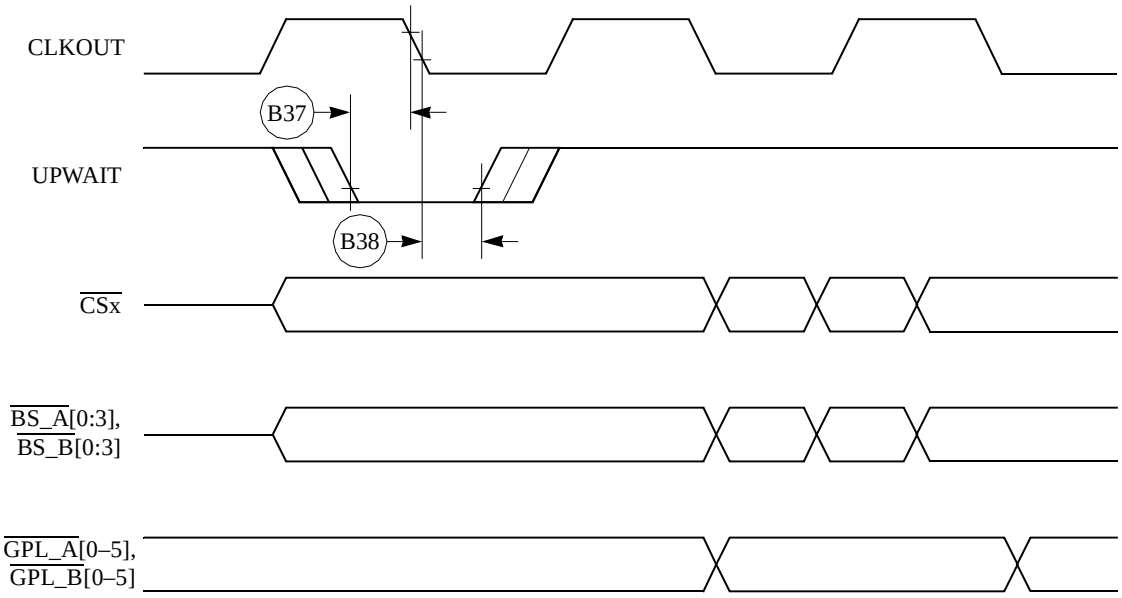



**Figure 18. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

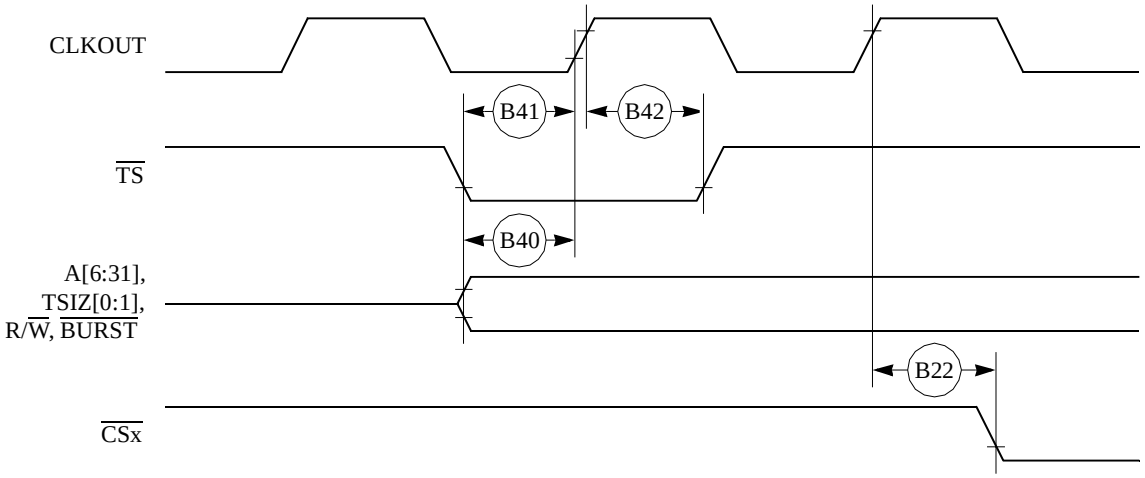



**Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

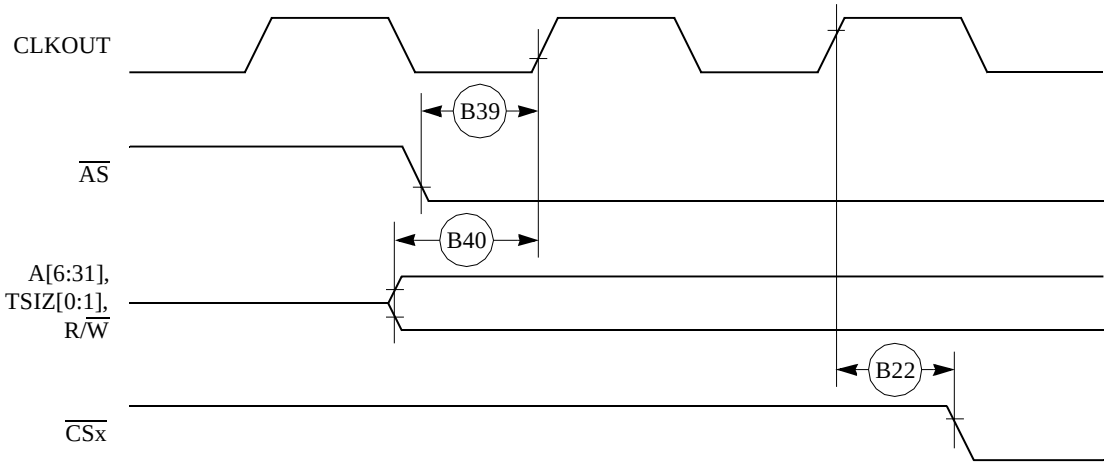



**Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 21 provides the timing for the asynchronous external master control signals negation.

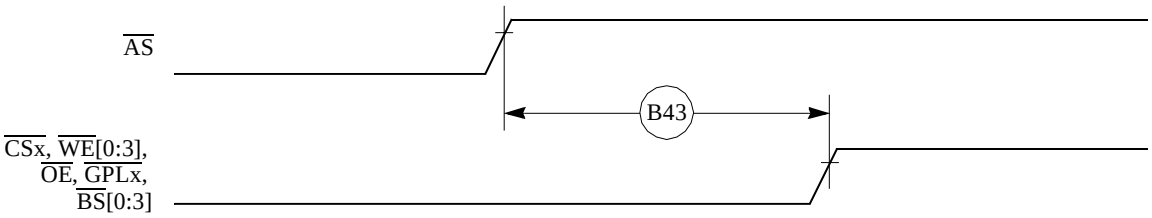



**Figure 21. Asynchronous External Master—Control Signals Negation Timing**

Table 7 provides interrupt timing for the MPC850.

**Table 7. Interrupt Timing**

| Num | Characteristic [1] | 50 MHz | | 66MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| I39 | $\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time) | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| I40 | $\overline{\text{IRQx}}$ hold time after CLKOUT. | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| I41 | $\overline{\text{IRQx}}$ pulse width low | 3.00 | — | 3.00 | — | 3.00 | — | ns |
| I42 | $\overline{\text{IRQx}}$ pulse width high | 3.00 | — | 3.00 | — | 3.00 | — | ns |
| I43 | $\overline{\text{IRQx}}$ edge-to-edge time | 80.00 | — | 121.0 | — | 100.0 | — | ns |

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

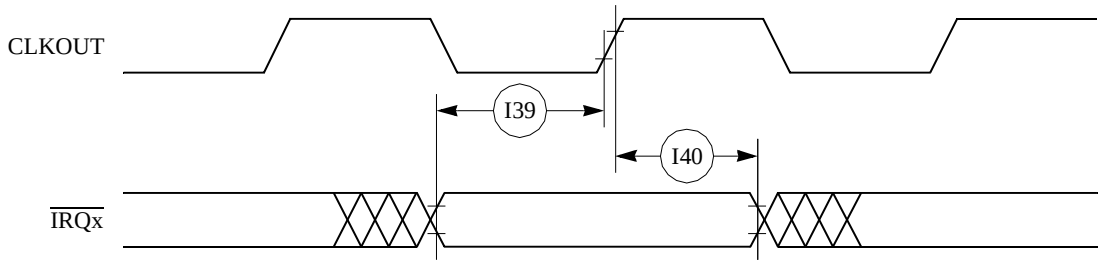



**Figure 22. Interrupt Detection Timing for External Level Sensitive Lines**

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

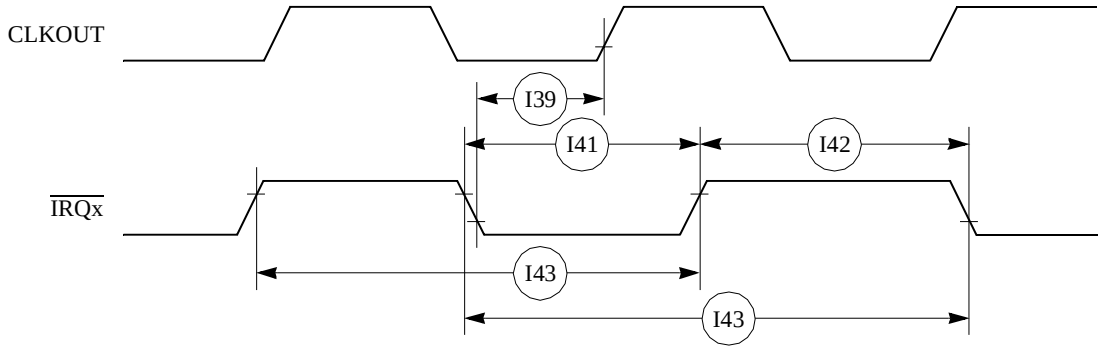



**Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines**

Table 8 shows the PCMCIA timing for the MPC850.

**Table 8. PCMCIA Timing**

| Num | Characteristic | 50MHz | | 66MHz | | 80 MHz | | FFACTOR | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| P44 | A[6–31], REG valid to PCMCIA strobe asserted. [1] | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | ns |
| P45 | A[6–31], REG valid to ALE negation.[1] | 18.00 | — | 28.00 | — | 23.00 | — | 1.000 | ns |
| P46 | CLKOUT to REG valid | 5.00 | 13.00 | 8.00 | 16.00 | 6.00 | 14.00 | 0.250 | ns |
| P47 | CLKOUT to REG Invalid. | 6.00 | — | 9.00 | — | 7.00 | — | 0.250 | ns |
| P48 | CLKOUT to CE1, CE2 asserted. | 5.00 | 13.00 | 8.00 | 16.00 | 6.00 | 14.00 | 0.250 | |
| P49 | CLKOUT to CE1, CE2 negated. | 5.00 | 13.00 | 8.00 | 16.00 | 6.00 | 14.00 | 0.250 | ns |
| P50 | CLKOUT to PCOE, IORD, PCWE, IOWR assert time. | — | 11.00 | — | 11.00 | — | 11.00 | — | ns |
| P51 | CLKOUT to PCOE, IORD, PCWE, IOWR negate time. | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | — | ns |
| P52 | CLKOUT to ALE assert time | 5.00 | 13.00 | 8.00 | 16.00 | 6.00 | 14.00 | 0.250 | ns |
| P53 | CLKOUT to ALE negate time | — | 13.00 | — | 16.00 | — | 14.00 | 0.250 | ns |
| P54 | PCWE, IOWR negated to D[0–31] invalid.[1] | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | ns |
| P55 | WAIT_B valid to CLKOUT rising edge.[1] | 8.00 | — | 8.00 | — | 8.00 | — | — | ns |
| P56 | CLKOUT rising edge to WAIT_B invalid.[1] | 2.00 | — | 2.00 | — | 2.00 | — | — | ns |

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAIT_B signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The WAIT_B assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

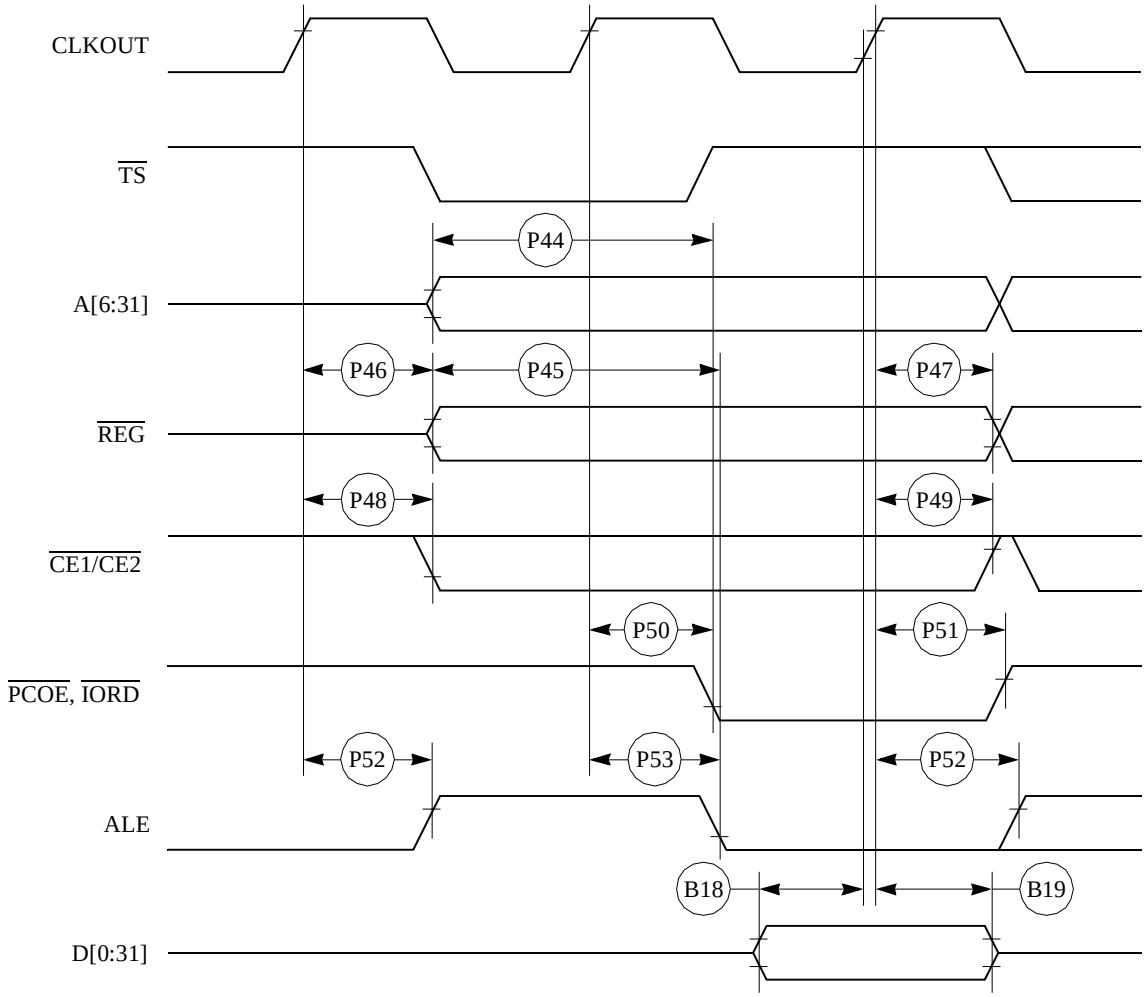



**Figure 24. PCMCIA Access Cycles Timing External Bus Read**

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

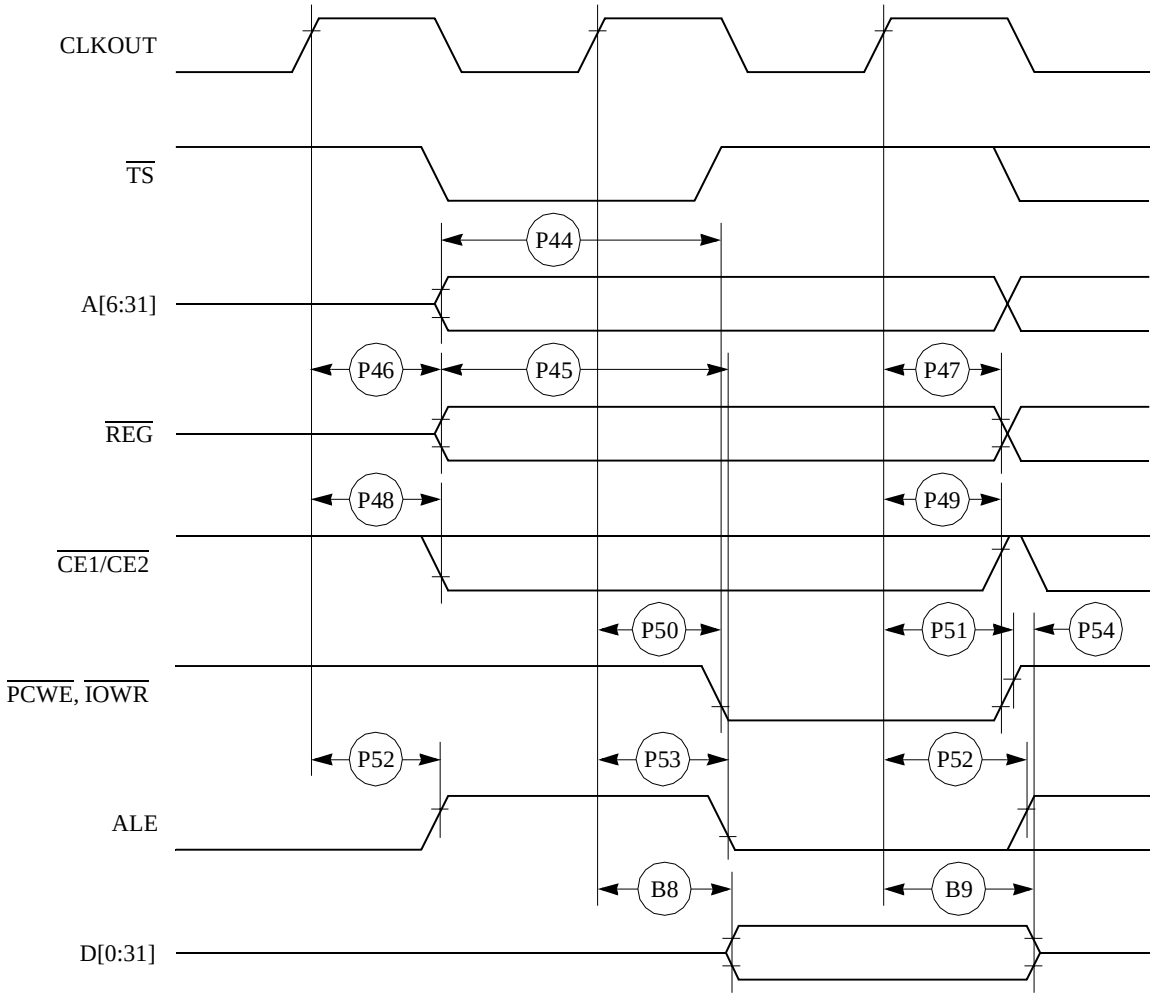



**Figure 25. PCMCIA Access Cycles Timing External Bus Write**

Figure 26 provides the PCMCIA WAIT signals detection timing.

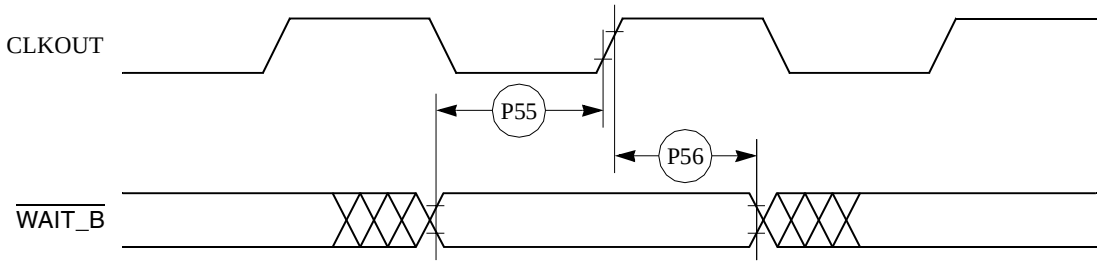



**Figure 26. PCMCIA WAIT Signal Detection Timing**

Table 9 shows the PCMCIA port timing for the MPC850.

**Table 9. PCMCIA Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx valid | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive [1] | 18.00 | — | 26.00 | — | 22.00 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid | 1.00 | — | 1.00 | — | 1.00 | — | ns |

[1] OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

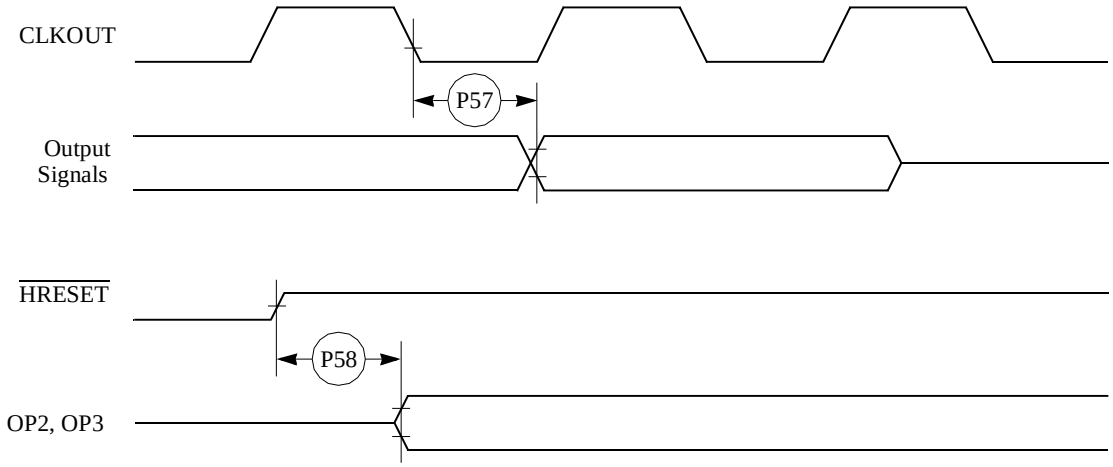



**Figure 27. PCMCIA Output Port Timing**

Figure 28 provides the PCMCIA output port timing for the MPC850.

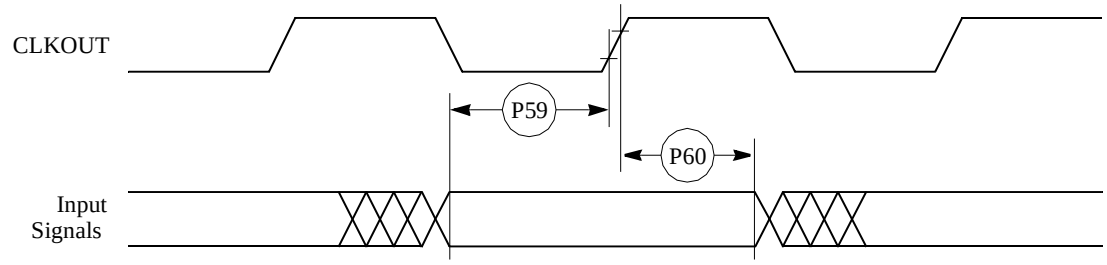



**Figure 28. PCMCIA Input Port Timing**

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| D61 | DSCK cycle time | 60.00 | — | 91.00 | — | 75.00 | — | ns |
| D62 | DSCK clock pulse width | 25.00 | — | 38.00 | — | 31.00 | — | ns |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | 0.00 | 3.00 | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | 0.00 | 15.00 | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | 0.00 | 2.00 | 0.00 | 2.00 | ns |

Figure 29 provides the input timing for the debug port clock.

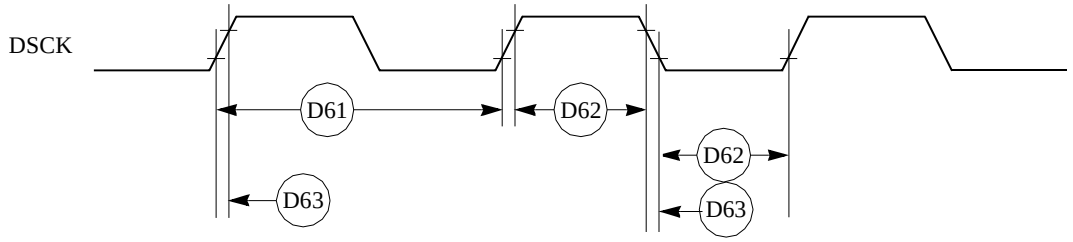



**Figure 29. Debug Port Clock Input Timing**

Figure 30 provides the timing for the debug port.

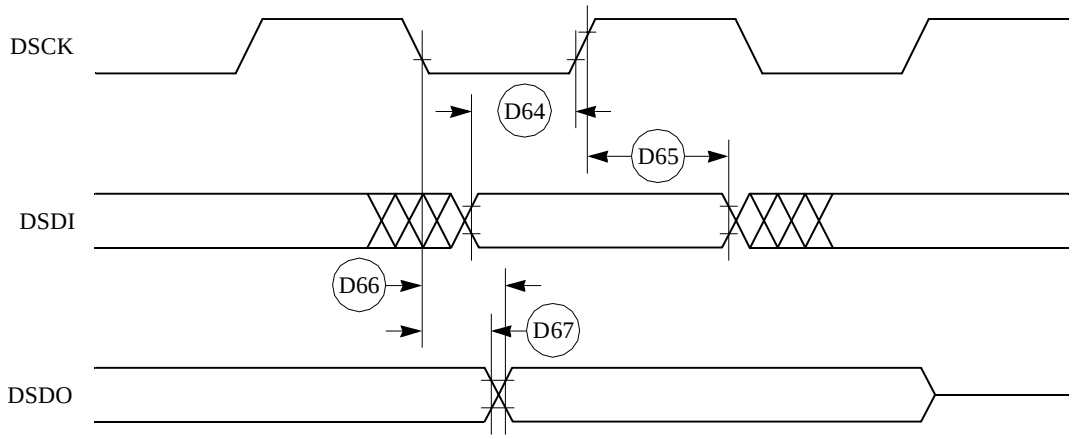



**Figure 30. Debug Port Timings**

Table 11 shows the reset timing for the MPC850.

**Table 11. Reset Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | FFACTOR | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width | 340.00 | — | 515.00 | — | 425.00 | — | 17.000 | ns |
| R72 | | — | — | — | — | — | — | — | |
| R73 | Configuration data to $\overline{\text{HRESET}}$ rising edge set up time | 350.00 | — | 505.00 | — | 425.00 | — | 15.000 | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time | 350.00 | — | 350.00 | — | 350.00 | — | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R79 | CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R80 | DSDI, DSCK set up | 60.00 | — | 90.00 | — | 75.00 | — | 3.000 | ns |
| R81 | DSDI, DSCK hold time | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample | 160.00 | — | 242.00 | — | 200.00 | — | 8.000 | ns |

Figure 31 shows the reset timing for the data bus configuration.

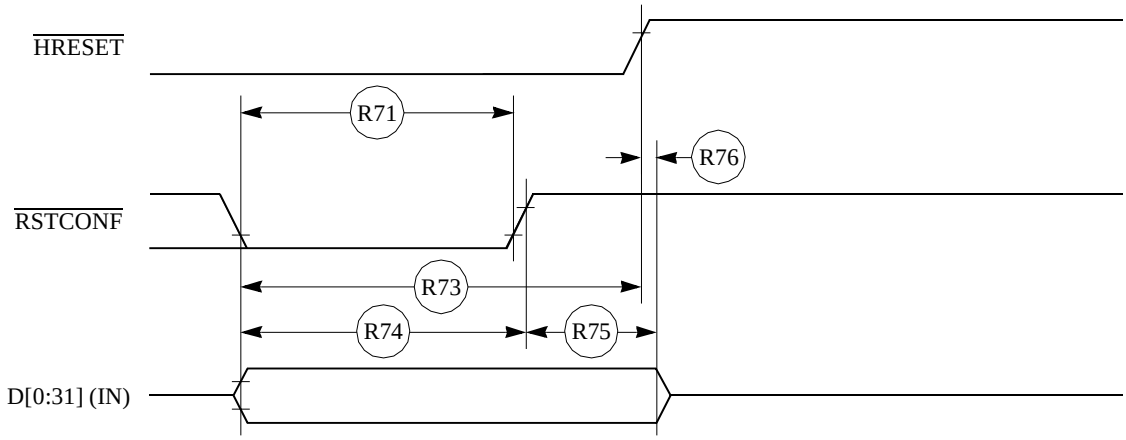



**Figure 31. Reset Timing—Configuration from Data Bus**

Figure 32 provides the reset timing for the data bus weak drive during configuration.

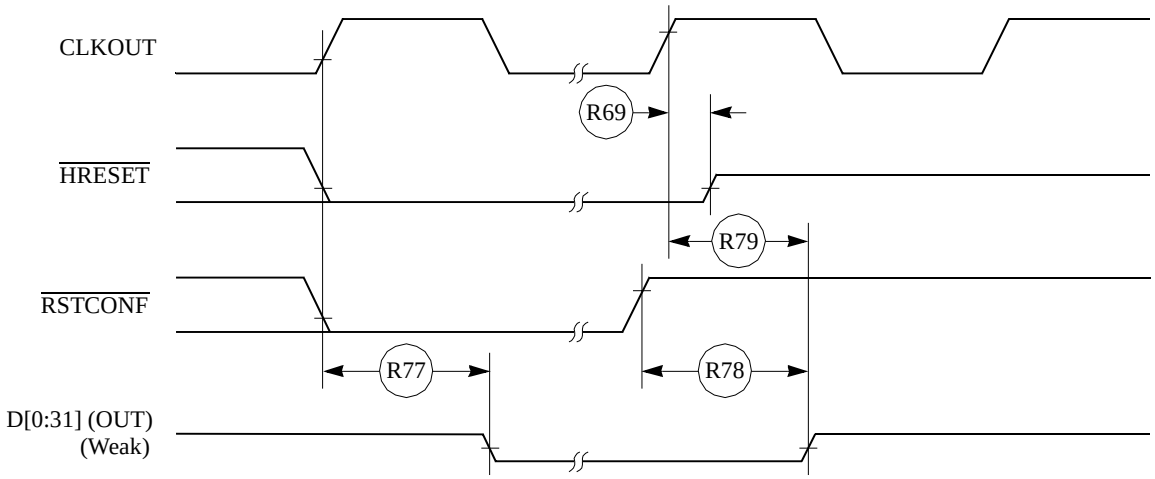



**Figure 32. Reset Timing—Data Bus Weak Drive during Configuration**

Figure 33 provides the reset timing for the debug port configuration.

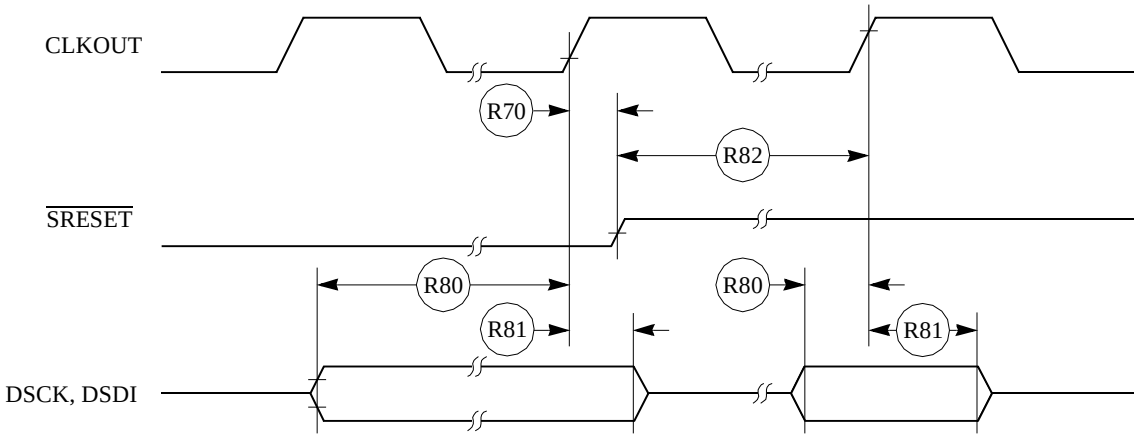



**Figure 33. Reset Timing—Debug Port Configuration**

# 7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

**Table 12. JTAG Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | 0.00 | 10.00 | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | — | 27.00 | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | 50.00 | — | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | 50.00 | — | 50.00 | — | ns |

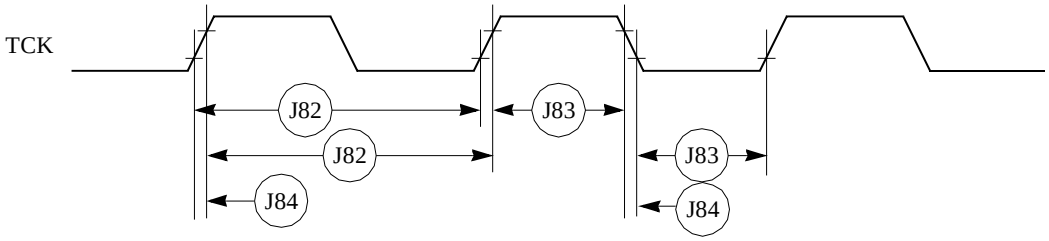



**Figure 34. JTAG Test Clock Input Timing**

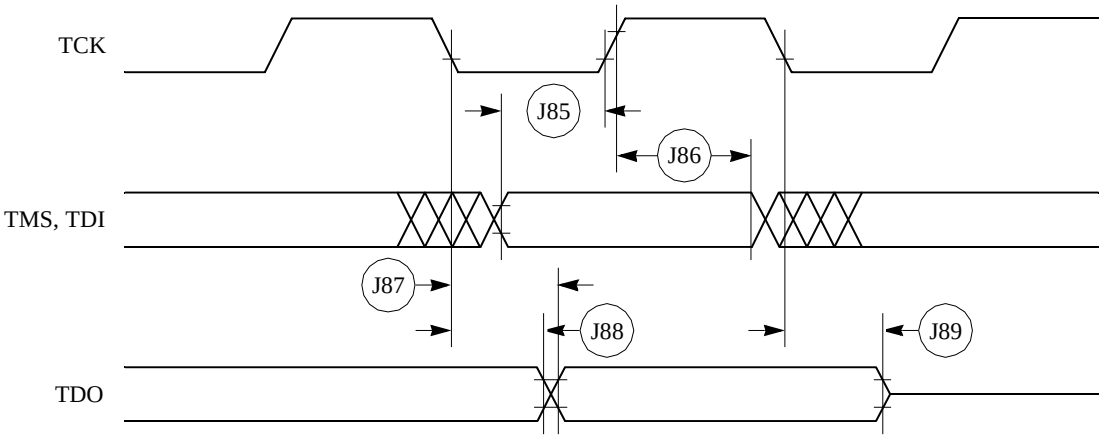



**Figure 35. JTAG Test Access Port Timing Diagram**

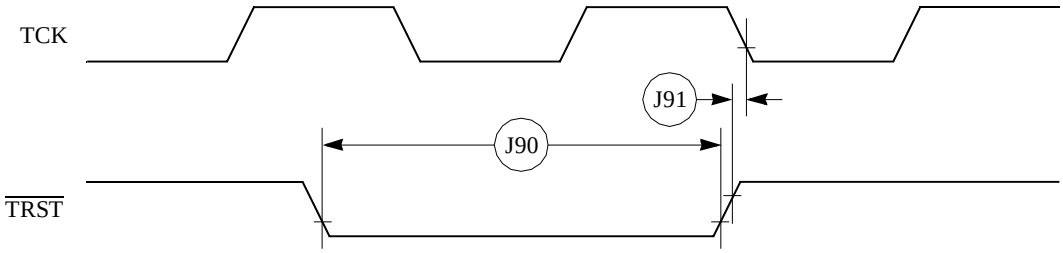



**Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram**

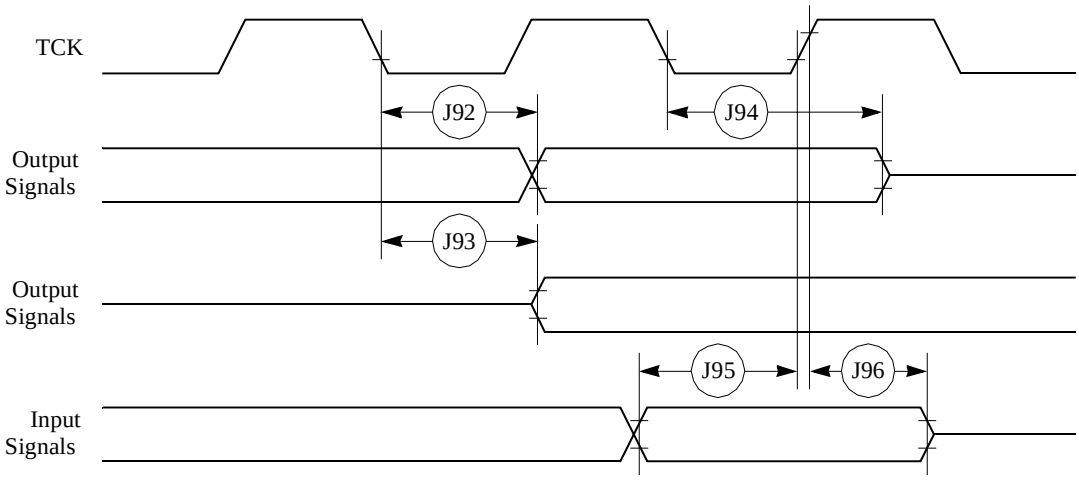



**Figure 37. Boundary Scan (JTAG) Timing Diagram**

# 8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

## 8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

**Table 13. Parallel I/O Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 29 | Data-in setup time to clock high | 15 | — | ns |
| 30 | Data-in hold time from clock high | 7.5 | — | ns |
| 31 | Clock low to data-out valid (CPU writes data, control, or direction) | — | 25 | ns |

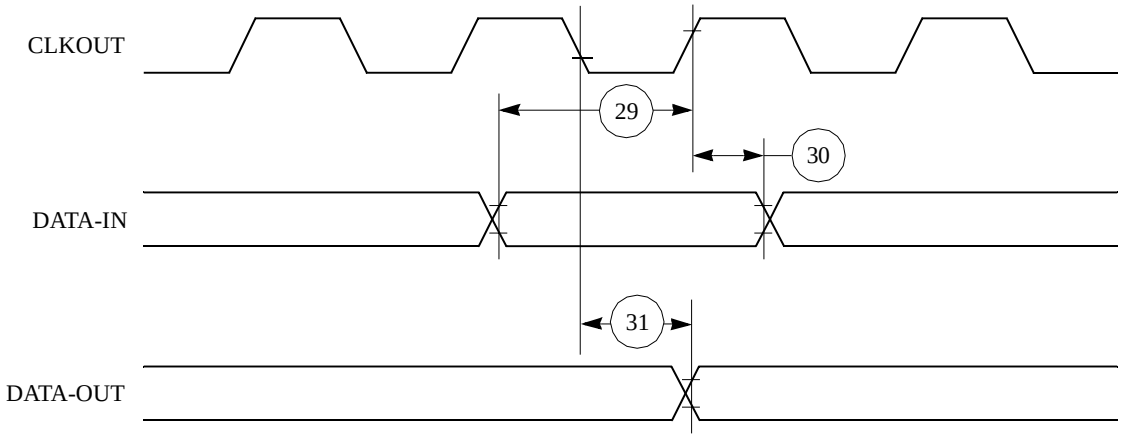



**Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram**

## 8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

**Table 14. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7.00 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3.00 | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12.00 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12.00 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20.00 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15.00 | ns |
| 46 | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7.00 | — | ns |

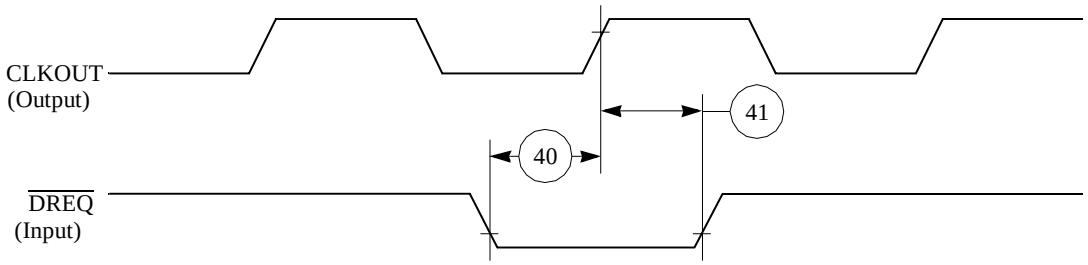



**Figure 39. IDMA External Requests Timing Diagram**

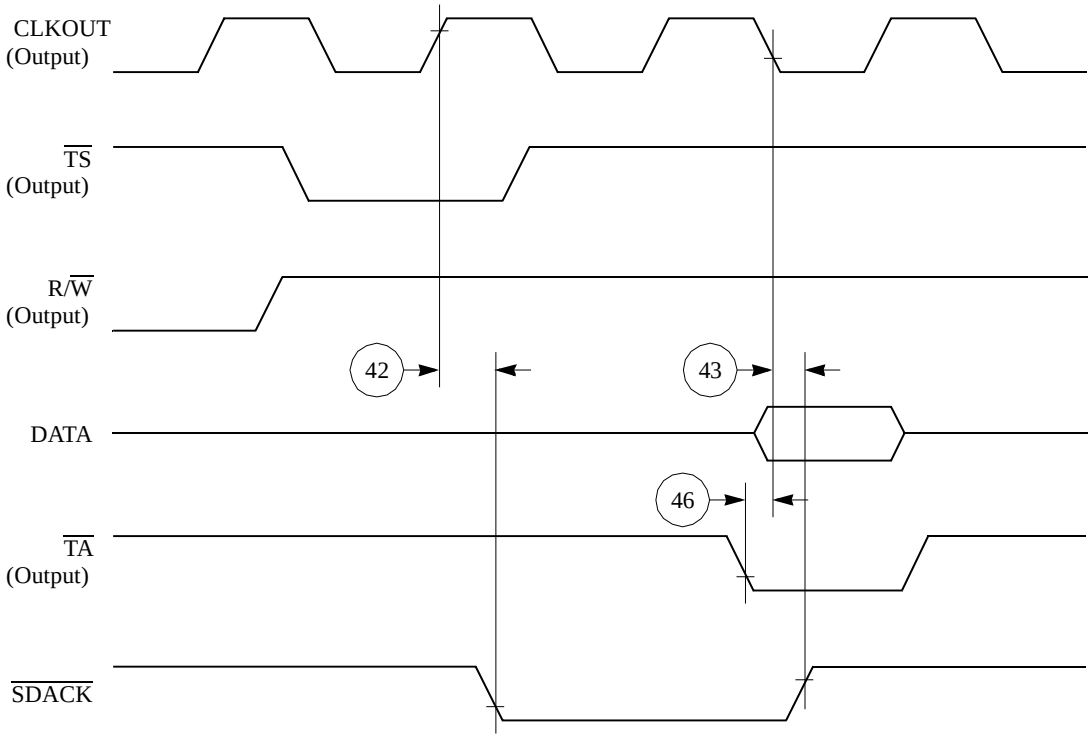



**Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock**

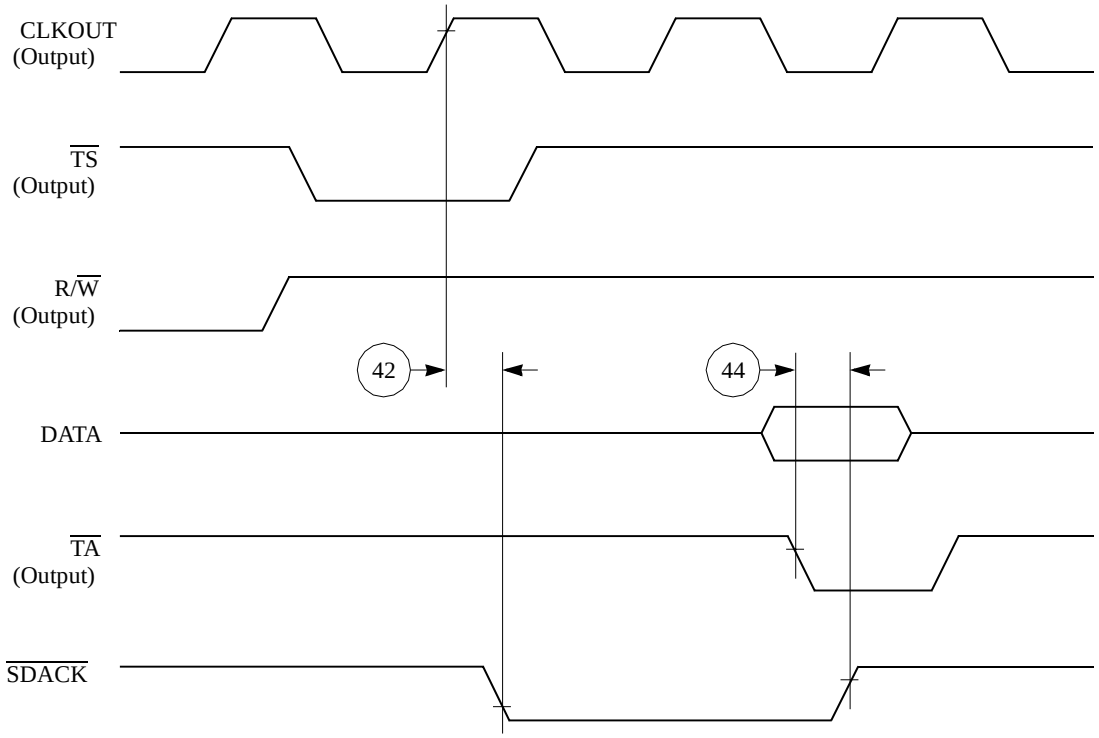



**Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock**

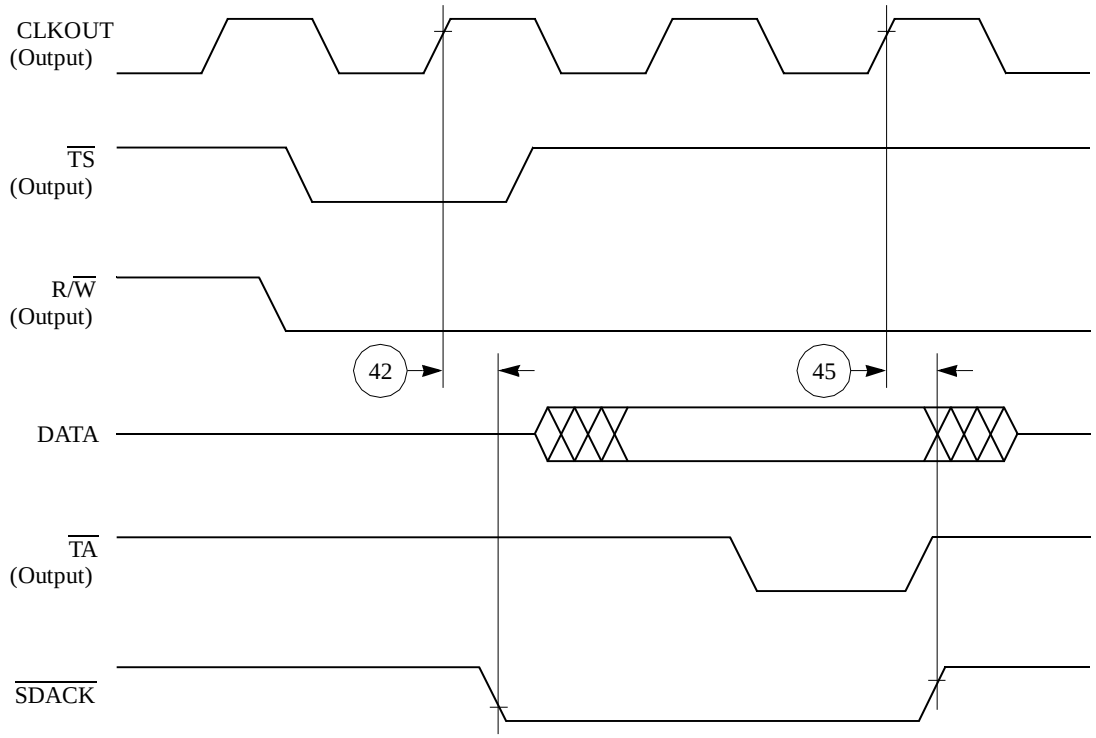



**Figure 42. SDACK Timing Diagram—Peripheral Read**

## 8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

**Table 15. Baud Rate Generator Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10.00 | ns |
| 51 | BRGO duty cycle | 40.00 | 60.00 | % |
| 52 | BRGO cycle | 40.00 | — | ns |

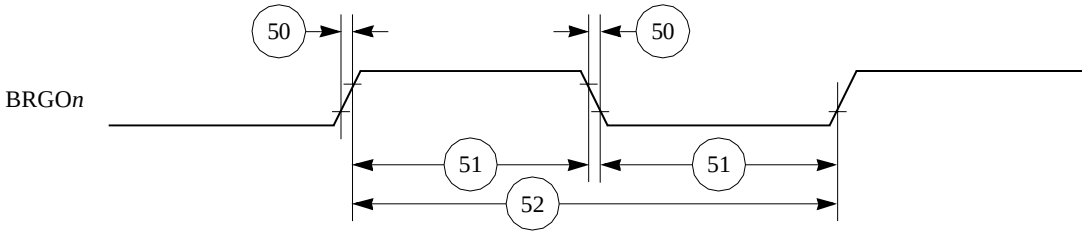



**Figure 43. Baud Rate Generator Timing Diagram**

## 8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

**Table 16. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10.00 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1.00 | — | clk |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2.00 | — | clk |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3.00 | — | clk |
| 65 | CLKO high to $\overline{\text{TOUT}}$ valid | 3.00 | 25.00 | ns |

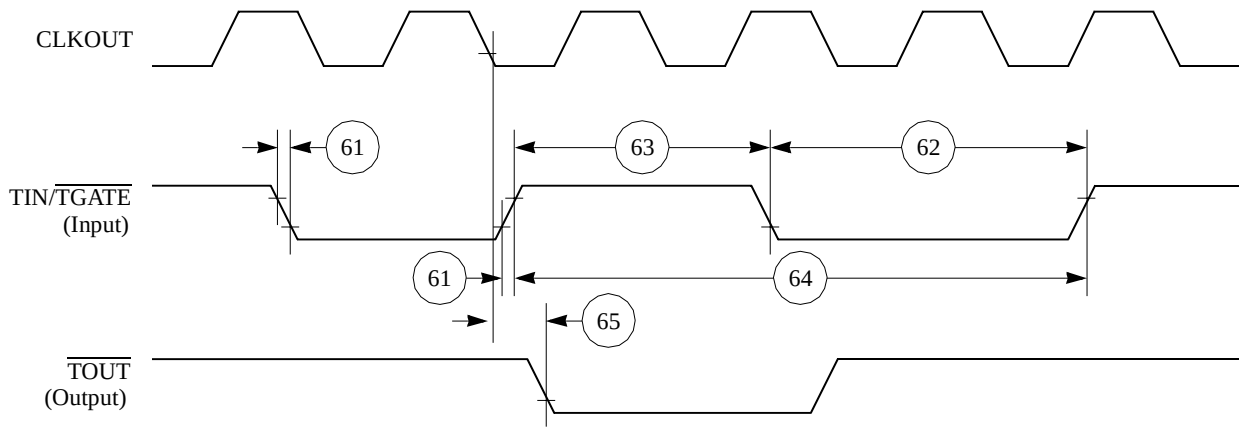



**Figure 44. CPM General-Purpose Timers Timing Diagram**

## 8.5 Serial Interface AC Electrical Specifications

Table 17 provides the serial interface timings as shown in Figure 45 to Figure 49.

**Table 17. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0) [1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0) [2] | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0) [3] | P + 10 | — | ns |
| 72 | L1TXD, L1ST*n*, $\overline{\text{L1RQ}}$, L1xCLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1xCLK edge Edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1xCLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |
| 76 | L1RXD valid to L1xCLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1xCLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1xCLK edge to L1ST*n* valid [4] | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST*n* valid | 10.00 | 45.00 | ns |
| 79 | L1xCLK edge to L1ST*n* invalid | 10.00 | 45.00 | ns |
| 80 | L1xCLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid [4] | 10.00 | 55.00 | ns |
| 81 | L1xCLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |

**Table 17. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 82 | L1RCLK, L1TCLK frequency (DSC =1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC =1) | P + 10 | — | ns |
| 83A | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4] | 1.00 | — | L1TCLK |
| 86 | L1GR setup time[2] | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

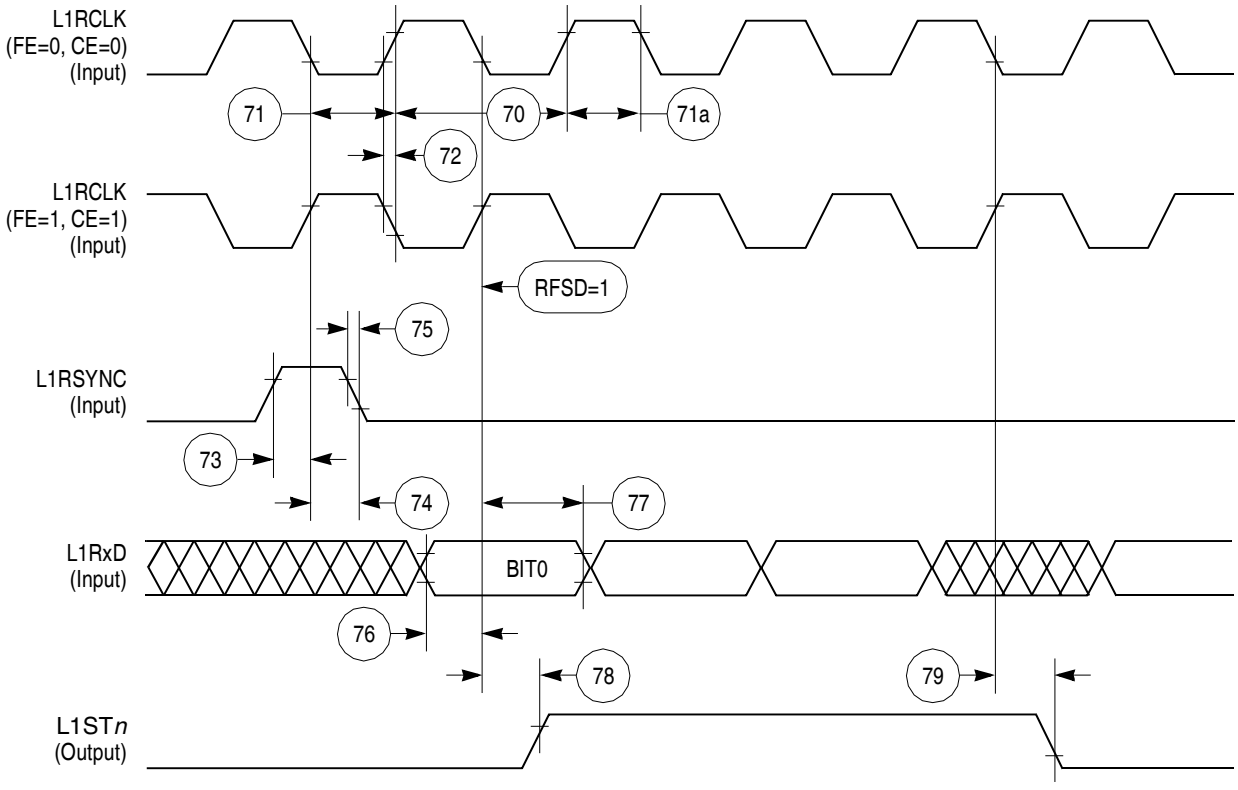



**Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)**

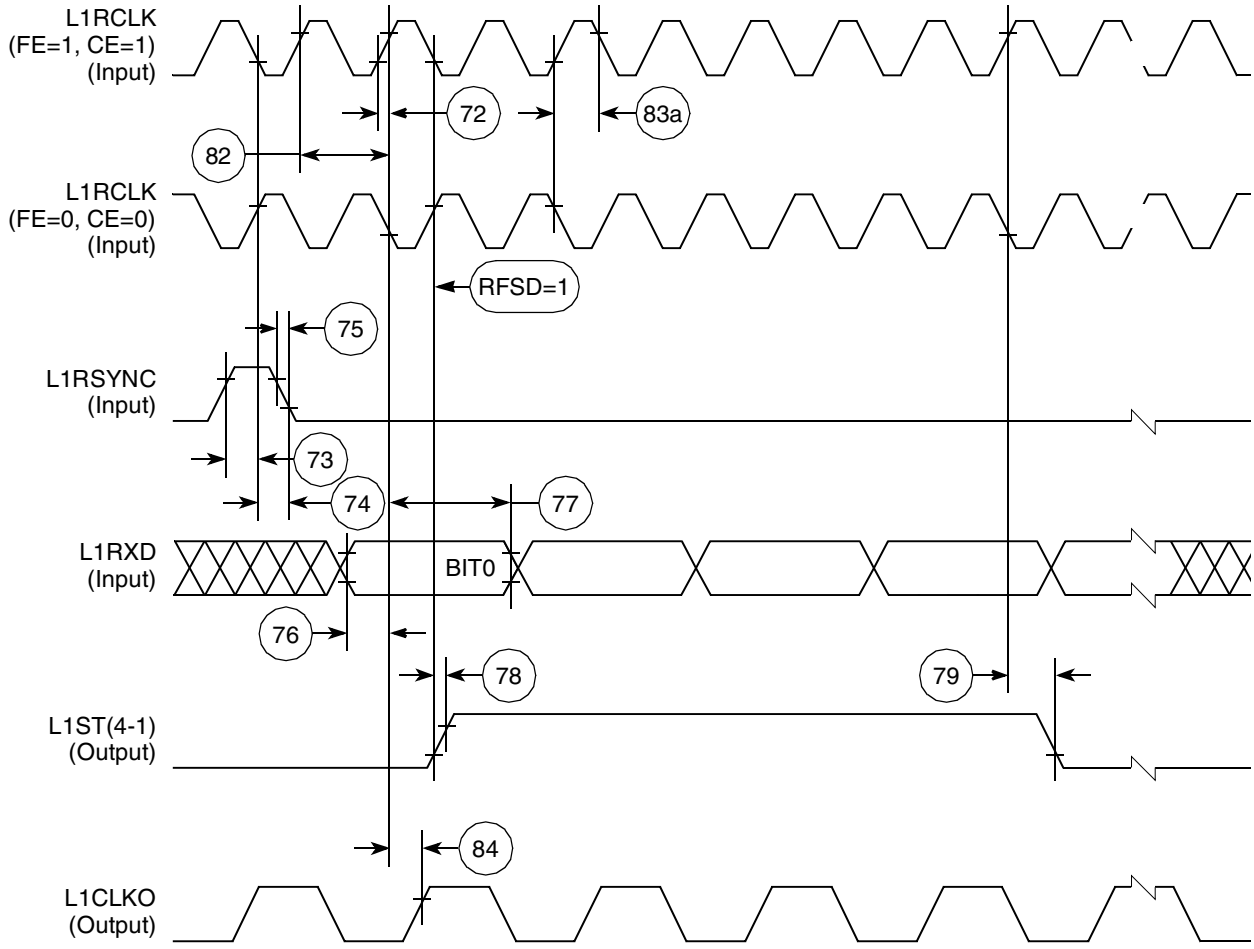



**Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)**

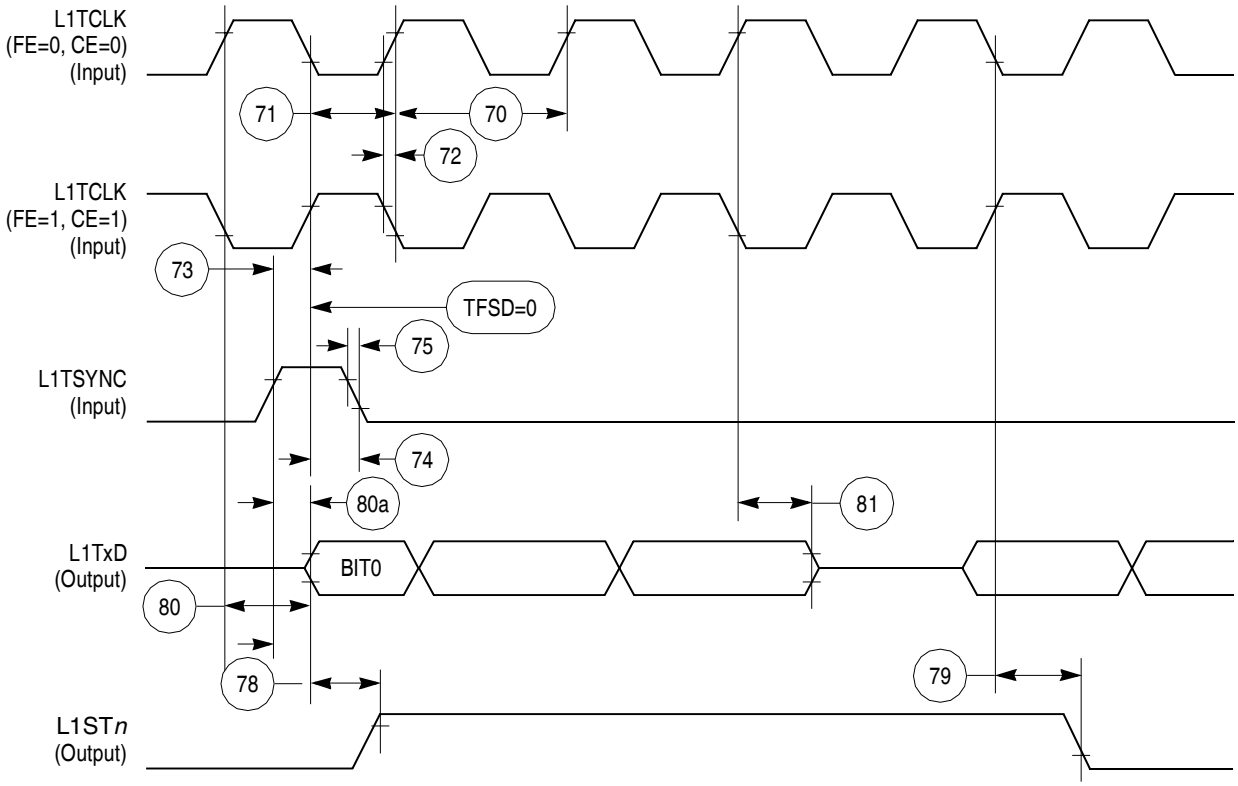



**Figure 47. SI Transmit Timing Diagram**

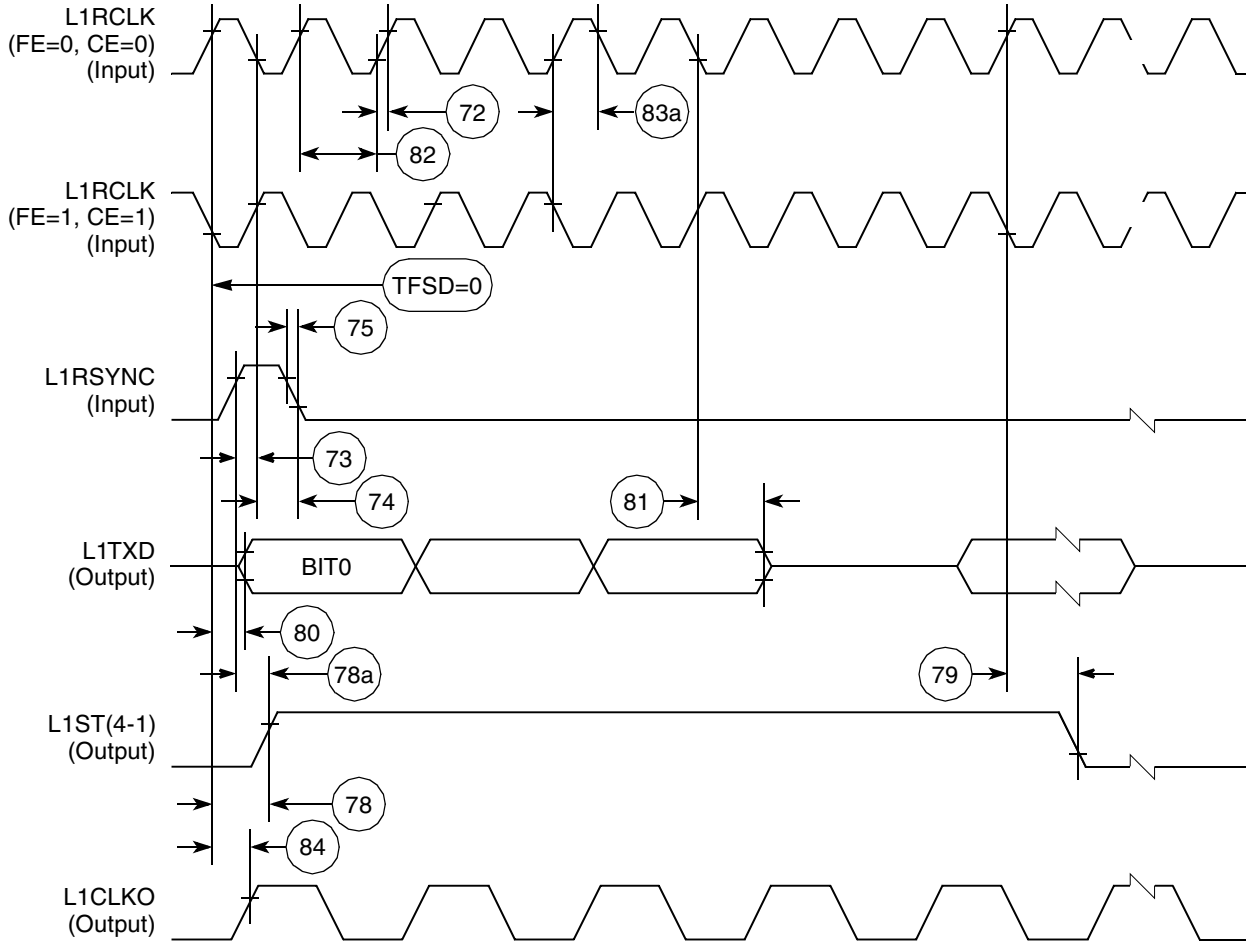



**Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

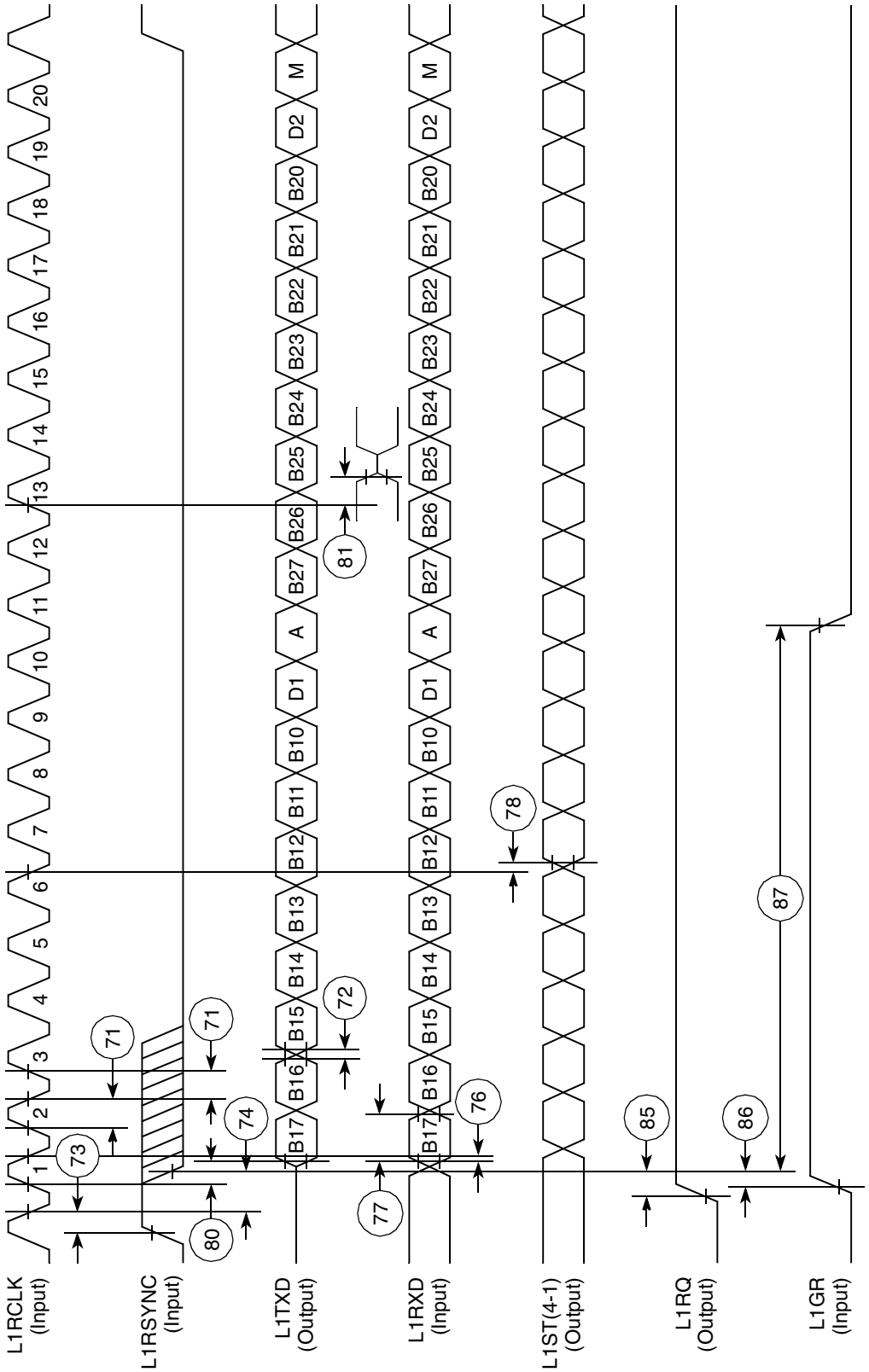



**Figure 49. IDL Timing**

## 8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

**Table 18. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 1/SYNCCLK | — | ns |
| 101 | RCLKx and TCLKx width low | 1/SYNCCLK +5 | — | ns |
| 102 | RCLKx and TCLKx rise/fall time | — | 15.00 | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 5.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 5.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 5.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

**Table 19. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLKx and TCLKx rise/fall time | — | — | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 40.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 40.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 0.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 50 through Figure 52 show the NMSI timings.

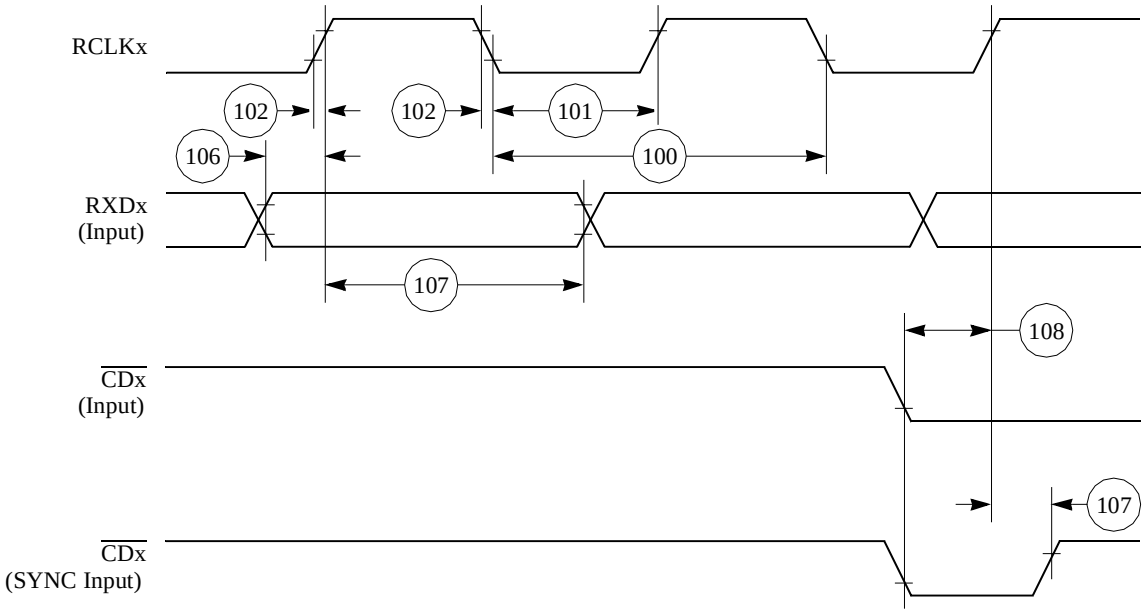



**Figure 50. SCC NMSI Receive Timing Diagram**

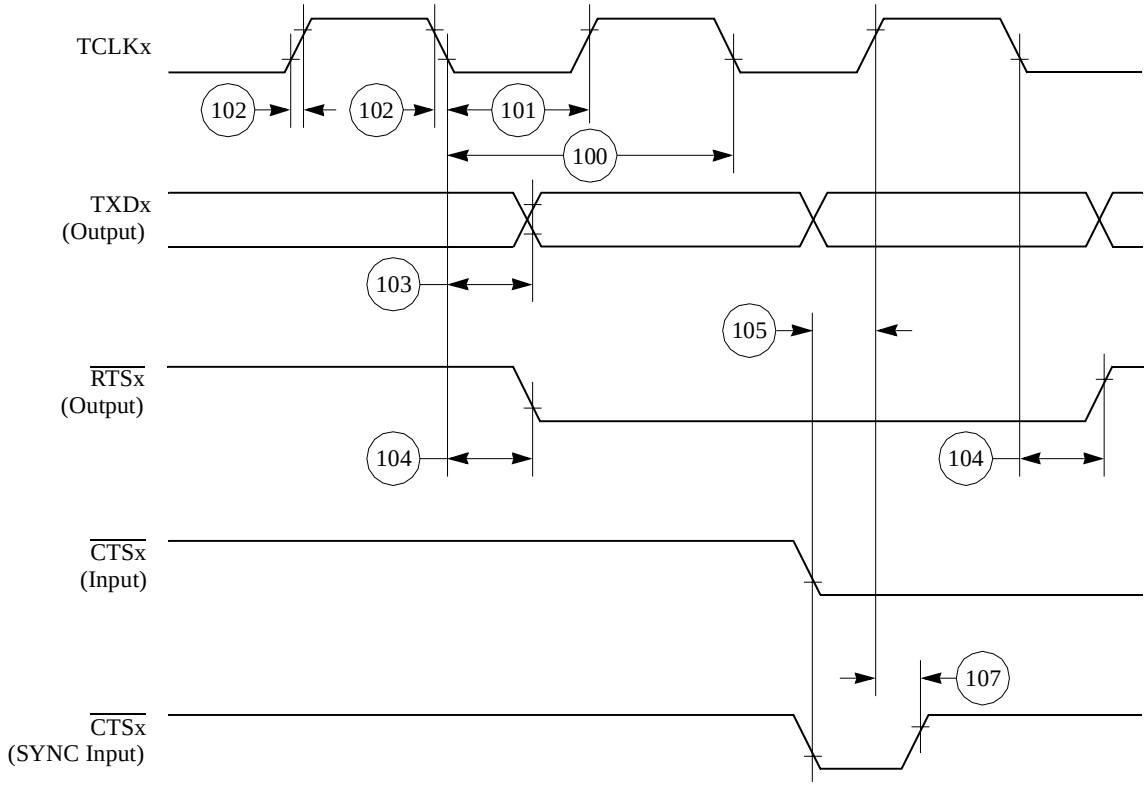



**Figure 51. SCC NMSI Transmit Timing Diagram**

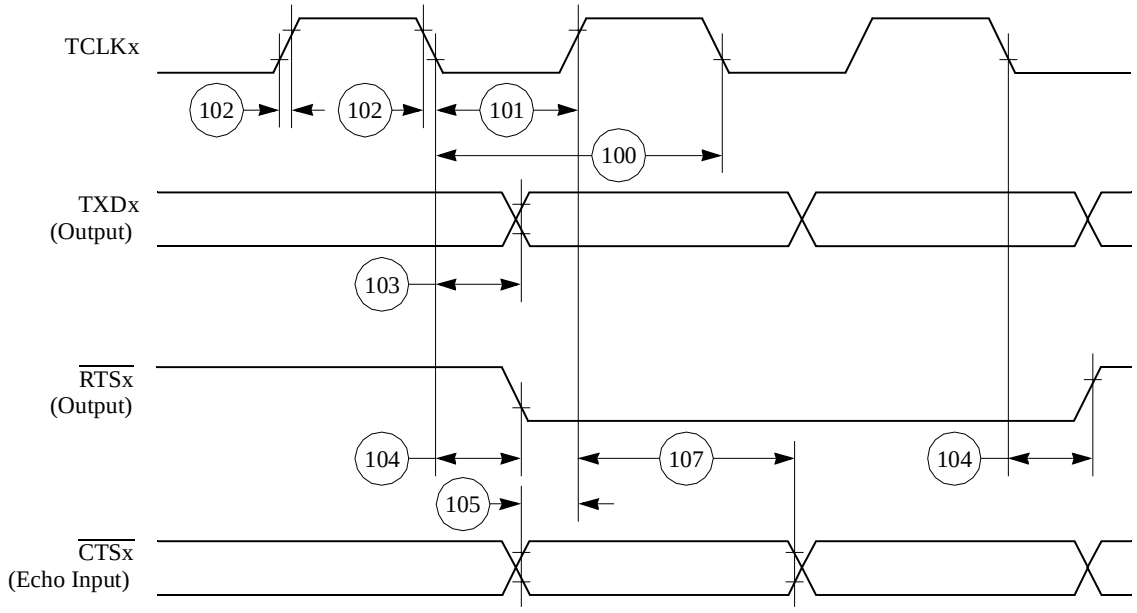



**Figure 52. HDLC Bus Timing Diagram**

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

**Table 20. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40.00 | — | ns |
| 121 | RCLKx rise/fall time (x = 2, 3 for all specs in this table) | — | 15.00 | ns |
| 122 | RCLKx width low | 40.00 | — | ns |
| 123 | RCLKx clock period [1] | 80.00 | 120.00 | ns |
| 124 | RXDx setup time | 20.00 | — | ns |
| 125 | RXDx hold time | 5.00 | — | ns |
| 126 | RENA active delay (from RCLKx rising edge of the last data bit) | 10.00 | — | ns |
| 127 | RENA width low | 100.00 | — | ns |
| 128 | TCLKx rise/fall time | — | 15.00 | ns |
| 129 | TCLKx width low | 40.00 | — | ns |
| 130 | TCLKx clock period[1] | 99.00 | 101.00 | ns |
| 131 | TXDx active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 132 | TXDx inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 133 | TENA active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |

**Table 20. Ethernet Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 134 | TENA inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 138 | CLKOUT low to $\overline{\text{SDACK}}$ asserted [2] | — | 20.00 | ns |
| 139 | CLKOUT low to $\overline{\text{SDACK}}$ negated [2] | — | 20.00 | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

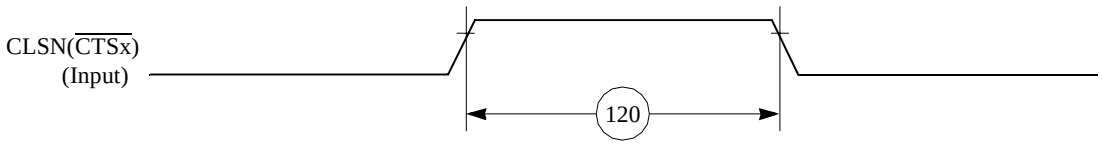



**Figure 53. Ethernet Collision Timing Diagram**

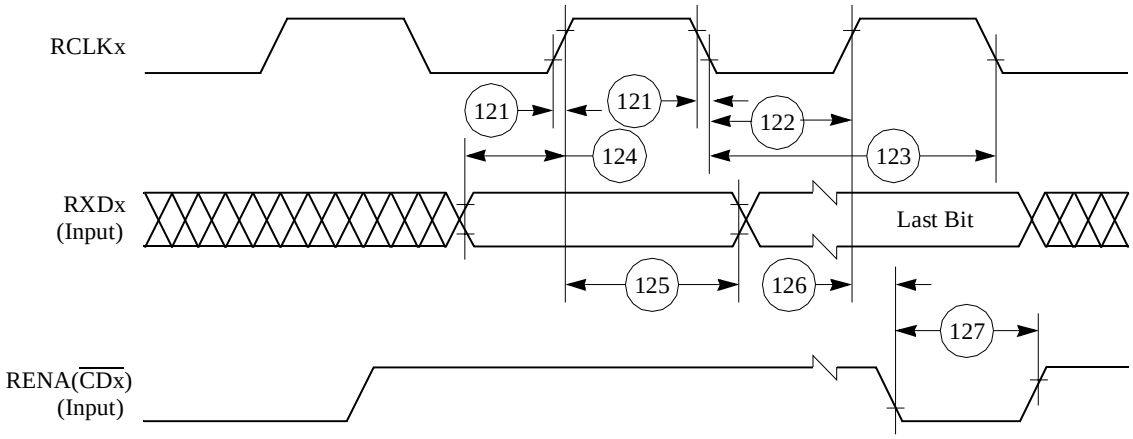
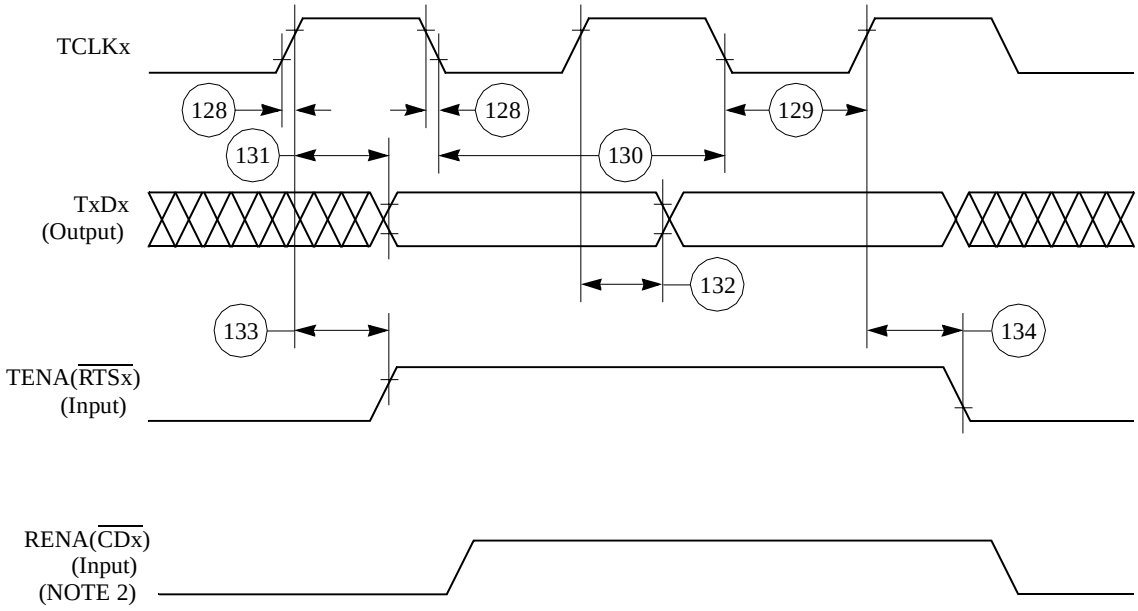



**Figure 54. Ethernet Receive Timing Diagram**




NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 55. Ethernet Transmit Timing Diagram**

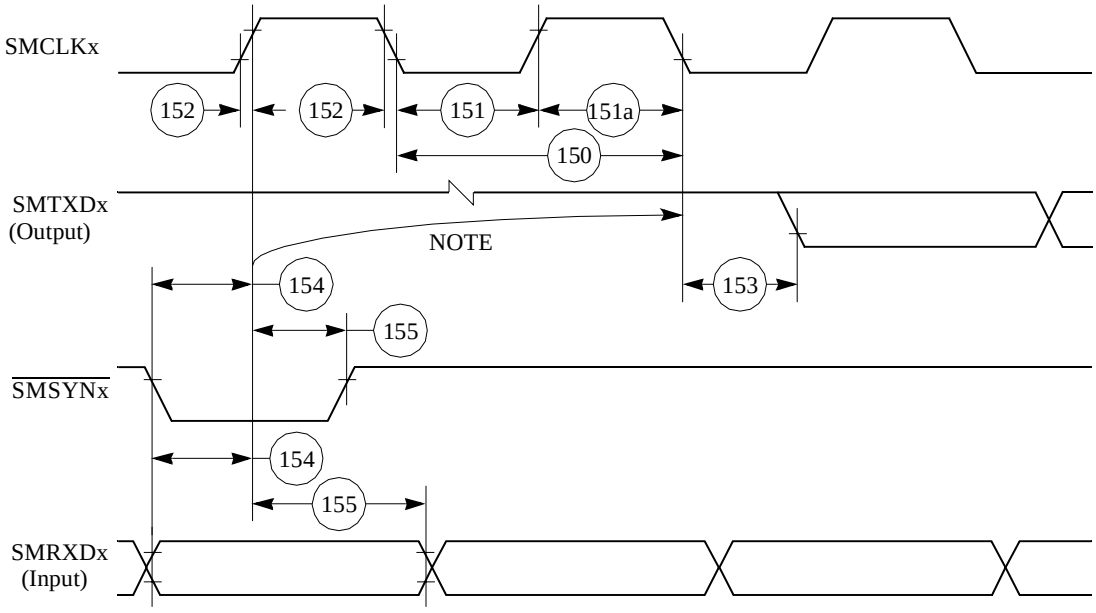
## 8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

**Table 21. Serial Management Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLKx clock period [1] | 100.00 | — | ns |
| 151 | SMCLKx width low | 50.00 | — | ns |
| 151a | SMCLKx width high | 50.00 | — | ns |
| 152 | SMCLKx rise/fall time | — | 15.00 | ns |
| 153 | SMTXDx active delay (from SMCLKx falling edge) | 10.00 | 50.00 | ns |
| 154 | SMRXDx/SMSYNx setup time | 20.00 | — | ns |
| 155 | SMRXDx/SMSYNx hold time | 5.00 | — | ns |

[1] The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.




NOTE:
1. This delay is equal to an integer number of character-length clocks.

**Figure 56. SMC Transparent Timing Diagram**

## 8.9 SPI Master AC Electrical Specifications

Table 22 provides the SPI master timings as shown in Figure 57 and Figure 58.

**Table 22. SPI Master Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 160 | MASTER cycle time | 4 | 1024 | $t_{cyc}$ |
| 161 | MASTER clock (SCK) high or low time | 2 | 512 | $t_{cyc}$ |
| 162 | MASTER data setup time (inputs) | 50.00 | — | ns |
| 163 | Master data hold time (inputs) | 0.00 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 20.00 | ns |
| 165 | Master data hold time (outputs) | 0.00 | — | ns |
| 166 | Rise time output | — | 15.00 | ns |
| 167 | Fall time output | — | 15.00 | ns |

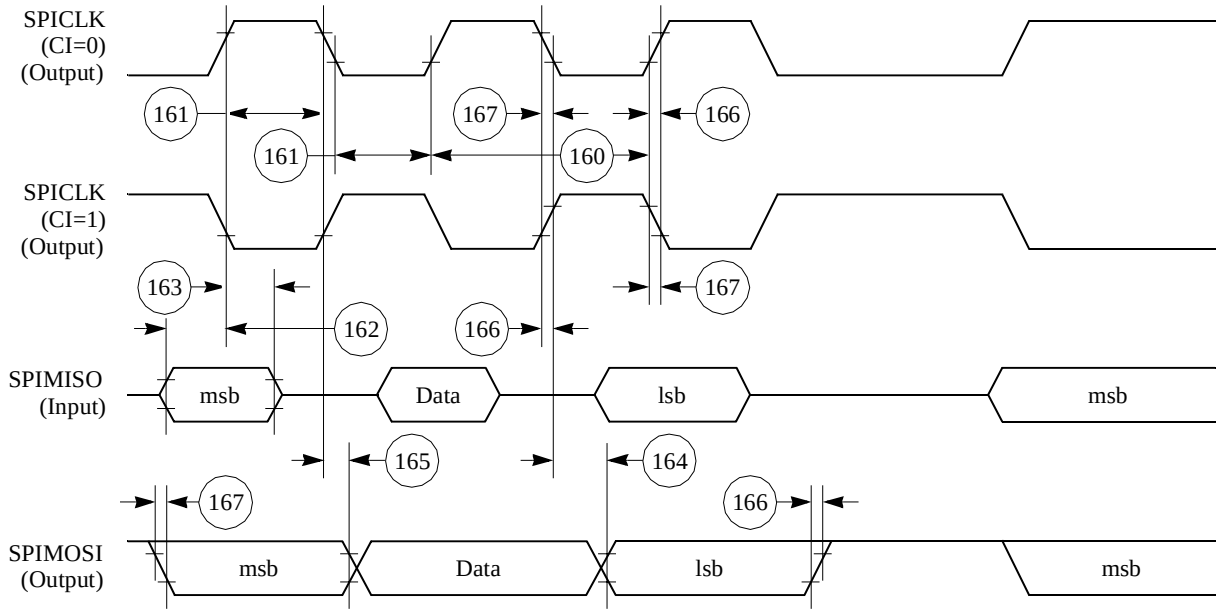



**Figure 57. SPI Master (CP = 0) Timing Diagram**

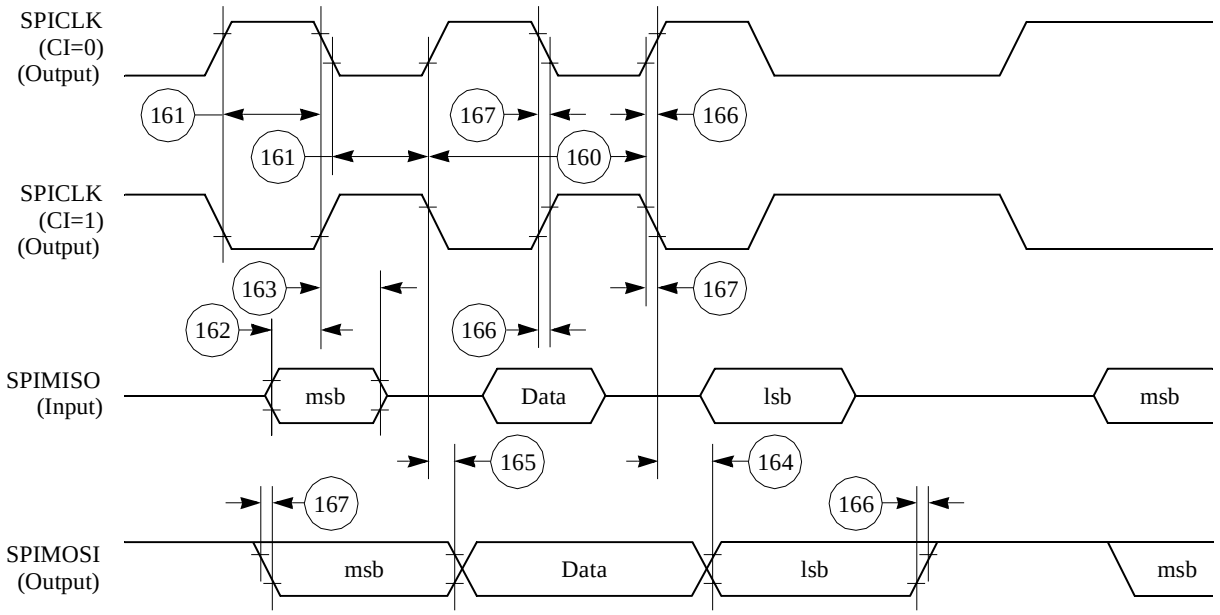



**Figure 58. SPI Master (CP = 1) Timing Diagram**

## 8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

**Table 23. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15.00 | — | ns |
| 172 | Slave enable lag time | 15.00 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20.00 | — | ns |
| 176 | Slave data hold time (inputs) | 20.00 | — | ns |
| 177 | Slave access time | — | 50.00 | ns |
| 178 | Slave SPI MISO disable time | — | 50.00 | ns |
| 179 | Slave data valid (after SPICLK edge) | — | 50.00 | ns |
| 180 | Slave data hold time (outputs) | 0.00 | — | ns |
| 181 | Rise time (input) | — | 15.00 | ns |
| 182 | Fall time (input) | — | 15.00 | ns |

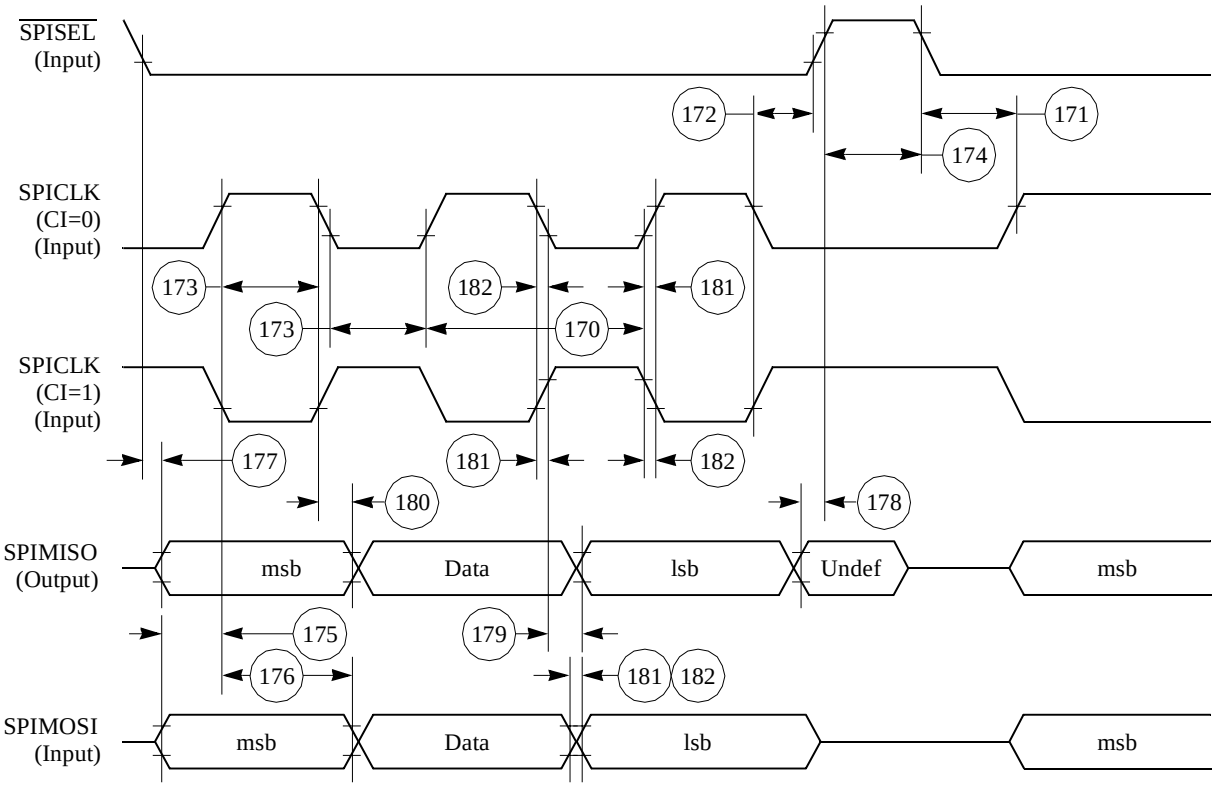



**Figure 59. SPI Slave (CP = 0) Timing Diagram**

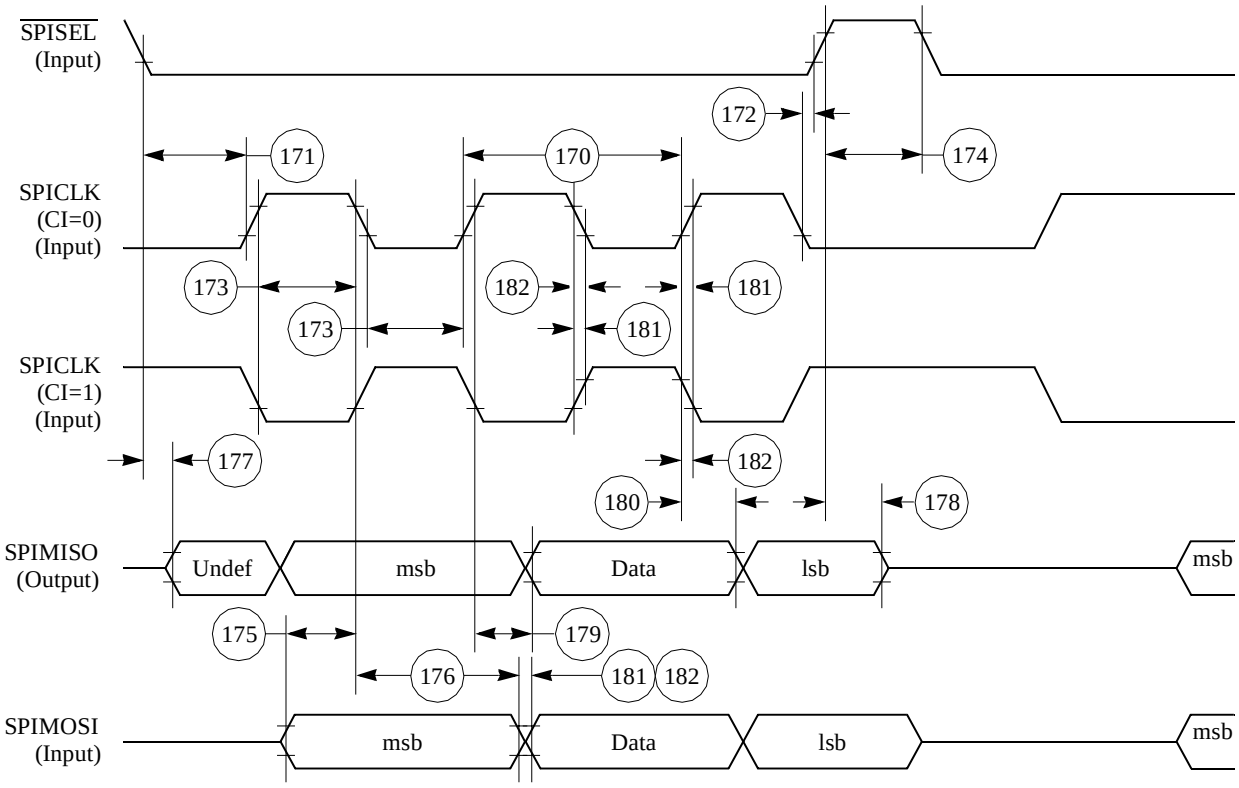



**Figure 60. SPI Slave (CP = 1) Timing Diagram**

## 8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

**Table 24. I²C Timing (SCL < 100 KHz)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0.00 | 100.00 | KHz |
| 200 | SCL clock frequency (master) [1] | 1.50 | 100.00 | KHz |
| 202 | Bus free time between transmissions | 4.70 | — | µs |
| 203 | Low period of SCL | 4.70 | — | µs |
| 204 | High period of SCL | 4.00 | — | µs |
| 205 | Start condition setup time | 4.70 | — | µs |
| 206 | Start condition hold time | 4.00 | — | µs |
| 207 | Data hold time | 0.00 | — | µs |
| 208 | Data setup time | 250.00 | — | ns |
| 209 | SDL/SCL rise time | — | 1.00 | µs |

**Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300.00 | ns |
| 211 | Stop condition setup time | 4.70 | — | µs |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

**Table 25. I²C Timing (SCL > 100 KHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) [1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

1 SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

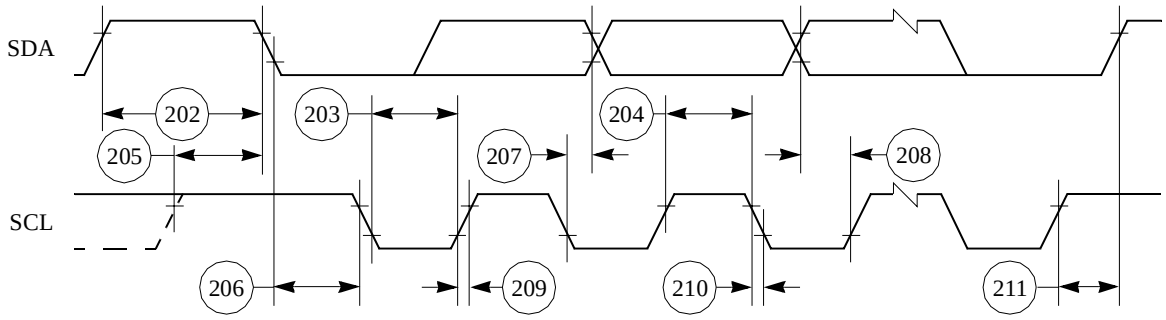



**Figure 61. I²C Bus Timing Diagram**

# 9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

**Table 26. MPC850 Family Derivatives**

| Device | Ethernet Support | Number of SCCs [1] | 32-Channel HDLC Support | 64-Channel HDLC Support [2] |
|---|---|---|---|---|
| MPC850 | N/A | One | N/A | N/A |
| MPC850DE | Yes | Two | N/A | N/A |
| MPC850SR | Yes | Two | N/A | Yes |
| MPC850DSL | Yes | Two | No | No |

1 Serial Communication Controller (SCC)

2 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

**Table 27. MPC850 Package/Frequency/Availability**

| Package Type | Frequency (MHz) | Temperature (Tj) | Order Number |
|---|---|---|---|
| 256-Lead Plastic Ball Grid Array (ZT suffix) | 50 | 0°C to 95°C | XPC850ZT50BU<br>XPC850DEZT50BU<br>XPC850SRZT50BU<br>XPC850DSLZT50BU |
| | 66 | 0°C to 95°C | XPC850ZT66BU<br>XPC850DEZT66BU<br>XPC850SRZT66BU |
| | 80 | 0°C to 95°C | XPC850ZT80BU<br>XPC850DEZT80BU<br>XPC850SRZT80BU |
| 256-Lead Plastic Ball Grid Array (CZT suffix) | 50 | -40°C to 95°C | XPC850CZT50BU<br>XPC850DECZT50BU<br>XPC850SRCZT50BU<br>XPC850DSLCZT50BU |
| | 66 | | XPC850CZT66BU<br>XPC850DECZT66BU<br>XPC850SRCZT66BU |
| | 80 | | XPC850CZT80B<br>XPC850DECZT80B<br>XPC850SRCZT80B |

## 9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

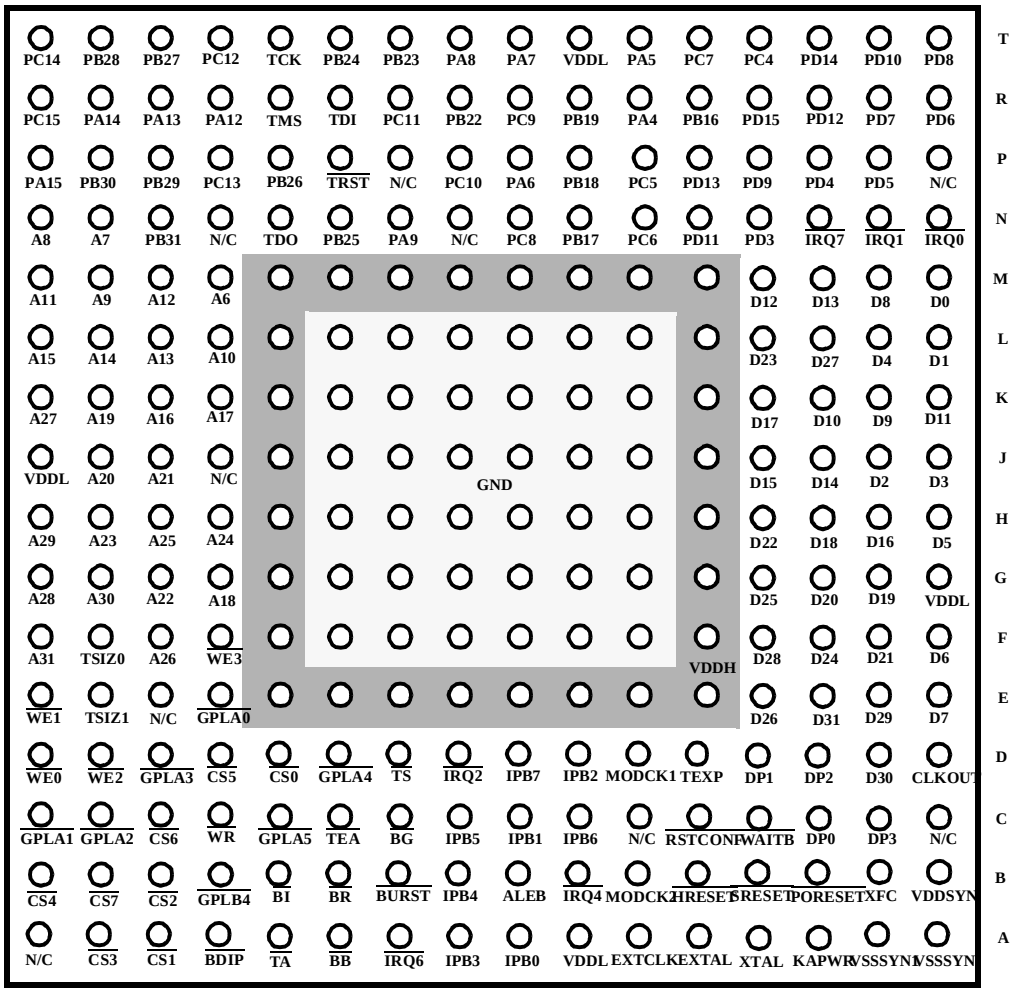



**Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard**

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

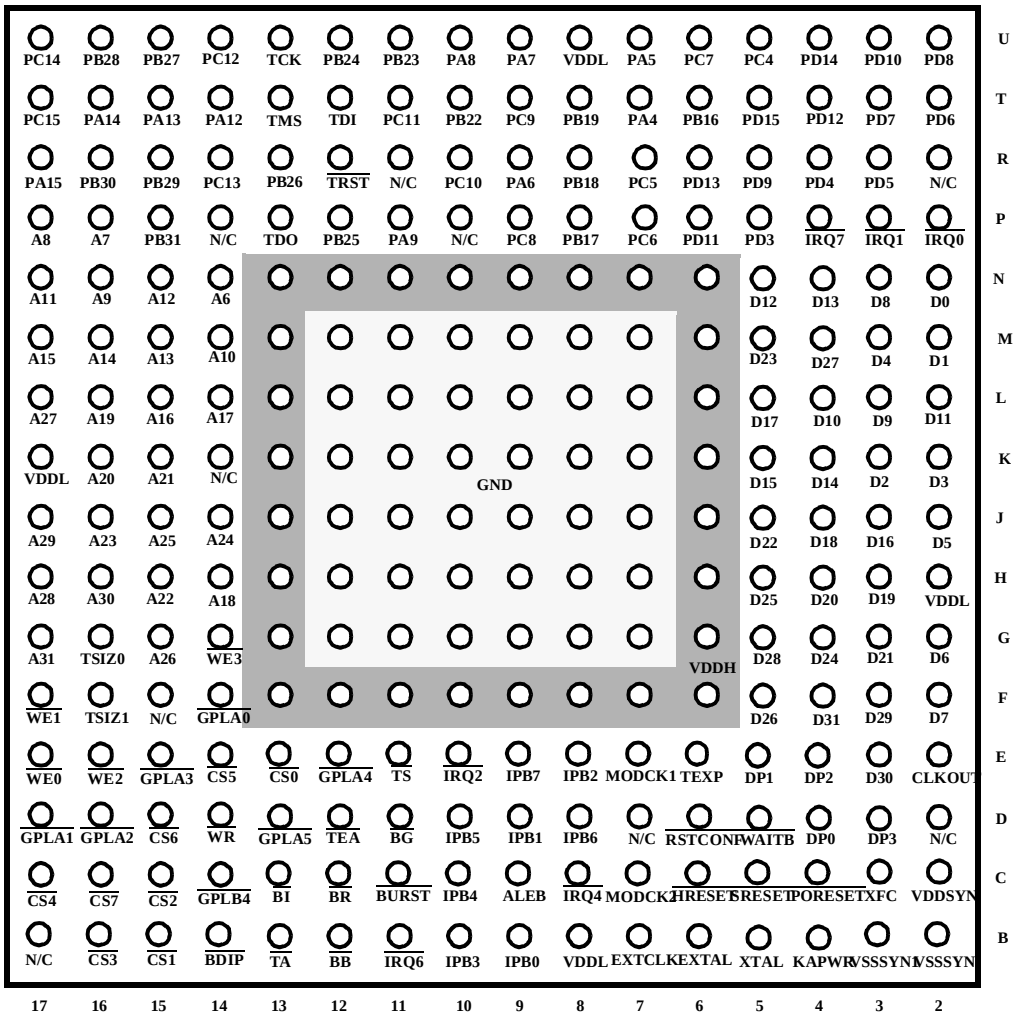
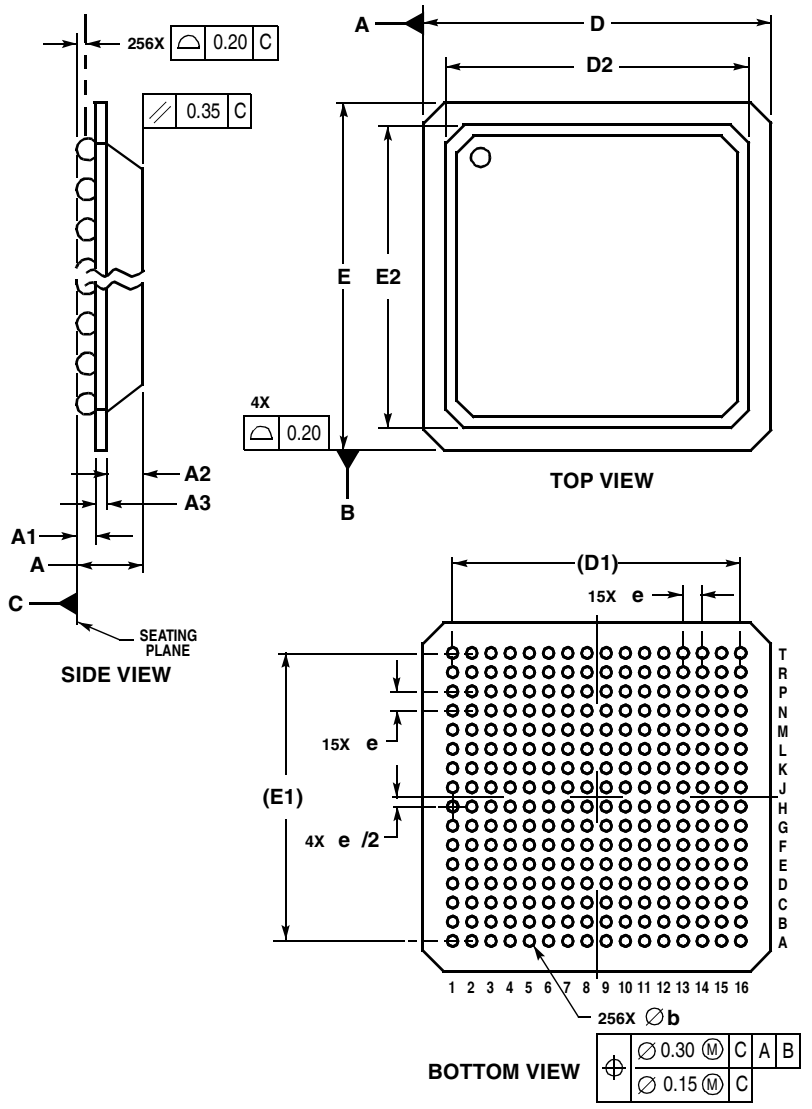



**Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard**

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

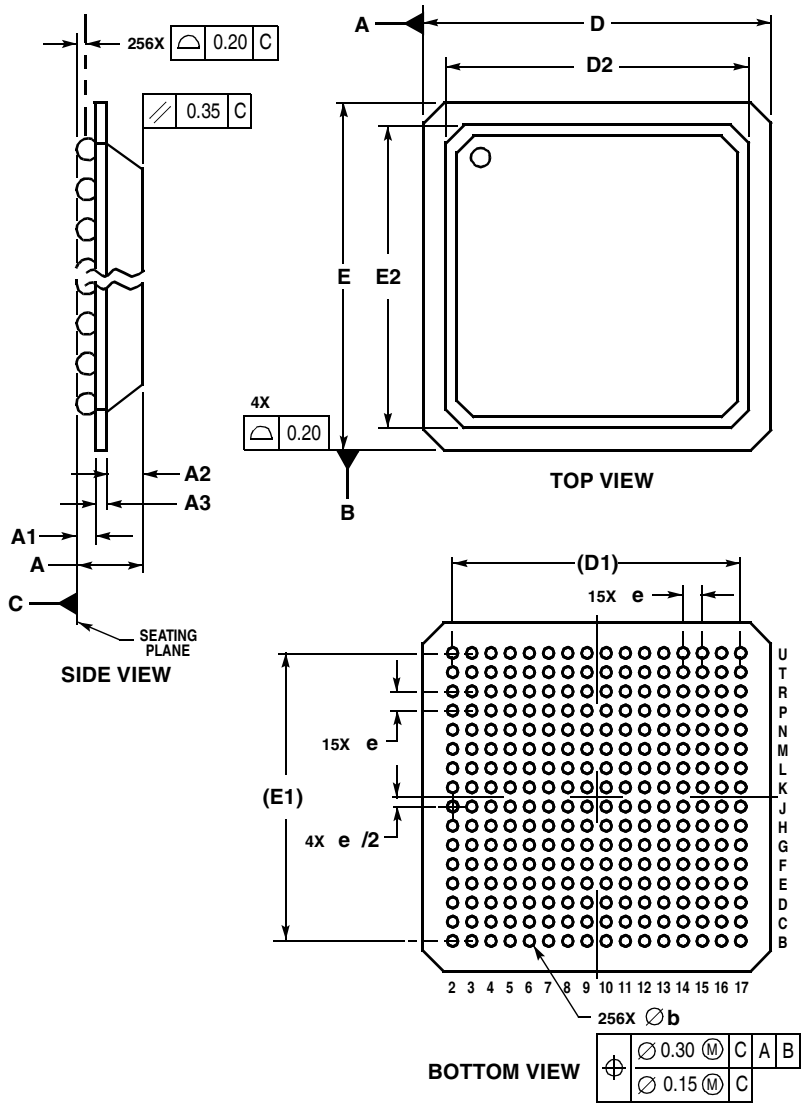



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.91 | 2.35 |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 | 0.29 | 0.43 |
| b | 0.60 | 0.90 |
| D | 23.00 BSC | |
| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

**Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard**

Figure 65 shows the JEDEC package dimensions of the PBGA.




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
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3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
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| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

**CASE 1130-01**
**ISSUE B**

**Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard**

# 10 Document Revision History

Table 28 lists significant changes between revisions of this document.

**Table 28. Document Revision History**

| Revision | Date | Change |
|---|---|---|
| 2 | 7/2005 | Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit. |
| 1 | 10/2002 | Added MPC850DSL. Corrected Figure 25 on page 34. |
| 0.2 | 04/2002 | Updated power numbers and added Rev. C |
| 0.1 | 11/2001 | Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table. |

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