Freescale Semiconductor
Technical Data

MPC860EC
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# MPC860 PowerQUICC Family Hardware Specifications

This hardware specification contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC860 family.

To locate published errata or updates for this document, see the MPC860 product summary page on the website listed on the back cover of this document or contact your local Freescale sales office.

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# 1 Overview

The MPC860 power quad integrated communications controller (PowerQUICC™) is a versatile one-chip integrated microprocessor and peripheral combination designed for a variety of controller applications. It particularly excels in communications and networking systems. The PowerQUICC unit is referred to as the MPC860 in this hardware specification.

The MPC860 implements Power Architecture™ technology and contains a superset of Freescale's MC68360 quad integrated communications controller (QUICC), referred to here as the QUICC, RISC communications proccessor module (CPM). The CPU on the MPC860 is a 32-bit core built on Power Architecture technology that incorporates memory management units (MMUs) and instruction and data caches.. The CPM from the MC68360 QUICC has been enhanced by the addition of the inter-integrated controller ($I^2C$) channel. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high-performance memories and new types of DRAMs. A PCMCIA socket controller supports up to two sockets. A real-time clock has also been integrated.

Table 1 shows the functionality supported by the MPC860 family.

**Table 1. MPC860 Family Functionality**

| Part | Cache (Kbytes) | | Ethernet | | ATM | SCC | Reference[1] |
|---|---|---|---|---|---|---|---|
| | Instruction Cache | Data Cache | 10T | 10/100 | | | |
| MPC860DE | 4 | 4 | Up to 2 | — | — | 2 | 1 |
| MPC860DT | 4 | 4 | Up to 2 | 1 | Yes | 2 | 1 |
| MPC860DP | 16 | 8 | Up to 2 | 1 | Yes | 2 | 1 |
| MPC860EN | 4 | 4 | Up to 4 | — | — | 4 | 1 |
| MPC860SR | 4 | 4 | Up to 4 | — | Yes | 4 | 1 |
| MPC860T | 4 | 4 | Up to 4 | 1 | Yes | 4 | 1 |
| MPC860P | 16 | 8 | Up to 4 | 1 | Yes | 4 | 1 |
| MPC855T | 4 | 4 | 1 | 1 | Yes | 1 | 2 |

[1] Supporting documentation for these devices refers to the following:
1. MPC860 PowerQUICC Family User's Manual (MPC860UM, Rev. 3)
2. MPC855T User's Manual (MPC855TUM, Rev. 1)

# 2 Features

The following list summarizes the key MPC860 features:

- Embedded single-issue, 32-bit core (implementing the Power Architecture technology) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch without conditional execution.
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - 16-Kbyte instruction caches are four-way, set-associative with 256 sets; 4-Kbyte instruction caches are two-way, set-associative with 128 sets.
    - 8-Kbyte data caches are two-way, set-associative with 256 sets; 4-Kbyte data caches are two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully-associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4-, 16-, and 512-Kbytes, and 8-Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Operates at up to 80 MHz
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 15 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROM, Flash EPROM, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes to 256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC)
  - Reset controller
  - IEEE 1149.1™ Std. test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- 10/100 Mbps Ethernet support, fully compliant with the IEEE 802.3u® Standard (not available when using ATM over UTOPIA interface)
- ATM support compliant with ATM forum UNI 4.0 specification
  - Cell processing up to 50–70 Mbps at 50-MHz system clock
  - Cell multiplexing/demultiplexing
  - Support of AAL5 and AAL0 protocols on a per-VC basis. AAL0 support enables OAM and software implementation of other protocols.
  - ATM pace control (APC) scheduler, providing direct support for constant bit rate (CBR) and unspecified bit rate (UBR) and providing control mechanisms enabling software support of available bit rate (ABR)
  - Physical interface support for UTOPIA (10/100-Mbps is not supported with this interface) and byte-aligned serial (for example, T1/E1/ADSL)
  - UTOPIA-mode ATM supports level-1 master with cell-level handshake, multi-PHY (up to four physical layer devices), connection to 25-, 51-, or 155-Mbps framers, and UTOPIA/system clock ratios of 1/2 or 1/3.
  - Serial-mode ATM connection supports transmission convergence (TC) function for T1/E1/ADSL lines, cell delineation, cell payload scrambling/descrambling, automatic idle/unassigned cell insertion/stripping, header error control (HEC) generation, checking, and statistics.
- Communications processor module (CPM)
  - RISC communications processor (CP)
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels

  - Up to 8 Kbytes of dual-port RAM
  - 16 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud-rate generators (BRGs)
  - Independent (can be tied to any SCC or SMC)
  - Allows changes during operation
  - Autobaud support option
- Four serial communications controllers (SCCs)
  - Ethernet/IEEE 802.3® standard optional on SCC1–4, supporting full 10-Mbps operation (available only on specially programmed devices)
  - HDLC/SDLC (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support point-to-point protocol (PPP)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One $I^2C$ (inter-integrated circuit) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking

  - Allows dynamic changes
  - Can be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on the MPC860 or the MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports two independent PCMCIA sockets
  - Supports eight memory or I/O windows
- Low power support
  - Full on—all units fully powered
  - Doze—core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—all units disabled except RTC and PIT, PLL active for fast wake up
  - Deep sleep—all units disabled including PLL except RTC and PIT
  - Power down mode—all units powered down except PLL, RTC, PIT, time base, and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: $= \neq < >$
  - Each watchpoint can generate a break-point internally.
- 3.3-V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin ball grid array (BGA) package

# 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC860. Table 2 provides the maximum ratings.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{DD}$).

**Table 2. Maximum Tolerated Ratings**

(GND = 0 V)

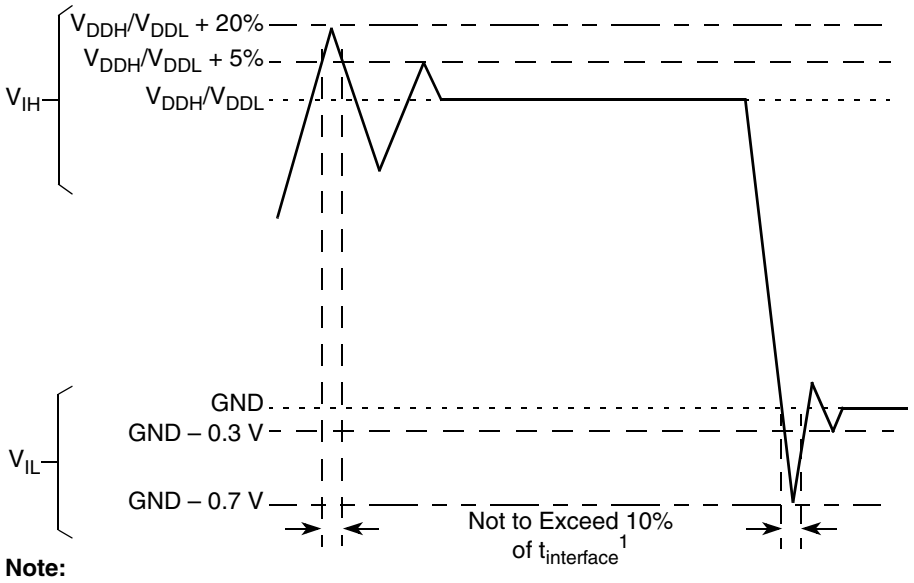
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage[1] | $V_{DDH}$ | –0.3 to 4.0 | V |
| | $V_{DDL}$ | –0.3 to 4.0 | V |
| | KAPWR | –0.3 to 4.0 | V |
| | $V_{DDSYN}$ | –0.3 to 4.0 | V |
| Input voltage[2] | $V_{in}$ | GND – 0.3 to $V_{DDH}$ | V |
| Temperature[3] (standard) | $T_{A(min)}$ | 0 | °C |
| | $T_{j(max)}$ | 95 | °C |
| Temperature[3] (extended) | $T_{A(min)}$ | –40 | °C |
| | $T_{j(max)}$ | 95 | °C |
| Storage temperature range | $T_{stg}$ | –55 to 150 | °C |

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
**Caution**: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC860 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, $T_A$. Maximum temperatures are guaranteed as junction temperature, $T_j$.

Figure 1 shows the undershoot and overshoot voltages at the interface of the MPC860.




**Note:**
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

**Figure 1. Undershoot/Overshoot Voltage for $V_{DDH}$ and $V_{DDL}$**

# 4 Thermal Characteristics

**Table 3. Package Description**

| Package Designator | Package Code (Case No.) | Package Description |
|---|---|---|
| ZP | 5050 (1103-01) | PBGA 357 25*25*0.9P1.27 |
| ZQ/VR | 5058 (1103D-02) | PBGA 357 25*25*1.2P1.27 |

Table 4 shows the thermal characteristics for the MPC860.

**Table 4. MPC860 Thermal Resistance Data**

| Rating | Environment | | Symbol | ZP MPC860P | ZQ / VR MPC860P | Unit |
|---|---|---|---|---|---|---|
| Mold Compound Thickness | | | | 0.85 | 1.15 | mm |
| Junction-to-ambient [1] | Natural convection | Single-layer board (1s) | $R_{\theta JA}$ [2] | 34 | 34 | °C/W |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ [3] | 22 | 22 | |
| | Airflow (200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ [3] | 27 | 27 | |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ [3] | 18 | 18 | |
| Junction-to-board [4] | | | $R_{\theta JB}$ | 14 | 13 | |
| Junction-to-case [5] | | | $R_{\theta JC}$ | 6 | 8 | |
| Junction-to-package top [6] | Natural convection | | $\Psi_{JT}$ | 2 | 2 | |

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

# 5 Power Dissipation

Table 5 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice the bus speed.

**Table 5. Power Dissipation ($P_D$)**

| Die Revision | Frequency (MHz) | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|
| D.4 (1:1 mode) | 50 | 656 | 735 | mW |
| | 66 | TBD | TBD | mW |
| D.4 (2:1 mode) | 66 | 722 | 762 | mW |
| | 80 | 851 | 909 | mW |

1 Typical power dissipation is measured at 3.3 V.
2 Maximum power dissipation is measured at 3.5 V.

**NOTE**

Values in Table 5 represent $V_{DDL}$-based power dissipation and do not include I/O power dissipation over $V_{DDH}$. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

# 6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC860.

**Table 6. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage at 40 MHz or less | $V_{DDH}$, $V_{DDL}$, $V_{DDSYN}$ | 3.0 | 3.6 | V |
| | KAPWR (power-down mode) | 2.0 | 3.6 | V |
| | KAPWR (all other operating modes) | $V_{DDH}$ – 0.4 | $V_{DDH}$ | V |
| Operating voltage greater than 40 MHz | $V_{DDH}$, $V_{DDL}$, KAPWR, $V_{DDSYN}$ | 3.135 | 3.465 | V |
| | KAPWR (power-down mode) | 2.0 | 3.6 | V |
| | KAPWR (all other operating modes) | $V_{DDH}$ – 0.4 | $V_{DDH}$ | V |
| Input high voltage (all inputs except EXTAL and EXTCLK) | $V_{IH}$ | 2.0 | 5.5 | V |
| Input low voltage[1] | $V_{IL}$ | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | $V_{IHC}$ | 0.7 × ($V_{DDH}$) | $V_{DDH}$ + 0.3 | V |
| Input leakage current, $V_{in}$ = 5.5 V (except TMS, $\overline{TRST}$, DSCK, and DSDI pins) | $I_{in}$ | — | 100 | µA |

**Table 6. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input leakage current, $V_{in}$ = 3.6 V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input leakage current, $V_{in}$ = 0 V (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance[2] | $C_{in}$ | — | 20 | pF |
| Output high voltage, $I_{OH}$ = –2.0 mA, $V_{DDH}$ = 3.0 V (except XTAL, XFC, and open-drain pins) | $V_{OH}$ | 2.4 | — | V |
| Output low voltage<br>$I_{OL}$ = 2.0 mA, CLKOUT<br>$I_{OL}$ = 3.2 mA [3]<br>$I_{OL}$ = 5.3 mA [4]<br>$I_{OL}$ = 7.0 mA, TXD1/PA14, TXD2/PA12<br>$I_{OL}$ = 8.9 mA, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ | $V_{OL}$ | — | 0.5 | V |

1 $V_{IL}$(max) for the $I^2C$ interface is 0.8 V rather than the 1.5 V as specified in the $I^2C$ standard.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{\text{REG}}$, TSIZ1, D(0:31), DP(0:3)/$\overline{\text{IRQ}}$(3:6), RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, $\overline{\text{RSV}}$/$\overline{\text{IRQ2}}$, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1/PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/$\overline{\text{TOUT1}}$/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, $\overline{\text{TOUT2}}$/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/$\overline{\text{TOUT3}}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/$\overline{\text{TOUT4}}$/CLK8/PA0, $\overline{\text{REJCT1}}$/$\overline{\text{SPISEL}}$/PB31, SPICLK/PB30,SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, $\overline{\text{SMSYN1}}$/$\overline{\text{SDACK1}}$/PB23, $\overline{\text{SMSYN2}}$/$\overline{\text{SDACK2}}$/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/$\overline{\text{RTS1}}$/PB19, L1ST2/$\overline{\text{RTS2}}$/PB18, L1ST3/$\overline{\text{L1RQB}}$/PB17, L1ST4/$\overline{\text{L1RQA}}$/PB16, BRGO3/PB15, $\overline{\text{RSTRT1}}$/PB14, L1ST1/$\overline{\text{RTS1}}$/$\overline{\text{DREQ0}}$/PC15, L1ST2/$\overline{\text{RTS2}}$/$\overline{\text{DREQ1}}$/PC14, L1ST3/$\overline{\text{L1RQB}}$/PC13, L1ST4/$\overline{\text{L1RQA}}$/PC12, $\overline{\text{CTS1}}$/PC11, $\overline{\text{TGATE1}}$/$\overline{\text{CD1}}$/PC10, $\overline{\text{CTS2}}$/PC9, $\overline{\text{TGATE2}}$/$\overline{\text{CD2}}$/PC8, $\overline{\text{SDACK2}}$/L1TSYNCB/PC7, L1RSYNCB/PC6, $\overline{\text{SDACK1}}$/L1TSYNCA/PC5, L1RSYNCA/PC4, PD15, PD14, PD13, PD12, PD11, PD10, PD9, PD8, PD5, PD6, PD7, PD4, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, and MII_TXD[0:3]

4 $\overline{\text{BDIP}}$/$\overline{\text{GPL_B}}$(5), $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/$\overline{\text{IRQ6}}$, $\overline{\text{CS}}$(0:5), $\overline{\text{CS}}$(6)/$\overline{\text{CE}}$(1)_B, $\overline{\text{CS}}$(7)/$\overline{\text{CE}}$(2)_B, $\overline{\text{WE0}}$/$\overline{\text{BS_B0}}$/$\overline{\text{IORD}}$, $\overline{\text{WE1}}$/$\overline{\text{BS_B1}}$/$\overline{\text{IOWR}}$, $\overline{\text{WE2}}$/$\overline{\text{BS_B2}}$/$\overline{\text{PCOE}}$, $\overline{\text{WE3}}$/$\overline{\text{BS_B3}}$/$\overline{\text{PCWE}}$, $\overline{\text{BS_A}}$(0:3), $\overline{\text{GPL_A0}}$/$\overline{\text{GPL_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL_A1}}$/$\overline{\text{GPL_B1}}$, $\overline{\text{GPL_A}}$(2:3)/$\overline{\text{GPL_B}}$(2:3)/$\overline{\text{CS}}$(2:3), UPWAITA/$\overline{\text{GPL_A4}}$, UPWAITB/$\overline{\text{GPL_B4}}$, $\overline{\text{GPL_A5}}$, ALE_A, $\overline{\text{CE}}$1_A, $\overline{\text{CE}}$2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/$\overline{\text{STS}}$, OP3/MODCK2/DSDO, and BADDR(28:30)

# 7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

## 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in ºC can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

## 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature; see Figure 2.

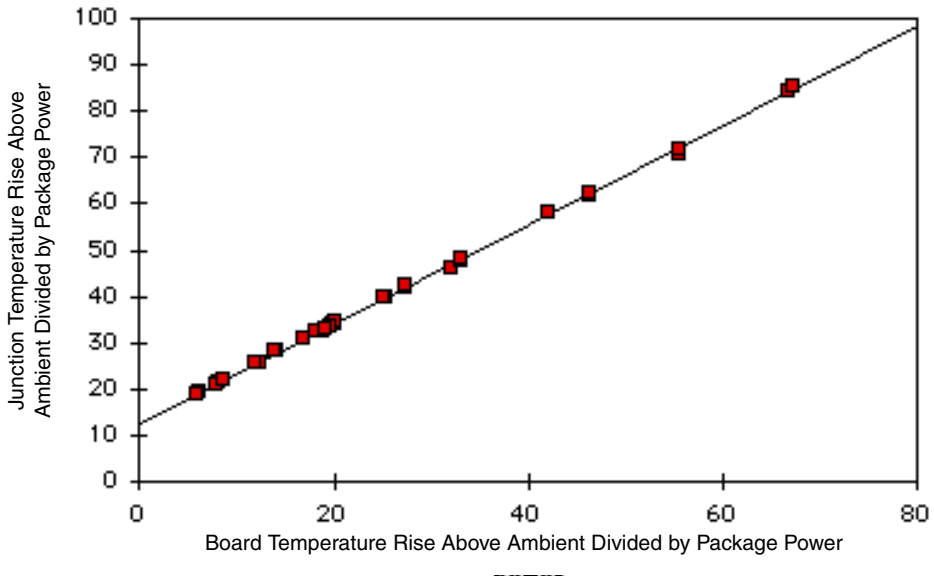



**Figure 2. Effect of Board Temperature Rise on Thermal Behavior**

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 7.6 References

| | |
|---|---|
| Semiconductor Equipment and Materials International<br>805 East Middlefield Rd.<br>Mountain View, CA 94043 | (415) 964-5111 |
| MIL-SPEC and EIA/JESD (JEDEC) Specifications<br>(Available from Global Engineering Documents) | 800-854-7179 or<br>303-397-7956 |
| JEDEC Specifications | http://www.jedec.org |

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 8 Layout Practices

Each $V_{DD}$ pin on the MPC860 should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The $V_{DD}$ power supply should be bypassed to ground using at least four 0.1 µF-bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{DD}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board employing two inner layers as $V_{CC}$ and GND planes is recommended.

All output pins on the MPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6 inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 9 Bus Signal Timing

Table 7 provides the bus operation timing for the MPC860 at 33, 40, 50, and 66 MHz.

The maximum bus speed supported by the MPC860 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC860 used at 80 MHz must be configured for a 40-MHz bus).

The timing for the MPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

**Table 7. Bus Operation Timings**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | CLKOUT period | 30.30 | 30.30 | 25.00 | 30.30 | 20.00 | 30.30 | 15.15 | 30.30 | ns |
| B1a | EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2) | –0.90 | 0.90 | –0.90 | 0.90 | –0.90 | 0.90 | –0.90 | 0.90 | ns |
| B1b | EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10) | –2.30 | 2.30 | –2.30 | 2.30 | –2.30 | 2.30 | –2.30 | 2.30 | ns |
| B1c | CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2)[1] | –0.60 | 0.60 | –0.60 | 0.60 | –0.60 | 0.60 | –0.60 | 0.60 | ns |
| B1d | CLKOUT phase jitter[1] | –2.00 | 2.00 | –2.00 | 2.00 | –2.00 | 2.00 | –2.00 | 2.00 | ns |
| B1e | CLKOUT frequency jitter (MF < 10)[1] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B1f | CLKOUT frequency jitter (10 < MF < 500)[1] | — | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | % |
| B1g | CLKOUT frequency jitter (MF > 500)[1] | — | 3.00 | — | 3.00 | — | 3.00 | — | 3.00 | % |
| B1h | Frequency jitter on EXTCLK[2] | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B2 | CLKOUT pulse width low | 12.12 | — | 10.00 | — | 8.00 | — | 6.06 | — | ns |
| B3 | CLKOUT width high | 12.12 | — | 10.00 | — | 8.00 | — | 6.06 | — | ns |
| B4 | CLKOUT rise time[3] | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5[33] | CLKOUT fall time[3] | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4] | 7.58 | — | 6.25 | — | 5.00 | — | 3.80 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3) $\overline{BDIP}$, PTR valid | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B8b | CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [4] | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B11 | CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion | 7.58 | 13.58 | 6.25 | 12.25 | 5.00 | 11.00 | 3.80 | 11.29 | ns |
| B11a | CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) | 2.50 | 9.25 | 2.50 | 9.25 | 2.50 | 9.25 | 2.50 | 9.75 | ns |
| B12 | CLKOUT to $\overline{TS}$, $\overline{BB}$ negation | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 8.54 | ns |
| B12a | CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) | 2.50 | 11.00 | 2.50 | 11.00 | 2.50 | 11.00 | 2.50 | 9.00 | ns |
| B13 | CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z | 7.58 | 21.58 | 6.25 | 20.25 | 5.00 | 19.00 | 3.80 | 14.04 | ns |
| B13a | CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B14 | CLKOUT to $\overline{TEA}$ assertion | 2.50 | 10.00 | 2.50 | 10.00 | 2.50 | 10.00 | 2.50 | 9.00 | ns |
| B15 | CLKOUT to $\overline{TEA}$ High-Z | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | $\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) | 9.75 | — | 9.75 | — | 9.75 | — | 6.00 | — | ns |
| B16a | $\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) | 10.00 | — | 10.00 | — | 10.00 | — | 4.50 | — | ns |
| B16b | $\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time)[5] | 8.50 | — | 8.50 | — | 8.50 | — | 4.00 | — | ns |
| B17 | CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |
| B17a | CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B18 | D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time)[6] | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B19 | CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time)[6] | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |
| B20 | D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time)[7] | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B21 | CLKOUT falling edge to D(0:31), DP(0:3) valid (hold time)[7] | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B22 | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 | — | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | ns |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 | 10.86 | 17.99 | 8.88 | 16.00 | 7.00 | 14.13 | 5.18 | 12.31 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B23 | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0, and CSNT = 0 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | ns |
| B24 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B24a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B25 | CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B26 | CLKOUT rising edge to $\overline{OE}$ negated | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | ns |
| B27 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 | 35.88 | — | 29.25 | — | 23.00 | — | 16.94 | — | ns |
| B27a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 | 43.45 | — | 35.50 | — | 28.00 | — | 20.73 | — | ns |
| B28 | CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1, EBDF = 0 | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | — | 14.33 | — | 13.00 | — | 11.75 | — | 10.54 | ns |
| B28c | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, 1, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 | 10.86 | 17.99 | 8.88 | 16.00 | 7.00 | 14.13 | 5.18 | 12.31 | ns |
| B28d | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | — | 17.99 | — | 16.00 | — | 14.13 | — | 12.31 | ns |
| B29 | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access CSNT = 0, EBDF = 0 | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B29a | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 | 13.15 | — | 10.5 | — | 8.00 | — | 5.58 | — | ns |
| B29b | $\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0, 1, and CSNT = 0 | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B29c | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | 13.15 | — | 10.5 | — | 8.00 | — | 5.58 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B29d | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 | 43.45 | — | 35.5 | — | 28.00 | — | 20.73 | — | ns |
| B29e | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | 43.45 | — | 35.5 | — | 28.00 | — | 29.73 | — | ns |
| B29f | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 | 8.86 | — | 6.88 | — | 5.00 | — | 3.18 | — | ns |
| B29g | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 8.86 | — | 6.88 | — | 5.00 | — | 3.18 | — | ns |
| B29h | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B29i | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B30 | $\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [8] | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B30a | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, or ACS = 11, EBDF = 0 | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B30b | $\overline{WE}$(0:3) negated to A(0:31), invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31), Invalid GPCM, write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 | 43.45 | — | 35.50 | — | 28.00 | — | 20.73 | — | ns |
| B30c | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, ACS = 11, EBDF = 1 | 8.36 | — | 6.38 | — | 4.50 | — | 2.68 | — | ns |
| B30d | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT =1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B31 | CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid—as requested by control bit CST3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.04 | ns |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM, EBDF = 1 | 13.26 | 17.99 | 11.28 | 16.00 | 9.40 | 14.13 | 7.58 | 12.31 | ns |
| B32 | CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 0 | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid—as requested by control bit BST3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM, EBDF = 1 | 13.26 | 17.99 | 11.28 | 16.00 | 9.40 | 14.13 | 7.58 | 12.31 | ns |
| B33 | CLKOUT falling edge to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B33a | CLKOUT rising edge to $\overline{GPL}$ valid—as requested by control bit GxT3 in the corresponding word in UPM | 7.58 | 14.33 | 6.25 | 13.00 | 5.00 | 11.75 | 3.80 | 10.54 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST4 in the corresponding word in UPM | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST1 in the corresponding word in UPM | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid—as requested by control bit CST2 in the corresponding word in UPM | 20.73 | — | 16.75 | — | 13.00 | — | 9.36 | — | ns |

**Table 7. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B35 | A(0:31), BADDR(28:30) to $\overline{CS}$ valid—as requested by control bit BST4 in the corresponding word in UPM | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST1 in the corresponding word in UPM | 13.15 | — | 10.50 | — | 8.00 | — | 5.58 | — | ns |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid—as requested by control bit BST2 in the corresponding word in UPM | 20.73 | — | 16.75 | — | 13.00 | — | 9.36 | — | ns |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid—as requested by control bit GxT4 in the corresponding word in UPM | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| B37 | UPWAIT valid to CLKOUT falling edge[9] | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid[9] | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge[10] | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | $\overline{AS}$ negation to memory controller signals negation | — | TBD | — | TBD | — | TBD | — | TBD | ns |

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC860 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC860 is selected to work with internal bus arbiter.

5 The timing required for $\overline{BR}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC860 is selected to work with external bus arbiter.

6 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 3 is the control timing diagram.

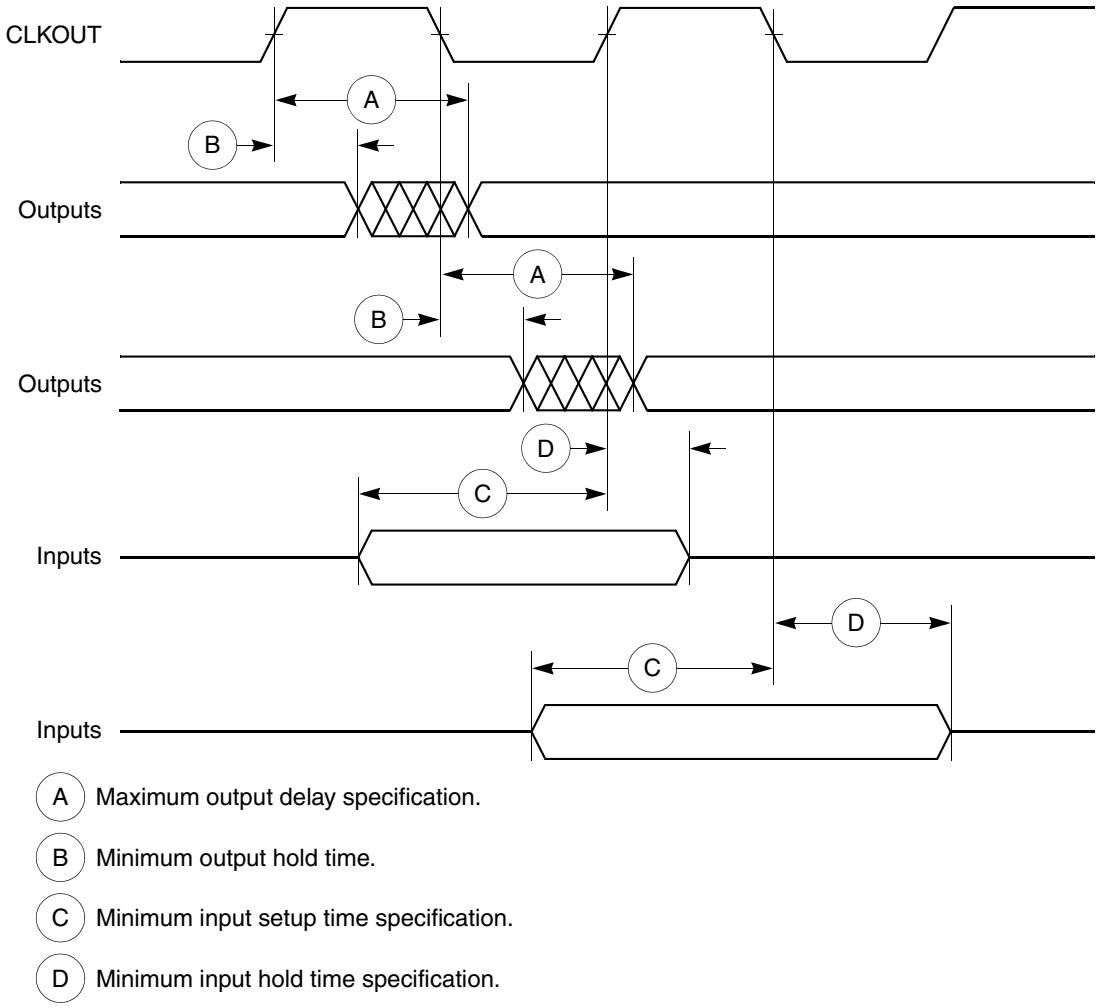



**Figure 3. Control Timing**

Figure 4 provides the timing for the external clock.

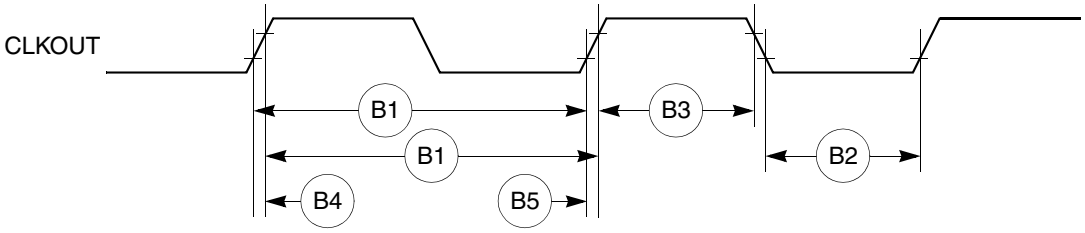



**Figure 4. External Clock Timing**

Figure 5 provides the timing for the synchronous output signals.

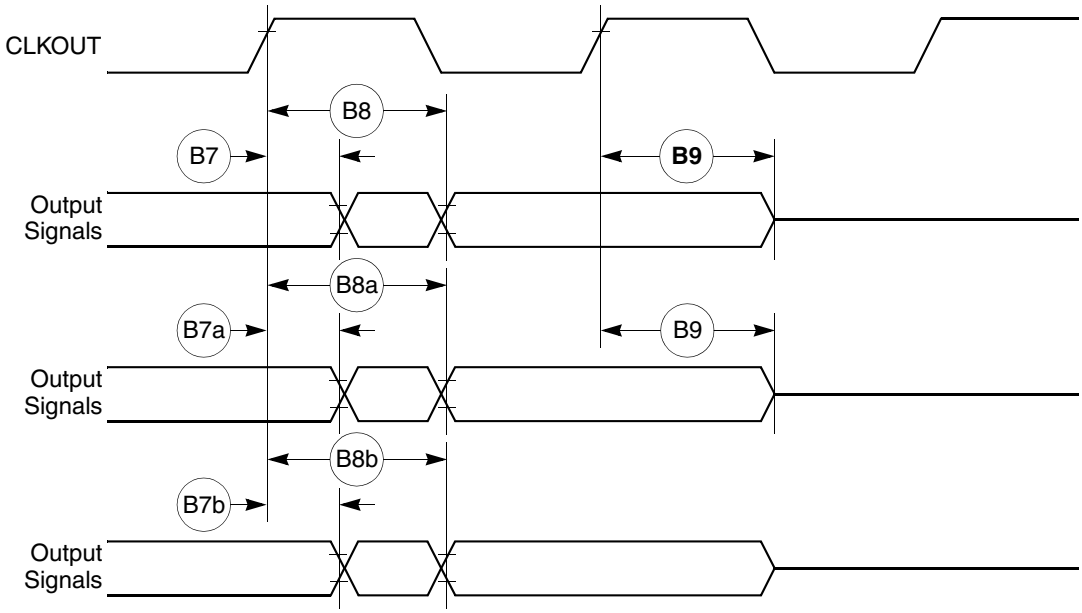



**Figure 5. Synchronous Output Signals Timing**

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

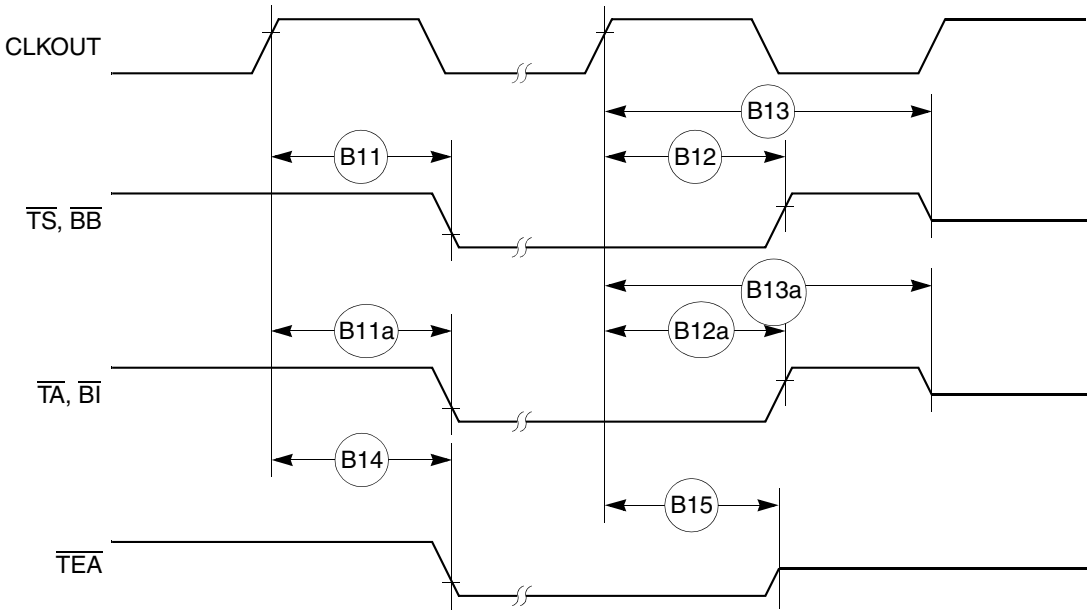



**Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing**

Figure 7 provides the timing for the synchronous input signals.

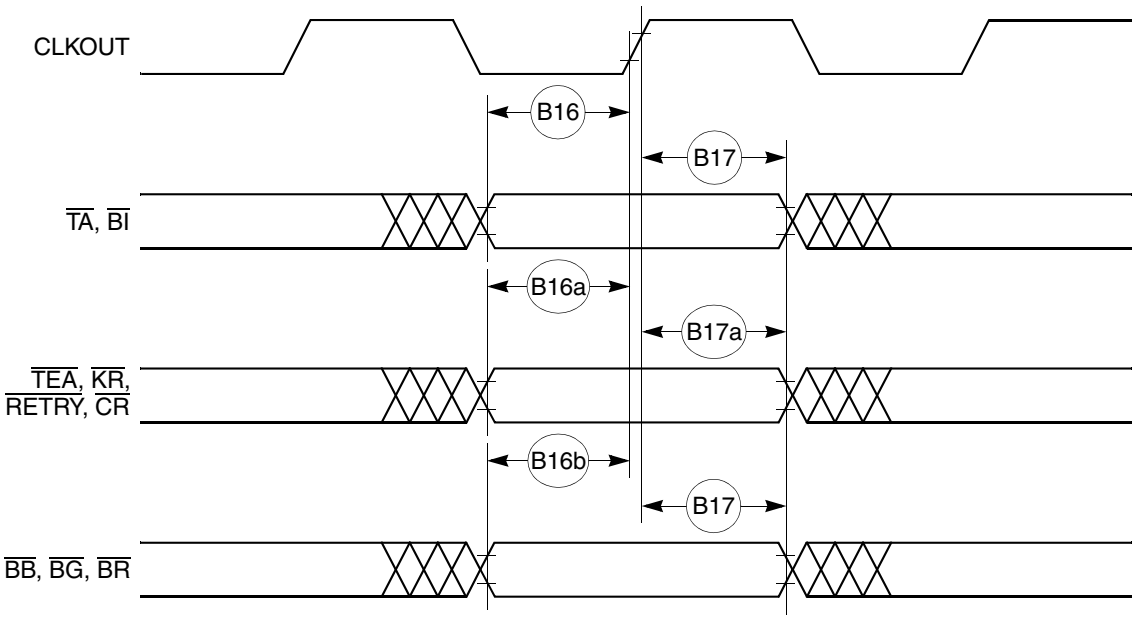



**Figure 7. Synchronous Input Signals Timing**

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

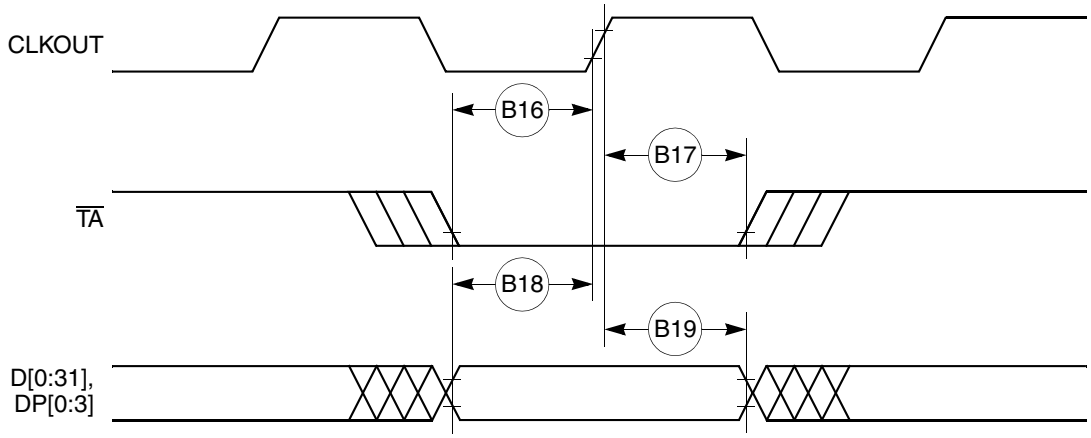



**Figure 8. Input Data Timing in Normal Case**

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

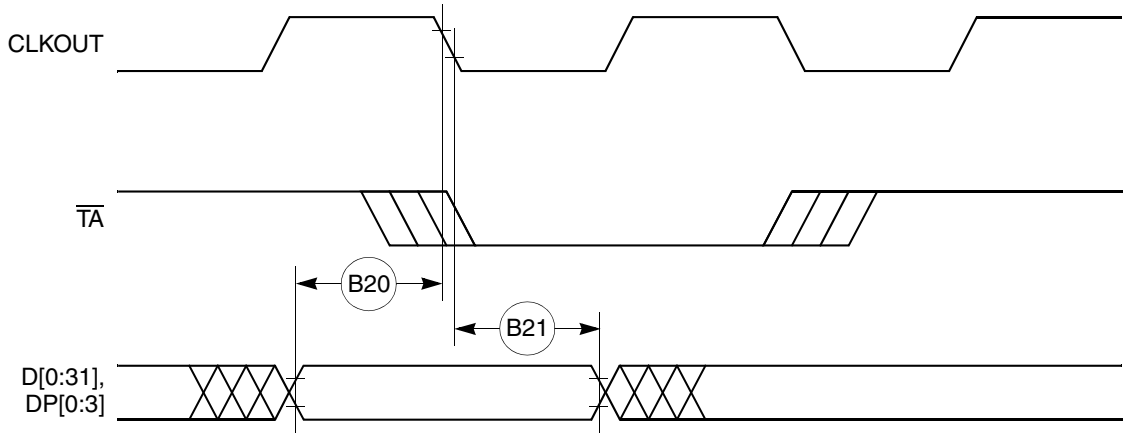



**Figure 9. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1**

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

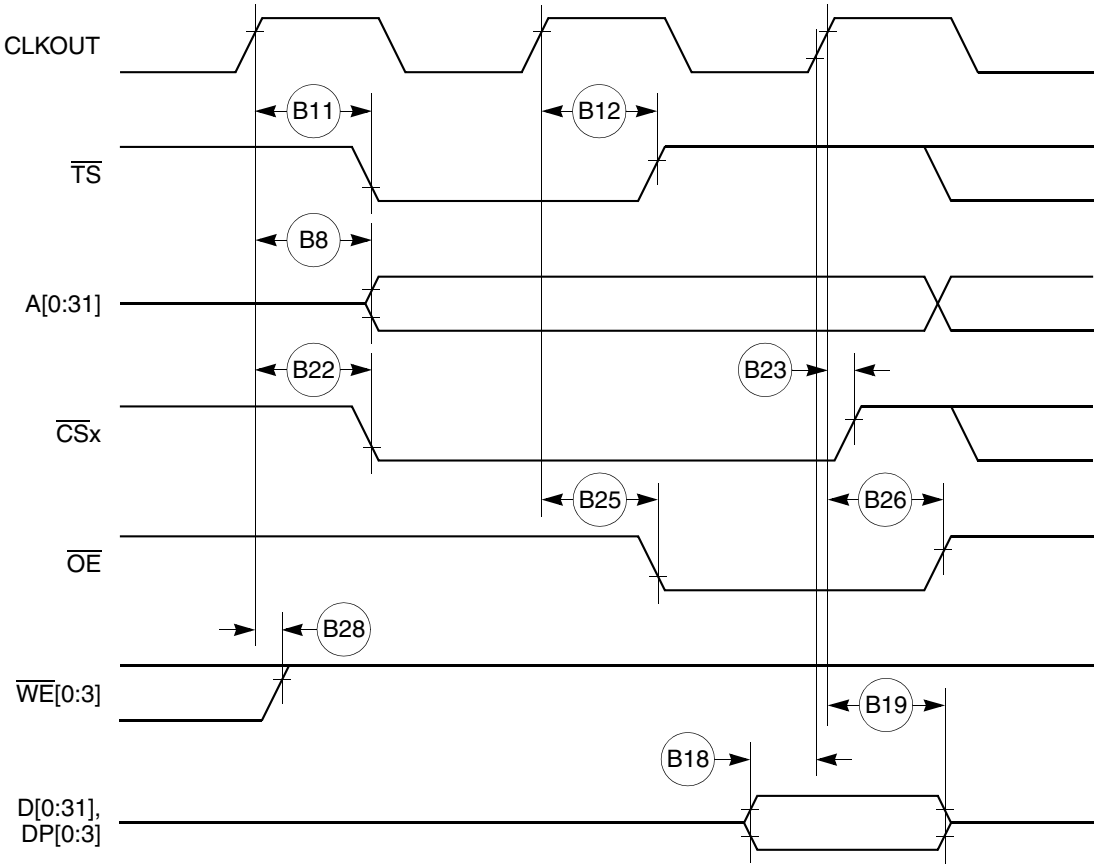



**Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)**

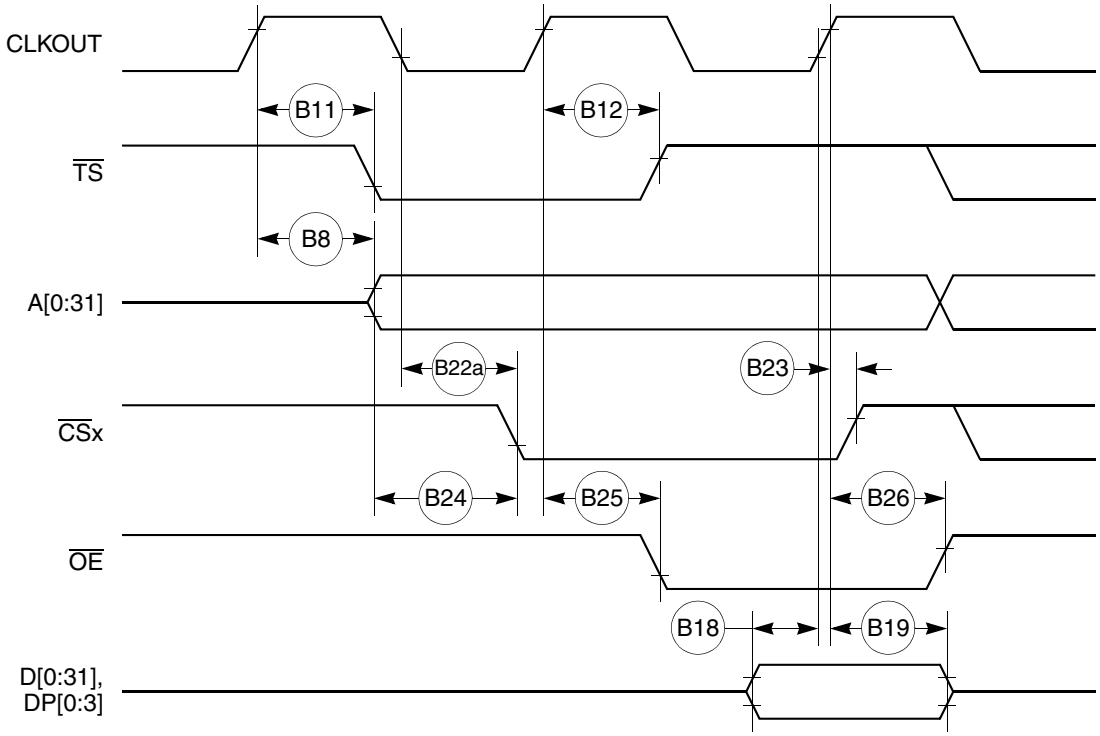



**Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)**

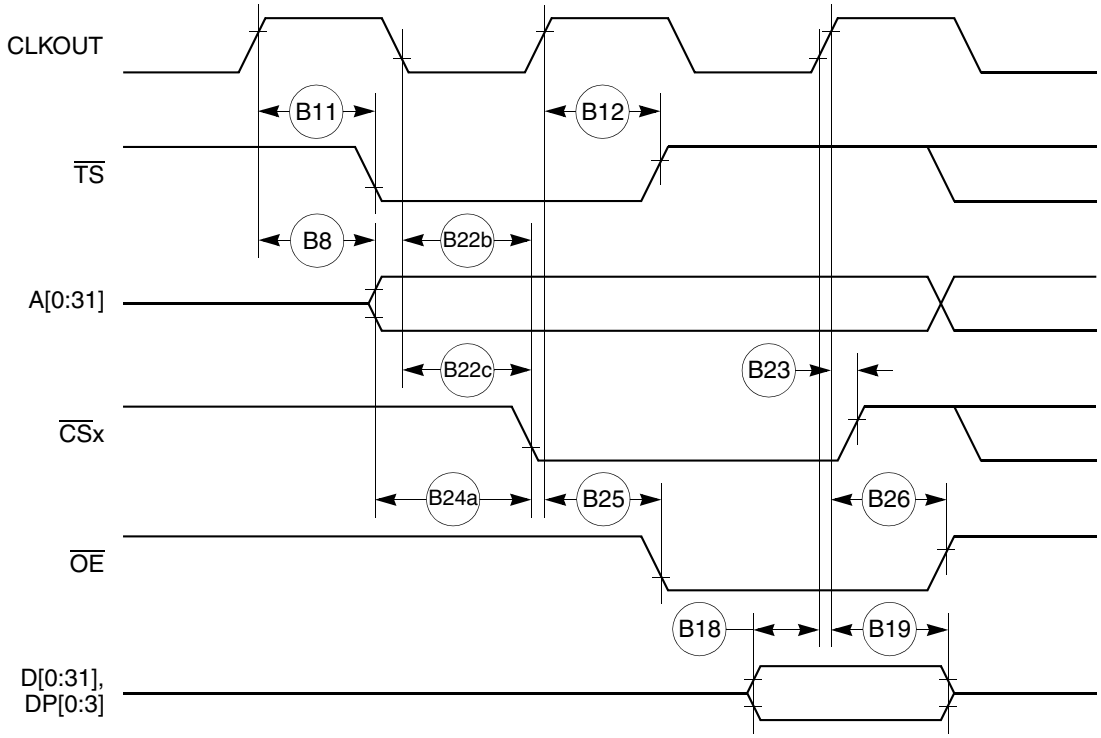



**Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

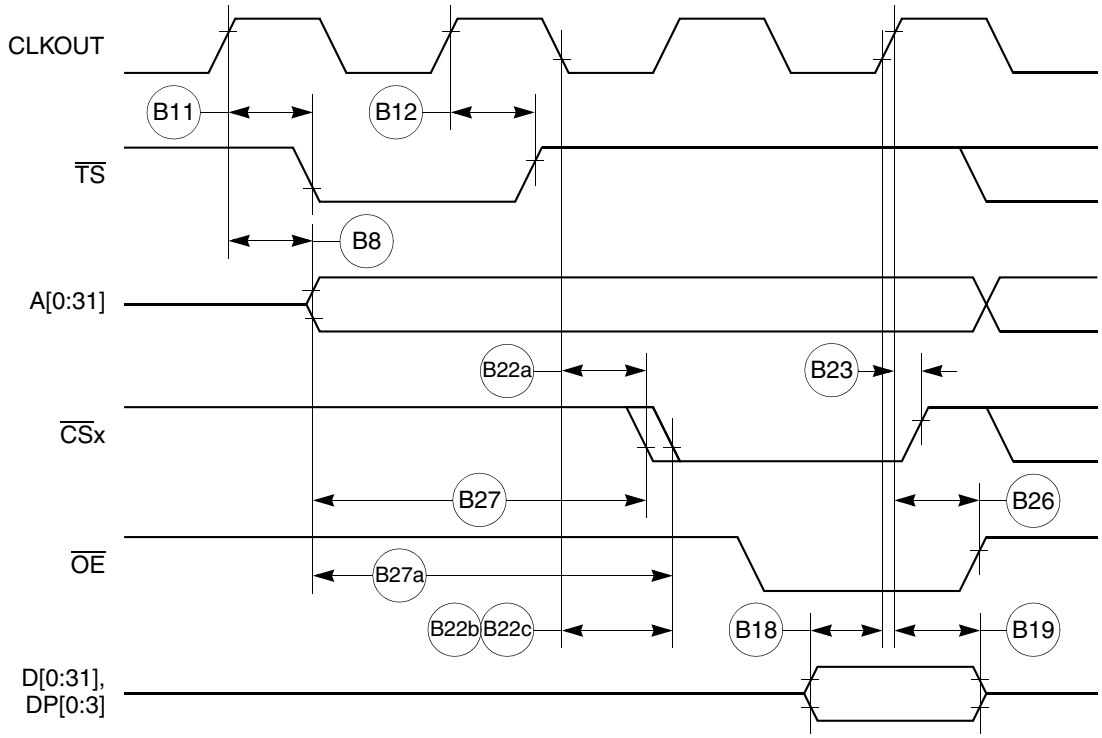



**Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)**

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

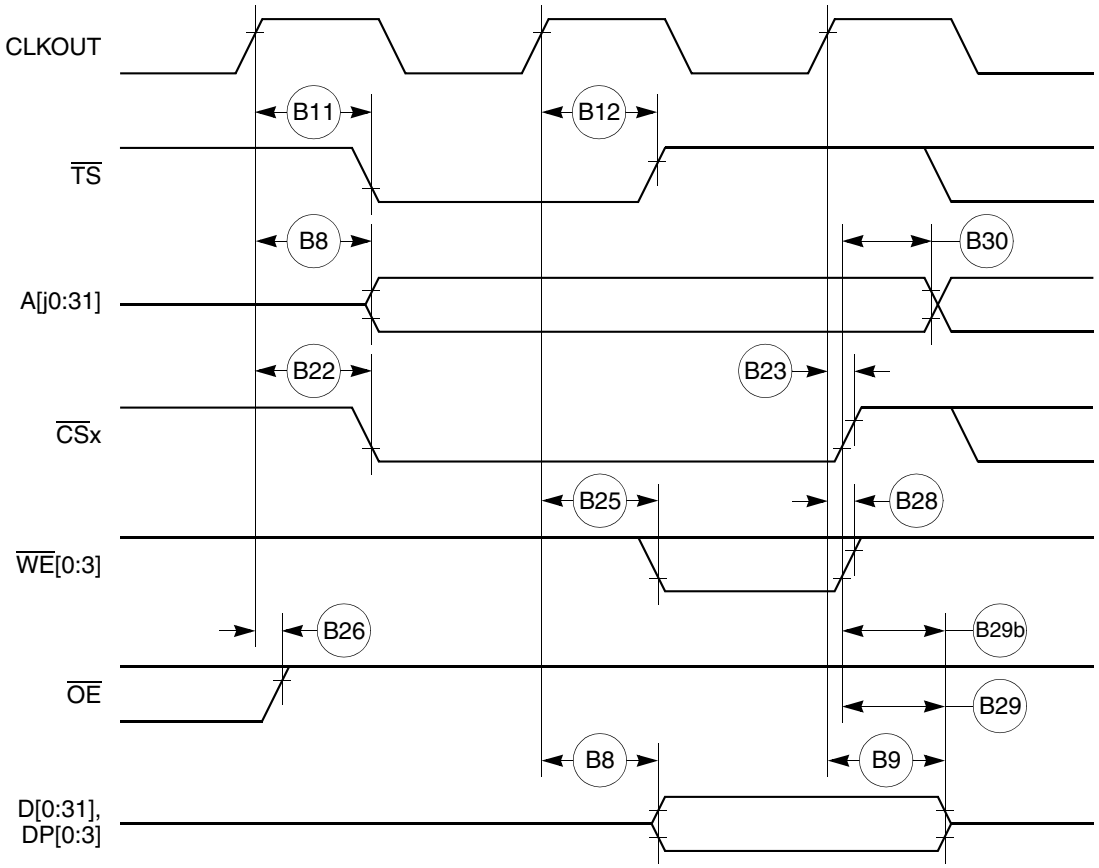



**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)**

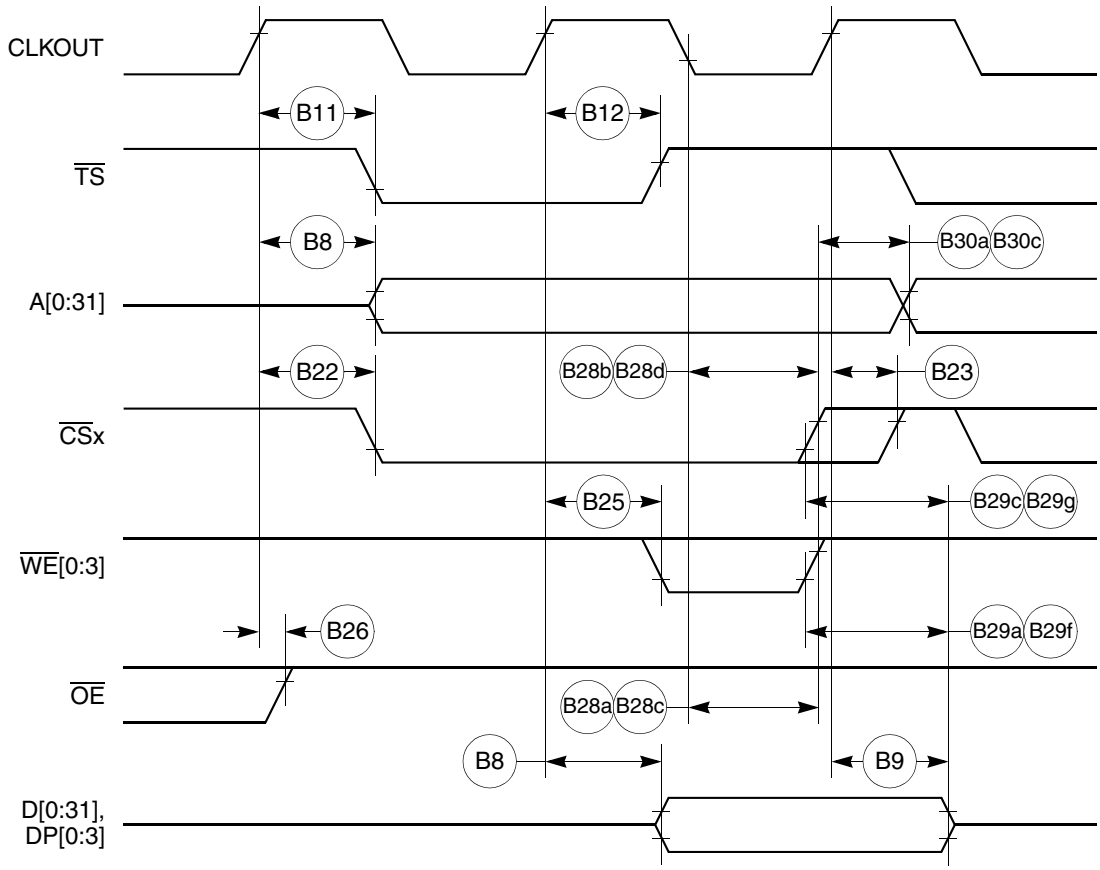



**Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)**

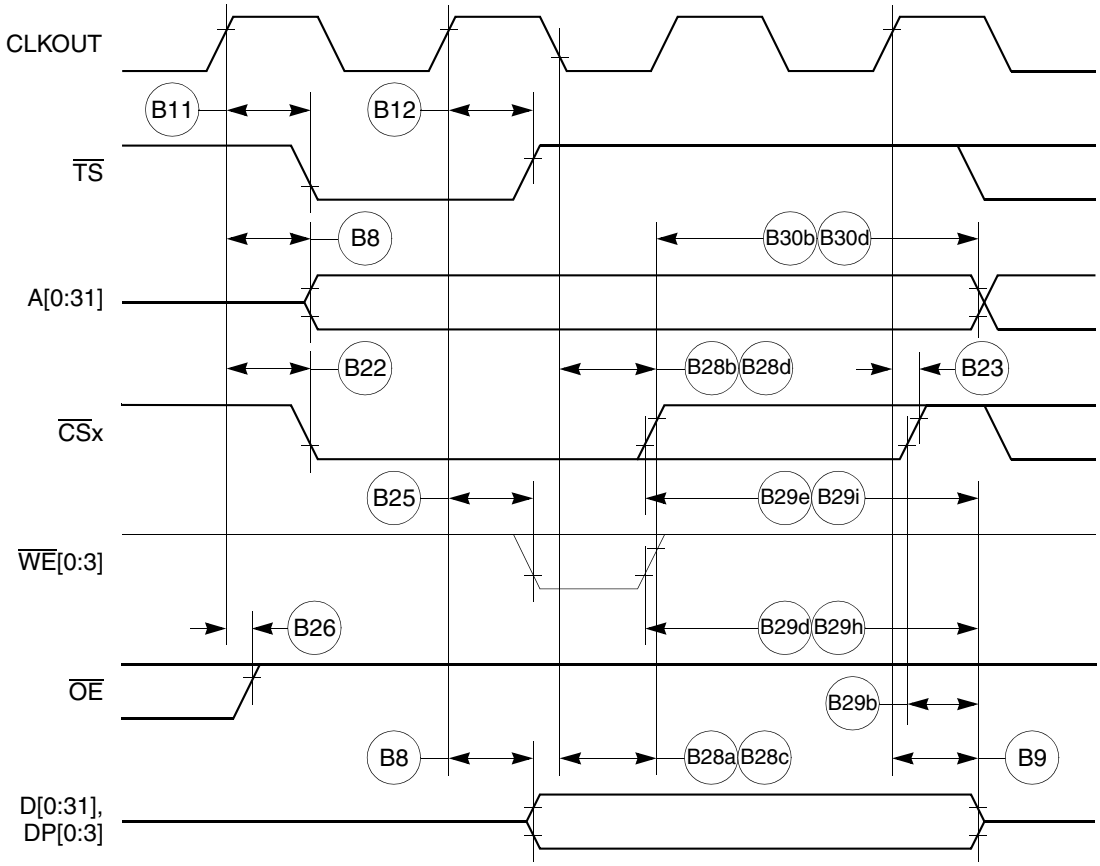



**Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)**

Figure 17 provides the timing for the external bus controlled by the UPM.

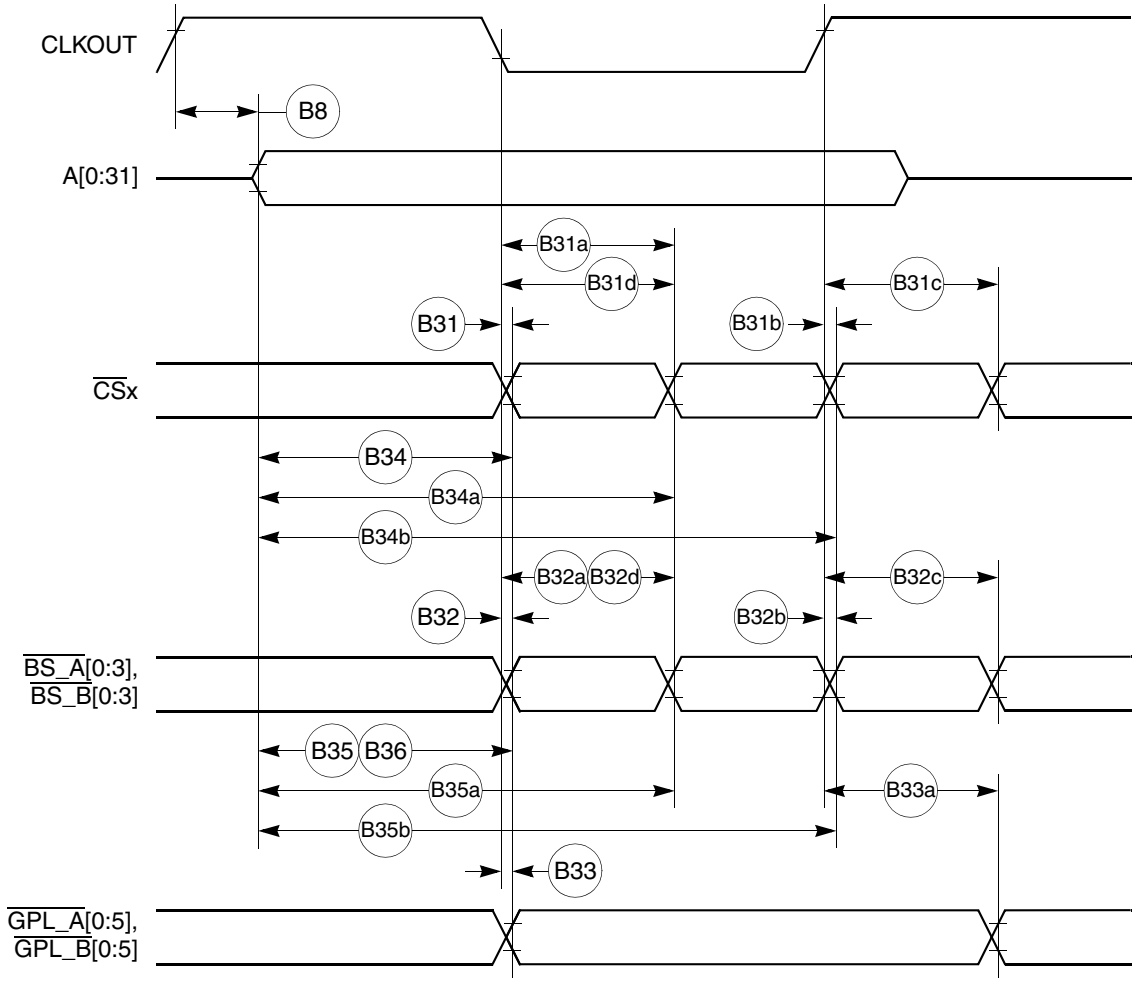



**Figure 17. External Bus Timing (UPM Controlled Signals)**

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

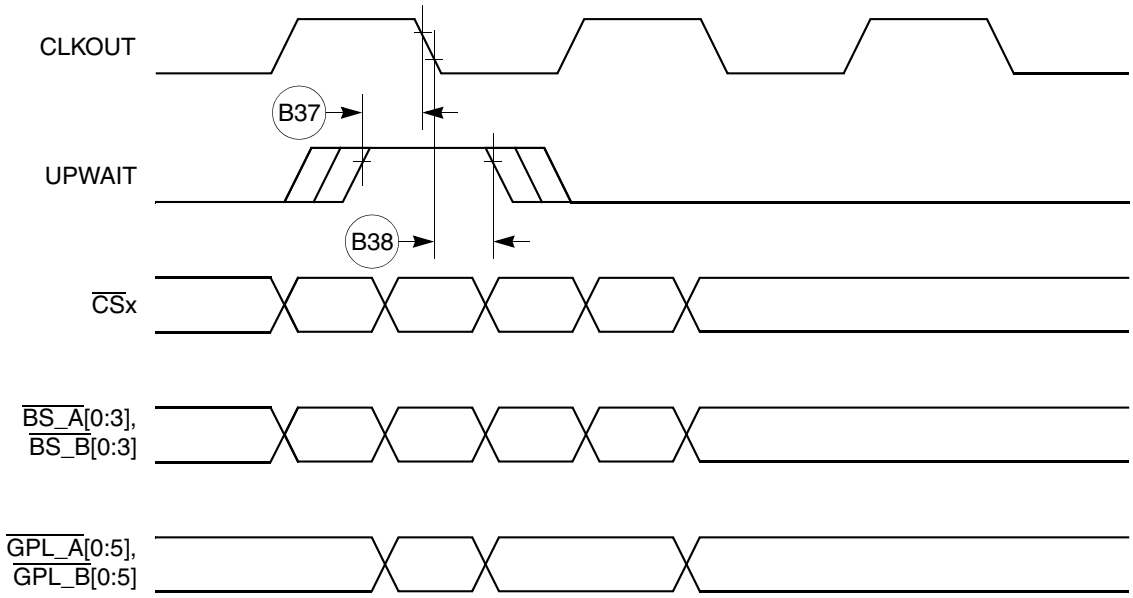



**Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

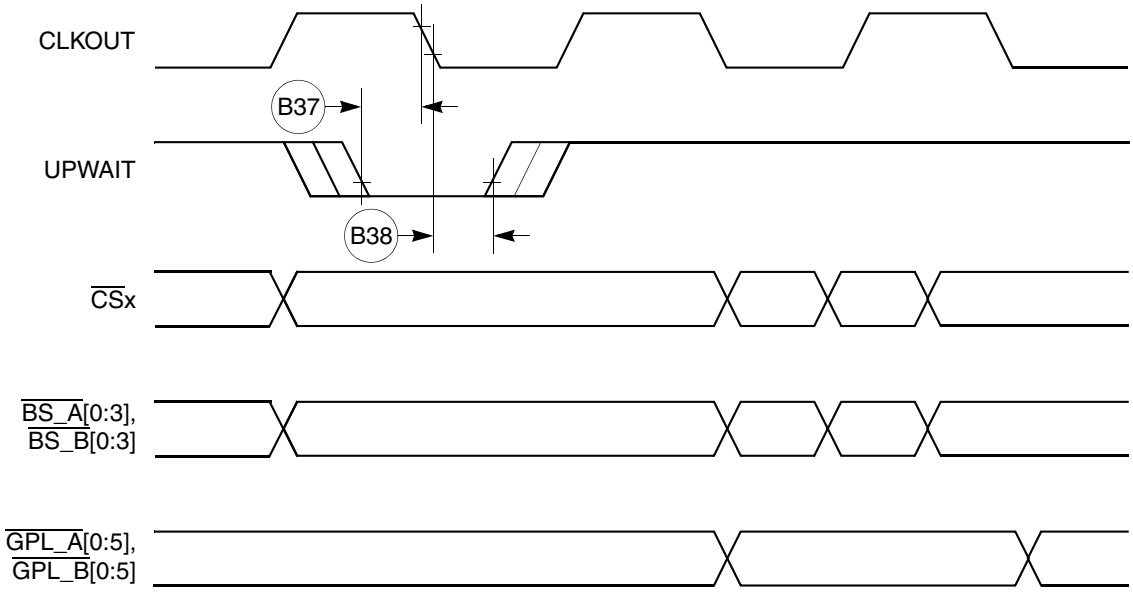



**Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

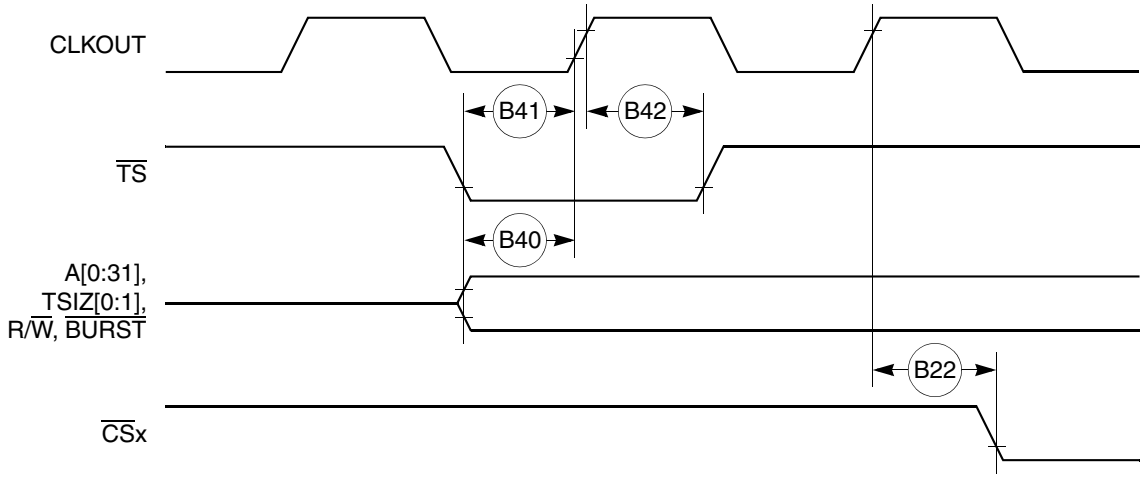



**Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

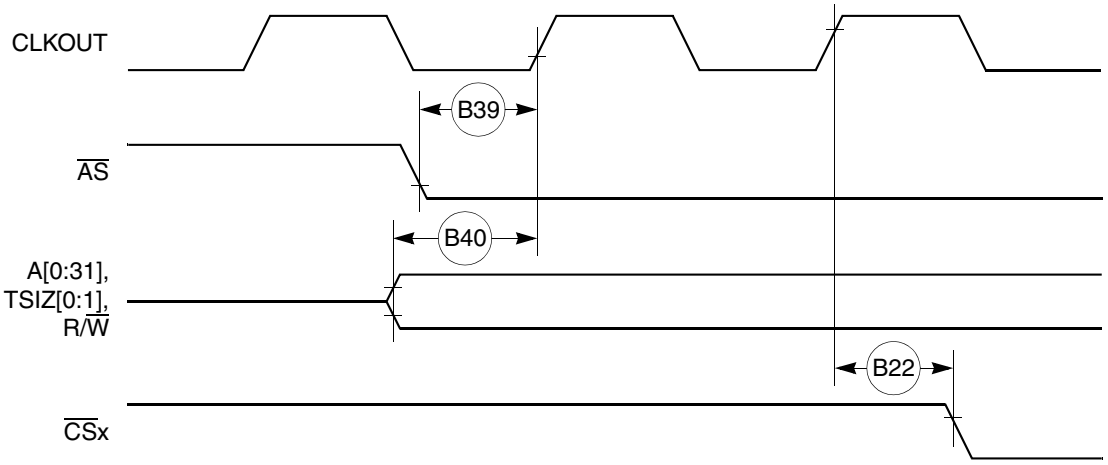



**Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 22 provides the timing for the asynchronous external master control signals negation.

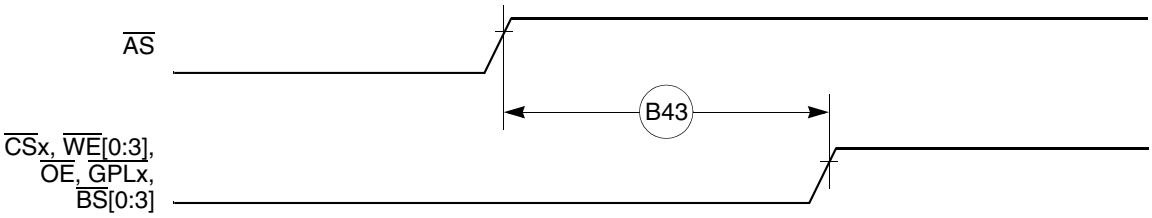



**Figure 22. Asynchronous External Master—Control Signals Negation Timing**

Table 8 provides interrupt timing for the MPC860.

**Table 8. Interrupt Timing**

| Num | Characteristic[1] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| I39 | $\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time) | 6.00 | — | ns |
| I40 | $\overline{\text{IRQ}}$x hold time after CLKOUT | 2.00 | — | ns |
| I41 | $\overline{\text{IRQ}}$x pulse width low | 3.00 | — | ns |
| I42 | $\overline{\text{IRQ}}$x pulse width high | 3.00 | — | ns |
| I43 | $\overline{\text{IRQ}}$x edge-to-edge time | $4 \times T_{CLOCKOUT}$ | — | — |

1 The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level-sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC860 is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

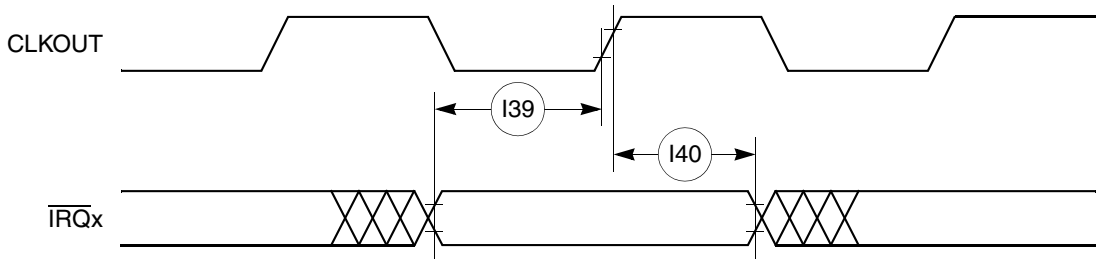



**Figure 23. Interrupt Detection Timing for External Level Sensitive Lines**

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

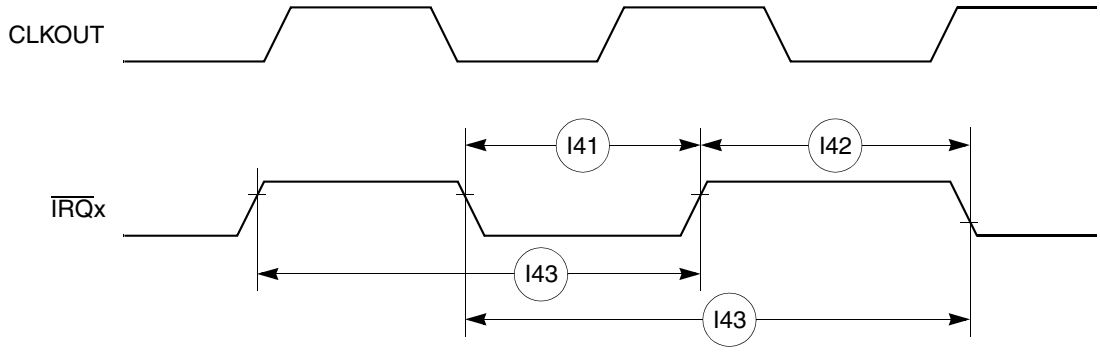



**Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines**

Table 9 shows the PCMCIA timing for the MPC860.

**Table 9. PCMCIA Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P44 | A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted[1] | 20.73 | — | 16.75 | — | 13.00 | — | 9.36 | — | ns |
| P45 | A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] | 28.30 | — | 23.00 | — | 18.00 | — | 13.15 | — | ns |
| P46 | CLKOUT to $\overline{\text{REG}}$ valid | 7.58 | 15.58 | 6.25 | 14.25 | 5.00 | 13.00 | 3.79 | 11.84 | ns |
| P47 | CLKOUT to $\overline{\text{REG}}$ invalid | 8.58 | — | 7.25 | — | 6.00 | — | 4.84 | — | ns |
| P48 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted | 7.58 | 15.58 | 6.25 | 14.25 | 5.00 | 13.00 | 3.79 | 11.84 | ns |
| P49 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated | 7.58 | 15.58 | 6.25 | 14.25 | 5.00 | 13.00 | 3.79 | 11.84 | ns |
| P50 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time | — | 11.00 | | 11.00 | — | 11.00 | — | 11.00 | ns |
| P51 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | ns |
| P52 | CLKOUT to ALE assert time | 7.58 | 15.58 | 6.25 | 14.25 | 5.00 | 13.00 | 3.79 | 10.04 | ns |
| P53 | CLKOUT to ALE negate time | — | 15.58 | | 14.25 | — | 13.00 | — | 11.84 | ns |
| P54 | $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] | 5.58 | — | 4.25 | — | 3.00 | — | 1.79 | — | ns |
| P55 | $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| P56 | CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, “PCMCIA Interface,” in the *MPC860 PowerQUICC™ Family User’s Manual*.

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

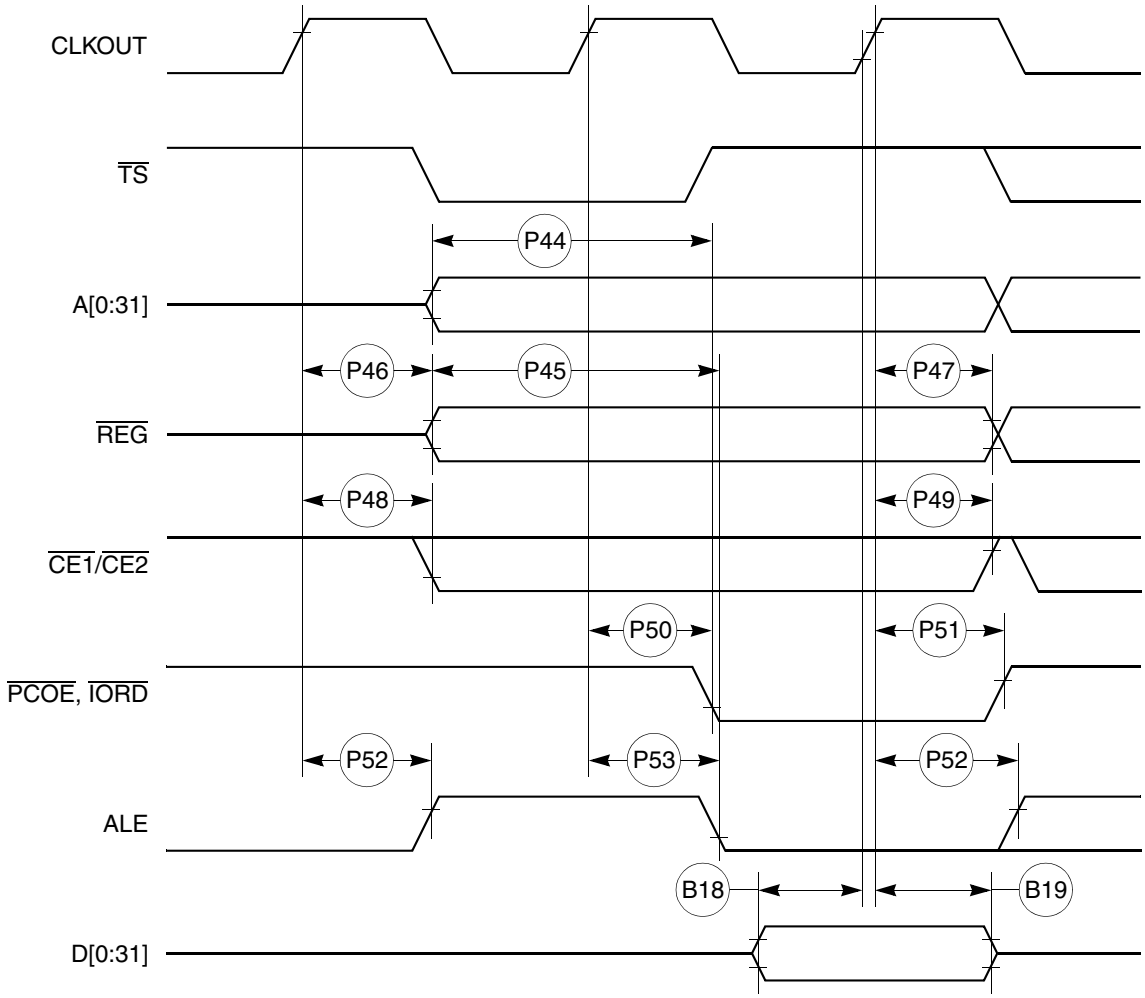



**Figure 25. PCMCIA Access Cycle Timing External Bus Read**

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

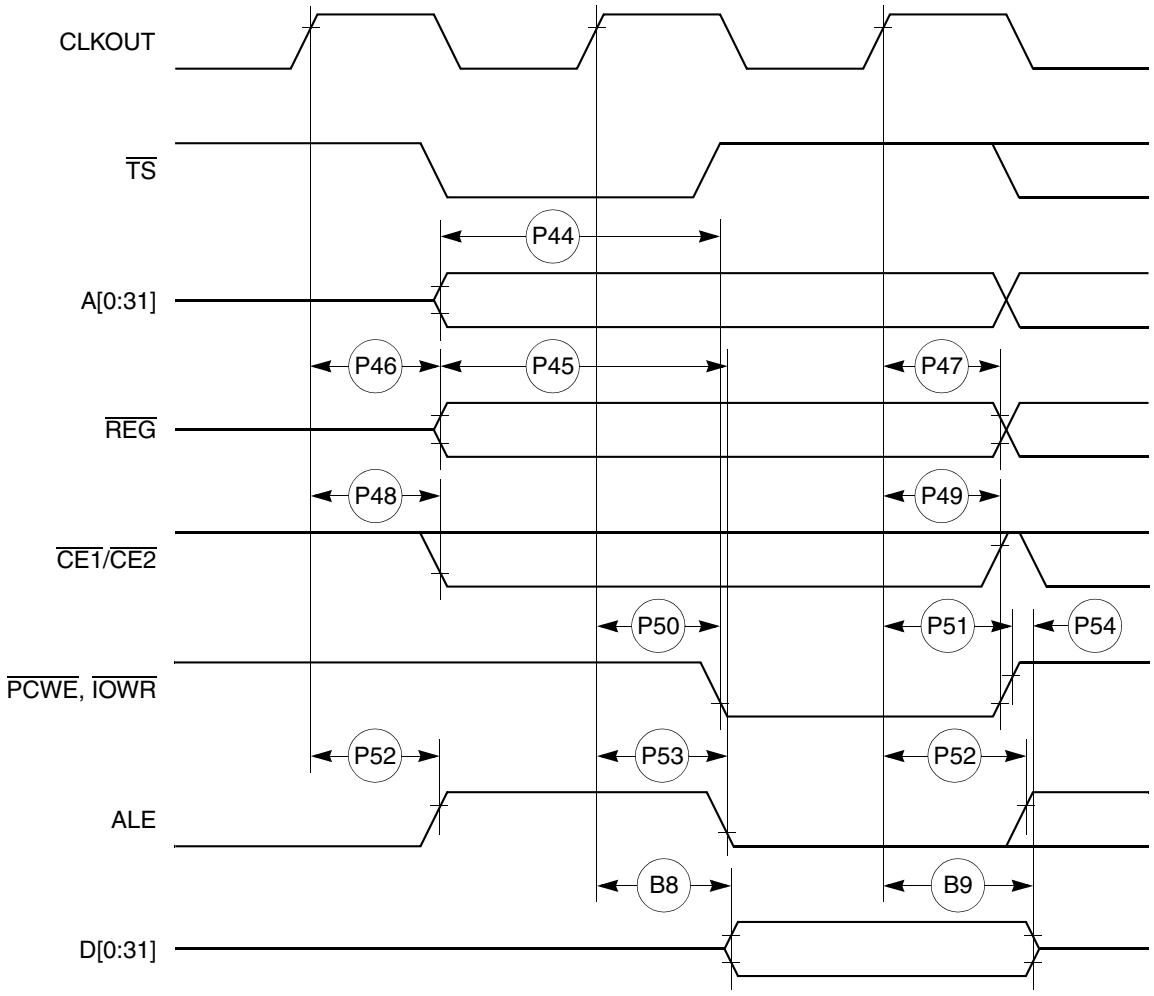



**Figure 26. PCMCIA Access Cycle Timing External Bus Write**

Figure 27 provides the PCMCIA WAIT signal detection timing.

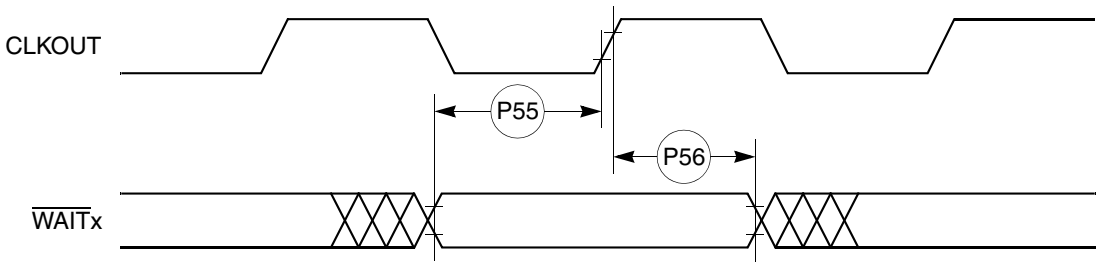



**Figure 27. PCMCIA WAIT Signal Detection Timing**

Table 10 shows the PCMCIA port timing for the MPC860.

**Table 10. PCMCIA Port Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx valid | — | 19.00 | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive[1] | 25.73 | — | 21.75 | — | 18.00 | — | 14.36 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge | 5.00 | — | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |

1 OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC860.

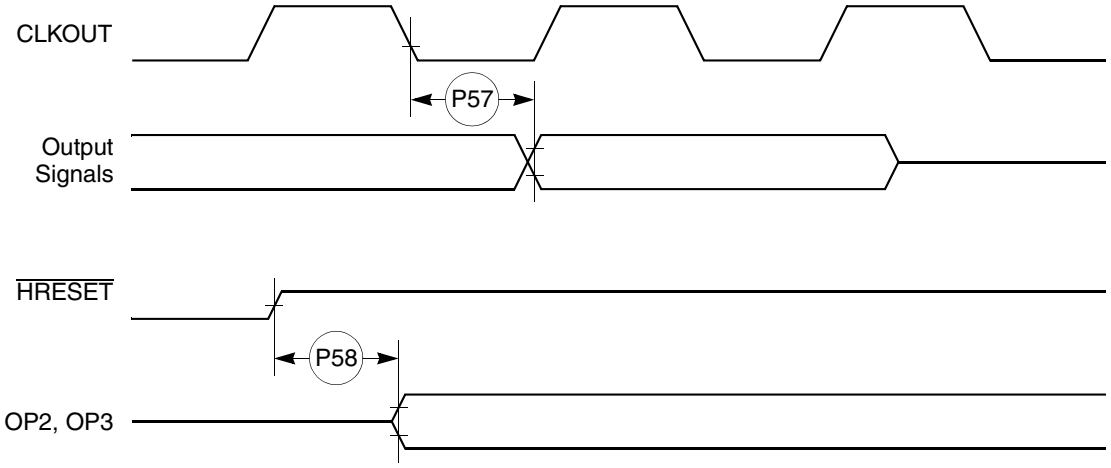



**Figure 28. PCMCIA Output Port Timing**

Figure 29 provides the PCMCIA output port timing for the MPC860.

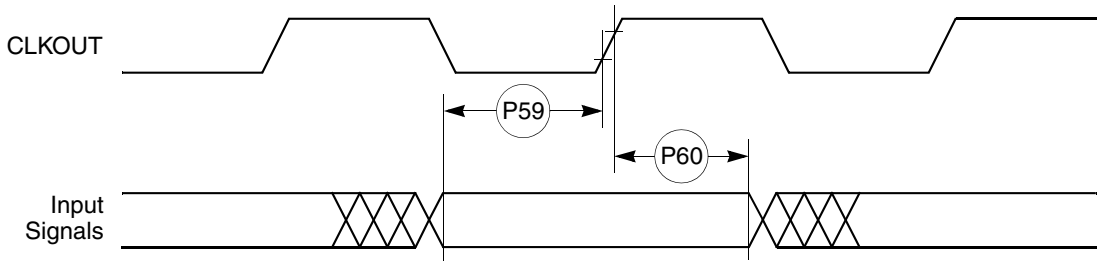



**Figure 29. PCMCIA Input Port Timing**

Table 11 shows the debug port timing for the MPC860.

**Table 11. Debug Port Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| P61 | DSCK cycle time | $3 \times T_{CLOCKOUT}$ | — | — |
| P62 | DSCK clock pulse width | $1.25 \times T_{CLOCKOUT}$ | — | — |
| P63 | DSCK rise and fall times | 0.00 | 3.00 | ns |
| P64 | DSDI input data setup time | 8.00 | — | ns |
| P65 | DSDI data hold time | 5.00 | — | ns |
| P66 | DSCK low to DSDO data valid | 0.00 | 15.00 | ns |
| P67 | DSCK low to DSDO invalid | 0.00 | 2.00 | ns |

Figure 30 provides the input timing for the debug port clock.

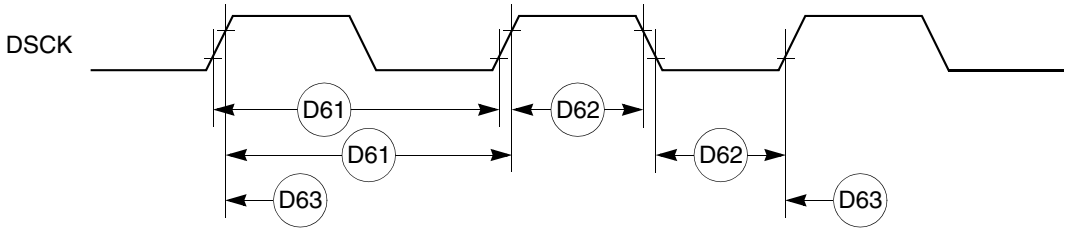



**Figure 30. Debug Port Clock Input Timing**

Figure 31 provides the timing for the debug port.

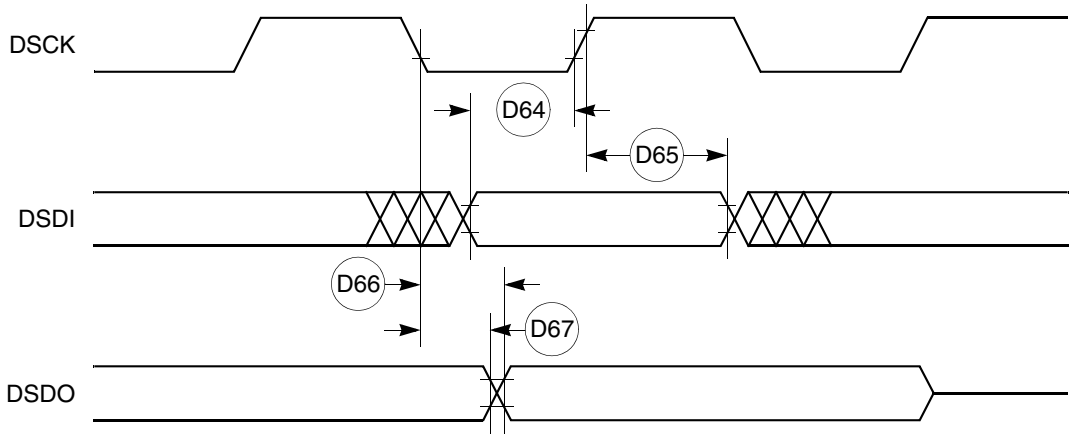



**Figure 31. Debug Port Timings**

Table 12 shows the reset timing for the MPC860.

**Table 12. Reset Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width | 515.15 | — | 425.00 | | 340.00 | — | 257.58 | — | ns |
| R72 | — | — | — | — | — | — | — | — | — | |
| R73 | Configuration data to HRESET rising edge setup time | 504.55 | — | 425.00 | — | 350.00 | — | 277.27 | — | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time | 350.00 | — | 350.00 | — | 350.00 | — | 350.00 | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive | — | 25.00 | | 25.00 | — | 25.00 | — | 25.00 | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R79 | CLKOUT of last rising edge before chip three-state $\overline{\text{HRESET}}$ to data out high impedance | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R80 | DSDI, DSCK setup | 90.91 | — | 75.00 | — | 60.00 | — | 45.45 | — | ns |
| R81 | DSDI, DSCK hold time | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample | 242.42 | — | 200.00 | — | 160.00 | — | 121.21 | — | ns |

Figure 32 shows the reset timing for the data bus configuration.

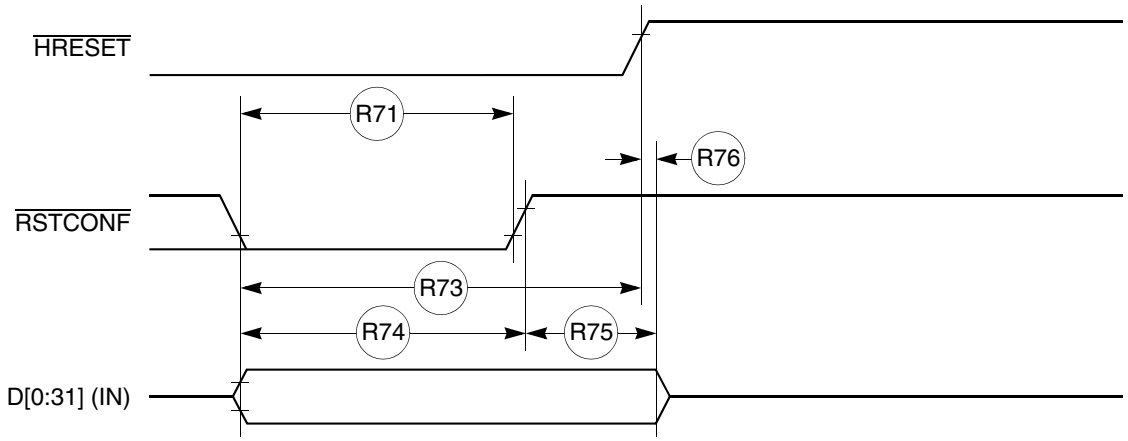



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.

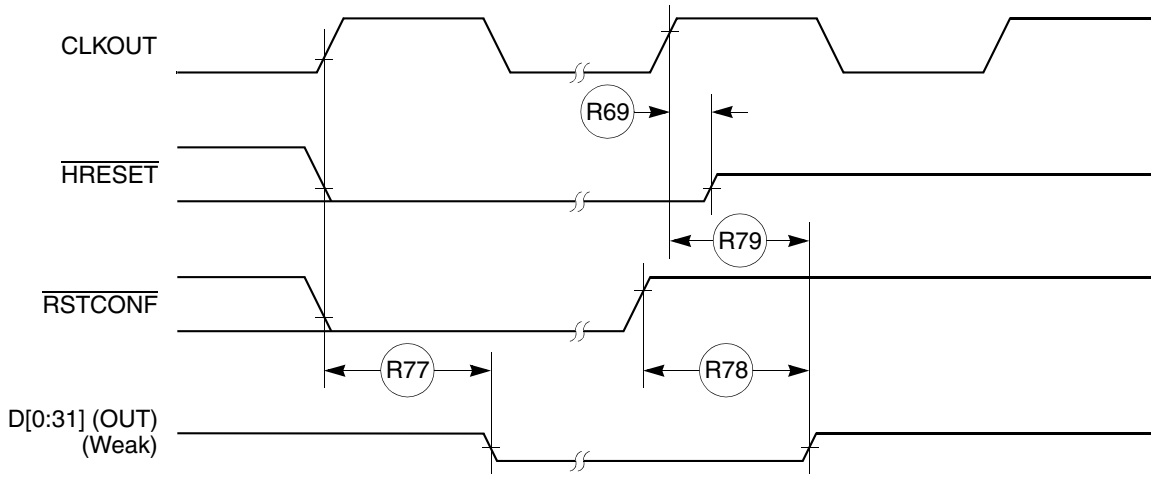



**Figure 33. Reset Timing—Data Bus Weak Drive During Configuration**

Figure 34 provides the reset timing for the debug port configuration.

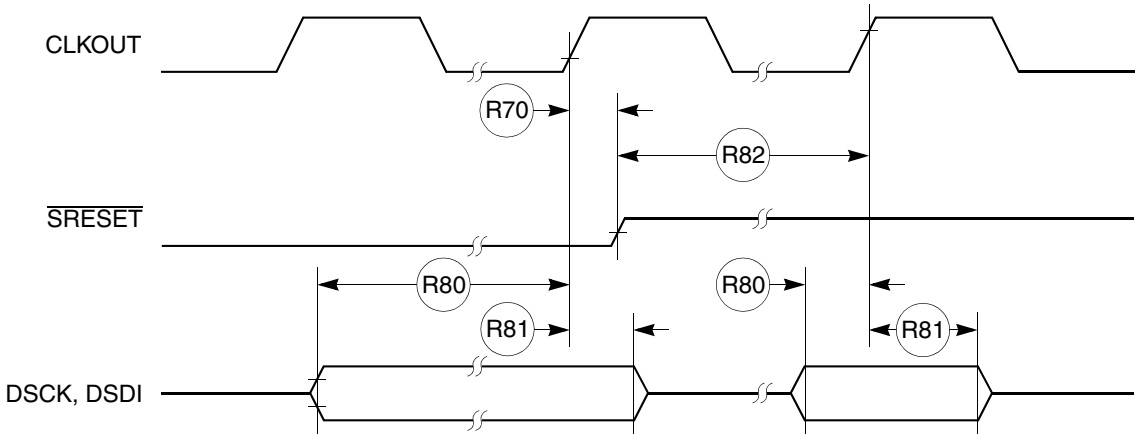



**Figure 34. Reset Timing—Debug Port Configuration**

# 10 IEEE 1149.1 Electrical Specifications

Table 13 provides the JTAG timings for the MPC860 shown in Figure 35 through Figure 38.

**Table 13. JTAG Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | ns |

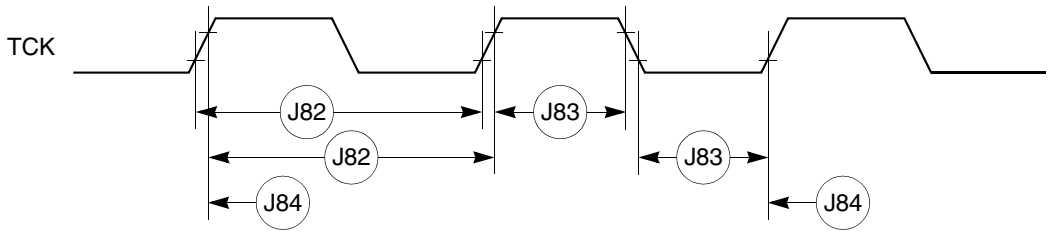



**Figure 35. JTAG Test Clock Input Timing**

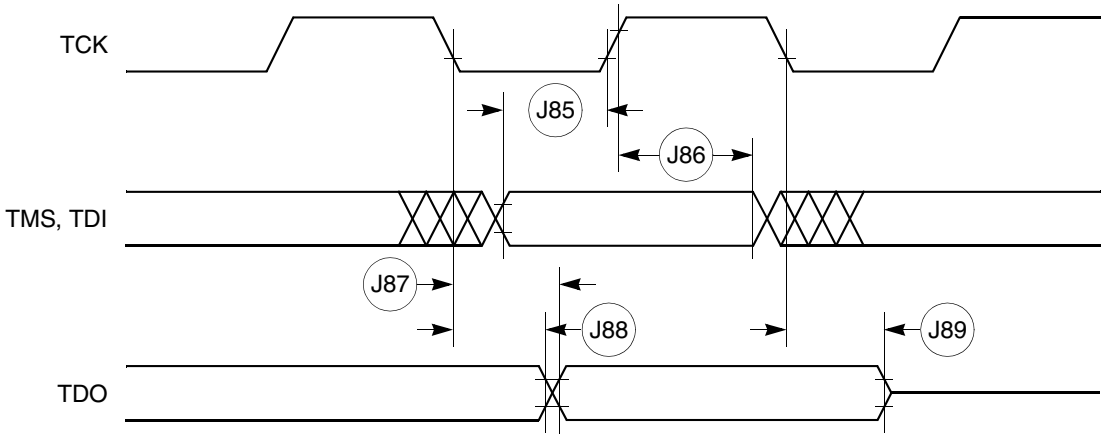



**Figure 36. JTAG Test Access Port Timing Diagram**

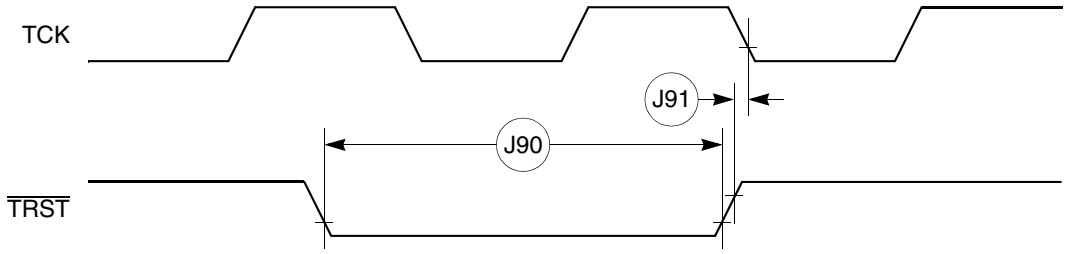



**Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram**

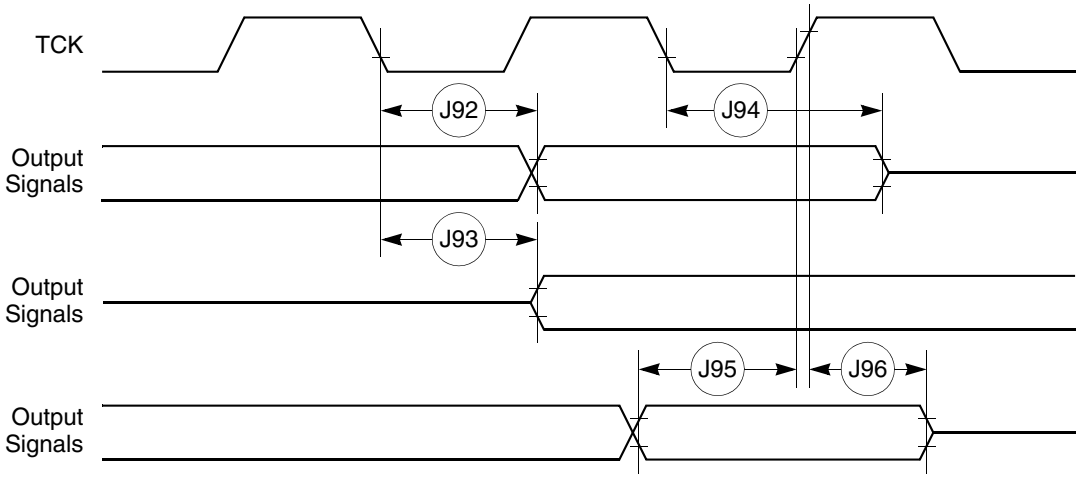



**Figure 38. Boundary Scan (JTAG) Timing Diagram**

# 11 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC860.

## 11.1 PIP/PIO AC Electrical Specifications

Table 14 provides the PIP/PIO AC timings as shown in Figure 39 through Figure 43.

**Table 14. PIP/PIO Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 21 | Data-in setup time to STBI low | 0 | — | ns |
| 22 | Data-in hold time to STBI high | 2.5 – t3[1] | — | CLK |
| 23 | STBI pulse width | 1.5 | — | CLK |
| 24 | STBO pulse width | 1 CLK – 5 ns | — | ns |
| 25 | Data-out setup time to STBO low | 2 | — | CLK |
| 26 | Data-out hold time from STBO high | 5 | — | CLK |
| 27 | STBI low to STBO low (Rx interlock) | — | 2 | CLK |
| 28 | STBI low to STBO high (Tx interlock) | 2 | — | CLK |
| 29 | Data-in setup time to clock high | 15 | — | ns |
| 30 | Data-in hold time from clock high | 7.5 | — | ns |
| 31 | Clock low to data-out valid (CPU writes data, control, or direction) | — | 25 | ns |

[1] t3 = Specification 23.

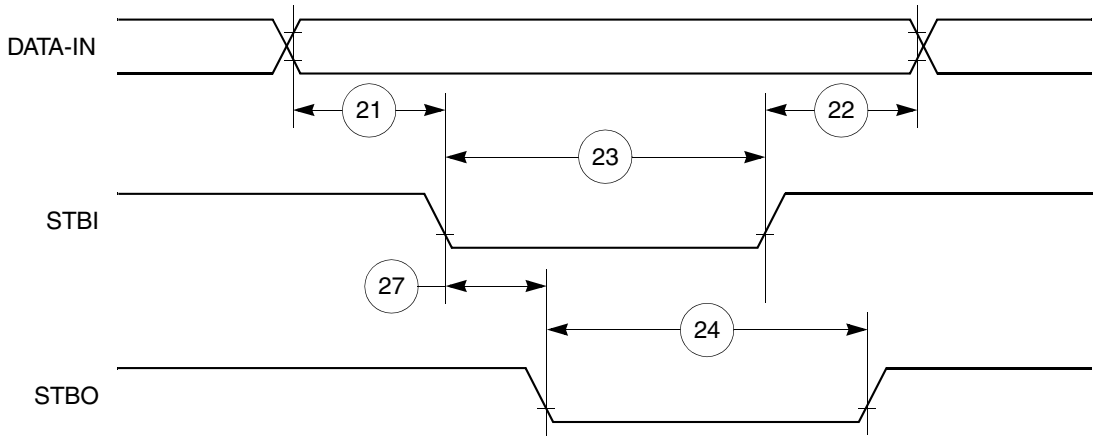



**Figure 39. PIP Rx (Interlock Mode) Timing Diagram**

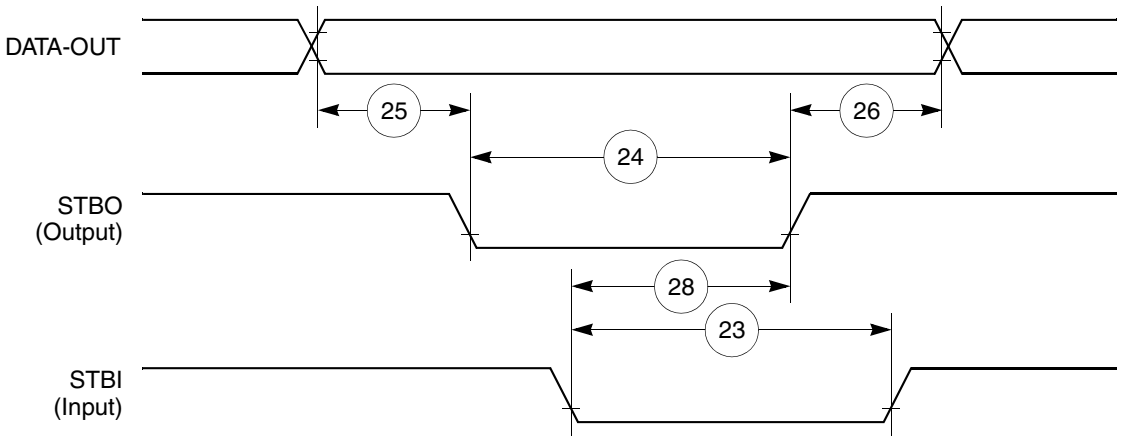



**Figure 40. PIP Tx (Interlock Mode) Timing Diagram**

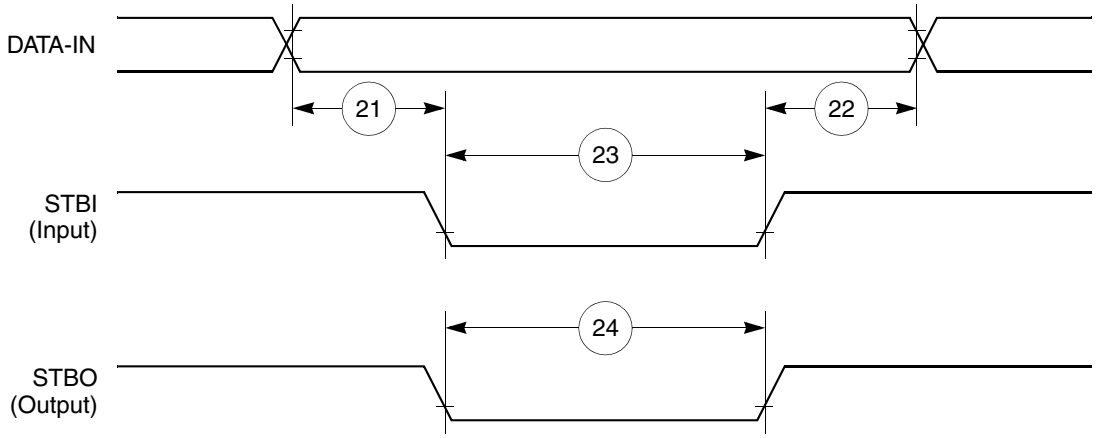



**Figure 41. PIP Rx (Pulse Mode) Timing Diagram**

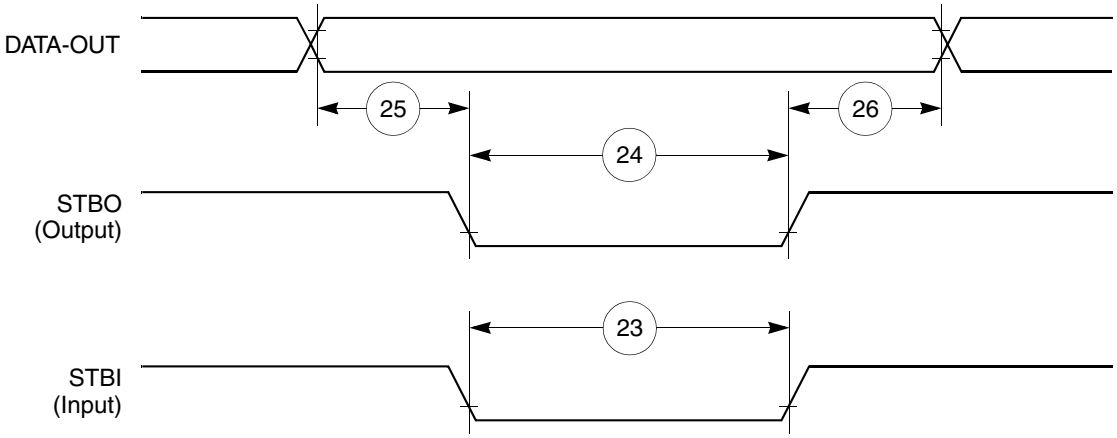



**Figure 42. PIP TX (Pulse Mode) Timing Diagram**

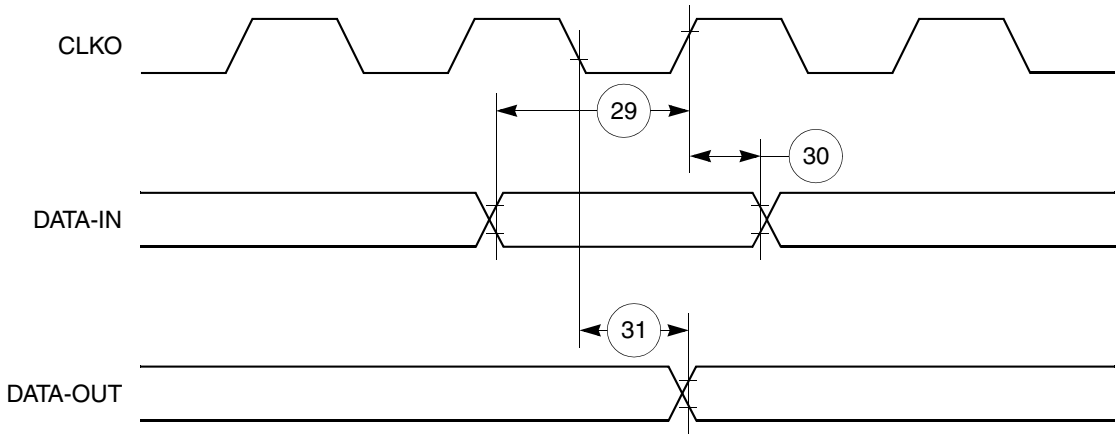



**Figure 43. Parallel I/O Data-In/Data-Out Timing Diagram**

## 11.2 Port C Interrupt AC Electrical Specifications

Table 15 provides the timings for port C interrupts.

**Table 15. Port C Interrupt Timing**

| Num | Characteristic | ≥ 33.34 MHz[1] | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 35 | Port C interrupt pulse width low (edge-triggered mode) | 55 | — | ns |
| 36 | Port C interrupt minimum time between active edges | 55 | — | ns |

1 External bus frequency of greater than or equal to 33.34 MHz.

Figure 44 shows the port C interrupt detection timing.

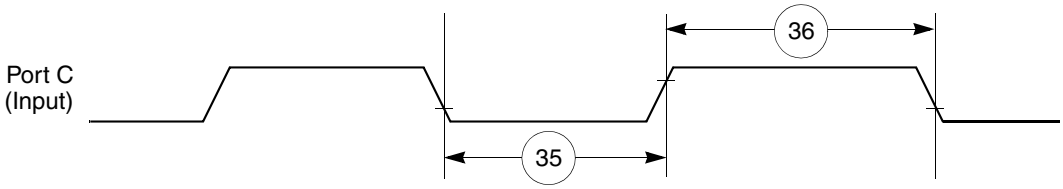



**Figure 44. Port C Interrupt Detection Timing**

## 11.3 IDMA Controller AC Electrical Specifications

Table 16 provides the IDMA controller timings as shown in Figure 45 through Figure 48.

**Table 16. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3 | — | ns |

**Table 16. IDMA Controller Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15 | ns |
| 46 | $\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7 | — | ns |

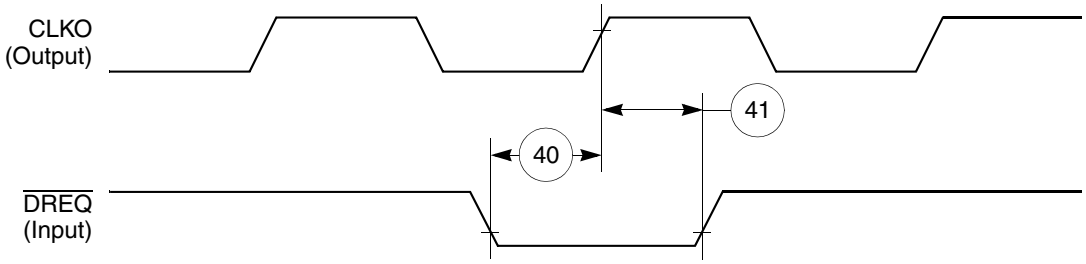



**Figure 45. IDMA External Requests Timing Diagram**

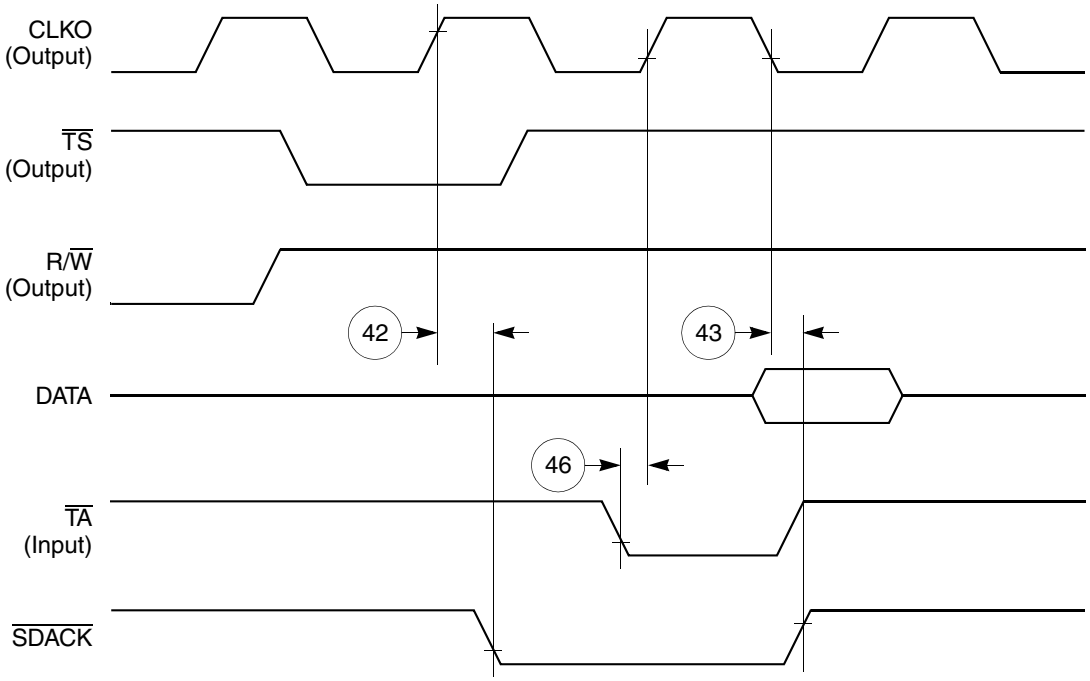



**Figure 46. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$**

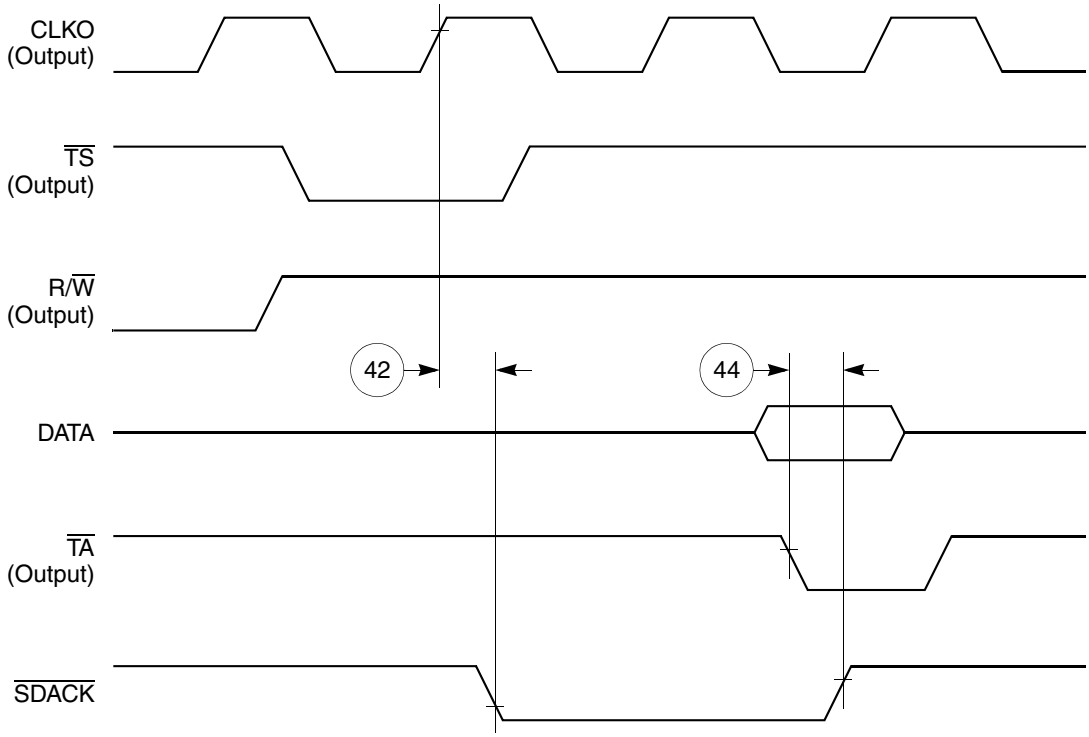



**Figure 47. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA**

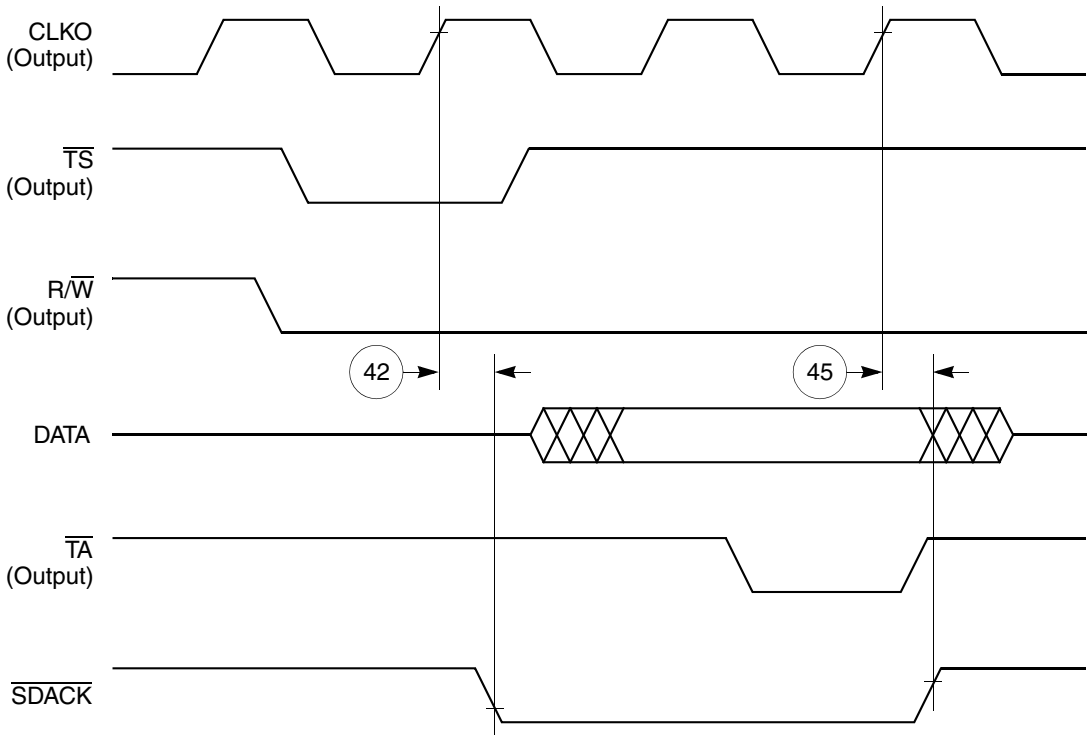



**Figure 48. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA**

## 11.4 Baud Rate Generator AC Electrical Specifications

Table 17 provides the baud rate generator timings as shown in Figure 49.

**Table 17. Baud Rate Generator Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10 | ns |
| 51 | BRGO duty cycle | 40 | 60 | % |
| 52 | BRGO cycle | 40 | — | ns |

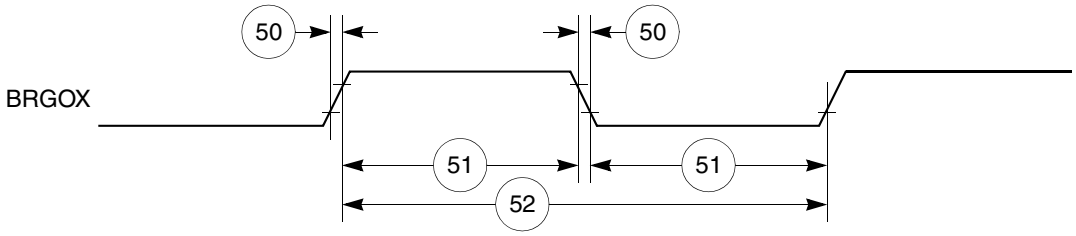



**Figure 49. Baud Rate Generator Timing Diagram**

## 11.5 Timer AC Electrical Specifications

Table 18 provides the general-purpose timer timings as shown in Figure 50.

**Table 18. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1 | — | CLK |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2 | — | CLK |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3 | — | CLK |
| 65 | CLKO low to $\overline{\text{TOUT}}$ valid | 3 | 25 | ns |

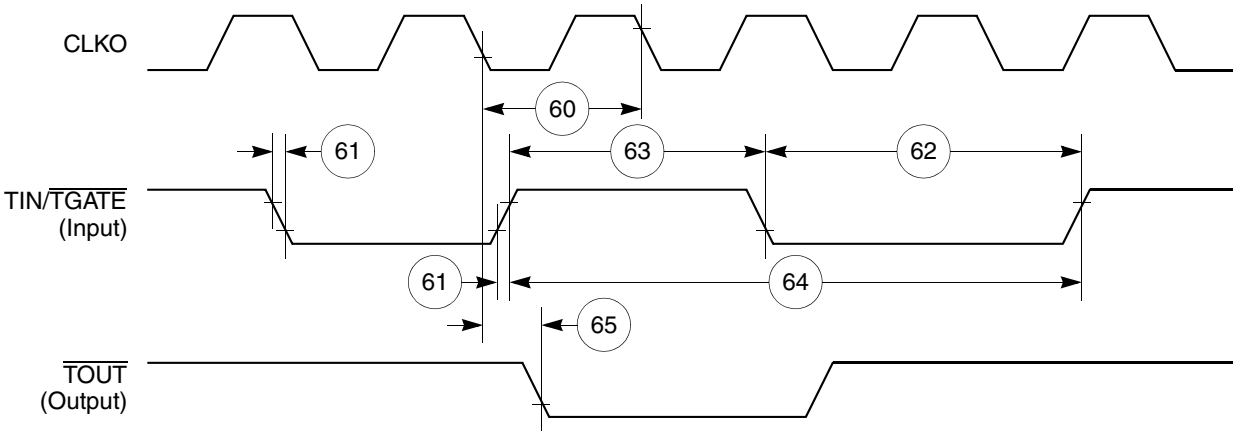



**Figure 50. CPM General-Purpose Timers Timing Diagram**

## 11.6 Serial Interface AC Electrical Specifications

Table 19 provides the serial interface timings as shown in Figure 51 through Figure 55.

**Table 19. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0)[1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0)[2] | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0)[3] | P + 10 | — | ns |
| 72 | L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |
| 76 | L1RXD valid to L1CLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1CLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1CLK edge to L1ST(1–4) valid [4] | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST(1–4) valid | 10.00 | 45.00 | ns |
| 79 | L1CLK edge to L1ST(1–4) invalid | 10.00 | 45.00 | ns |
| 80 | L1CLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid [4] | 10.00 | 55.00 | ns |
| 81 | L1CLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLK, L1TCLK frequency (DSC =1 ) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC = 1) | P + 10 | — | ns |
| 83a | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |

**Table 19. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4] | 1.00 | — | L1TCLK |
| 86 | L1GR setup time[2] | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

1 The ratio SYNCCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

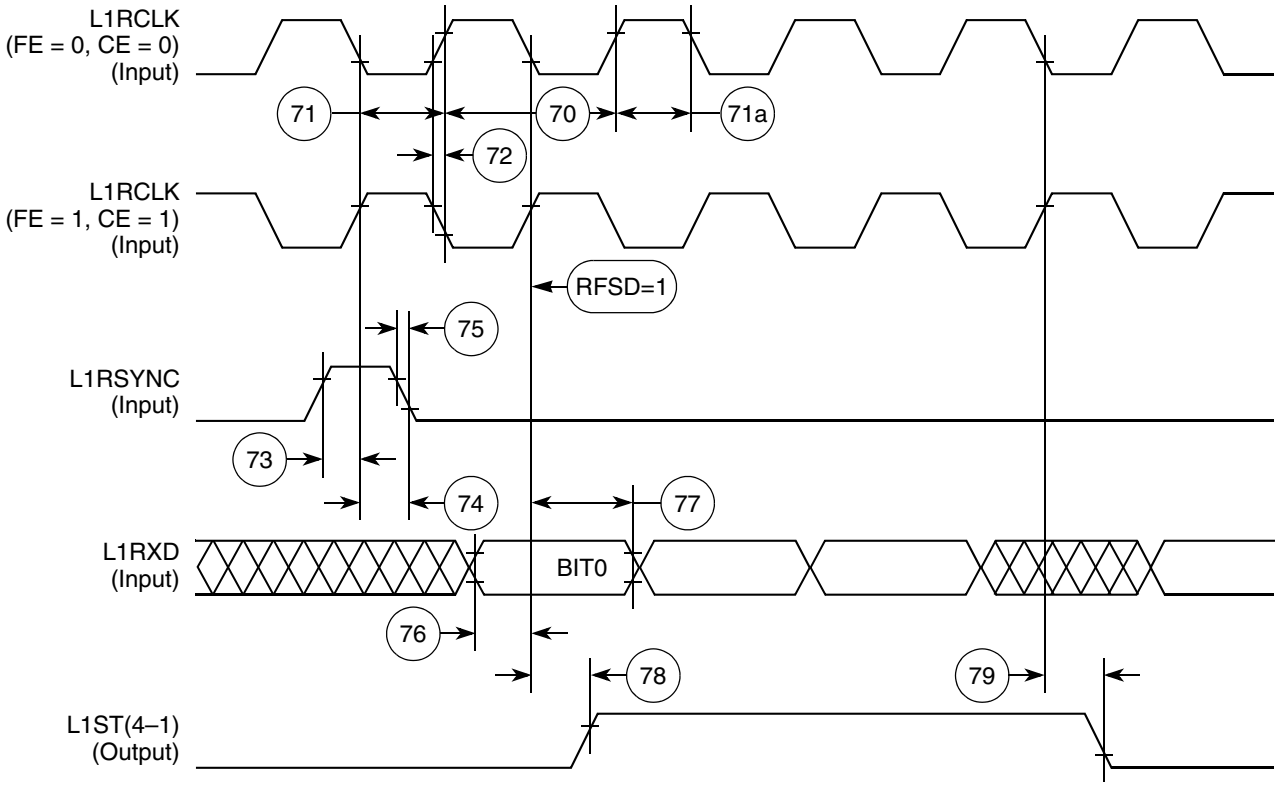



**Figure 51. SI Receive Timing Diagram with Normal Clocking (DSC = 0)**

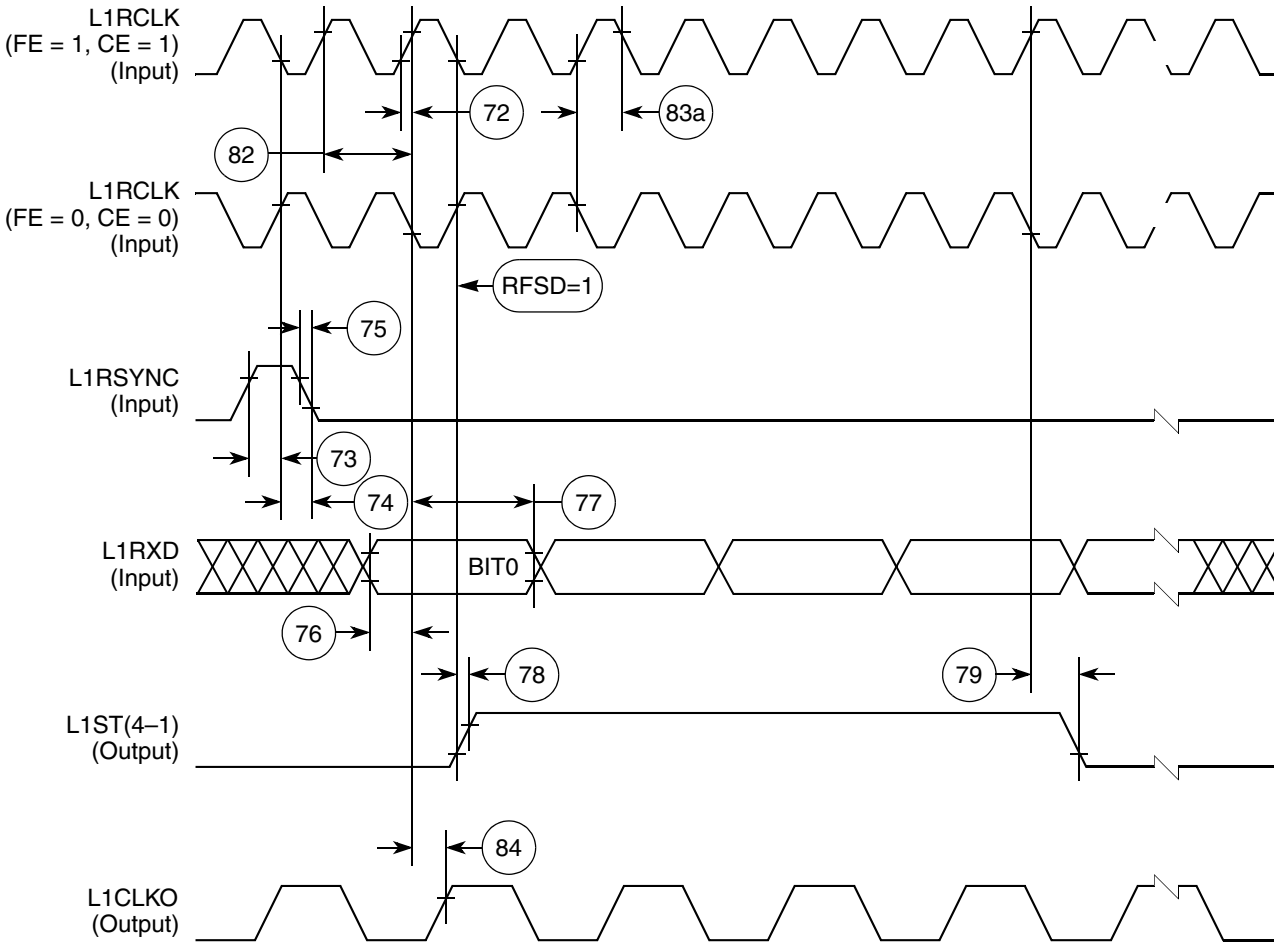



**Figure 52. SI Receive Timing with Double-Speed Clocking (DSC = 1)**

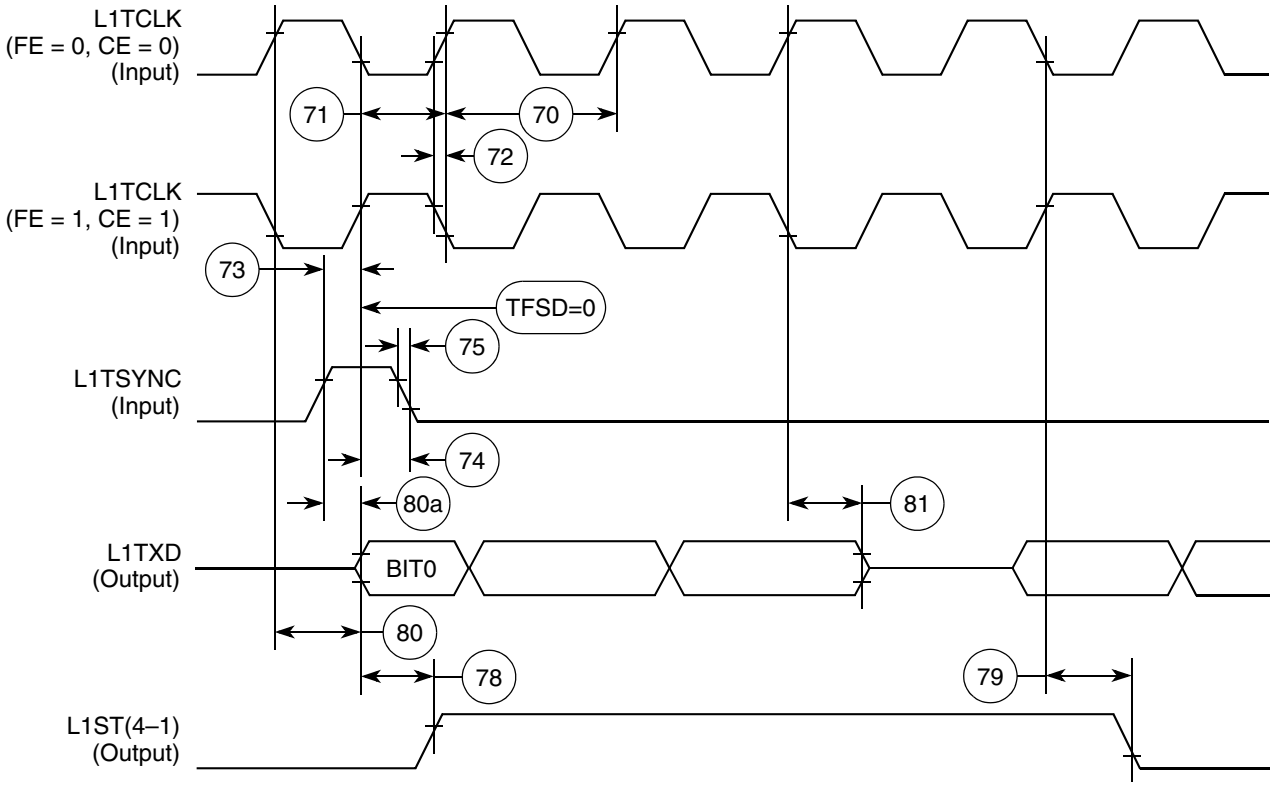



**Figure 53. SI Transmit Timing Diagram (DSC = 0)**

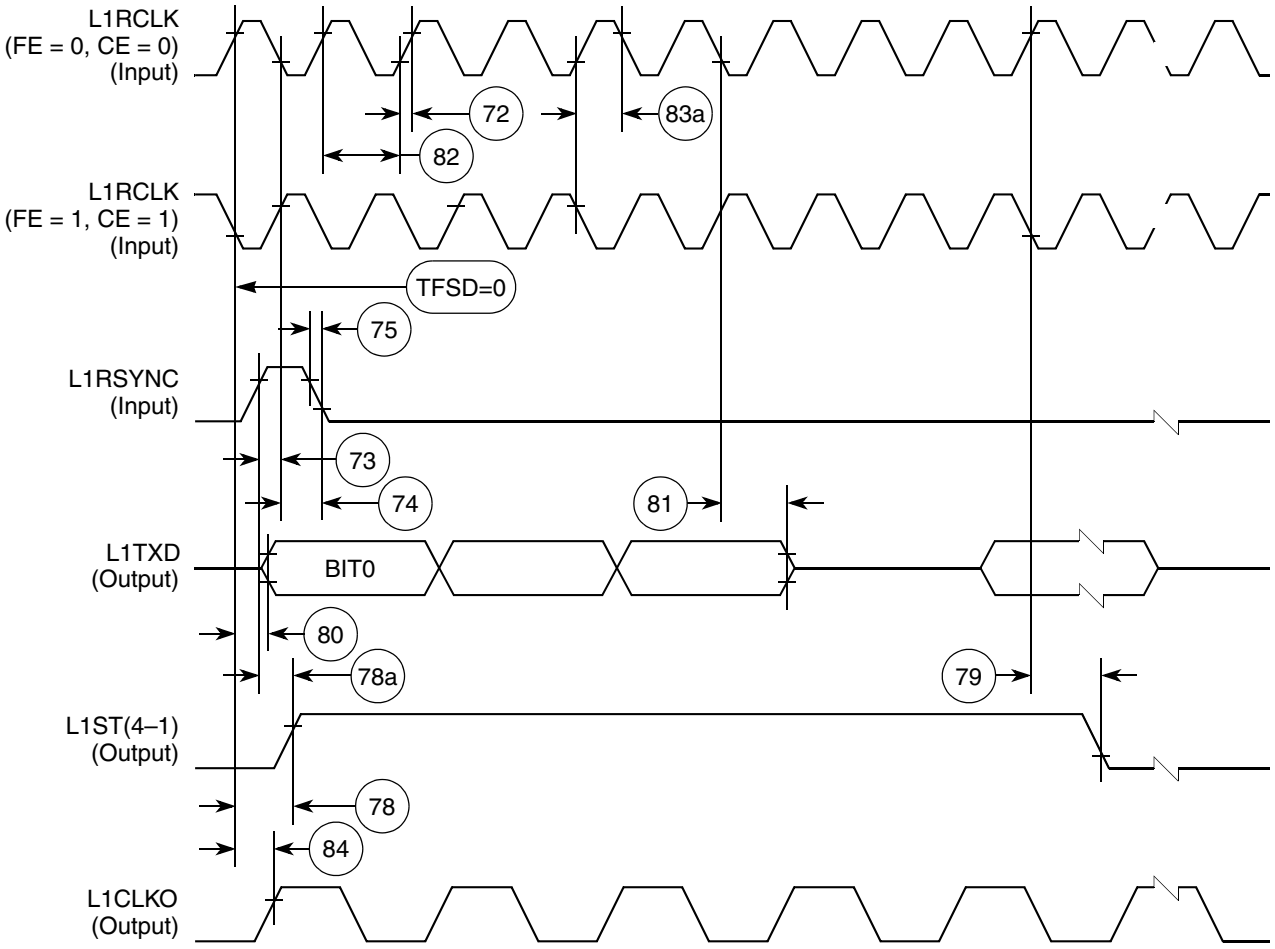



**Figure 54. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

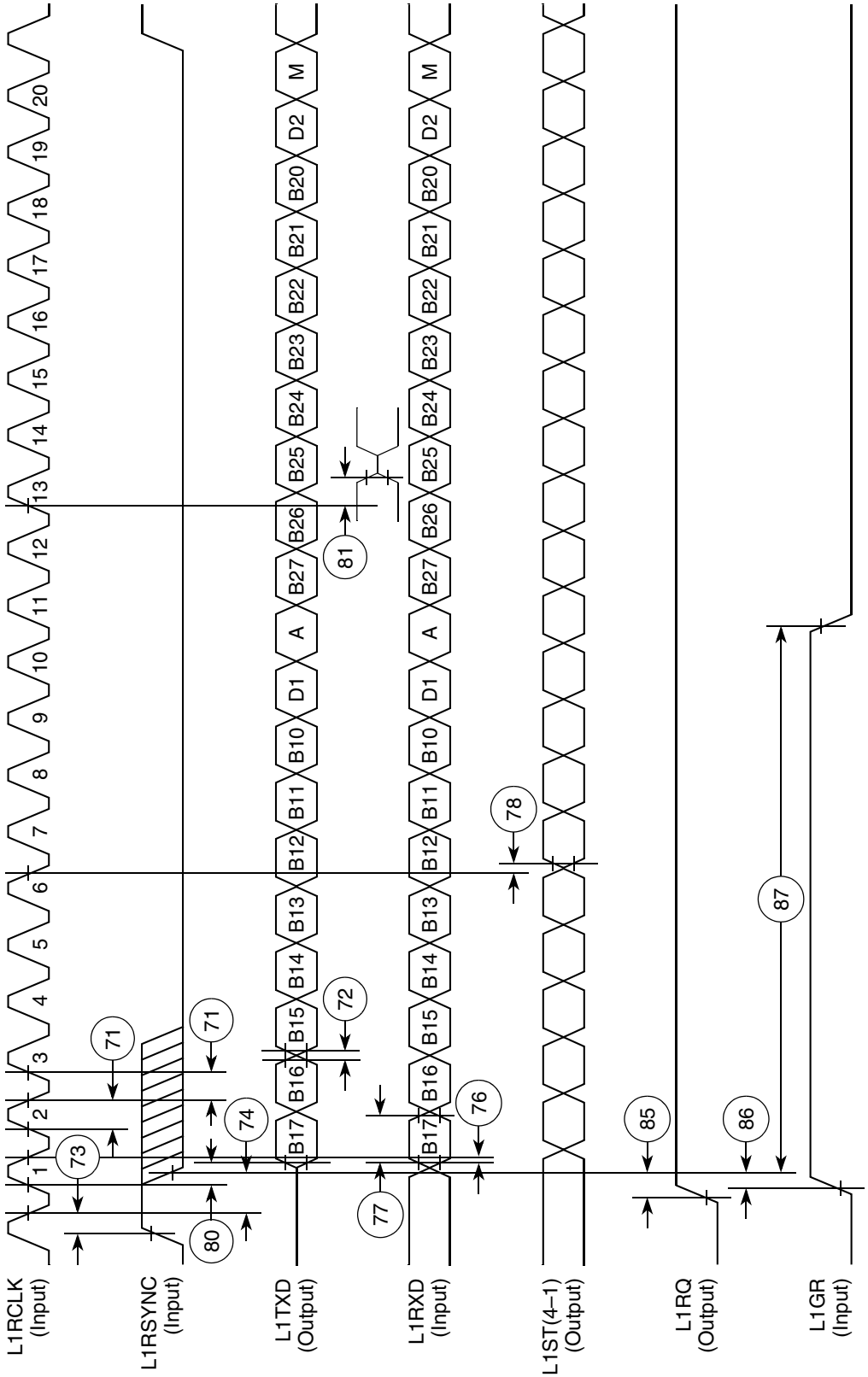



**Figure 55. IDL Timing**

## 11.7 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

**Table 20. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high[1] | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 5.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup Time to RCLK1 rising edge | 5.00 | — | ns |

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2.25/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 21 provides the NMSI internal clock timing.

**Table 21. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency[1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge[2] | 0.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 3/1.
2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Figure 56 through Figure 58 show the NMSI timings.

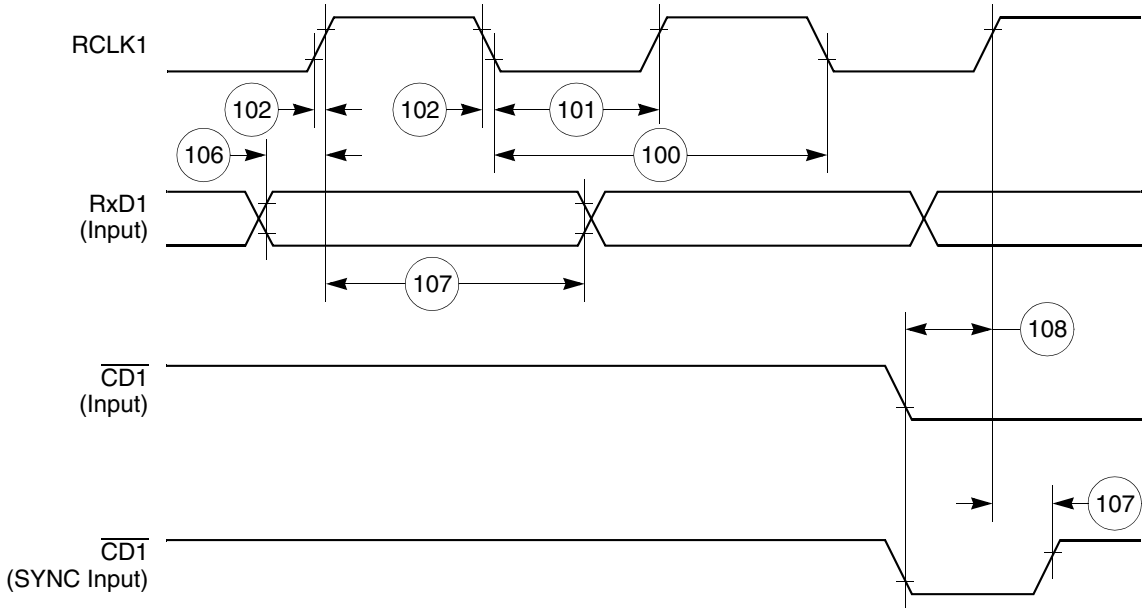



**Figure 56. SCC NMSI Receive Timing Diagram**

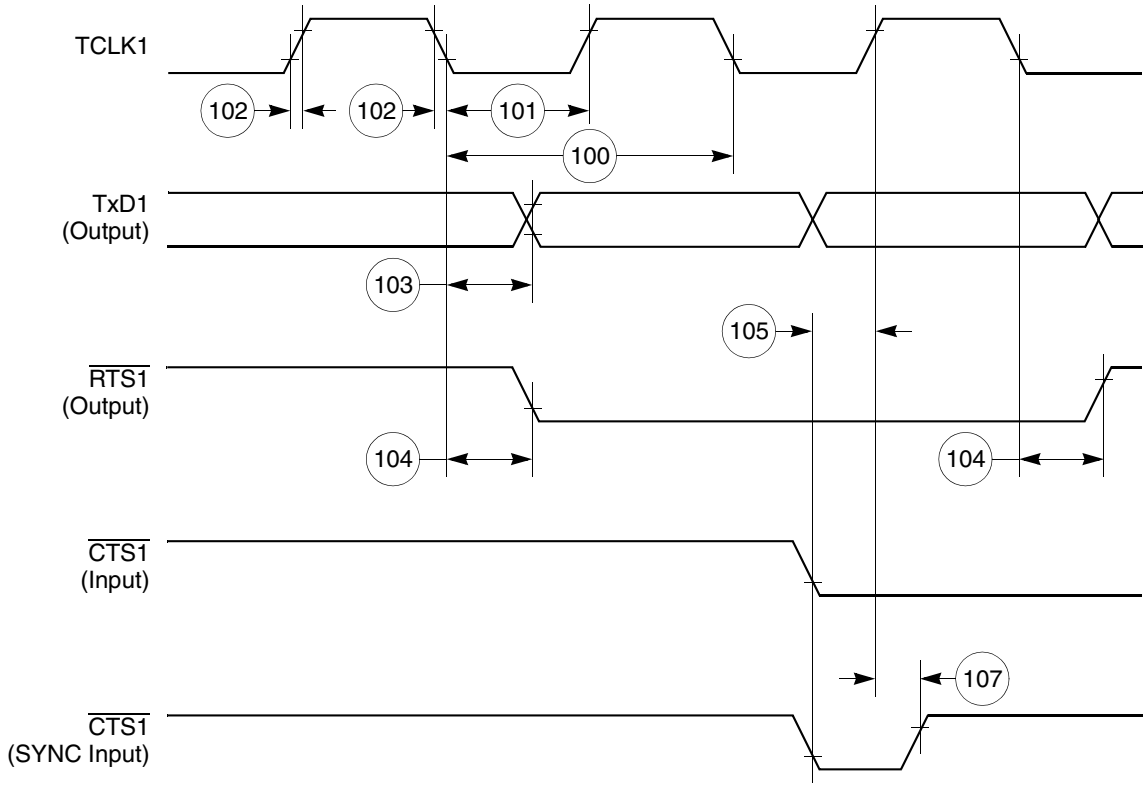



**Figure 57. SCC NMSI Transmit Timing Diagram**

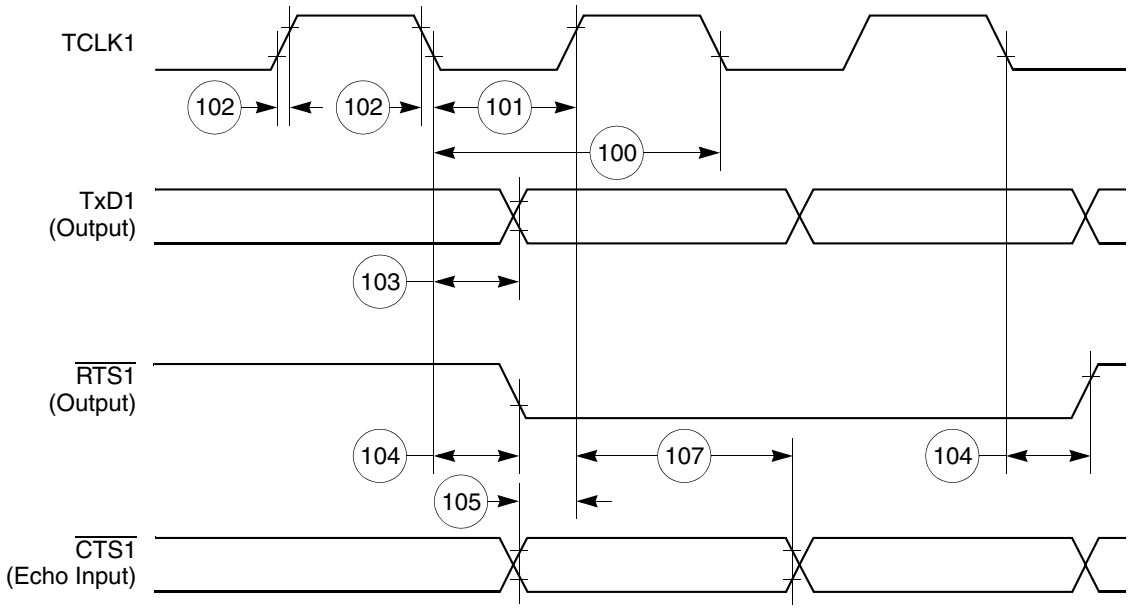



**Figure 58. HDLC Bus Timing Diagram**

## 11.8 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 59 through Figure 63.

**Table 22. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK1 rise/fall time | — | 15 | ns |
| 122 | RCLK1 width low | 40 | — | ns |
| 123 | RCLK1 clock period[1] | 80 | 120 | ns |
| 124 | RXD1 setup time | 20 | — | ns |
| 125 | RXD1 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK1 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK1 rise/fall time | — | 15 | ns |
| 129 | TCLK1 width low | 40 | — | ns |
| 130 | TCLK1 clock period[1] | 99 | 101 | ns |
| 131 | TXD1 active delay (from TCLK1 rising edge) | 10 | 50 | ns |
| 132 | TXD1 inactive delay (from TCLK1 rising edge) | 10 | 50 | ns |
| 133 | TENA active delay (from TCLK1 rising edge) | 10 | 50 | ns |
| 134 | TENA inactive delay (from TCLK1 rising edge) | 10 | 50 | ns |

**Table 22. Ethernet Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 135 | $\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge) | 10 | 50 | ns |
| 136 | $\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge) | 10 | 50 | ns |
| 137 | $\overline{\text{REJECT}}$ width low | 1 | — | CLK |
| 138 | CLKO1 low to $\overline{\text{SDACK}}$ asserted[2] | — | 20 | ns |
| 139 | CLKO1 low to $\overline{\text{SDACK}}$ negated[2] | — | 20 | ns |

1 The ratios SYNCCLK/RCLK1 and SYNCCLK/TCLK1 must be greater than or equal to 2/1.
2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

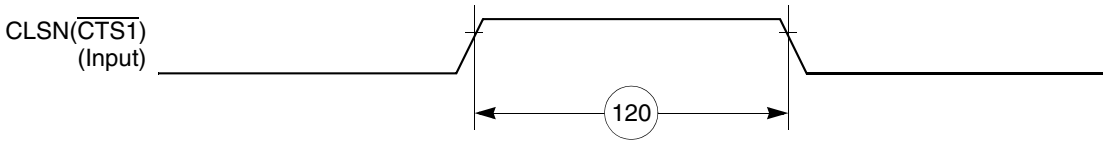



**Figure 59. Ethernet Collision Timing Diagram**

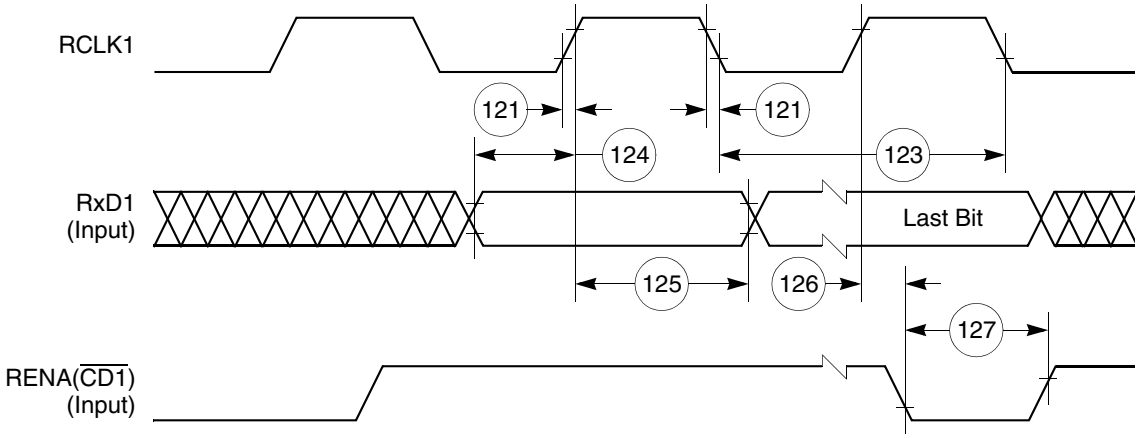
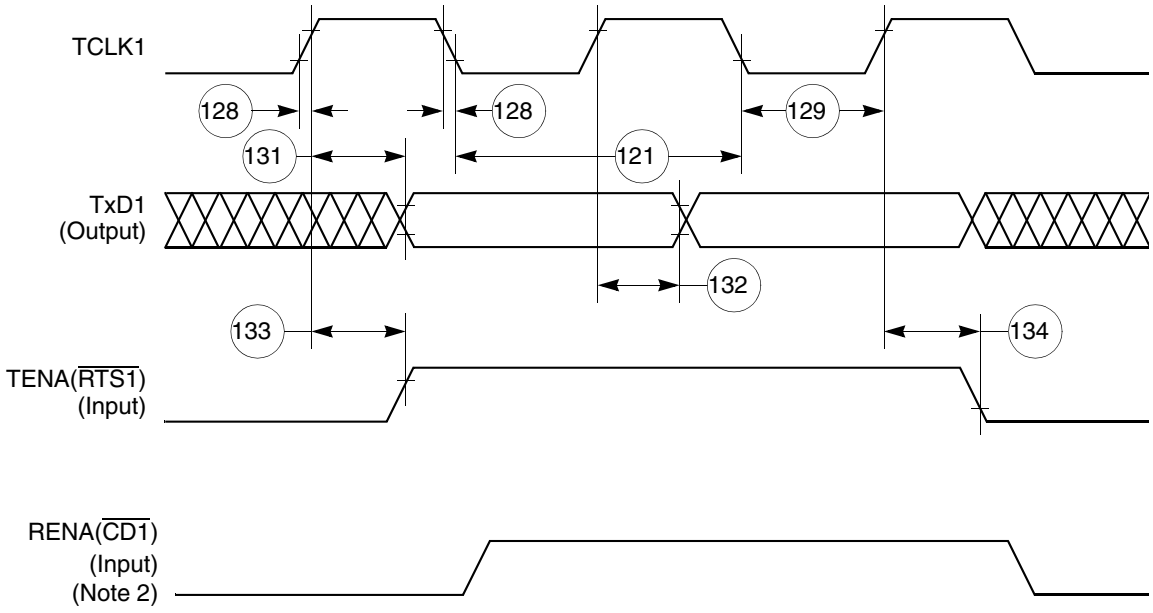



**Figure 60. Ethernet Receive Timing Diagram**




**Notes:**
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 61. Ethernet Transmit Timing Diagram**

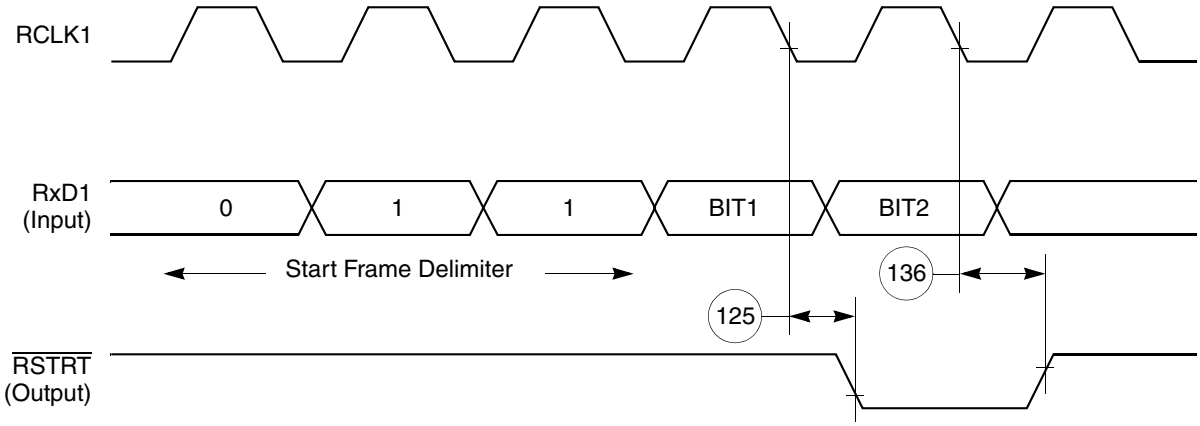



**Figure 62. CAM Interface Receive Start Timing Diagram**

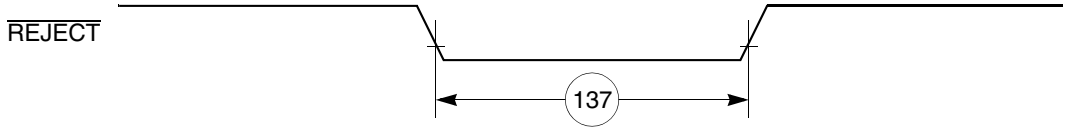



**Figure 63. CAM Interface REJECT Timing Diagram**

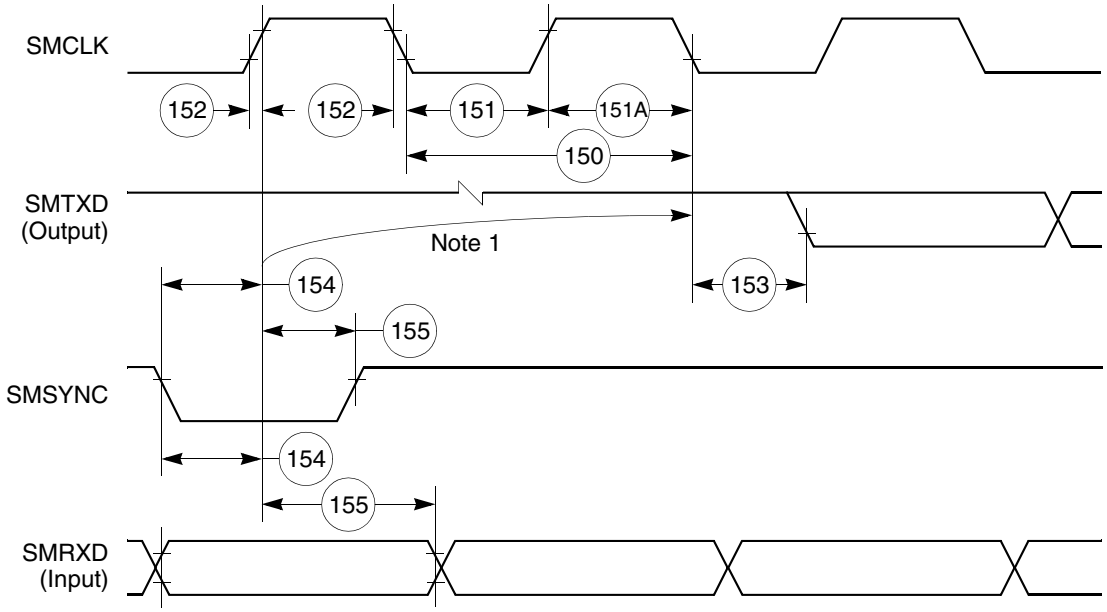
## 11.9 SMC Transparent AC Electrical Specifications

Table 23 provides the SMC transparent timings as shown in Figure 64.

**Table 23. SMC Transparent Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLK clock period[1] | 100 | — | ns |
| 151 | SMCLK width low | 50 | — | ns |
| 151A | SMCLK width high | 50 | — | ns |
| 152 | SMCLK rise/fall time | — | 15 | ns |
| 153 | SMTXD active delay (from SMCLK falling edge) | 10 | 50 | ns |
| 154 | SMRXD/SMSYNC setup time | 20 | — | ns |
| 155 | RXD1/SMSYNC hold time | 5 | — | ns |

1 SYNCCLK must be at least twice as fast as SMCLK.




**Note:**
1. This delay is equal to an integer number of character-length clocks.

**Figure 64. SMC Transparent Timing Diagram**

## 11.10 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 65 and Figure 66.

**Table 24. SPI Master Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 160 | MASTER cycle time | 4 | 1024 | $t_{cyc}$ |
| 161 | MASTER clock (SCK) high or low time | 2 | 512 | $t_{cyc}$ |
| 162 | MASTER data setup time (inputs) | 50 | — | ns |
| 163 | Master data hold time (inputs) | 0 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 20 | ns |
| 165 | Master data hold time (outputs) | 0 | — | ns |
| 166 | Rise time output | — | 15 | ns |
| 167 | Fall time output | — | 15 | ns |

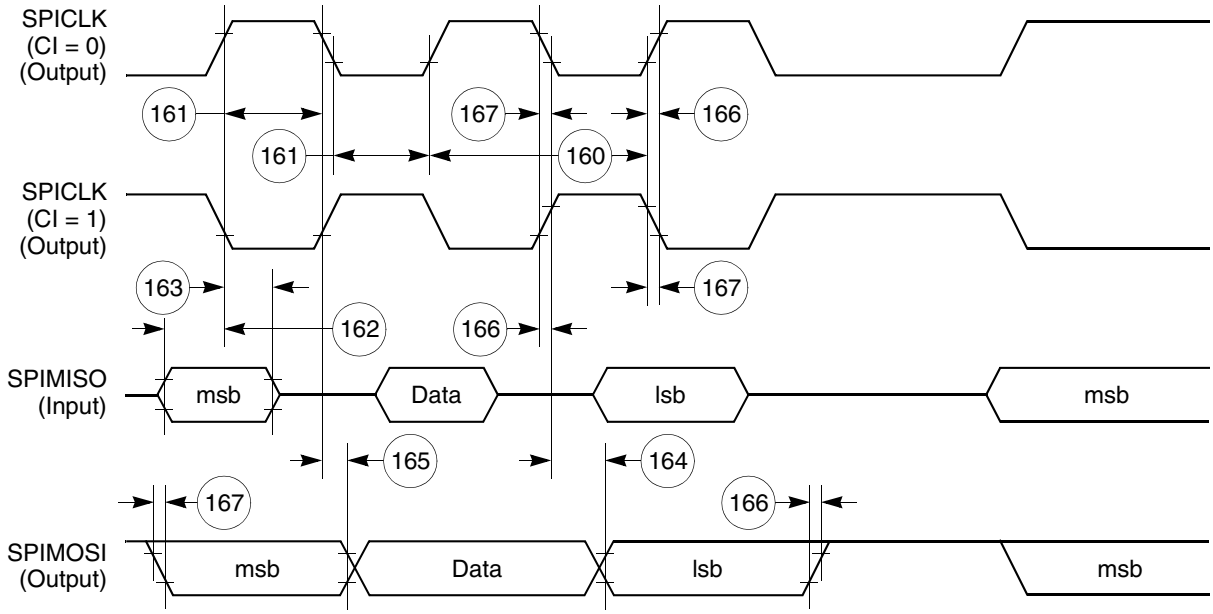



**Figure 65. SPI Master (CP = 0) Timing Diagram**

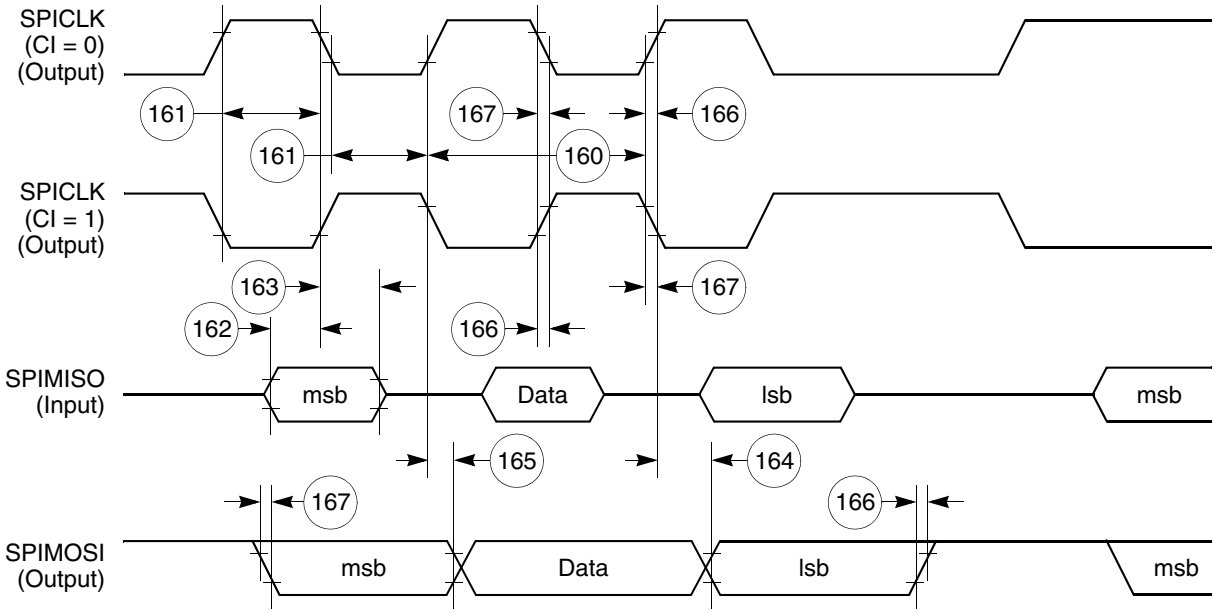



**Figure 66. SPI Master (CP = 1) Timing Diagram**

## 11.11 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 67 and Figure 68.

**Table 25. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15 | — | ns |
| 172 | Slave enable lag time | 15 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20 | — | ns |
| 176 | Slave data hold time (inputs) | 20 | — | ns |
| 177 | Slave access time | — | 50 | ns |

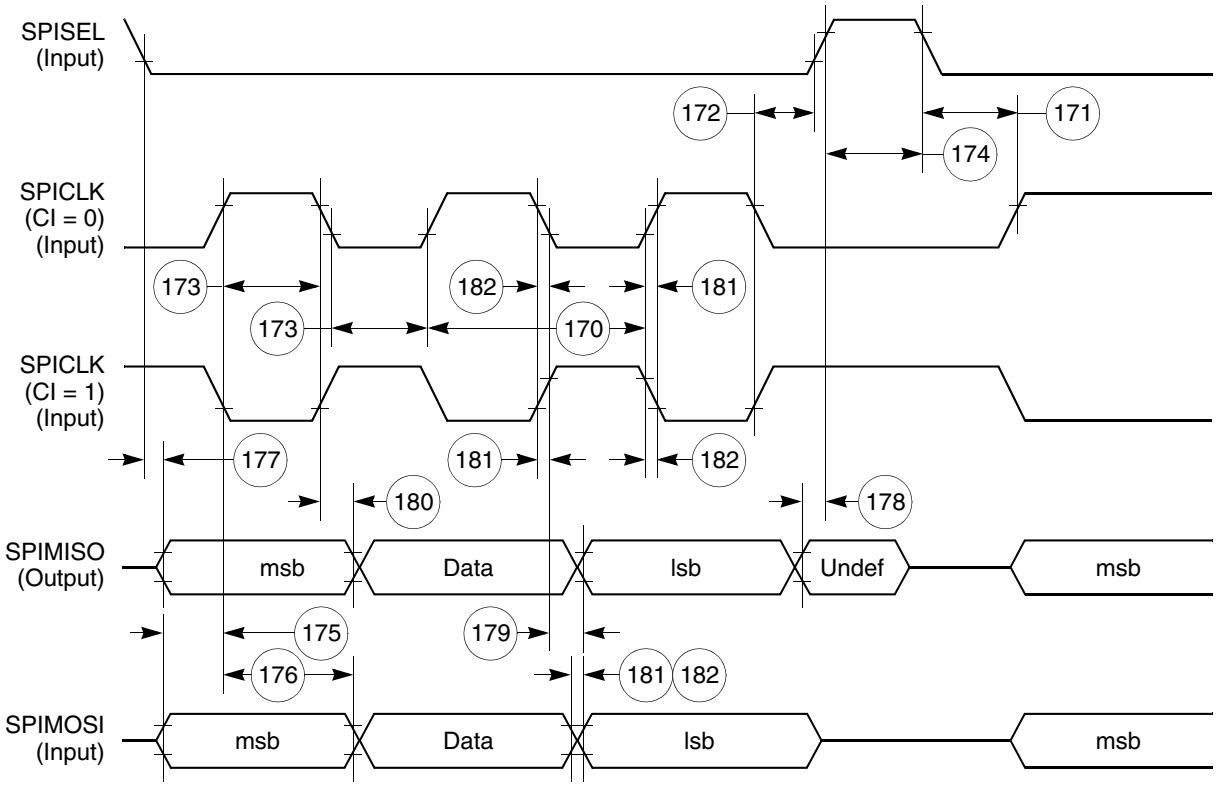



**Figure 67. SPI Slave (CP = 0) Timing Diagram**

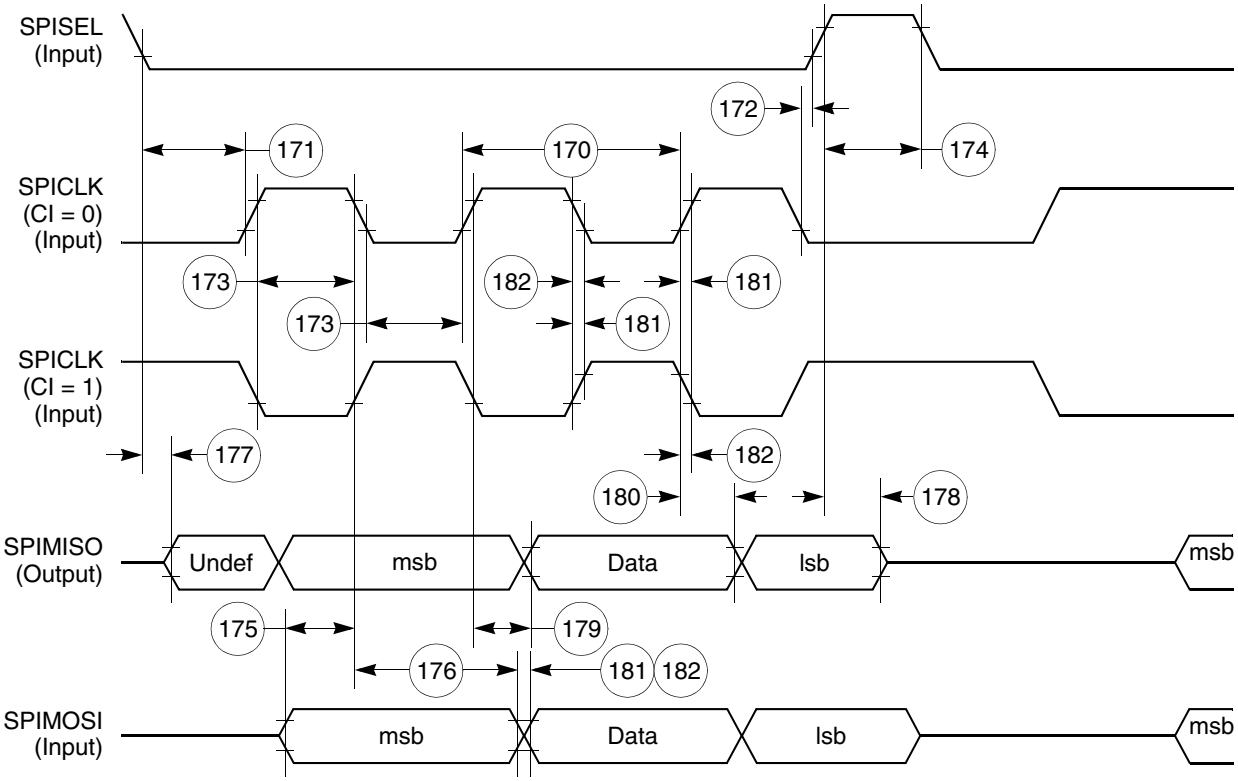



**Figure 68. SPI Slave (CP = 1) Timing Diagram**

## 11.12 I²C AC Electrical Specifications

Table 26 provides the I²C (SCL < 100 kHz) timings.

**Table 26. I²C Timing (SCL < 100 kHz)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master)[1] | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | µs |
| 203 | Low period of SCL | 4.7 | — | µs |
| 204 | High period of SCL | 4.0 | — | µs |
| 205 | Start condition setup time | 4.7 | — | µs |
| 206 | Start condition hold time | 4.0 | — | µs |
| 207 | Data hold time | 0 | — | µs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | µs |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | µs |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3 × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK/pre_scaler) must be greater than or equal to 4/1.

Table 27 provides the I²C (SCL > 100 kHz) timings.

**Table 27. . I²C Timing (SCL > 100 kHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master)[1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) × pre_scaler × 2).
The ratio SYNCCLK/(BRGCLK / pre_scaler) must be greater than or equal to 4/1.

Figure 69 shows the $I^2C$ bus timing.

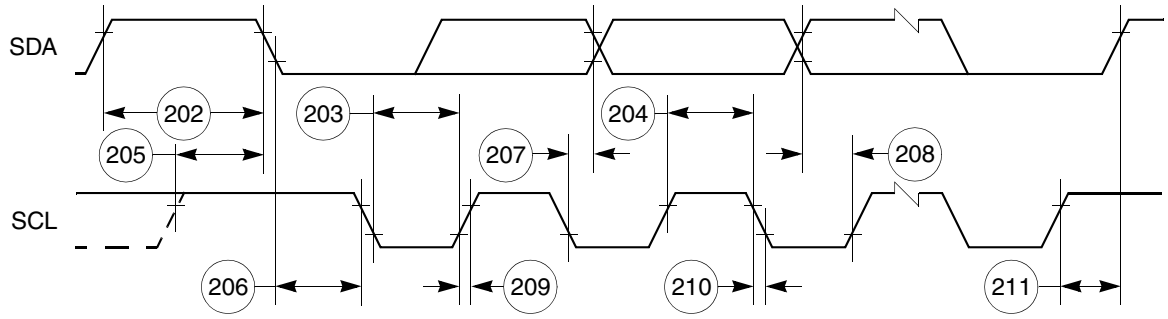



**Figure 69. $I^2C$ Bus Timing Diagram**

# 12 UTOPIA AC Electrical Specifications

Table 28 shows the AC electrical specifications for the UTOPIA interface.

**Table 28. UTOPIA AC Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (Internal clock option) | Output | — | 3.5 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | — | 50 | MHz |
| U1a | UtpClk rise/fall time (external clock option) | Input | — | 3.5 | ns |
| | Duty cycle | | 40 | 60 | % |
| | Frequency | | — | 50 | MHz |
| U2 | $\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay | Output | 2 | 16 | ns |
| U3 | UTPB, SOC, Rxclav and Txclav setup time | Input | 8 | — | ns |
| U4 | UTPB, SOC, Rxclav and Txclav hold time | Input | 1 | — | ns |
| U5 | UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode) | Output | 2 | 16 | ns |

Figure 70 shows signal timings during UTOPIA receive operations.

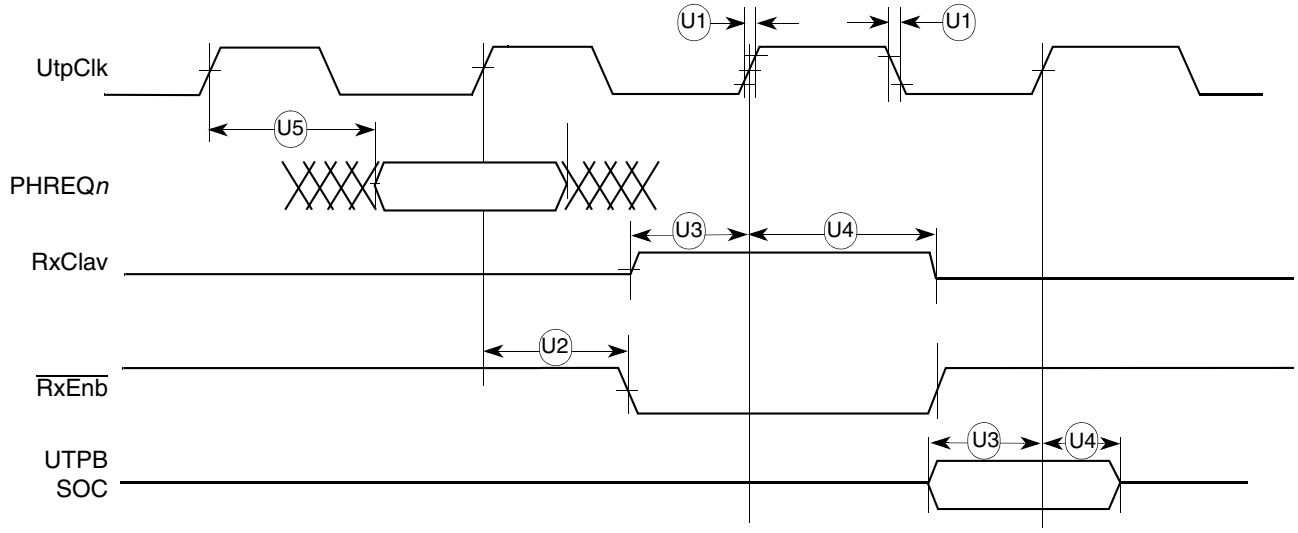



**Figure 70. UTOPIA Receive Timing**

Figure 71 shows signal timings during UTOPIA transmit operations.

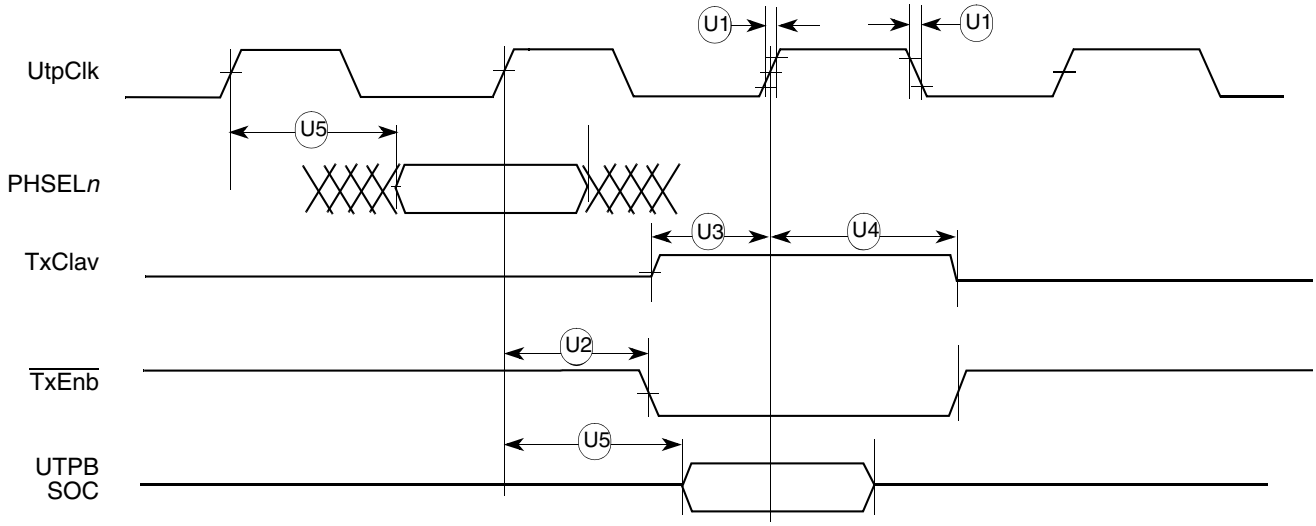



**Figure 71. UTOPIA Transmit Timing**

# 13 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

## 13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 29 provides information on the MII receive signal timing.

**Table 29. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup | 5 | — | ns |
| M2 | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold | 5 | — | ns |
| M3 | MII_RX_CLK pulse width high | 35% | 65% | MII_RX_CLK period |
| M4 | MII_RX_CLK pulse width low | 35% | 65% | MII_RX_CLK period |

Figure 72 shows MII receive signal timing.

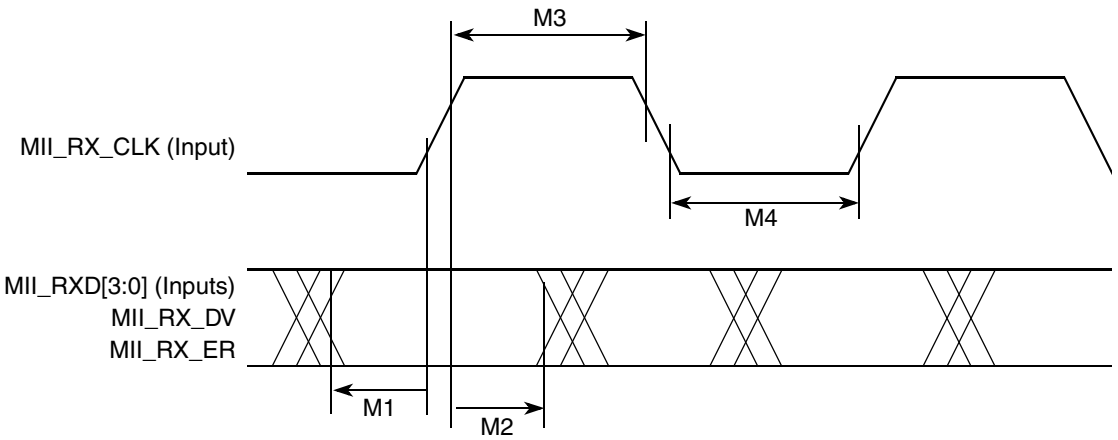



**Figure 72. MII Receive Signal Timing Diagram**

## 13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 30 provides information on the MII transmit signal timing.

**Table 30. MII Transmit Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid | 5 | — | ns |
| M6 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid | — | 25 | |
| M7 | MII_TX_CLK pulse width high | 35 | 65% | MII_TX_CLK period |
| M8 | MII_TX_CLK pulse width low | 35% | 65% | MII_TX_CLK period |

Figure 73 shows the MII transmit signal timing diagram.

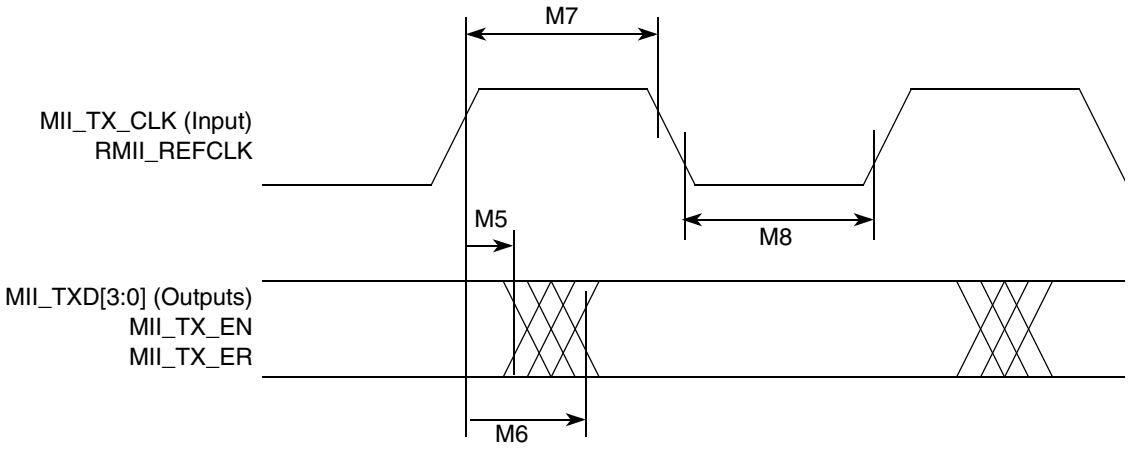



**Figure 73. MII Transmit Signal Timing Diagram**

## 13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 31 provides information on the MII async inputs signal timing.

**Table 31. MII Async Inputs Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | MII_CRS, MII_COL minimum pulse width | 1.5 | — | MII_TX_CLK period |

Figure 74 shows the MII asynchronous inputs signal timing diagram.

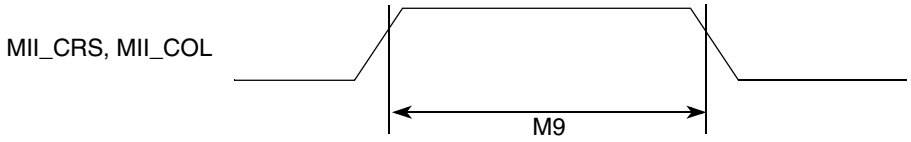



**Figure 74. MII Async Inputs Timing Diagram**

## 13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 32 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

**Table 32. MII Serial Management Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M10 | MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | MII_MDC falling edge to MII_MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | MII_MDIO (input) to MII_MDC rising edge setup | 10 | — | ns |
| M13 | MII_MDIO (input) to MII_MDC rising edge hold | 0 | — | ns |
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low | 40% | 60% | MII_MDC period |

Figure 75 shows the MII serial management channel timing diagram.

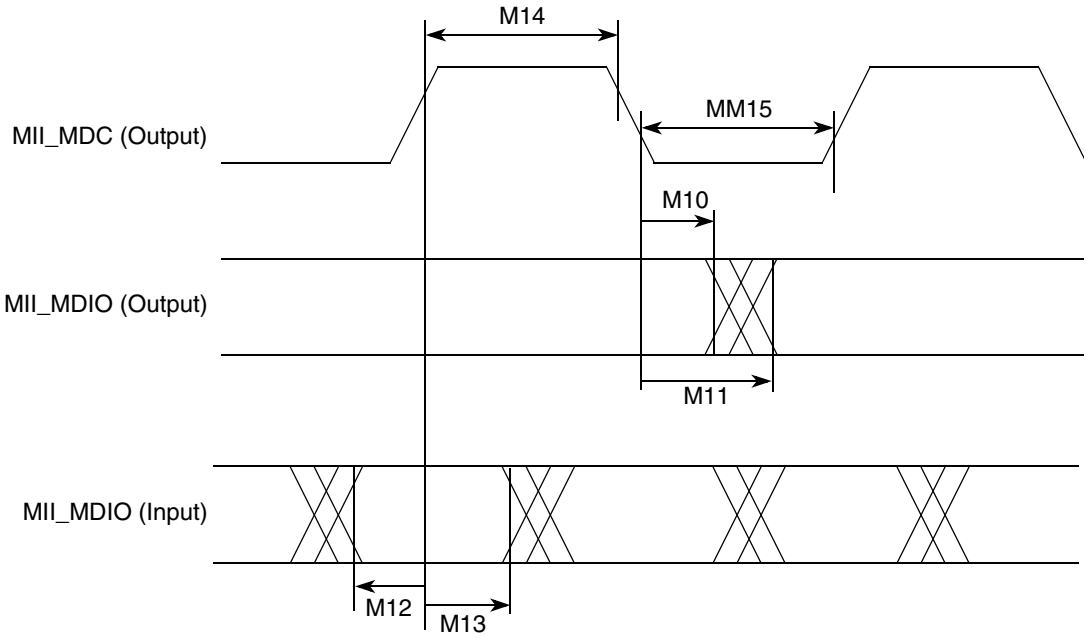



**Figure 75. MII Serial Management Channel Timing Diagram**

# 14 Mechanical Data and Ordering Information

## 14.1 Ordering Information

Table 33 provides information on the MPC860 Revision D.4 derivative devices.

**Table 33. MPC860 Family Revision D.4 Derivatives**

| Device | Number of SCCs[1] | Ethernet Support[2] (Mbps) | Multichannel HDLC Support | ATM Support |
|---|---|---|---|---|
| MPC855T | 1 | 10/100 | Yes | Yes |
| MPC860DE | 2 | 10 | N/A | N/A |
| MPC860DT | | 10/100 | Yes | Yes |
| MPC860DP | | 10/100 | Yes | Yes |
| MPC860EN | 4 | 10 | N/A | N/A |
| MPC860SR | | 10 | Yes | Yes |
| MPC860T | | 10/100 | Yes | Yes |
| MPC860P | | 10/100 | Yes | Yes |

1 Serial communications controller (SCC)
2 Up to 4 channels at 40 MHz or 2 channels at 25 MHz

Table 34 identifies the packages and operating frequencies available for the MPC860.

**Table 34. MPC860 Family Package/Frequency Availability**

| Package Type | Freq. (MHz) / Temp. (Tj) | Package | Order Number |
|---|---|---|---|
| Ball grid array<br>ZP suffix—leaded<br>ZQ suffix—leaded<br>VR suffix—lead-free | 50<br>0° to 95°C | ZP/ZQ[1] | MPC855TZQ50D4<br>MPC860DEZQ50D4<br>MPC860DTZQ50D4<br>MPC860ENZQ50D4<br>MPC860SRZQ50D4<br>MPC860TZQ50D4<br>MPC860DPZQ50D4<br>MPC860PZQ50D4 |
| | | Tape and Reel | MPC855TZQ50D4R2<br>MPC860DEZQ50D4R2<br>MPC860ENZQ50D4R2<br>MPC860SRZQ50D4R2<br>MPC860TZQ50D4R2<br>MPC860DPZQ50D4R2<br>MPC855TVR50D4R2<br>MPC860ENVR50D4R2<br>MPC860SRVR50D4R2<br>MPC860TVR50D4R2 |
| | | VR | MPC855TVR50D4<br>MPC860DEVR50D4<br>MPC860DPVR50D4<br>MPC860DTVR50D4<br>MPC860ENVR50D4<br>MPC860PVR50D4<br>MPC860SRVR50D4<br>MPC860TVR50D4 |
| | 66<br>0° to 95°C | ZP/ZQ[1] | MPC855TZQ66D4<br>MPC860DEZQ66D4<br>MPC860DTZQ66D4<br>MPC860ENZQ66D4<br>MPC860SRZQ66D4<br>MPC860TZQ66D4<br>MPC860DPZQ66D4<br>MPC860PZQ66D4 |
| | | Tape and Reel | MPC860SRZQ66D4R2<br>MPC860PZQ66D4R2 |
| | | VR | MPC855TVR66D4<br>MPC860DEVR66D4<br>MPC860DPVR66D4<br>MPC860DTVR66D4<br>MPC860ENVR66D4<br>MPC860PVR66D4<br>MPC860SRVR66D4<br>MPC860TVR66D4 |

**Table 34. MPC860 Family Package/Frequency Availability (continued)**

| Package Type | Freq. (MHz) / Temp. (Tj) | Package | Order Number |
|---|---|---|---|
| Ball grid array *(continued)*<br>ZP suffix—leaded<br>ZQ suffix—leaded<br>VR suffix—lead-free | 80<br>0° to 95°C | ZP/ZQ[1] | MPC855TZQ80D4<br>MPC860DEZQ80D4<br>MPC860DTZQ80D4<br>MPC860ENZQ80D4<br>MPC860SRZQ80D4<br>MPC860TZQ80D4<br>MPC860DPZQ80D4<br>MPC860PZQ80D4 |
| | | Tape and Reel | MPC860PZQ80D4R2<br>MPC860PVR80D4R2 |
| | | VR | MPC855TVR80D4<br>MPC860DEVR80D4<br>MPC860DPVR80D4<br>MPC860ENVR80D4<br>MPC860PVR80D4<br>MPC860SRVR80D4<br>MPC860TVR80D4 |
| Ball grid array (CZP suffix)<br>CZP suffix—leaded<br>CZQ suffix—leaded<br>CVR suffix—lead-free | 50<br>–40° to 95°C | ZP/ZQ[1] | MPC855TCZQ50D4<br>MPC855TCVR50D4<br>MPC860DECZQ50D4<br>MPC860DTCZQ50D4<br>MPC860ENCZQ50D4<br>MPC860SRCZQ50D4<br>MPC860TCZQ50D4<br>MPC860DPCZQ50D4<br>MPC860PCZQ50D4 |
| | | Tape and Reel | MPC855TCZQ50D4R2<br>MC860ENCVR50D4R2 |
| | | CVR | MPC860DECVR50D4<br>MPC860DTCVR50D4<br>MPC860ENCVR50D4<br>MPC860PCVR50D4<br>MPC860SRCVR50D4<br>MPC860TCVR50D4 |
| | 66<br>–40° to 95°C | ZP/ZQ[1] | MPC855TCZQ66D4<br>MPC855TCVR66D4<br>MPC860ENCZQ66D4<br>MPC860SRCZQ66D4<br>MPC860TCZQ66D4<br>MPC860DPCZQ66D4<br>MPC860PCZQ66D4 |
| | | CVR | MPC860DTCVR66D4<br>MPC860ENCVR66D4<br>MPC860PCVR66D4<br>MPC860SRCVR66D4<br>MPC860TCVR66D4 |

[1] The ZP package is no longer recommended for use. The ZQ package replaces the ZP package.

## 14.2 Pin Assignments

Figure 76 shows the top view pinout of the PBGA package. For additional information, see the *MPC860 PowerQUICC User's Manual*, or the *MPC855T User's Manual*.

**NOTE:** This is the top view of the device.

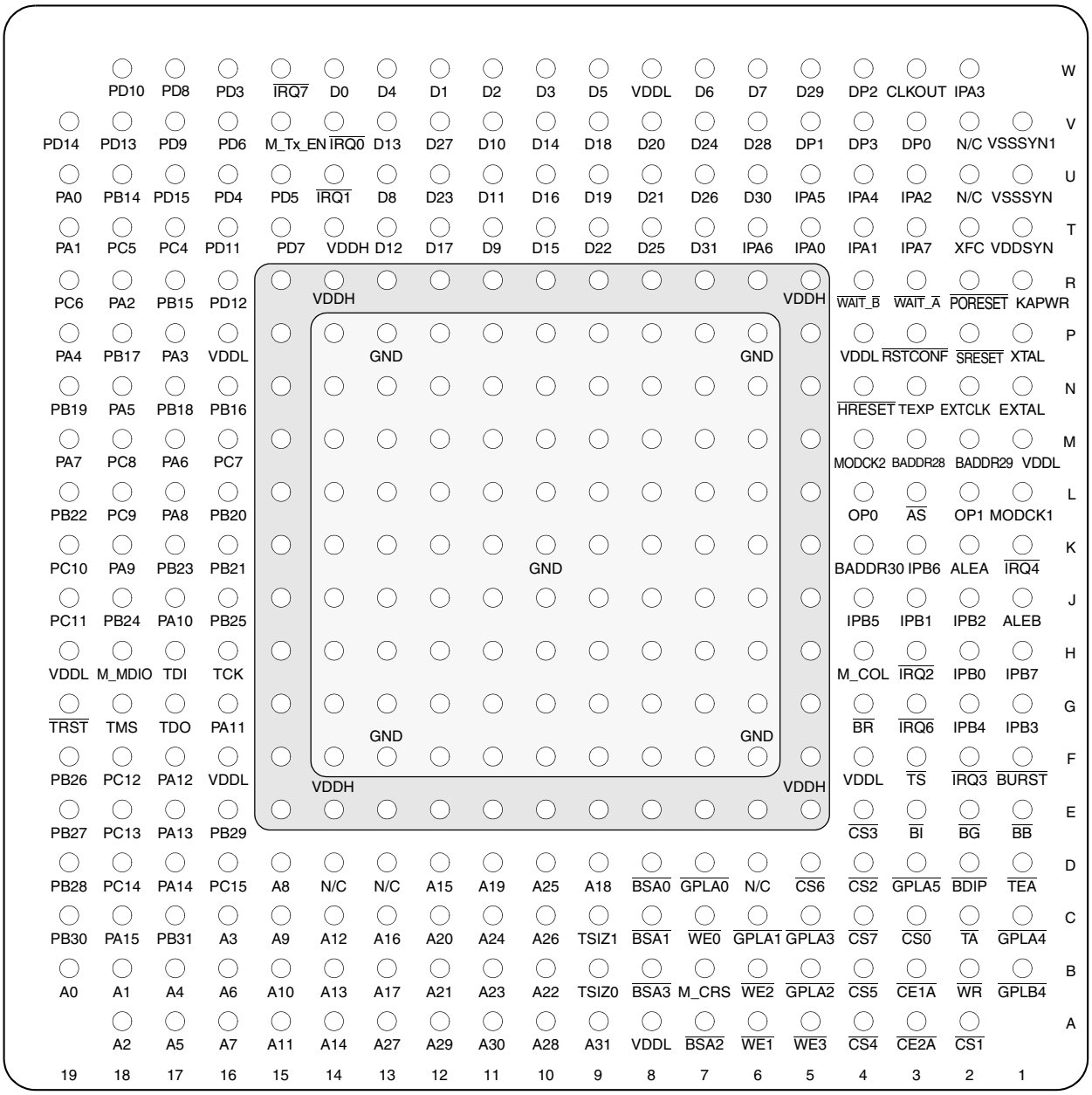
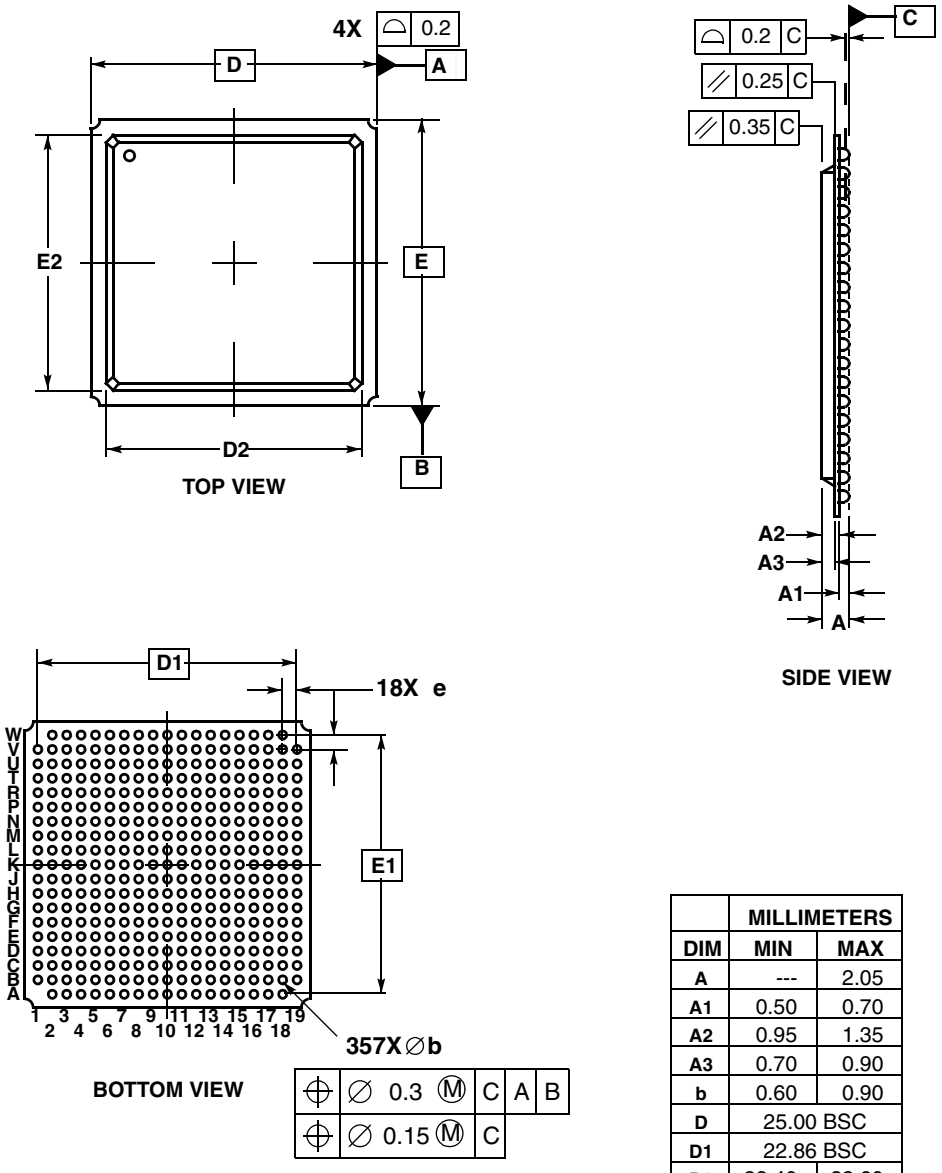



**Figure 76. Pinout of the PBGA Package**

## 14.3 Mechanical Dimensions of the PBGA Package

Figure 77 shows the mechanical dimensions of the ZP PBGA package.



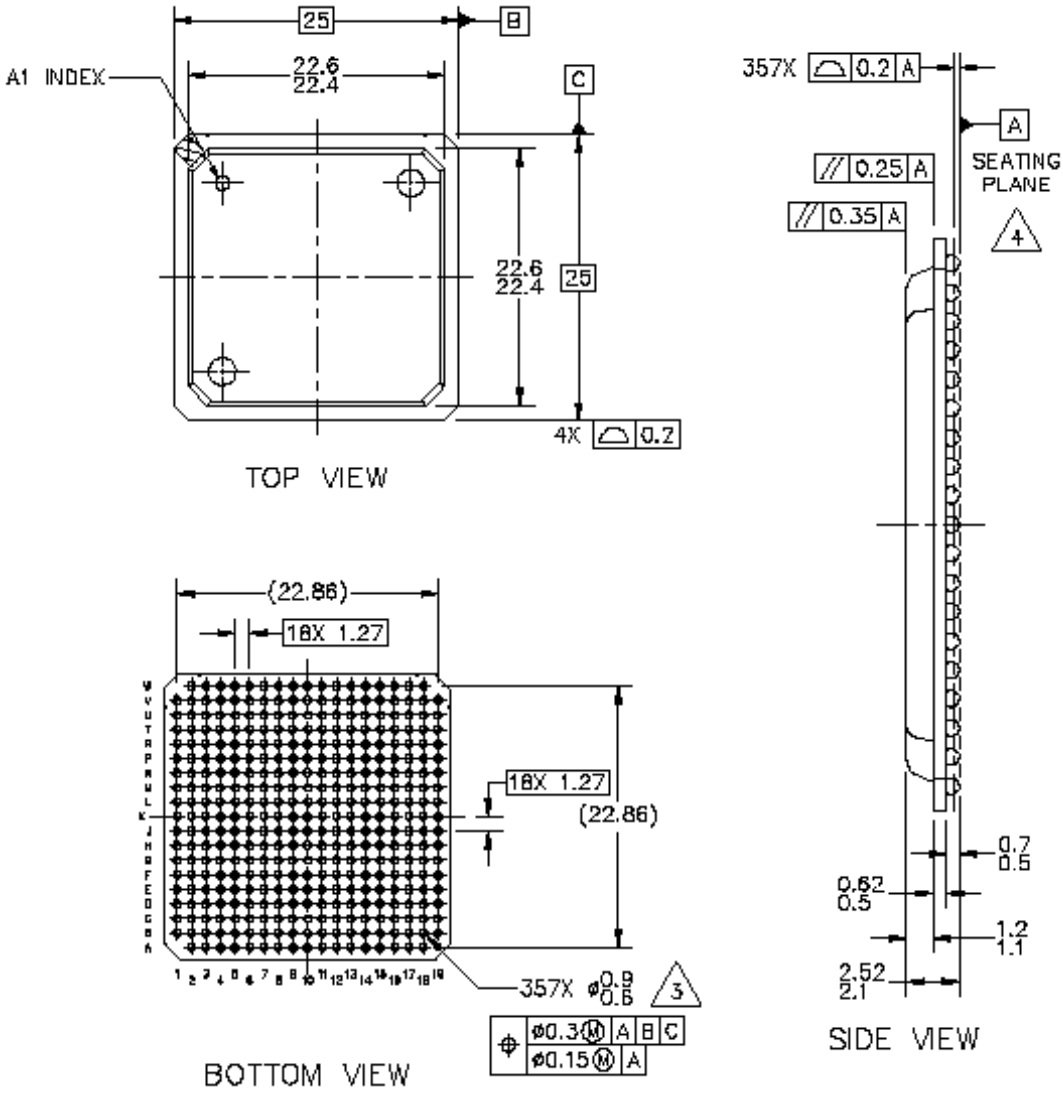

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 2.05 |
| A1 | 0.50 | 0.70 |
| A2 | 0.95 | 1.35 |
| A3 | 0.70 | 0.90 |
| b | 0.60 | 0.90 |
| D | 25.00 BSC | |
| D1 | 22.86 BSC | |
| D2 | 22.40 | 22.60 |
| e | 1.27 BSC | |
| E | 25.00 BSC | |
| E1 | 22.86 BSC | |
| E2 | 22.40 | 22.60 |

**NOTE**

1. Dimensions and tolerance per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to data C.

**Figure 77. Mechanical Dimensions and Bottom Surface Nomenclature of the ZP PBGA Package**

Figure 78 shows the mechanical dimensions of the ZQ PBGA package.




**NOTE**

1. All Dimensions in millimeters.
2. Dimensions and tolerance per ASME Y14.5M, 1994.
3. Maximum Solder Ball Diameter measured parallel to Datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

**Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the ZQ PBGA Package**

# 15 Document Revision History

Table 35 lists significant changes between revisions of this hardware specification.

**Table 35. Document Revision History**

| Revision | Date | Changes |
|---|---|---|
| 10 | 09/2015 | In Table 34, moved MPC855TCVR50D4 and MPC855TCVR66D4 under the extended temperature (–40° to 95°C) and removed MC860ENCVR50D4R2 from the normal temperature Tape and Reel. |
| 9 | 10/2011 | Updated orderable part numbers in Table 34, “MPC860 Family Package/Frequency Availability.” |
| 8 | 08/2007 | • Updated template.<br>• On page 1, added a second paragraph.<br>• After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 1) and renumbered the rest of the figures.<br>• In Figure 3, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level.<br>• In Table 16, changed num 46 description to read, “$\overline{TA}$ assertion to rising edge ...”<br>• In Figure 46, changed $\overline{TA}$ to reflect the rising edge of the clock. |
| 7.0 | 9/2004 | • Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard<br>• Replaced the thermal characteristics in Table 4 by the ZQ package<br>• Add the new parts to the Ordering and Availablity Chart in Table 34<br>• Added the mechanical spec of the ZQ package in Figure 78<br>• Removed all of the old revisions from Table 5 |
| 6.3 | 9/2003 | • Added Section 11.2 on the Port C interrupt pins<br>• Nontechnical reformatting |
| 6.2 | 8/2003 | • Changed B28a through B28d and B29d to show that TRLX can be 0 or 1<br>• Changed reference documentation to reflect the Rev 2 MPC860 PowerQUICC Family Users Manual<br>• Nontechnical reformatting |
| 6.1 | 11/2002 | • Corrected UTOPIA RXenb* and TXenb* timing values<br>• Changed incorrect usage of Vcc to Vdd<br>• Corrected dual port RAM to 8 Kbytes |
| 6 | 10/2002 | • Added the MPC855T. Corrected Figure 26 on page -36. |
| 5.1 | 11/2001 | • Revised template format, removed references to MAC functionality, changed Table 7 B23 max value @ 66 MHz from 2ns to 8ns, added this revision history table |

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