Freescale Semiconductor

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MPC8250
Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC8250 PowerQUICC II™ communications processor.

The following topics are addressed:

The MPC8250 is available in two packages—the standard TBGA package (480 pins) and an alternate PBGA package (516 pins)—as described in Section 4, “Pinout,” and Section 5, “Package Description.” For more information on PBGA packages, contact your Freescale sales office. Note that throughout this document references to the MPC8250 are inclusive of its PBGA version unless otherwise specified.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Figure 1 shows the block diagram for the MPC8250.

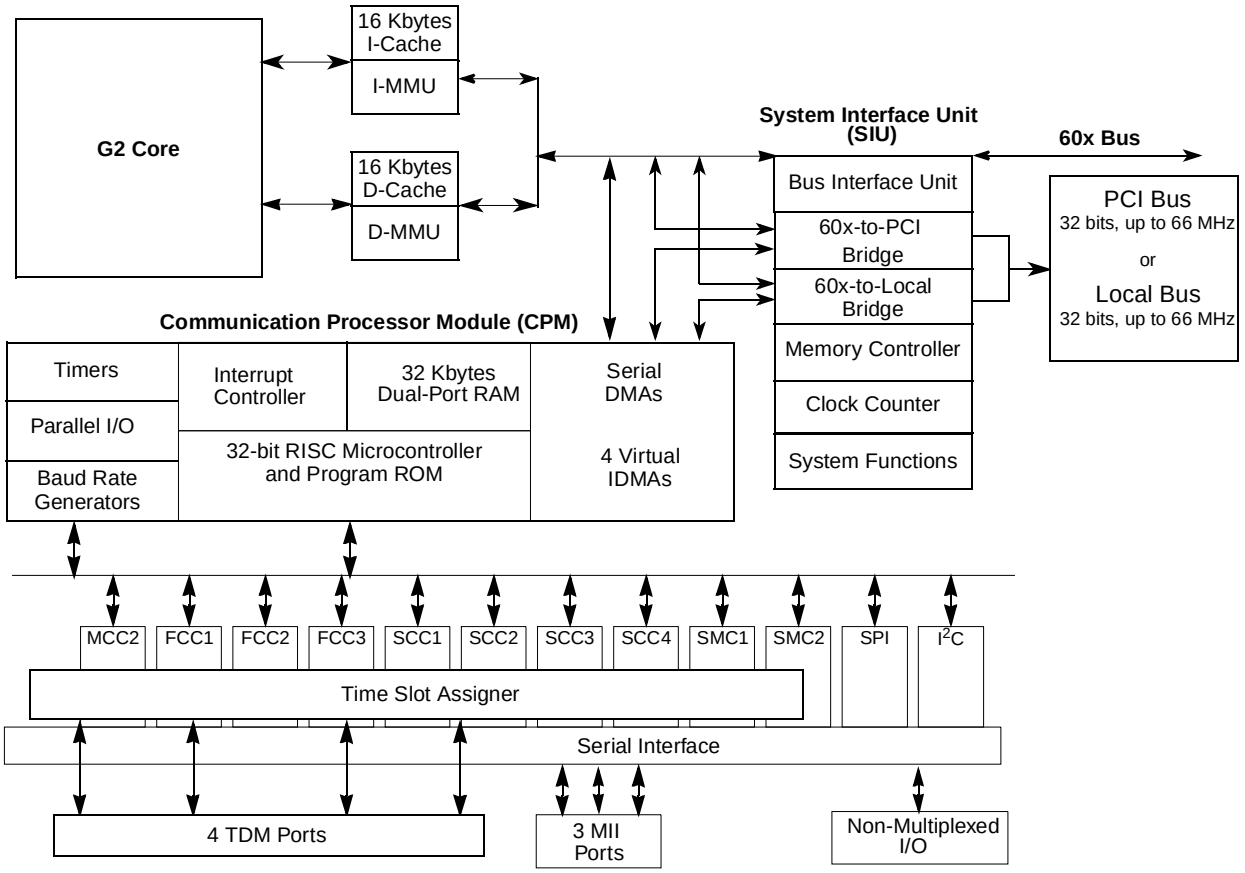


Figure 1. MPC8250 Block Diagram

1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - — A core version of the EC603e microprocessor
  - — System core microprocessor supporting frequencies of 150–200 MHz
  - — Separate 16-Kbyte data and instruction caches:
    - – Four-way set associative
    - – Physically addressed
    - – LRU replacement algorithm
  - — PowerPC architecture-compliant memory management unit (MMU)
  - — Common on-chip processor (COP) test interface
  - — High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)

  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic (1.8 V) and for I/O (3.3V)
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1™ JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)

  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3® CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - One multichannel controller (MCC2)
    - Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    - Transparent
    - UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
    - Microwire compatible
    - Multiple-master, single-master, and slave modes
  - Up to four TDM interfaces
    - Supports one group of four TDM channels

  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  - Supports the I_2O standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  - Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8250.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8250. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings [1]

Rating	Symbol	Value	Unit
Core supply voltage [2]	VDD	-0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.5	V
I/O supply voltage [3]	VDDH	-0.3 – 4.0	V
Input voltage [4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions [1]

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9 [2]	1.7–2.1 [3]	1.9 –2.2 [4]	V
PLL supply voltage	VCCSYN	1.7 – 1.9[2]	1.7–2.1[3]	1.9–2.2[4]	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (-0.3) – 3.465			V
Junction temperature (maximum)	T_j	105 [5]			°C
Ambient temperature	T_A	0–70[5]			°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

2 CPU frequency less than or equal to 200 MHz.

3 CPU frequency greater than 200 MHz but less than 233 MHz.

4 CPU frequency greater than or equal to 233 MHz.

5 Note that for extended temperature parts the range is $(-40)_{T_A}$ – 105_{T_j}.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

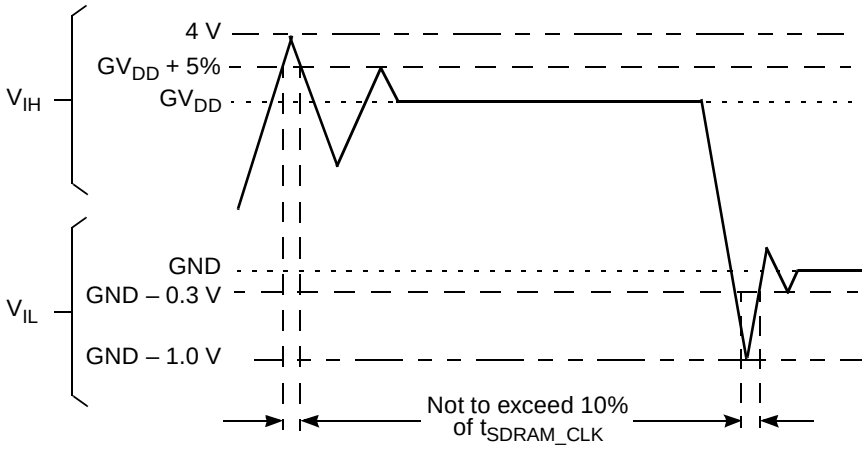


Figure 2. Overshoot/Undershoot Voltage

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics [1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH [2]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA
Output high voltage, I_{OH} = –2 mA	V_{OH}	2.4	—	V

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3]/PCI_CFG[0–3 LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 LOE/LSDRAS/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR L_A15/FRAME/SMI L_A16/TRDY L_A17/IRDY/CKSTP_OUT L_A18/STOP L_A19/DEVSEL L_A20/IDSEL L_A21/PERR L_A22/SERR L_A23/REQ0 L_A24/REQ1/HSEJSW L_A25/GNT0 L_A26/GNT1/HSLED L_A27/GNT2/HSENUM L_A28/RST/CORE_SRESET L_A29/INTA L_A30/REQ2 L_A31 LCL_D(0-31)/AD(0-31) LCL_DP(0-3)/C/BE(0-3) PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 The leakage current is measured for nominal VDD, VCCSYN, and VDD.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient—single-layer board [1]	θ_{JA}	13	24	°C/W	Natural convection
		10	18		1 m/s
Junction to ambient—four-layer board		11	16		Natural convection
		8	13		1 m/s
Junction to board [2]	θ_{JB}	4	8	°C/W	—
Junction to case [3]	θ_{JC}	1.1	6	°C/W	—

1 Assumes no thermal vias

2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8250 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations [1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W) [2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

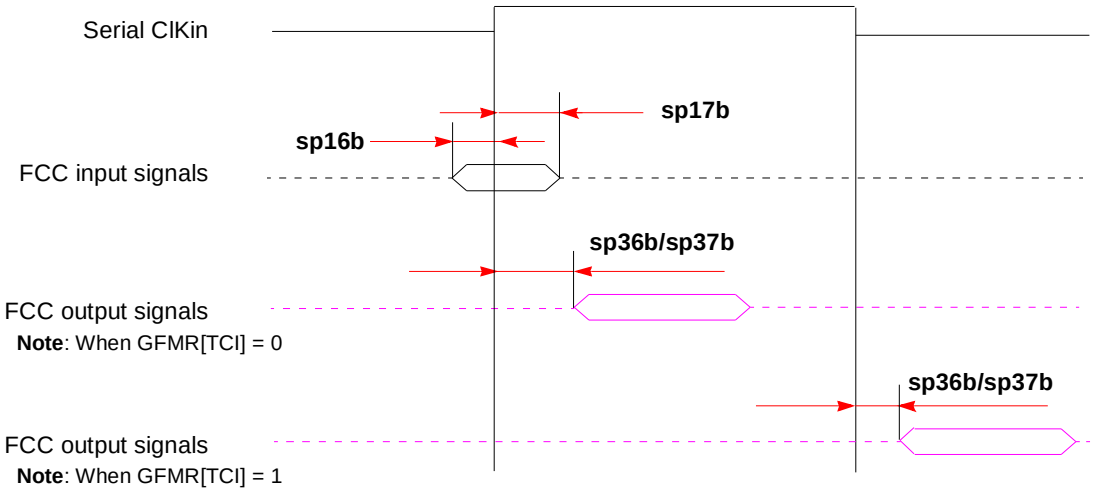


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

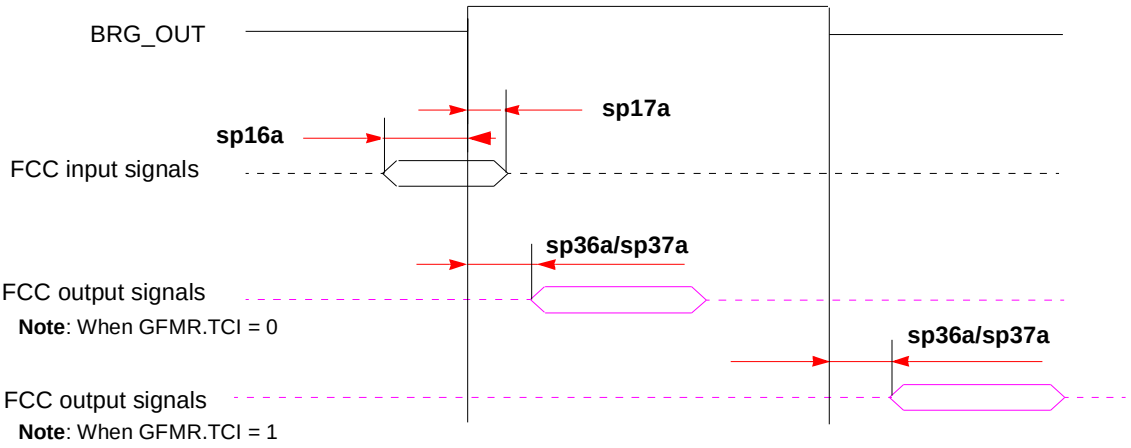
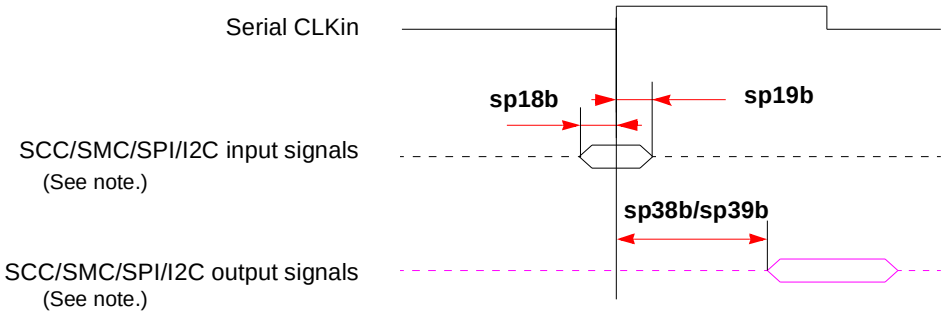


Figure 4. FCC Internal Clock Diagram

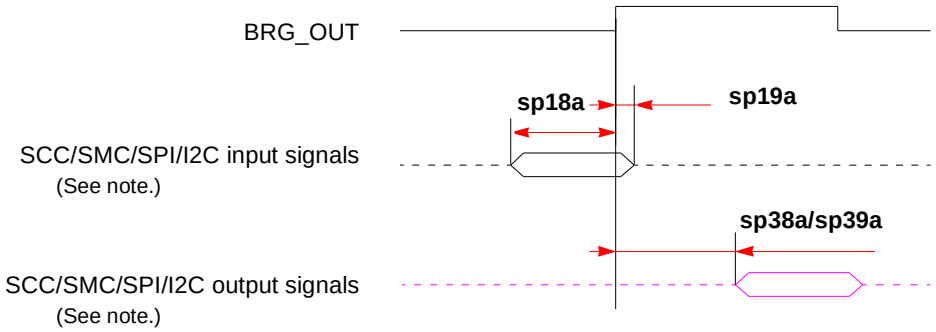
Figure 5 shows the SCC/SMC/SPI/I^{2}C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^{2}C External Clock Diagram

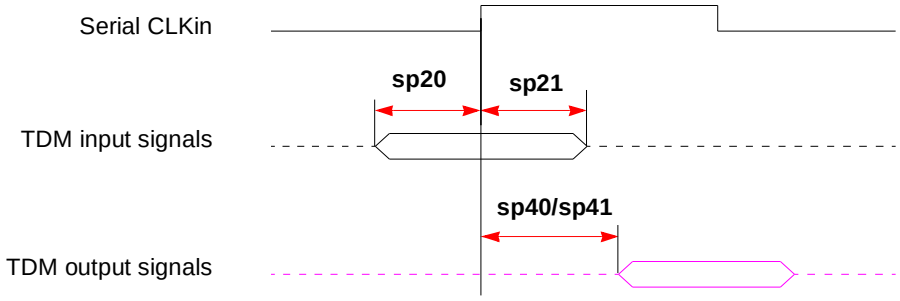
Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

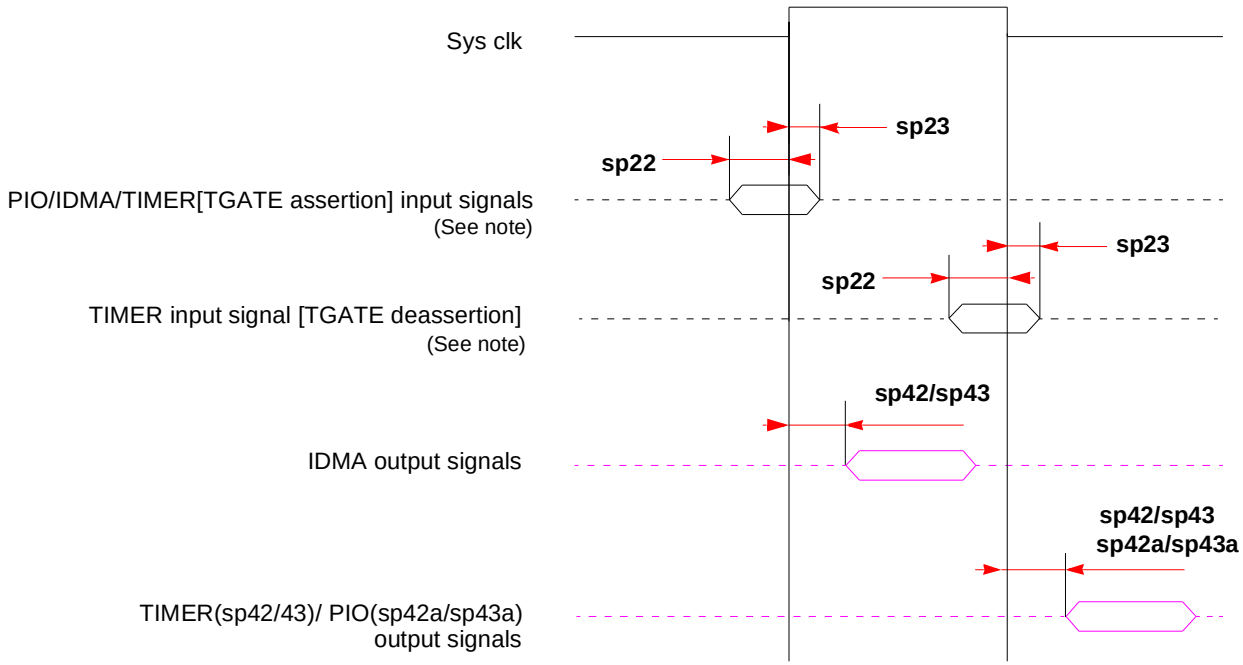
Figure 7 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 9 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 9 shows the interaction of several bus signals.

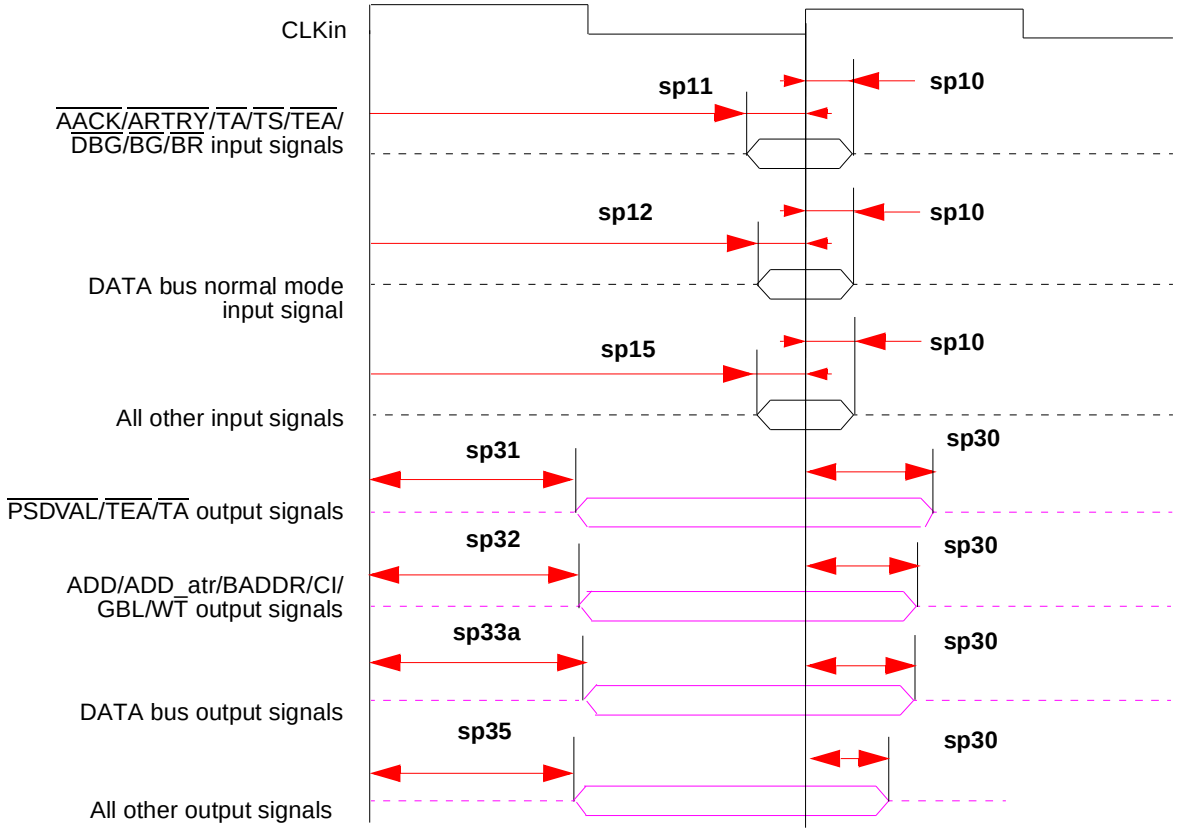


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

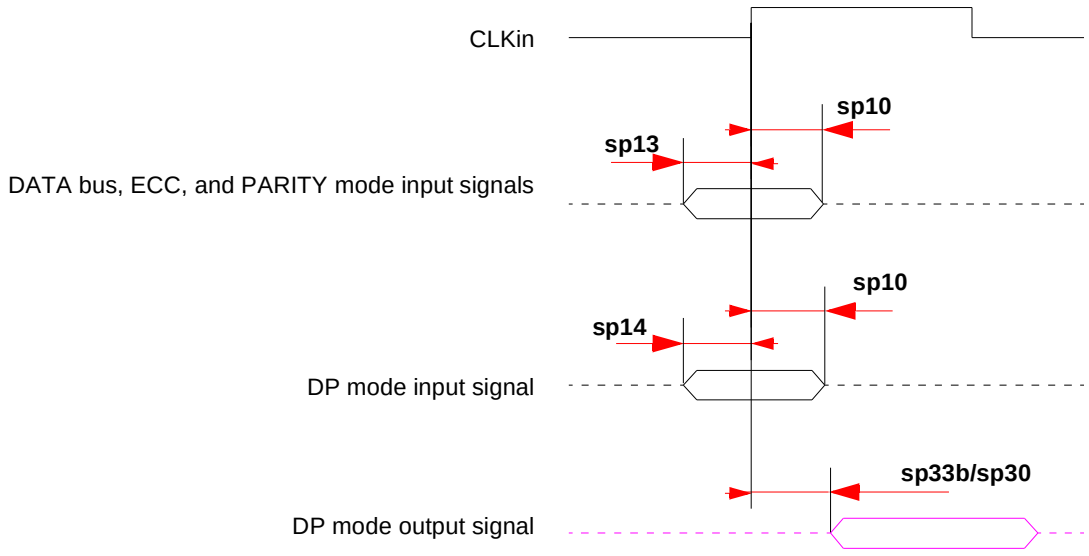


Figure 10. Parity Mode Diagram

Figure 11 shows signal behavior in MEMC mode.

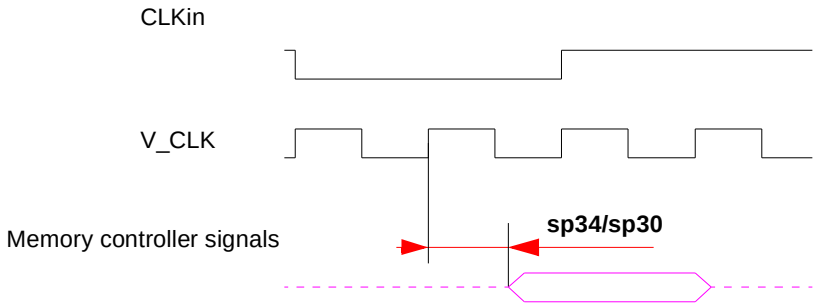


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC8250 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

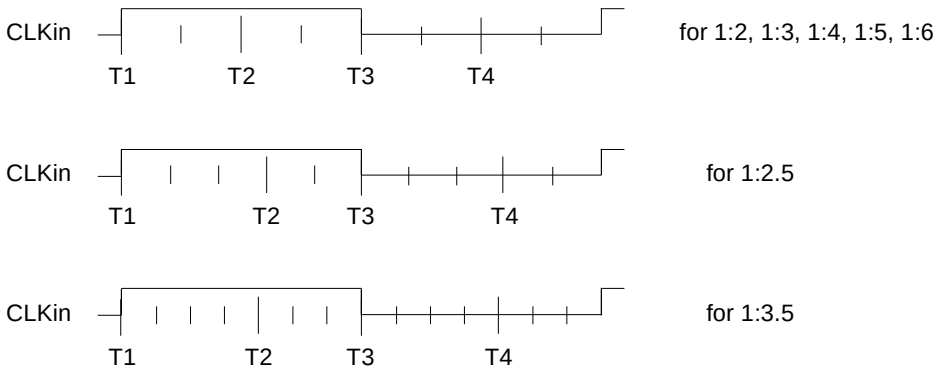


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

The MPC8250 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 12.

Table 12. MPC8250 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 13 and Table 14
0	0	0	PCI host	50–66	Table 15 and Table 16
0	0	1		25–50	
0	1	0	PCI agent	50–66	Table 17 and Table 18
0	1	1		25–50	

1 Determines PCI clock frequency range. Refer to Section 3.2, "PCI Mode."

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected MPC8250 clock operation mode as described in the following sections.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 shows the eight basic clock configurations for the MPC8250. Another 49 configurations are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

Table 13. Clock Default Configurations

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz

Table 13. Clock Default Configurations

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in **boldface** type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 14. Clock Configuration Modes [1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 133 MHz (150 MHz for extended temperature parts) and the CPM ranges between 66–233 MHz.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

3.2 PCI Mode

The PCI mode is selected according to three input pins, as shown in Table 12. In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.2.1 PCI Host Mode

The frequencies listed in Table 15 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 15. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

1 Assumes MODCK_HI = 0000.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to Table 12.

Table 16 describes all possible clock configurations when using the MPC8250's internal PCI bridge in host mode.

Table 16. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**	**4/8**	**33**/16 **MHz**
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 [3]	33 MHz	5	166 MHz	5	166 MHz	5	**33 MHz**
0011_001[3]	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

1 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to Table 12

3 In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in Table 17 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 17. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor [2]	CPM Frequency	Core Multiplication Factor	Core Frequency [3]	Bus Division Factor	60x Bus Frequency[4]
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 17. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor [2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 Assumes MODCK_HI = 0000.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 12

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency / bus division factor

Table 18 describes all possible clock configurations when using the MPC8250’s internal PCI bridge in agent mode.

Table 18. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000 [5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 12

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency / bus division factor

5 In this mode, PCI_MODCK must be “1”.

4 Pinout

This section provides the pin assignments and pinout list for the MPC8250.

4.1 TBGA Package

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, refer to Section 4.2, “PBGA Package.”

4.1.1 TBGA Pin Assignments

Figure 13 shows the pinout of the TBGA package as viewed from the top surface.

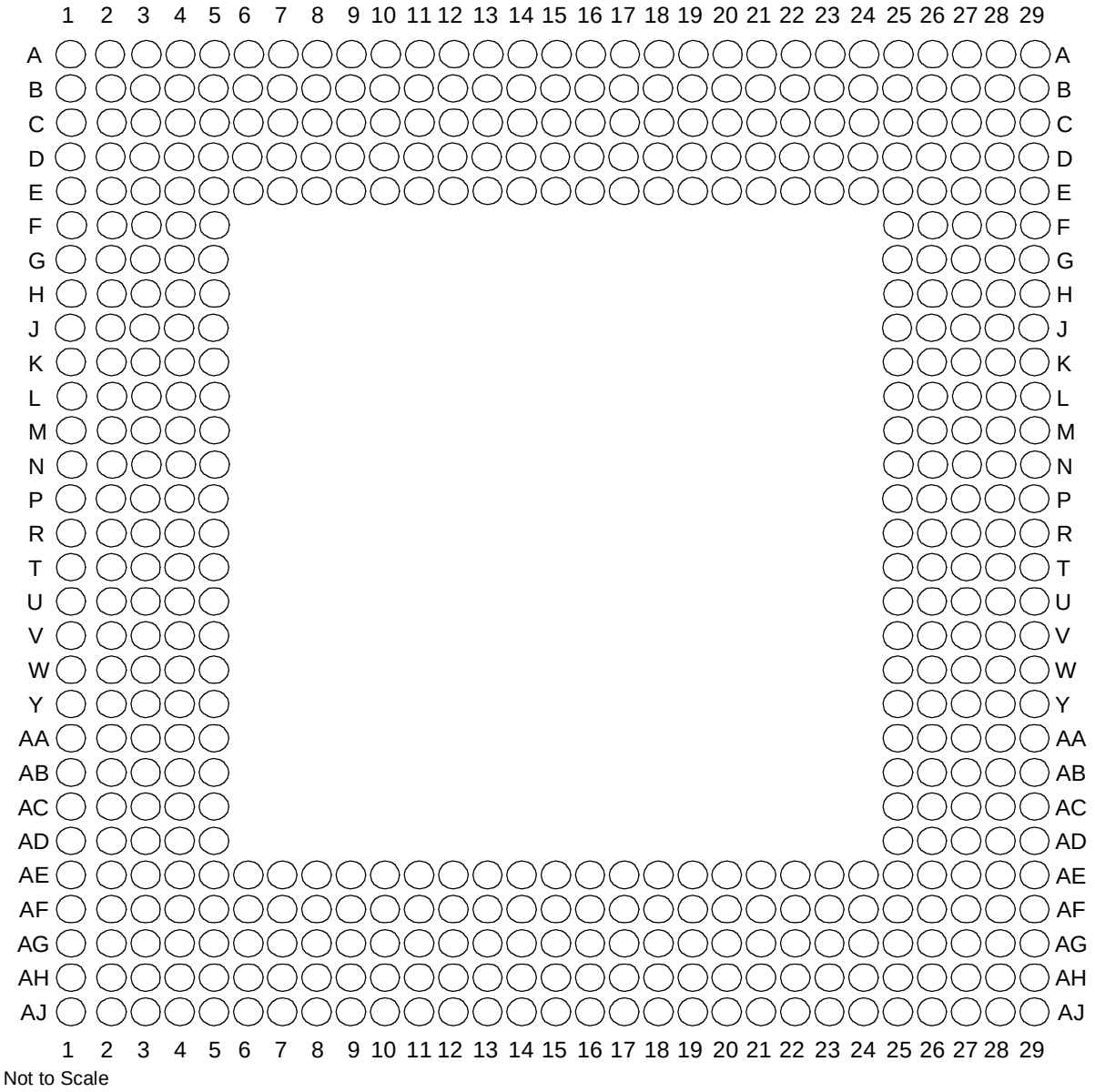


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

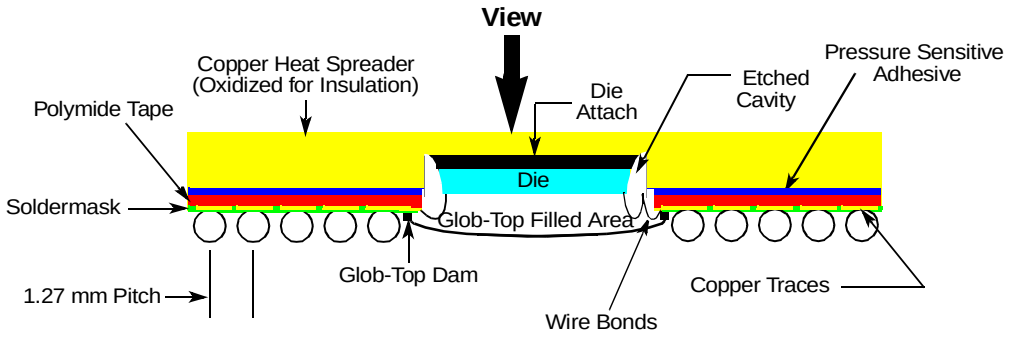


Figure 14. Side View of the TBGA Package

Table 20 shows the pinout list of the TBGA package of the MPC8250. Table 19 defines the conventions and acronyms used in Table 20.

Table 19. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 20. MPC8250 TBGA Package Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP_OUT}}$/$\overline{\text{EXT_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE_SRESET}}$/$\overline{\text{EXT_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
L2_HIT/IRQ4	Y4
$\overline{\text{CPU_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
$\overline{\text{CS10}}$/$\overline{\text{BCTL1}}$	F29
$\overline{\text{CS11}}$/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3	G29
LSDA10/LGPL0/PCI_MODCKH0	D27
LSDWE/LGPL1/PCI_MODCKH1	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2	E26
LSDCAS/LGPL3/PCI_MODCKH3	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK	B27
LWR	D28
L_A14/PAR	N27
L_A15/FRAME/SMI	T29
L_A16/TRDY	R27
L_A17/IRDY/CKSTP_OUT	R26
L_A18/STOP	R29
L_A19/DEVSEL	R28
L_A20/IDSEL	W29
L_A21/PERR	P28
L_A22/SERR	N26
L_A23/REQ0	AA27
L_A24/REQ1/HSEJSW	P29
L_A25/GNT0	AA26
L_A26/GNT1/HSLED	N25
L_A27/GNT2/HSENUM	AA25
L_A28/RST/CORE_SRESET	AB29
L_A29/INTA	AB28
L_A30/REQ2	P25
L_A31/DLLOUT	AB27
LCL_D0/AD0	H29

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{\text{BE0}}$	L28
LCL_DP1/C1/$\overline{\text{BE1}}$	N28
LCL_DP2/C2/$\overline{\text{BE2}}$	T28
LCL_DP3/C3/$\overline{\text{BE3}}$	W28

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC29 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC25[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AE28[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AG28[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AG26[1]
PA6	AE24[1]
PA7/SMSYN2	AH25[1]
PA8/SMRXD2	AF23[1]
PA9/SMTXD2	AH23[1]
PA10/MSNUM5	AE22[1]
PA11/MSNUM4	AH22[1]
PA12/MSNUM3	AJ21[1]
PA13/MSNUM2	AH20[1]
PA14/FCC1_RXD3	AG19[1]
PA15/FCC1_RXD2	AF18[1]
PA16/FCC1_RXD1	AF17[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PA17/FCC1_RXD0/FCC1_RXD	AE16[1]
PA18/FCC1_TXD0/FCC1_TXD	AJ16[1]
PA19/FCC1_TXD1	AG15[1]
PA20/FCC1_TXD2	AJ13[1]
PA21/FCC1_TXD3	AE13[1]
PA22	AF12[1]
PA23	AG11[1]
PA24/MSNUM1	AH9[1]
PA25/MSNUM0	AJ8[1]
PA26/FCC1_MII_RX_ER	AH7[1]
PA27/FCC1_MII_RX_DV	AF7[1]
PA28/FCC1_MII_TX_EN	AD5[1]
PA29/FCC1_MII_TX_ER	AF1[1]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1_RTS}}$	AD3[1]
PA31/FCC1_MII_COL	AB5[1]
PB4/FCC3_TXD3/L1RSYNCA2/$\overline{\text{FCC3_RTS}}$	AD28[1]
PB5/FCC3_TXD2/L1TSYNCA2/L1GNTA2	AD26[1]
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	AD25[1]
PB7/FCC3_TXD0/FCC3_TXD/L1TXDA2/L1TXD0A2	AE26[1]
PB8/FCC3_RXD0/FCC3_RXD/TXD3	AH27[1]
PB9/FCC3_RXD1/L1TXD2A2	AG24[1]
PB10/FCC3_RXD2	AH24[1]
PB11/FCC3_RXD3	AJ24[1]
PB12/FCC3_MII_CRS/TXD2	AG22[1]
PB13/FCC3_MII_COL/L1TXD1A2	AH21[1]
PB14/FCC3_MII_TX_EN/RXD3	AG20[1]
PB15/FCC3_MII_TX_ER/RXD2	AF19[1]
PB16/FCC3_MII_RX_ER/CLK18	AJ18[1]
PB17/FCC3_MII_RX_DV/CLK17	AJ17[1]
PB18/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[1]
PB19/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[1]
PB20/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[1]
PB21/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2	AH11[1]
PB22/FCC2_TXD0/FCC2_TXD/L1RXDD2	AH16[1]
PB23/FCC2_TXD1/L1TXDD2	AE15[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[1]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[1]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[1]
PC30/CLK2/$\overline{\text{TOUT1}}$	AE1[1]
PC31/CLK1/BRGO1	AD1[1]
PD4/BRGO8/$\overline{\text{FCC3_RTS}}$/SMRXD2	AC28[1]
PD5/$\overline{\text{DONE1}}$	AD27[1]
PD6/$\overline{\text{DACK1}}$	AF29[1]
PD7/SMSYN1FCC1_TXCLAV2	AF28[1]
PD8/SMRXD1/BRGO5	AG25[1]
PD9/SMTXD1/BRGO3	AH26[1]
PD10/L1CLKOB2/BRGO4	AJ27[1]
PD11/$\overline{\text{L1RQB2}}$	AJ23[1]
PD12	AG23[1]
PD13	AJ22[1]
PD14/L1CLKOC2/I2CSCL	AE20[1]
PD15/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[1]
PD16/SPIMISO	AG18[1]
PD17/BRGO2/SPIMOSI	AG17[1]
PD18/SPICLK	AF16[1]
PD19/SPISEL/BRGO	AH15[1]
PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2	AJ14[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	AH13[1]
PD22/RXD4/L1TXD0A2/L1TXDA2	AJ12[1]
PD23/$\overline{\text{RTS3}}$/TENA3	AE12[1]
PD24/TXD3	AF10[1]
PD25/RXD3	AG9[1]
PD26/$\overline{\text{RTS2}}$/TENA2	AH8[1]
PD27/TXD2	AG7[1]
PD28/RXD2	AE4[1]
PD29/$\overline{\text{RTS1}}$/TENA1	AG1[1]
PD30/TXD1	AD4[1]
PD31/RXD1	AD2[1]
VCCSYN	AB3
VCCSYN1	B9

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
GNDSYN	AB1
CLKIN2	AE11
SPARE4 [2]	U5
$\overline{\text{PCI_MODE}}$ [3]	AF25
SPARE6[2]	V4
THERMAL0 [4]	AA1
THERMAL1[4]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, this pin should be pulled up or left floating.

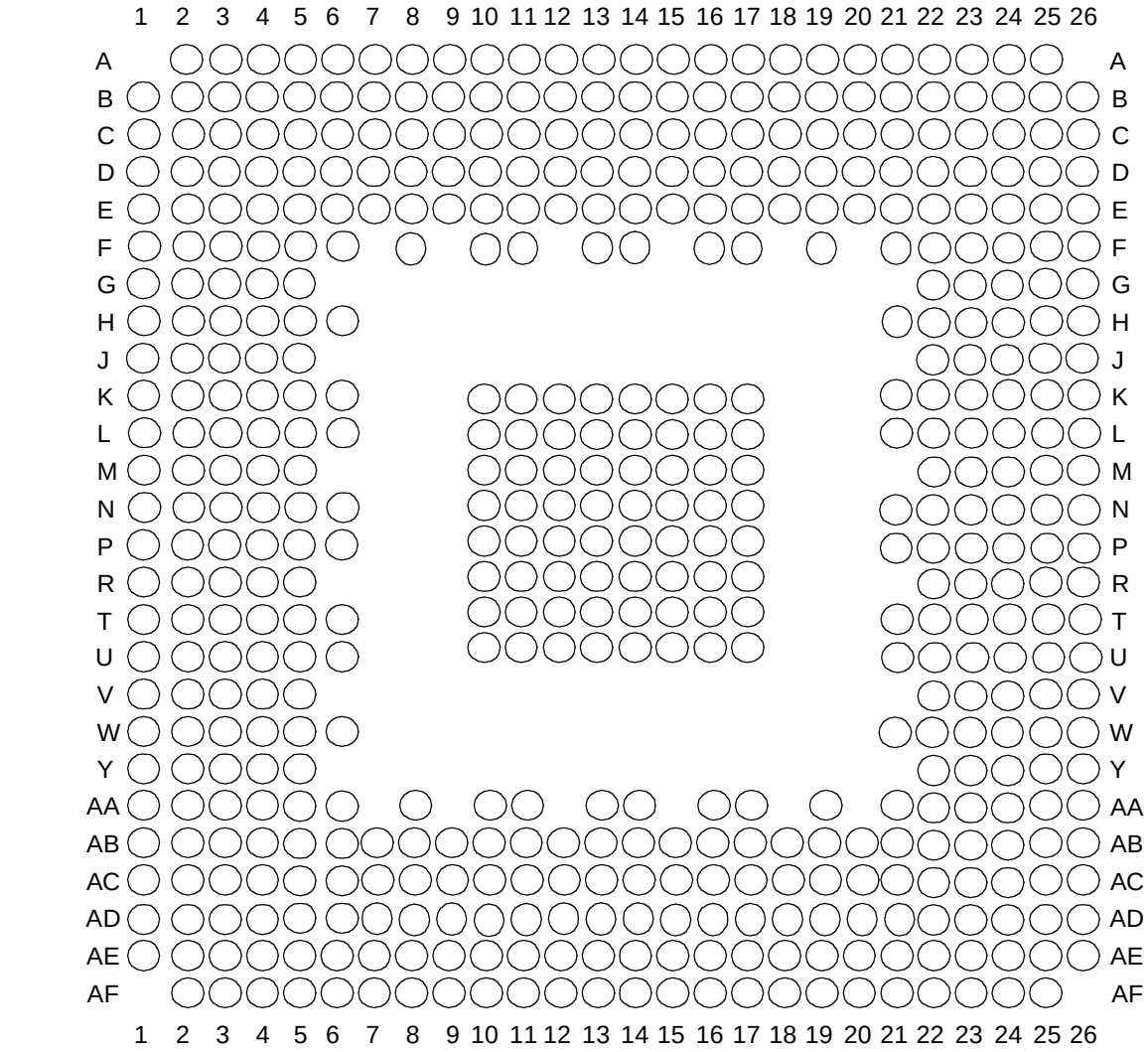
4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D) available at www.freescale.com.

4.2 PBGA Package

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8250, refer to Section 4.1, “TBGA Package.”

4.2.1 PBGA Pin Assignments

Figure 15 shows the pinout of the PBGA package as viewed from the top surface.



Not to Scale

Figure 15. Pinout of the 516 PBGA Package (View from Top)

Figure 16 shows the side profile of the PBGA package to indicate the direction of the top surface view.

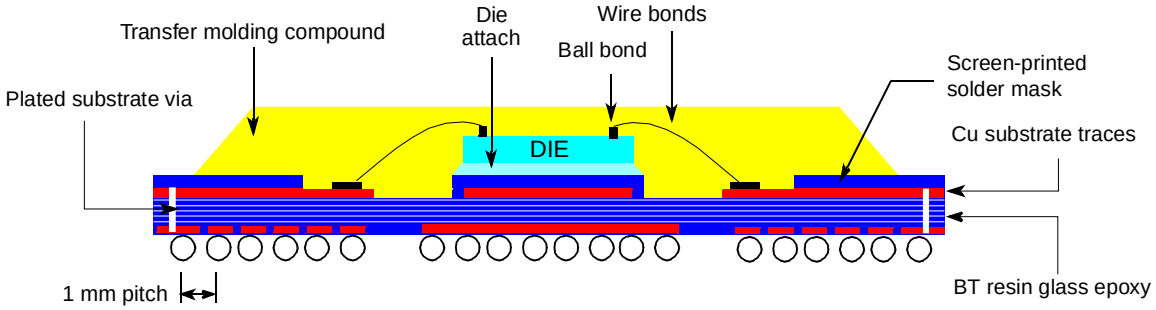


Figure 16. Side View of the PBGA Package

Table 22 shows the pinout list of the PBGA package of the MPC8250. Table 21 defines conventions and acronyms used in Table 22.

Table 21. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 22. MPC8250 PBGA Package Pinout List

Pin Name	Ball
BR	C16
BG	D2
ABB/IRQ2	C1
TS	D1
A0	D5
A1	E8
A2	C4
A3	B4
A4	A4
A5	D7
A6	D8
A7	C6
A8	B5
A9	B6
A10	C7
A11	C8
A12	A6
A13	D9

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
A14	F11
A15	B7
A16	B8
A17	C9
A18	A7
A19	B9
A20	E11
A21	A8
A22	D11
A23	B10
A24	C11
A25	A9
A26	B11
A27	C12
A28	D12
A29	A10
A30	B12
A31	B13
TT0	E7
TT1	B3
TT2	F8
TT3	A3
TT4	C3
TBST	F5
TSIZ0	E3
TSIZ1	E2
TSIZ2	E1
TSIZ3	E4
AACK	D3
ARTRY	C2
DBG	A14
DBB/IRQ3	C15
D0	W4
D1	Y1
D2	V1

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D3	P4
D4	N3
D5	K5
D6	J4
D7	G1
D8	AB1
D9	U4
D10	U2
D11	N6
D12	N1
D13	L1
D14	J5
D15	G3
D16	AA2
D17	W1
D18	T3
D19	T1
D20	M2
D21	K2
D22	J1
D23	G4
D24	U5
D25	T5
D26	P5
D27	P3
D28	M3
D29	K3
D30	H2
D31	G5
D32	AA1
D33	V2
D34	U1
D35	P2
D36	M4
D37	K4

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D38	H3
D39	F2
D40	Y2
D41	U3
D42	T2
D43	N2
D44	M5
D45	K1
D46	H4
D47	F1
D48	W2
D49	T4
D50	R3
D51	N4
D52	M1
D53	J2
D54	H5
D55	F3
D56	V3
D57	R5
D58	R2
D59	N5
D60	L2
D61	J3
D62	H1
D63	F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT_BR2}}$	AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT_BG2}}$	W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT_DBG2}}$	AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP_OUT}}$/$\overline{\text{EXT_BR3}}$	AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE_SRESET}}$/$\overline{\text{EXT_BG3}}$	AD1
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT_DBG3}}$	AC1
$\overline{\text{IRQ6}}$/DP6/CSE0	AB2
$\overline{\text{IRQ7}}$/DP7/CSE1	Y3
PSDVAL	D15

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
TA	Y4
TEA	D16
GBL/IRQ1	E15
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	D14
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	E14
L2_HIT/IRQ4	A17
$\overline{\text{CPU_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	B14
CPU_DBG	F13
CPU_BR	B17
CS0	AC6
CS1	AD6
CS2	AE6
CS3	AB7
CS4	AF7
CS5	AC7
CS6	AD7
CS7	AF8
CS8	AE8
CS9	AD8
$\overline{\text{CS10}}$/$\overline{\text{BCTL1}}$	AC8
$\overline{\text{CS11}}$/AP0	AB8
BADDR27	C13
BADDR28	A12
ALE	D13
BCTL0	AF4
PWE0/PSDDQM0/PBS0	AA5
PWE1/PSDDQM1/PBS1	AE4
PWE2/PSDDQM2/PBS2	AD4
PWE3/PSDDQM3/PBS3	AF3
PWE4/PSDDQM4/PBS4	AB4
PWE5/PSDDQM5/PBS5	AE3
PWE6/PSDDQM6/PBS6	AF2
PWE7/PSDDQM7/PBS7	AD3
PSDA10/PGPL0	AE2
$\overline{\text{PSDWE}}$/PGPL1	AD2

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
POE/PSDRAS/PGPL2	AE1
PSDCAS/PGPL3	AC3
PGTA/PUPMWAIT/PGPL4/PPBS	W6
PSDAMUX/PGPL5	AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0	AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1	AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2	AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3	AF9
LSDA10/LGPL0/PCI_MODCKH0	AB6
LSDWE/LGPL1/PCI_MODCKH1	AF5
LOE/LSDRAS/LGPL2/PCI_MODCKH2	AE5
LSDCAS/LGPL3/PCI_MODCKH3	AD5
LGTA/LUPMWAIT/LGPL4/LPBS	AC5
LGPL5/LSDAMUX/PCI_MODCK	AB5
LWR	AF6
L_A14/PAR	AE13
L_A15/FRAME/SMI	AD15
L_A16/TRDY	AF16
L_A17/IRDY/CKSTP_OUT	AF15
L_A18/STOP	AE15
L_A19/DEVSEL	AE14
L_A20/IDSEL	AC17
L_A21/PERR	AD14
L_A22/SERR	AF13
L_A23/REQ0	AE20
L_A24/REQ1/HSEJSW	AC14
L_A25/GNT0	AC19
L_A26/GNT1/HSLED	AD13
L_A27/GNT2/HSENUM	AF21
L_A28/RST/CORE_SRESET	AF22
L_A29/INTA	AE21
L_A30/REQ2	AB14
L_A31/DLLOUT	AD20
LCL_D0/AD0	AB9
LCL_D1/AD1	AB10

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
LCL_D2/AD2	AC10
LCL_D3/AD3	AD10
LCL_D4/AD4	AE10
LCL_D5/AD5	AF10
LCL_D6/AD6	AF11
LCL_D7/AD7	AB12
LCL_D8/AD8	AB11
LCL_D9/AD9	AF12
LCL_D10/AD10	AE11
LCL_D11/AD11	AC13
LCL_D12/AD12	AC12
LCL_D13/AD13	AB13
LCL_D14/AD14	AD12
LCL_D15/AD15	AF14
LCL_D16/AD16	AF17
LCL_D17/AD17	AE16
LCL_D18/AD18	AD16
LCL_D19/AD19	AC16
LCL_D20/AD20	AB16
LCL_D21/AD21	AF18
LCL_D22/AD22	AE17
LCL_D23/AD23	AD17
LCL_D24/AD24	AB17
LCL_D25/AD25	AE18
LCL_D26/AD26	AD18
LCL_D27/AD27	AC18
LCL_D28/AD28	AE19
LCL_D29/AD29	AF20
LCL_D30/AD30	AD19
LCL_D31/AD31	AB18
LCL_DP0/C0/$\overline{\text{BE0}}$	AE12
LCL_DP1/C1/$\overline{\text{BE1}}$	AA13
LCL_DP2/C2/$\overline{\text{BE2}}$	AC15
LCL_DP3/C3/$\overline{\text{BE3}}$	AF19
IRQ0/NMI_OUT	A11

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
IRQ7/INT_OUT/APE	E5
TRST	F22
TCK	A24
TMS	C24
TDI	A25
TDO	B24
TRIS	C19
PORESET	B25
HRESET	D24
SRESET	E23
QREQ	D18
RSTCONF	E24
MODCK1/AP1/TC0/BNKSEL0	B16
MODCK2/AP2/TC1/BNKSEL1	F16
MODCK3/AP3/TC2/BNKSEL2	A15
XFC	A18
CLKIN1	G22
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC20 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC21[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AF25[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AE24[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AA21[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AD25[1]
PA6	AC24[1]
PA7/SMSYN2	AA22[1]
PA8/SMRXD2	AA23[1]
PA9/SMTXD2	Y26[1]
PA10/MSNUM5	W22[1]
PA11/MSNUM4	W23[1]
PA12/MSNUM3	V26[1]
PA13/MSNUM2	V25[1]
PA14/FCC1_RXD3	T22[1]
PA15/FCC1_RXD2	T25[1]
PA16/FCC1_RXD1	R24[1]
PA17/FCC1_RXD0/FCC1_RXD	P22[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PA18/FCC1_TXD0/FCC1_TXD	N26[1]
PA19/FCC1_TXD1	N23[1]
PA20/FCC1_TXD2	K26[1]
PA21/FCC1_TXD3	L23[1]
PA22	K23[1]
PA23	H26[1]
PA24/MSNUM1	F25[1]
PA25/MSNUM0	D26[1]
PA26/FCC1_MII_RX_ER	D25[1]
PA27/FCC1_MII_RX_DV	C25[1]
PA28/FCC1_MII_TX_EN	C22[1]
PA29/FCC1_MII_TX_ER	B21[1]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1_RTS}}$	A20[1]
PA31/FCC1_MII_COL	A19[1]
PB4/FCC3_TXD3/L1RSYNCA2/ $\overline{\text{FCC3_RTS}}$	AD21[1]
PB5/FCC3_TXD2/L1TSYNCA2/ L1GNTA2	AD22[1]
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	AC22[1]
PB7/FCC3_TXD0/FCC3_TXD/ L1TXDA2/L1TXD0A2	AE26[1]
PB8/FCC3_RXD0/FCC3_RXD/TXD3	AB23[1]
PB9/FCC3_RXD1/L1TXD2A2	AC26[1]
PB10/FCC3_RXD2	AB26[1]
PB11/FCC3_RXD3	AA25[1]
PB12/FCC3_MII_CRS/TXD2	W26[1]
PB13/FCC3_MII_COL/L1TXD1A2	W25[1]
PB14/FCC3_MII_TX_EN/RXD3	V24[1]
PB15/FCC3_MII_TX_ER/RXD2	U24[1]
PB16/FCC3_MII_RX_ER/CLK18	R22[1]
PB17/FCC3_MII_RX_DV/CLK17	R23[1]
PB18/FCC2_RXD3/L1CLKOD2/ L1RXD2A2	M23[1]
PB19FCC2_RXD2/L1RQD2/L1RXD3A2	L24[1]
PB20/FCC2_RXD1/L1RSYNCD2/ L1TXD1A1	K24[1]
PB21/FCC2_RXD0/FCC2_RXD/ L1TSYNCD2/L1GNTD2	L21[1]
PB22/FCC2_TXD0/FCC2_TXD/ L1RXDD2	P25[1]
PB23/FCC2_TXD1/L1TXDD2	N25[1]
PB24/FCC2_TXD2/L1RSYNCC2	E26[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	H23[1]
PB26/FCC2_MII_CRS/L1RXDC2	C26[1]
PB27/FCC2_MII_COL/L1TXDC2	B26[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1	A22[1]
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	A21[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	E20[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	C20[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/ L1CLKOA2	AE22[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AA19[1]
PC2/$\overline{\text{FCC3_CD}}$/$\overline{\text{DONE2}}$	AF24[1]
PC3/$\overline{\text{FCC3_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE25[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2_CD}}$	AB22[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2_CTS}}$	AC25[1]
PC6/$\overline{\text{FCC1_CD}}$	AB25[1]
PC7/$\overline{\text{FCC1_CTS}}$	AA24[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	Y24[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2	U22[1]
PC10/$\overline{\text{CD3}}$/RENA3	V23[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	U23[1]
PC12/$\overline{\text{CD2}}$/RENA2	T26[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	R26[1]
PC14/$\overline{\text{CD1}}$/RENA1	P26[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	P24[1]
PC16/CLK16/TIN4	M26[1]
PC17/CLK15/TIN3/BRGO8	L26[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	M24[1]
PC19/CLK13/BRGO7/SPICLK	L22[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	K25[1]
PC21/CLK11/BRGO6	J25[1]
PC22/CLK10/$\overline{\text{DONE1}}$	G26[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	F26[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	G24[1]
PC25/CLK7/BRGO4	E25[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	G23[1]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3	B23[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	E22[1]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	E21[1]
PC30/CLK2/TOUT1	D21[1]
PC31/CLK1/BRGO1	B20[1]
PD4/BRGO8/FCC3_RTS/SMRXD2	AF23[1]
PD5/DONE1	AE23[1]
PD6/DACK1	AB21[1]
PD7/SMSYN1/FCC1_TXCLAV2	AD23[1]
PD8/SMRXD1/BRGO5	AD26[1]
PD9/SMTXD1/BRGO3	Y22[1]
PD10/L1CLKOB2/BRGO4	AB24[1]
PD11/L1RQB2	Y23[1]
PD12	AA26[1]
PD13	W24[1]
PD14/L1CLKOC2/I2CSCL	V22[1]
PD15/L1RQC2/I2CSDA	U26[1]
PD16/SPIMISO	T23[1]
PD17/BRGO2/SPIMOSI	R25[1]
PD18/SPICLK	P23[1]
PD19/SPISEL/BRGO1	N22[1]
PD20/RTS4/TENA4/L1RSYNCA2	M25[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	L25[1]
PD22/RXD4L1TXD0A2/L1TXDA2	J26[1]
PD23/RTS3/TENA3	K22[1]
PD24/TXD3	G25[1]
PD25/RXD3	H24[1]
PD26/RTS2/TENA2	F24[1]
PD27/TXD2	H22[1]
PD28/RXD2	B22[1]
PD29/RTS1/TENA1	D22[1]
PD30/TXD1	C21[1]
PD31/RXD1	E19[1]
VCCSYN	D19
VCCSYN1	K6
GNDSYN	B18

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
CLKIN2	K21
SPARE4 [2]	C14
$\overline{\text{PCI_MODE}}$ [3]	AD24
SPARE6[2]	B15
THERMAL0 [4]	E17
THERMAL1[4]	C23
I/O power	E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power	L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground	A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, must be pulled up or left floating.

4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D).

5 Package Description

The following sections provide the package parameters and mechanical dimensions.

5.1 Package Parameters

Package parameters are provided in Table 23.

Table 23. Package Parameters

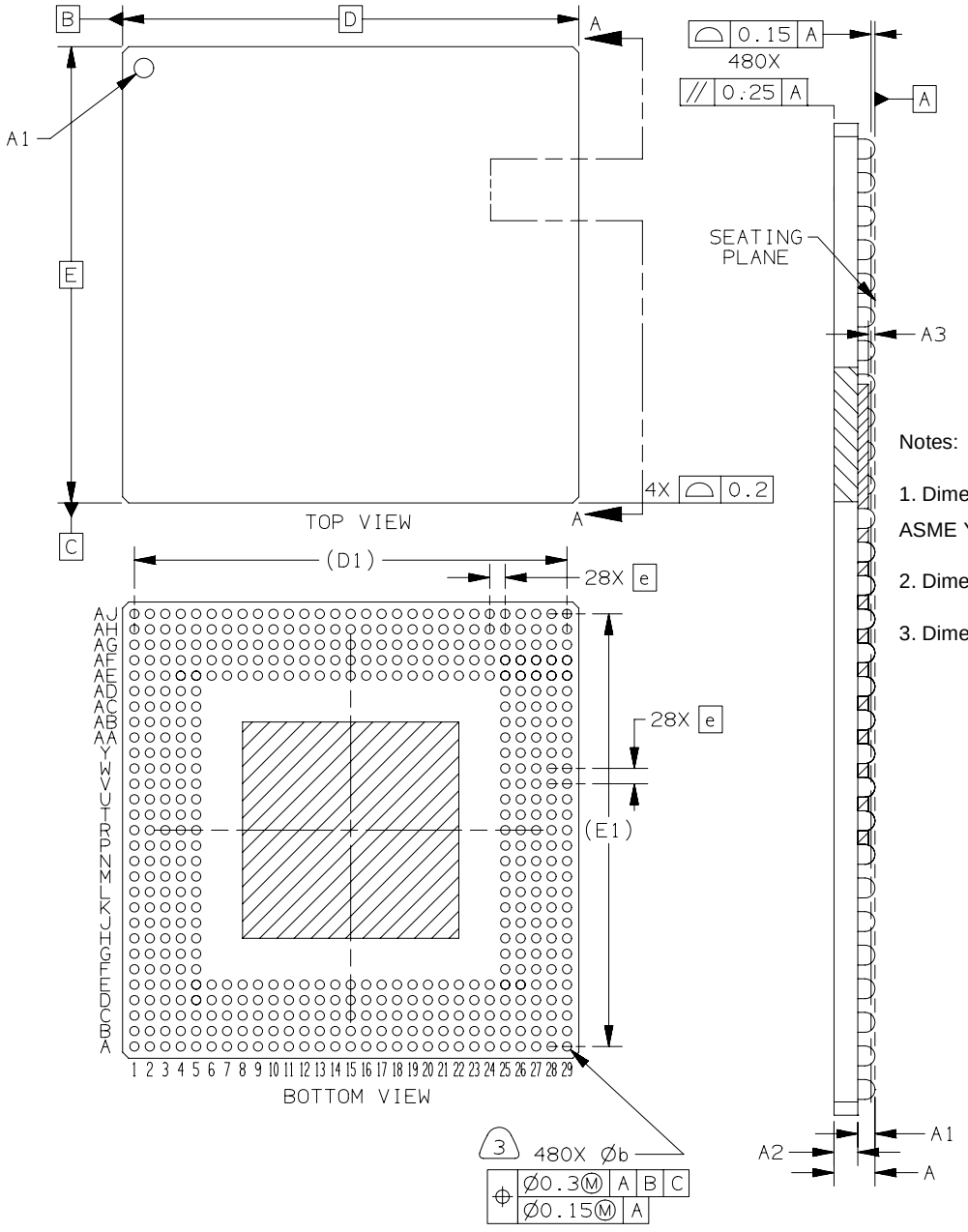
Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8250	37.5 × 37.5	TBGA	480	1.27	1.55
VV			TBGA (Pb free)			
ZO		27 × 27	PBGA	516	1	2.25
VR			PBGA (Pb free)			

5.2 Mechanical Dimensions

This section discusses the TBGA and PBGA package dimensions.

5.2.1 TBGA Package Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

5.2.2 PBGA Package Dimensions

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

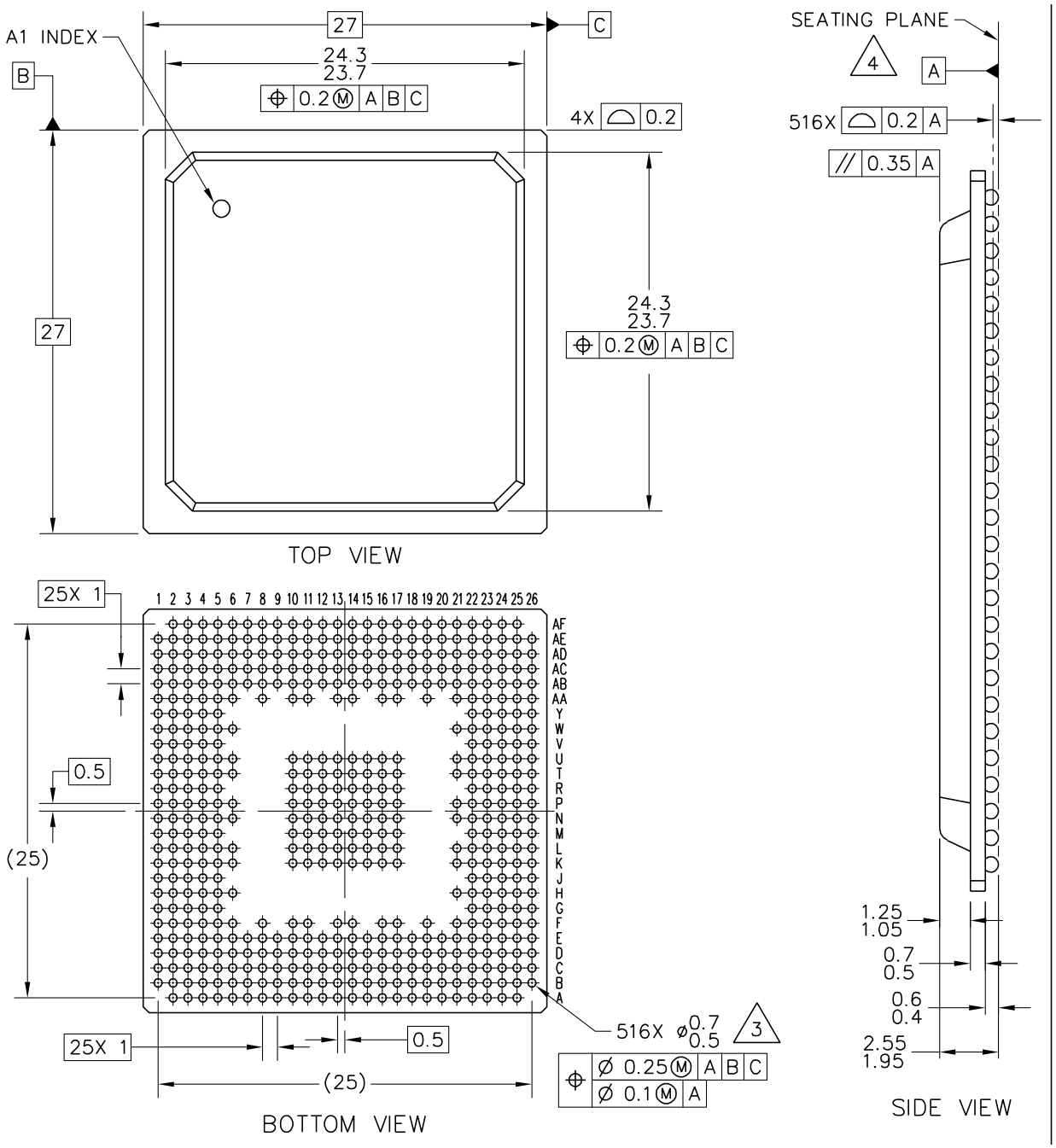


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

6 Ordering Information

Figure 19 provides an example of the Freescale part numbering nomenclature for the MPC8250. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

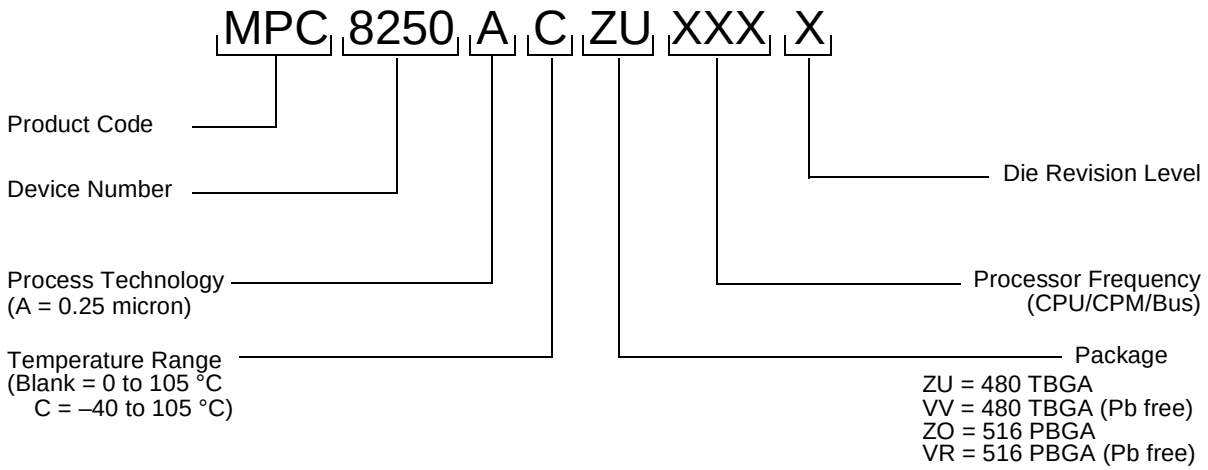


Figure 19. Freescale Part Number Key

7 Document Revision History

Table 24 provides a revision history for this template.

Table 24. Document Revision History

Revision	Date	Substantive Changes
2	7/2009	Updated TBGA and PBGA packaging information.
1	3/2005	Document template update
0.9	8/2003	• Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4 • Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 • Addition of Figure 2 • Addition of note 1 to Table 3 • Table 4: Changes to θ_{JA}. Addition of θ_{JB} and θ_{JC} • Table 7, Figure 8: Addition of sp42a/sp43a • Figure 3 through Figure 8: Addition of notes or modifications • Table 9: Change to sp10 • Table 14, Table 16, and Table 18: Removal of PLL bypass mode from clock tables • Table 20 and Table 22: Addition of note 1 • Addition of SPICLK to PC19 in Table 20 and Table 22. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 20 and Table 22.
0.8	11/2002	Table 22, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 53)
0.7	10/2002	Table 22, “VR Pinout”: Addition of L3 to the Core (VDDx) pin list (page 53)

Table 24. Document Revision History (continued)

Revision	Date	Substantive Changes
0.6	10/2002	Table 22, “VR Pinout”: corrected ball assignment for the following pins—A12–A17, $\overline{TA}$, PD5, PC2.
0.5	9/2002	Addition of VR (516 PBGA) package information. Refer to sections 2.2, 4.2, and 5.
0.4	5/2002	• Table 2: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 14: Note 3 • Table 16: Note 1 • Table 18: Note 3
0.3	3/2002	• Table 20: modified note to pin AF25.
0.2	3/2202	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.1	2/2002	• Note 2 for Table 4 (changes in italics): “...greater than *or equal to 266* MHz, *200* MHz CPM...” • Table 18: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: footnotes added to pins at AE11, AF25, U5, and V4.
0	11/2001	Initial version

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How to Reach Us:

Home Page:
www.freescale.com

email:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
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