Freescale Semiconductor
Technical Data

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MPC8241 Integrated Processor Hardware Specifications

The MPC8241 combines a PowerPC™ MPC603E core with a PCI bridge so that system designers can rapidly design systems using peripherals designed for PCI and other standard interfaces. Also, a high-performance memory controller supports various types of ROM and SDRAM. The MPC8241 is the second of a family of products that provide system-level support for industry-standard interfaces with an MPC603e processor core.

This hardware specification describes pertinent electrical and physical characteristics of the MPC8241, which is based on the MPC8245 design. For functional characteristics of the processor, refer to the *MPC8245 Integrated Processor Reference Manual* (MPC8245UM).

For published errata or updates to this document, visit the web site listed on the back cover of the document.

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1 Overview

The MPC8241 integrated processor is composed of a peripheral logic block and a 32-bit superscalar MPC603e core, as shown in Figure 1.

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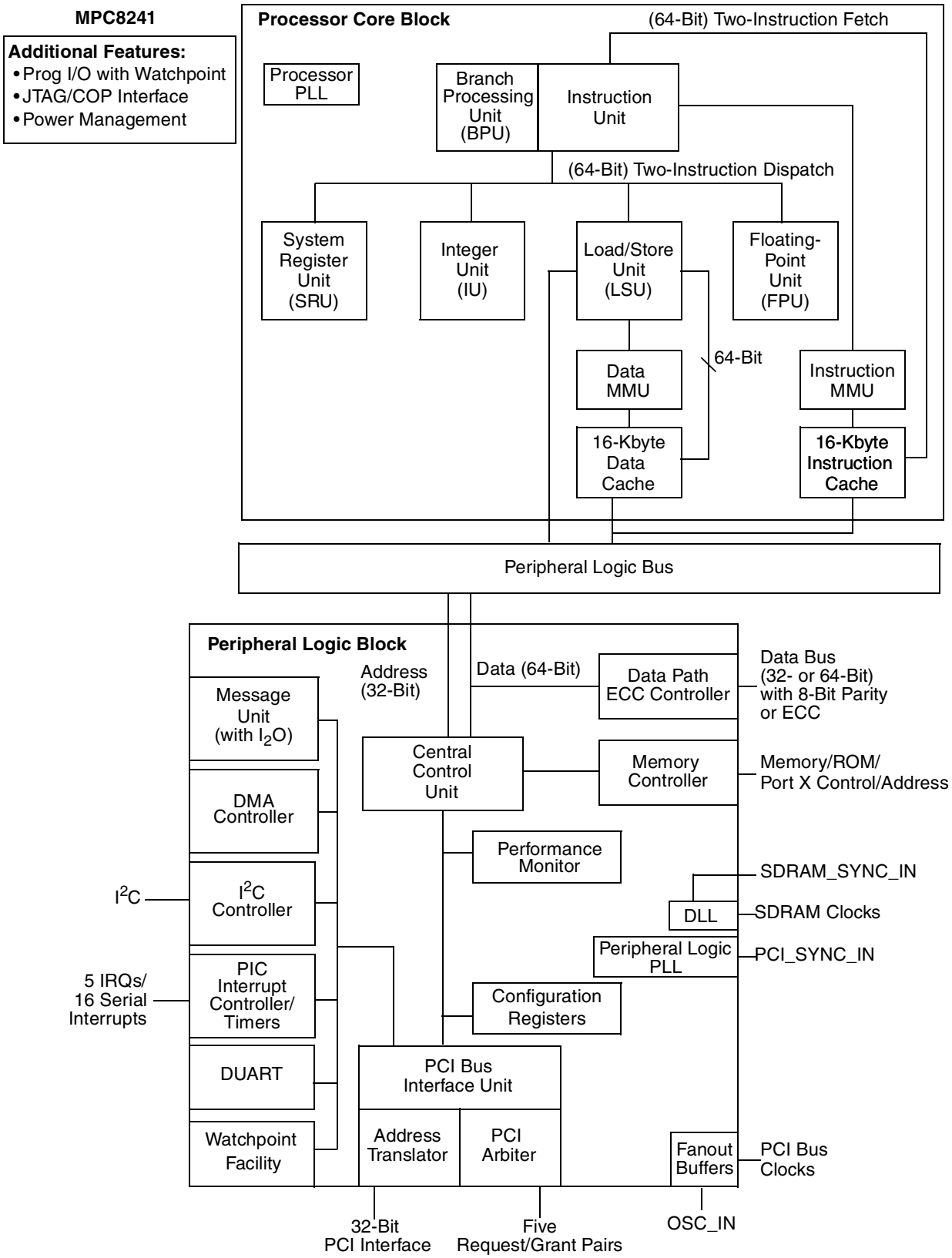


Figure 1. MPC8241 Block Diagram

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, PIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

An internal peripheral logic bus interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade performance for power consumption. The processor core is clocked from a separate PLL that is referenced to the peripheral logic PLL, allowing the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8241 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The general-purpose processor core and peripheral logic serve a variety of embedded applications. The MPC8241 can be used as either a PCI host or PCI agent controller.

2 Features

Major features of the MPC8241 are as follows:

- Processor core
  - — High-performance, superscalar processor core
  - — Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - — 16-Kbyte instruction cache
  - — 16-Kbyte data cache
  - — Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - — Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - — Peripheral logic bus
    - – Various operating frequencies and bus divider ratios
    - – 32-bit address bus, 64-bit data bus
    - – Full memory coherency
    - – Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - – Store gathering on peripheral logic bus-to-PCI writes
  - — Memory interface
    - – Up to 2 Gbytes of SDRAM memory
    - – High-bandwidth data bus (32- or 64-bit) to SDRAM
    - – Programmable timing for SDRAM
    - – One to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices

- Write buffering for PCI and processor accesses
- Normal parity, read-modify-write (RMW), or ECC
- Data-path buffering between memory interface and processor
- Low-voltage TTL logic (LVTTL) interfaces
- 272 Mbytes of base and extended ROM/Flash/PortX space
- Base ROM space for 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- Extended ROM space for 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects

— 32-bit PCI interface
- Operates up to 66 MHz
- PCI 2.2-compatible
- PCI 5.0-V tolerance
- Dual address cycle (DAC) for 64-bit PCI addressing (master only)
- PCI locked accesses to memory
- Accesses to PCI memory, I/O, and configuration spaces
- Selectable big- or little endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)
- PCI agent mode capability
- Address translation with two inbound and outbound units (ATU)
- Internal configuration registers accessible from PCI

— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- Direct mode or chaining mode (automatic linking of DMA transfers)
- Scatter gathering—read or write discontinuous memory
- 64-byte transfer queue per channel
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- Local-to-PCI memory
- PCI memory-to-local memory

— Message unit
- Two doorbell registers
- Two inbound and two outbound messaging registers
- I_2O message interface

  - I^2C controller with full master/slave support that accepts broadcast messages
  - Programmable interrupt controller (PIC)
    - Five hardware interrupts (IRQs) or 16 serial interrupts
    - Four programmable timers with cascade
  - Two (dual) universal asynchronous receiver/transmitters (UARTs)
  - Integrated PCI bus and SDRAM clock generation
  - Programmable PCI bus and memory interface output drivers
- System level performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal—marks valid address and data bus cycles on the memory bus
  - Programmable input and output signals with watchpoint capability
  - Error injection/capture on data path
  - IEEE Std. 1149.1 (JTAG)/test interface

3 General Parameters

The following list summarizes the general parameters of the MPC8241:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 357 (thick substrate and thick mold cap) plastic ball grid array (PBGA)
Core power supply	1.8 V ± 100 mV DC (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8241.

4.1 DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

4.1.1 Absolute Maximum Ratings

This section describes the MPC8241 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.1	V
Supply voltage—memory bus drivers, PCI and standard I/O buffers	$GV_{DD_}OV_{DD}$	–0.3 to 3.6	V
Supply voltage—PLLs	$AV_{DD}/AV_{DD}2$	–0.3 to 2.1	V
Supply voltage—PCI reference	LV_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	•C
Storage temperature range	T_{stg}	–55 to 150	•C

Notes:
1. Table 2 provides functional and tested operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8241.

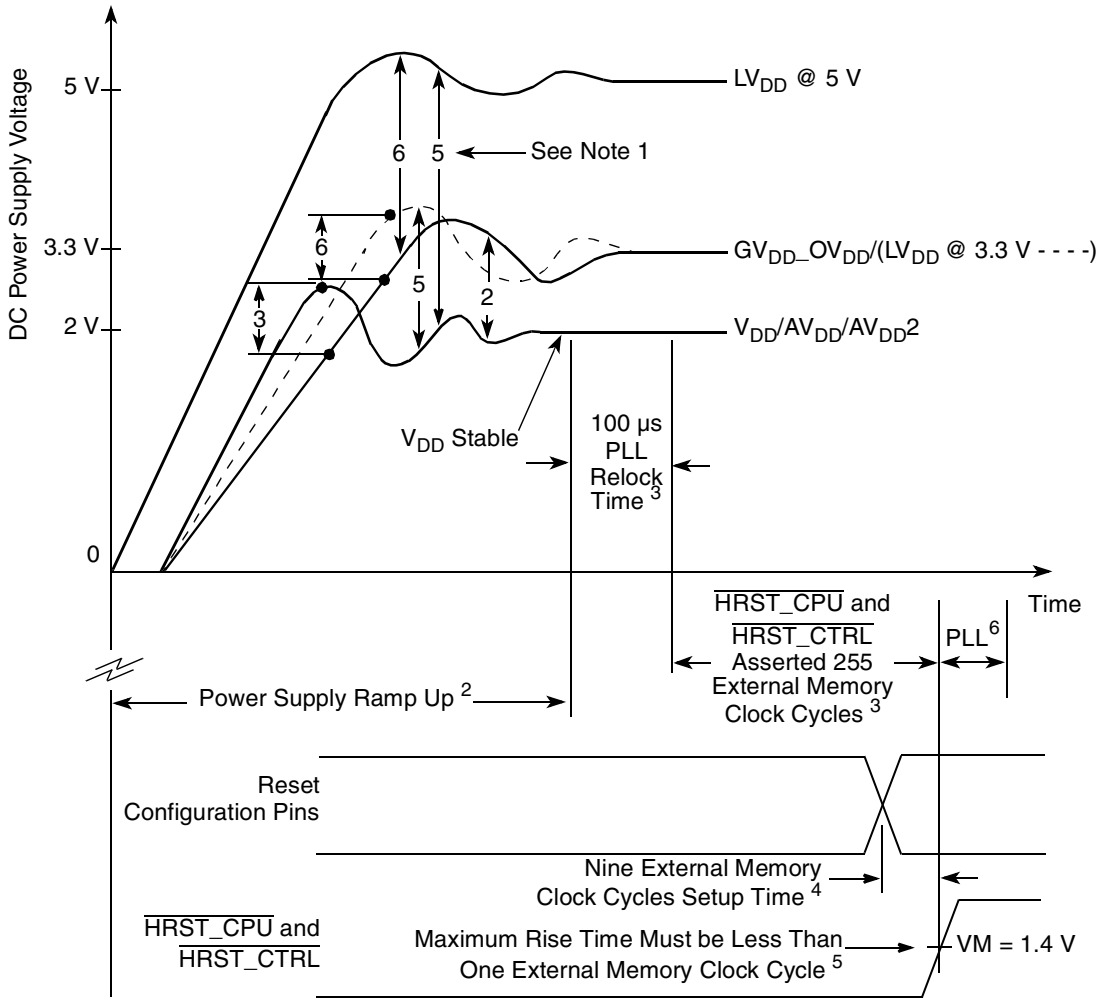
Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	1.8 ± 100 mV	V	2
I/O buffer supply for PCI and standard; supply voltages for memory bus drivers		$GV_{DD}_OV_{DD}$	3.3 ± 0.3	V	2
CPU PLL supply voltage		AV_{DD}	1.8 ± 100 mV		2
PLL supply voltage—peripheral logic		$AV_{DD}2$	1.8 ± 100 mV	V	2
PCI reference		LV_{DD}	5.0 ± 5%	V	4, 5, 6
			3.3 ± 0.3	V	5, 6, 7
Input voltage	PCI inputs	V_{in}	0 to 3.6 or 5.75	V	4, 7
	All other inputs		0 to 3.6	V	8
Die-junction temperature		T_j	0 to 105	•C	

Notes:

1. Freescale has tested these operating conditions and recommends them. Proper device operation outside of these conditions is not guaranteed.
2. **Caution:** $GV_{DD}_OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 1.8 V at any time including during power-on reset. Note that $GV_{DD}_OV_{DD}$ pins are all shorted together: This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences. Connections should not be made to individual PWRRING pins.
3. **Caution:** $V_{DD}/AV_{DD}/AV_{DD}2$ must not exceed $GV_{DD}_OV_{DD}$ by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 5.0 V DC power supply.
5. **Caution:** LV_{DD} must not exceed $V_{DD}/AV_{DD}/AV_{DD}2$ by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** LV_{DD} must not exceed $GV_{DD}_OV_{DD}$ by more than 3.0 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. PCI pins are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3 V DC power supply.
8. **Caution:** Input voltage (V_{in}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/AV_{DD}2$) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{in}) must not be greater than $GV_{DD}_OV_{DD}$ by more than 0.6 V at all times including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. See the Cautions section of Table 2 for details on this topic.
3. Refer to Table 8 for details on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 10 for details on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.
6. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST_CTRL}}$ and $\overline{\text{HRST_CPU}}$ negate in order to be latched.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface.

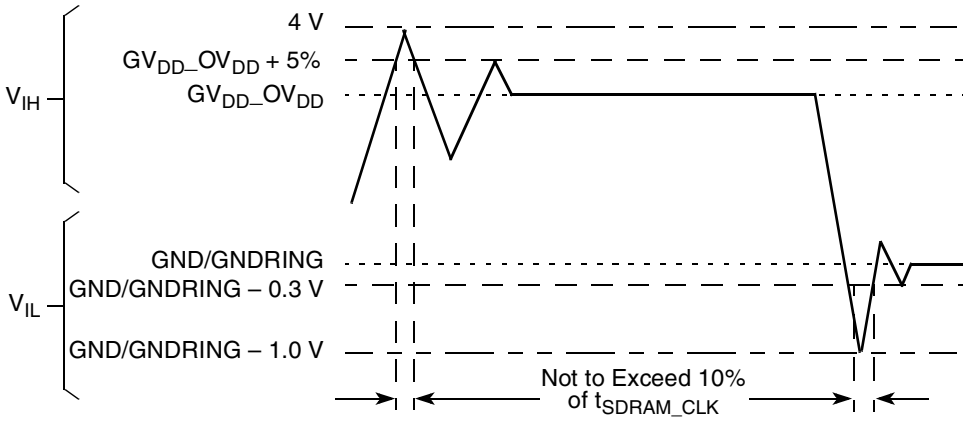


Figure 3. Overshoot/Undershoot Voltage

Figure 4 and Figure 5 show the undershoot and overshoot voltage of the PCI interface for the 3.3- and 5-V signals, respectively.

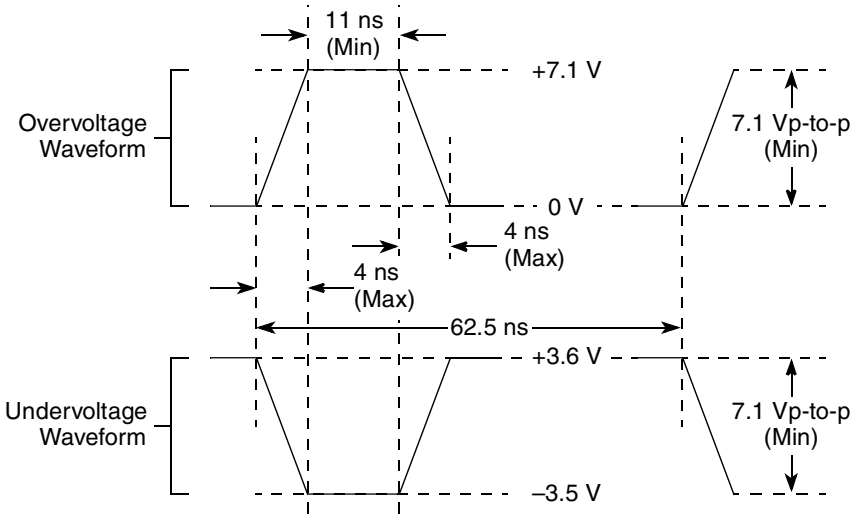


Figure 4. Maximum AC Waveforms for 3.3-V Signaling

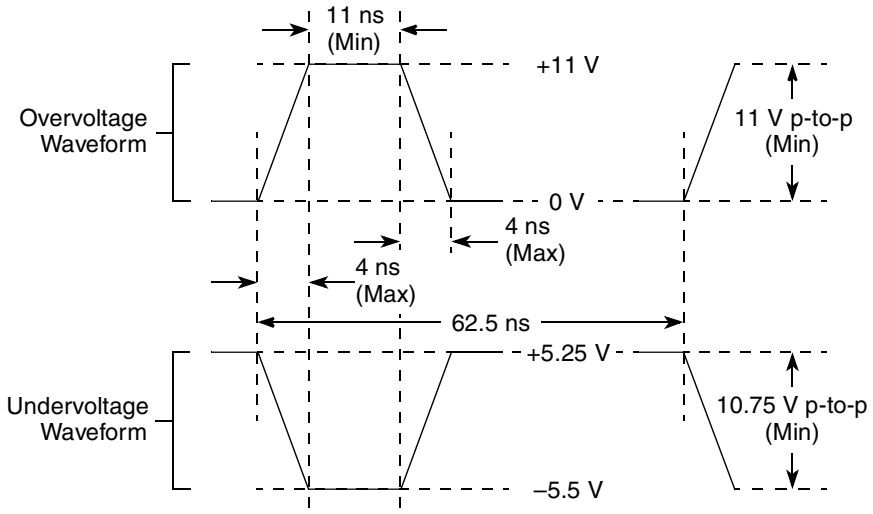


Figure 5. Maximum AC Waveforms for 5-V Signaling

4.2 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8241 at recommended operating conditions.

Table 3. DC Electrical Specifications

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Input high voltage	PCI only, except PCI_SYNC_IN	V_{IH}	$0.65 \times GV_{DD}_OV_{DD}$	LV_{DD}	V	1
Input low voltage	PCI only, except PCI_SYNC_IN	V_{IL}	—	$0.3 \times GV_{DD}_OV_{DD}$	V	
Input high voltage	All other pins, including PCI_SYNC_IN ($GV_{DD}_OV_{DD}$ = 3.3 V)	V_{IH}	2.0	3.3	V	
Input low voltage	All inputs, including PCI_SYNC_IN	V_{IL}	GND/GNDRING	0.8	V	2
Input leakage current for pins using DRV_PCI driver	$0.5\ V \le V_{in} \le 2.7$ V @ LV_{DD} = 4.75 V	I_L	—	±70	μA	3
Input leakage current all others	LV_{DD} = 3.6 V $GV_{DD}_OV_{DD} \le 3.465$ V	I_L	—	±10	μA	3
Output high voltage	I_{OH} = driver dependent ($GV_{DD}_OV_{DD}$ = 3.3 V)	V_{OH}	2.4	—	V	4
Output low voltage	I_{OL} = driver dependent ($GV_{DD}_OV_{DD}$ = 3.3 V)	V_{OL}	—	0.4	V	4

Table 3. DC Electrical Specifications (continued)

Characteristics	Conditions	Symbol	Min	Max	Unit	Notes
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	16.0	pF	

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. All grounded pins are connected together.
3. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} or both GV_{DD}_OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
4. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.

4.2.1 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8241 Output Pins [5, 6]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20 (default)	GV_{DD}_OV_{DD} = 3.3 V	36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)		89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) where table entry voltage = GV_{DD}_OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD}_ OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GV_{DD}_OV_{DD} – V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1 × GV_{DD}_OV_{DD} (GV_{DD}_OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.
4. For all others with GV_{DD}_OV_{DD} = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4-V table entry.
5. See driver bit details for output driver control register (0x73) in the *MPC8245 Integrated Processor Reference Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*.

4.3 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8241.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	33/66/133	33/66/166	33/66/200	33/100/200	66/100/200	66/66/ 266	66/133/ 266		
Typical	0.7	0.8	1.0	1.0	1.0	1.5	1.8	W	1, 5
Max—CFP	0.8	1.0	1.2	1.3	1.3	1.9	2.1	W	1, 2
Max—INT	0.8	0.9	1.0	1.2	1.2	1.6	1.8	W	1, 3
Doze	0.5	0.6	0.7	0.8	0.8	1.0	1.3	W	1, 4, 6
Nap	0.2	0.2	0.3	0.4	0.4	0.4	0.7	W	1, 4, 6
Sleep	0.2	0.2	0.2	0.2	0.3	0.2	0.4	W	1, 4, 6
I/O Power Supplies [7]									
Mode	**Minimum**				**Maximum**			**Unit**	**Notes**
GV_{DD}_OV_{DD}	500				1130			mW	8

Notes:

1. The values include V_{DD}, AV_{DD}, and $AV_{DD}2$ but do not include I/O supply power.
2. Maximum—FP power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 1.9 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 1.9 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 1.8 V, GV_{DD}_OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. Power consumption of PLL supply pins (AV_{DD} and $AV_{DD}2$) < 15 mW, guaranteed by design, but not tested.
8. The typical maximum GV_{DD}_OV_{DD} value resulted from the MPC8241 operating at the fastest frequency combination of 66:133:266 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory and on 64-bit boundaries to local memory.

4.4 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8241. For details, see Section 7.7, "Thermal Management."

Table 6. Thermal Characterization Data

Rating	Thermal Test Board Description	Symbol	Value [7] (166- and 200-MHz Parts)	Value [7] (266-MHz Part)	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	38	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JMA}$	25	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	31	22	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	22	17	°C/W	1, 3
Junction-to-board (bottom)	Four-layer board (2s2p)	$R_{\theta JB}$	17	11	°C/W	4
Junction-to-case (top)	Single-layer board (1s)	$R_{\theta JC}$	8	7	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	2	2	°C/W	6

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the board horizontal.
3. Per EIA/JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per EIA/JESD51-2.
7. Note that the 166- and 200-MHz parts are in a two-layer package and the 266-MHz part is in a four-layer package, which causes the two package types to have different thermal characterization data.

4.5 AC Electrical Characteristics

After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 8, "Ordering Information."

Table 7 provides the operating frequency information for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V.

Table 7. Operating Frequency

Characteristic	166 MHz		200 MHz		266 MHz		Unit
	$V_{DD}/AV_{DD}/AV_{DD}2$ = 1.8 ± 100 mV						
	Min	Max	Min	Max	Min	Max	
Processor frequency (CPU)	100	166	100	200	100	266	MHz
Memory bus frequency	33	83	33	100	33	133	MHz
PCI input frequency	25–66						MHz

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

4.5.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 4.5.2, "Input AC Timing Specifications." These specifications are for the default driver strengths indicated in Table 4. Figure 6 shows the PCI_SYNC_IN input clock timing diagram with the labeled number items listed in Table 8.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	1
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN jitter	—	200	ps	
8a	PCI_CLK[0:4] skew (pin-to-pin)	—	250	ps	
8b	SDRAM_CLK[0:3] skew (pin-to-pin)	—	190	ps	3
10	Internal PLL relock time	—	100	µs	2, 4, 5
15	DLL lock range with DLL_EXTEND = 0 (disabled) and normal tap delay; (default DLL mode)	See Figure 7		ns	6
16	DLL lock range for other modes	See Figure 8 through Figure 10		ns	6
17	Frequency of operation (OSC_IN)	25	66	MHz	
19	OSC_IN rise and fall times	—	5	ns	7
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	

Table 8. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
21	OSC_IN frequency stability	—	100	ppm	

Notes:

1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 through 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. *N* is a non-zero integer (see Figure 7 through Figure 10). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. For details about how Figure 7 through Figure 10 may be used, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines,* for details on MPC8241 memory clock design.
7. Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Figure 6 shows the PCI_SYNC_IN input clock timing diagram, and Figure 7 through Figure 10 show the DLL locking range loop delay versus frequency of operation.

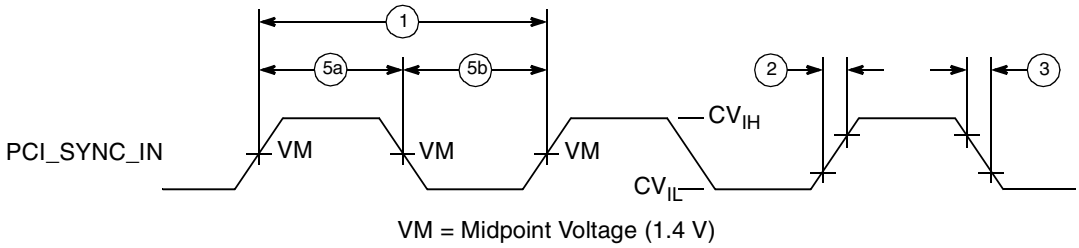


Figure 6. PCI_SYNC_IN Input Clock Timing Diagram

Register settings that define each DLL mode are shown in Table 9.

Table 9. DLL Mode Definition

DLL Mode	Bit 2 of Configuration Register at 0x76	Bit 7 of Configuration Register at 0x72
Normal tap delay, No DLL extend	0	0
Normal tap delay, DLL extend	0	1
Max tap delay, No DLL extend	1	0
Max tap delay, DLL extend	1	1

The DLL_MAX_DELAY bit can lengthen the amount of time through the delay line by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock is within the DLL lock range, there may be slightly more jitter in the output clock of the DLL if the phase comparator shifts the clock between adjacent tap points. Refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1*, for details on DLL modes and memory design.

The value of the current tap point after the DLL locks can be determined by reading bits 6–0 (DLL_TAP_COUNT) of the DLL tap count register (DTCR, located at offset 0xE3). These bits store the value (binary 0 through 127) of the current tap point and can indicate whether the DLL advances or decrements as it maintains the DLL lock. Therefore, for evaluation purposes, DTCR can be read for all DLL modes that support the T_{loop} value used for the trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN. The DLL mode with the smallest tap point value in the DTCR should be used because the bigger the tap point value, the more jitter that can be expected for clock signals. Keeping a DLL mode locked below tap point decimal 12 is not recommended.

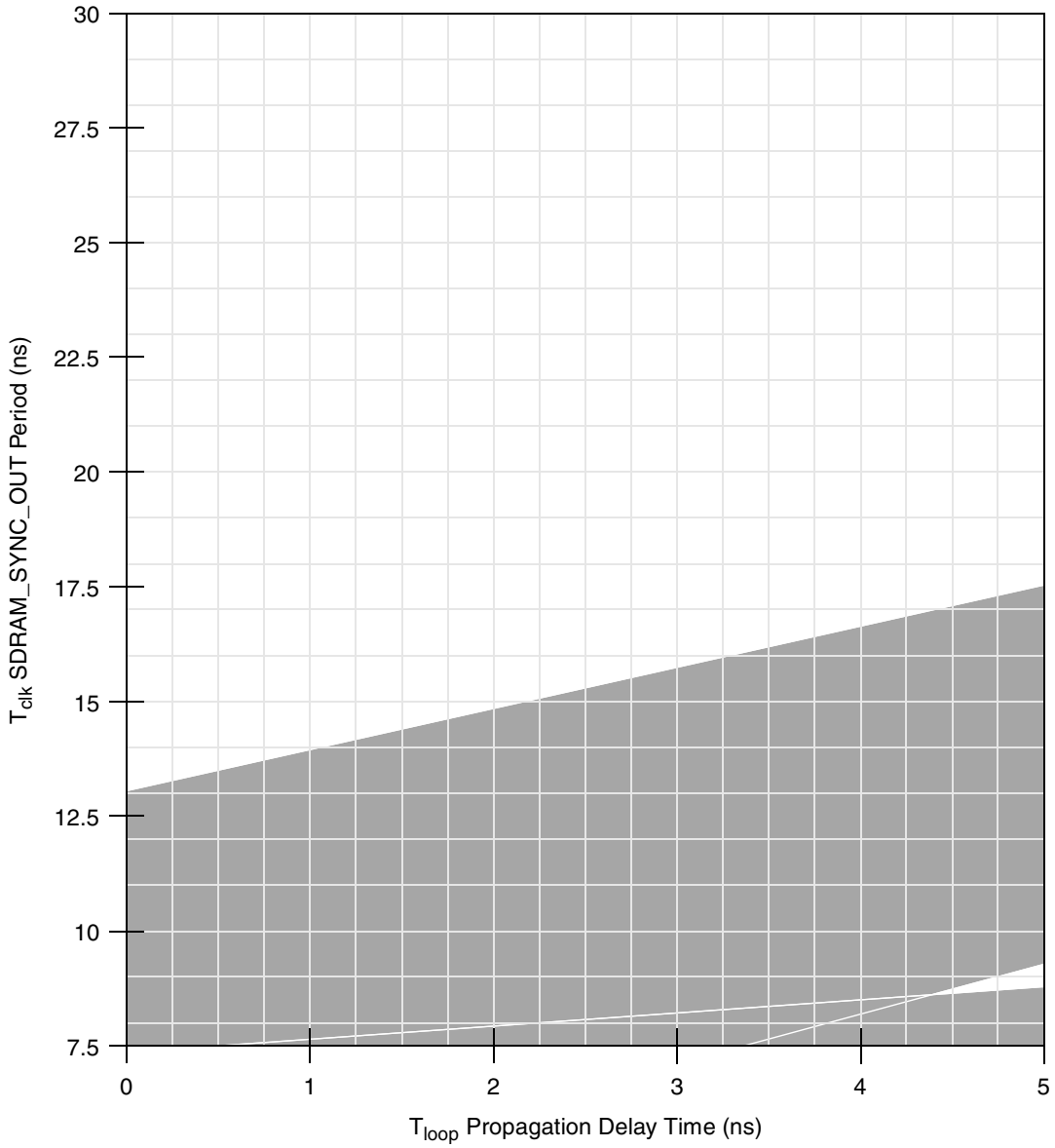


Figure 7. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Normal Tap Delay

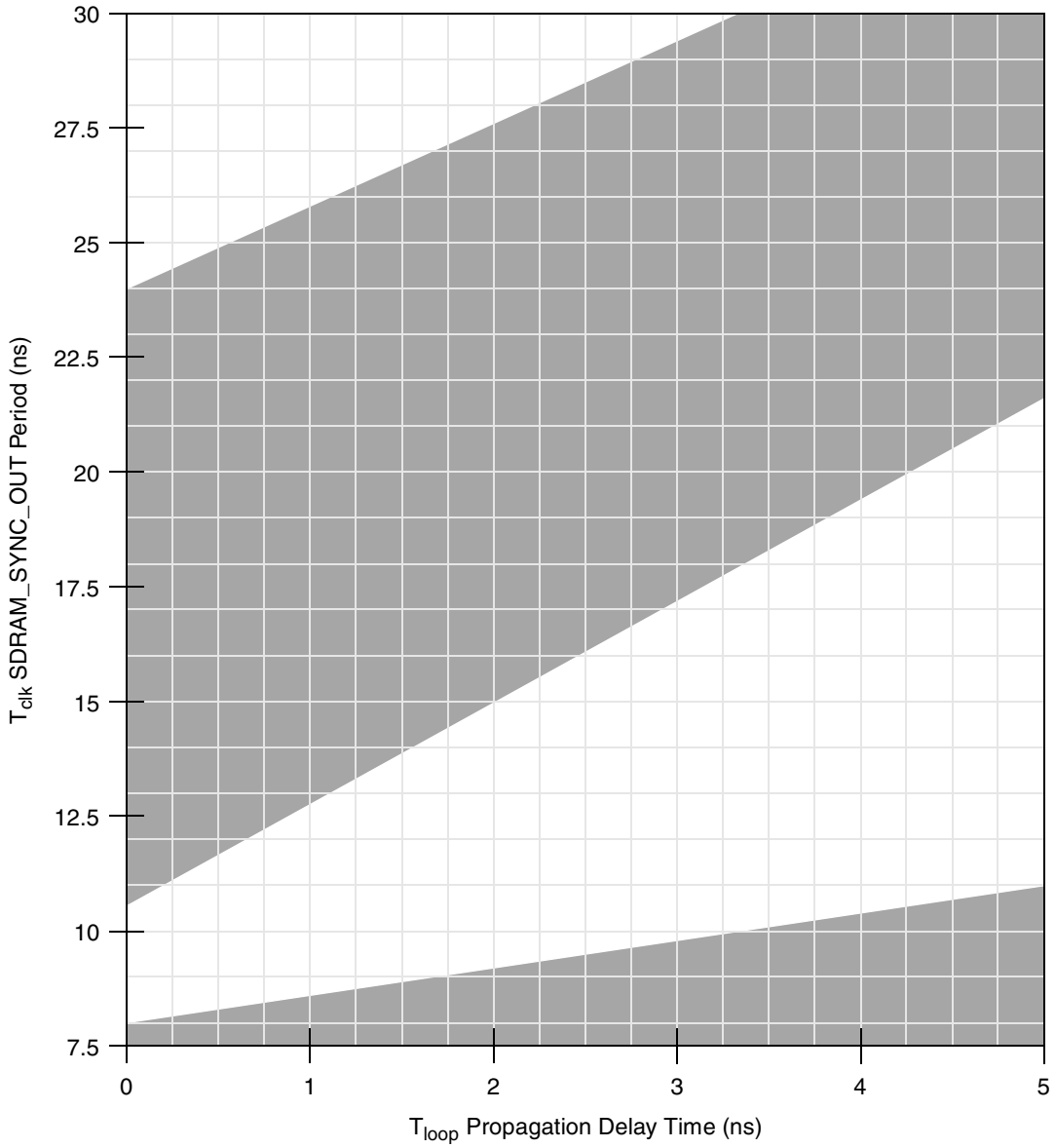


Figure 8. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Normal Tap Delay

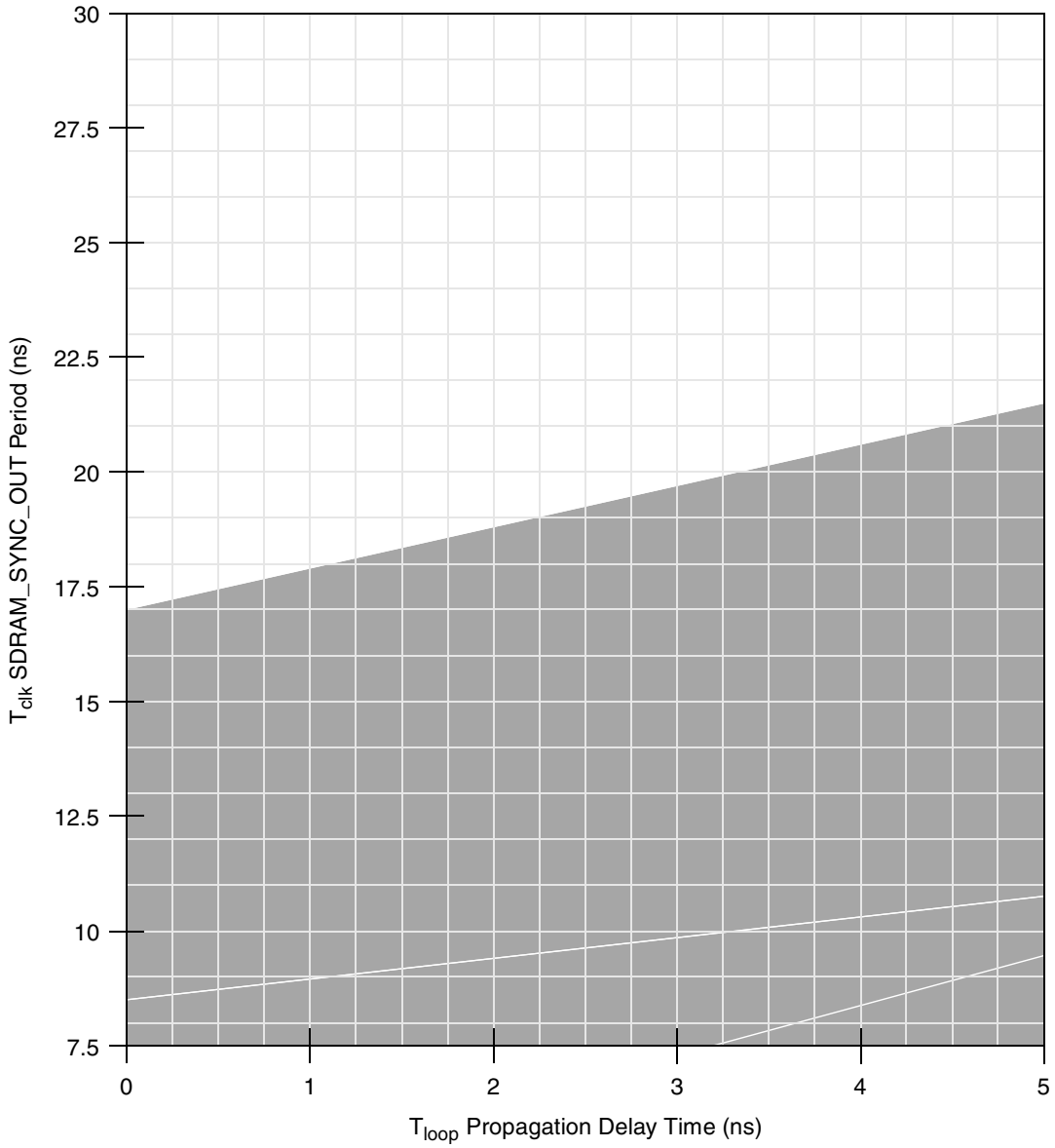


Figure 9. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=0 and Max Tap Delay

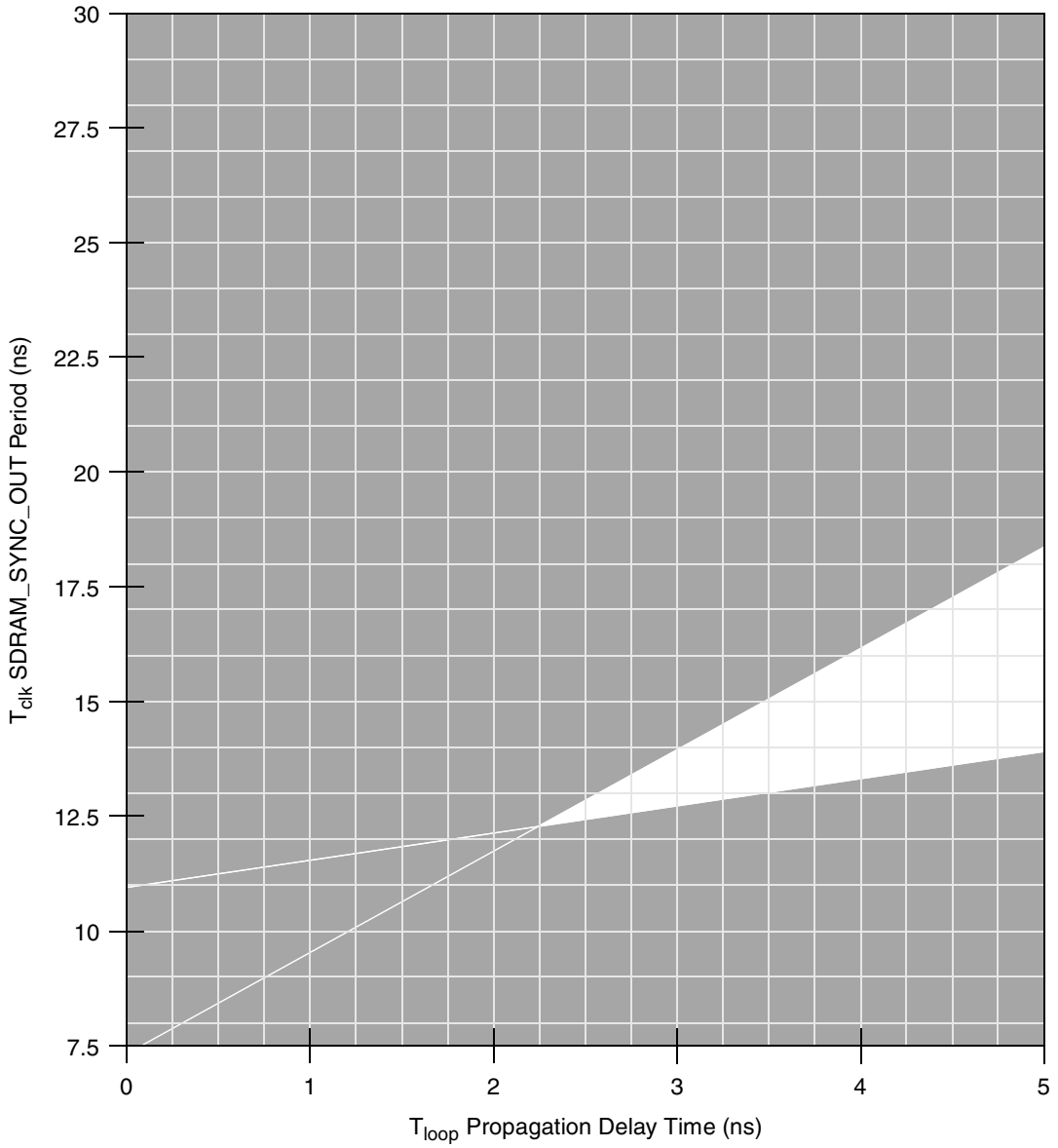


Figure 10. DLL Locking Range Loop Delay versus Frequency of Operation for DLL_Extend=1 and Max Tap Delay

4.5.2 Input AC Timing Specifications

Table 10 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. See Figure 11 and Figure 12.

Table 10. Input AC Timing Specifications

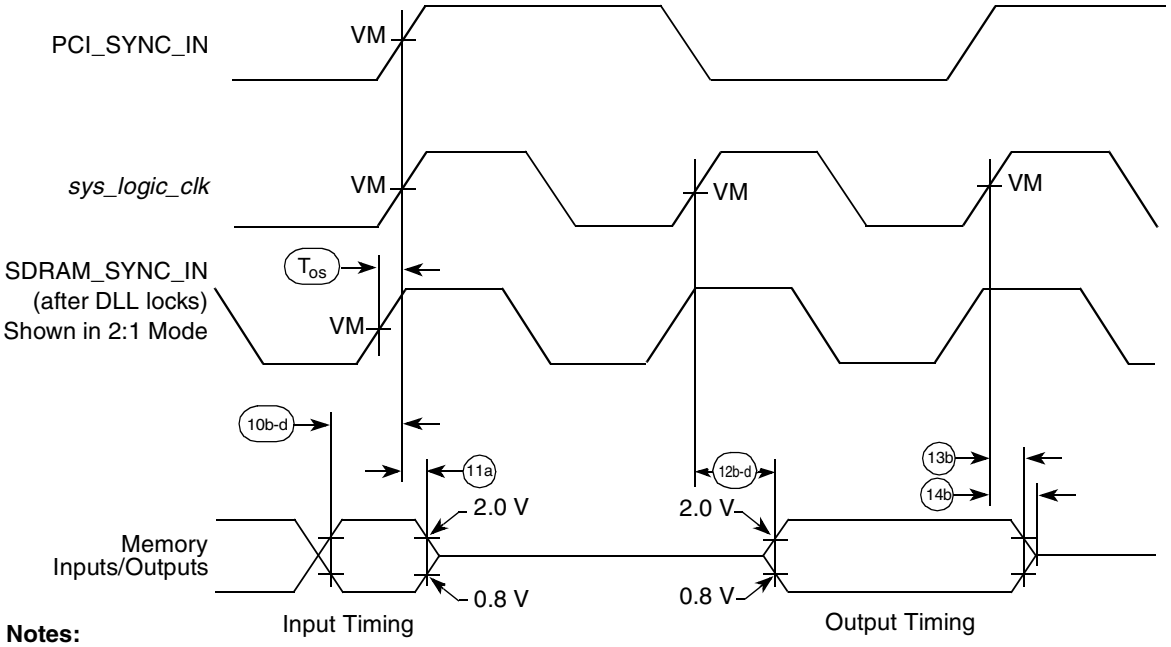
Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b	Memory input signals valid to *sys_logic_clk* (input setup)				

Table 10. Input AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
10b0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	2.6	—	ns	2, 3, 6
10b1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	1.9	—		
10b2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.2	—		
10b3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	0.5	—		
10c	PIC miscellaneous debug input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10d	I^2C input signals valid to *sys_logic_clk* (input setup)	3.0	—	ns	2, 3
10e	Mode select inputs valid to $\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.4	1.0	ns	7
11a	*sys_logic_clk* to memory signal inputs invalid (input hold)				
11a0	Tap 0, register offset <0x77>, bits 5:4 = 0b00	0	—	ns	2, 3, 6
11a1	Tap 1, register offset <0x77>, bits 5:4 = 0b01	0.7	—		
11a2	Tap 2, register offset <0x77>, bits 5:4 = 0b10 (default)	1.4	—		
11a3	Tap 3, register offset <0x77>, bits 5:4 = 0b11	2.1	—		
11b	$\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to inputs invalid (input hold)	1.0	—	ns	1, 2, 3

Notes:

1. All PCI signals are measured from $GV_{DD}_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times GV_{DD}_OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 12.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock. *sys_logic_clk*. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ signal. See Figure 13.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened to accommodate this range relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*. It is recommended that the length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN be shortened by 0.7 ns because that is the midpoint of the range of T_{os} and allows the impact from the range of T_{os} to be reduced. Additional analyses of trace lengths and SDRAM loading must be performed to optimize timing. For details on trace measurements and the T_{os} problem, refer to the Freescale application note AN2164, *MPC8245/MPC8241 Memory Clock Design Guidelines*.



Notes:
VM = Midpoint voltage (1.4 V).
10b-d = Input signals valid timing.
11a = Input hold time of SDRAM_SYNC_IN to memory.
12b-d = *sys_logic_clk* to output valid timing.
13b = Output hold time for non-PCI signals.
14b = SDRAM-SYNC_IN to output high-impedance timing for non-PCI signals.
T_{os} = Offset timing required to align *sys_logic_clk* with SDRAM_SYNC_IN. The SDRAM_SYNC_IN signal is adjusted by the DLL to accommodate for internal delay. This causes SDRAM_SYNC_IN to appear before *sys_logic_clk* once the DLL locks.

Figure 11. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN

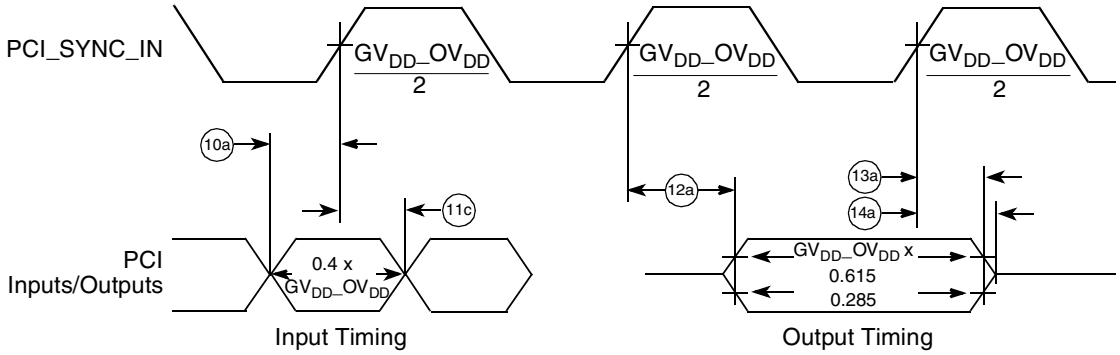


Figure 12. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 13 shows the input timing diagram for mode select signals.

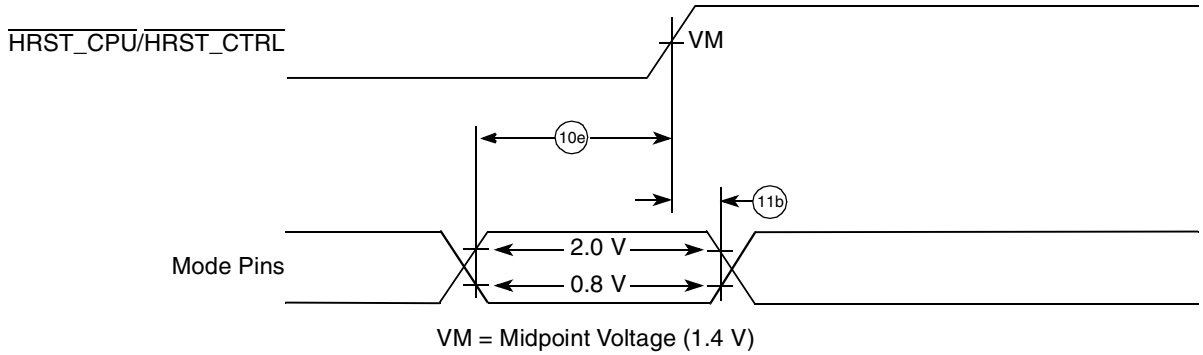


Figure 13. Input Timing Diagram for Mode Select Signals

4.5.3 Output AC Timing Specification

Table 11 provides the processor bus AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V (see Figure 11). All output timings assume a purely resistive 50-Ω load (see Figure 14). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths that Table 4 indicates.

Table 11. Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, see Figure 15				
12a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	—	7.5		
12b	*sys_logic_clk* to output valid (memory address, control, and data signals)	—	4.5	ns	2
12c	*sys_logic_clk* to output valid (for all others)	—	7.0	ns	2
12d	*sys_logic_clk* to output valid (for I^2C)	—	5.0	ns	2
12e	*sys_logic_clk* to output valid (ROM/Flash/Port X)	—	6.0	ns	2
13a	Output hold (PCI), see Figure 15				
13a0	Tap 0, PCI_HOLD_DEL = 00, [$\overline{\text{MCP}}$,CKE] = 11, 66 MHz PCI (default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL = 01, [$\overline{\text{MCP}}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL = 10, [$\overline{\text{MCP}}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL = 11, [$\overline{\text{MCP}}$,CKE] = 00	3.5	—		
13b	Output hold (all others)	1.0	—	ns	2
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	1, 3

Table 11. Output AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Unit	Notes
14b	*sys_logic_clk* to output high impedance (for all others)	—	4.0	ns	2

Notes:

1. All PCI signals are measured from $GV_{DD}_OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times GV_{DD}_OV_{DD}$ or $0.615 \times GV_{DD}_OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 12.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, *sys_logic_clk* to the TTL level (0.8 or 2.0 V) of the signal in question. *sys_logic_clk* is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 11.
3. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[3:0], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[31:0], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
4. To meet minimum output hold specifications relative to PCI_SYNC_IN for both 33- and 66-MHz PCI systems, the MPC8241 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals; the values on these two signals are inverted and subsequently stored as the initial settings of PCI_HOLD_DEL = PMCR2[5, 4] (power management configuration register 2 <0x72>), respectively. Because $\overline{\text{MCP}}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Additional output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 15 for PCI_HOLD_DEL effect on output valid and hold time.

Figure 14 provides the AC test load for the MPC8241.

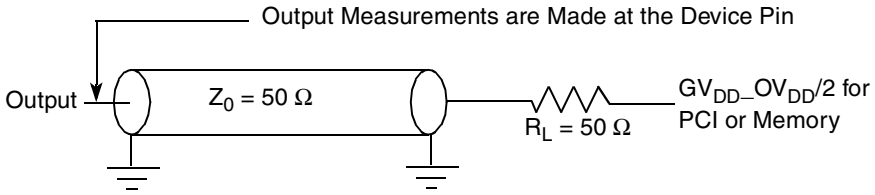
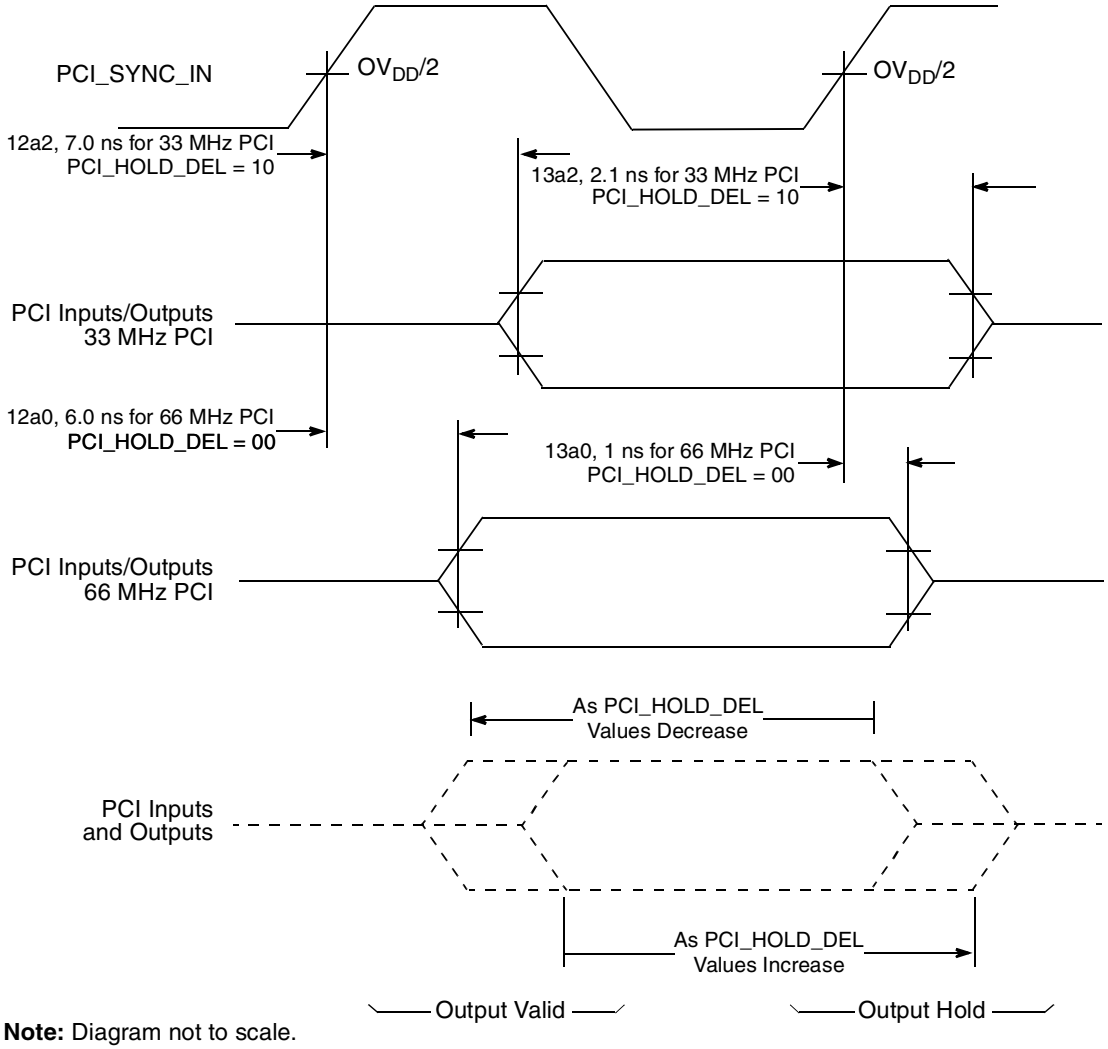


Figure 14. AC Test Load for the MPC8241



Note: Diagram not to scale.

Figure 15. PCI_HOLD_DEL Effect on Output Valid and Hold Time

4.6 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8241.

4.6.1 I²C DC Electrical Characteristics

Table 12 provides the DC electrical characteristics for the I²C interfaces.

Table 12. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1

Table 12. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8245 Integrated Processor Reference Manual* for information on the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if the OV_{DD} is switched off.

4.6.2 I^2C AC Electrical Specifications

Table 13 provides the AC timing parameters for the I^2C interfaces.

Table 13. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	µs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	µs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	µs
Data output delay time:	t_{I2OVKL}	—	0.9[3]	
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

Table 13. I^2C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 12).

Parameter	Symbol [1]	Min	Max	Unit
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8245 provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid the unintended generation of a Start or Stop condition. When the MPC8245 acts as the I^2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA is balanced, the MPC8245 does not cause an unintended generation of a Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8245 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I^2C SCL clock frequency and SDA output delay time are achieved. It is assumed that the desired I^2C SCL clock frequency is 400 KHz and the digital filter sampling rate register (DFFSR bits in I2CFDR) is programmed with its default setting of 0x10 (decimal 16):

SDRAM Clock Frequency	100 MHz	133 MHz
FDR Bit Setting	0x00	0x2A
Actual FDR Divider Selected	384	896
Actual I^2C SCL Frequency Generated	260.4 KHz	148.4 KHz

   For details on I^2C frequency calculation, refer to the application note AN2919 “Determining the I^2C Frequency Divider Ratio for SCL”.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design

Figure 16 provides the AC test load for the I^2C.

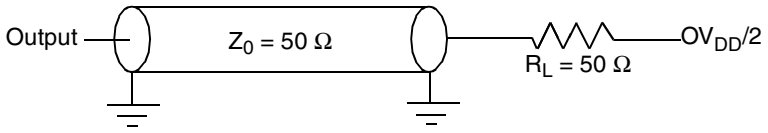


Figure 16. I^2C AC Test Load

Figure 17 shows the AC timing diagram for the I^2C bus.

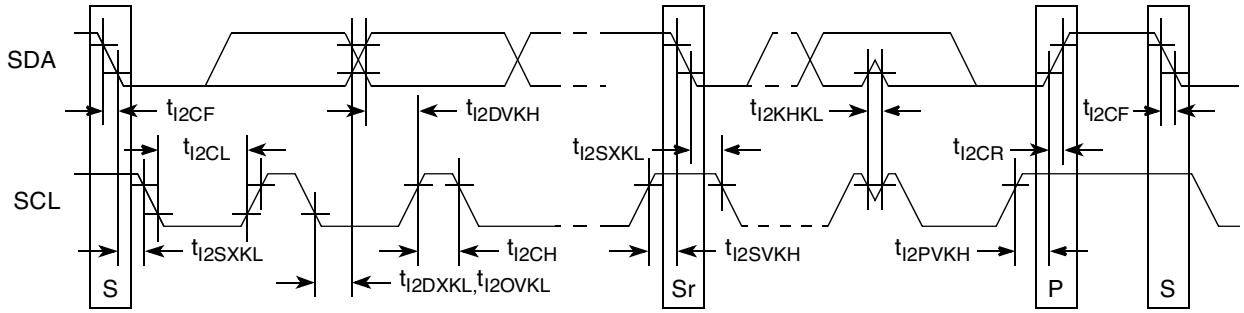


Figure 17. I^2C Bus AC Timing Diagram

4.7 PIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the PIC serial interrupt mode AC timing specifications for the MPC8241 at recommended operating conditions (see Table 2) with GV_{DD}–OV_{DD} = 3.3 V ± 5% and LV_{DD} = 3.3 V ± 0.3 V.

Table 14. PIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	—
3	S_CLK output valid time	—	6	ns	—
4	Output hold time	0	—	ns	—
5	$\overline{\text{S_FRAME}}$, S_RST output valid time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT input setup time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor Reference Manual* for a description of the PIC interrupt control register (ICR) and S_CLK frequency programming.
2. S_RST, $\overline{\text{S_FRAME}}$, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S_FRAME}}$, and S_INT. The *MPC8245 Integrated Processor Reference Manual* describes the functional relationships between these signals.
3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor Reference Manual* for a complete clocking description.

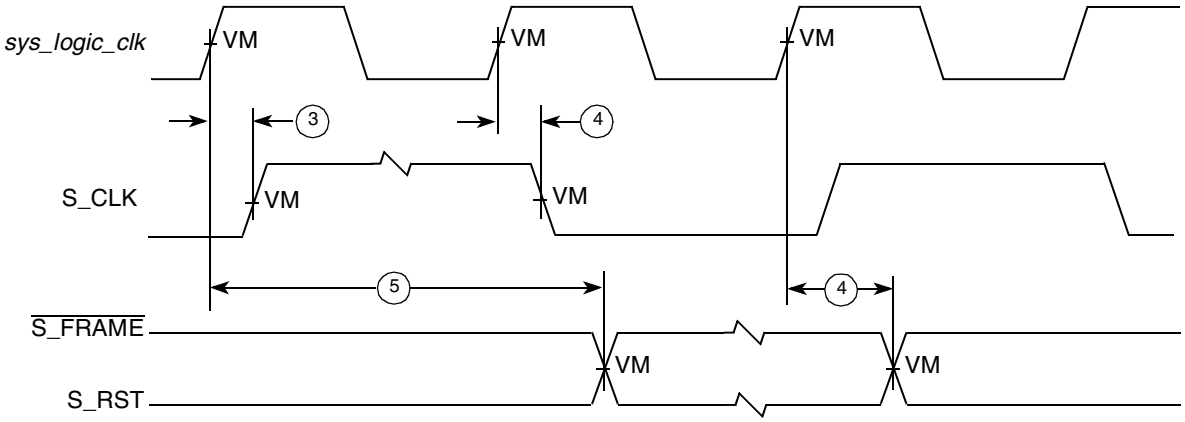


Figure 18. PIC Serial Interrupt Mode Output Timing Diagram

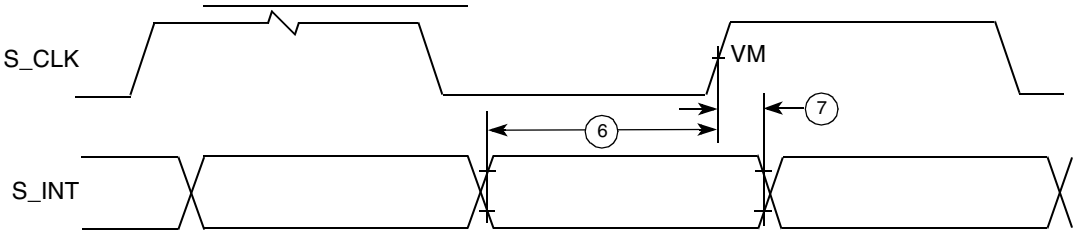


Figure 19. PIC Serial Interrupt Mode Input Timing Diagram

4.7.1 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8241 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	—
1	TCK cycle time	40	—	ns	—
2	TCK clock pulse width measured at 1.5 V	20	—	ns	—
3	TCK rise and fall times	0	3	ns	—
4	$\overline{\text{TRST}}$ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$ assert time	10	—	ns	—
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	—

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

Num	Characteristic	Min	Max	Unit	Notes
11	TMS, TDI data hold time	15	—	ns	—
12	TCK to TDO data valid	0	15	ns	—
13	TCK to TDO high impedance	0	15	ns	—

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

Figure 20 through Figure 23 show the different timing diagrams for JTAG.

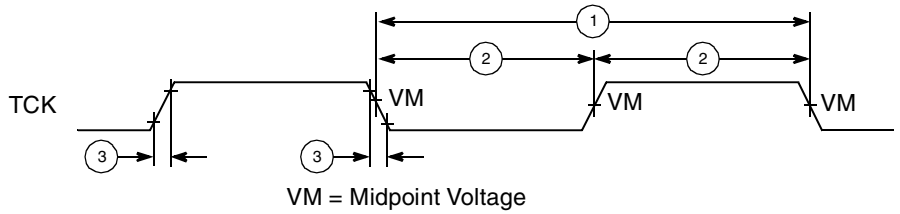


Figure 20. JTAG Clock Input Timing Diagram

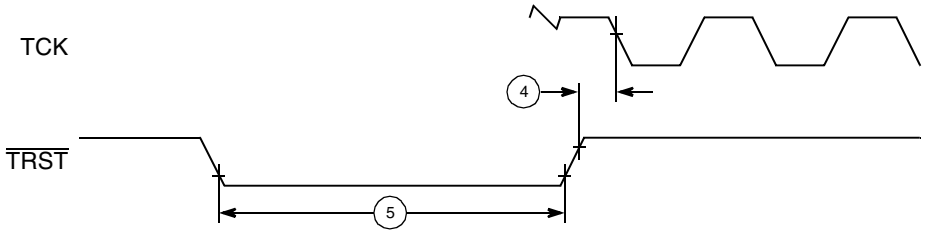


Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram

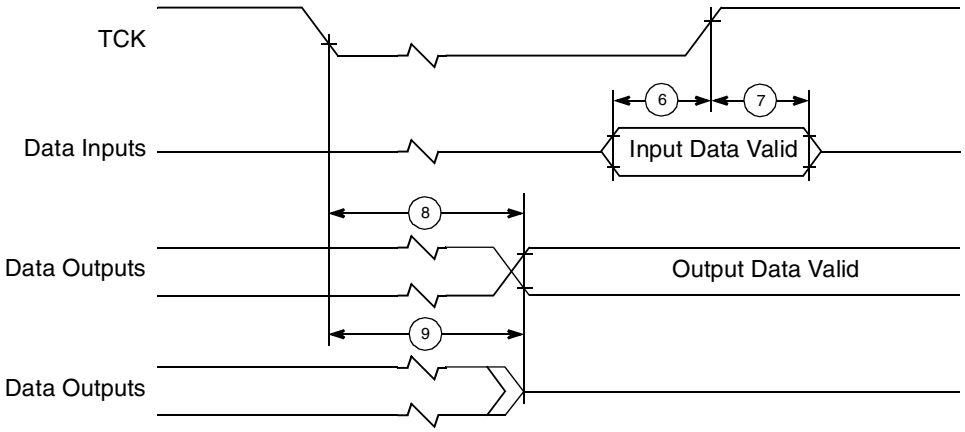


Figure 22. JTAG Boundary Scan Timing Diagram

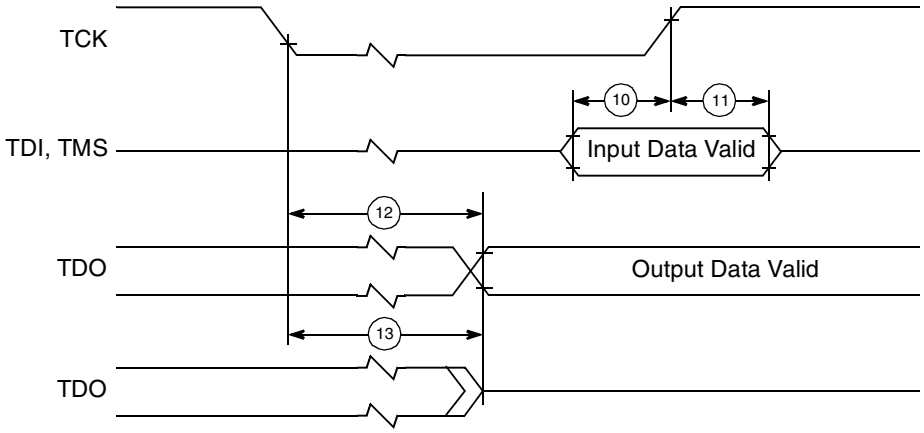


Figure 23. Test Access Port Timing Diagram

5 Package Description

This section details package parameters, pin assignments, and dimensions.

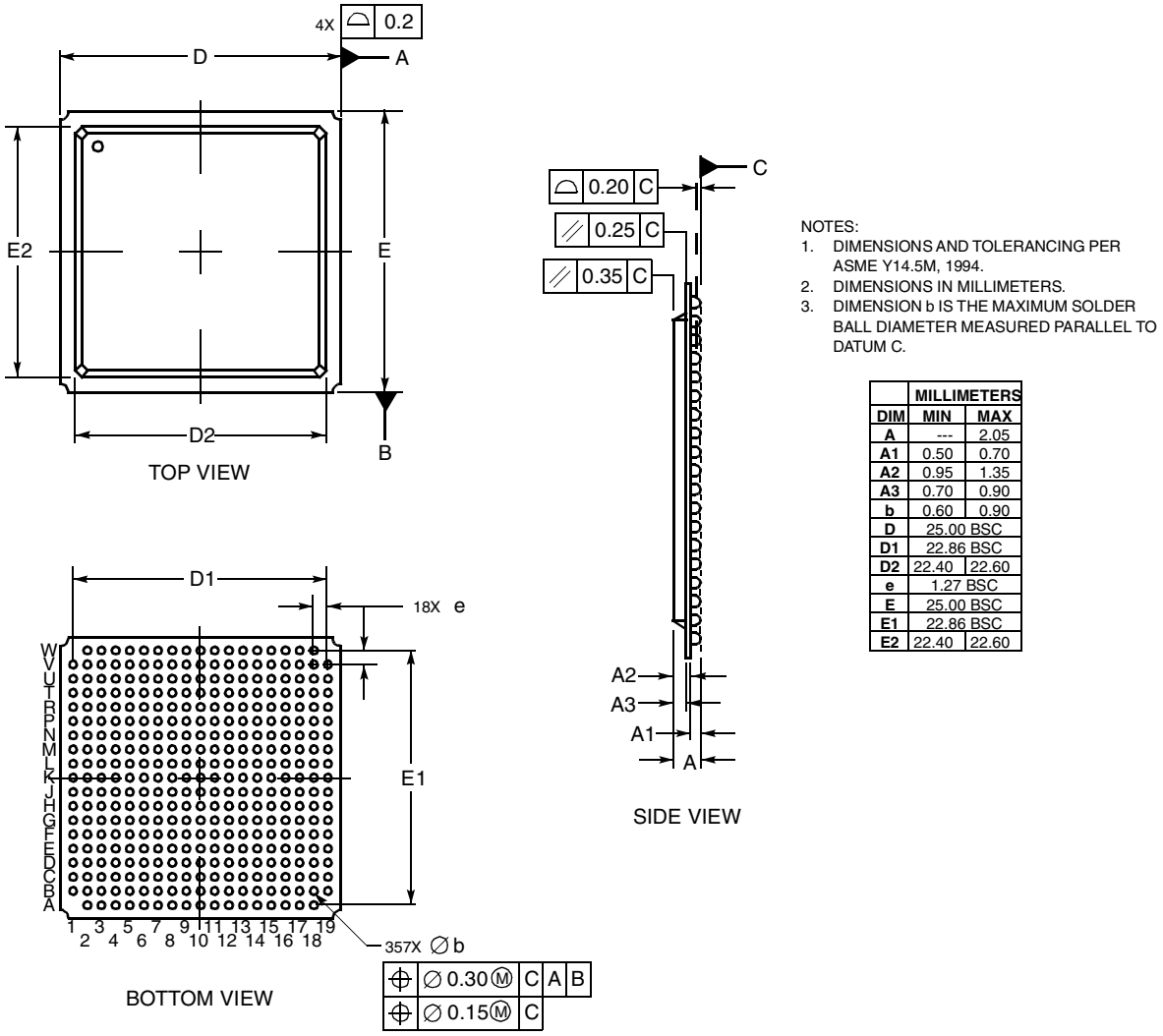
5.1 Package Parameters for the MPC8241

The MPC8241 uses a 25 mm × 25 mm, cavity up, 357-pin plastic ball grid array (PBGA) package. The package parameters are as follows.

Package outline	25 mm × 25 mm
Interconnects	357
Pitch	1.27 mm
Solder balls	ZP (PBGA)—62 Sn/36 Pb/2 Ag—available only in Rev B parts ZQ (Thick substrate thick mold cap PBGA)—62 Sn/36 Pb/2 Ag VR (Lead free version of package)—95.5 Sn/4.0 Ag/0.5 Cu
Solder ball diameter	0.75 mm
Maximum module height	2.52 mm
Co-planarity specification	0.15 mm
Maximum force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZP package. Note that this is available for Rev. B parts only.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Figure 24. MPC8241 Package Dimensions and Pinout Assignments (ZP Package)

Figure 25 shows the top surface, side profile, and pinout of the MPC8241, 357 PBGA ZQ and VR packages.

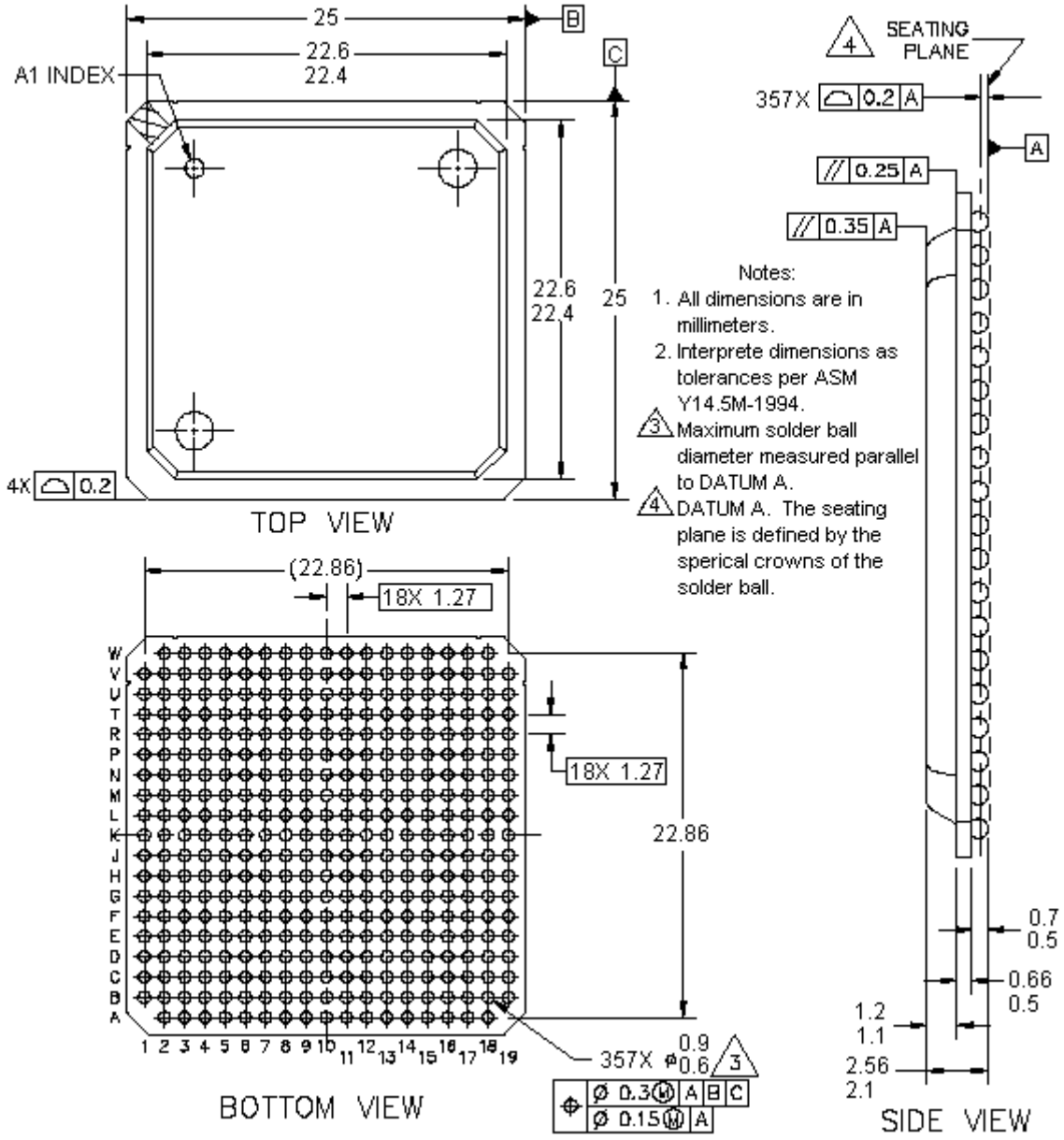


Figure 25. MPC8241 Package Dimensions and Pinout Assignments (ZQ and VR Packages)

5.3 Pinout Listings

Table 16 provides the pinout listing for the MPC8241, 357 PBGA package.

Table 16. MPC8241 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	V11 V7 W3 R3	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{DEVSEL}}$	U6	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{FRAME}}$	T8	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{IRDY}}$	U7	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{LOCK}}$	V6	Input	$GV_{DD}_OV_{DD}$	—	3
AD[31:0]	U13 V13 U11 W14 V14 U12 W10 T10 V10 U9 V9 W9 W8 T9 W7 V8 V4 W4 V3 V2 T5 R6 V1 T2 U3 P3 T4 R1 T3 R4 U2 U1	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	1, 2
PAR	R7	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2
$\overline{\text{GNT}}$[3:0]	W15 U15 W17 V12	Output	$GV_{DD}_OV_{DD}$	DRV_PCI	1, 2
$\overline{\text{GNT4}}$/DA5	T11	Output	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 4, 5
$\overline{\text{REQ}}$[3:0]	V16 U14 T15 V15	Input	$GV_{DD}_OV_{DD}$	—	1, 6
$\overline{\text{REQ4}}$/DA4	W13	I/O	$GV_{DD}_OV_{DD}$	—	5, 6
$\overline{\text{PERR}}$	T7	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3, 7
$\overline{\text{SERR}}$	U5	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3, 8
$\overline{\text{STOP}}$	W5	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{TRDY}}$	W6	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 3
$\overline{\text{INTA}}$	T12	Output	$GV_{DD}_OV_{DD}$	DRV_PCI	2, 8
IDSEL	U10	Input	$GV_{DD}_OV_{DD}$	—	—
Memory Interface Signals					
MDL[0:31]	M19 M17 L16 L17 K18 J18 K17 K16 J15 J17 H18 F16 H16 H15 G17 D19 B3 C4 C2 D3 G5 E1 H5 E2 F1 F2 G2 J5 H1 H4 J4 J1	I/O	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1, 9
MDH[0:31]	M18 L18 L15 K19 K15 J19 J16 H17 G19 G18 G16 D18 F18 E18 G15 E15 C3 D4 E5 F5 D1 E4 D2 E3 F4 G3 G4 G1 H2 J3 J2 K5	I/O	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1
DQM[0:7]	A18 B18 A6 C7 D15 D14 A9 B8	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{CS}}$[0:7]	A17 B17 C16 C17 C9 C8 A10 B10	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	1
FOE	A7	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{RCS0}}$	C10	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10, 11

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{RCS1}}$	B9	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{RCS2}}$/TRIG_IN	P18	I/O	$GV_{DD}_OV_{DD}$	—	5, 12
$\overline{\text{RCS3}}$/TRIG_OUT	N18	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	5
SDMA[1:0]	A15 B15	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	1, 10, 11
SDMA[11:2]	A11 B12 A12 C12 B13 C13 D12 A14 C14 B14	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	1
$\overline{\text{DRDY}}$	P1	Input	$GV_{DD}_OV_{DD}$	—	12, 13
SDMA12/$\overline{\text{SRESET}}$	L3	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA13/TBEN	K3	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDMA14/$\overline{\text{CHKSTOP_IN}}$	K2	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
SDBA1	C11	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	—
SDBA0	B11	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	—
PAR[0:7]	E19 C19 D5 D6 E16 F17 B2 C1	I/O	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1
$\overline{\text{SDRAS}}$	B19	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10
$\overline{\text{SDCAS}}$	D16	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10
CKE	C6	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10, 11
$\overline{\text{WE}}$	B16	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	—
$\overline{\text{AS}}$	A16	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	10, 11
PIC Control Signals					
IRQ0/S_INT	P4	Input	$GV_{DD}_OV_{DD}$	—	—
IRQ1/S_CLK	R2	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	—
IRQ2/S_RST	U19	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	—
IRQ3/$\overline{\text{S_FRAME}}$	P15	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	—
IRQ4/$\overline{\text{L_INT}}$	P2	I/O	$GV_{DD}_OV_{DD}$	DRV_PCI	—
I^2C Control Signals					
SDA	P17	I/O	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	8, 12
SCL	R19	I/O	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	8, 12
DUART Control Signals					
SOUT1/PCI_CLK0	T16	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN1/PCI_CLK1	U16	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
SOUT2/$\overline{\text{RTS1}}$/PCI_CLK2	W18	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 14
SIN2/$\overline{\text{CTS1}}$/PCI_CLK3	V19	I	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 14, 24
Clock-Out Signals					
PCI_CLK0/SOUT1	T16	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	5, 14

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI_CLK1/SIN1	U16	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	5, 14, 24
PCI_CLK2/$\overline{\text{RTS1}}$/SOUT2	W18	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	5, 14
PCI_CLK3/$\overline{\text{CTS1}}$/SIN2	V19	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	5, 14, 24
PCI_CLK4/DA3	V17	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	5, 14
PCI_SYNC_OUT	U17	Output	$GV_{DD}_OV_{DD}$	DRV_PCI_CLK	—
PCI_SYNC_IN	V18	Input	$GV_{DD}_OV_{DD}$	—	—
SDRAM_CLK[0:3]	D7 B7 C5 A5	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	1, 22
SDRAM_SYNC_OUT	B4	Output	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	—
SDRAM_SYNC_IN	A4	Input	$GV_{DD}_OV_{DD}$	—	—
CKO/DA1	L1	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	5
OSC_IN	R17	Input	$GV_{DD}_OV_{DD}$	—	15
Miscellaneous Signals					
$\overline{\text{HRST_CTRL}}$	M2	Input	$GV_{DD}_OV_{DD}$	—	25
$\overline{\text{HRST_CPU}}$	L4	Input	$GV_{DD}_OV_{DD}$	—	25
$\overline{\text{MCP}}$	K4	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	10, 11, 16
NMI	M1	Input	$GV_{DD}_OV_{DD}$	—	—
$\overline{\text{SMI}}$	L2	Input	$GV_{DD}_OV_{DD}$	—	12
$\overline{\text{SRESET}}$/SDMA12	L3	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
TBEN/SDMA13	K3	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
$\overline{\text{QACK}}$/DA0	A3	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	5, 11, 12
$\overline{\text{CHKSTOP_IN}}$/SDMA14	K2	I/O	$GV_{DD}_OV_{DD}$	DRV_MEM_CTRL	5, 12
TRIG_IN/$\overline{\text{RCS2}}$	P18	I/O	$GV_{DD}_OV_{DD}$	—	5, 12
TRIG_OUT/$\overline{\text{RCS3}}$	N18	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	5
MAA[0:2]	E17 D17 C18	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1, 10, 11
$\overline{\text{MIV}}$	K1	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	23
PMAA[0:1]	N19 N17	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1, 2, 10, 11
PMAA[2]	M15	Output	$GV_{DD}_OV_{DD}$	DRV_STD_MEM	1, 2, 10, 11
Test/Configuration Signals					
PLL_CFG[0:4]/DA[10:6]	N3 N2 N1 M4 M3	I/O	$GV_{DD}_OV_{DD}$	—	1, 5, 20
$\overline{\text{TEST0}}$	P16	Input	$GV_{DD}_OV_{DD}$	—	13, 21
RTC	D13	Input	$GV_{DD}_OV_{DD}$	—	12
TCK	T19	Input	$GV_{DD}_OV_{DD}$	—	6, 13
TDI	N15	Input	$GV_{DD}_OV_{DD}$	—	6, 13
TDO	T17	Output	$GV_{DD}_OV_{DD}$	DRV_PCI	23

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
TMS	T18	Input	GV_{DD}_OV_{DD}	—	6, 13
$\overline{TRST}$	R16	Input	GV_{DD}_OV_{DD}	—	6, 13
Power and Ground Signals					
GNDRING/GND	F07 F08 F09 F10 F11 F12 F13 G07 G08 G09 G10 G11 G12 G13 H07 H08 H09 H10 H11 H12 H13 J07 J08 J09 J10 J11 J12 J13 K07 K08 K09 K10 K11 K12 K13 L07 L08 L09 L10 L11 L12 L13 M07 M08 M09 M10 M11 M12 M13 N07 N08 N09 N10 N11 N12 N13 P08 P09 P10 P11 P12 P13 R15	Ground	—	—	17
LV_{DD}	R18 U18 T1 U4 T6 W11 T14	Reference voltage 3.3 V, 5.0 V	LV_{DD}	—	—
GV_{DD}_OV_{DD}/PWRRING	D09 D10 D11 E06 E07 E08 E09 E10 E11 E12 E13 E14 F06 F14 G06 G14 H06 H14 J06 J14 K06 K14 L06 L14 M06 M14 N06 N14 P06 P07 P14 R08 R09 R10 R11 R12	Power for memory drivers and PCI/Stnd 3.3 V	GV_{DD}_OV_{DD}	—	18
V_{DD}	F03 H3 L5 N4 P5 V5 U8 W12 W16 R13 P19 L19 H19 F19 F15 C15 A13 A8 B5 A2	Power for core 1.8 V	V_{DD}	—	—
No Connect	N5 W2 B1	—	—	—	—
AV_{DD}	M5	Power for PLL (CPU core logic) 1.8 V	AV_{DD}	—	—
$AV_{DD}2$	R14	Power for PLL (peripheral logic) 1.8 V	$AV_{DD}2$	—	—
Debug/Manufacturing Pins					
DA0/$\overline{QACK}$	A3	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5, 11, 12
DA1/CKO	L1	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	5
DA2	R5	Output	GV_{DD}_OV_{DD}	DRV_PCI	19
DA3/PCI_CLK4	V17	Output	GV_{DD}_OV_{DD}	DRV_PCI_CLK	5
DA4/$\overline{REQ4}$	W13	I/O	GV_{DD}_OV_{DD}	—	5, 6
DA5/$\overline{GNT4}$	T11	Output	GV_{DD}_OV_{DD}	DRV_PCI	2, 4, 5

Table 16. MPC8241 Pinout Listing (continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
DA[10:6]/ PLL_CFG[0:4]	N3 N2 N1 M4 M3	I/O	GV_{DD}_OV_{DD}	—	1, 5, 20
DA[11]	T13	Output	GV_{DD}_OV_{DD}	DRV_PCI	1, 19
DA[12:13]	M16 N16	Output	GV_{DD}_OV_{DD}	DRV_STD_MEM	19
DA[14:15]	B6 D8	Output	GV_{DD}_OV_{DD}	DRV_MEM_CTRL	1, 19

Notes:

1. Multi-pin signals such as AD[31:0] or MDL[0:31] physical package pin numbers are listed in order corresponding to the signal names. Ex: AD0 is on pin U1, AD1 is on pin U2,..., AD31 is on pin U13.
2. This pin is affected by a programmable PCI_HOLD_DEL parameter.
3. A weak pull-up resistor (2–10 kΩ) should be placed on this PCI control pin to LV_{DD}.
4. $\overline{\text{GNT4}}$ is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state.
5. This pin is a multiplexed signal and appears more than once in this table.
6. This pin has an internal pull-up resistor that is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
7. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification* (Rev. 2.2).
8. This pin is an open-drain signal.
9. DL[0] is a reset configuration pin with an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
10. This pin has an internal pull-up resistor that is enabled only when in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
11. This pin is a reset configuration pin.
12. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to GV_{DD}_OV_{DD}.
13. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
14. External PCI clocking source or fanout buffer may be required for system if using the MPC8241 DUART functionality because PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
15. OSC_IN uses the 3.3-V PCI interface driver, which is 5-V tolerant. See Table 2 for details.
16. This pin can be programmed as driven (default) or as open-drain (in MIOCR 1).
17. All grounded pins are connected together. Connections should not be made to individual pins. The list represents the balls that are connected to ground.
18. GV_{DD}_OV_{DD} must not exceed V_{DD}/AV_{DD}/AV_{DD}2 by more than 1.8 V at any time including during power-on reset. Note that GV_{DD}_OV_{DD} pins are all shorted together, PWRRING. The list represents the balls that are connected to PWRRING. Connections should not be made to individual PWRRING pins.
19. Treat these pins as no connects unless debug address functionality is used.
20. PLL_CFG signals must be driven on reset and must be held for at least 25 clock cycles after the negation of $\overline{\text{HRST_CTRL}}$ and $\overline{\text{HRST_CPU}}$ in order to be latched.
21. Place a pull-up resistor of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
22. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev. 1.1 (A). These signals use DRV_MEM_CLK for chip Rev. 1.2B.
23. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.
24. Freescale typically expects that customers using the serial port will have sufficient drivers available in the RS232 transceiver to drive the $\overline{\text{CTS}}$ pin actively as an input if they are using that mode. No pullups would be needed in these circumstances.
25. $\overline{\text{HRST_CPU}}$/$\overline{\text{HRST_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state

6 PLL Configuration

The PLL_CFG[0:4] are configured by the internal PLLs. For a specific PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations are shown in Table 17 and Table 18.

Table 17. PLL Configurations (166- and 200-MHz)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	Not available			25-26[5]	75-78	188-195	3 (2)	2.5 (2)
2	00010	34[4]–37[5]	34–37	153–166	34[4]–44[5]	34–44	153–200	1 (4)	4.5 (2)
3	00011[6]	50[7]–66[3]	50–66	100–132	50[7]–66[3]	50–66	100–132	1 (Bypass)	2 (4)
4	00100	25–41[5]	50–82	100–164	25–44[8,10]	50–88	100–176	2 (4)	2 (4)
6	00110[9]	Bypass			Bypass			Bypass	Bypass
7 Rev. B	00111[6]	50[4]–55 [5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (Bypass)	3 (2)
7 Rev. D	00111	Not available							
8	01000	50[4]–55[5]	50–55	150–166	50[4]–66[3]	50–66	150–198	1 (4)	3 (2)
9	01001	38[4]–41[5,11]	76–82	152–164	38[4]–50[5,12]	76–100	152–200	2 (2)	2 (2)
B	01011	Not available			44[5]	66	198	2(2)	2.5(2)
C	01100	30[4]–33[5]	60–66	150–165	30[4]–40[5]	60–80	150–200	2 (4)	2.5 (2)
E	01110	25–27[5]	50–54	150–162	25–33[5]	60–66	150–198	2 (4)	3 (2)
10	10000	25–27[5,11]	75–83	150–166	25–33[5,12]	75–100	150–200	3 (2)	2 (2)
12	10010	50[4]–55[5,11]	75–83	150–166	50[4]–66[3]	75–99	150–198	1.5 (2)	2 (2)
14	10100	Not available			25–28[5]	50–56	175–196	2 (4)	3.5 (2)
16	10110				25[5]	50	200	2(4)	4(2)
17	10111				25[5]	100	200	4(2)	2(2)
19	11001	33[5,13]	66	165	33[13]–40[5]	66–80	165–200	2(2)	2.5(2)
1A	11010	37[4]–41[5]	37–41	150–166	37[4]–50[5]	37–50	150–200	1 (4)	4 (2)
1B	11011	Not available			33[5,13]	66	198	2(2)	3(2)
1C	11100				44[5,13]	66	198	1.5(2)	3(2)
1D	11101	44[5,13]	66	166	44[13]–53[5]	66–80	165–200	1.5 (2)	2.5 (2)

Table 17. PLL Configurations (166- and 200-MHz) (continued)

Ref [2]	PLL_CFG [0:4] [1]	166 MHz-Part [2]			200-MHz Part [2]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [3] (MHz)	Peripheral Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1E	11110[14]	Not usable			Not usable			Off	Off
1F	11111[14]	Not usable			Not usable			Off	Off

Notes:

1. PLL_CFG[0:4] settings not listed are reserved. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value. Note the impact of the relevant revisions for mode 7.
2. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
3. Limited by maximum PCI input frequency (66 MHz).
4. Limited by minimum CPU VCO frequency (300 MHz).
5. Limited by maximum CPU operating frequency.
6. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
7. Limited by minimum CPU operating frequency (100 MHz).
8. Limited due to maximum memory VCO frequency (352 MHz).
9. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
10. Limited by maximum CPU VCO frequency (704 MHz).
11. Limited by maximum system memory interface operating frequency (83 MHz @ 166 MHz CPU bus speed).
12. Limited by maximum system memory interface operating frequency (100 MHz @ 200 MHz CPU bus speed).
13. Limited by minimum memory VCO frequency (132 MHz).
14. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.

Table 18. PLL Configurations (266-MHz Parts)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
0	00000	25–35[5]	75–105	188–263	3 (2)	2.5 (2)
1	00001	25–29[5]	75–88	225–264	3 (2)	3 (2)
2	00010	50[15]–59[5]	50–59	225–266	1 (4)	4.5 (2)
3	00011[12]	50[14]–66[1]	50–66	100–133	1 (Bypass)	2 (4)
4	00100	25–44[4]	50–88	100–176	2 (4)	2 (4)

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
6	00110[13]	Bypass			Bypass	
7 (Rev. B)	00111[12]	50[6]–66[1]	50–66	150–198	1 (Bypass)	3 (2)
7 (Rev. D)	00111[14]	Not Available				
8	01000	50[6]–66[1]	50–66	150–198	1 (4)	3 (2)
9	01001	38[6]–66[1]	76–132	152–264	2 (2)	2 (2)
A	01010	25–29[5]	50–58	225–261	2 (4)	4.5 (2)
B	01011	45[3]–59[5]	68–88	204–264	1.5 (2)	3 (2)
C	01100	30[6]–44[4]	60–88	150–220	2 (4)	2.5 (2)
D	01101	45[3]–50[5]	68–75	238–263	1.5 (2)	3.5 (2)
E	01110	25–44[5]	50–88	150–264	2 (4)	3 (2)
F	01111	25[5]	75	263	3 (2)	3.5 (2)
10	10000	25–44[5]	75–132	150–264	3 (2)	2 (2)
11	10001	25–26[5]	100–106	250–266	4 (2)	2.5 (2)
12	10010	50[6]–66[1]	75–99	150–198	1.5 (2)	2 (2)
13	10011	Not available			4 (2)	3 (2)
14	10100	25–38[5]	50–76	175–266	2 (4)	3.5 (2)
15	10101	Not available			2.5 (2)	4 (2)
16	10110	25–33[5]	50–66	200–264	2 (4)	4 (2)
17	10111	25–33[5]	100–132	200–264	4 (2)	2 (2)
18	11000	27[3]–35[5]	68–88	204–264	2.5 (2)	3 (2)
19	11001	33[3]–53[5]	66–106	165–265	2 (2)	2.5 (2)
1A	11010	50[18]–66[1]	50–66	200–264	1 (4)	4 (2)
1B	11011	34[3]–44[5]	68–88	204–264	2 (2)	3 (2)
1C	11100	44[3]–59[5]	66–88	198–264	1.5 (2)	3 (2)
1D	11101	44[3]–66[1]	66–99	165–248	1.5 (2)	2.5 (2)
1E (Rev. B)	11110[8]	Not usable			Off	Off
1E (Rev. D)	11110	33[3]-38[5]	66-76	231-266	2(2)	3.5(2)

Table 18. PLL Configurations (266-MHz Parts) (continued)

Ref [2]	PLL_CFG[0:4] [10,11]	266-MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO)	Mem-to-CPU (CPU VCO)
1F	11111[8]	Not usable			Off	Off

Notes:

1. Limited by maximum PCI input frequency (66 MHz).
2. Note the impact of the relevant revisions for modes 7 and 1E.
3. Limited by minimum memory VCO frequency (132 MHz).
4. Limited due to maximum memory VCO frequency (352 MHz).
5. Limited by maximum CPU operating frequency.
6. Limited by minimum CPU VCO frequency (300 MHz).
7. Limited by maximum CPU VCO frequency (704 MHz).
8. In clock off mode, no clocking occurs inside the MPC8241, regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings that are not listed are reserved.
11. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
12. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in PLL bypass mode.
13. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling. The AC timing specifications in this document do not apply in dual PLL bypass mode.
14. Limited by minimum CPU operating frequency (100 MHz).
15. Limited by minimum memory bus frequency (50 MHz).

7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8241.

7.1 PLL Power Supply Filtering

The AV_{DD} and $AV_{DD}2$ power signals on the MPC8241 provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and $AV_{DD}2$ input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 26 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD} and $AV_{DD}2$ power signal pins. In *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), Dr. Howard Johnson recommends using multiple small capacitors of equal value instead of multiple values.

Place the circuits as closely as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing from the capacitors to the input signal pins should be as direct as possible with minimal inductance of vias.

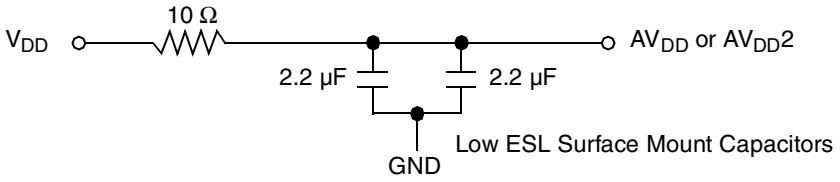


Figure 26. PLL Power Supply Filter Circuit

7.2 Decoupling Recommendations

Dynamic power management, large address and data buses, and high operating frequencies enable the MPC8241 to generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8241 system, and the MPC8241 itself requires a clean, tightly regulated source of power. Therefore, place at least one decoupling capacitor at each V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} pin. These decoupling capacitors receive their power from dedicated power planes in the PCB, using short traces to minimize inductance. These capacitors should have a value of 0.1 µF. To minimize lead inductance, use only ceramic SMT (surface mount technology) capacitors, preferably 0508 or 0603, on which connections are made along the length of the part.

In addition, distribute several bulk storage capacitors around the PCB to feed the V_{DD}, GV_{DD}_OV_{DD}, and LV_{DD} planes and enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the necessary quick response time, and should be connected to the power and ground planes through two vias to minimize inductance. Freescale recommends using bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

7.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Tie unused active-low inputs to OV_{DD}. Connect unused active-high inputs to GND. All no connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}_OV_{DD}, LV_{DD}, and GND pins.

The PCI_SYNC_OUT signal is to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input.

The SDRAM_SYNC_OUT signal is to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8241. The trace length can be used to skew or adjust the timing window as needed. See the Tundra *Tsi107™ Design Guide* (AN1849) and Freescale application notes AN2164/D, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part 1* and AN2746, *MPC8245/MPC8241 Memory Clock Design Guidelines: Part* 2 for more details. Note the SDRAM_SYNC_IN to PCI_SYNC_IN time requirement (see Table 10).

7.4 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) are disabled, and their outputs drive logic zeros when they would otherwise be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to GV_{DD}_OV_{DD}.

RTC should have weak pull-up resistors (2–10 kΩ) connected to GV_{DD}_OV_{DD} and that the following signals should be pulled up to GV_{DD}_OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, $\overline{\text{QACK}}$/DA0, and $\overline{\text{DRDY}}$.

The following PCI control signals should be pulled up to LV_{DD} (the clamping voltage) with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to have stronger adjustment to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16.

The following pins have internal pull-up resistors that are enabled only while the device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], and PMAA[0:2]. See Table 16.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST_CPU}}$ and $\overline{\text{HRST_CTRL}}$.

Reset configuration pins should be tied to GND by means of 1-kΩ pull-down resistors to ensure that a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level by means of weak pull-up resistors (2–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND by means of weak pull-down resistors (2–10 kΩ).

7.5 PCI Reference Voltage—LV_{DD}

The MPC8241 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8241 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 V ± 5% power supply if interfacing the MPC8241 into a 5-V PCI bus system. For either reference voltage, the MPC8241 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8241 tolerates 5-V signals when interfaced into a 5-V PCI bus system. (See Errata No. 18 in the *MPC8245/MPC8241 Integrated Processor Chip Errata*).

7.6 JTAG Configuration Signals

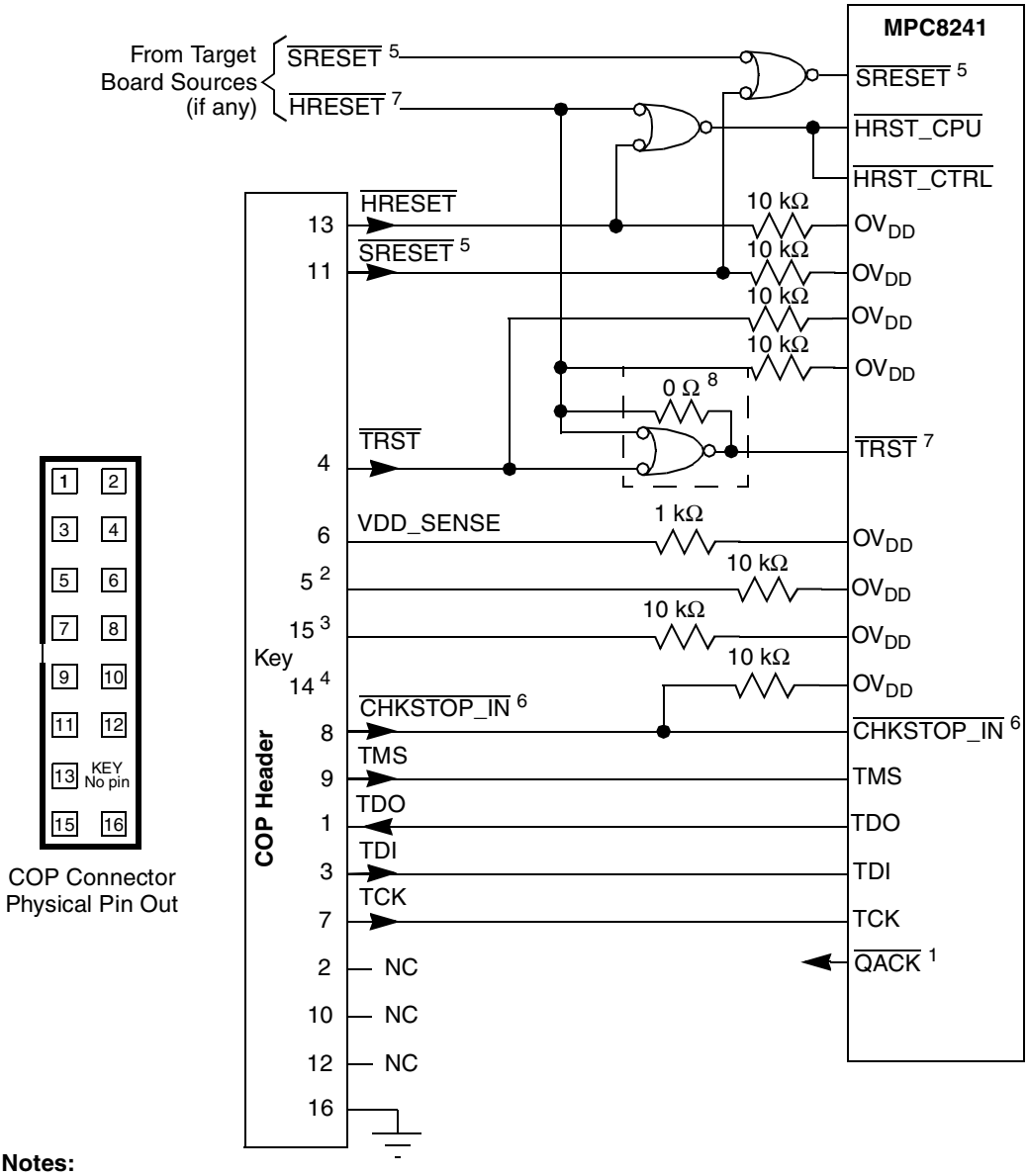
Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port, with additional status monitoring signals. The COP port must independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 27 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during power-on. Although Freescale recommends that the COP header be designed into the system as shown in Figure 27, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). Typically, pin 14 is removed as a connector key.

There is no standardized way to number the COP header shown in Figure 27. Consequently, different emulator vendors number the pins differently. Some pins are numbered top-to-bottom and left-to-right while others use left-to-right then top-to-bottom and still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 27 is common to all known emulators.



Notes:

1. $\overline{\text{QACK}}$ is an output and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally on pin 5 of the COP header is not implemented on the MPC8241. Connect pin 5 of the COP header to OV_{DD} with a 1- kΩ pull-up resistor.
3. $\overline{\text{CKSTP_OUT}}$ normally on pin 15 of the COP header is not implemented on the MPC8241. Connect pin 15 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
6. $\overline{\text{CHKSTOP_IN}}$ functions as output SDMA14 in extended ROM mode.
7. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown.
8. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header through an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.

Figure 27. COP Connector Diagram

7.7 Thermal Management

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, a heat sink may be required to maintain junction temperature within specifications. Proper thermal control design primarily depends on the system-level design: heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks can be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly (see Figure 28).

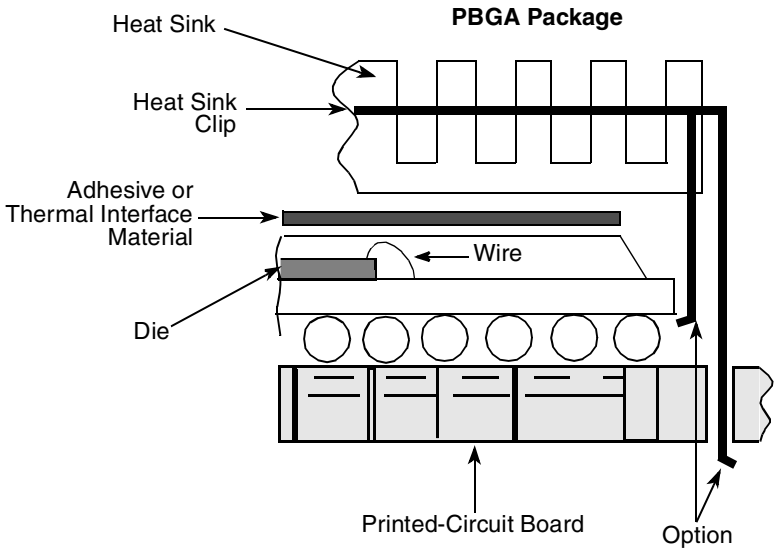


Figure 28. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 29 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s).
- A heat sink is not attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a high board-level thermal loading from adjacent components exists (label used—1s/sink).
- A large heat sink (cross cut extrusion, $38 \times 38 \times 16.5$ mm) is attached to the PBGA package and a low board-level thermal loading from adjacent components exists (label used—2s2p/sink).

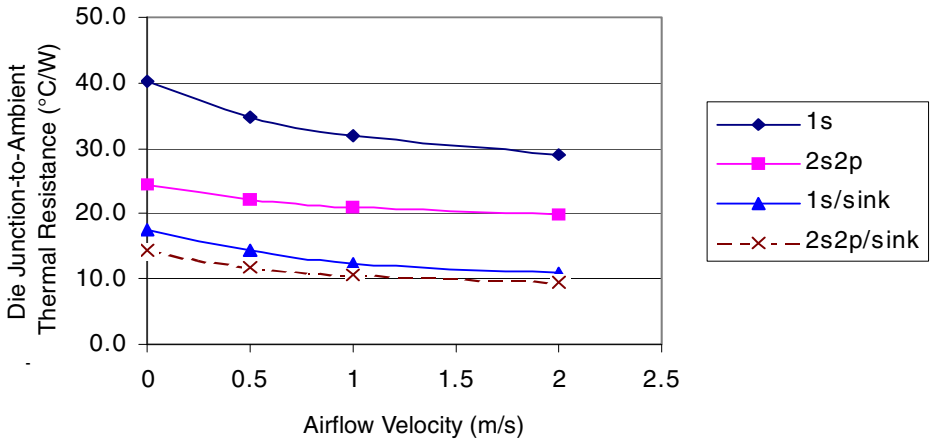


Figure 29. Die Junction-to-Ambient Resistance

The board designer can choose among several types of heat sinks to place on the MPC8241. Several commercially available heat sinks for the MPC8241 are provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

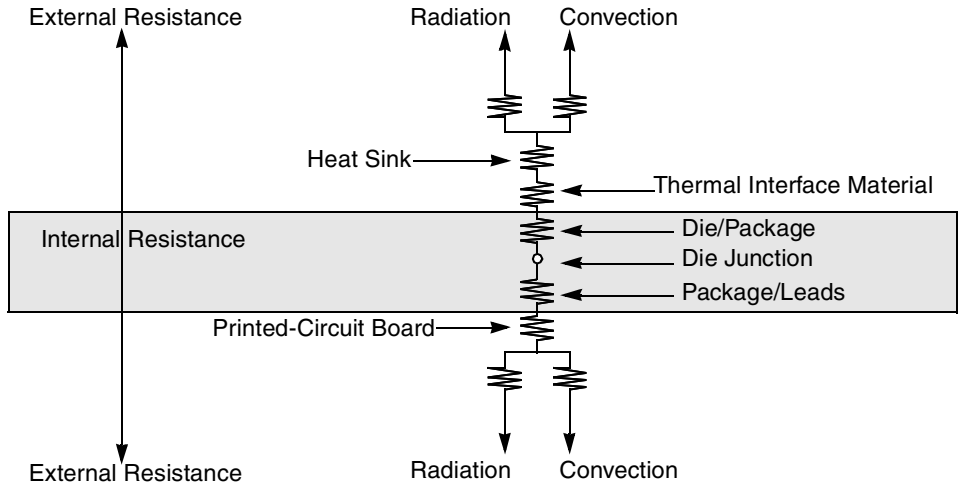
Selection of an appropriate heat sink depends on thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

7.7.1 Internal Package Conduction Resistance

For the PBGA, die-up, packaging technology, shown in Figure 28, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 30 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 30. PBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this die-up, wire-bond PBGA package, heat generated on the active side of the chip is conducted mainly through the mold cap, the heat sink attach material (or thermal interface material), and finally through the heat sink where forced-air convection removes it.

7.7.2 Adhesives and Thermal Interface Materials

A thermal interface material should be used between the top of the mold cap and the bottom of the heat sink minimizes thermal contact resistance. For applications that attach the heat sink by a spring clip mechanism, Figure 31 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. Thermal grease significantly reduces the interface thermal resistance. That is, the bare joint offers a thermal resistance approximately seven times greater than the thermal grease joint.

A spring clip attaches heat sinks to holes in the printed-circuit board (see Figure 28). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. The selection of any thermal interface material depends on factors such as thermal performance requirements, manufacturability, service temperature, dielectric properties, and cost.

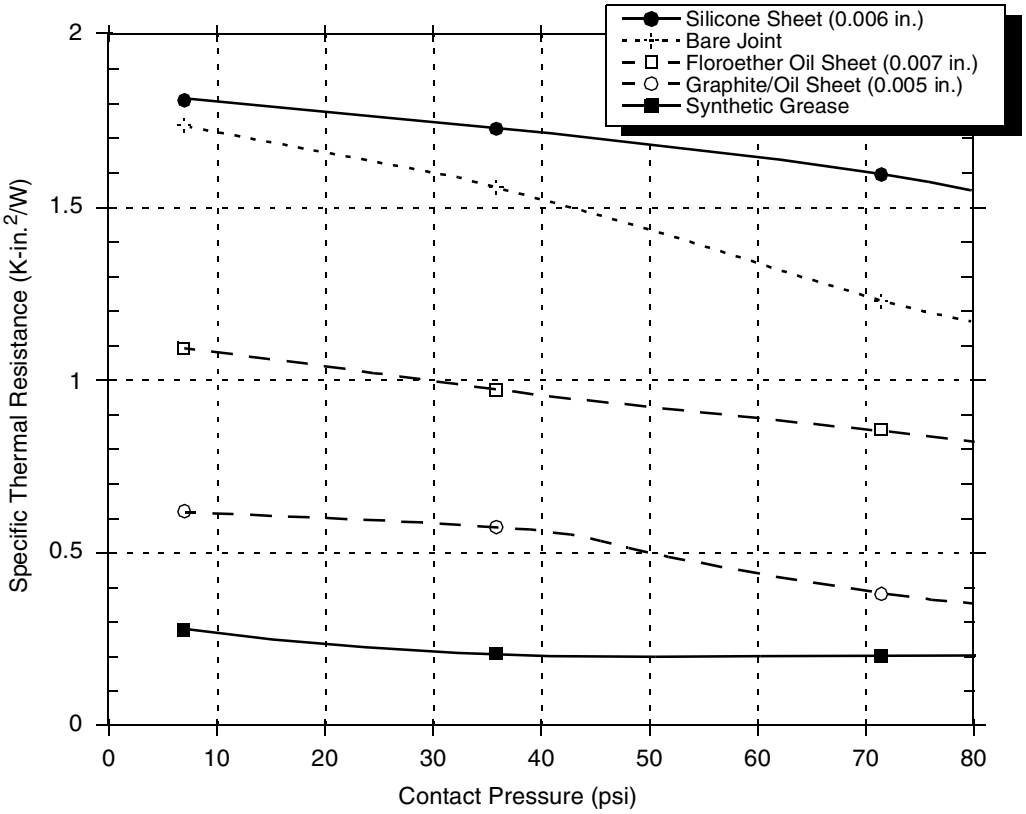


Figure 31. Thermal Performance of Select Thermal Interface Material

The board designer can choose among several types of thermal interface. Heat sink adhesive materials are selected on the basis of high conductivity and adequate mechanical strength to meet equipment shock/vibration requirements. Several commercially-available thermal interfaces and adhesive materials are provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

7.7.3 Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (ψ_{JT}) measures the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance minimizes the change in thermal performance that is caused by removing part of the thermal interface to the heat sink. Considering the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

7.8 References

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MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the web at http://www.jedec.org.

8 Ordering Information

Ordering information for the parts that this document fully covers is provided in Section 8.1, “Part Numbers Fully Addressed by This Document.” Section 8.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

8.1 Part Numbers Fully Addressed by This Document

Table 19 provides the Freescale part numbering nomenclature for the MPC8241. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number. Read the Revision ID register at address offset 0x08 to determine the revision level.

Table 19. Part Numbering Nomenclature

MPC	*nnnn*	L	*xx*	*nnn*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**
MPC	8241	L = Standard spec. 0° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14
			ZQ = thick substrate and thick mold cap PBGA (four layers, thermally enhanced)	266 1.8 V ± 100 mV	
			VR = Lead-free version of package	166, 200, 266 1.8 V ± 100 mV	

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specifications addendums that supplement and supersede this document (see Table 20).

Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2] (MHz)**	**Revision Level**	**Processor Version Register Value**

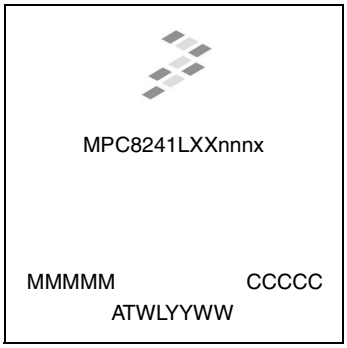
Table 20. Part Numbers Addressed by MPC8241TXXPNS Series (Document No. MPC8241ECSO1AD))

MPC	*nnnn*	T	*xx*	*nnn*	*x*	
MPC	8241	T = Extended temperature spec. –40° to 105°C	ZQ = thick substrate and thick mold cap PBGA (two layers)	166, 200 @ 1.8 V ± 100 mV	D:1.4 = Rev. ID:0x14	0x80811014

Notes:
1. See Section 5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by hardware specifications addendums may support other maximum core frequencies.

8.3 Part Marking

Parts are marked as the example shown in Figure 32.



Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is traceability code.
CCCCC is the country code.

Figure 32. Part Marking for MPC8241 Device

9 Document Revision History

Table 21 provides a revision history for this hardware specification.

Table 21. Revision History Table

Revision	Date	Substantive Change(s)
10	02/2009	In Table 16, “MPC8241 Pinout Listing,” added footnote 10 to PMAA[2]. In Table 16, “MPC8241 Pinout Listing,” removed footnote 12 for second listing of $\overline{\text{RCS3}}$/TRIG_OUT .
9	09/2007	Completely replaced Section 4.6 with compliant I^2C specifications as with other related integrated processor devices. Section 7.6, “JTAG Configuration Signals” Reworded paragraph beginning “The arrangement shown in Figure 27 .. .”

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
8	12/19/2005	Document—Imported new template and made minor editoral corrections. Section 4.3.1—Before Figure 7, added paragraph for using DLL mode that provides lowest locked tap point read in 0xE3. Section 4.3.2—After Figure 12, added a sentence to introduce Figure 13. Section 4.3.3—After Table 11, added a sentence to introduce Figure 14. Section 4.3.4—After Table 13, added to the sentence to introduce Figures 16 thru 19. Section 4.3.6—After Table 16, added a sentence to introduce Figures 22 thru 25. Section 5.3—Updated the driver and I/O assignment information for the multiplexed PCI clock and DUART signals. Added note for HRST_CPU and HRST_CTRL, which had been mentioned only in Figure 2. Section 9.2—Updated the part ordering specifications for the extended temperature parts. Also updated Section 9.2 to reflect what we offer for new orders. Updated Figure 34 to match with current part marking format. Section 8.3—Added new section for part marking information.
7	05/11/2004	Section 4.1.4 —Table 4: Changed the default for drive strength of DRV_STD_MEM. Section 4.3.1 —Table 8: Changed the wording for item 15 description. Section 4.3.4 —Table 10: Changed T_{os} range and wording in note 7; Figure 11: changed wording for SDRAM_SYNC_IN description relative to T_{OS}.
6.1	—	Section 4.3.1 — Table 9: Corrected last row to state the correct description for the bit setting: Max tap delay, DLL extend. Figure 8: Corrected the label name for the DLL graph to state “DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay”
6	—	Section 4.1.2 — Figure 2: Added note 6 and related label for latching of the PLL_CFG signals. Section 4.1.3 — Updated specifications for the input high and input low voltages of PCI_SYNC_IN. Section 4.3.1 — Table 8: Corrected typo for first number 1a to 1; Updated characteristics for the DLL lock range for the default and remaining three DLL locking modes; Reworded note description for note 6. Replaced contents of Table 9 with bit descriptions for the four DLL locking modes. In Figures 7 through 10, updated the DLL locking mode graphs. Section 4.3.2 — Table 10: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 4.3.3— Table 11: Changed the name of references for timing parameters from SDRAM_SYNC_IN to *sys_logic_clk* to be consistent with Figure 11. Followed the same change for note 2. Section 5.3 — Table 17: Removed extra listing of DRDY in test/configuration signal list and updated relevant notes for signal in memory Interface signal listing. Updated note #20. Added note 24 for the signals of the UART interface. Section 7.6 — Added relevant notes to this section and updated Figure 29.
5	—	Section 5.1— Updated package information to include all package offerings. Section 5.2 — Included package case outline for ZP (Rev. B) packaging parts. Section 9 — Updated Part markings for the offerings of the MPC8241. All sections — Nontechnical reformatting

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
4	—	Section 1.4.1.2—Table 2: Changed note 1. Figure 2: Updated note 2 and removed 'voltage regulator delay' label since Section 1.7.2 is being deleted this revision. Also, updated Table 5, note 1 to reflect deletion of Section 1.7.2. Section 1.4.1.3—Table 3: Updated the maximum input capacitance from 15 to 16 pF based on characterization data. Section 1.4.3.1—Updated PCI_SYNC_IN jitter specifications to 200 ps. Section 1.4.3.3—Table 11, item 12b: added the word 'address' to help clarify which signals the spec applies to. Figure 15: edited timing for items 12a0 and 12a2 to correspond with Table 11. Section 1.5.2—Changed some dimension values for the side view of package. Section 1.5.3—Updated notes for the $\overline{\text{QACK}}$/DA0 signal because this signal has been found to have no internal pull resistor. Section 1.6—Updated note numbering list for Table 19. Removed mode 5 from PLL tables since that mode is no longer supported. Section 1.7.2 —This section was removed as it was not necessary since the power information is covered in Section 1.4.1.5. Section 1.7.4—Added the words 'the clamping voltage' to describe LV_{DD} in the sixth paragraph. Changed the $\overline{\text{QACK}}$/DA0 signal from the list of signals having an internal pull-up resistor to the list of signals needing a weak pull-up resistor to OV_{DD}. Section 1.9.1—Table 21: Added processor version register value column.
3	—	Section 1.4.1.2—Changed recommended value in Table 2 for I/O buffer supply to 3.3 ± 0.3 V. Changed wording referencing Figure 4 to refer to the MPC8241. Section 1.4.2—Table 6: Updated values for thermal characterization data as per the new packaging and 266-MHz part. Added note 7 for the difference between the 166-/200-MHz and the 266-MHz packaging. Section 1.4.3—Corrected the voltage listing for the 266-MHz part to 1.8 ± 0.1 V in Table 7. Section 1.5—Changed package parameters and illustration based on new packaging. Section 1.6—Table 18: Modified PLL configuration for 166- and 200-MHz parts for mode 7 to specify that this mode is not available for Rev. D of the part. Added sentence to note 1 referencing update for mode 7. Table 19: Made several range updates for various modes to accommodate VCO limits. Added mode 7 and 1E updates for Rev. D. Updated VCO limits listed in notes 4, 6, and 7.
2	—	Section 1.4.1.2—Updated note 1 to include 266-MHz part. Added a line to cautions 2 and 3 in the notes section of Table 2. Added Figures 4 and 5 to show the overshoot and undershoot requirements for the PCI interface. Section 1.4.1.3—Table 3: Updated minimum value for input high voltage, and maximum value for capacitance. Section 1.4.3.2—Appended Figures 9 and 10. Section 1.4.3.4—Added a column to Table 13 to include 133-MHz memory bus speed for 266-MHz part. Section 1.5.2—Changed Figure 24 to accommodate new package offerings. Section 1.6—Added Table 19 for PLL of the 266-MHz part. Section 1.7.7—Corrected note numbering in COP connector diagram. Section 1.9.1—Updated package description in part marking nomenclature.

Table 21. Revision History Table (continued)

Revision	Date	Substantive Change(s)
1	—	Updated document template. Section 1.4.1.5—Updated driver type names in Table 4 so that they are consistent with the driver types referred to in the *MPC8245 Integrated Processor Reference Manual*. Added notes 5 and 6 to Table 4. Section 1.4.3.1—Added reference to AN2164 in note 7. Labeled N value in Figures 5 through 8. Section 1.4.3.2—Updated Figure 9 to show T_{os}. Table 9—Changed default for 0x77 bits 5:4 to 0b10. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid Timing. Updated Figure 13 to state GV_{DD}_OV_{DD} instead of OV_{DD}. Section 1.5.3—Updated driver type names to match those used in Table 4. Updated notes for the following signals: $\overline{\text{DRDY}}$, SDRAM_CLK[0:3], $\overline{\text{MIV}}$, RTC, TDO, and DA[11]. Section 1.6—Updated PLL table and notes. Removed old Section 1.7.2 on voltage sequencing requirements. Added cautions regarding voltage sequencing to the end of Table 2 in Section 1.4.1.2. Section 1.7.3—Changed sentence recommendation regarding decoupling capacitors. Section 1.7.5—Added reference to AN2164. Section 1.7.6—Added sentence regarding the PLL_CFG signals. Removed old Section 1.7.8 since the MPC8241 cannot be used as a drop in replacement for the MPC8240 because of pin compatibility issues. Section 1.7.8—Updated $\overline{\text{TRST}}$ information in this section and Figure 26. Section 1.7.9—Updated list for heat sink and thermal interface vendors. Section 1.9—Changed format of ordering information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.
0.3	—	Corrected solder ball information in Section 1.5.1 to 62 Sn/36 Pb/2 Ag. Section 1.4.3.1—Corrected DLL_EXTEND labeling in Figures 5 through 8. Removed note for pin TRIG_OUT/RCS3 in Table 16, as well as from the list of pins needing to be pulled up to IV_{DD} in Section 1.7.6. Corrected order information labeling in Section 1.9 to MPC8241XZPXXXX. Also corrected label description of ZU = PBGA to ZP = PBGA.
0.2	—	Table 16—Corrected pin number for PLL_CFG0/DA10 to N3. The pin was already correctly listed for DA10/PLL_CFG0. Updated note 1 to reflect pin assignments for the MPC8241. Updated footnotes throughout document. Section 1.4.3.3—Updated note 4 to correct bit values of PCI_HOLD_DEL in PMCR2. Section 1.6—Updated notes in Table 17. Included memory VCO minimum and maximum numbers. Section 1.7.8—Updated description of bits PCI_HOLD_DEL in PMCR2. Section 1.7.10.3—Replaced thermal characterization parameter (YJT) with correct thermal characterization parameter (Ψ_{JT}). Changed Ψ_{π} symbol to Ψ_{JT}.
0.1	—	Updated Features list in Section 1.2. Corrected pin assignments in Table 16 for DA[15] and DQM[3] signals. Added vendor (Cool Innovations, Inc.) to list of heat sink vendors.
0	—	Initial release.

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