

FS5502

High voltage PMIC with multiple SMPS and LDO

Rev. 4 — 27 October 2021 Product data sheet

1 General description

This device family is part of a global platform including FS5502/VR5500 (Quality Management), FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. This data sheet covers FS5502 device only.

The FS5502 is an automotive high voltage multi-output power supply integrated circuit, with focus on radio and radar applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance and it is qualified in compliance with AEC-Q100 rev H (Grade1, MSL3).

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- Low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- One linear voltage regulator for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode with very low sleep current (10 µA typ)
- Two input pins for wake-up detection and battery voltage sensing
- Device control via I^2C interface with CRC
- Power synchronization pin to operate two FS5502 devices or FS5502 plus an external PMIC
- Three voltage monitoring circuits, dedicated interface for MCU monitoring, power good, reset and interrupt outputs
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

3 Applications

- Radio
- V2x
- Infotainment

4 Simplified application diagram

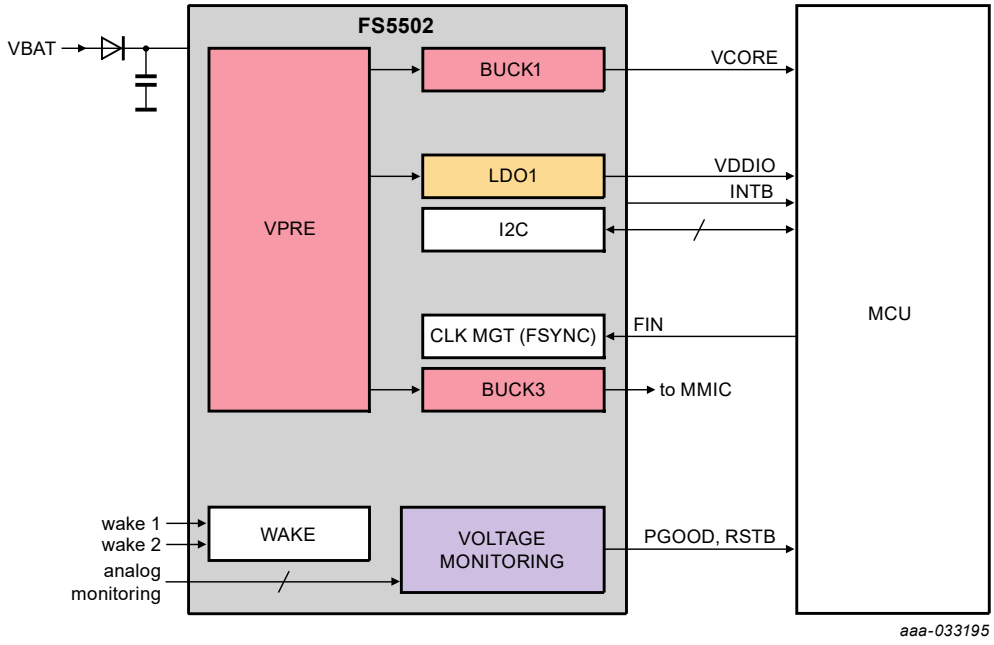


Figure 1. Simplified application diagram of FS5502

5 Ordering information

Table 1. Ordering information

Part number [1] [2] [3]	Package			OTP ID
	Name	Description	Version	
MC33FS5502Y0ES	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT684-23	—
MC33FS5502Y3ES				http://www.nxp.com/MC33FS5502Y3ES-OTP-Report
MC33FS5502Y0KS				—
MC33FS5502Y3KS				http://www.nxp.com/MC33FS5502Y3KS-OTP-Report

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Step-cut wettable flank for part numbers ending in ES. Dimple wettable flank for part numbers ending in KS.
[3] The part numbers with KS suffix are recommended for new designs.

Y0 part is a non-programmed OTP configuration. Pre-programmed OTP configurations (other than BUCK regulators) will be managed through suffix Y1 to ZZ.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

6 Block diagram

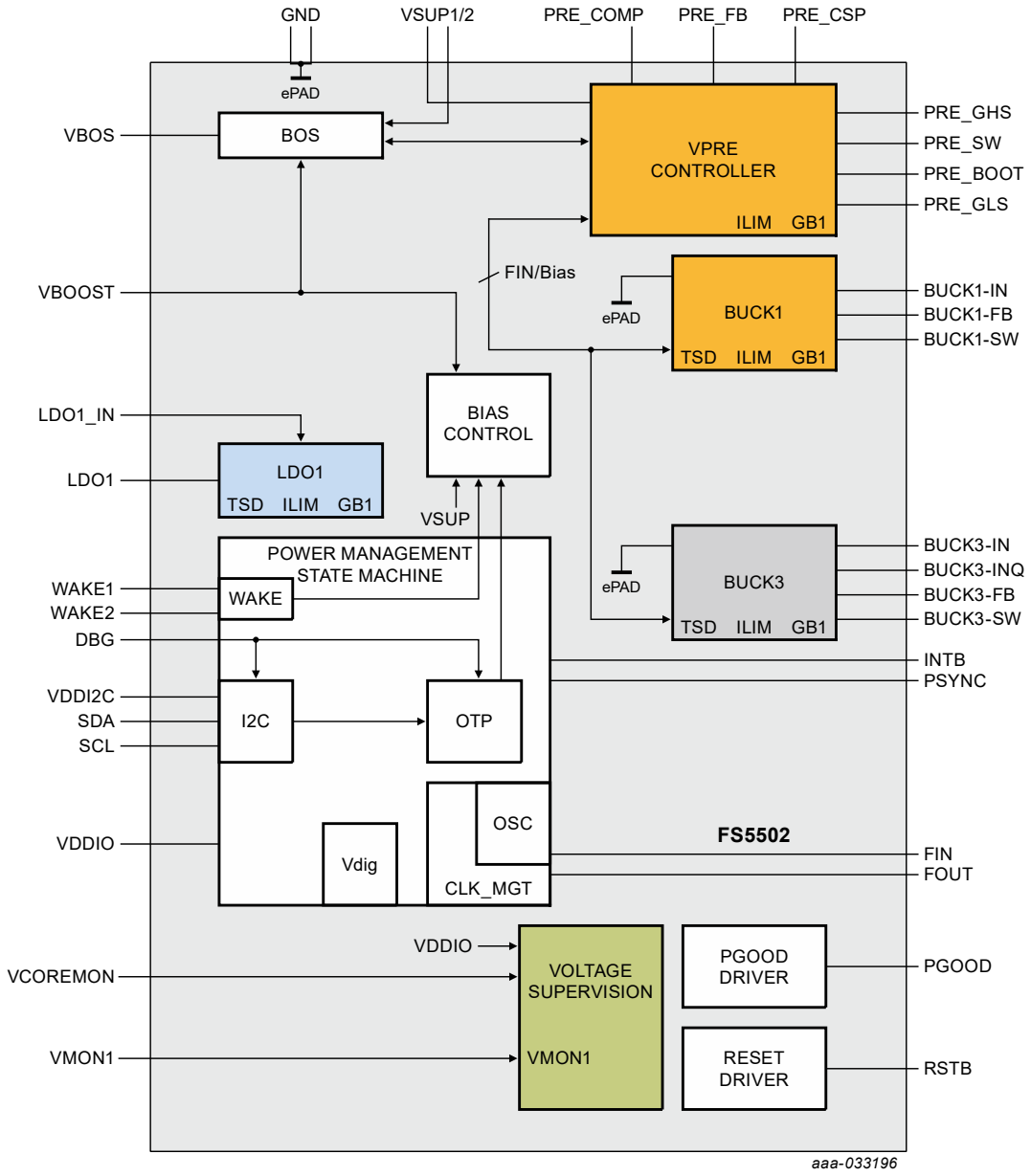


Figure 2. Block diagram of FS5502

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7 Pinning information

7.1 Pinning

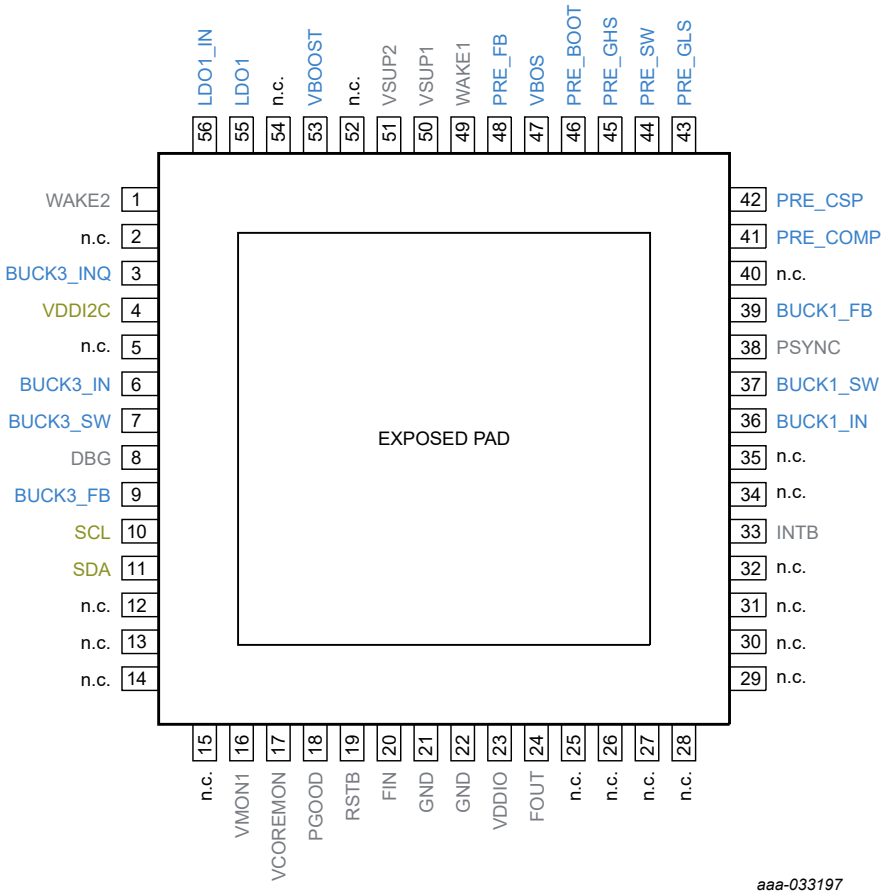


Figure 3. Pin configuration for HVQFN56

7.2 Pin description

See Section 7.3 for connection of unused pins.

Table 2. Pin description

Symbol	Pin	Type	Description
WAKE2	1	A_IN / D_IN	Wake-up input 2 An external serial resistor is required if WAKE2 is a global pin
n.c.	2	n.c.	Not connected pin
BUCK3_INQ	3	A_IN	Low voltage BUCK3 quiet input voltage
VDDI2C	4	A_IN	Input voltage for I^2C buffers
n.c.	5	n.c.	Not connected pin
BUCK3_IN	6	A_IN	Low voltage BUCK3 input voltage
BUCK3_SW	7	A_OUT	Low voltage BUCK3 switching node
DBG	8	A_IN	Debug mode entry
BUCK3_FB	9	A_IN	Low voltage BUCK3 voltage feedback

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 2. Pin description...*continued*

Symbol	Pin	Type	Description
SCL	10	D_IN	I^2C bus Clock input
SDA	11	D_IN/OUT	I^2C bus Bidirectional data line
n.c.	12	n.c.	Not connected pin
n.c.	13	n.c.	Not connected pin
n.c.	14	n.c.	Not connected pin
n.c.	15	n.c.	Not connected pin
VMON1	16	A_IN	Voltage monitoring input 1
VCOREMON	17	A_IN	VCORE monitoring input: Must be connected to BUCK1 output voltage
PGOOD	18	D_OUT	Power good output Active low Pull up to VDDIO mandatory
RSTB	19	D_OUT	Reset output Active low The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault condition. Pull up to VDDIO mandatory
FIN	20	D_IN	Frequency synchronization input
GND	21	GND	Ground
GND	22	GND	Ground
VDDIO	23	A_IN	Input voltage FOUT buffers Allow voltage compatibility with MCU I/Os
FOUT	24	D_OUT	Frequency synchronization output
n.c.	25	n.c.	Not connected pin
n.c.	26	n.c.	Not connected pin
n.c.	27	GND	External pull down to GND
n.c.	28	n.c.	Not connected pin
n.c.	29	n.c.	Not connected pin
n.c.	30	n.c.	Not connected pin
n.c.	31	n.c.	Not connected pin
n.c.	32	n.c.	Not connected pin
INTB	33	D_OUT	Interrupt output
n.c.	34	n.c.	Not connected pin
n.c.	35	n.c.	Not connected pin
BUCK1_IN	36	A_IN	Low voltage BUCK1 input voltage
BUCK1_SW	37	A_OUT	Low voltage BUCK1 switching node
PSYNC	38	D_IN/OUT	Power synchronization input/output
BUCK1_FB	39	A_IN	Low voltage BUCK1 voltage feedback
n.c.	40	GND	External pull down to GND
PRE_COMP	41	A_IN	VPRE compensation network
PRE_CSP	42	A_IN	VPRE positive current sense input

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 2. Pin description*...continued*

Symbol	Pin	Type	Description
PRE_GLS	43	A_OUT	VPRE low-side gate driver for external MOSFET
PRE_SW	44	A_OUT	VPRE switching node
PRE_GHS	45	A_OUT	VPRE high-side gate driver for external MOSFET
PRE_BOOT	46	A_IN/OUT	VPRE bootstrap capacitor
VBOS	47	A_OUT	Best of supply output voltage
PRE_FB	48	A_IN	VPRE voltage feedback and negative current sense input
WAKE1	49	A_IN / D_IN	Wake up input 1 An external serial resistor is required if WAKE1 is a global pin
VSUP1	50	A_IN	Power supply 1 of the device An external reverse battery protection diode in series is mandatory
VSUP2	51	A_IN	Power supply 2 of the device An external reverse battery protection diode in series is mandatory
n.c.	52	n.c.	Not connected pin
VBOOST	53	A_IN	VBOOST voltage feedback Must be connected to PRE_FB
n.c.	54	n.c.	Not connected pin
LDO1	55	A_OUT	Linear regulator 1 output voltage
LDO1_IN	56	A_IN	Linear regulator 1 input voltage
EP	57	GND	Exposed pad (BUCK1 and BUCK3 low-side GNDs are connected to the expose pad)

7.3 Connection of unused pins

Table 3. Connection of unused pins

Pin	Name	Type	Connection if not used
1	WAKE2	A_IN / D_IN	External pull down to GND
2	n.c.	n.c.	Open
3	BUCK3_INQ	A_IN	Open
4	VDDI2C	A_IN	Open
5	n.c.	n.c.	Open
6	BUCK3_IN	A_IN	Open
7	BUCK3_SW	A_OUT	Open
8	DBG	A_IN	**Connection mandatory**
9	BUCK3_FB	A_IN	Open
10	SCL	D_IN	External pull down to GND
11	SDA	D_IN/OUT	External pull down to GND
12	n.c.	n.c.	Open
13	n.c.	n.c.	Open
14	n.c.	n.c.	Open
15	n.c.	n.c.	Open
16	VMON1	A_IN	Open – 2 MΩ internal pull down to GND, OTP_VMON1_EN=0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 3. Connection of unused pins*...continued*

Pin	Name	Type	Connection if not used
17	VCOREMON	A_IN	**Connection mandatory**
18	PGOOD	D_OUT	**Connection mandatory**
19	RSTB	D_OUT	**Connection mandatory**
20	FIN	D_IN	External pull down to GND
21	GND	GND	**Connection mandatory**
22	GND	GND	**Connection mandatory**
23	VDDIO	A_IN	**Connection mandatory**
24	FOUT	D_OUT	Open – push pull structure
25	n.c.	n.c.	Open
26	n.c.	n.c.	Open
27	n.c.	GND	External pull down to GND
28	n.c.	n.c.	Open
29	n.c.	n.c.	Open
30	n.c.	n.c.	Open
31	n.c.	n.c.	Open
32	n.c.	n.c.	Open
33	INTB	D_OUT	Open – 10 kΩ internal pull up to VDDIO
34	n.c.	n.c.	Open
35	n.c.	n.c.	Open
36	BUCK1_IN	A_IN	**Connection mandatory**
37	BUCK1_SW	A_OUT	**Connection mandatory**
38	PSYNC	D_IN/OUT	External pull up to VBOS
39	BUCK1_FB	A_IN	**Connection mandatory**
40	n.c.	n.c.	External pull down to GND
41	PRE_COMP	A_IN	See Section 14.7 "VPRE not populated"
42	PRE_CSP	A_IN	See Section 14.7 "VPRE not populated"
43	PRE_GLS	A_OUT	See Section 14.7 "VPRE not populated"
44	PRE_SW	A_OUT	See Section 14.7 "VPRE not populated"
45	PRE_GHS	A_OUT	See Section 14.7 "VPRE not populated"
46	PRE_BOOT	A_IN/OUT	See Section 14.7 "VPRE not populated"
47	VBOS	A_OUT	**Connection mandatory**
48	PRE_FB	A_IN	See Section 14.7 "VPRE not populated"
49	WAKE1	A_IN / D_IN	External pull down to GND
50	VSUP1	A_IN	**Connection mandatory**
51	VSUP2	A_IN	**Connection mandatory**
52	n.c.	n.c.	Open
53	VBOOST	A_IN	**Connection mandatory**
54	n.c.	n.c.	Open
55	LDO1	A_OUT	Open
56	LDO1_IN	A_IN	Open

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 3. Connection of unused pins...*continued*

Pin	Name	Type	Connection if not used
57	EP	GND	**Connection mandatory**

8 Functional description

The FS5502 device has two independent logic blocks. The main state machine manages the power management, the Standby mode and the wake-up sources. The fail-safe state machine manages the voltage monitoring of the power management.

8.1 Simplified functional state diagram

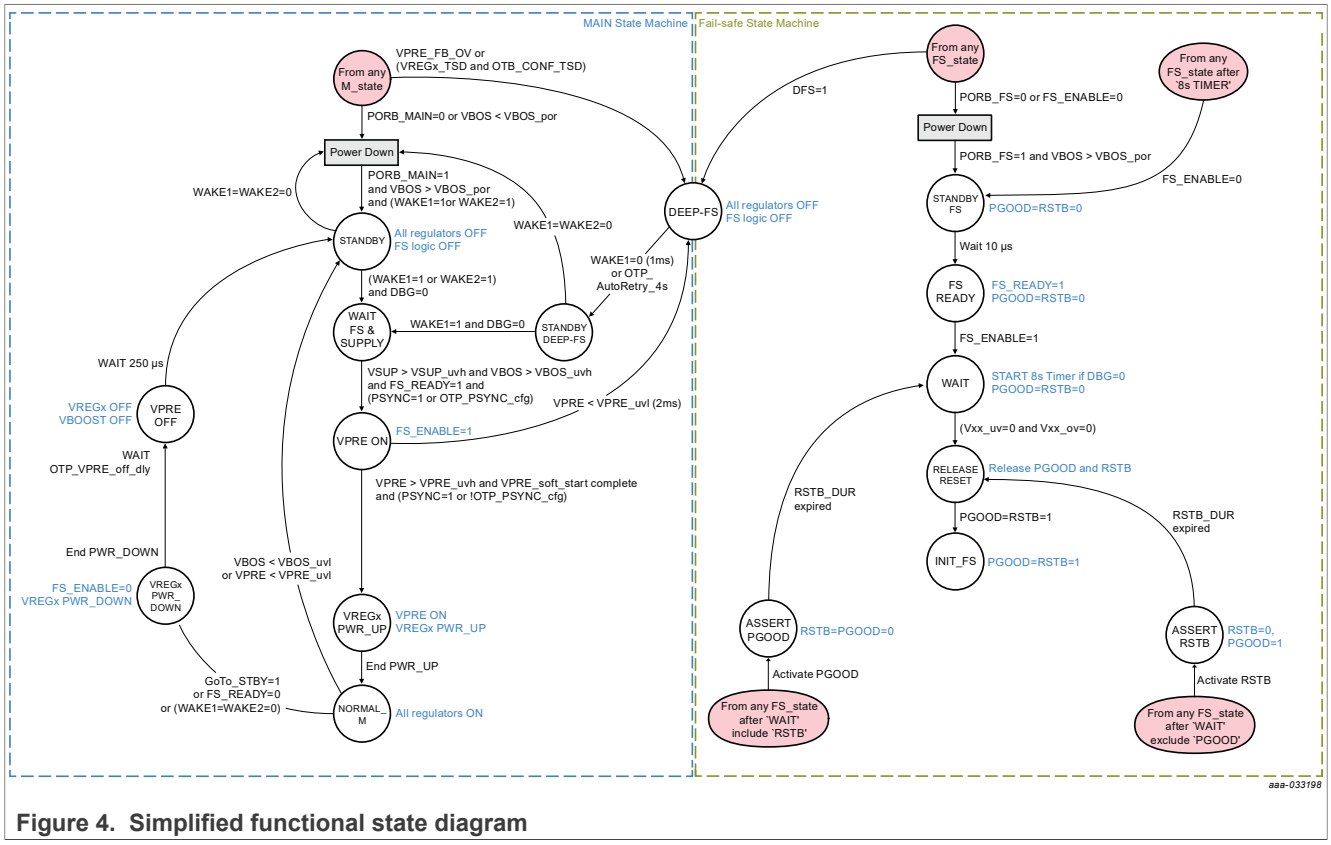


Figure 4. Simplified functional state diagram

8.2 Main state machine

The FS5502 start when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$ with VBOS first, followed by VPRE, and the power-up sequencing from the OTP programming for the remaining regulators if PSYNC pin is pulled up to VBOS. If during the power-up sequence VSUP < V_{SUP_UVL}, the device goes back to Standby mode. When the power-up is finished, the main state machine is in Normal_M mode, which is the application running mode with all the regulators ON and V_{SUP_UVL} has no effect even if VSUP < V_{SUP_UVL}. See Figure 29 for the minimum operating voltage.

The power up sequence can be synchronized with another PMIC using the PSYNC pin in order to stop before or after VPRE is ON and wait for the PMIC feedback on PSYNC pin before allowing FS5502 to continue its power up sequence. If the power up sequence

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

from VPRE ON to NORMAL_M is not completed within 1 second, the device goes back to Standby mode. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

The device goes to Standby mode by an I^2C command from the MCU. The device goes to Standby mode when both WAKE1 and WAKE 2 = 0. The device goes to Standby mode following the power down sequence to stop all the regulators in the reverse order of the power up sequence. VPRE shutdown can be delayed from 250 µs to 32 ms by OTP_VPRE_off_dly bit in case VPRE is supplying an external PMIC to wait its power down sequence completion.

In case of loss of VPRE (VPRE < V_{PRE_UVL}) or loss of VBOS (VBOS < V_{BOS_UVL}), the device stops and goes directly to Standby mode without power down sequence. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

In case of VPRE_FB_OV detection, or TSD detection on a regulator depending on OTP_conf_tsd[5:0] bits configuration, or deep fail-safe request from the fail-safe state machine when DFS = 1, the device stops and goes directly to DEEP-FS mode without power down sequence.

Exit of DEEP-FS mode is only possible by WAKE1 = 0 or after 4 s if the autoretry feature is activated by OTP_Autorety_en bit. The number of autoretry can be limited to 15 or infinite depending on OTP_Autoretry_infinite bit. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

8.3 Fail-safe state machine

The fail-safe state machine starts when VBOS > V_{BOS_POR}. RSTB and PGOOD pins are released and the initialization of the device is opened.

When RSTB and PGOOD pins are released, the device is ready for application running mode with all the selected monitoring activated. From now on, the FS5502 reacts by asserting the pins (PGOOD, RSTB) according to its configuration when a fault is detected.

8.4 Power sequencing

VPRE is the first regulator to start automatically, before the SLOT_0. The other regulators are starting from the OTP power sequencing configuration. Seven slots are available to program the start-up sequence of BUCK1, BUCK 3 and LDO1 regulators. The delay between each slot is configurable to 250 µs or 1 ms by OTP using OTP_Tslot bit to accommodate the different ramp up speed of BUCK1 and BUCK3.

The power up sequence starts at SLOT_0 and ends at SLOT_7 while the power down sequence is executed in reverse order. All the SLOTs are executed even if there is no regulator assigned to a SLOT. The regulators assigned to SLOT_7 are not started during the power up sequence. They can be started (or not) later in Normal_M mode with an I^2C command to write in M_REG_CTRL1 register, if they are enabled by OTP.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

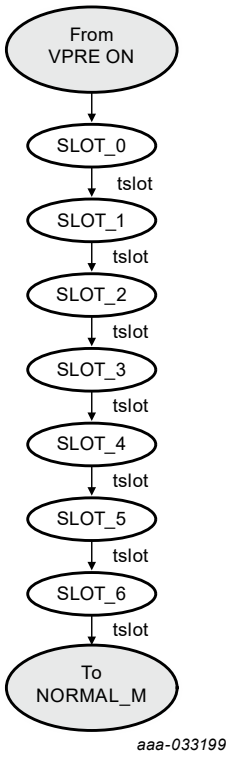


Figure 5. Power sequencing (VREGx PWR_UP)

Each regulator is assigned to a SLOT by OTP configuration using OTP_VB1S[2:0] for BUCK1, OTP_VB3S[2:0] for BUCK3, and OTP_LDO1S[2:0] for LDO1.

The different soft start duration of the BUCKs and the LDO should be considered in the SLOT assignment to achieve the correct sequence.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

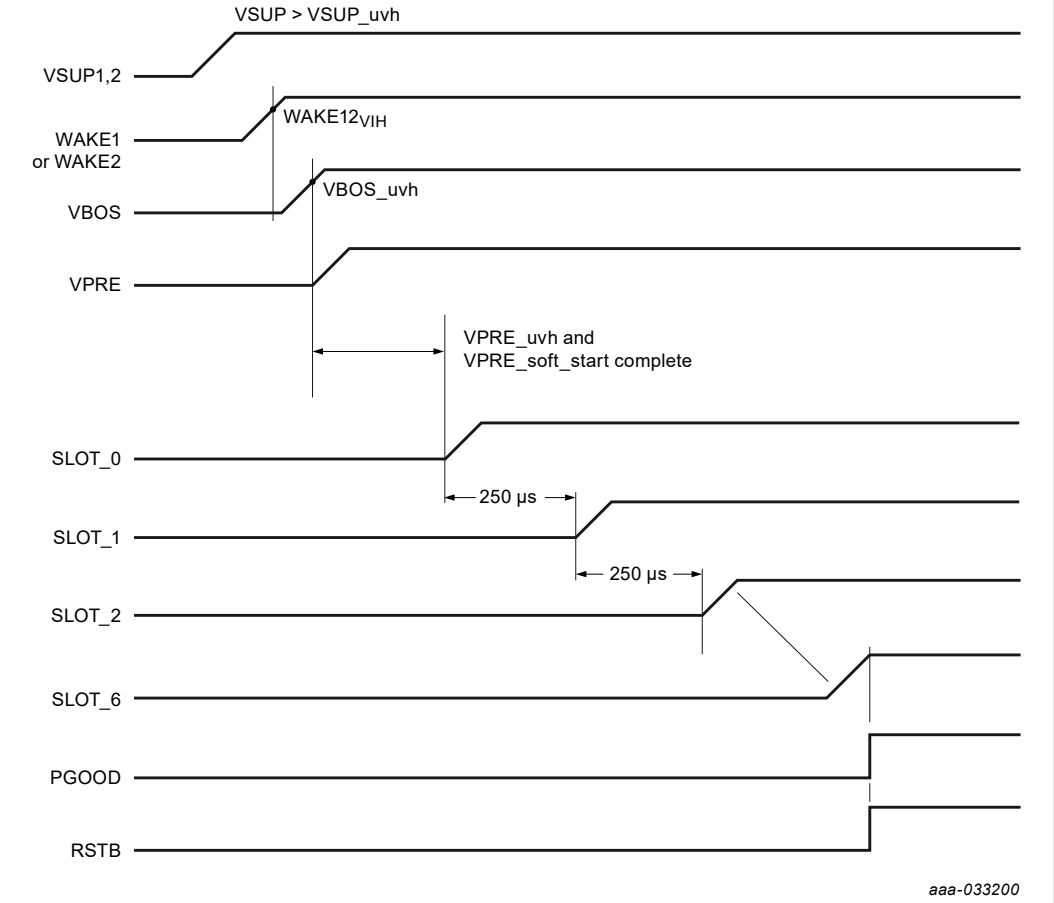


Figure 6. Power up sequence example

The FS5502_OTP_Mapping file used to generate the OTP configuration of the device draws the power up sequence of an OTP configuration in the OTP_conf_summary sheet.

8.5 Debug mode

The FS5502 enter in Debug mode with the sequence described in Figure 7:

1. DBG pin = V_{DBG} and VSUP > V_{SUP_UVH}
2. WAKE1 or WAKE2 > $WAKE12_{VIH}$

V_{DBG} and VSUP can come up at the same time as long as WAKE1 or WAKE2 comes up the last.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

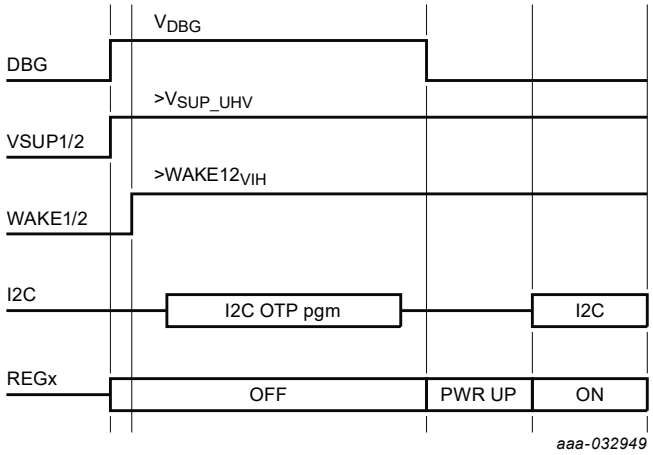


Figure 7. Debug mode entry

When the DBG pin is asserted low after T_{DBG} without I^2C command access, the device starts with the internal OTP configuration.

If V_{DBG} voltage is maintained at DBG pin, a new OTP configuration can be emulated or programmed by I^2C communication using NXP FlexGUI interface and NXP socket EVB. When the OTP process is completed, the device starts with the new OTP configuration when DBG pin is asserted low. The OTP emulation/programming is possible for during engineering development only. The OTP programming in production is done by NXP only.

In OTP Debug mode (DBG = 5.0 V), the I^2C address is fixed to 0x20 for the main digital access and 0x21 for the fail-safe digital access.

Table 4. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DBG}	Debug mode entry threshold	4.5	—	5.5	V
T_{DBG}	Debug mode entry filtering time (minimum duration of DBG = V_{DBG} after VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$)	7.0	—	—	ms

9 Register mapping

Register	M/FS	Address						R/W I^2C	Read / Write	Reference
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0			
M_FLAG	0	0	0	0	0	0	0	1/0	Read / Write	Section 10.3
M_MODE	0	0	0	0	0	0	1	1/0	Read / Write	Section 10.4
M_REG_CTRL1	0	0	0	0	0	1	0	1/0	Read / Write	Section 10.5
M_REG_CTRL2	0	0	0	0	0	1	1	1/0	Read / Write	Section 10.6
M_CLOCK	0	0	0	0	1	0	1	1/0	Read / Write	Section 10.7
M_INT_MASK1	0	0	0	0	1	1	0	1/0	Read / Write	Section 10.8
M_INT_MASK2	0	0	0	0	1	1	1	1/0	Read / Write	Section 10.9
M_FLAG1	0	0	0	1	0	0	0	1/0	Read / Write	Section 10.10
M_FLAG2	0	0	0	1	0	0	1	1/0	Read / Write	Section 10.11
M_VMON_REGX	0	0	0	1	0	1	0	1/0	Read / Write	Section 10.12
M_LVB1_SVS	0	0	0	1	0	1	1	1	Read only	Section 10.13
M_MEMORY0	0	1	0	0	0	1	1	1/0	Read / Write	Section 10.14
M_MEMORY1	0	1	0	0	1	0	0	1/0	Read / Write	Section 10.15
M_DEVICEID	0	1	0	0	1	0	1	1	Read only	Section 10.16

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Register	M/FS	Address						R/W I²C	Read / Write	Reference
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0			
FS_GRL_FLAGS	1	0	0	0	0	0	0	1	Read only	Section 11.3
FS_I_OVUV_SAFE_REACTION1	1	0	0	0	0	0	1	1/0	Write during INIT then Read only	Section 11.4
FS_I_NOT_OVUV_SAFE_REACTION1	1	0	0	0	0	1	0	1/0	Write during INIT then Read only	
FS_I_OVUV_SAFE_REACTION2	1	0	0	0	0	1	1	1/0	Write during INIT then Read only	Section 11.5
FS_I_NOT_OVUV_SAFE_REACTION2	1	0	0	0	1	0	0	1/0	Write during INIT then Read only	
FS_I_FSSM	1	0	0	1	0	0	1	1/0	Write during INIT then Read only	
FS_I_NOT_FSSM	1	0	0	1	0	1	0	1/0	Write during INIT then Read only	
FS_I_SVS	1	0	0	1	0	1	1	1/0	Write during INIT then Read only	Section 11.7
FS_I_NOT_SVS	1	0	0	1	1	0	0	1/0	Write during INIT then Read only	
FS_OVUVREG_STATUS	1	0	1	0	0	0	1	1/0	Read / Write	Section 11.8
FS_SAFE_IOS	1	0	1	0	0	1	1	1/0	Read / Write	Section 11.9
FS_DIAG	1	0	1	0	1	0	0	1/0	Read / Write	Section 11.10
FS_INTB_MASK	1	0	1	0	1	0	1	1/0	Read / Write	Section 11.11
FS_STATES	1	0	1	0	1	1	0	1/0	Read / Write	Section 11.12

10 Main register mapping

10.1 Main writing registers overview

Table 5. Main writing registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Main	M_FLAG	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
	M_MODE	0	0	0	0	0	0	0	0
		0	EXT_FIN_DIS	0	0	0	W2DIS	W1DIS	GoToSTBY
	M_REG_CTRL1	VPRE_PD_DIS	VPDIS	RESERVED	BUCK1DIS	RESERVED	BUCK3DIS	LDO1DIS	RESERVED
		0	VPEN	RESERVED	BUCK1EN	RESERVED	BUCK3EN	LDO1EN	RESERVED
	M_REG_CTRL2	RESERVED		RESERVED	BUCK1TSDCFG	RESERVED	BUCK3TSDCFG	LDO1TSDCFG	RESERVED
		0	0	0	VPRESRLS[1:0]		0	VPRESRHS[1:0]	
	M_CLOCK	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
		FOUT_ CLK_SEL	EXT_FIN_SEL	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
	M_INT_MASK1	0	VPREOC_M	0	BUCK1OC_M	RESERVED	BUCK3OC_M	LDO1OC_M	RESERVED
		0	0	RESERVED	BUCK1TSD_M	RESERVED	BUCK3TSD_M	LDO1TSD_M	RESERVED
	M_INT_MASK2	0	0	0	0	RESERVED	VBOSUVH_M	COM_M	VPRE_ FB_OV_M
		RESERVED	VSUPUV7	0	VPREUVH	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
	M_FLAG1	RESERVED	RESERVED	VPREOC	BUCK1OC	RESERVED	BUCK3OC	LDO1OC	RESERVED
		0	RESERVED	RESERVED	BUCK1OT	RESERVED	BUCK3OT	LDO1OT	RESERVED
	M_FLAG2	VPRE_FB_OV	VSUPUV7	0	0	0	0	0	0
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
	M_VMON_REGX	0	0	0	0	0	0	0	0
		0	0	0	0	0	VMON1_REG[2:0]		
	M_MEMORY0	MEMORY0[15:0]							
	M_MEMORY1	MEMORY1[15:0]							

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

10.2 Main reading registers overview

Table 6. Main reading registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Main	M_FLAG	COM_ERR	WU_G	VPRE_G	RESERVED	VBUCK1_G	RESERVED	VBUCK3_G	VLDO1_G
		RESERVED	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
	M_MODE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_LOCK_RT
		EXT_FIN_ SEL_RT	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2DIS	W1DIS	RESERVED
	M_REG_CTRL1	VPRE_PD_DIS	VPDIS	RESERVED	BUCK1DIS	RESERVED	BUCK3DIS	LDO1DIS	RESERVED
		0	VPEN	RESERVED	BUCK1EN	RESERVED	BUCK3EN	LDO1EN	RESERVED
	M_REG_CTRL2	RESERVED		RESERVED	BUCK1TSDCFG	RESERVED	BUCK3TSDCFG	LDO1TSDCFG	RESERVED
		RESERVED	RESERVED	RESERVED	VPRESRLS[1:0]		RESERVED	VPRESRHS[1:0]	
	M_CLOCK	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
		FOUT_ CLK_SEL	RESERVED	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
	M_INT_MASK1	RESERVED	VPREOC_M	RESERVED	BUCK1OC_M	RESERVED	BUCK3OC_M	LDO1OC_M	RESERVED
		RESERVED	RESERVED	RESERVED	BUCK1TSD_M	RESERVED	BUCK3TSD_M	LDO1TSD_M	RESERVED
	M_INT_MASK2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_M	COM_M	VPRE_ FB_OV_M
		RESERVED	VSUPUV7_M	RESERVED	VPREUVH_M	VSUPUV_M	VSUPUVH_M	WAKE1_M	WAKE2_M
	M_FLAG1	VBOSUVH	RESERVED	VPREOC	BUCK1OC	RESERVED	BUCK3OC	LDO1OC	RESERVED
		CLK_FIN_ DIV_OK	RESERVED	RESERVED	BUCK1OT	RESERVED	BUCK3OT	LDO1OT	RESERVED
	M_FLAG2	VPRE_FB_OV	VSUPUV7	RESERVED	BUCK1_ST	RESERVED	BUCK3_ST	LDO1_ST	RESERVED
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
	M_VMON_REGX	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VMON1_REG[2:0]		
	M_LVB1_SVS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	LVB1_SVS[4:0]				
	M_MEMORY0	MEMORY0[15:0]							
	M_MEMORY1	MEMORY1[15:0]							
	M_DEVICEID	FM_REV[3:0]				MM_REV[3:0]			
		M_DEVICEID[7:0]							

10.3 M_FLAG register

Table 7. M_FLAG register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	COM_ERR	WU_G	VPRE_G	RESERVED	VBUCK1_G	RESERVED	VBUCK3_G	VLDO1_G
Reset	0	1	1	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
Read	RESERVED	0	0	0	0	0	I2C_M_CRC	I2C_M_REQ
Reset	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 8. M_FLAG register bit description

Bit	Symbol	Description
23	COM_ERR	Report an error in the Communication (I^2C) **COM_ERR** = I2C_M_CRC or I2C_M_REQ or FS_COM_G
		0 No failure
		1 Failure
		Reset condition: Real time information - cleared when all individual bits are cleared
22	WU_G	Report a wake-up event by WAKE1 or WAKE2 **WU_G** = WK1FLG or WK2FLG
		0 No wake event
		1 Wake event
		Reset condition: Real time information - cleared when all individual bits are cleared
21	VPRE_G	Report an event on VPRE (status change or failure) **VPRE_G** = VPREOC or VPREUVH or VPREUVL or VPRE_FB_OV
		0 No event
		1 Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared
19	VBUCK1_G	Report an event on BUCK1 (status change or failure) **VBUCK1_G** = BUCK1OC or BUCK1OT
		0 No event
		1 Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared
17	VBUCK3_G	Report an event on BUCK3 (status change or failure) **VBUCK3_G** = BUCK3OC or BUCK3OT
		0 No event
		1 Event occurred
		Reset condition: Real time information - cleared when all individual bits are cleared
16	VLDO1_G	Report an event on LDO1 (status change or failure) **VLDO1_G** = LDO1OC or LDO1OT
		0 No event
		1 Event occurred
		Reset condition: Real time information
9	I2C_M_CRC	Main domain I^2C communication CRC issue
		0 No error
		1 Error detected in the I^2C CRC
		Reset condition: POR / clear on write (write 1)
8	I2C_M_REQ	Invalid main domain I^2C access (wrong Write or Read, Write to INIT registers in normal mode, wrong address)
		0 No error
		1 I^2C violation
		Reset condition: POR / clear on Write (write 1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

10.4 M_MODE register

Table 9. M_MODE register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_ LOCK_RT
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	EXT_ FIN_DIS	0	0	0	W2DIS	W1DIS	GoToSTBY
Read	EXT_FIN_ SEL_RT	RESERVED	MAIN_ NORMAL	RESERVED	RESERVED	W2DIS	W1DIS	RESERVED
Reset	0	0	1	0	0	0	0	0

Table 10. M_MODE register bit description

Bit	Symbol	Description
16	PLL_LOCK_RT	Real time status of the PPL
		0 PLL not locked
		1 PLL locked
		Reset condition: POR
15	EXT_FIN_SEL_RT	Real time status of FIN clock selection
		0 Internal clock oscillator is selected
		1 External FIN clock is selected
		Reset condition: POR
14	EXT_FIN_DIS	Disable request of EXT FIN selection at PLL input
		0 No effect
		1 Disable FIN selection
		Reset condition: POR
13	MAIN_NORMAL	Main state machine status
		0 Main state machine is not in Normal mode
		1 Main state machine is in Normal mode
		Reset condition: POR
10	W2DIS	WAKE2 wake up disable
		0 wake up enable
		1 wake up disable
		Reset condition: POR
9	W1DIS	WAKE1 wake up disable
		0 Wake up enable
		1 Wake up disable
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 10. M_MODE register bit description*...continued*

Bit	Symbol	Description
8	GOTOSTBY	Standby mode request
		0 Device remains in current state
		1 Device enters in Standby mode
		Reset condition: n.a.

10.5 M_REG_CTRL1 register

Table 11. M_REG_CTRL1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VPRE_PD_DIS	VPDIS	0	BUCK1DIS	0	BUCK3DIS	LDO1DIS	0
Read	VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	VPEN	0	BUCK1EN	0	BUCK3EN	LDO1EN	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 12. M_REG_CTRL1 register bit description

Bit	Symbol	Description
23	VPRE_PD_DIS	Force disable of VPRE pull down
		0 No effect (VPRE pull down is automatically controlled by the logic)
		1 VPRE pull down disable request
		Reset condition: POR
22	VPDIS	Disable request of VPRE
		0 No effect (regulator remains in existing state)
		1 VPRE disable request
		Reset condition: POR
20	BUCK1DIS	Disable request of BUCK1
		0 No effect (regulator remains in existing state)
		1 BUCK1 disable request
		Reset condition: POR
18	BUCK3DIS	Disable request of BUCK3
		0 No effect (regulator remains in existing state)
		1 BUCK3 disable request
		Reset condition: POR
17	LDO1DIS	Disable request of LDO1
		0 No effect (regulator remains in existing state)
		1 LDO1 disable request
		Reset condition: POR
14	VPEN	Enable request of VPRE

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 12. M_REG_CTRL1 register bit description*...continued*

Bit	Symbol	Description
		0 No effect (regulator remains in existing state)
		1 VPRE enable request (after a VPDIS request)
		Reset condition: POR
12	BUCK1EN	Enable request of BUCK1
		0 No effect (regulator remains in existing state)
		1 BUCK1 enable request
		Reset condition: POR
10	BUCK3EN	Enable request of BUCK3
		0 No effect (regulator remains in existing state)
		1 BUCK3 enable request
		Reset condition: POR
9	LDO1EN	Enable request of LDO1
		0 No effect (regulator remains in existing state)
		1 LDO1 enable request
		Reset condition: POR

10.6 M_REG_CTRL2 register

Table 13. M_REG_CTRL2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	BUCK1T SDCFG	0	BUCK3T SDCFG	LDO1T SDCFG	0
Read	RESERVED	RESERVED	RESERVED	BUCK1T SDCFG	RESERVED	BUCK3T SDCFG	LDO1T SDCFG	RESERVED
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	VPRESRLS[1:0]		0	VPRESRHS[1:0]	
Read	RESERVED	RESERVED	RESERVED	VPRESRLS[1:0]		RESERVED	VPRESRHS[1:0]	
Reset	0	0	0	1	1	0	OTP	OTP

Table 14. M_REG_CTRL2 register bit description

Bit	Symbol	Description
20	BUCK1TSDCFG	BUCK1 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
18	BUCK3TSDCFG	BUCK3 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 14. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Description
17	LDO1TSDCFG	LDO1 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
12 to 11	VPRESRLS[1:0]	VPRE low-side slew rate control
		00 130 mA typical drive capability - slow
		01 260 mA typical drive capability - medium
		10 520 mA typical drive capability - fast
		11 900 mA typical drive capability - ultra fast
		Reset condition: POR
9 to 8	VPRESRHS[1:0]	VPRE high-side slew rate control
		00 130 mA typical drive capability - slow
		01 260 mA typical drive capability - medium
		10 520 mA typical drive capability - fast
		11 900 mA typical drive capability - ultra fast
		Reset condition: POR

10.7 M_CLOCK register

Table 15. M_CLOCK register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
Read	MOD_CONF	FOUT_MUX_SEL[3:0]				FOUT_PHASE[2:0]		
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	FOUT_ CLK_SEL	EXT_ FIN_SEL	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
Read	FOUT_ CLK_SEL	RESERVED	FIN_DIV	MOD_EN	CLK_TUNE[3 :0]			
Reset	0	0	0	0	0	0	0	0

Table 16. M_CLOCK register bit description

Bit	Symbol	Description
23	MOD_CONF	Modulation configuration of main oscillator
		0 range ± 5 % 23 kHz
		1 range ± 5 % 94 kHz
		Reset condition: POR
22 to 19	FOUT_MUX_SEL[3:0]	See Table 68

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 16. M_CLOCK register bit description*...continued*

Bit	Symbol	Description
18 to 16	FOUT_PHASE[2:0]	FOUT phase shifting configuration (see Section 18.2 "Phase shifting")
		000 No shift
		001 Shifted by 1 clock cycle of CLK running at 20 MHz
		010 Shifted by 2 clock cycle of CLK running at 20 MHz
		011 Shifted by 3 clock cycle of CLK running at 20 MHz
		100 Shifted by 4 clock cycle of CLK running at 20 MHz
		101 Shifted by 5 clock cycle of CLK running at 20 MHz
		110 Shifted by 6 clock cycle of CLK running at 20 MHz
		111 Shifted by 7 clock cycle of CLK running at 20 MHz
		Reset condition: POR
15	FOUT_CLK_SEL	FOUT_clk frequency selection (CLK1 or CLK2)
		0 FOUT_clk = CLK1
		1 FOUT_clk = CLK2
		Reset condition: POR
14	EXT_FIN_SEL	Enable request of EXT FIN selection at PLL input
		0 No effect
		1 FIN selection request
		Reset condition: POR
13	FIN_DIV	FIN input signal divider selection
		0 Divider by 1
		1 Divider by 6
		Reset condition: POR
12	MOD_EN	Modulation activation of main oscillator
		0 Modulation disabled
		1 Modulation enabled
		Reset condition: POR
11 to 8	CLK_TUNE[3:0]	See Table 67

10.8 M_INT_MASK1 register

Table 17. M_INT_MASK1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	VPREOC_M	0	BUCK1OC_M	0	BUCK3OC_M	LDO1OC_M	0
Read	RESERVED	VPREOC_M	RESERVED	BUCK1OC_M	RESERVED	BUCK3OC_M	LDO1OC_M	RESERVED
Reset	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	BUCK1TSD_M	0	BUCK3TSD_M	LDO1TSD_M	0
Read	RESERVED	RESERVED	RESERVED	BUCK1TSD_M	RESERVED	BUCK3TSD_M	LDO1TSD_M	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 18. M_INT_MASK1 register bit description

Bit	Symbol	Description
22	VPREOC_M	Inhibit INTERRUPT for VPRE overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
20	BUCK1OC_M	Inhibit INTERRUPT for BUCK1 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
18	BUCK3OC_M	Inhibit INTERRUPT for BUCK3 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
17	LDO1OC_M	Inhibit INTERRUPT for LDO1 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
12	BUCK1TSD_M	Inhibit INTERRUPT for BUCK1 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
10	BUCK3TSD_M	Inhibit INTERRUPT for BUCK3 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
9	LDO1TSD_M	Inhibit INTERRUPT for LDO1 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

10.9 M_INT_MASK2 register

Table 19. M_INT_MASK2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	VBOSUVH_M	COM_M	VPRE_FB_OV_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VBOSUVH_M	COM_M	VPRE_FB_OV_M
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	VSUPUV7_M	0	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Read	RESERVED	VSUPUV7_M	RESERVED	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Reset	0	0	0	0	0	0	0	0

Table 20. M_INT_MASK2 register bit description

Bit	Symbol	Description
18	VBOSUVH_M	Inhibit INTERRUPT for VBOS_UVH any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
17	COM_M	Inhibit INTERRUPT for COM any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
16	VPRE_FB_OV_M	Inhibit INTERRUPT for VPRE_FB_OV
		0 INT not masked
		1 INT masked
		Reset condition: POR
14	VSUPUV7_M	Inhibit INTERRUPT for VSUP_UV7
		0 INT not masked
		1 INT masked
		Reset condition: POR
12	VREUVH_M	Inhibit INTERRUPT for VSUP_UVH
		0 INT not masked
		1 INT masked
		Reset condition: POR
11	VSUPUVL_M	Inhibit INTERRUPT for VSUP_UVL
		0 INT not masked
		1 INT masked
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 20. M_INT_MASK2 register bit description*...continued*

Bit	Symbol	Description
10	VSUPUVH_M	Inhibit INTERRUPT for VPRE_UVH
		0 INT not masked
		1 INT masked
		Reset condition: POR
9	WAKE1_M	Inhibit INTERRUPT for WAKE1 any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
8	WAKE2_M	Inhibit INTERRUPT for WAKE2 any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR

10.10 M_FLAG1 register

Table 21. M_FLAG1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VBOSUVH	0	VPREOC	BUCK1OC	0	BUCK3OC	LDO1OC	0
Read	VBOSUVH	RESERVED	VPREOC	BUCK1OC	RESERVED	BUCK3OC	LDO1OC	RESERVED
Reset	1	1	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	BUCK1OT	0	BUCK3OT	LDO1OT	0
Read	CLK_FIN_ DIV_OK	RESERVED	RESERVED	BUCK1OT	RESERVED	BUCK3OT	LDO1OT	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 22. M_FLAG1 register bit description

Bit	Symbol	Description
23	VBOSUVH	VBOS undervoltage high event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
21	VPREOC	VPRE overcurrent event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
20	BUCK1OC	BUCK1 overcurrent event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 22. M_FLAG1 register bit description*...continued*

Bit	Symbol	Description
18	BUCK3OC	BUCK3 overcurrent
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
17	LDO1OC	LDO1 overcurrent
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
15	CLK_FIN_DIV_OK	CLK_FIN_DIV monitoring
		0 Not OK: FIN_{ERR_LONG} < CLK_FIN_DIV deviation < FIN_{ERR_SHORT}
		1 OK: FIN_{ERR_SHORT} < CLK_FIN_DIV deviation < FIN_{ERR_LONG}
		Reset condition: Real time information
12	BUCK1OT	BUCK1 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
10	BUCK3OT	BUCK3 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
9	LDO1OT	LDO1 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)

10.11 M_FLAG2 register

Table 23. M_FLAG2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VPRE_FB_OV	VSUPUV7	0	0	0	0	0	0
Read	VPRE_FB_OV	VSUPUV7	RESERVED	BUCK1_ST	RESERVED	BUCK3_ST	LDO1_ST	RESERVED
Reset	0	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
Write	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
Read	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
Reset	1	1	1	1	0	1	0	1

Note: *Reset value for FS5502, wake up by Wake1, all regulators started by default during power up sequence.*

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 24. M_FLAG2 register bit description

Bit	Symbol	Description
23	VPRE_FB_OV	VPRE_FB_OV event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
22	VSUPUV7	VSUP_UV7 event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
20	BUCK1_ST	BUCK1 state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real time information
18	BUCK3_ST	BUCK3 state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real time information
17	LDO1_ST	LDO1 state
		0 regulator OFF
		1 regulator ON
		Reset condition: Real time information
15	VPREUVL	VPRE_UVL event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
14	VPREUVH	VPRE_UVH event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
13	VSUPUVL	VSUP_UVL event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
12	VSUPUVH	VSUP_UVH event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
11	WK2RT	Report event: WAKE2 real time state
		0 WAKE2 is low level
		1 WAKE2 is high
		Reset condition: Real time information

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 24. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description
10	WK1RT	Report event: WAKE1 real time state
		0 WAKE1 is low level
		1 WAKE1 is high
		Reset condition: Real time information
9	WK2FLG	WAKE2 wake up source flag
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)
8	WK1FLG	WAKE1 wake up source flag
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write 1)

10.12 M_VMON_REGx register

Table 25. M_VMON_REGx register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	VMON1_REG[2:0]		
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VMON1_REG[2:0]		
Reset	0	0	0	0	0	0	0	0

Table 26. M_VMON_REGx register bit description

Bit	Symbol	Description
10 to 8	VMON1_REG[2:0]	Regulator assignment to VMON1
		000 External regulator
		001 VPRE
		010 LDO1
		011 RESERVED
		100 RESERVED
		101 BUCK3
		11x External regulator
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

10.13 M_LVB1_SVS register

Table 27. M_LVB1_SVS register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	RESERVED	RESERVED	RESERVED	LVB1_SVS[4:0]				
Reset	0	0	0	0	0	0	0	0

Table 28. M_LVB1_SVS register bit description

Bit	Symbol	Description
12 to 8	LVB1_SVS[4:0]	Static voltage scaling negative offset
		00000 0 mV
		00001 −6.25 mV
		00010 −12.50 mV
		00011 −18.75 mV
		00100 −25 mV
		00101 −31.25 mV
		00110 −37.5 mV
		00111 −43.75 mV
		01000 −50 mV
		01001 −56.25 mV
		01010 −62.5 mV
		01011 −68.75 mV
		01100 −75 mV
		01101 −81.25 mV
		01110 −87.5 mV
		01111 −93.75 mV
		10000 −100 mV
		Reset condition: POR

10.14 M_MEMORY0 register

Table 29. M_MEMORY0 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MEMORY0[15:8]							
Read	MEMORY0[15:8]							
Reset	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Bit	15	14	13	12	11	10	9	8
Write	MEMORY0[7:0]							
Read	MEMORY0[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 30. M_MEMORY0 register bit description

Bit	Symbol	Description
23 to 8	MEMORY0[15:0]	Free memory field for data storage
		0... 16 bits free memory
		...1
		Reset condition: POR

10.15 M_MEMORY1 register

Table 31. M_MEMORY1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MEMORY1[15:0]							
Read	MEMORY1[15:0]							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	MEMORY1[15:0]							
Read	MEMORY1[15:0]							
Reset	0	0	0	0	0	0	0	0

Table 32. M_MEMORY1 register bit description

Bit	Symbol	Description
23 to 8	MEMORY1[15:0]	Free memory field for data storage
		0… 16 bits free memory
		…1
		Reset condition: POR

10.16 M_DEVICEID register

Table 33. M_DEVICEID register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	FMREV[3:0]				MMREV[3:0]			
Reset	0	0	1	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	DEVICEID[7:0]							
Reset	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 34. M_DEVICEID register bit description

Bit	Symbol	Description
23 to 20	FMREV[3:0]	Full mask revision
		Full mask revision configured by metal connection
		Reset condition: POR
19 to 16	MMREV[3:0]	Metal mask revision
		Full mask revision configured by metal connection
		Reset condition: POR
15 to 8	DEVICEID[7:0]	Device ID
		x…x Device ID from OTP_DEVICEID[7:0] bits
		Reset condition: POR

11 Fail-safe register mapping

11.1 Fail-safe writing registers overview

Table 35. Fail-safe writing registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Fail-safe	FS_I_OVUV_SAFE_REACTION1	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		0	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	0	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
	FS_I_OVUV_SAFE_REACTION2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		0	RESERVED	RESERVED	0	RSTB_DUR	0
		RESERVED	0	RESERVED	DIS_8s	0	0	0	0
	FS_I_SVS	SVS_OFFSET[4:0]					0	0	0
		0	0	0	0	0	0	0	0
	FS_OVUVREG_STATUS	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	VMON1_OV	VMON1_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
	FS_RELEASE_FS0B	RELEASE_FS0B[15:8]							
		RELEASE_FS0B[7:0]							
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_EVENT	0	EXT_RSTB	0	0	RSTB_EVENT	RSTB_DIAG
		RSTB_REQ	0	0	0	0	0	0	0
	FS_DIAG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	I2C_FS_CRC	I2C_FS_REQ	RESERVED
	FS_INTB_MASK	0	0	0	0	0	0	RESERVED	RESERVED
		RESERVED	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	RESERVED	RESERVED	RESERVED	RESERVED
	FS_STATES	0	DBG_EXIT	0	0	OTP_CORRUPT	0	REG_CORRUPT	0
		0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

11.2 Fail-safe reading registers overview

Table 36. Fail-safe reading registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Fail-safe	FS_GRL_FLAGS	FS_COM_G	RESERVED	FS_IO_G	FS_REG_ OVUV_G	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	FS_I_OVUV_ SAFE_REACTION1	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
	FS_I_OVUV_ SAFE_REACTION2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	RESERVED	RESERVED	RESERVED	RSTB_DUR	RESERVED
		RESERVED	RESERVED	RESERVED	DIS_8s	FLT_ERR_CNT[3:0]			
	FS_I_SVS	SVS_OFFSET[4:0]					RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	FS_OVUVREG_ STATUS	VCOREMON_ OV	VCOREMON_ UV	VDDIO_OV	VDDIO_UV	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	VMON1_OV	VMON1_UV	RESERVED	FS_DIG_ REF_OV	FS_OSC_DRIFT	RESERVED
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_ EVENT	PGOOD_SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_EVENT	RSTB_DIAG
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	FS_DIAG	RESERVED	RESERVED	RESERVED	RESERVED	ERRMON	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	I2C_FS_CRC	I2C_FS_REQ	RESERVED
	FS_INTB_MASK	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	INT_INH_ VMON1_OV_UV	INT_INH_ VDDIO_OV_UV	INT_INH_ VCOREMON_ OV_UV	RESERVED	RESERVED	RESERVED	RESERVED
	FS_STATES	RESERVED	RESERVED	DBG_MODE	RESERVED	OTP_ CORRUPT	RESERVED	REG_ CORRUPT	RESERVED
		RESERVED	RESERVED	RESERVED	FSM_STATE[4:0]				

11.3 FS_GRL_FLAGS register

Table 37. FS_GRL_FLAGS register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	FS_COM_G	RESERVED	FS_IO_G	FS_REG_ OVUV_G	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 38. FS_GRL_FLAGS register bit description

Bit	Symbol	Description
23	FS_COM_G	Report an issue in the communication (I2C) **FS_COM_G** = I2C_FS_CRC or I2C_FS_REQ
		0 No failure
		1 Failure
		Reset condition: Real time information - cleared when all individual bits are cleared

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 38. FS_GRL_FLAGS register bit description*...continued*

Bit	Symbol	Description
21	FS_IO_G	Report an issue in one of the fail-safe IOs **FS_IO_G** = PGOOD_DIAG or RSTB_DIAG
		0 No failure
		1 Failure
		Reset condition: real time information - cleared when all individual bits are cleared
20	FS_REG_OVUV_G	Report an issue in one of the voltage monitoring (OV or UV) **FS_REG_OVUV_G** = VCOREMON_OV or VCOREMON_UV or VDDIO_OV or VDDIO_UV or VMON1_OV or VMON1_UV
		0 No failure
		1 Failure
		Reset condition: real time information - cleared when all individual bits are cleared

11.4 FS_I_OVUV_SAFE_REACTION1 register

Table 39. FS_I_OVUV_SAFE_REACTION1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		0	RESERVED	RESERVED	RESERVED
Read	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		RESERVED	RESERVED	RESERVED	RESERVED
Reset	1	1	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	RESERVED	RESERVED	0	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
Read	RESERVED	RESERVED	RESERVED	RESERVED	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
Reset	0	0	0	0	1	1	0	1

Table 40. FS_I_OVUV_SAFE_REACTION1 register bit description

Bit	Symbol	Description
23 to 22	VCOREMON_OV_FS_IMPACT[1:0]	Table 81
21 to 20	VCOREMON_UV_FS_IMPACT[1:0]	Table 81
11 to 10	VDDIO_OV_FS_IMPACT[1:0]	Table 84
9 to 8	VDDIO_UV_FS_IMPACT[1:0]	Table 84

11.5 FS_I_OVUV_SAFE_REACTION2 register

Table 41. FS_I_OVUV_SAFE_REACTION2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	1	1	0	1	1	1	0	1

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	RESERVED	RESERVED	RESERVED	VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
Read	RESERVED	RESERVED	RESERVED	RESERVED	VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1

Table 42. FS_I_OVUV_SAFE_REACTION2 register bit description

Bit	Symbol	Description
11 to 10	VMON1_OV_FS_IMPACT[1:0]	See Table 86
9 to 8	VMON1_UV_FS_IMPACT[1:0]	

11.6 FS_I_FSSM register

Table 43. FS_I_FSSM register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	FLT_ERR_CNT_LIMIT[1:0]		0	RESERVED	RESERVED	0	RSTB_DUR	0
Read	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	RESERVED	RESERVED	RESERVED	RSTB_DUR	RESERVED
Reset	0	1	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	0	RESERVED	DIS_8s	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	DIS_8s	FLT_ERR_CNT[3:0]			
Reset	1	0	0	0	0	0	0	1

Table 44. FS_I_FSSM register bit description

Bit	Symbol	Description
23 to 22	FLT_ERR_CNT_LIMIT[1:0]	See Table 89
17	RSTB_DUR	RSTB pulse duration configuration
		0 10 ms
		1 1.0 ms
		Reset condition: POR
12	DIS_8s	Disable 8 s timer
		0 RSTB low 8 s counter enabled
		1 RSTB low 8 s counter disabled
		Reset condition: POR

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 44. FS_I_FSSM register bit description*...continued*

Bit	Symbol	Description
11 to 8	FLT_ERR_CNT[3:0]	Reflect the value of the fault error counter
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12
		Reset condition: Real time information

11.7 FS_I_SVS register

Table 45. FS_I_SVS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	SVS_OFFSET[4:0]					0	0	0
Read	SVS_OFFSET[4:0]					RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 46. FS_I_SVS register bit description

Bit	Symbol	Description
23 to 19	SVS_OFFSET[4:0]	Static voltage scaling negative offset
		0 0000 0 mV
		0 0001 −6.25 mV
		0 0010 −12.50 mV
		0 0011 −18.75 mV
		0 0100 −25 mV
		0 0101 −31.25 mV
		0 0110 −37.5 mV
		0 0111 −43.75 mV
		0 1000 −50 mV
		0 1001 −56.25 mV
		0 1010 −62.5 mV
		0 1011 −68.75 mV
		0 1100 −75 mV
		0 1101 −81.25 mV
		0 1110 −87.5 mV
		0 1111 −93.75 mV
		1 0000 −100 mV
		Reset condition: POR

11.8 FS_OVUVREG_STATUS register

Table 47. FS_OVUVREG_STATUS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	RESERVED	RESERVED	RESERVED	RESERVED
Read	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	1	0	1	0	1	0	1

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	RESERVED	VMON1_OV	VMON1_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
Read	RESERVED	RESERVED	VMON1_OV	VMON1_UV	RESERVED	FS_DIG_REF_OV	FS_OSC_DRIFT	RESERVED
Reset	0	1	0	1	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 48. FS_OVUVREG_STATUS register bit description

Bit	Symbol	Description
23	VCOREMON_OV	Overvoltage monitoring on VCOREMON
		0 No overvoltage
		1 Overvoltage reported on VCOREMON
		Reset condition: POR / clear on write (write 1)
22	VCOREMON_UV	Undervoltage monitoring on VCOREMON
		0 No undervoltage
		1 Undervoltage reported on VCOREMON
		Reset condition: POR / clear on write (write 1)
21	VDDIO_OV	Overvoltage monitoring on VDDIO
		0 No overvoltage
		1 Overvoltage reported on VDDIO
		Reset condition POR / clear on write (write 1)
20	VDDIO_UV	Undervoltage monitoring on VDDIO
		0 No undervoltage
		1 Undervoltage reported on VDDIO
		Reset condition: POR / clear on write (write 1)
13	VMON1_OV	Overvoltage monitoring on VMON1
		0 No overvoltage
		1 Overvoltage reported on VMON1
		Reset condition: POR / clear on write (write 1)
12	VMON1_UV	Undervoltage monitoring on VMON1
		0 No undervoltage
		1 Undervoltage reported on VMON1
		Reset condition: POR / clear on write (write 1)
10	FS_DIG_REF_OV	Overvoltage of the internal digital fail-safe reference voltage
		0 No overvoltage
		1 Overvoltage reported of the internal digital fail-safe reference voltage
		Reset condition: POR / clear on write (write 1)
9	FS_OSC_DRIFT	Drift of the fail-safe OSC
		0 No drift
		1 Oscillator drift
		Reset condition: POR / clear on write (write 1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

11.9 FS_SAFE_IOs register

Table 49. FS_SAFE_IOS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	PGOOD_ DIAG	PGOOD_ EVENT	0	EXT_RSTB	0	0	RSTB_ EVENT	RSTB_DIAG
Read	PGOOD_ DIAG	PGOOD_ EVENT	PGOOD_ SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_ EVENT	RSTB_DIAG
Reset	0	1	0	0	0	0	1	0

Bit	15	14	13	12	11	10	9	8
Write	RSTB_REQ	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 50. FS_SAFE_IOS register bit description

Bit	Symbol	Description
23	PGOOD_DIAG	Report a PGOOD Short to High
		0 No failure
		1 Short circuit HIGH
		Reset condition: POR / clear on write (write 1)
22	PGOOD_EVENT	Report a Power GOOD event
		0 No Power GOOD
		1 Power GOOD event occurred
		Reset condition: POR / clear on write (write 1)
21	PGOOD_SNS	Sense of PGOOD pad
		0 PGOOD pad sensed low
		1 PGOOD pad sensed high
		Reset condition: Real time information
20	EXT_RSTB	Report an external RESET
		0 No external RESET
		1 External RESET
		Reset condition: POR / clear on write (write 1)
19	RSTB_DRV	RSTB driver – digital command
		0 RSTB driver command sensed low
		1 RSTB driver command sensed high
		Reset condition: Real time information
18	RSTB_SNS	Sense of RSTB pad
		0 RSTB pad sensed low
		1 RSTB pad sensed high
		Reset condition: Real time information

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 50. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description
17	RSTB_EVENT	Report a RSTB event
		0 No RESET
		1 RESET occurred
		Reset condition: POR / clear on write (write 1)
16	RSTB_DIAG	Report a RSTB short to high
		0 No failure
		1 Short circuit high
		Reset condition: POR / clear on write (write 1)
15	RSTB_REQ	Request assertion of RSTB (Pulse)
		0 No assertion
		1 RSTB assertion (pulse)
		Reset condition: POR

11.10 FS_DIAG register

Table 51. FS_DIAG register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	I2C_FS_CRC	I2C_FS_REQ	RESERVED
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	I2C_FS_CRC	I2C_FS_REQ	RESERVED
Reset	1	0	0	0	0	0	0	1

Table 52. FS_DIAG register bit description

Bit	Symbol	Description
10	I2C_FS_CRC	Fail-safe I^2C communication CRC issue
		0 No error
		1 Error detected in the CRC
		Reset condition: POR / clear on write (write 1)
9	I2C_FS_REQ	Invalid fail-safe I^2C access (wrong write or read, write to INIT registers in normal mode, wrong address)
		0 No error
		1 I^2C violation
		Reset condition: POR / clear on write (write 1)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

11.11 FS_INTB_MASK register

Table 53. FS_INTB_MASK register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	RESERVED	RESERVED
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	RESERVED	RESERVED	RESERVED	RESERVED
Read	RESERVED	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 54. FS_INTB_MASK register bit description

Bit	Symbol	Description
14	INT_INH_VMON1_OV_UV	Inhibit INTERRUPT on VMON1 OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
13	INT_INH_VDDIO_OV_UV	Inhibit INTERRUPT on VDDIO OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
12	INT_INH_VCOREMON_OV_UV	Inhibit INTERRUPT on VCOREMON OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR

11.12 FS_STATES register

Table 55. FS_STATES register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	DBG_EXIT	0	0	OTP_CORRUPT	0	REG_CORRUPT	0
Read	RESERVED	RESERVED	DBG_MODE	RESERVED	OTP_CORRUPT	RESERVED	REG_CORRUPT	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	FSM_STATE[4:0]				
Reset	0	0	0	0	0	1	1	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 56. FS_STATES register bit description

Bit	Symbol	Description
22	DBG_EXIT	Leave DEBUG mode
		0 No action
		1 Leave DEBUG mode
		Reset condition: POR
21	DBG_MODE	DEBUG mode status
		0 NOT in DEBUG mode
		1 In DEBUG mode
		Reset condition: Real time information
19	OTP_CORRUPT	OTP bits corruption detection (5 ms cyclic check)
		0 No error
		1 OTP CRC error detected
		Reset condition: POR / clear on write (write 1)
16 7	REG_CORRUPT	INIT register corruption detection (real time comparison)
		0 No error
		1 INIT register content error detected (mismatch between FS_I_Register / FS_I_NOT_ Register)
		Reset condition: POR / clear on write (write 1)
12 to 8	FSM_STATE[4:0]	Report fail-safe state machine current state
		0 0110 INIT_FS
		Reset condition: Real time information

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

12 OTP bits configuration

12.1 Overview

Table 57. Main OTP_REGISTERS

*Legend: **bold** — Regulator behavior in case of TSD and VPRE slew rate parameters can be changed later by I^2C.*

Name	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_VPRE_1	14	0	0	VPREV[5:0]					
OTP_CFG_VPRE_2	15	0	0	VPRESC[5:0]					
OTP_CFG_VPRE_3	16	VPREILIM[1:0]		1	0	1	1	**VPRESRHS[1:0]**	
OTP_CFG_BOOST_1	17	0	0	0	0	0000			
OTP_CFG_BOOST_2	18	0	00		00000				
OTP_CFG_BOOST_3	19	0	0	0	0	0	1	00	
OTP_CFG_BUCK1_1	1A	VB1V[7:0]							
OTP_CFG_BUCK1_2	1B	0	0	0	VB1INDOPT[1:0]		VB1SWILIM[1:0]		0
OTP_CFG_BUCK1_3	1C	00000000							
OTP_CFG_BUCK1_4	1D	0	00		0	00		0	0
OTP_CFG_BUCK3_1	1E	BUCK3EN	VB3INDOPT[1:0]		VB3V[4:0]				
OTP_CFG_BUCK3_2	1F	000			VB1GMCOMP[2:0]			VB3SWILIM[1:0]	
OTP_CFG_LDO	20	0	000			LDO1ILIM	LDO1V[2:0]		
OTP_CFG_SEQ_1	21	0	0	111			VB1S[2:0]		
OTP_CFG_SEQ_2	22	0	0	111			LDO1S[2:0]		
OTP_CFG_SEQ_3	23	DVS_BUCK1[1:0]		DVS_BUCK3[1:0]		Tslot	VB3S[2:0]		
OTP_CFG_CLOCK_1	24	0	0	VPRE_ph[2:0]			1	0	0
OTP_CFG_CLOCK_2	25	0	0	BUCK1_ph[2:0]			000		
OTP_CFG_CLOCK_3	26	0	0	BUCK3_ph[2:0]			000		
OTP_CFG_CLOCK_4	27	BUCK3_ clk_sel	0	BUCK1_ clk_sel	0	VPRE_clk_sel	PLL_sel	0	1
OTP_CFG_SM_1	28	0	0	**conf_TSD[5:0]**					
OTP_CFG_SM_2	29	0	0	0	VPRE_off_dly	1	1	PSYNC_CFG	PSYNC_EN
OTP_CFG_VSUP_UV	2A	0	0	0	0	0	0	0	VSUPCFG
OTP_CFG_I2C	2B	0	0	0	0	M_I2CDEVADDR[3:0]			
OTP_CFG_OV	2C	0	0	0	0	0	VDDIO_REG_ASSIGN[2:0]		
OTP_CFG_DEVID	2D	DeviceID[7:0]							

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 58. Fail-safe OTP_REGISTERS

Name	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_UVOV_1	0A	VCORE_V[7:0]							
OTP_CFG_UVOV_2	0B	VDDIOOVTH[3:0]				VCOREOVTH[3:0]			
OTP_CFG_UVOV_3	0C	0	0	VDDIO_V	VCORE_SVS_CLAMP[4:0]				
OTP_CFG_UVOV_4	0D	0	0	0	0	VMON1OVTH[3:0]			
OTP_CFG_UVOV_5	0E	0	0	0	0	0	0	0	0
OTP_CFG_UVOV_6	0F	VDDIOUVTH[3:0]				VCOREUVTH[3:0]			
OTP_CFG_UVOV_7	10	0	0	0	0	VMON1UVTH[3:0]			
OTP_CFG_UVOV_8	11	0	0	0	0	0	0	0	0
OTP_CFG_PGOOD	12	0	PGOOD_RSTB	0	0	0	PGOOD_VMON1	PGOOD_VDDIO	PGOOD_VCORE
OTP_CFG_ABIST1	13	0	0	0	0	0	0	0	0
OTP_CFG_ASIL	14	1	0	0	0	0	0	0	VMON1_EN
OTP_CFG_I2C	15	0	0	0	0	FS_I2CDEVADDR[3:0]			
OTP_CFG_DGLT_DUR_1	16	0	0	VCORE_UV_DGLT[1:0]		VCORE_OV_DGLT	VDDIO_UV_DGLT[1:0]		VDDIO_OV_DGLT
OTP_CFG_DGLT_DUR_2	17	0	0	0	0	0	VMON1_UV_DGLT[1:0]		VMON1_OV_DGLT

12.2 Main OTP bit description

Table 59. Main OTP bit description

Address	Register	Bit	Symbol	Value	Description
14	OTP_CFG_VPRE_1	5 to 0	VPREV[5:0]		VPRE output voltage
				01 0111	4.1 V
				10 0000	5.0 V
15	OTP_CFG_VPRE_2	5 to 0	VPRESC[5:0]		VPRE slope compensation
				00 0100	40 mV/µs
				00 0101	50 mV/µs
				00 0110	60 mV/µs
				00 0111	70 mV/µs
				00 1000	80 mV/µs
				00 1001	90 mV/µs
				00 1010	100 mV/µs
				00 1110	140 mV/µs
				01 0001	170 mV/µs
				01 0100	200 mV/µs
				01 1000	240 mV/µs
16	OTP_CFG_VPRE_3	7 to 6	VPREILIM[1:0]		VPRE current limitation threshold
				00	50 mV
				01	80 mV
				10	120 mV
				11	150 mV
		3 to 2	VPRESRLS[1:0]		VPRE low-side slew rate control
				11	PU/PD/900 mA
		1 to 0	VPRESRHS[1:0]		VPRE high-side slew rate control
				00	PU/PD/130 mA
				01	PU/PD/260 mA
				10	PU/PD/520 mA
				11	PU/PD/900 mA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 59. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
1A	OTP_CFG_BUCK1_1	7 to 0	VB1V[7:0]		VBUCK1 output voltage
				0100 0000	0.8 V
				0100 0100	0.825 V
				0101 0000	0.9 V
				0101 1000	0.95 V
				0110 0000	1.0 V
				01100100	1.025 V
				0110 0101	1.03125 V
				0111 0000	1.1 V
				1000 0000	1.2 V
				1000 1000	1.25 V
				1001 0000	1.3 V
				1001 1000	1.35 V
				1010 0000	1.4 V
				1011 0000	1.5 V
				1011 0001	1.8 V
1B	OTP_CFG_BUCK1_2	4 to 3	VB1INDOPT[1:0]		BUCK1 inductor selection
				00	1 µH
				01	0.47 µH
				10	1.5 µH
		2 to 1	VB1SWILIM{1:0]		BUCK1 current limitation
				01	Reserved
				11	4.5 A
1E	OTP_CFG_BUCK3_1	7	BUCK3EN		BUCK3 enable
				0	Disabled
				1	Enabled
		6 to 5	VB3INDOPT[1:0]		BUCK3 inductor selection
				00	1 µH
				01	0.47 µH
				10	1.5 µH
		4 to 0	VB3V[4:0]		VBUCK3 output voltage
				0 0000	1.0 V
				0 0001	1.1 V
				0 0010	1.2 V
				0 0011	1.25 V
				0 0100	1.3 V
				0 0101	1.35 V
				0 0110	1.5 V
				0 0111	1.6 V
				0 1000	1.8 V
				0 1110	2.3 V
				1 0000	2.5 V
				1 0001	2.8 V
				1 0101	3.3 V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 59. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
1F	OTP_CFG_BUCK3_2	4 to 2	VB1GMCOMP[2:0]		BUCK1 compensation network
				001	16.25 GM
				010	32.5 GM
				011	48.75 GM
				100	65 GM
				101	81.25 GM
				110	97.5 GM
		1 to 0	VB3SWILIM[1:0]		BUCK3 current limitation
				01	2.6 A
				11	4.5 A
20	OTP_CFG_LDO	3	LDO1ILIM		VLDO1 current limitation
				0	400 mA
				1	150 mA
		2 to 0	LDO1V[2:0]		VLDO1 output voltage
				000	1.1 V
				001	1.2 V
				010	1.6 V
				011	1.8 V
				100	2.5 V
				101	2.8 V
				110	3.3 V
				111	5.0 V
21	OTP_CFG_SEQ_1	2 to 0	VB1S[2:0]		BUCK1 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by I^2C)
22	OTP_CFG_SEQ_2	2 to 0	LDO1S[2:0]		LDO1 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by I^2C)
23	OTP_CFG_SEQ_3	7 to 6	DVS_BUCK1[1:0]		BUCK1 soft start/stop configurability
				00	7.81 mV/µs
				01	3.13 mV/µs

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 59. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
				10	2.6 mV/µs
				11	2.23 mV/µs
		5 to 4	DVS_BUCK3[1:0]		BUCK3 soft start/stop configurability
				00	10.41 mV/µs
				01	3.47 mV/µs
				10	2.6 mV/µs
				11	2.08 mV/µs
		3	Tslot		Power up/down slot duration
				0	250 µs
				1	1.0 ms
		2 to 0	VB3S[2:0]		BUCK3 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and Stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by I2C)
24	OTP_CFG_CLOCK_1	5 to 3	VPRE_ph[2:0]		VPRE phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
25	OTP_CFG_CLOCK_2	5 to 3	BUCK1_ph[2:0]		VBUCK1 phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 59. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
26	OTP_CFG_CLOCK_3	5 to 3	BUCK3_ph[2:0]		VBUCK3 phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
27	OTP_CFG_CLOCK_4	7	BUCK3_clk_sel		BUCK3 clock selection
				0	CLK_DIV1 = 2.22 MHz
		6	BUCK2_clk_sel		BUCK2 clock selection
				0	CLK_DIV1 = 2.22 MHz
		5	BUCK1_clk_sel		BUCK1 clock selection
				0	CLK_DIV1 = 2.22 MHz
		4	VBST_clk_sel		VBOOST clock selection
				0	CLK_DIV1 = 2.22 MHz
		3	VPRE_clk_sel		VPRE clock selection
				0	CLK_DIV1 = 2.22 MHz
				1	CLK_DIV2 = 455 kHz
		2	PLL_sel		PLL enable
				0	Disabled
				1	Enabled
28	OTP_CFG_SM_1	5 to 0	conf_TSD[5]	RESERVED	
			conf_TSD[4]		BUCK1 behavior in case of TSD
				0	BUCK1 shutdown
				1	BUCK1 shutdown + DFS
			conf_TSD[3]	RESERVED	
			conf_TSD[2]		BUCK3 behavior in case of TSD
				0	BUCK3 shutdown
				1	BUCK3 Shutdown + DFS
			conf_TSD[1]		LDO1 behavior in case of TSD
				0	LDO1 shutdown
				1	LDO1 shutdown + DFS
			conf_TSD[0]	RESERVED	
29	OTP_CFG_SM_2	4	VPRE_off_dly		Delay to turn OFF VPRE at device power down
				0	250 µs
				1	32 ms
		1	PSYNC_CFG		Synchronization with 1x FS5502 or 1x PF82
				0	2x FS5502
				1	1x FS5502 and 1x PF82
		0	PSYNC_EN		Synchronization with two devices
				0	Disabled
				1	Enabled

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 59. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
2A	OTP_CFG_VSUP_UV	0	VSUP_CFG		VSUP undervoltage threshold configuration
				0	4.9 V for Vpre < 4.5 V
				1	6.2 V for Vpre > 4.5 V
2B	OTP_CFG_I2C	3 to 0	M_I2CDEVADDR[3:0]		Device I^2C address
				0000	Address D0
				…	...
				1111	Address D15
2C	OTP_CFG_OV	2 to 0	VDDIO_REG_ASSIGN[2:0]		Regulator assigned to VDDIO
				000	External regulator
				001	VPRE
				010	RESERVED
				011	LDO2
				100	BUCK3
				101	External regulator
				110	External regulator
				111	External regulator
2D	OTP_CFG_DEVID	7 to 0	DeviceID[7:0]		Device ID

12.3 Fail-safe OTP bit description

Table 60. Fail-safe OTP bit description

Address	Register	Bit	Symbol	Value	Description
0A	OTP_CFG_UVOV_1	7 to 0	VCORE_V[7:0]		VCORE (VBUCK1) monitoring voltage
				0100 0000	0.8 V
				0100 0100	0.825 V
				0101 0000	0.9 V
				0101 1000	0.95 V
				0110 0000	1 V
				01100100	1.025 V
				0110 0101	1.03125 V
				0110 0000	1.1 V
				1000 0000	1.2 V
				1000 1000	1.25 V
				1001 0000	1.3 V
				1001 1000	1.35 V
				1010 0000	1.4 V
				1011 0000	1.5 V
				1011 0001	1.8 V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 60. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0B	OTP_CFG_UVOV_2	7 to 4	VDDIOOVTH[3:0]		VDDIO overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
		3 to 0	VCOREOVTH[3:0]		VCOREMON overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
0C	OTP_CFG_UVOV_3	5	VDDIO_V		VDDIO voltage selection
				0	3.3 V
				1	5 V
0C	OTP_CFG_UVOV_3	4 to 0	VCORE_SVS_CLAMP[4:0]		SVS max value allowed (mask)
				00000	No SVS
				00001	2 steps available
				00011	4 steps available
				00111	8 steps available
				01111	16 steps available

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 60. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0D	OTP_CFG_UVOV_4	3 to 0	VMON1OVTH[3:0]		VMON1 overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 60. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0F	OTP_CFG_UVOV_6	7 to 4	VDDIOUVTH[3:0]		VDDIO undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %
		3 to 0	VCOREUVTH[3:0]		VCOREMON undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 60. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
10	OTP_CFG_UVOV_7	3 to 0	VMON1UVTH[3:0]		VMON1 undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %
12	OTP_CFG_PGOOD	6	PGOOD_RSTB		RSTB assignment to PGOOD
				0	Not assigned
				1	Assigned
		2	PGOOD_VMON1		VMON1 assignment to PGOOD
				0	Not assigned
				1	Assigned
		1	PGOOD_VDDIO		VDDIO assignment to PGOOD
				0	Not assigned
				1	Assigned
		0	PGOOD_VCORE		VCORE (BUCK1) assignment to PGOOD
				0	Not assigned
				1	Assigned
14	OTP_CFG_ASIL	0	VMON1_EN		VMON1 monitoring enable
				0	Disabled
				1	Enabled
15	OTP_CFG_I2C	3 to 0	FS_I2CDEVADDR[3:0]		Device I^2C address
				0000	Address D0
				…	…
				1111	Address D15

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 60. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
16	OTP_CFG_DGLT_DUR_1	5 to 4	VCORE_UV_DGLT[1:0]		VCORE undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		3	VCORE_OV_DGLT		VCORE overvoltage filtering time
				0	25 µs
				1	45 µs
		2 to 1	VDDIO_UV_DGLT[1:0]		VDDIO undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		0	VDDIO_OV_DGLT		VDDIO overvoltage filtering time
				0	25 µs
				1	45 µs
17	OTP_CFG_DGLT_DUR_2	2 to 1	VMON1_UV_DGLT[1:0]		VMON1 undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		0	VMON1_OV_DGLT		VMON1 overvoltage filtering time
				0	25 µs
				1	45 µs

13 Best of supply

13.1 Functional description

VBOS regulator manages the best of supply from VSUP and VPRE to efficiently generate 5.0 V output to supply the internal biasing of the device. VBOS is also the supply of VPRE high side.

VBOS undervoltage might not guarantee the full functionality of the device. Consequently, VBOS_UVL detection powers down the device.

V_{SUP_UV7} undervoltage threshold is used to enable the path from VSUP to VBOS when VSUP < V_{SUP_UV7} to have a low drop path from VSUP, while VPRE is going low and to power up the device when VPRE is not started. When VSUP > V_{SUP_UV7}, VBOS is forced to use VPRE to optimize the efficiency.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

13.2 Best of supply electrical characteristics

Table 61. Best of supply electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BOS}	Best of supply output voltage	3.3	5.0	5.25	V
V_{BOS_UVH}	VBOS undervoltage threshold high (VBOS rising)	4.1	—	4.5	V
V_{BOS_UVL}	VBOS undervoltage threshold low (VBOS falling)	3.2	—	3.4	V
T_{BOS_UV}	V_{BOS_UVH} and V_{BOS_UVL} filtering time	6.0	10	15	µs
V_{BOS_POR}	VBOS power on reset threshold	—	—	2.5	V
T_{BOS_POR}	V_{BOS_POR} filtering time	0.5	—	1.5	µs
I_{BOS}	Best of supply current capability	—	—	60	mA
C_{OUT_BOS}	Effective output capacitor	4.7	—	10	µF
	Output decoupling capacitor	—	0.1	—	µF

14 High voltage buck: VPRE

14.1 Functional description

VPRE block is a high voltage, synchronous, peak current mode buck controller. VPRE is working with external logical level NMOS in force PWM mode at 455 kHz and in Automatic Pulse Skipping (APS) mode at 2.22 MHz. The APS mode helps to maintain the correct output voltage at high input voltage by skipping some turn ON cycles of the HS FET below the minimum duty cycle. VPRE input voltage is naturally limited to $V_{SUP} = L_{PI_DCR} \times I_{PRE} + V_{PRE_UVL} / D_{MAX}$ with $D_{MAX} = 1 – (F_{PRE_SW} \times T_{PRE_OFF_MIN})$. A bootstrap capacitor is required to supply the gate drive circuit of the high-side NMOS. The output voltage is configurable by OTP from 3.3 V to 5.0 V, and the switching frequency is configurable by OTP at 455 kHz for 12 V and 24 V transportation applications or 2.22 MHz for 12 V automotive applications. The stability is ensured by an external Type 2 compensation network with slope compensation.

The output current is sensed via an external shunt in series with the inductor and the maximum current capability is defined by the external components (NMOS gate charge, inductor, shunt resistor), the gate driver current capability and the switching frequency. An overcurrent detection is implemented to protect the external MOSFETs. If an overcurrent is detected after the HS minimum TON time, the HS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on VPRE and/or one of the cascaded regulators.

The maximum input voltage is 60 V and allows operation in 24 V truck applications without external protection to sustain ISO 16750-2:2012 load dump pulse 5b. VPRE must be the input supply of the BUCK1. VPRE can be the input supply of BUCK3 and LDO1. VPRE can be the supply of local loads remaining inside the ECU.

By default, VPRE switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied at FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

V_{PRE_UVH}, V_{PRE_UVL} and $V_{PRE_FB_OV}$ thresholds are monitored from PRE_FB pin and manage some transitions of the main state machine described in Section 8.1 "Simplified functional state diagram".

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

14.2 Application schematic

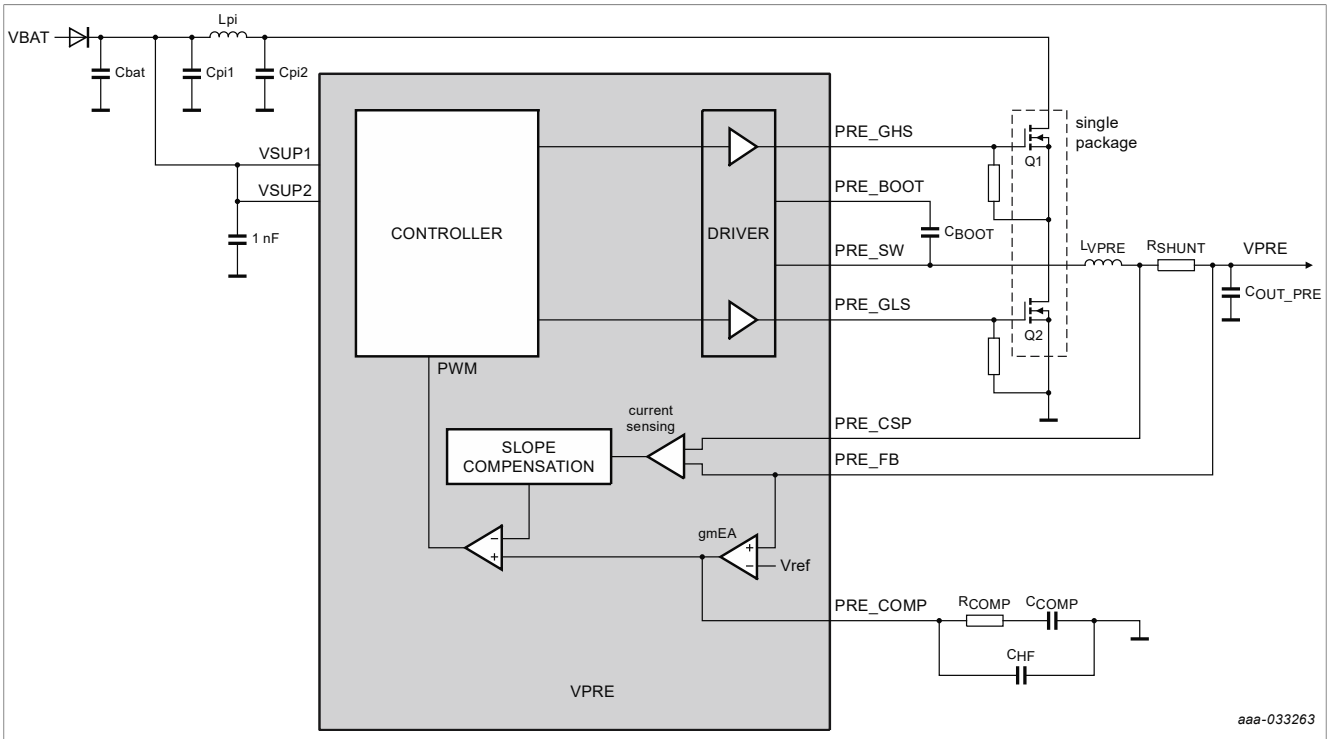


Figure 8. VPRE schematic

A PI filter, with F_{RES} = 1 / [2π x √(LCpi1)] and calculated for Fres < F_{PRE_SW} / 10, is required to filter VPRE switching frequency on the Battery line. VSUP1,2 pins must be connected before the PI filter for a clean biasing of the device. Cpi1 capacitor shall be implemented close to VSUP1,2 pins. Cpi2 capacitor shall be implemented close to Q1. The bootstrap capacitor value should be sized to be >10 times the gate source capacitor of Q1. Gate to source resistor on Q1 and Q2 is recommended in case of pin disconnection to guarantee a passive switch OFF of the transistors.

14.3 Compensation network and stability

The external compensation network, made with R_{COMP}, C_{COMP} and C_{HF} shall be calculated for best compromise between stability and transient response, based on below conceptual plot of Type 2 compensation network transfer function.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

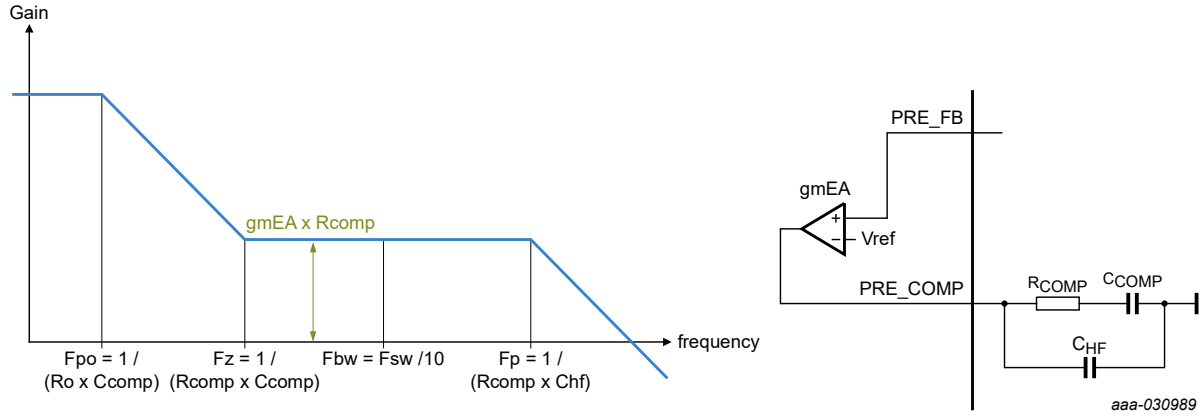


Figure 9. Type 2 compensation network concept

Calculation guideline

- System bandwidth for VPRE = 455 kHz: $F_{bw} = F_{PRE_SW} / 10$
  System bandwidth for VPRE = 2.22 MHz: $F_{bw} = F_{PRE_SW} / 15$
- Compensation zero: $Fz = F_{bw} / 10$
- Compensation pole for VPRE = 455 kHz: $Fp = F_{PRE_SW} / 2$
- Compensation pole for VPRE = 2.22 MHz: $Fp = F_{PRE_SW} / 4$
- $F_{GBW} = 1 / (2\pi \times R_{SHUNT} \times V_{PRE_LIM_GAIN} \times C_{OUT_PRE})$
- Error amplifier gain: $EA_gain = (V_{REF} / V_{PRE}) \times gmEA_{PRE} \times R_{COMP} = 10 \text{ ^ } LOG (F_{BW} / F_{GBW})$
- $V_{REF} = 1.0$ V, $R_{COMP} = V_{PRE} \times (EA_gain / gmEA_{PRE})$
- $C_{COMP} = 1 / (2\pi \times Fz \times R_{COMP})$
- $C_{HF} = 1 / (2\pi \times Fp \times R_{COMP})$
- Slope compensation: $Se > (V_{PRE} / L_{VPRE}) \times R_{SHUNT} \times V_{PRE_LIM_GAIN}$

The compensation network can be automatically calculated in the FS5502_OTP_Config.xlsm file which is using the same formulas. A Simplis simulation is recommended to verify the Phase and Gain Margin with normalized components.

Use case calculation with V_{PRE} = 4.1 V, L_{VPRE} = 6.8 µH, F_{PRE_SW} = 455 kHz, C_{OUT_PRE} = 66 µF, R_{SHUNT} = 10.0 mΩ

- System bandwidth: $F_{bw} = 45$ kHz
- Compensation zero: $Fz = 4.5$ kHz
- Compensation pole: $Fp = 227.5$ kHz
- $F_{GBW} = 53$ kHz
- Error amplifier gain: $EA_gain = 10 \text{ ^ } LOG (F_{BW} / F_{GBW}) = 0.86$
- $R_{COMP} = 2.34$ kΩ = 2.2 kΩ
- $C_{COMP} = 15.9$ nF = 16 nF
- $C_{HF} = 318$ pF = 330 pF
- Slope compensation: Se > 30 mV/µs

Use case stability verification

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

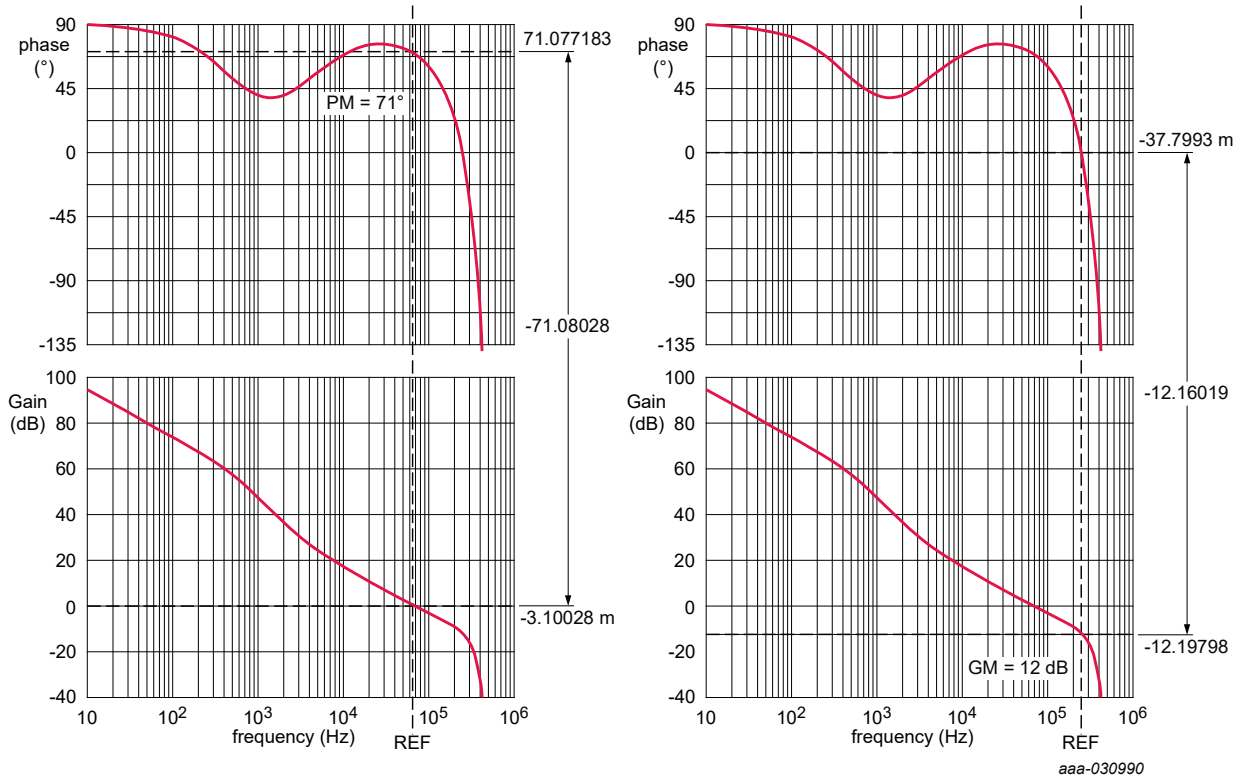


Figure 10. Phase and gain margin simulation

Use case transient response verification

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

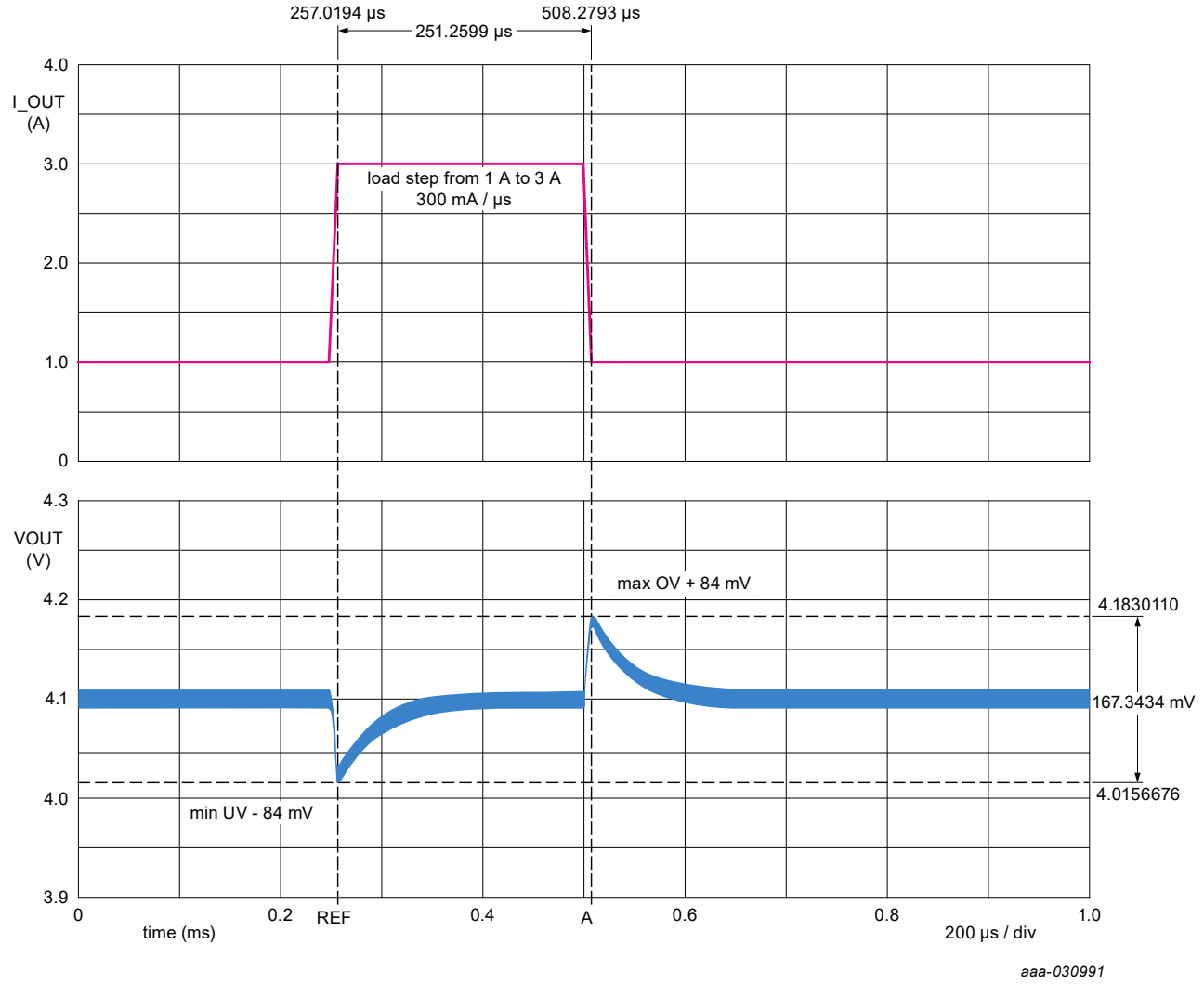


Figure 11. Transient response simulation

14.4 VPRE electrical characteristics

Table 62. VPRE electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{PRE}	Output voltage (OTP_VPREV[5:0] bits)	3.98	4.1	4.22	V
		4.85	5.0	5.15	V
$V_{PRE_SOFT_START}$	Output voltage from 10 % to 90 %	250	450	650	µs
	Digital DAC soft start completion	—	—	1.35	ms
$V_{PRE_STARTUP}$	Overshoot at startup	—	—	3	%
$V_{PRE_FB_OV}$	Overvoltage threshold protection	5.5	6.0	6.5	V
$T_{PRE_FB_OV}$	$V_{PRE_FB_OV}$ filtering time	1	2	3	µs
V_{PRE_UVH}	Undervoltage threshold high	2.9	—	3.1	V
V_{PRE_UVL}	Undervoltage threshold low	2.5	—	2.7	V
T_{PRE_UV}	V_{PRE_UVH} and V_{PRE_UVL} filtering time	6.0	10	15	µs
F_{PRE_SW}	Switching frequency range (OTP_VPRE_clk_sel bit)	430	455	480	kHz
		2.1	2.22	2.35	MHz

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 62. VPRE electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
L_{VPRE}	Inductor for F_{PRE_SW} = 455 kHz	4.7	6.8	10	µH
	Inductor for F_{PRE_SW} = 2.55 MHz	1.5	2.2	4.7	µH
$V_{PRE_LOAD_REG_455k}$	Transient load regulation at 455 kHz VSUP = 6.0 V to 36 V (L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, from 1.0 A to 3.0 A, di/dt = 300 mA/µs)	−3	—	3	%
$V_{PRE_LOAD_REG_2.2M}$	Transient load regulation at 2.22 MHz VSUP = 6.0 V to 18 V (L_{VPRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, from 1.0 A to 3.0 A, di/dt = 300 mA/µs)	−3	—	3	%
$V_{PRE_LINE_REG_455k}$	Transient line regulation at 455 kHz VSUP = 6.0 V to 18 V and VSUP = 12 V to 36 V (Cin = 47 µF + PI filter, L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, dv/dt = 100 mV/µs)	−3	—	3	%
$V_{PRE_LINE_REG_2.2M}$	Transient line regulation at 2.2 MHz VSUP = 6.0 V to 18 V (Cin = 47 µF + PI filter, L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 44 µF, dv/dt = 100 mV/µs)	−3	—	3	%
$V_{PRE_RIPPLE_455k}$	Ripple at 455 kHz VSUP = 12 V and VSUP = 24 V (L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, V_{PRE} = 3.3 V and 5.0 V, I_{PRE} = 4.0 A)	1	—	1	%
$V_{PRE_RIPPLE_2.2M}$	Ripple at 2.22 MHz VSUP = 12 V (LVPRE = 2.2 µH, C_{OUT_PRE} = 44 µF, VPRE = 3.3 V and 5.0 V, I_{PRE} = 2.0 A	−0.5	—	0.5	%
$T_{PRE_ON_MIN}$	HS minimum ON time	15	25	35	ns
$T_{PRE_OFF_MIN}$	HS minimum OFF time	20	40	60	ns
R_{SHUNT}	Current sense resistor (±1 %)	10	—	20	mΩ
$V_{PRE_LIM_GAIN}$	Current sense amplifier gain	4.5	5	5.5	
$V_{PRE_LIM_TH1}$	Current sense amplifier peak detection threshold (OTP_VPREILIM[1:0] bits)	37	50	63	mV
		60.8	80	99.2	mV
		93.6	120	146.4	mV
		117	150	183	mV
I_{LIM_PRE}	$I_{LIM_PRE} = V_{PRE_LIM_TH} / R_{SHUNT}$ Inductor peak current limitation range (R_{SHUNT} = 10 mΩ, $V_{PRE_LIM_TH1}$ = 50 mV)	3.75	5.0	6.25	A
	Inductor peak current limitation range (R_{SHUNT} = 10 mΩ, $V_{PRE_LIM_TH1}$ = 150 mV) To be recalculated for different R_{SHUNT} and different $V_{PRE_LIM_TH}$	12	15	18	A
V_{PRE_DRV}	HS and LS gate driver output voltage	—	VBOS	—	V
$I_{PRE_GATE_DRV}$	HS and LS gate driver pull up and pull down current capability (OTP_VPRESRHS[1:0] and OTP_VPRESRLS[1:0] bits by default + VPRESRHS[1:0] and VPRESRLS[1:0] bits by I^2C)	60	130	220	mA
		120	260	430	mA
		220	520	860	mA
		420	900	1490	mA
C_{OUT_PRE}	Effective output capacitor for F_{PRE_SW} = 455 kHz	44	66	220	µF
	Effective output capacitor for F_{PRE_SW} = 2.22 MHz	22	44	110	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_PRE}	Input capacitor (Cpi2)	20	—	—	µF
	Input decoupling capacitor	—	0.1	—	µF
I_{PRE_DRV}	Combined HS + LS gate driver average current capability $I_{PRE_DRV} < V_{PRE_SW} \times (QC_{HS} + QC_{LS})$ with QC_{HS} = gate charge of Q2 at VBOS with QC_{LS} = gate charge of Q1 at VBOS	—	—	30	mA
gmEA	Error amplifier transconductance	1.0	1.5	2.1	mS

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 62. VPRE electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{PRE_SLOPE}	Slope compensation (OTP_VPRESC[5:0] bits)	29	40	51	mV/µs
		36	50	64	mV/µs
		43	60	77	mV/µs
		51	70	89	mV/us
		58	80	102	mV/µs
		65	90	115	mV/µs
		73	100	127	mV/µs
		102	140	178	mV/µs
		124	170	216	mV/µs
		146	200	254	mV/µs
		175	240	305	mV/µs
$T_{PRE_UV_DFS}$	V_{PRE_UVL} filtering time to go to DEEP-FS during VPRE start up	1.8	2	2.2	ms
T_{PRE_DT}	Dead time to avoid cross conduction (this timing does not take into account the external FET turn ON/OFF times)	20	30	40	ns
R_{PRE_DIS}	Discharge resistor (when VPRE is disabled)	250	500	1000	Ω
$I_{PRE_SW_LKG}$	PRE_SW leakage	—	—	10	µA
R_{DRV_OFF}	HS and LS gate driver pull-down resistor when VPRE is disabled	5	—	35	kΩ
R_{BOOT_OFF}	PRE_BOOT pull-down resistor when VPRE is disabled	1.2	—	2.6	kΩ
I_{BOOT_LKG}	PRE_BOOT leakage	—	—	10	µA

14.5 VPRE external MOSFETs

MOSFETs selection:

- Logical level NMOS, gate drive comes from VBOS (5.0 V)
- VDS > 60 V for 24 V truck, bus applications
- VDS > 40 V for 12 V automotive applications
- Qg < 15 nC at Vgs = 5.0 V is recommended for 455 kHz
- Qg < 7 nC at Vgs = 5.0 V is recommended for 2.22 MHz
- Recommended references

Table 63. VPRE external MOSFETs recommendation

Applications	Fpre	Ipre < 2.0 A	Ipre < 4.0 A	Ipre < 6.0 A	Ipre < 10 A
12 V	455 kHz	BUK9K25-40E, BUK9K18-40E	BUK9K25-40E, BUK9K18-40E	BUK9K18-40E	BUK9K18-40E, NVTFS5C471NLWFTAG, HS = BUK9M9R5-40H, LS = BUK9M3R3-40H
	2.22 MHz	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	na
24 V	455 kHz	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E	BUK9K12-60E

Other MOSFETs are possible but should have similar performances as compared to the recommended references. The maximum current at 2.22 MHz is limited to 6.0 A for which the efficiency is equivalent to 10 A at 455 kHz. The power dissipation in the external MOSFETs is important and the junction temperature may rise above 175 ℃.

VPRE switching slew rate can be configured by I^2C to align with external MOSFET selection, VPRE switching frequency, and to optimize power dissipation and EMC performance. It is recommended to configure the maximum slew rate by OTP and reduce it later by I^2C if needed. FS5502 is using current source to drive the external MOSFET so adding an external serial resistor with the gate does not affect the slew rate. It is recommended to change the current source selection by I^2C to change the slew rate.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

VPRE MOSFET switching time can be estimated to $T_{SW} = (Q_{GD} + Q_{GS} / 2) / I_{PRE_GATE_DRV}$ using the gate charge definition from Figure 12. Q_{GD} and Q_{GS} can be extracted from the MOSFET data sheet.

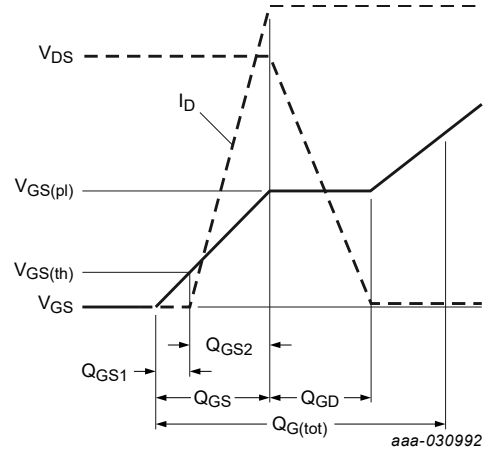


Figure 12. MOSFET gate charge definition

14.6 VPRE efficiency

VPRE efficiency versus current load is given for information based on external component criteria provided and VSUP voltage 14 V. If the conditions change, it has to be recalculated with the FS5502_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

VPRE at 455 kHz: BUK9K18-40E
VPRE at 2.22 MHz: BUK9K25-40E

Ext. C and L			
Fpre	455	2220	kHz
Cin	47	47	µF
ESR Cin	30	30	mΩ
Cout	66	44	µF
ESR Cout	10	10	mΩ
L coil	6.8	2.2	µH
DCR coil	25	25	mΩ
Rshunt	10	10	mΩ
Ext. MOSFET's			
GHS_drive	5	5	V
HS_Rdson	17	24	mΩ
HS_QGtot	7	5	nC
HS_QGD	3	2.4	nC
HS_QGS	2	1.4	nC
HS_Igate	900	900	mA
THS_sw	5	4	ns
GLS_drive	5	5	V
LS_Rdson	17	24	mΩ
LS_QGtot	7	5	nC
LS_QGD	3	2.4	nC
LS_QGS	2	1.4	nC
LS_QRR	16	7.6	nC
LS_Igate	900	900	mA
TLS_sw	5	4	ns

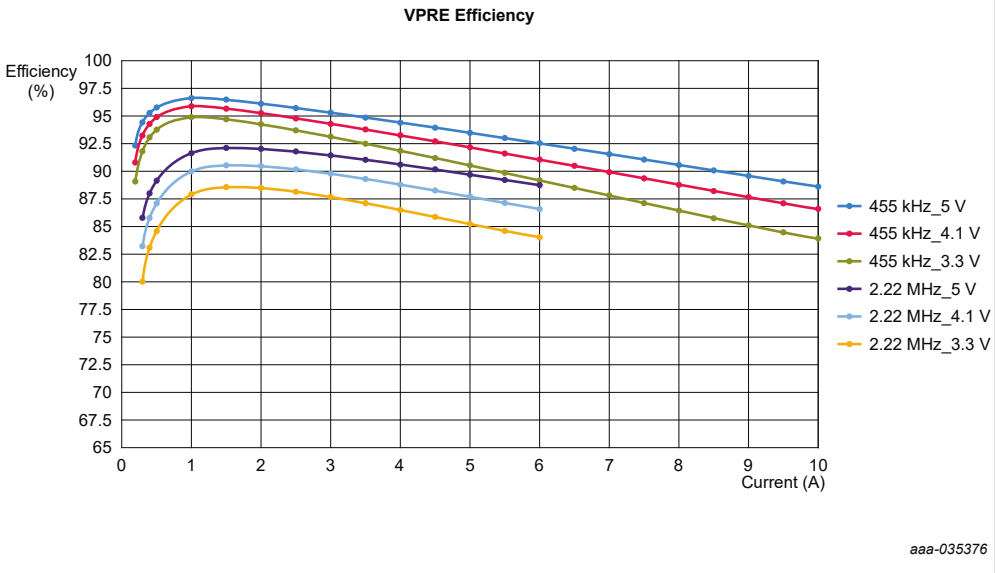


Figure 13. VPRE theoretical efficiency

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

14.7 VPRE not populated

When two FS5502 are used, only one VPRE may be required. It is possible to not populate the external components of the second VPRE to optimize the bill of material.

In that case, specific connection of the VPRE2 pins is required:

- PRE_FB2 must be connected to PRE_FB1
- PRE_CSP2 must be connected to PRE_FB1
- PRE_COMP2 must be left open
- PRE_SW2 must be connected to GND
- PRE_BOOT2 must be connected to VBOS2
- PRE_GHS2 and PRE_GLS2 must be left open

After the startup phase, VPRE2 shall be disabled by I^2C with VPDIS bit.

15 Low voltage buck: BUCK1

15.1 Functional description

BUCK1 block is low voltage, synchronous, valley current mode buck converters with integrated HS PMOS and LS NMOS. BUCK1 works in force with PWM. The output voltage is configurable by OTP from 0.8 V to 1.8 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of these blocks must be connected to the output of VPRE. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK1 switching frequency is derived from the internal oscillator and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

An overcurrent detection and a thermal shutdown are implemented on BUCK1 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

The ramp up and ramp down of BUCK1 when they are enabled and disabled is configurable with OTP_DVS_BUCK1[1:0] bits to accommodate multiple MCU soft start requirements. Static Voltage Scaling (SVS) feature is available to decrease the output voltage after power up during INIT_FS. Programmable phase shift control is implemented, see Section 18 "Clock management".

15.2 Application schematic: Single phase mode

In this configuration, BUCK1 output is configured and controlled independently by I^2C.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

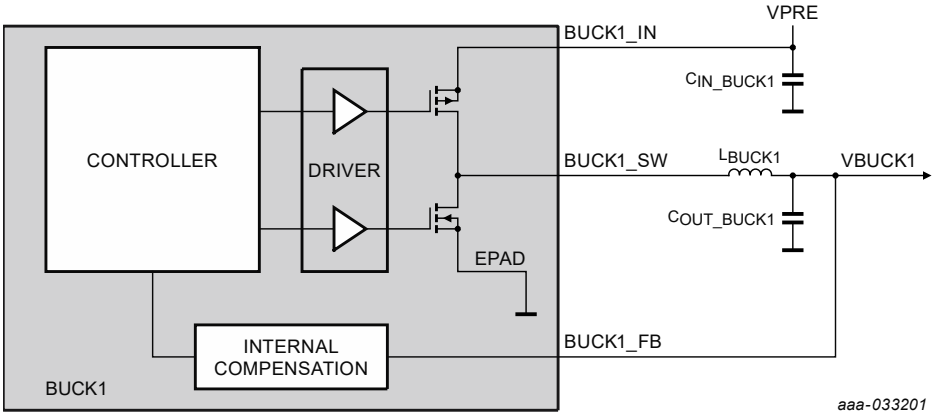


Figure 14. BUCK1 standalone schematic

15.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. The error amplifier gain is configurable with OTP_VB1GMCOMP[2:0] bits for BUCK 1 regulator. It is recommended to use the default value that covers most of the use cases.

Decreasing the gain reduces the regulation bandwidth and increase the phase and gain margin but transient performance is degraded. Increasing the gain enlarges the regulation bandwidth and improves the transient performance but the phase and gain margin is degraded.

OTP_VB1INDOPT[1:0] scales the slope compensation and the zero cross detection according to the inductor value. 1.0 µH is the recommended inductor value for BUCK1.

Use case with V_{PRE} = 4.1 V, V_{BUCK1} = 1.0 V, L_{VBUCK1} = 1.0 µH, V_{BUCK1_SW} = 2.22 MHz, C_{OUT_BUCK1} = 44 µF, default Err Amp gain

Use case stability verification

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

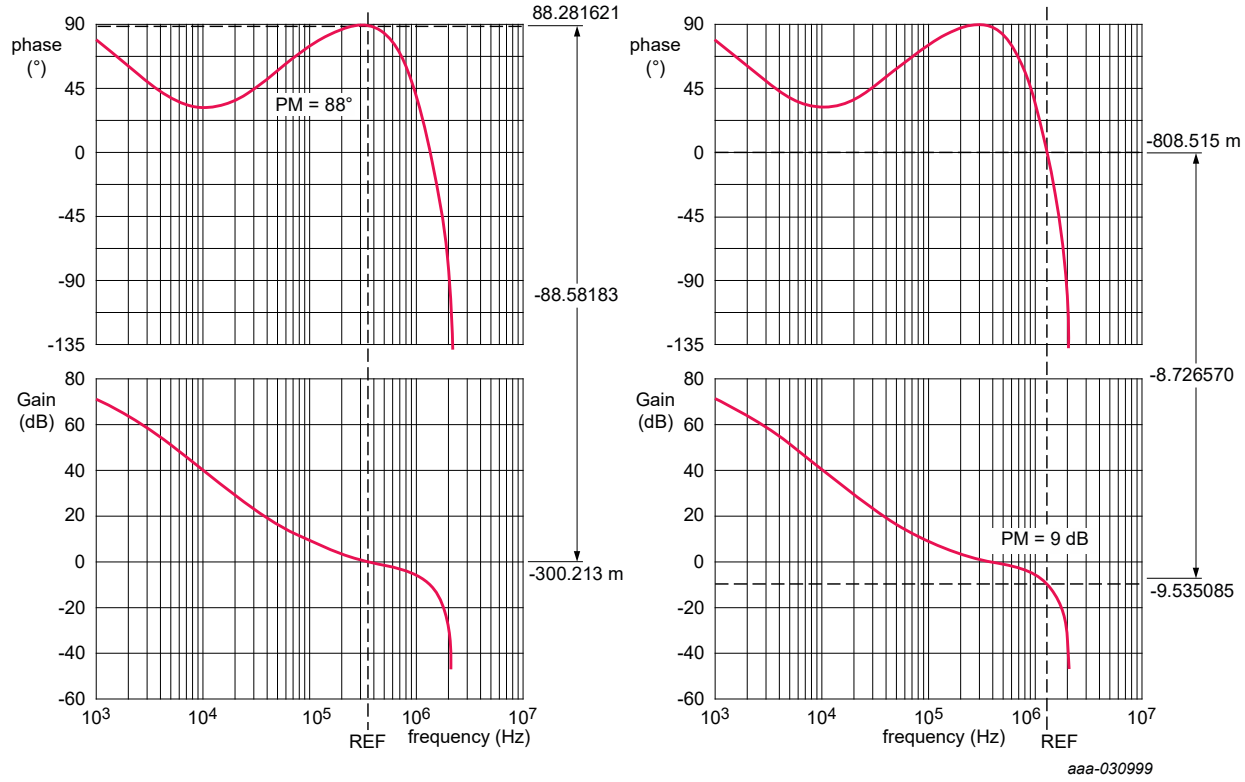


Figure 15. Phase and gain margin simulation

Use case transient response verification

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

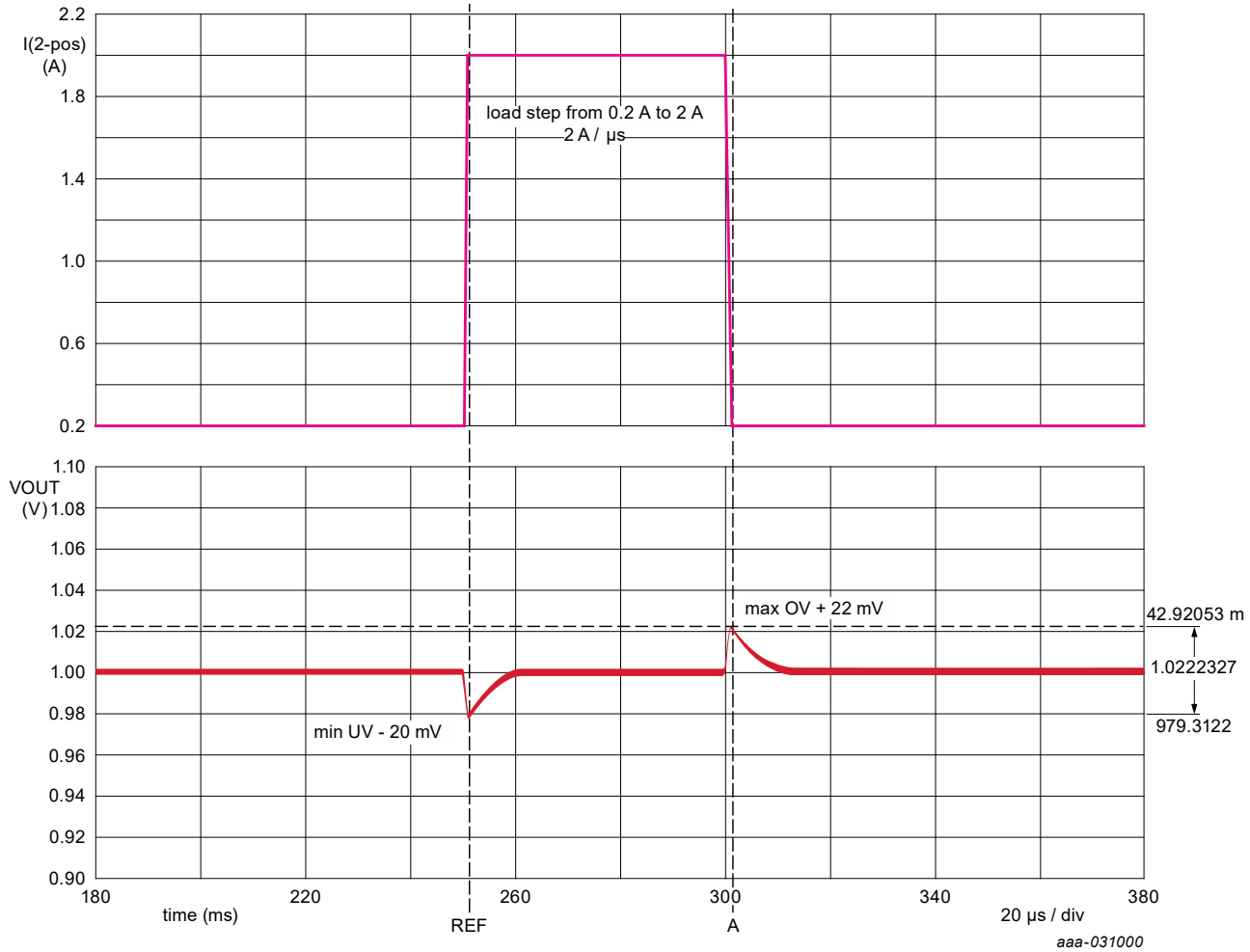


Figure 16. Transient response simulation

15.4 BUCK1 electrical characteristics

Table 64. BUCK1 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUCK1_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK1}	Output voltage (OTP_VB1V[7:0]) 0.8 V, 0.9 V, 0.95 V, 1.0 V, 1.025 V, 1.03125 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.4 V, 1.5 V, 1.8 V	0.8	—	1.8	V
I_{BUCK1}	DC output current capability (one phase)	—	—	2.5	A
V_{BUCK1_ACC}	Output voltage accuracy (I_{OUT} < 2.5 A)	−2	—	+2	%
V_{BUCK1_SW}	Switching frequency range	2.1	2.22	2.35	MHz
L_{BUCK1}	Inductor for V_{BUCK1_SW} = 2.22 MHz (OTP_VB1INDOPT[1:0])	0.47	1.0	1.5	µH
C_{OUT_BUCK1}	Effective output capacitor	40	—	160	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK1}	Input capacitor (close to BUCK1_IN)	4.7	—	—	µF
	Input decoupling capacitor (close to BUCK1_IN)	—	0.1	—	µF
V_{BUCK1_TLR}	Transient load regulation for V_{BUCK1} < 1.2 V (Cout = 44 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs) (Cout = 44 µF, from 400 mA to 2.0 A, di/dt = 4.0 A/µs)	−25	—	+25	mV

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 64. BUCK1 electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUCK1_TLR}	Transient load regulation for V_{BUCK1} >1.2 V (Cout = 44 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs) (Cout = 44 µF, from 400 mA to 2.0 A, di/dt = 4.0 A/µs)	−3	—	+3	%
I_{LIM_BUCK1}	Inductor peak current limitation range for one phase (OTP_VB1SWILIM[1:0])	3.6	4.5	5.45	A
$V_{BUCK1_DVS_UP}$ (for V_{BUCK1} up to 1.5 V)	Ramp up speed, OTP_DVS_BUCK1[1:0] = 00	5.86	7.81	9.77	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 01	2.34	3.13	3.91	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 10	1.95	2.60	3.26	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 11	1.67	2.23	2.79	mV/µs
$V_{BUCK1_DVS_UP}$ (for V_{BUCK1} = 1.8 V)	Ramp up speed, OTP_DVS_BUCK1[1:0] = 00	7.33	9.763	12.21	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 01	2.93	3.91	4.89	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 10	2.44	3.25	4.08	mV/µs
	Ramp up speed, OTP_DVS_BUCK1[1:0] = 11	2.09	2.79	3.49	mV/µs
$V_{BUCK1_DVS_DOWN}$ (for V_{BUCK1} up to 1.5 V)	Ramp down speed, OTP_DVS_BUCK1[1:0] = 00	3.91	5.21	6.51	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 01	2.34	3.13	3.91	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 10	1.95	2.6	3.26	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 11	1.67	2.23	2.79	mV/µs
$V_{BUCK1_DVS_DOWN}$ (for V_{BUCK1} = 1.8 V)	Ramp down speed, OTP_DVS_BUCK1[1:0] = 00	4.89	6.51	8.14	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 01	2.93	3.91	4.89	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 10	2.44	3.25	4.08	mV/µs
	Ramp down speed, OTP_DVS_BUCK1[1:0] = 11	2.09	2.79	3.49	mV/µs
$T_{BUCK1_SOFT_START}$	$T_{BUCK1_SOFT_START}$ = V_{BUCK1} / $V_{BUCK1_DVS_UP}$ Soft start for V_{BUCK1} = 1.2 V and OTP_DVS_BUCK1[1:0] = 00	122.9	153.6	204.8	µs
	Soft start for V_{BUCK1} = 1.2 V and OTP_DVS_BUCK1[1:0] = 11 To be recalculated for different V_{BUCK1} and different $V_{BUCK1_DVS_UP}$	430.1	538.1	718.5	µs
$V_{BUCK1_STARTUP}$	Overshoot at startup	—	—	50	mV
$T_{BUCK1_OFF_MIN}$	HS minimum OFF time	9	30	54	ns
T_{BUCK1_DT}	Dead time to avoid cross conduction	0.01	3	20	ns
$R_{BUCK1_HS_RON}$	HS PMOS RDSon	—	—	135	mΩ
$R_{BUCK1_LS_RON}$	LS NMOS RDSon	—	—	80	mΩ
R_{BUCK1_DISch}	Discharge resistance (when BUCK1 is disabled)	250	500	1000	Ω
TSD_{BUCK1}	Thermal shutdown threshold	160	—	—	°C
TSD_{BUCK1_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{BUCK1_TSD}	Thermal shutdown filtering time	3	5	8	µs

15.5 BUCK1 efficiency

BUCK1 efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, it has to be recalculated with the VR5502_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	20	mΩ
Int. MOSFET's		
HS_Rdson	135	mΩ
QHS	0.5	nC
THS_sw	3	ns
GHS_drive	5	V
LS_Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	3	ns
GLS_drive	5	V

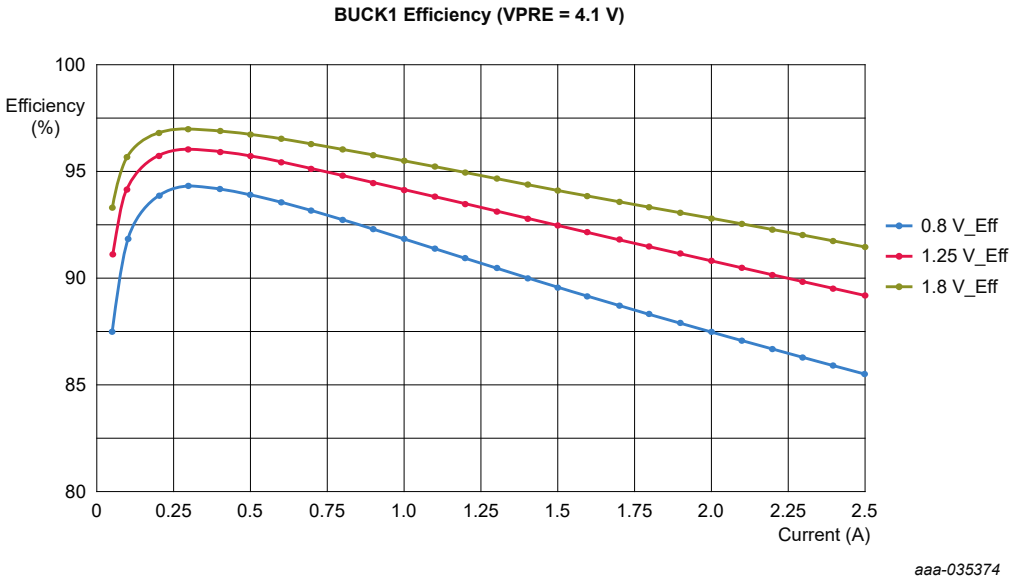


Figure 17. BUCK1 theoretical efficiency

16 Low voltage buck: BUCK3

16.1 Functional description

BUCK3 block is a low voltage, synchronous, peak current mode buck converter with integrated HS PMOS and LS NMOS. BUCK3 works in force PWM and the output voltage is configurable by OTP from 1.0 V to 3.3 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of this block can be connected to the output of VPRE. The stability is ensured by an internal Type 2 compensation network with slope compensation.

By default, BUCK3 switching frequency is derived from the internal oscillator, and can be synchronized with an external frequency signal applied on FIN input pin. The change from internal oscillator to external clock or vice versa is controlled by I^2C.

An overcurrent detection and a thermal shutdown are implemented on BUCK3 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

BUCK3 is part number dependent according to OTP_BUCK3EN bit. BUCK3_INQ pin, used to bias internal BUCK3 driver, and must be connected to the same source pin as BUCK3_IN pin. The ramp up and ramp down of BUCK3 when it is enabled and disabled is configurable with OTP_DVS_BUCK3[1:0] bits to accommodate multiple MCU soft start requirements.

Programmable phase shift control is implemented, see Section 18 "Clock management".

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

16.2 Application schematic

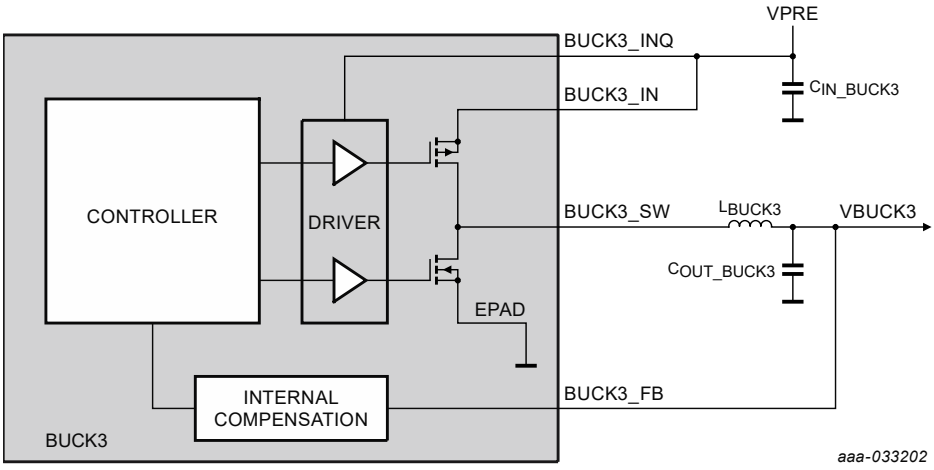


Figure 18. BUCK3 schematic

16.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. OTP_VB3INDOPT[1:0] scales the slope compensation and the zero cross detection according to inductor value. 1.0 µH is the recommended inductor value for BUCK3.

Use case with V_{PRE} = 4.1 V, V_{BUCK3} = 2.3 V, L_{VBUCK3} = 1.0 µH, V_{BUCK3_SW} = 2.22 MHz, C_{OUT_BUCK3} = 44 µF

Use case stability verification

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

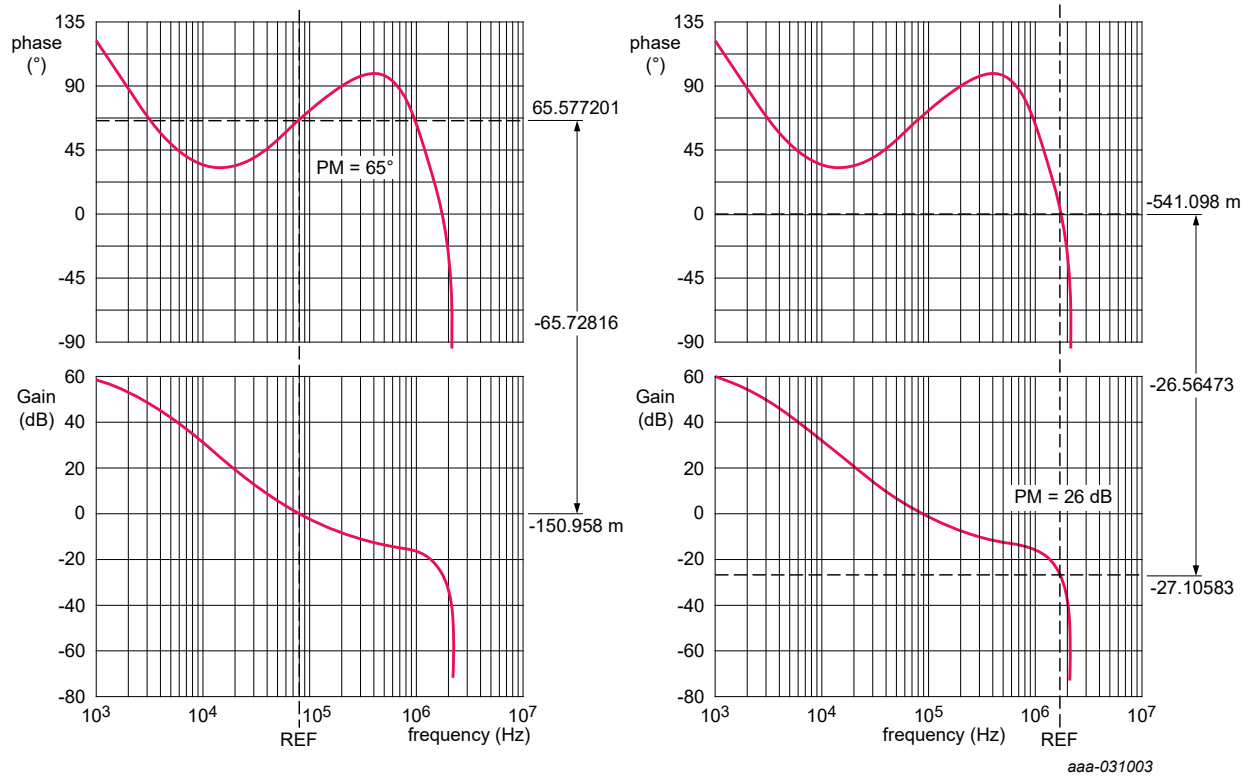


Figure 19. Phase and gain margin simulation

Use case transient response verification

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

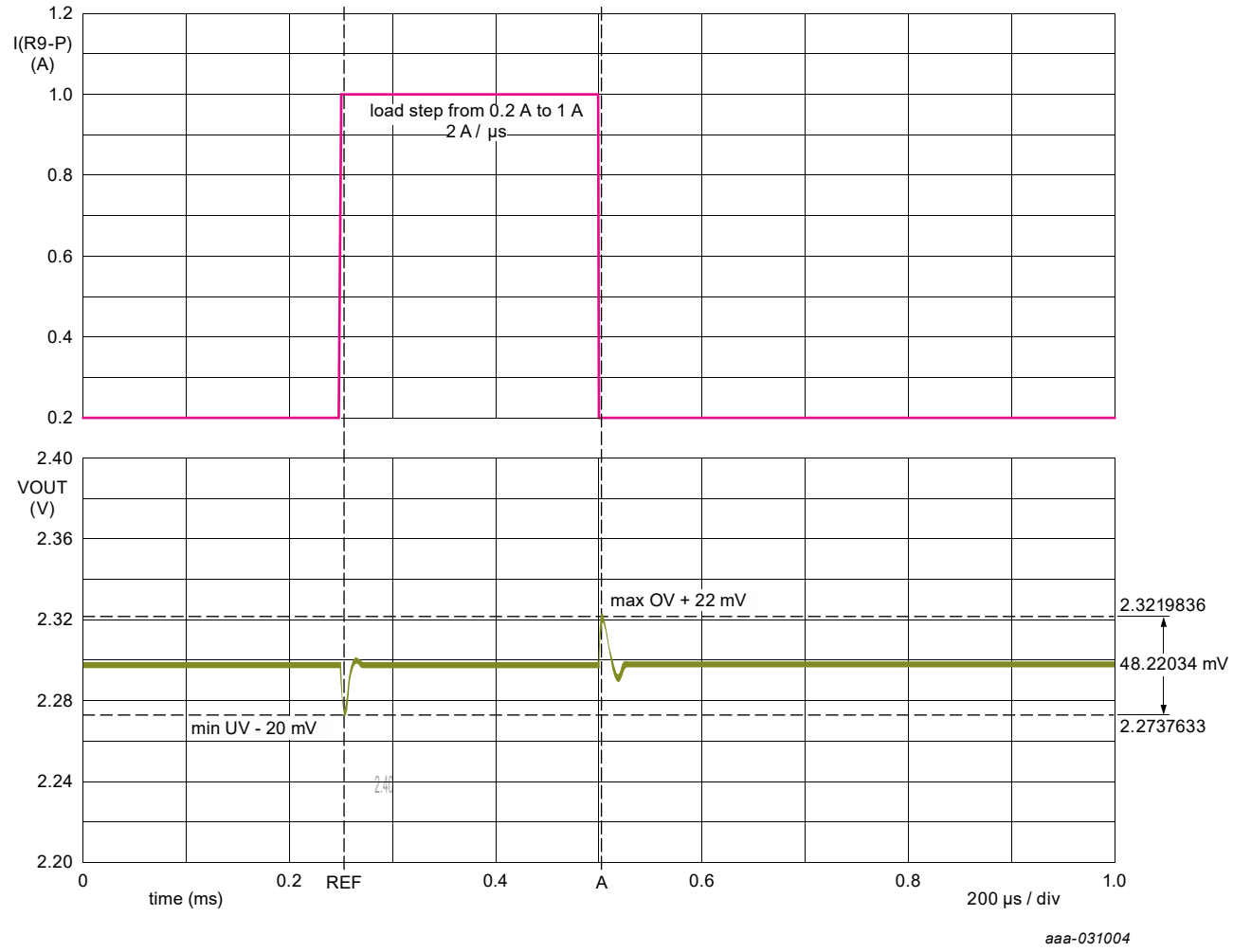


Figure 20. Transient response simulation

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

16.4 BUCK3 electrical characteristics

Table 65. BUCK3 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{BUCK3_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK3}	Output voltage (OTP_VB3V[4:0] bits) 1.0 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.5 V, 1.6 V, 1.8 V, 2.3 V, 2.5 V, 2.8 V, 3.3 V	1.0	—	3.3	V
I_{BUCK3}	DC output current capability	—	2.5	—	A
V_{BUCK3_ACC}	Output voltage accuracy (Iout < 2.5 A)	−2	—	+2	%
V_{BUCK3_SW}	Switching frequency range	2.1	2.22	2.35	MHz
L_{BUCK3}	Inductor for V_{BUCK3_SW} = 2.22 MHz (OTP_VB3INDOPT[1:0] bits)	0.47	1.0	1.5	µH
C_{OUT_BUCK3}	Effective output capacitor	40	—	120	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK3}	Effective input capacitor (close to BUCK3_IN pin)	4.7	—	—	µF
	Input decoupling capacitor (close to BUCK3_IN pin)	—	0.1	—	µF
V_{BUCK3_TLR}	Transient load regulation (Cout = 44 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs)	−50	—	+50	mV
I_{LIM_BUCK3}	Inductor peak current limitation range (OTP_VB3SWILIM[1:0] bits)	2.0	2.6	3.1	A
		3.6	4.5	5.45	A
$T_{BUCK3_ON_MIN}$	HS minimum ON time	5	50	80	ns
$V_{BUCK3_DVS_UP_DOWN}$	Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 00	7.81	10.42	13.02	mV/µs
	Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 01	2.6	3.47	4.34	mV/µs
	Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 10	1.95	2.6	3.26	mV/µs
	Ramp up and ramp down speed, OTP_DVS_BUCK3[1:0] = 11	1.56	2.08	2.60	mV/µs
$T_{BUCK3_SOFT_START}$	$T_{BUCK3_SOFT_START}$ = V_{BUCK3} / $V_{BUCK3_DVS_UP}$ Soft start for V_{BUCK3} = 1.1 V and OTP_DVS_BUCK3[1:0] = 00	84.8	105.6	140.08	µs
	Soft start for V_{BUCK3} = 1.1 V and OTP_DVS_BUCK3[1:0] = 11 To be recalculated for different V_{BUCK3} and different $V_{BUCK3_DVS_UP_DOWN}$	422.4	528	704	µs
$V_{BUCK3_STARTUP}$	Overshoot at startup	—	—	50	mV
T_{BUCK3_DT}	Dead time to avoid cross conduction	0.01	3	20	ns
$R_{BUCK3_HS_RON}$	HS PMOS RDSon	—	—	135	mΩ
$R_{BUCK3_LS_RON}$	LS NMOS RDSon	—	—	80	mΩ
R_{BUCK3_DISCH}	Discharge resistance (when BUCK3 is disabled)	250	500	1000	Ω
TSD_{BUCK3}	Thermal shutdown threshold	160	—	—	°C
TSD_{BUCK3_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{BUCK3_TSD}	Thermal shutdown filtering time	3	5	8	µs

16.5 BUCK3 efficiency

BUCK3 efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, it has to be recalculated with the FS5502_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	20	mΩ
Int. MOSFETs		
HS_Rdson	135	mΩ
QHS	0.5	nC
THS_sw	3	ns
GHS_drive	5	V
LS_Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	3	ns
GLS_drive	5	V

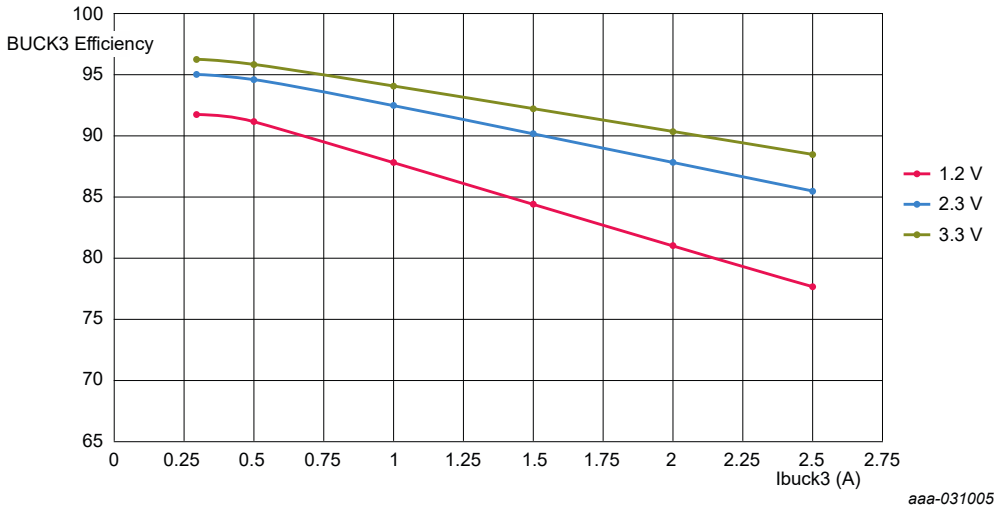


Figure 21. BUCK3 theoretical efficiency

17 Linear voltage regulator: LDO1

17.1 Functional description

An LDO1 block is a linear voltage regulator. The output voltage is configurable by OTP from 1.1 V to 5.0 V. A minimum voltage drop is required depending on the output current capability (0.5 V for 150 mA and 1.0 V for 400 mA). The LDO current capability is linear with the voltage drop and can be estimated to I(mA) = 500 x V_{LDO1_DROP} – 100 for intermediate voltage drop between 0.5 V and 1.0 V.

LDO1 input supply is externally connected to VPRE or another supply. An overcurrent detection and a thermal shutdown are implemented on LDO1 to protect the internal pass device.

17.2 Application schematics

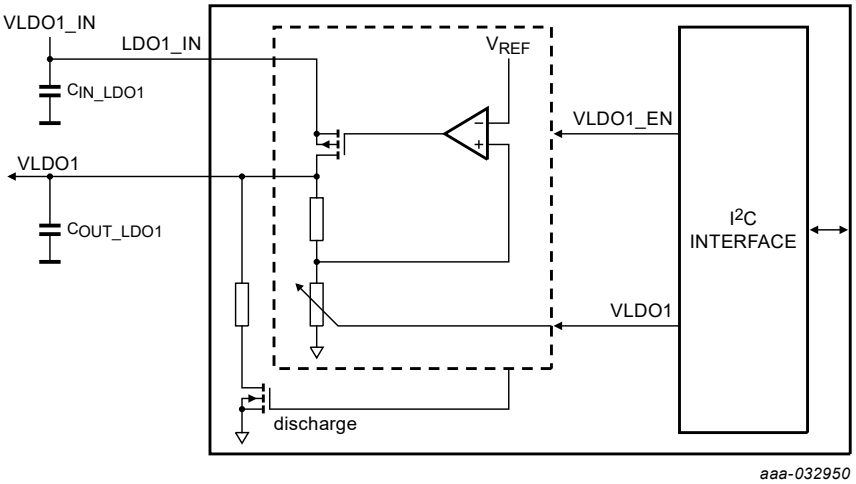


Figure 22. LDO1 block diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

17.3 LDO1 electrical characteristics

Table 66. LDO1 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO1_IN}	Input voltage range	2.5	—	6.5	V
V_{LDO1}	Output voltage (OTP_VLDO1V[2:0]) 1.1 V, 1.2 V, 1.6 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V	1.1	—	5.0	V
$V_{LDO1_ACC_150}$	Output voltage accuracy, 150 mA current capability	−2	—	+2	%
$V_{LDO1_ACC_400}$	Output voltage accuracy, 400 mA current capability	−3	—	+3	%
$V_{LDO1_DROP_150}$	Minimum voltage drop for 150 mA current capability	0.5	—	—	V
$V_{LDO1_DROP_400}$	Minimum voltage drop for 400 mA current capability	1.0	—	—	V
C_{IN_LDO1}	Input capacitor (close to LDO1_IN pin)	1.0	—	—	µF
$C_{OUT_LDO1_150}$	Output capacitor, 150 mA current capability	4.7	—	10	µF
$C_{OUT_LDO1_400}$	Output capacitor, 400 mA current capability	6.8	—	10	µF
C_{OUT_LDO1}	Output decoupling capacitor	0.1	—	—	µF
$V_{LDO1_LTR_150}$	Transient load regulation (from 10 mA to 150 mA in 2.0 µs)	−4	—	+4	%
$V_{LDO1_LTR_400}$	Transient load regulation (from 10 mA to 400 mA in 4.0 µs)	−5	—	+5	%
V_{LDO1_LR}	Line regulation	—	—	0.5	%
$V_{LDO1_ILIM_150}$	Current limitation, 150 mA current capability (OTP_LDO1ILIM)	200	280	500	mA
$V_{LDO1_ILIM_400}$	Current limitation, 400 mA current capability (OTP_LDO1ILIM)	430	560	800	mA
$V_{LDO1_SOFT_START}$	Soft start (enable to 90 %)	—	1.0	1.3	ms
$V_{LDO1_STARTUP}$	Overshoot at startup	—	—	2	%
R_{LDO1_DISCH}	Discharge resistance (when LDO1 is disabled)	10	20	60	Ω
TSD_{LDO1}	Thermal shutdown threshold	160	—	—	°C
TSD_{LDO1_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{LDO1_TSD}	Thermal shutdown filtering time	3	5	8	µs

18 Clock management

18.1 Clock description

The clock management block is made of the Internal oscillator, the Phase Locked Loop (PLL) and multiple dividers. This block manages the clock generation for the internal digital state machines, the switching regulators and the external clock synchronization.

The internal oscillator is running at 20 MHz by default after start up. The frequency is programmable by I^2C and a spread spectrum feature can be activated by I^2C to reduce the emission of the oscillator fundamental frequency.

VPRE switching frequency comes from CLK2 (455 kHz) or CLK1 (2.22 MHz). BUCK1 and BUCK3 switching frequency comes from CLK1 (2.22 MHz). The switching regulators can be synchronized with an external frequency coming from FIN pin. A dedicated watchdog monitoring is implemented to verify and report the correct FIN frequency range. Different clocks can be sent to FOUT pin to synchronize an external IC or for diagnostic.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

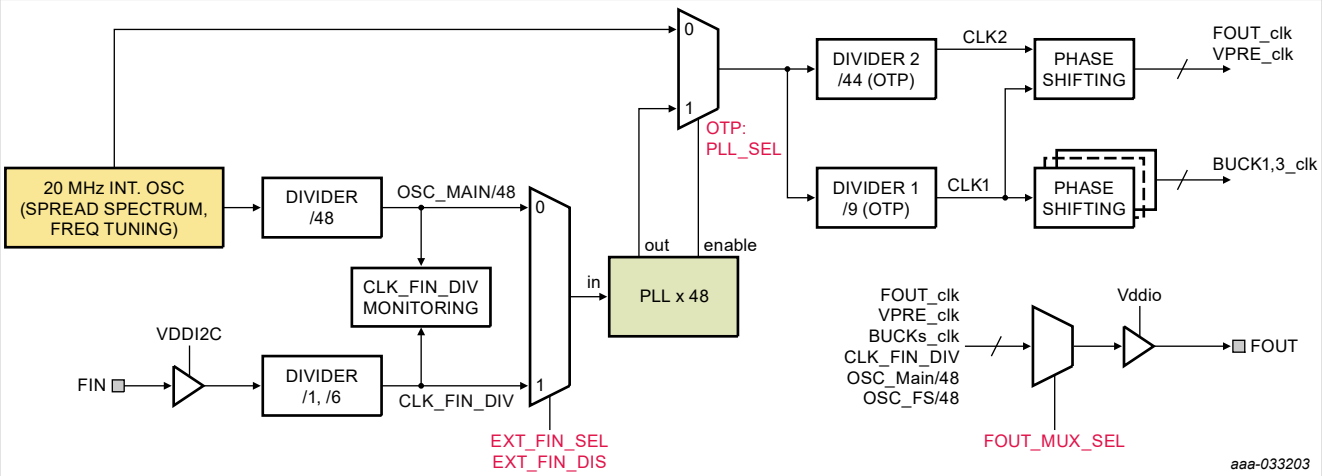


Figure 23. Clock management block diagram

18.2 Phase shifting

The clocks of the switching regulators (VPRE_clk, BUCK1_clk and BUCK3_clk) can be delayed in order to avoid all the regulators to turn ON at the same time to reduce peak current and improve EMC performance.

Each clock of each regulator can be shifted from 1 to 7 clock cycles of CLK running at 20 MHz what corresponds to 50 ns. The phase shift configuration is done by OTP configuration using OTP_VPRE_ph[2:0], OTP_BUCK1_ph[2:0] and OTP_BUCK3_ph[2:0].

VPRE and BUCK3 have a peak current detection architecture. The PWM synchronizes the turn ON of the high-side switch. BUCK1 has a valley current detection architecture. The PWM synchronizes the turn ON of the low-side switch.

18.3 Manual frequency tuning

The internal oscillator frequency, 20 MHz by default, can be programmed from 16 MHz to 24 MHz with 1.0 MHz frequency step by I^2C. The oscillator functionality is guaranteed for frequency increment of one step at a time in either direction, with a minimum of 10 µs between two steps. For any unused code of the CLK_TUNE [3:0] bits, the internal oscillator is set at the default 20 MHz frequency.

To change the internal oscillator frequency from 20 MHz to 24 MHz, four I^2C commands are required with 10 µs wait time between each command (21 MHz – wait 10 µs – 22 MHz – wait 10 µs – 23 MHz – wait 10 µs – 24 MHz). To change the internal oscillator frequency from 24 MHz to 16 MHz, eight I^2C commands are required with 10 µs wait time between each command (23 MHz – wait 10 µs – 22 MHz – wait 10 µs – 21 MHz – wait 10 µs – 20 MHz – wait 10 µs – 19 MHz – wait 10 µs – 18 MHz – wait 10 µs – 17 MHz – wait 10 µs – 16MHz).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 67. Manual frequency tuning configuration

CLK_TUNE [3:0]	Oscillator frequency [MHz]
0000 (default)	20
0001	21
0010	22
0011	23
0100	24
1001	16
1010	17
1011	18
1100	19
Reset condition	POR

18.4 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz with ±5 % deviation range around the oscillator frequency. The spread spectrum feature can be activated by I^2C with the MOD_EN bit and the carrier frequency can be selected by I^2C with the MOD_CONF bit. By default, the spread spectrum is disabled. The spread spectrum and the manual frequency tuning functions cannot be used at the same time.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and VPRE frequency on VBAT frequency spectrum. Consequently, it is recommended to select 23 kHz carrier frequency when VPRE is configured at 455 kHz and 94 kHz when VPRE is configured at 2.2 MHz for the best performance.

18.5 External clock synchronization

To synchronize the switching regulators with an external frequency coming from FIN pin, the PLL shall be enabled with OTP_PLL_SEL bit. The FIN pin accepts two ranges of frequency depending on the divider selection to always have CLK clock at the output of the PLL in the working range of the digital blocks from 16 MHz to 24 MHz. When FIN_DIV = 0, the input frequency range must be between 333 kHz and 500 kHz. When FIN_DIV = 1, the input frequency range must be between 2.0 MHz and 3.0 MHz.

After the FIN clock divider configuration with FIN_DIV bit, the FIN clock is routed to the PLL input with EXT_FIN_SEL bit. The CLK clock changes from the internal oscillator to FIN external clock with EXT_FIN_SEL bit. So, the configuration procedure is FIN_DIV first, then apply FIN and finally set EXT_FIN_SEL.

If FIN is out of range, CLK clock moves back to the internal oscillator and reports the error using the CLK_FIN_DIV_OK bit. When FIN comes back in the range, the configuration procedure described above is executed again.

The FOUT pin can be used to synchronize an external device with the FS5502. The frequency sent to FOUT is selected by I^2C with the FOUT_MUX_SEL [3:0] bits.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 68. FOUT multiplexer selection

FOUT_MUX_SEL [3:0]	FOUT multiplexer selection
0000 (default)	No signal, FOUT is low
0001	VPRE_clk
0010	RESERVED
0011	BUCK1_clk
0100	RESERVED
0101	BUCK3_clk
0110	FOUT_clk (CLK1 or CLK2 selected with FOUT_CLK_SEL bit)
0111	OSC_MAIN/48 (when PLL is enabled by OTP)
1000	OSC_FS/48
1001	CLK_FIN_DIV
Others	No signal, FOUT is low
Reset condition	POR

18.6 Electrical characteristics

Table 69. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
20 MHz internal oscillator					
F_{20MHz}	Oscillator nominal frequency (programmable)	—	20	—	MHz
F_{20MHz_ACC}	Oscillator accuracy	−6	—	+6	%
T_{20MHz_step}	Oscillator frequency tuning step transition time	—	10	—	µs
Spread spectrum					
FSS_{MOD}	Spread spectrum frequency modulation (MOD_CONF I^2C configuration)	—	23	—	kHz
		—	94	—	kHz
FSS_{RANGE}	Spread spectrum range (around the nominal frequency)	−5	—	+5	%
Clock synchronization (FIN)					
V_{FIN_IN}	Input voltage range	—	VDDI2C	—	V
DC_{FIN_FOUT}	FIN and FOUT duty cycle	40	50	60	%
FIN_{RANGE}	FIN input frequency range (FIN_DIV I^2C configuration)	333	417	500	kHz
		2.25	2.5	2.75	MHz
FIN_{VIL}	FIN low voltage threshold	0.3 x V_{DDI2C}	—	—	V
FIN_{VIH}	FIN high voltage threshold	—	—	0.7 x V_{DDI2C}	V
FIN_{HYST}	FIN hysteresis	0.1	—	—	V
FIN_{IPD}	FIN internal pull-down current source	7	10	13	µA
FIN_{DLY}	FIN input buffer propagation delay	—	—	8	ns
FIN_{ERR_LONG}	CLK_FIN_DIV monitoring, long deviation detection	5	—	—	µs
FIN_{ERR_SHORT}	CLK_FIN_DIV monitoring, short deviation detection	—	—	1.5	µs
FIN_{TLOST}	Time to switch to internal oscillator when FIN is lost	—	—	3	µs

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 69. Electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Clock synchronization (FOUT)					
V_{FOUT_OUT}	Output voltage range	—	VDDIO	—	V
$FOUT_{VOL}$	FOUT low voltage threshold at 2.0 mA	—	—	0.5	V
$FOUT_{VOH}$	FOUT high voltage threshold at −2.0 mA	V_{DDIO} − 0.5	—	—	V
I_{FOUT}	Tri-state leakage current (VDDIO = 5.0 V)	−1.0	—	1.0	µA
$FOUT_{TRISE}$	FOUT rise time (from 20 % to 80 % of VDDIO, Cout = 30 pF)	—	—	20	ns
$FOUT_{TFALL}$	FOUT fall time (from 80 % to 20 % of VDDIO, Cout = 30 pF)	—	—	20	ns
PLL_{TLOCK}	PLL lock time	—	—	90	µs
PLL_{TSET}	PLL settling time (from EXT_FIN_DIS enable to ±1 % of output frequency)	—	—	125	µs

19 I/O interface pins

19.1 WAKE1, WAKE2

WAKE pins are used to manage the internal biasing of the device and the main state machine transitions.

- When WAKE1 or WAKE2 is > $WAKE12_{VIH}$, the internal biasing is started and the equivalent digital state is 1
- When WAKE1 or WAKE2 is < $WAKE12_{VIL}$, the equivalent digital state is 0
- When WAKE1 and WAKE2 are < $WAKE12_{AVIL}$, the internal biasing is stopped if the device was in Standby mode

WAKE1 can be, for example, connected to VBAT and WAKE2 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, a CRC protection is required (see Section 26 "Application information").

Table 70. WAKE1, WAKE2 electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$WAKE12_{AVIL}$	Analog low input voltage threshold	1	—	—	V
$WAKE12_{VIL}$	Digital low input voltage threshold	2	—	—	V
$WAKE12_{VIH}$	Digital high input voltage threshold	—	—	4	V
I_{WAKE12}	Input current leakage at WAKE12 = 36 V	—	—	100	µA
	Input current leakage at WAKE12 = 60 V	—	—	300	µA
T_{WAKE12}	Filtering time	50	70	100	µs

19.2 INTB

INTB is an open drain output pin with internal pull up to VDDIO. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in M_INT_MASK registers.

Table 71. INTB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$INTB_{PULL\text{-}up}$	Internal pull-up resistor to VDDIO	5.5	10	15	kΩ

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 71. INTB electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$INTB_{VOL}$	Low output level threshold (I = 2.0 mA)	—	—	0.5	V
$INTB_{LKG}$	Input leakage current	—	—	1.0	µA
$INTB_{PULSE}$	Pulse duration (without manual frequency tuning)	90	100	110	µs

Table 72. List of interrupts from main logic

Interrupt main	Description
VSUP_UV7	VSUP undervoltage 7.0 V
VSUP_UVH	VSUP undervoltage high
VSUP_UVL	VSUP undervoltage low
VBOS_UVH	VBOS undervoltage high
VPRE_OC	VPRE overcurrent
VPRE_FB_OV	VPRE overvoltage protection
VPRE_UVH	VPRE undervoltage high
VPRE_UVL	VPRE undervoltage low
BUCK1_TSD	BUCK1 overtemperature shutdown event
BUCK1_OC	BUCK1 overcurrent
BUCK3_TSD	BUCK3 overtemperature shutdown event
BUCK3_OC	BUCK3 overcurrent
LDO1_TSD	LDO1 overtemperature shutdown event
LDO1_OC	LDO1 overcurrent
WAKE1	WAKE1 transition
WAKE2	WAKE2 transition
COM	I^2C communication error

Table 73. List of interrupts from fail-safe logic

Interrupt fail-safe	Description
VCOREMON_OV	VCOREMON overvoltage detected
VCOREMON_UV	VCOREMON undervoltage detected
VDDIO_OV	VDDIO overvoltage detected
VDDIO_UV	VDDIO undervoltage detected
VMON1_OV	VMON1 overvoltage detected
VMON1_UV	VMON1 undervoltage detected

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

19.3 PSYNC for two FS5502

PSYNC function allows to manage complex start up sequence with multiple power management ICs like two FS5502 (OTP_PSYNC_CFG = 0) or one FS5502 plus one PF82 (OTP_PSYNC_CFG = 1). This function is enabled with the OTP_PSYNC_EN bit.

When PSYNC is used to synchronize two FS5502, PSYNC pin of each device shall be connected together and pulled up to VBOS pin of the FS5502 master device as shown in Figure 24. In this configuration, FS5502 #1 state machine stops before FS5502 #1_VPRE starts and waits for FS5502 #2 to synchronize FS5502#2_VPRE start.

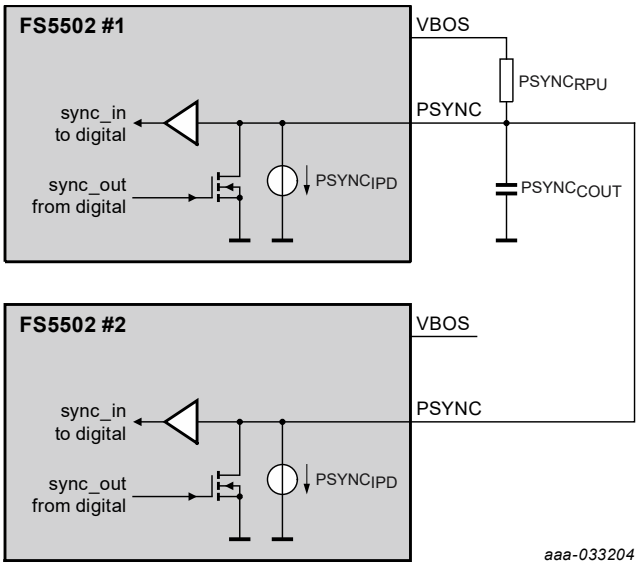


Figure 24. Synchronization of two FS5502

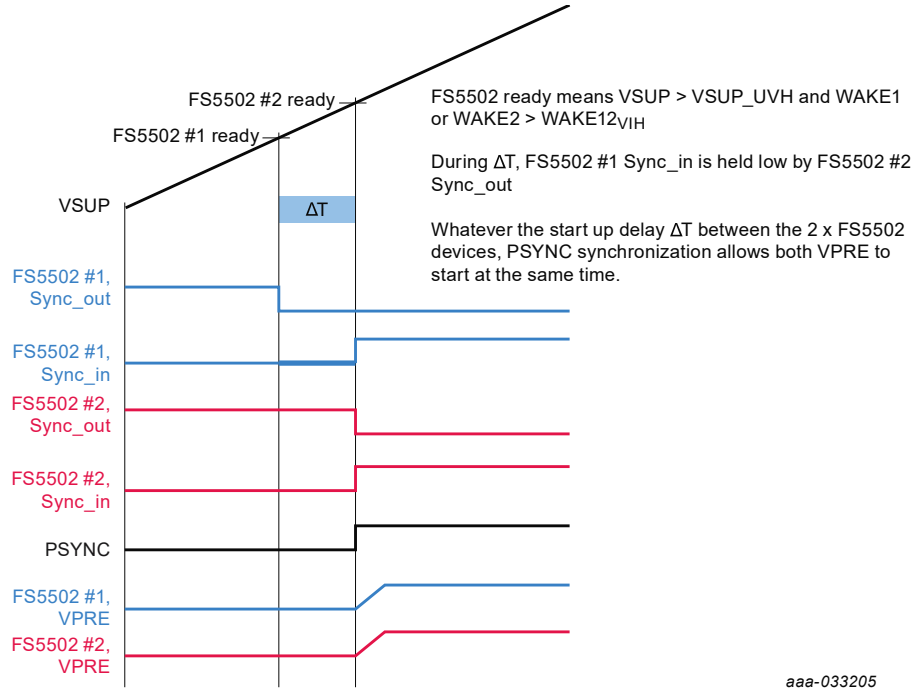


Figure 25. Two FS5502 synchronization timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

19.4 PSYNC for FS5502 and external PMIC

When PSYNC is used to synchronize one FS5502 and one external PMIC, PSYNC pin of FS5502 is connected to PGOOD pin of the external PMIC.

When the external PMIC is PF82 from NXP, it can be pulled up to VSNVS pin of PF82. In this configuration, FS5502 state machine stops after VPRE starts and waits for the PGOOD pin of the external PMIC to be released to continue its own power sequencing. It allows to synchronize the power up sequence of both devices.

During power-down sequence, FS5502 should wait for the external PMIC power-down sequence completion before turning OFF VPRE (VPRE is powering the external PMIC). OTP_VPRE_off_dly bit is configured to extend VPRE turn OFF delay from 250 µs default value to 32 ms.

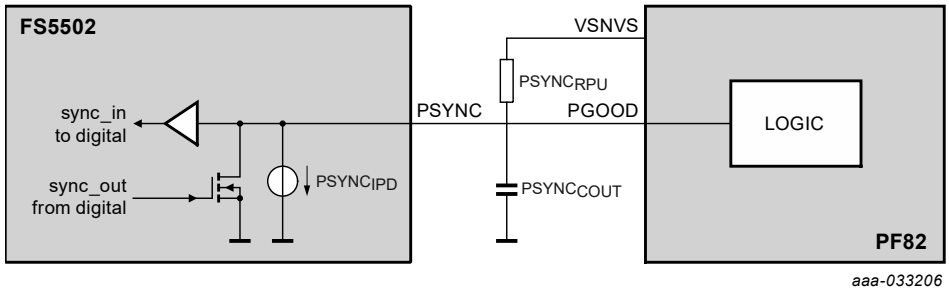


Figure 26. Synchronization of one FS5502 and one external PMIC (PF82)

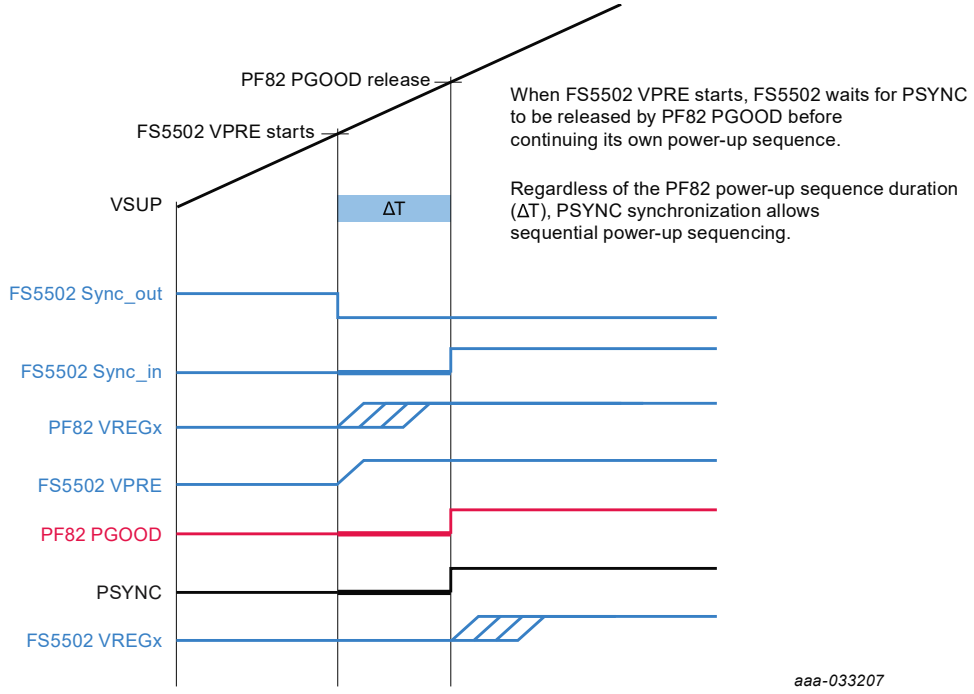


Figure 27. FS5502 and one PF82 synchronization timing diagram

Table 74. PSYNC electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$PSYNC_{VIL}$	Low level input voltage threshold	1	—	—	V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 74. PSYNC electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$PSYNC_{VIH}$	High level input voltage threshold	—	—	2	V
$PSYNC_{HYST}$	Hysteresis	0.1	—	—	V
$PSYNC_{VOL}$	Low level output threshold (I = 2.0 mA)	—	—	0.5	V
$PSYNC_{IPD}$	Internal pull-down current source	7	10	13	µA
$PSYNC_{RPU}$	External pull-up resistor to VBOS	—	10	—	kΩ
$PSYNC_{COUT}$	External decoupling capacitor	—	0.1	—	µF
$PSYNC_{TFB}$	Feedback filtering time	6	10	15	µs

20 I²C interface

20.1 I²C interface overview

The FS5502 use an I²C interface following the high-speed mode definition up to 3.4 Mbit/s. I²C interface protocol requires a device address for addressing the target IC on a multi-device bus. The FS5502 has two device address: one to access the main logic and one to access the fail-safe logic. These two I²C addresses are set by OTP.

The I²C interface is using a dedicated power input pin VDDI2C and it's compatible with 1.8 V / 3.3 V input supply. Timing, diagrams, and further details can be found in the NXP I²C specification UM10204 rev6.

Table 75. I²C message arrangement

B39	B38	B37	B36	B35	B34	B33	B32	B31	B30	B29	B28	B27	B26	B25	B24
ID_6-0							0	0	0	Adr_5-0					
Device address							Read/Write			Register address					
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8
Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8	Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Data MSB								Data LSB							
								B7	B6	B5	B4	B3	B2	B1	B0
								CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
								CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0

20.2 Device address

The FS5502 has two device address: one to access the Main logic and one to access the Fail-safe logic.

B39	B38	B37	B36	B35	B34	B33
0	1	OTP	OTP	OTP	OTP	M/FS

The I²C addresses have the following arrangement:

- Bit 39: 0
- Bit 38: 1
- Bit 37 to 34: OTP value
- Bit 33: 0 to access the main logic, 1 to access the fail-safe logic

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

20.3 Cyclic redundant check

An 8 bit CRC is required for each Write and Read I2C command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two.

The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'

The following table shows an example of CRC encoding HW implementation:

CRC calculation using XOR:

CRC_7 = XOR (B38, B35, B32, B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1, 1)
CRC_6 = XOR (B37, B34, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1)
CRC_5 = XOR (B39, B36, B33, B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1, 1)
CRC_4 = XOR (B39, B38, B35, B32, B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1, 1, 1)
CRC_3 = XOR (B37, B35, B34, B32, B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1, 1)
CRC_2 = XOR (B39, B38, B36, B35, B34, B33, B32, B27, B26, B24, B21, B20, B18, B16, B15, B13, B12 B10, B8, 1,1,1,1,1,1,1,1)
CRC_1 = XOR (B37, B34, B33, B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1)
CRC_0 = XOR (B39, B36, B33, B32, B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1, 1, 1)

CRC results examples:

- Main I2C device address: 0x20
- Fail-safe I2C device address: 0x21

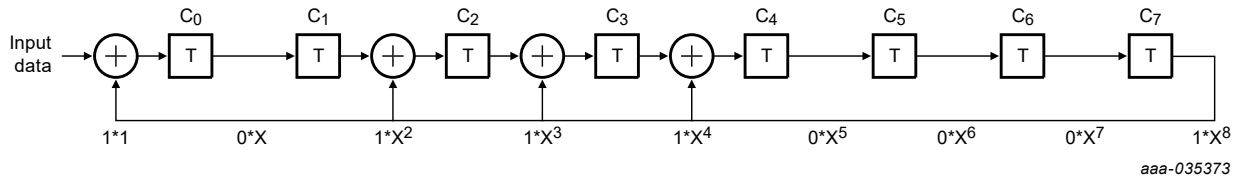


Figure 28. CRC encoder example

Table 76. CRC results example

Device address, R/W, 8 bit (Hex)	00, Register address, 8 bit (Hex)	Data MSB, 8 bit (Hex)	Data LSB, 8 bit (Hex)	CRC, 8 bit
0x40	0x02	0x00	0x00	0x31
0x42	0x01	0xD0	0x0D	0x8C

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

20.4 I²C electrical characteristics

Table 77. I²C electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VDDI2C	I²C interface power input	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
F_{SCL}	SCL clock frequency	—	—	3.4	MHz
$I2C_{VIL}$	SCL, SDA low level input voltage threshold	0.3 x V_{DDI2C}	—	—	V
$I2C_{VIH}$	SCL, SDA high level input voltage threshold	—	—	0.7 x V_{DDI2C}	V
SDA_{VOL}	Low level output voltage at SDA pin (I = 20 mA)	—	—	0.4	V
C_{I2C}	Input capacitance at SCL / SDA	—	—	10	pF
t_{SPSCL}	SLC pulse width filtering time, when 50 ns filter selected (fast speed, fast speed plus)	50	—	150	ns
t_{SPSDA}	SDA pulse width filtering time, when 50 ns filter selected (fast speed, fast speed plus)	50	—	150	ns
t_{SPHSCL}	SLC pulse width filtering time, when 10 ns filter selected (high speed)	10	—	25	ns
t_{SPHSDA}	SDA pulse width filtering time, when 10 ns filter selected (high speed)	10	—	25	ns

21 Maximum ratings

Table 78. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings could cause a malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage ratings					
VSUP1/2	DC voltage	power supply VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC voltage	WAKE1,2 pins; external serial resistor mandatory	−1.0	60	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	60	V
VMON1, VCOREMON	DC voltage	VMON1, VCOREMON pins	−0.3	60	V
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	–0.3	65.5	V
DBG	DC voltage	DBG pin	−0.3	10	V
LDO1_IN	DC voltage	LDO1_IN pin	−0.3	6.5	V
BUCKx_IN	DC voltage	BUCK1_IN, BUCK3_IN, BUCK3_INQ	−1.0	5.5	V
BUCKx_IN	Transient voltage < 3 µs	BUCK1_IN, BUCK3_IN, BUCK3_INQ	−1.0	6.5	V
BUCKx_SW	Transient voltage < 20 ns	BUCK1_SW, BUCK3_SW	−2.0	6.5	V
All other pins	DC voltage	at all other pins	−0.3	5.5	V
Current ratings					
I_WAKE	Maximum current capability	WAKE1,2	−5.0	5.0	mA
I_SUP	Maximum current capability	VSUP1,2	−5.0	—	mA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

22 Electrostatic discharge

22.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

22.2 Charged device model

- The device is protected up to ±500 V, according to AEC-Q100 - 011 charged device model standard. This protection is ensured at all pins.

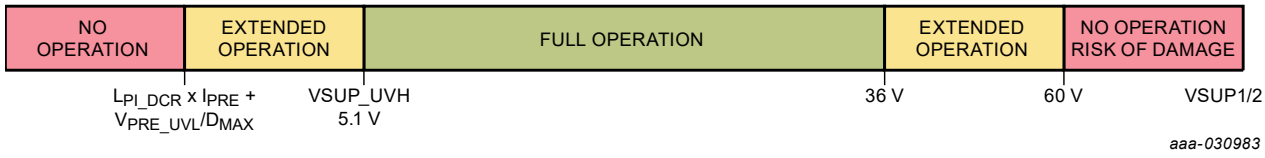
22.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2 pins.

23 Operating conditions



Assumptions

L_{PI_DCR} = 30 mΩ
D_{MAX} = 98.18 % with F_{PRE_SW} = 455 kHz and $T_{PRE_OFF_MIN}$ = 40 ns
I_{PRE} = 3.0 A
V_{RBD} = 0.56 V
V_{BAT_MIN} = 3.4 V when VPRE = V_{PRE_UVL}

Figure 29. Operating range

- Below VSUP_UVH threshold, the extended operation range depends on VPRE output voltage configuration and external components.
  - When VPRE is configured at 5.0 V, VPRE may not remain in its regulation range
  - VSUP minimum voltage depends on external components (L_{PI_DCR}) and application conditions (I_{PRE}, F_{PRE_SW})
- The FS5502 maximum continuous operating voltage is 36 V when VPRE is switching at 455 kHz.
- The FS5502 maximum continuous operating voltage is 36 V when VPRE is switching at 455 kHz. It has been validated at 48 V for limited duration of 15 minutes at room temperature to satisfy the jump-start requirement of 24 V applications. It can sustain 58 V load dump without external protection.
- When VPRE is switching at 2.2 MHz, the FS5502 maximum continuous operating voltage is 18 V. It is validated at 26 V for limited duration of 2 minutes at room

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

temperature to satisfy the jump-start requirement of 12 V applications and 35 V load dump.

24 Thermal characteristics

Table 79. Thermal ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient	2s2p circuit board [1]			°C/W
		Step-cut wettable flank	—	32	
		Dimple wettable flank	—	32	
$R_{\theta JA}$	Thermal resistance junction to ambient	2s6p circuit board [1]			°C/W
		Step-cut wettable flank	—	24	
		Dimple wettable flank	—	24	
$R_{\theta JB}$	Thermal resistance junction to board	2s2p circuit board [1]			°C/W
		Step-cut wettable flank	—	16	
		Dimple wettable flank	—	16	
$R_{\theta JB}$	Thermal resistance junction to board	2s6p circuit board [1]			°C/W
		Step-cut wettable flank	—	11	
		Dimple wettable flank	—	11	
$R_{\theta JC_BOT}$	Thermal resistance junction to case bottom	between the die and the solder pad on the bottom of the package [1]			°C/W
		Step-cut wettable flank	—	1.5	
		Dimple wettable flank	—	1.5	
$R_{\theta JP_TOP}$	Thermal resistance junction to package top	between package top and the junction temperature [1]			°C/W
		Step-cut wettable flank	—	4	
		Dimple wettable flank	—	4	
T_A	Ambient temperature (Grade 1)		−40	125	°C
T_J	Junction temperature (Grade 1)		−40	150	°C
T_{STG}	Storage temperature		−55	150	°C

[1] per JEDEC JESD51-2 and JESD51-8

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

25 Characteristics

Table 80. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
I_{SUP_NORMAL}	Current in Normal mode, all regulators ON (I_{OUT} = 0)	—	15	25	mA
$I_{SUP_STANDBY}$	Current in Standby mode, all regulators OFF except VBOS	—	5	10	mA
I_{SUP_OFF1}	Current in OFF mode (Power Down), T_A < 85 °C	—	10	15	µA
I_{SUP_OFF2}	Current in OFF mode (Power Down), T_A = 125 °C	—	—	25	µA
V_{SUP_UV7}	VSUP undervoltage threshold (7.0 V)	7.2	7.5	7.8	V
V_{SUP_UVH}	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 0	4.7	—	5.1	V
	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 1	6.0	—	6.4	V
V_{SUP_UVL}	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 0	4.0	—	4.4	V
	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 1	5.3	—	5.7	V
T_{SUP_UV}	V_{SUP_UV7}, V_{SUP_UVH} and V_{SUP_UVL} filtering time	6.0	10	15	µs

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

26 Application information

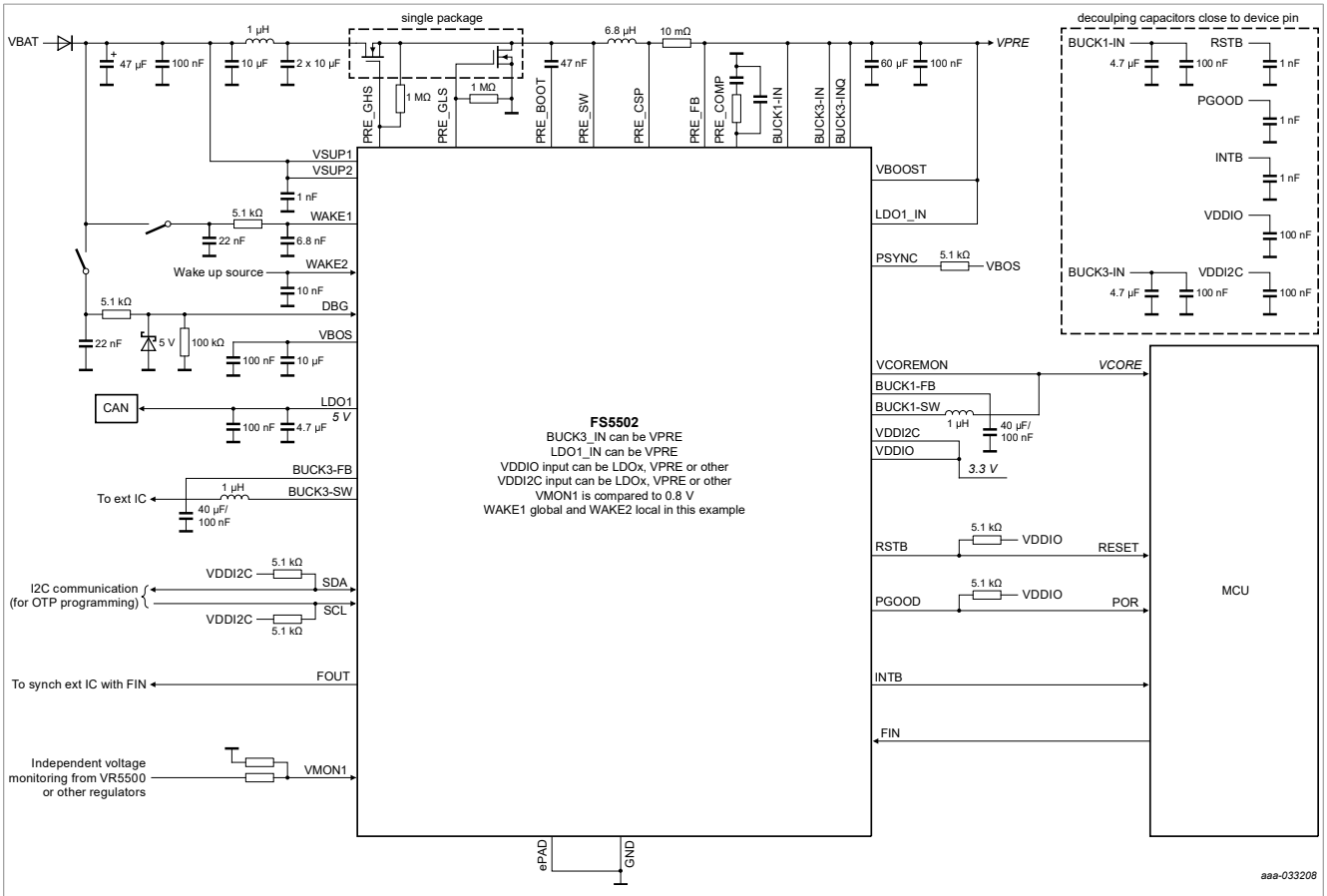


Figure 30. FS5502 Application diagram

27 Fail-safe domain description

27.1 Functional description

The fail-safe domain is electrically independent and physically isolated. The fail-safe domain is supplied by its own reference voltages and current, has its own oscillator.

The fail-safe domain and the dedicated pins are represented in Figure 31:

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

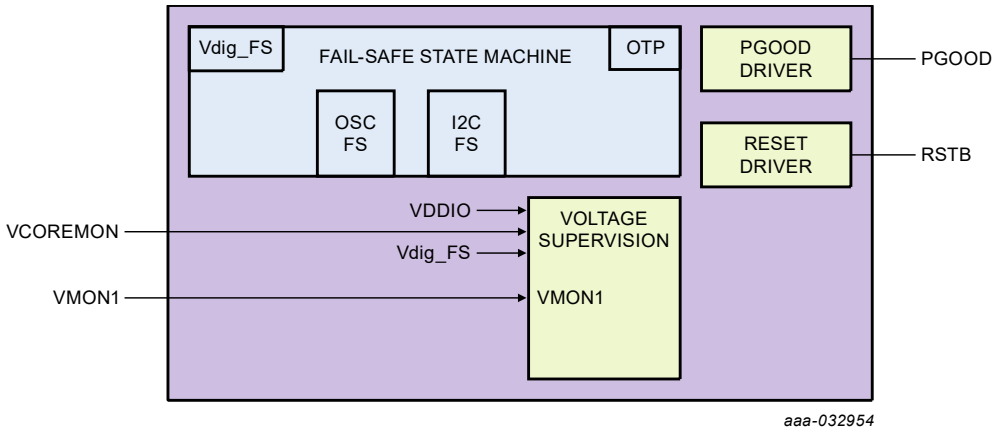


Figure 31. Fail-safe block diagram

27.2 Voltage supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of VCOREMON, VDDIO and VMON1 input pins. When an overvoltage occurs on a FS5502 regulator monitored by one of these pins, the associated FS5502 regulator is switched off till the fault is removed. The voltage monitoring is active as soon as FS_ENABLE=1 and UV/OV flags are then reported accordingly.

27.2.1 VCOREMON monitoring

VCOREMON input pin is dedicated to BUCK1. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VCOREMON_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 81. VCOREMON error impact configuration

VCOREMON_OV_FS_IMPACT[1:0]	VCOREMON OV impact on RSTB
00	No effect on RSTB
01	Reserved
1x (default)	**RSTB is asserted**
Reset condition	POR

VCOREMON_UV_FS_IMPACT[1:0]	VCOREMON UV impact on RSTB
00	No effect on RSTB
01 (default)	No effect on RSTB
1x	RSTB is asserted
Reset condition	POR

Table 82. VCOREMON electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VCOREMON_OV_min	Overvoltage threshold minimum	—	+4.5	—	%

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 82. VCOREMON electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VCOREMON_OV_max	Overvoltage threshold maximum	—	+12	—	%
VCOREMON_OV_step	Overvoltage threshold step (OTP_VCOREOVTH[7:0] bits)	—	+0.5	—	%
VCOREMON_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TCOREMON_OV	Overvoltage filtering time (OTP_VCORE_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VCOREMON_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VCOREMON_UV_max	Undervoltage threshold maximum	—	−12	—	%
VCOREMON_UV_step	Undervoltage threshold step (OTP_VCOREUVTH[7:0] bits)	—	−0.5	—	%
VCOREMON_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TCOREMON_UV	Undervoltage filtering time (OTP_VCORE_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

27.2.2 Static voltage scaling (SVS)

A static voltage scaling function is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1. The SVS configuration must be done in INIT_FS phase. The offset value is configurable by I^2C with the SVS_OFFSET[4:0] bits and the exact complemented value shall be written in the NOT_SVS_OFFSET[4:0] bits.

Table 83. SVS offset configuration

SVS_OFFSET[4:0]	NOT_SVS_OFFSET[4:0]	Offset applied to BUCK1
0 0000 (default)	**1 1111**	**0 mV**
0 0001	1 1110	−6.25 mV
...	...	−6.25 mV step per bit
1 0000	0 1111	−100 mV
Reset condition	POR	

The BUCK1 output voltage transition starts when the NOT_SVS_OFFSET[4:0] I^2C command is received and confirmed good. If the NOT_SVS_OFFSET[4:0] I^2C command is not the exact opposite to the SVS_OFFSET[4:0] I2C command, the SVS procedure is not executed and the BUCK1 output voltage remains at its original value. The OV/UV threshold changes immediately when the NOT_SVS_OFFSET[4:0] I^2C command is received and confirmed good. Therefore, the BUCK1 output voltage transition is done within TCOREMON_OV.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

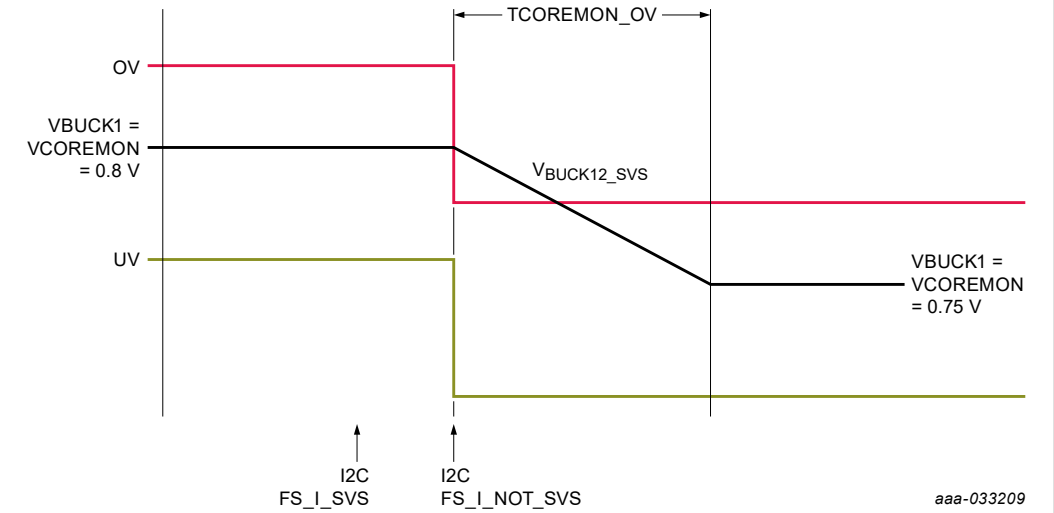


Figure 32. SVS principle

27.2.3 VDDIO monitoring

VDDIO input pin can be connected to VPRE, LDO1, BUCK3 or an external regulator. The regulator connected to VDDIO must be at 3.3 V or 5.0 V to be compatible with overvoltage and undervoltage monitoring thresholds. In order to turn OFF the regulator in case of overvoltage detection, the configuration of which regulator is connected to VDDIO is done with OTP_VDDIO_REG_ASSIGN[2:0] bits. If an external regulator (not delivered by the FS5502) is connected to VDDIO, this regulator cannot be turned OFF, but the overvoltage flag is reported to the MCU, which can take appropriate action. In all cases, the reaction on RSTB is configured with VDDIO_OV/UV_FS_IMPACT[1:0] bits.

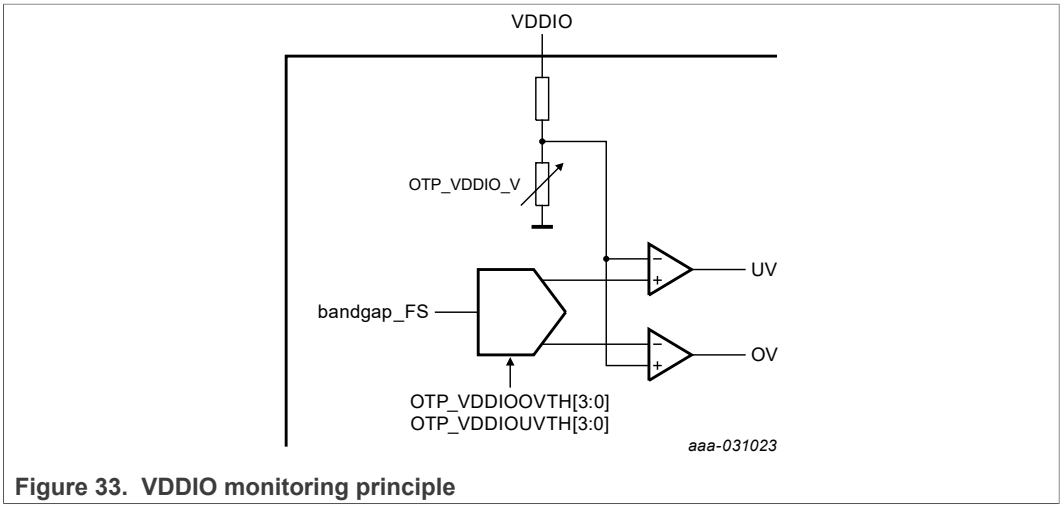


Figure 33. VDDIO monitoring principle

When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VDDIO_OV/UV_IMPACT[1:0] bits during the INIT_FS phase.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 84. VDDIO error impact configuration

VDDIO_OV_FS_IMPACT[1:0]	VDDIO OV impact on RSTB
00	No effect on RSTB
01	Reserved
1x (default)	**RSTB is asserted**
Reset condition	POR

VDDIO_UV_FS_IMPACT[1:0]	VDDIO UV impact on RSTB
00	No effect on RSTB
01 (default)	No effect on RSTB
1x	RSTB is asserted
Reset condition	POR

Table 85. VDDIO electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO_OV_min	Overvoltage threshold minimum	—	+4.5	—	%
VDDIO_OV_max	Overvoltage threshold maximum	—	+12	—	%
VDDIO_OV_step	Overvoltage threshold step (OTP_VDDIOOVTH[7:0] bits)	—	+0.5	—	%
VDDIO_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TVDDIO_OV	Overvoltage filtering time (OTP_VDDIO_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VDDIO_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VDDIO_UV_max	Undervoltage threshold maximum	—	−12	—	%
VDDIO_UV_step	Undervoltage threshold step (OTP_VDDIOUVTH[7:0] bits)	—	−0.5	—	%
VDDIO_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TVDDIO_UV	Undervoltage filtering time (OTP_VDDIO_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

27.2.4 VMON1 monitoring

Each VMON1 monitoring feature is enabled by OTP. VMON1 input pin can be connected to VPRE, LDO1, BUCK3 or even an external regulator. In order to turn OFF the regulator in case of Overvoltage detection, the configuration of which regulator is connected to VMON1 is done by I^2C in the register M_VMON_REGx. If an external regulator (not delivered by the FS5502) is connected to VMON1, this regulator cannot be turned OFF, but the Overvoltage flag is reported to the MCU, which can take appropriate action. In all cases, the fail-safe reaction on RSTB is configured with VMON1_OV/UV_FS_IMPACT[1:0] bits.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

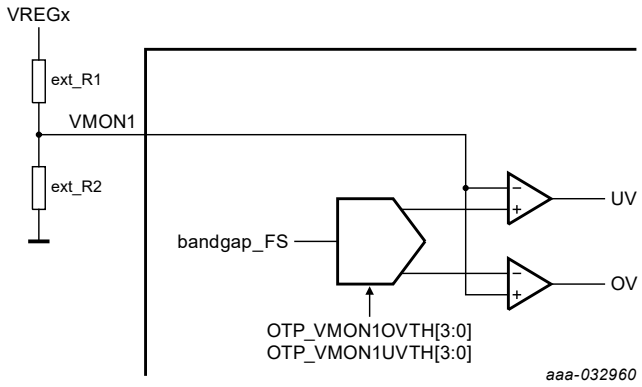


Figure 34. VMON1 monitoring principle

The external resistor bridge connected to VMON1 shall be calculated to deliver a middle point of 0.8V. It is recommended to use ±1 % or less resistor accuracy. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB is configurable with the VMON1_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 86. VMONx error impact configuration

VMONx_OV_FS_IMPACT[1:0]	VMON1 OV impact on RSTB
00	No effect on RSTB
01	Reserved
1x (default)	**RSTB is asserted**
Reset condition	POR

VMONx_UV_FS_IMPACT[1:0]	VMON1 UV impact on RSTB
00	No effect on RSTB
01 (default)	No effect on RSTB
1x	RSTB is asserted
Reset condition	POR

Table 87. VMON1 (without ext resistor accuracy) electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VMON1_OV_min	Overvoltage threshold minimum	—	+4.5	—	%
VMON1_OV_max	Overvoltage threshold maximum	—	+12	—	%
VMON1_OV_step	Overvoltage threshold step (OTP_VMON1OVTH[7:0] bits)	—	+0.5	—	%
VMON1_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TMON1_OV	Overvoltage filtering time (OTP_VMON1_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VMON1_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VMON1_UV_max	Undervoltage threshold maximum	—	−12	—	%

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 87. VMON1 (without ext resistor accuracy) electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VMON1_UV_step	Undervoltage threshold step (OTP_VMON1UVTH[7:0] bits)	—	−0.5	—	%
VMON1_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TMON1_UV	Undervoltage filtering time (OTP_VMON1_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs
VMON1_PD	Internal passive pull down	1	2	4	MΩ

27.3 Fault management

27.3.1 Fault source and reaction

In normal operation when RSTB is released, the fault error counter is incremented when a fault is detected by the FS5502 fail-safe state machine. Table 88 lists the faults and their impact on PGOOD and RSTB pins according to the device configuration. The faults that are configured to not assert RSTB will not increment the fault error counter. In that case, only the flags are available for MCU diagnostic.

Table 88. Application related fail-safe fault list and reaction

In Orange, the reaction in not configurable.

In Green, the reaction is configurable by OTP for PGOOD and I^2C for RSTB during INIT_FS.

Apps related fail-safe faults	FLT_ERR_CNT increment	RSTB assertion	PGOOD assertion
VCOREMON_OV	+1	VCOREMON_OV_FS_IMPACT[1]	OTP config
VDDIO_OV	+1	VDDIO_OV_FS_IMPACT[1]	OTP config
VMON1_OV	+1	VMON1_OV_FS_IMPACT[1]	OTP config
VCOREMON_UV	+1	VCOREMON_UV_FS_IMPACT[1]	OTP config
VDDIO_UV	+1	VDDIO_UV_FS_IMPACT[1]	OTP config
VMON1_UV	+1	VMON1_UV_FS_IMPACT[1]	OTP config
External RESET (out of extended RSTB)	+1	Yes (low externally)	No
RSTB pulse request by MCU	No	Yes	No
RSTB short to high	+1	No (high externally)	No
REG_CORRUPT = 1	+1	No	No
OTP_CORRUPT = 1	+1	No	No

If OTP_PGOOD_RSTB = 0 (default configuration), RSTB and PGOOD pins work independently according to Table 88. If OTP_PGOOD_RSTB = 1, RSTB and PGOOD pins work concurrently and all the faults asserting RSTB will also assert PGOOD.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

27.3.2 Fault error counter

The FS5502 integrates a configurable fault error counter that counts the number of faults related to the device itself and also caused by external events. The fault error counter starts at level 1 after a POR or resuming from Standby. The final value of the fault error counter is used to transition in DEEP-FS mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the INIT_FS phase.

Table 89. Fault error counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Fault error counter max value configuration
00	2
01 (default)	**6**
10	8
11	12
Reset condition	POR

27.4 PGOOD, RSTB

These two output pins have a hierarchical implementation in order to guarantee the safe state.

- PGOOD has the priority one. If PGOOD is asserted, RSTB is asserted.
- RSTB has the priority two. If RSTB is asserted, PGOOD may not be asserted.

27.4.1 PGOOD

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU. PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pull-down RPD ensures PGOOD low level in Standby and Power down mode. VCOREMON, VDDIO, VMON1 can be assigned to PGOOD by OTP.

PGOOD is asserted low by the FS_LOGIC when any of the assigned regulators are in undervoltage or overvoltage. When PGOOD is asserted low, RSTB is also asserted low. An internal pull up on the gate of the low-side MOS ensures PGOOD low level in case of FS_LOGIC failure.

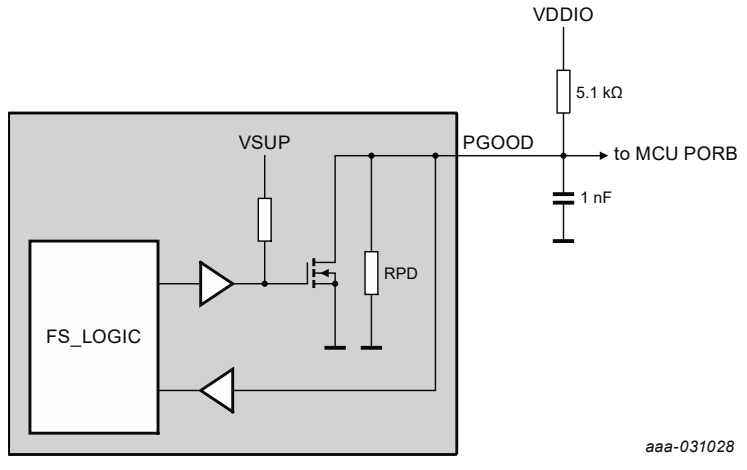


Figure 35. PGOOD pin implementation

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 90. PGOOD electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$PGOOD_{VIL}$	Low level input voltage threshold	1.0	—	—	V
$PGOOD_{VIH}$	High level input voltage threshold	—	—	2.0	V
$PGOOD_{HYST}$	Input voltage hysteresis	100	—	—	mV
$PGOOD_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.5	V
$PGOOD_{RPD}$	Internal pull-down resistor	200	400	800	kΩ
$PGOOD_{ILIM}$	Current limitation	4.0	—	20	mA
$PGOOD_{TFB}$	Feedback filtering time	8.0	—	15	µs

27.4.2 RSTB

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pull-down RPD ensure RSTB low level in Standby and Power down mode. RSTB assertion depends on the device configuration during INIT_FS phase. An internal pull up on the gate of the low-side MOS ensures RSTB low level in case of FS_LOGIC failure. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transitions in DEEP-FS mode.

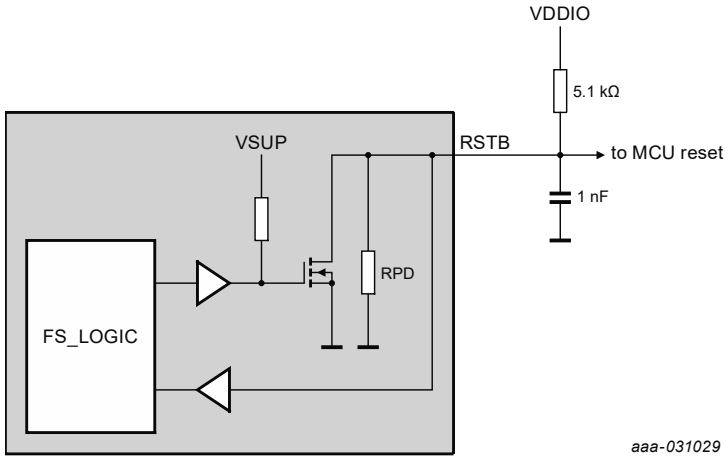


Figure 36. RSTB pin implementation

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 91. RSTB electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$RSTB_{VIL}$	Low level input voltage threshold	1.0	—	—	V
$RSTB_{VIH}$	High level input voltage threshold	—	—	2.0	V
$RSTB_{HYST}$	Input voltage hysteresis	100	—	—	mV
$RSTB_{VOL}$	Low level output voltage (I = 2.0 mA)	—	—	0.5	V
$RSTB_{RPB}$	Internal pull-down resistor	200	400	800	kΩ
$RSTB_{ILIM}$	Current limitation	4.0	—	20	mA
$RSTB_{TFB}$	Feedback filtering time	8.0	—	15	µs
$RSTB_{TSC}$	Short to high filtering time	500	—	800	us
$RSTB_{TLG}$	Long pulse (configurable with RSTB_DUR bit)	9.0	—	11	ms
$RSTB_{TST}$	Short pulse (configurable with RSTB_DUR bit)	0.9	—	1.1	ms
$RSTB_{T8S}$	8 second timer	7.0	8.0	9.0	s
$RSTB_{TRELEASE}$	Time to release RSTB from Wake-up or POR with all regulators started in Slot 0	—	8	—	ms

28 Package information

FS5502 package is a QFN (sawn), thermally enhanced wettable flanks, 8 x 8 x 0.85 mm, 0.5 mm pitch, 56 pins. The assembly can be done at two different NXP assembly sites with slight wettable flank difference but sharing the same PCB footprint.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

29 Package outline

29.1 Step-cut wettable flank

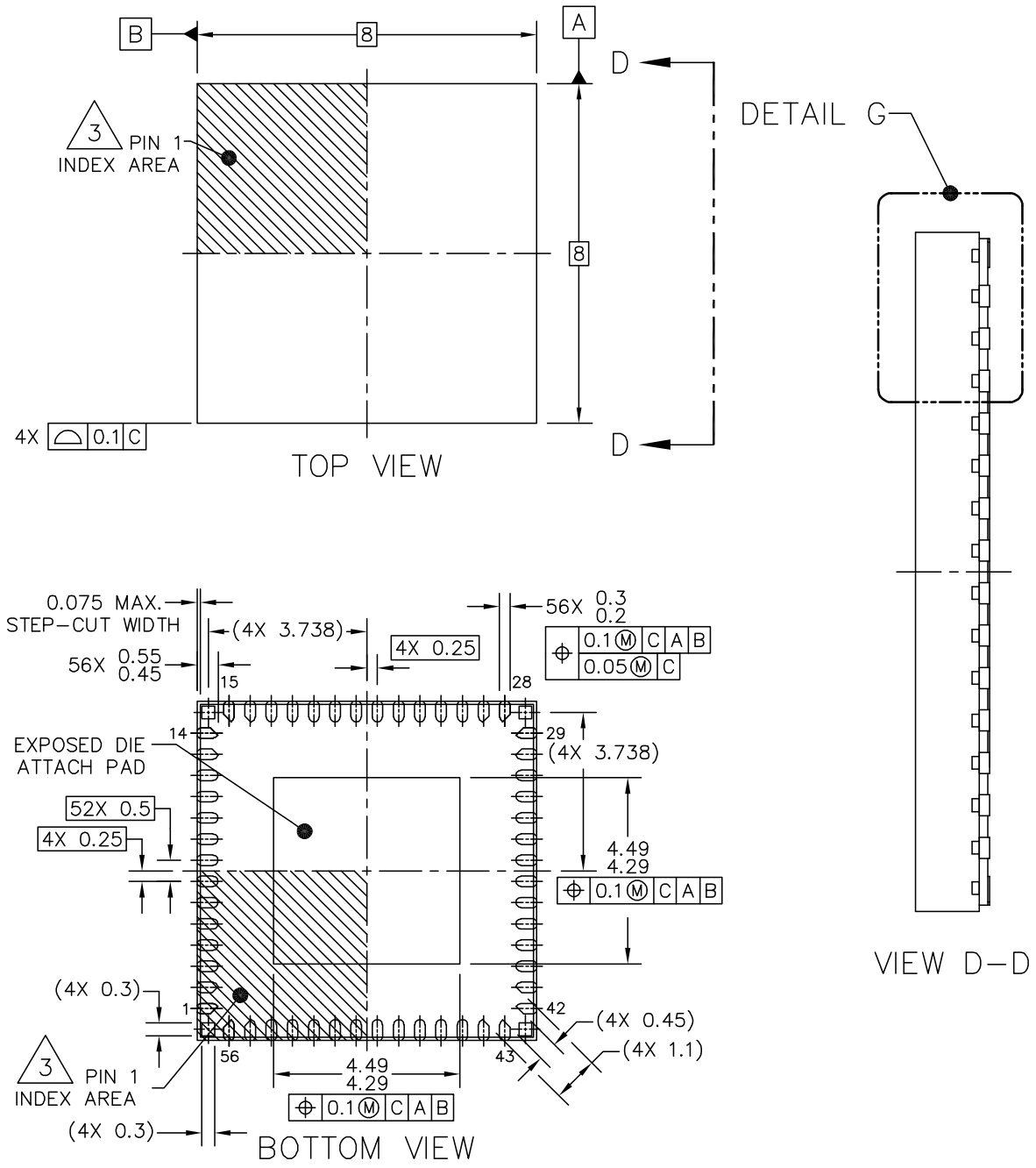


Figure 37. Package outline for HVQFN56 (SOT684-23, Step-cut)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

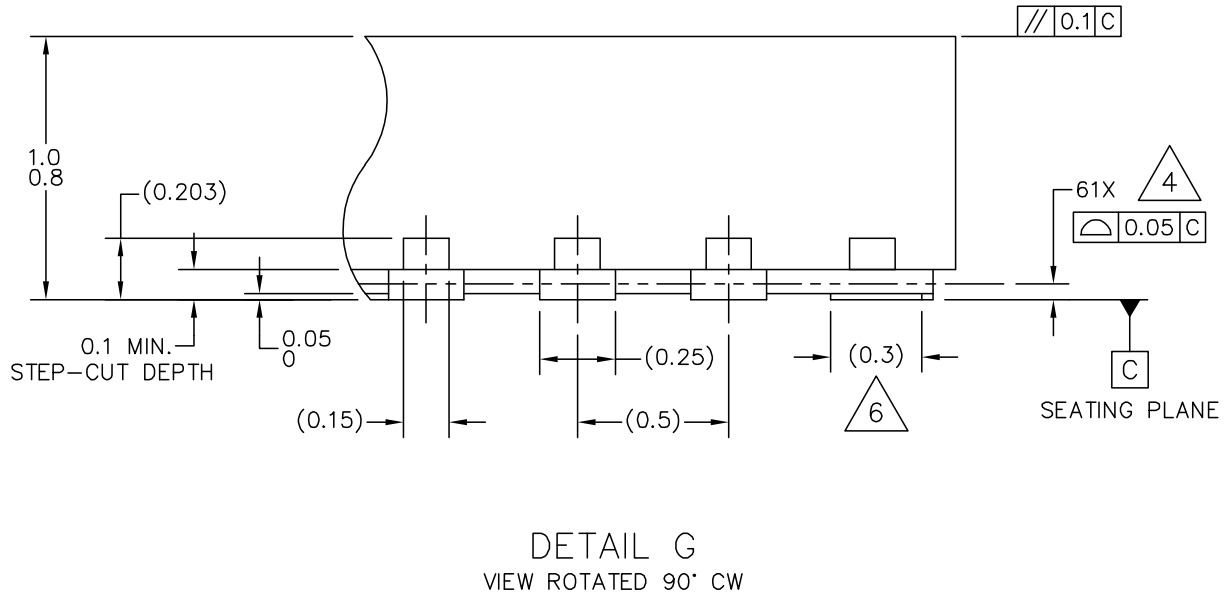


Figure 38. Package outline detail for HVQFN56 (SOT684-23, Step-cut)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

29.2 Dimple wettable flank

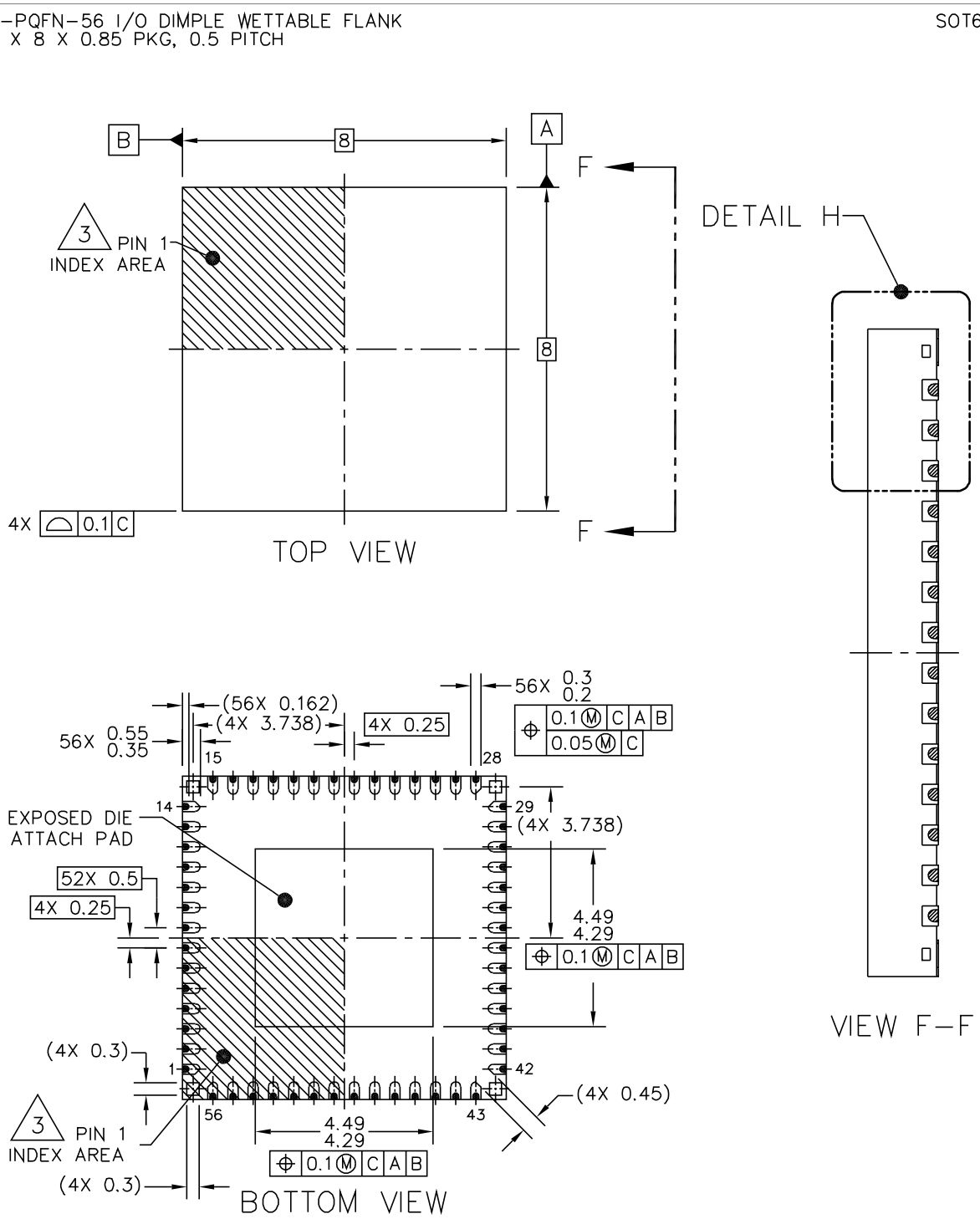


Figure 39. Package outline for HVQFN56 (SOT684-23, Dimple)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

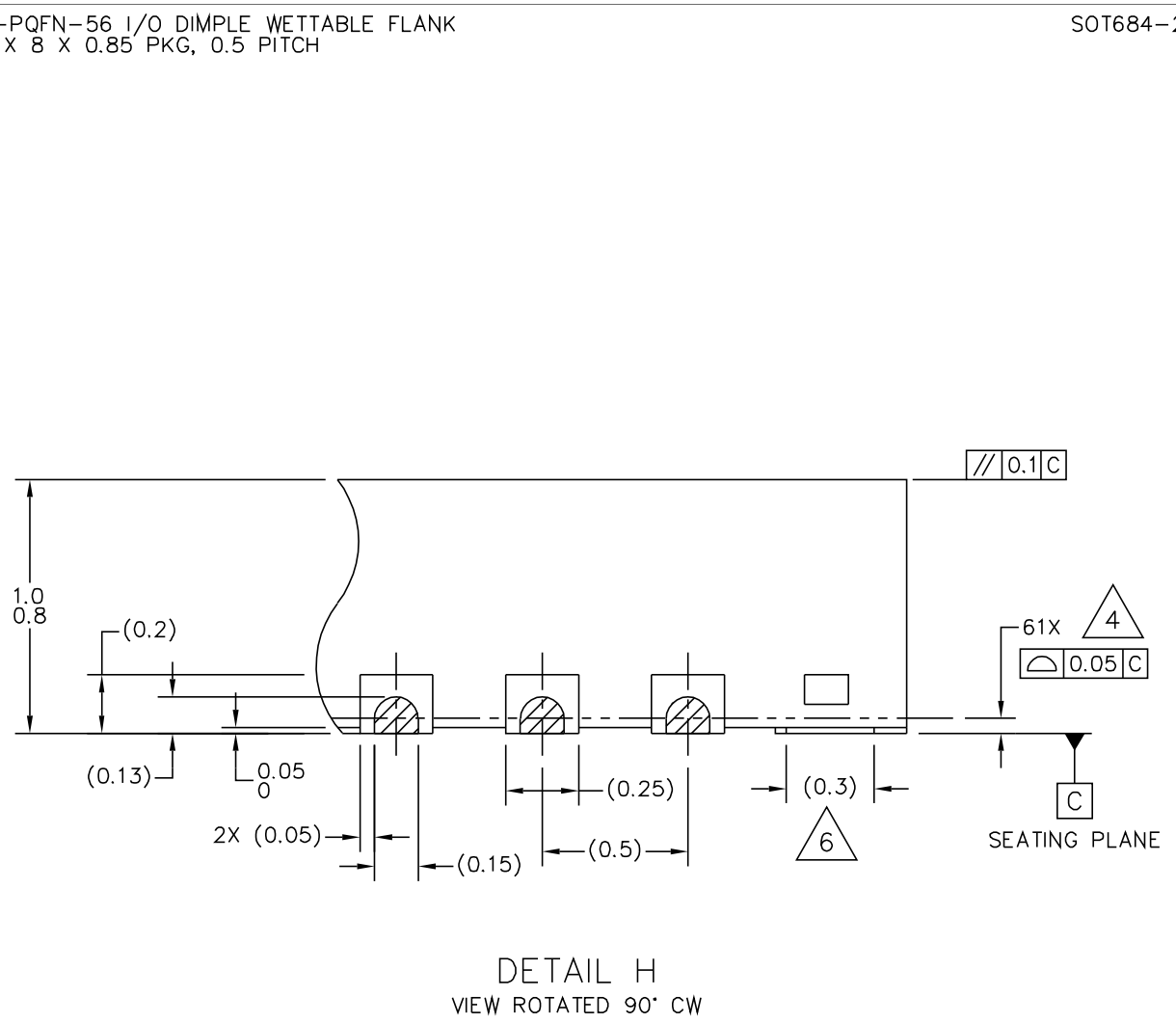


Figure 40. Package outline detail for HVQFN56 (SOT684-23, Dimple)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 41. Package outline notes for HVQFN56 (SOT684-23)

29.3 Package comparison

Table 92. Package comparison

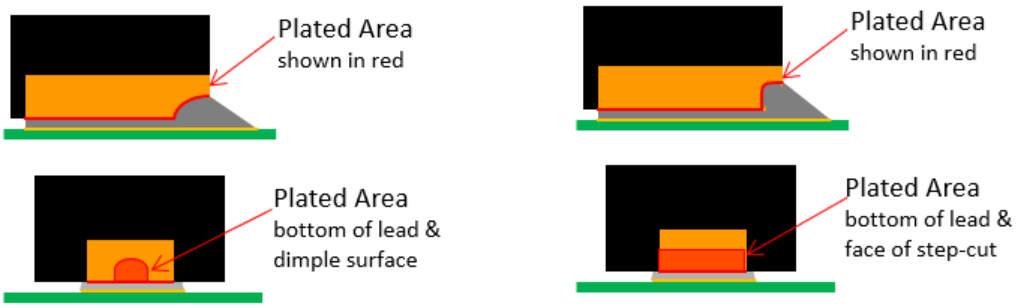
Item	Dimple wettable flank	Step-cut wettable flank
Package size (x,y,z)	8x8x0.85 mm3	8x8x0.85 mm3

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 92. Package comparison*...continued*

Item	Dimple wettable flank	Step-cut wettable flank
Package	QFN56 8*8	QFN56 8*8
Epoxy	EN4900G*	EN4900G*
Wire	AuPdCu Wire 1.3mil	AuPdCu Wire 1.3mil
Compound	CEL-9240HF10AN4	G700LA fine catalyst
Lead frame	PPF+RT	SN Plated
Wettable flank	Dimple solution	Step Cut
Part number	MC33FS5502xxKS	MC33FS5502xxES
MSL / Reflow ℃	3 / 260	3 / 260



All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

30 Layout and PCB guidelines

30.1 Landing pad information

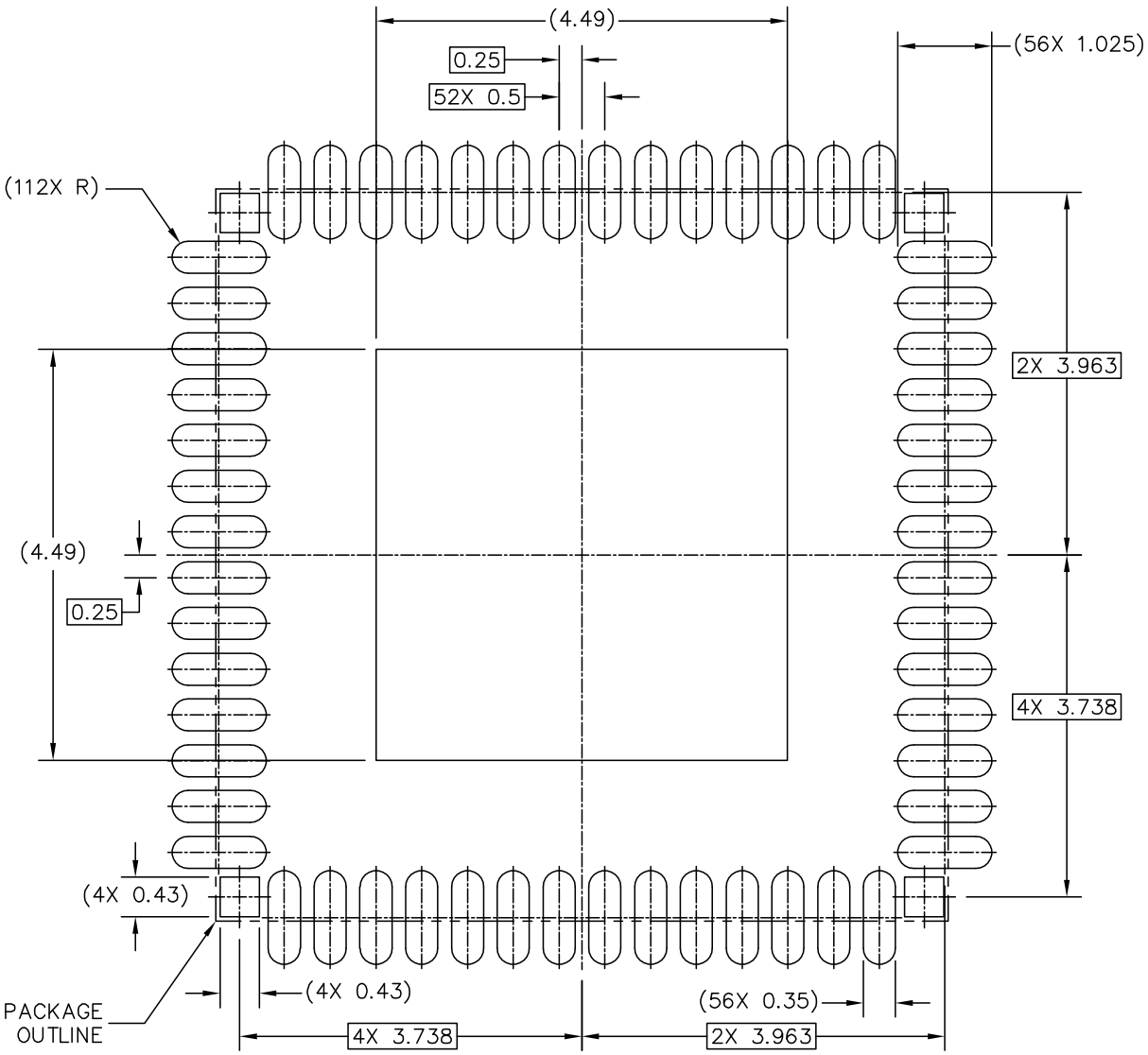


Figure 42. Solder mask pattern

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

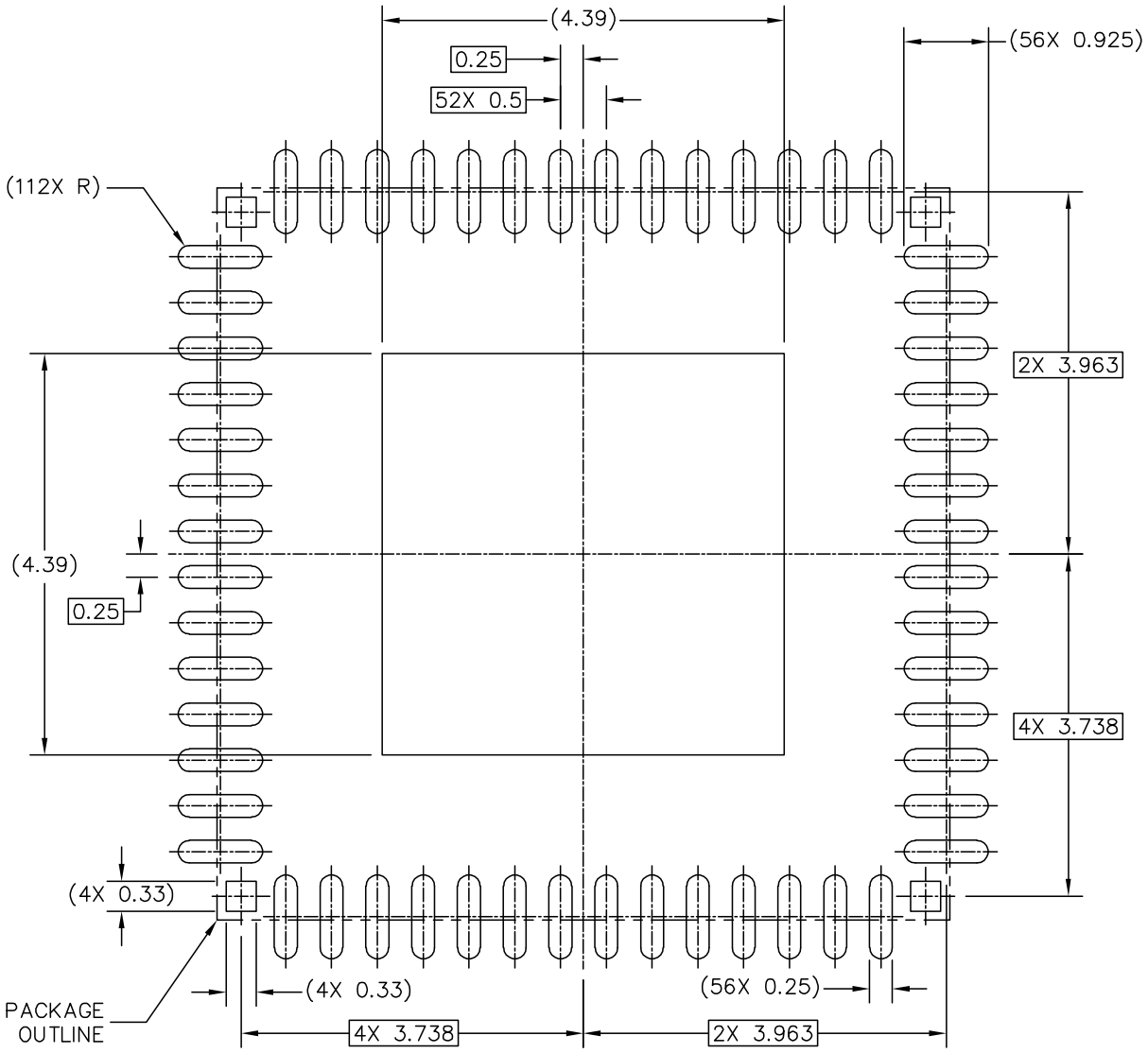


Figure 43. I/O pads and solderable areas

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

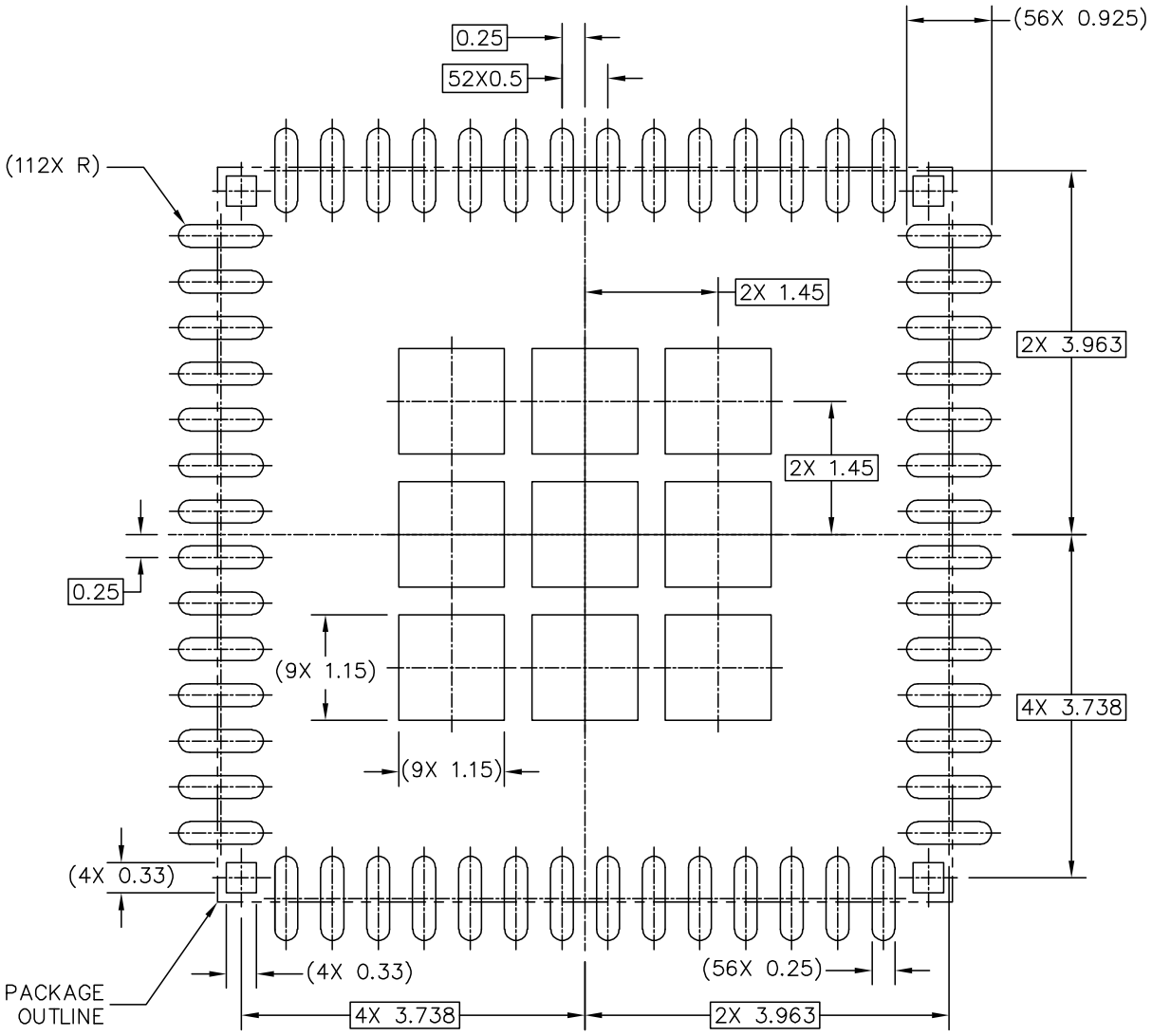


Figure 44. Solder paste stencil

30.2 Component selection

- SMPS input and output capacitors shall be chosen with low ESR (ceramic or MLCC type of capacitors). X7R ceramic type is preferred. Input decoupling capacitors shall be placed as close as possible to the device pin. Output capacitor voltage rating shall be selected to be 3x the voltage output value to minimize the DC bias degradation.
- SMPS inductors shall be shielded with ISAT higher than maximum inductor peak current.

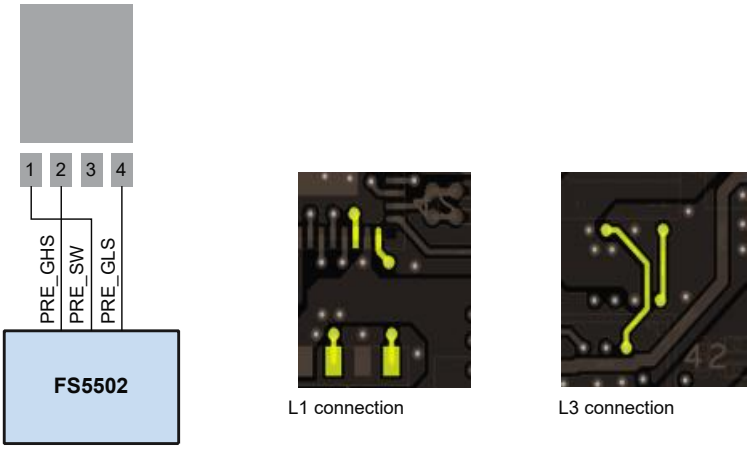
30.3 VPRE

- Inductor charging and discharging current loop is designed as small as possible.
- Input decoupling capacitors are placed close to the high-side drain transistor pin.
- The boot strap capacitor is placed close to the device pin using wide and short track to connect to the external low-side drain transistor.

All information provided in this document is subject to legal disclaimers.

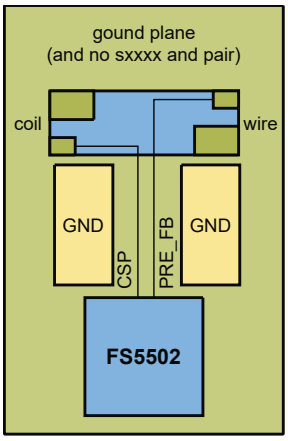
© NXP B.V. 2021. All rights reserved.

- PRE_GLS, PRE_GHS and PRE_SW tracks are wide and short and should not cross any sensitive signal (current sensing, for example).



implementation
Note : L2 is system ground.

- PRE_FB used as voltage feedback and current sense shall be connected to R_{SHUNT} and routed as a pair with CSP.



layout as a pair
do not cross any noisy signal

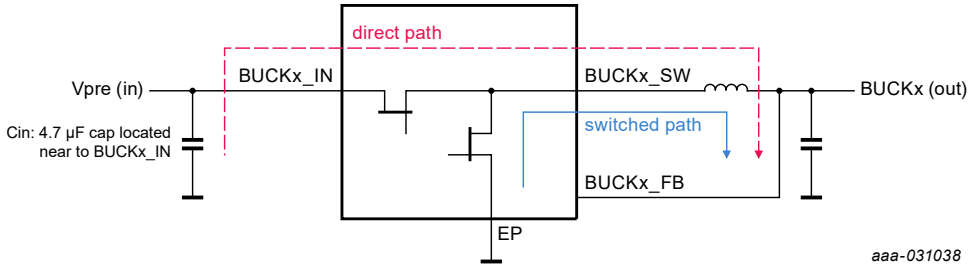
- The external transistor thermal shape should be in the range of 25 x 25 mm for optimum Rth.
- The LFPAK56 application note can give better insight: http://assets.nexperia.com/documents/application-note/AN10874.pdf

All information provided in this document is subject to legal disclaimers.

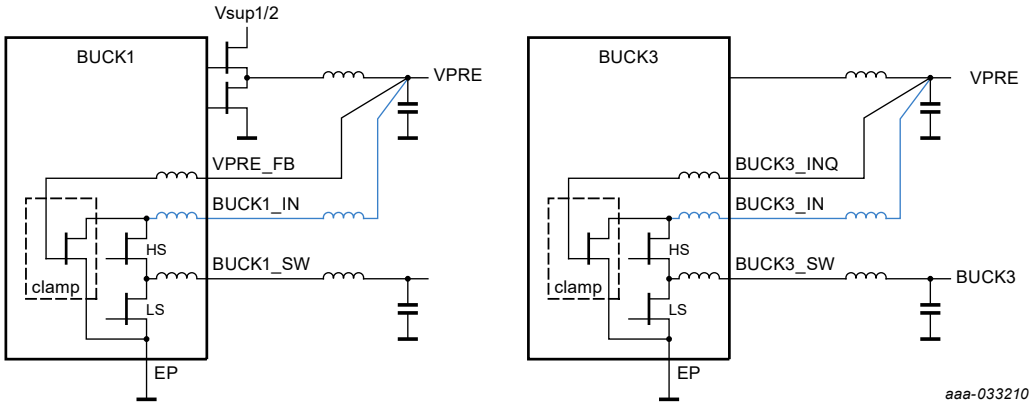
© NXP B.V. 2021. All rights reserved.

30.4 VBUCKx

- Inductor charging and discharging current loop is designed as small as possible.



- Input decoupling capacitors is placed close to BUCKx_IN pins.
- BUCK3_FB and BUCK3_INQ pins shall be tied to the same capacitor, VPRE output capacitor depending on BUCK3_IN supply selected (in the blue path below, the coil is parasitic from tracks). In the package, the coil is parasitic from the bonding.



31 EMC compliance

The FS5502 EMC performance will be verified against BISS generic IC EMC test specification version 2.0 from 07.2012 and FMC1278 electromagnetic compatibility specification for electrical/electronic components and subsystems from 2016 with the following specific conditions:

- Conducted emission: IEC 61967-4
  - Global pins: VBAT (Vsup1 and Vsup2), WAKE1/2, 150 Ω method, 12-M level
  - Local pins: VPRE, BUCK1/3, LDO1, 150 Ω method, 10-K level

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

- Conducted immunity: IEC 62132-4
  - Global pins: VBAT (Vsup1 and Vsup2), 36 dBm, Class A (no state change on RSTB, PGOOD and all regulators in spec)
  - Global pins: WAKE1, WAKE2, 30 dBm, Class A (no state change on RSTB, PGOOD and all regulators in spec)
  - Local pins: RSTB, PGOOD, VDDIO, VDDI2C, VBOS, 12 dBm, Class A (no state change on RSTB, PGOOD and all regulators in spec)
  - Supply pins: VPRE, BUCK1/3, LDO1, 12 dBm, Class A (no state change on RSTB, PGOOD and all regulators in spec)
- Radiated emission: FMC1278 from July 2015
  - Compliance with FMC1278 RE310 Level 2 requirement in Normal mode
- Radiated immunity: FMC1278 from July 2015
  - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode,
  - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode,
  - No wake up when injecting FMC1278 RI112 Level 2 requirement in Standby mode

32 References

[1] **FS5502_PDTCALC**[1] — VPRE compensation network calculation and power dissipation tool (Excel file)

[2] **FS5502_OTP_Mapping**[1] — OTP programming configuration (Excel file)

[3] **FS5502_VPRE_Simplis_Model**[1] — Simplis model for stability and transient simulations

[4] **Schematic**[1] — Reference schematic in Cadence and PDF formats

[5] **Layout**[1] — Reference layout in Cadence format

[6] **EVB**[1] — Evaluation board (EVB)

[7] **FlexGUI**[1] — Graphical user interface to be used with the EVB

[1] Contact NXP sales representative.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

33 Revision history

Table 93. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FS5502 v.4.0	20211027	Product data sheet	CIN 202110030I	FS5502 v.3.0
Modifications	• Table 1: added MC33FS5502Y0KS and MC33FS5502Y3KS parts and OTP links • Table 48: updated bit position of FS_DIG_REF_OV and FS_OSC_DRIFT bits • Table 60: updated description for OTP_CFG_UVOV_3 register • Table 64: updated VBUCK1_SOFT_START description • Table 65: updated description for $T_{BUCK3_SOFT_START}$ (1.8 V replaced by 1.1 V) • Section 16.5: updated Figure 21 • Table 79: updated table to include step-cut and wettable flank values • Section 29: added drawings of dimple wettable flank type package for MC33FS5502xxKS • Section 30: updated Dimple wettable flank type package information			
FS5502 v.3.0	2020127	Product data sheet	201912015I	FS5502 v.2.1
Modifications	• Global: multiple formatting and wording updates, deleted "SPI" references • Global: changed data sheet status from Preliminary to Product • Section 5: replaced PC part by MC and added MC33FS5502Y3ES • Table 2: updated ground pin description • Table 78: added values for BUCKx_SW and updated min value for DC voltage (replaced −1.0 by −0.3) • Section 12.1: updated values in Table 57 • Table 79: updated T_A and T_J description (added "Grade1") • Figure 7: corrected typo (replaced WAKE1 by WAKE1/2) • Table 4: updated T_{DBG} values and unit • Table 21: updated reset value for Bit 22 and Bit 23 (replaced 0 by 1) • Table 49: updated reset value for Bit 17 and Bit 22 (replaced 0 by 1) • Table 57: corrected typo (replaced "OTP_CFG_BUCK2_1" by "OTP_CFG_BUCK1_3 and "OTP_CFG_BUCK2_2" by "OTP_CFG_BUCK1_4" • Table 59: updated OTP_CFG_BUCK1_2 register description (replaced 2.6 A by Reserved) • Table 59: updated OTP_CFG_CLOCK_4 register description • Section 14.1: updated description (first paragraph) • Section 14.3: updated calculation method • Section 18.5: updated description • Section 14.5: updated description and values in Table 63 • Section 23: updated assumptions and description (replaced "V_{FPRE_SW}" by "F_{PRE_SW}") • Table 91: updated min and max values for $RSTB_{ILIM}$ (replaced 6.0 by 4.0 and 22 by 20) • Section 8.4: updated description and corrected typo in Figure 5 • Section 8.5: updated T_{DBG} description • Section 20.3: enhanced description (added Figure 28 and Table 76) • Section 22.2: updated description for charged device model • Section 30.3, Section 30.4: updated description • Table 59: updated OTP description • Table 60: updated OTP_CFG_UVOV_3 register description • Table 61, Table 62, Table 64, Table 65: updated parameters • Section 14.6: updated Figure 13 • Table 13: updated reset value for Bit 12 and Bit 11 (replaced OTP by 1) • Section 10.16: updated read and rest values and register bit description • Table 90: updated min and max values for $PGOOD_{ILIM}$ • Section 9: corrected typo (deleted R/W SPI column)			
FS5502 v.2.1	20190521	Preliminary data sheet	—	FS5502 v.2

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 93. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications	• Changed data sheet status from Objective to Preliminary • Section 8.3, last sentence, changed "...asserting the Safety pins (PGOOD, RSTB)..." to "...asserting the pins (PGOOD, RSTB)..." • Section 9, changed register name from "FS_DIAG_SAFETY" to "FS_DIAG" • Table 35, changed register name from "FS_DIAG_SAFETY" to "FS_DIAG" • Table 36, changed register name from "FS_DIAG_SAFETY" to "FS_DIAG" • Section 11.10 – Changed section title from "FS_DIAG_SAFETY register" to "FS_DIAG register" – Changed name of Table 51 from "FS_DIAG_SAFETY register bit allocation" to "FS_DIAG register bit allocation" – Changed name of Table 52 from "FS_DIAG_SAFETY register bit description" to "FS_DIAG register bit description" • Section 14.1, deleted last sentence: "These monitoring are not safety related." • Section 27, changed section title from "Functional safety" to "Fail Safe domain description" • Section 27.4, changed "These two safety output pins..." to "These two output pins..."			
FS5502 v.2	20190416	Objective data sheet	—	FS5502 v.1
FS5502 v.1	20190228	Objective data sheet	—	—

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

34 Legal information

34.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

34.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

34.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"),

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

34.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Tables

Tab. 1. Ordering information 2
Tab. 2. Pin description 4
Tab. 3. Connection of unused pins 6
Tab. 4. Electrical characteristics 12
Tab. 5. Main writing registers overview 13
Tab. 6. Main reading registers overview 14
Tab. 7. M_FLAG register bit allocation 14
Tab. 8. M_FLAG register bit description 15
Tab. 9. M_MODE register bit allocation 16
Tab. 10. M_MODE register bit description 16
Tab. 11. M_REG_CTRL1 register bit allocation 17
Tab. 12. M_REG_CTRL1 register bit description 17
Tab. 13. M_REG_CTRL2 register bit allocation 18
Tab. 14. M_REG_CTRL2 register bit description 18
Tab. 15. M_CLOCK register bit allocation 19
Tab. 16. M_CLOCK register bit description 19
Tab. 17. M_INT_MASK1 register bit allocation 20
Tab. 18. M_INT_MASK1 register bit description 21
Tab. 19. M_INT_MASK2 register bit allocation 22
Tab. 20. M_INT_MASK2 register bit description 22
Tab. 21. M_FLAG1 register bit allocation 23
Tab. 22. M_FLAG1 register bit description 23
Tab. 23. M_FLAG2 register bit allocation 24
Tab. 24. M_FLAG2 register bit description 25
Tab. 25. M_VMON_REGx register bit allocation 26
Tab. 26. M_VMON_REGx register bit description 26
Tab. 27. M_LVB1_SVS register bit allocation 27
Tab. 28. M_LVB1_SVS register bit description 27
Tab. 29. M_MEMORY0 register bit allocation 27
Tab. 30. M_MEMORY0 register bit description 28
Tab. 31. M_MEMORY1 register bit allocation 28
Tab. 32. M_MEMORY1 register bit description 28
Tab. 33. M_DEVICEID register bit allocation 28
Tab. 34. M_DEVICEID register bit description 29
Tab. 35. Fail-safe writing registers overview 29
Tab. 36. Fail-safe reading registers overview 30
Tab. 37. FS_GRL_FLAGS register bit allocation 30
Tab. 38. FS_GRL_FLAGS register bit description 30
Tab. 39. FS_I_OVUV_SAFE_REACTION1 register bit allocation 31
Tab. 40. FS_I_OVUV_SAFE_REACTION1 register bit description 31
Tab. 41. FS_I_OVUV_SAFE_REACTION2 register bit allocation 31
Tab. 42. FS_I_OVUV_SAFE_REACTION2 register bit description 32
Tab. 43. FS_I_FSSM register bit allocation 32
Tab. 44. FS_I_FSSM register bit description 32
Tab. 45. FS_I_SVS register bit allocation 33
Tab. 46. FS_I_SVS register bit description 34
Tab. 47. FS_OVUVREG_STATUS register bit allocation 34
Tab. 48. FS_OVUVREG_STATUS register bit description 35
Tab. 49. FS_SAFE_IOS register bit allocation 36
Tab. 50. FS_SAFE_IOS register bit description 36
Tab. 51. FS_DIAG register bit allocation 37
Tab. 52. FS_DIAG register bit description 37
Tab. 53. FS_INTB_MASK register bit allocation 38
Tab. 54. FS_INTB_MASK register bit description 38
Tab. 55. FS_STATES register bit allocation 38
Tab. 56. FS_STATES register bit description 39
Tab. 57. Main OTP_REGISTERS 40
Tab. 58. Fail-safe OTP_REGISTERS 41
Tab. 59. Main OTP bit description 41
Tab. 60. Fail-safe OTP bit description 46
Tab. 61. Best of supply electrical characteristics 52
Tab. 62. VPRE electrical characteristics 56
Tab. 63. VPRE external MOSFETs recommendation 58
Tab. 64. BUCK1 electrical characteristics 63
Tab. 65. BUCK3 electrical characteristics 69
Tab. 66. LDO1 electrical characteristics 71
Tab. 67. Manual frequency tuning configuration 73
Tab. 68. FOUT multiplexer selection 74
Tab. 69. Electrical characteristics 74
Tab. 70. WAKE1, WAKE2 electrical characteristics 75
Tab. 71. INTB electrical characteristics 75
Tab. 72. List of interrupts from main logic 76
Tab. 73. List of interrupts from fail-safe logic 76
Tab. 74. PSYNC electrical characteristics 78
Tab. 75. I2C message arrangement 79
Tab. 76. CRC results example 80
Tab. 77. I2C electrical characteristics 81
Tab. 78. Maximum ratings 81
Tab. 79. Thermal ratings 83
Tab. 80. Electrical characteristics 84
Tab. 81. VCOREMON error impact configuration 86
Tab. 82. VCOREMON electrical characteristics 86
Tab. 83. SVS offset configuration 87
Tab. 84. VDDIO error impact configuration 89
Tab. 85. VDDIO electrical characteristics 89
Tab. 86. VMONx error impact configuration 90
Tab. 87. VMON1 (without ext resistor accuracy) electrical characteristics 90
Tab. 88. Application related fail-safe fault list and reaction 91
Tab. 89. Fault error counter configuration 92
Tab. 90. PGOOD electrical characteristics 93
Tab. 91. RSTB electrical characteristics 94
Tab. 92. Package comparison 98
Tab. 93. Revision history 106

Figures

Fig. 1. Simplified application diagram of FS5502 2
Fig. 2. Block diagram of FS5502 3

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Fig. 3. Pin configuration for HVQFN56 4
Fig. 4. Simplified functional state diagram 8
Fig. 5. Power sequencing (VREGx PWR_UP) 10
Fig. 6. Power up sequence example 11
Fig. 7. Debug mode entry 12
Fig. 8. VPRE schematic 53
Fig. 9. Type 2 compensation network concept 54
Fig. 10. Phase and gain margin simulation 55
Fig. 11. Transient response simulation 56
Fig. 12. MOSFET gate charge definition 59
Fig. 13. VPRE theoretical efficiency 59
Fig. 14. BUCK1 standalone schematic 61
Fig. 15. Phase and gain margin simulation 62
Fig. 16. Transient response simulation 63
Fig. 17. BUCK1 theoretical efficiency 65
Fig. 18. BUCK3 schematic 66
Fig. 19. Phase and gain margin simulation 67
Fig. 20. Transient response simulation 68
Fig. 21. BUCK3 theoretical efficiency 70
Fig. 22. LDO1 block diagram 70
Fig. 23. Clock management block diagram 72
Fig. 24. Synchronization of two FS5502 77
Fig. 25. Two FS5502 synchronization timing diagram 77
Fig. 26. Synchronization of one FS5502 and one external PMIC (PF82) 78
Fig. 27. FS5502 and one PF82 synchronization timing diagram 78
Fig. 28. CRC encoder example 80
Fig. 29. Operating range 82
Fig. 30. FS5502 Application diagram 85
Fig. 31. Fail-safe block diagram 86
Fig. 32. SVS principle 88
Fig. 33. VDDIO monitoring principle 88
Fig. 34. VMON1 monitoring principle 90
Fig. 35. PGOOD pin implementation 92
Fig. 36. RSTB pin implementation 93
Fig. 37. Package outline for HVQFN56 (SOT684-23, Step-cut) 95
Fig. 38. Package outline detail for HVQFN56 (SOT684-23, Step-cut) 96
Fig. 39. Package outline for HVQFN56 (SOT684-23, Dimple) 97
Fig. 40. Package outline detail for HVQFN56 (SOT684-23, Dimple) 98
Fig. 41. Package outline notes for HVQFN56 (SOT684-23) 98
Fig. 42. Solder mask pattern 100
Fig. 43. I/O pads and solderable areas 101
Fig. 44. Solder paste stencil 102

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Simplified application diagram 2
5 Ordering information 2
6 Block diagram 3
7 Pinning information 4
7.1 Pinning 4
7.2 Pin description 4
7.3 Connection of unused pins 6
8 Functional description 8
8.1 Simplified functional state diagram 8
8.2 Main state machine 8
8.3 Fail-safe state machine 9
8.4 Power sequencing 9
8.5 Debug mode 11
9 Register mapping 12
10 Main register mapping 13
10.1 Main writing registers overview 13
10.2 Main reading registers overview 14
10.3 M_FLAG register 14
10.4 M_MODE register 16
10.5 M_REG_CTRL1 register 17
10.6 M_REG_CTRL2 register 18
10.7 M_CLOCK register 19
10.8 M_INT_MASK1 register 20
10.9 M_INT_MASK2 register 22
10.10 M_FLAG1 register 23
10.11 M_FLAG2 register 24
10.12 M_VMON_REGx register 26
10.13 M_LVB1_SVS register 27
10.14 M_MEMORY0 register 27
10.15 M_MEMORY1 register 28
10.16 M_DEVICEID register 28
11 Fail-safe register mapping 29
11.1 Fail-safe writing registers overview 29
11.2 Fail-safe reading registers overview 30
11.3 FS_GRL_FLAGS register 30
11.4 FS_I_OVUV_SAFE_REACTION1 register 31
11.5 FS_I_OVUV_SAFE_REACTION2 register 31
11.6 FS_I_FSSM register 32
11.7 FS_I_SVS register 33
11.8 FS_OVUVREG_STATUS register 34
11.9 FS_SAFE_IOs register 36
11.10 FS_DIAG register 37
11.11 FS_INTB_MASK register 38
11.12 FS_STATES register 38
12 OTP bits configuration 40
12.1 Overview 40
12.2 Main OTP bit description 41
12.3 Fail-safe OTP bit description 46
13 Best of supply 51
13.1 Functional description 51
13.2 Best of supply electrical characteristics 52
14 High voltage buck: VPRE 52
14.1 Functional description 52
14.2 Application schematic 53
14.3 Compensation network and stability 53
14.4 VPRE electrical characteristics 56
14.5 VPRE external MOSFETs 58
14.6 VPRE efficiency 59
14.7 VPRE not populated 60
15 Low voltage buck: BUCK1 60
15.1 Functional description 60
15.2 Application schematic: Single phase mode 60
15.3 Compensation network and stability 61
15.4 BUCK1 electrical characteristics 63
15.5 BUCK1 efficiency 64
16 Low voltage buck: BUCK3 65
16.1 Functional description 65
16.2 Application schematic 66
16.3 Compensation network and stability 66
16.4 BUCK3 electrical characteristics 69
16.5 BUCK3 efficiency 69
17 Linear voltage regulator: LDO1 70
17.1 Functional description 70
17.2 Application schematics 70
17.3 LDO1 electrical characteristics 71
18 Clock management 71
18.1 Clock description 71
18.2 Phase shifting 72
18.3 Manual frequency tuning 72
18.4 Spread spectrum 73
18.5 External clock synchronization 73
18.6 Electrical characteristics 74
19 I/O interface pins 75
19.1 WAKE1, WAKE2 75
19.2 INTB 75
19.3 PSYNC for two FS5502 77
19.4 PSYNC for FS5502 and external PMIC 78
20 I2C interface 79
20.1 I2C interface overview 79
20.2 Device address 79
20.3 Cyclic redundant check 80
20.4 I2C electrical characteristics 81
21 Maximum ratings 81
22 Electrostatic discharge 82
22.1 Human body model (JESD22/A114) 82
22.2 Charged device model 82
22.3 Discharged contact test 82
23 Operating conditions 82
24 Thermal characteristics 83
25 Characteristics 84
26 Application information 85
27 Fail-safe domain description 85
27.1 Functional description 85
27.2 Voltage supervisor 86
27.2.1 VCOREMON monitoring 86
27.2.2 Static voltage scaling (SVS) 87
27.2.3 VDDIO monitoring 88
27.2.4 VMON1 monitoring 89
27.3 Fault management 91

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

27.3.1 Fault source and reaction 91
27.3.2 Fault error counter 92
27.4 PGOOD, RSTB 92
27.4.1 PGOOD 92
27.4.2 RSTB 93
28 Package information 94
29 Package outline 95
29.1 Step-cut wettable flank 95
29.2 Dimple wettable flank 97
29.3 Package comparison 98
30 Layout and PCB guidelines 100
30.1 Landing pad information 100
30.2 Component selection 102
30.3 VPRE 102
30.4 VBUCKx 104
31 EMC compliance 104
32 References 105
33 Revision history 106
34 Legal information 108

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2021. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 October 2021
Document identifier: FS5502

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MC33FS5502Y0ES on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management