QorIQ LS1028A/LS1018A Data Sheet

LS1028A

- LS1028A has two cores and LS1018A has a single core.
- Two 32/64-bit ARM® Cortex®-A72 cores with the following capabilities:
  - Up to 1.5 GHz operation
  - Single-threaded cores with 48KB L1 instruction cache and 32KB L1 data cache
  - Single cluster of two cores sharing 1MB L2 cache
- Cache Coherent Interconnect (CCI-400)
  - Up to 400 MHz operation
- One 32-bit DDR3L/DDR4 SDRAM memory controller with ECC support
  - Up to 1.6 GT/s
- Four SerDes lanes for high-speed peripheral interfaces
  - Two PCI Express 3.0 controllers
  - One Serial ATA (SATA 6 Gbit/s) controller
  - Up to four SGMII interfaces supporting four switch ports at 1000 Mbps
  - Up to one 2.5G-SGMII, supporting one Ethernet controller
  - Up to four 2.5G-SGMII supporting four switch ports at 2.5 Gbps
  - Up to one QSGMII interface, supporting four switch ports
  - Supports 1000Base-KX
  - Up to one 10G-SXGMII, supporting one Ethernet controller at 2.5 Gbps, 1000 Mbps, 100 Mbps, and 10 Mbps
  - Up to one 10G-QXGMII, supporting four switch ports with independent rates of 2.5 Gbps, 1000 Mbps, 100 Mbps, and 10 Mbps
- One LCD controller and Display port/eDP interface
  - Supports Display port 1.3 and eDP 1.4
  - Supports link transfer rates up to HBR2 (5.4Gbit/s) and display resolution upto 4Kp60
- Graphics processing unit
  - Supports Geometry rate 100 Mtri/sec, Pixel rate 650 Mpixel/sec, GFLOPS(32-bit high precision) = 10.4
  - Supports OpenGL ES 3.0, 2.0, 1.1
  - Supports OpenCL 1.1, 1.2
- TSN-capable Ethernet Switch with four external ports
- Ethernet Controller (ENETC) with TSN functionality
  - One RGMII interface
  - One 1G/2.5G SerDes-based interface with TSN support
- Additional peripheral interfaces
  - Two high-speed USB 2.0/3.0 controllers with integrated PHY
  - Two Enhanced Secure Digital Host Controllers (eSDHC) supporting SD 3.0, eMMC 4.4 and eMMC 4.5 and eMMC 5.1
  - Two Controller Area Network (CAN) modules, optionally supporting Flexible Data-rate
  - Three Serial Peripheral Interface (SPI) controllers
  - Eight I2C controllers
  - One 16550-compliant DUART
  - Six LPUARTs
  - One FlexSPI controller
  - General Purpose IO (GPIO)
  - Eight FlexTimers/PWM controllers
  - Six Synchronous Audio Interface (SAI)
- One Queue Direct Memory Access Controller (qDMA)
- One Enhanced Direct Memory Access Controller (eDMA)
- Generic Interrupt Controller (GIC)
- Thermal Monitor Unit (TMU)
- FC-PBGA package, 17 mm x 17 mm

NXP reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 Introduction

LS1028A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP value-performance line of QorIQ communications processors. Featuring extremely power-efficient 64-bit Arm® Cortex®-A72 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.5 GHz.

This chip can be used for networking and wireless access points, industrial gateways, industrial automation, printing, imaging, and M2M for enterprise and consumer networking and router applications.

This figure shown below represents the block diagram of the chip.

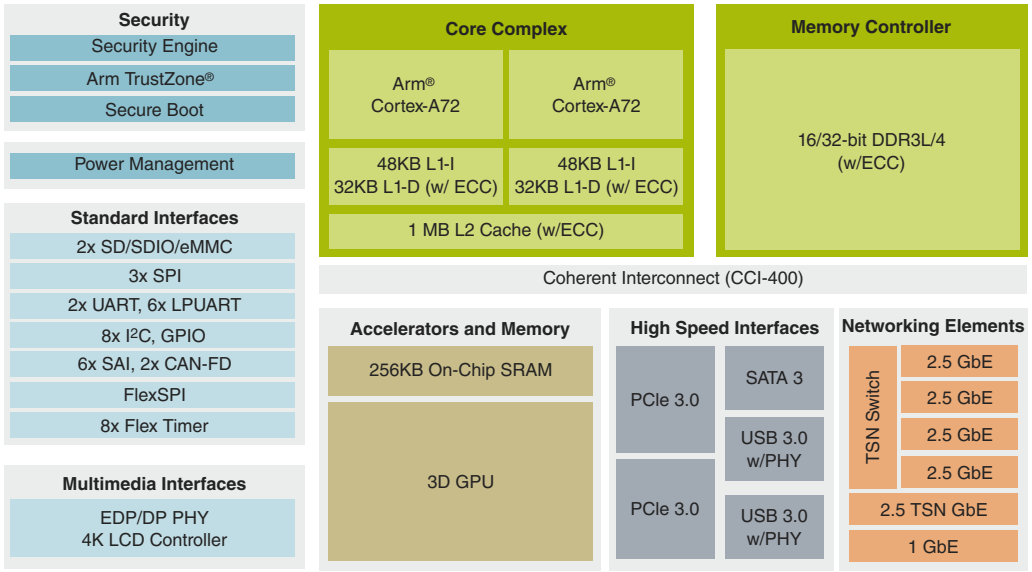


Figure 1. LS1028A block diagram

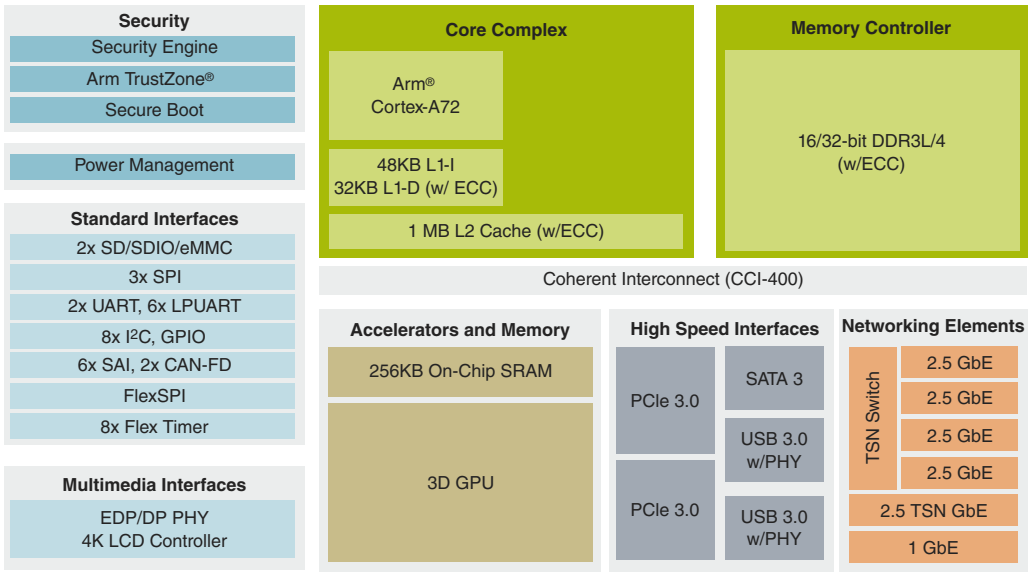


Figure 2. LS1018A block diagram

2 Pin assignments

2.1 448 ball layout diagrams

This figure shows the complete view of the LS1028A BGA ball map diagram. Figure 4. on page 7, Figure 5. on page 8, Figure 6. on page 9, and Figure 7. on page 10 show quadrant views.

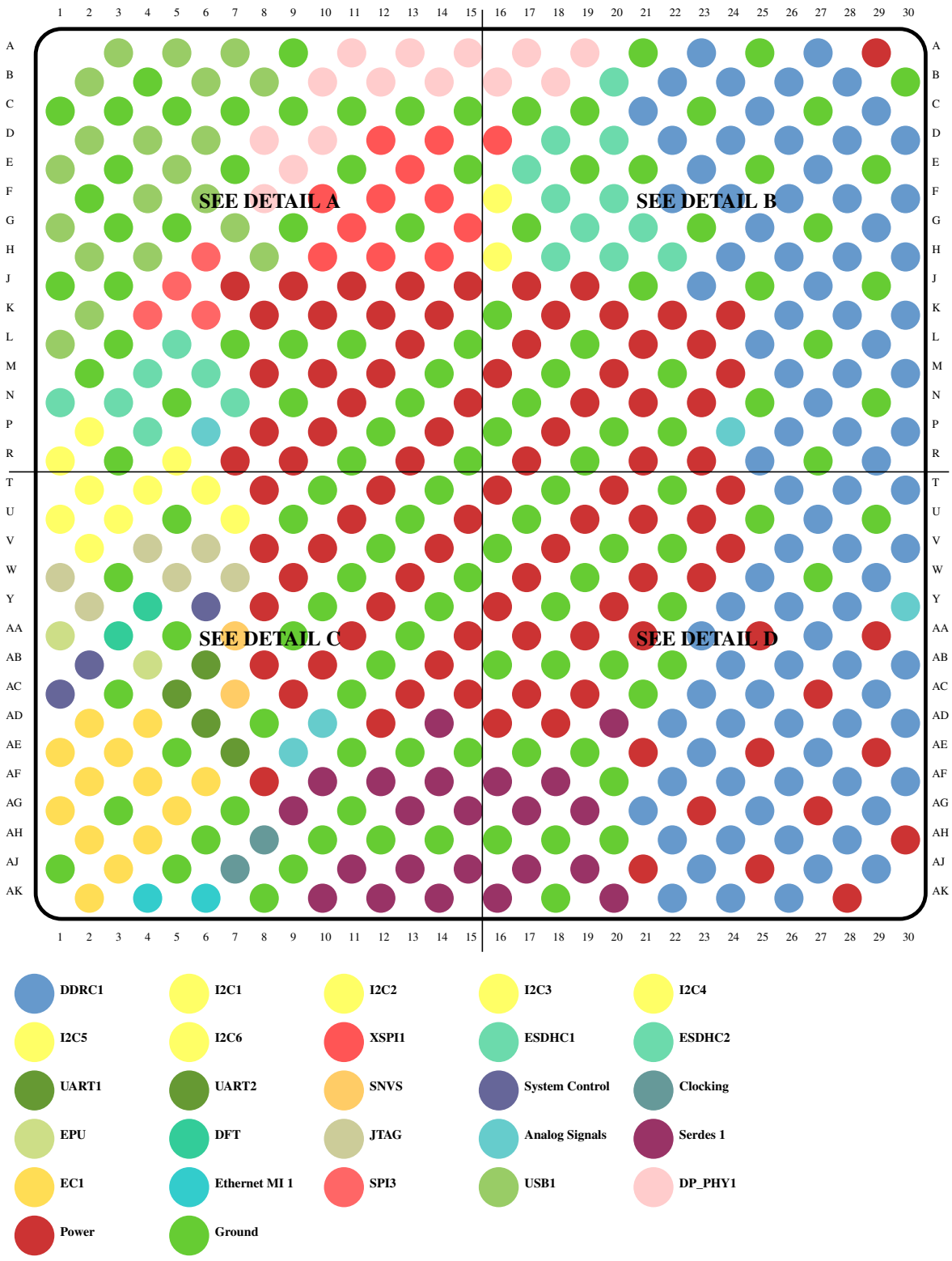


Figure 3. Complete BGA Map for the LS1028A

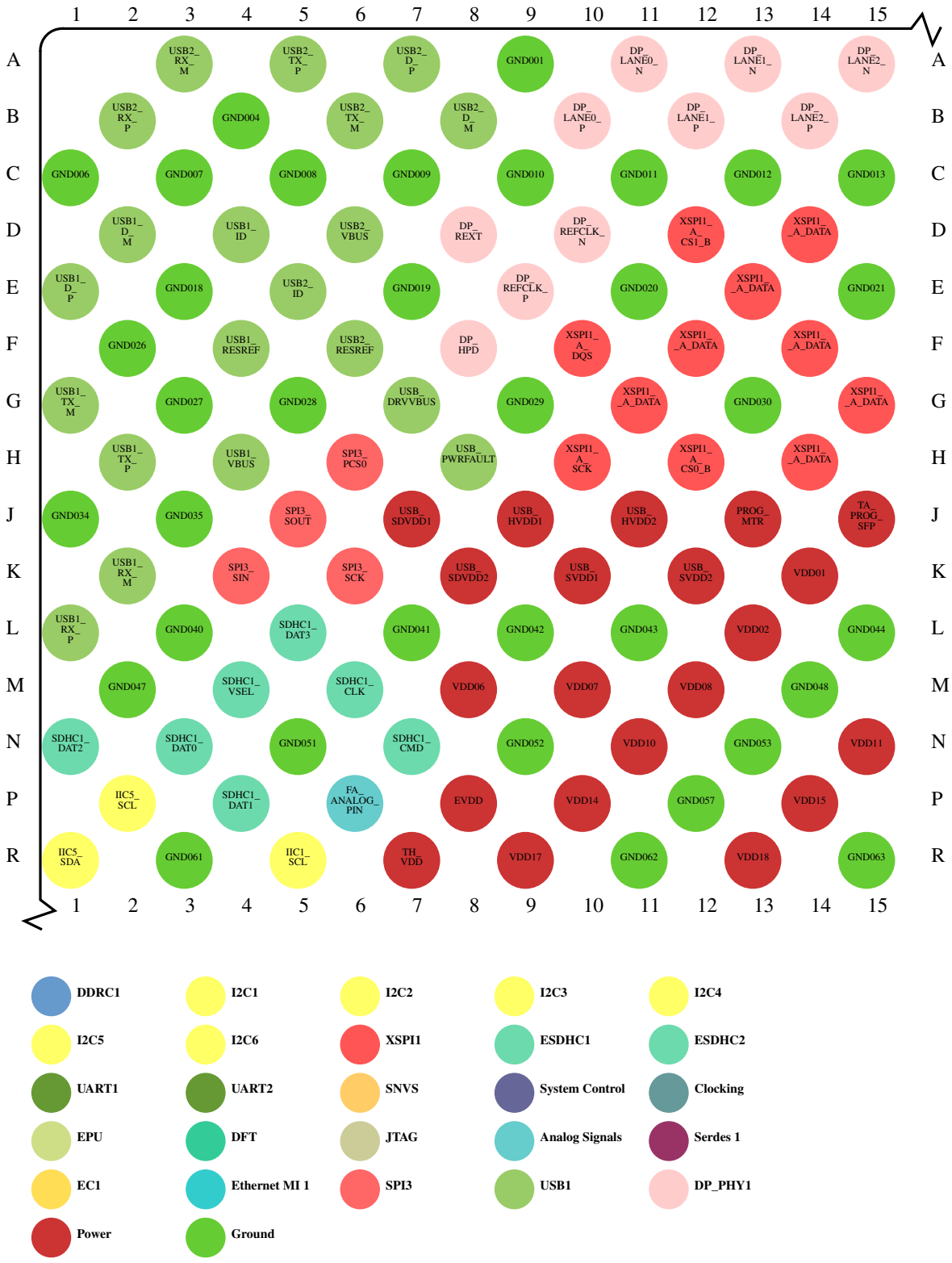


Figure 4. Detail A

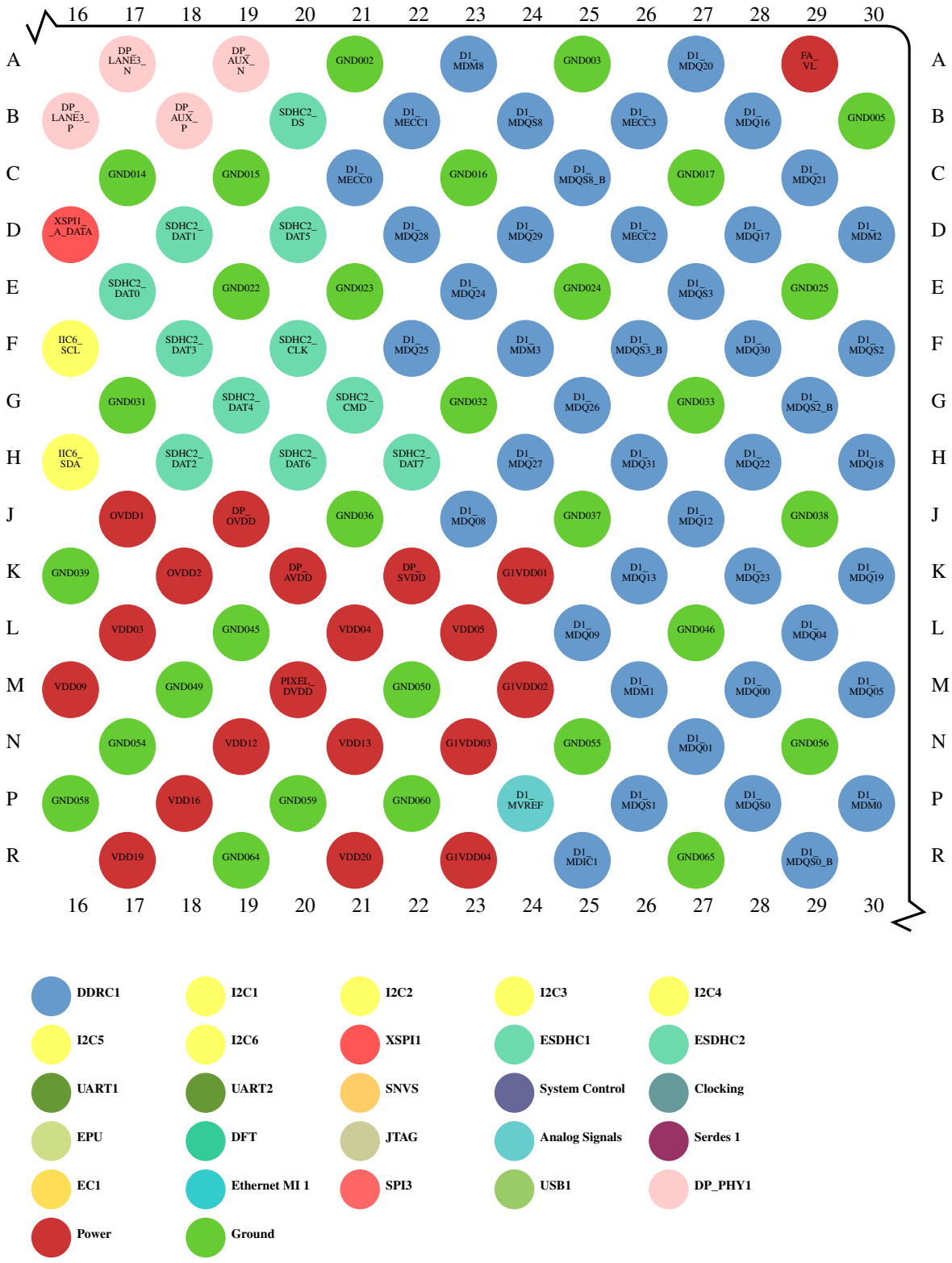


Figure 5. Detail B

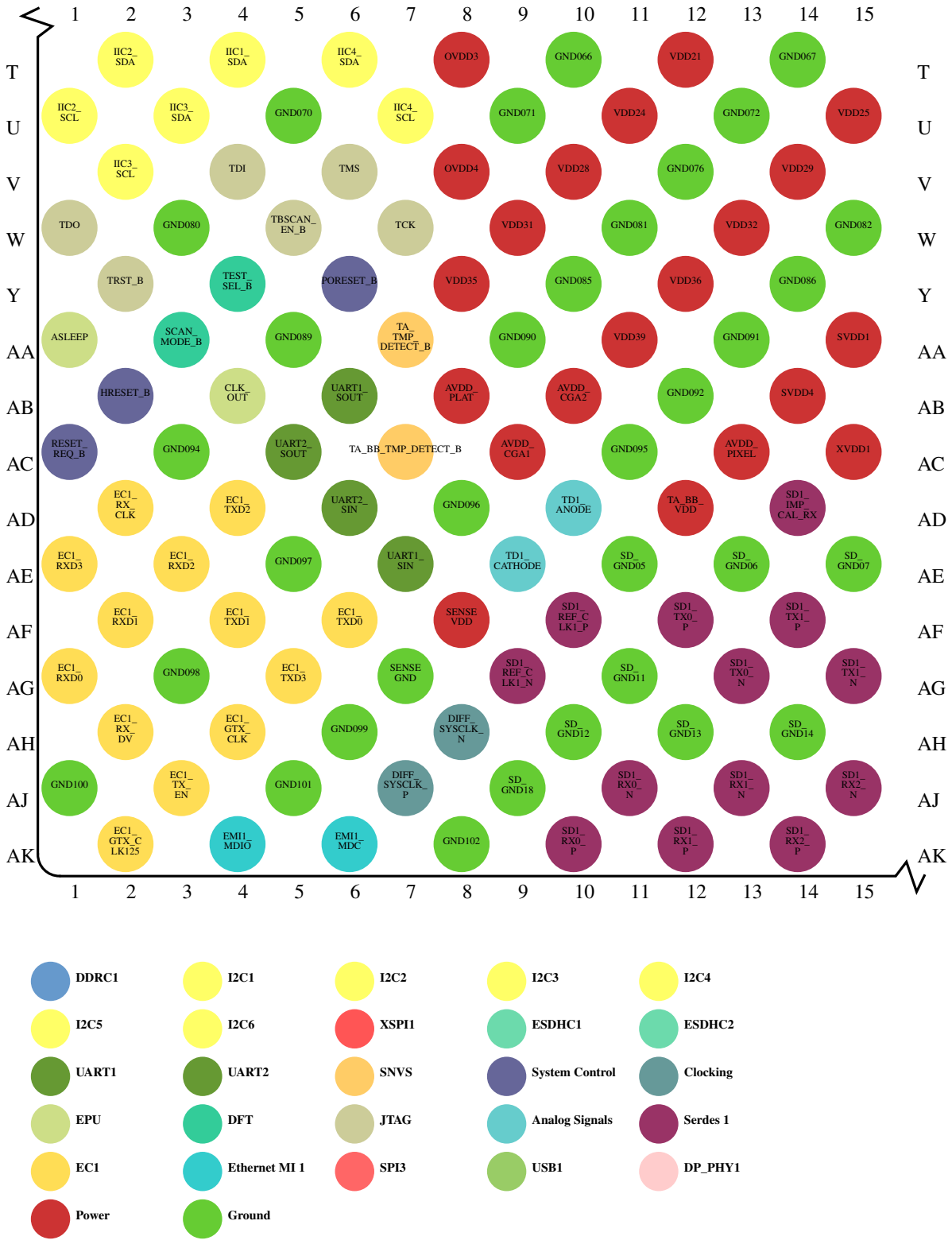


Figure 6. Detail C

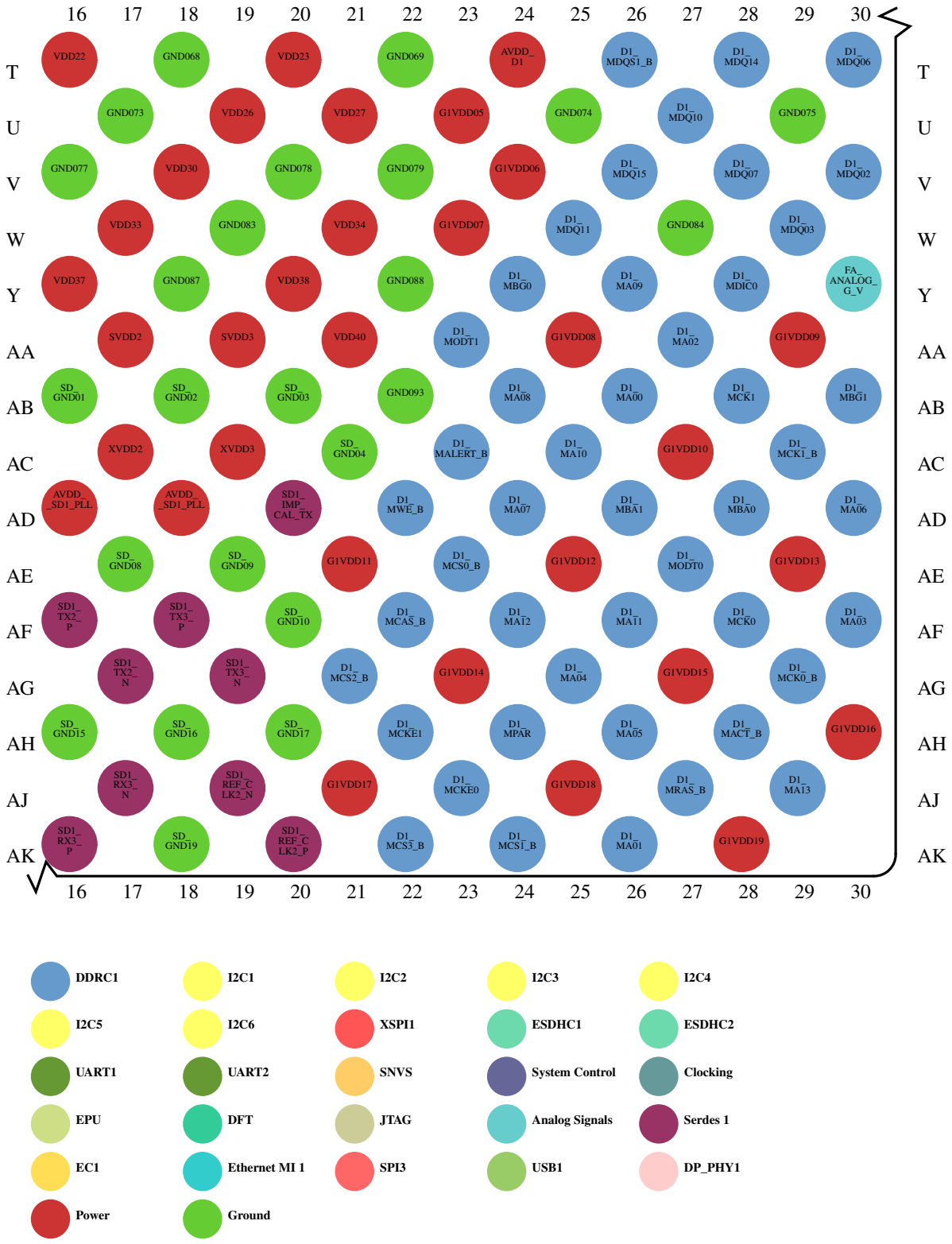


Figure 7. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS1028A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	AB26	O	$G1V_{DD}$	---
D1_MA01	Address	AK26	O	$G1V_{DD}$	---
D1_MA02	Address	AA27	O	$G1V_{DD}$	---
D1_MA03	Address	AF30	O	$G1V_{DD}$	---
D1_MA04	Address	AG25	O	$G1V_{DD}$	---
D1_MA05	Address	AH26	O	$G1V_{DD}$	---
D1_MA06	Address	AD30	O	$G1V_{DD}$	---
D1_MA07	Address	AD24	O	$G1V_{DD}$	---
D1_MA08	Address	AB24	O	$G1V_{DD}$	---
D1_MA09	Address	Y26	O	$G1V_{DD}$	---
D1_MA10	Address	AC25	O	$G1V_{DD}$	---
D1_MA11	Address	AF26	O	$G1V_{DD}$	---
D1_MA12	Address	AF24	O	$G1V_{DD}$	---
D1_MA13	Address	AJ29	O	$G1V_{DD}$	---
D1_MACT_B	Activate	AH28	O	$G1V_{DD}$	---
D1_MALERT_B	Alert	AC23	I	$G1V_{DD}$	1, 6
D1_MBA0	Bank Select	AD28	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	AD26	O	$G1V_{DD}$	---
D1_MBG0	Bank Group	Y24	O	$G1V_{DD}$	---
D1_MBG1	Bank Group	AB30	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	AF22	O	$G1V_{DD}$	---
D1_MCK0	Clock	AF28	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	AG29	O	$G1V_{DD}$	---
D1_MCK1	Clock	AB28	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	AC29	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	AJ23	O	$G1V_{DD}$	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MCKE1	Clock Enable	AH22	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	AE23	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	AK24	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select / MCID[0]	AG21	O	$G1V_{DD}$	---
D1_MCS3_B	Chip Select / MCID[1]	AK22	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedence Calibration	Y28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	R25	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	P30	O	$G1V_{DD}$	---
D1_MDM1	Data Mask	M26	O	$G1V_{DD}$	---
D1_MDM2	Data Mask	D30	O	$G1V_{DD}$	---
D1_MDM3	Data Mask	F24	O	$G1V_{DD}$	---
D1_MDM8	Data Mask	A23	O	$G1V_{DD}$	---
D1_MDQ00	Data	M28	IO	$G1V_{DD}$	---
D1_MDQ01	Data	N27	IO	$G1V_{DD}$	---
D1_MDQ02	Data	V30	IO	$G1V_{DD}$	---
D1_MDQ03	Data	W29	IO	$G1V_{DD}$	---
D1_MDQ04	Data	L29	IO	$G1V_{DD}$	---
D1_MDQ05	Data	M30	IO	$G1V_{DD}$	---
D1_MDQ06	Data	T30	IO	$G1V_{DD}$	---
D1_MDQ07	Data	V28	IO	$G1V_{DD}$	---
D1_MDQ08	Data	J23	IO	$G1V_{DD}$	---
D1_MDQ09	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ10	Data	U27	IO	$G1V_{DD}$	---
D1_MDQ11	Data	W25	IO	$G1V_{DD}$	---
D1_MDQ12	Data	J27	IO	$G1V_{DD}$	---
D1_MDQ13	Data	K26	IO	$G1V_{DD}$	---
D1_MDQ14	Data	T28	IO	$G1V_{DD}$	---
D1_MDQ15	Data	V26	IO	$G1V_{DD}$	---
D1_MDQ16	Data	B28	IO	$G1V_{DD}$	---
D1_MDQ17	Data	D28	IO	$G1V_{DD}$	---
D1_MDQ18	Data	H30	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MDQ19	Data	K30	IO	$G1V_{DD}$	---
D1_MDQ20	Data	A27	IO	$G1V_{DD}$	---
D1_MDQ21	Data	C29	IO	$G1V_{DD}$	---
D1_MDQ22	Data	H28	IO	$G1V_{DD}$	---
D1_MDQ23	Data	K28	IO	$G1V_{DD}$	---
D1_MDQ24	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ25	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ26	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ27	Data	H24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	D24	IO	$G1V_{DD}$	---
D1_MDQ30	Data	F28	IO	$G1V_{DD}$	---
D1_MDQ31	Data	H26	IO	$G1V_{DD}$	---
D1_MDQS0	Data Strobe	P28	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	R29	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	T26	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F30	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	G29	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	E27	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	B24	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	C25	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	C21	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	B22	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	D26	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	B26	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AE27	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination / MCID[2]	AA23	O	$G1V_{DD}$	2
D1_MPAR	Address Parity Out	AH24	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	AJ27	O	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
D1_MWE_B	Write Enable / MA[14]	AD22	O	G1V $_{DD}$	---
I2C1					
IIC1_SCL /GPIO1_DAT03	Serial Clock	R5	IO	OV $_{DD}$	7, 8
IIC1_SDA /GPIO1_DAT02	Serial Data	T4	IO	OV $_{DD}$	7, 8
I2C2					
IIC2_SCL /GPIO1_DAT31 / FTM1_CH0 /SDHC1_CD_B	Serial Clock	U1	IO	OV $_{DD}$	7, 8
IIC2_SDA /GPIO1_DAT30 / FTM2_CH0 /SDHC1_WP	Serial Data	T2	IO	OV $_{DD}$	7, 8
I2C3					
IIC3_SCL /GPIO1_DAT29 / CAN1_TX /LPUART1_SOUT / FTM7_CH0 /EVT5_B	Serial Clock	V2	IO	OV $_{DD}$	7, 8
IIC3_SDA /GPIO1_DAT28 / CAN1_RX /LPUART1_SIN / FTM7_EXTCLK /EVT6_B	Serial Data	U3	IO	OV $_{DD}$	7, 8
I2C4					
IIC4_SCL /GPIO1_DAT27 / CAN2_TX / LPUART1_CTS_B / FTM7_CH2 /EVT7_B	Serial Clock	U7	IO	OV $_{DD}$	7, 8
IIC4_SDA /GPIO1_DAT26 / CAN2_RX / LPUART1_RTS_B / FTM7_CH1 /EVT8_B	Serial Data	T6	IO	OV $_{DD}$	7, 8
I2C5					
IIC5_SCL /GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT / EVT1_B	Serial Clock	P2	IO	OV $_{DD}$	7, 8
IIC5_SDA /GPIO1_DAT24 / SDHC1_CLK_SYNC_IN / EVT2_B	Serial Data	R1	IO	OV $_{DD}$	7, 8
I2C6					
IIC6_SCL /GPIO1_DAT23 / SDHC2_CLK_SYNC_OUT / USB2_PWRFAULT /EVT3_B	Serial Clock	F16	IO	OV $_{DD}$	7, 8

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
IIC6_SDA /GPIO1_DAT22 / SDHC2_CLK_SYNC_IN / USB2_DRVVBUS /EVT0_B	Serial Data	H16	IO	OV_{DD}	7, 8
I2C7					
IIC7_SCL/ **SDHC2_DAT5** / GPIO2_DAT16 / LPUART4_CTS_B / FTM4_CH2 /XSPI1_B_DATA5	Serial Clock	D20	IO	OV_{DD}	7, 8
IIC7_SDA/ **SDHC2_DAT4** / GPIO2_DAT15 / LPUART4_RTS_B / FTM4_CH1 /XSPI1_B_DATA4	Serial Data	G19	IO	OV_{DD}	7, 8
I2C8					
IIC8_SCL/ **SDHC2_DAT7** / GPIO2_DAT18 / LPUART4_SOUT / FTM4_CH0 /XSPI1_B_DATA7	Serial Clock	H22	IO	OV_{DD}	7, 8
IIC8_SDA/ **SDHC2_DAT6** / GPIO2_DAT17 / LPUART4_SIN / FTM4_EXTCLK / XSPI1_B_DATA6	Serial Data	H20	IO	OV_{DD}	7, 8
XSPI1					
XSPI1_A_CS0_B / GPIO2_DAT21 /FTM8_CH1 / cfg_svr0	Chip Select	H12	O	OV_{DD}	1, 4
XSPI1_A_CS1_B / GPIO2_DAT20 /FTM8_CH0 / cfg_svr1	Chip Select	D12	O	OV_{DD}	1, 5
XSPI1_A_DATA0 / GPIO2_DAT24 / LPUART3_RTS_B / FTM3_CH1	Data	G11	IO	OV_{DD}	---
XSPI1_A_DATA1 / GPIO2_DAT25 / LPUART3_CTS_B / FTM3_CH2	Data	F12	IO	OV_{DD}	---
XSPI1_A_DATA2 / GPIO2_DAT26 / LPUART3_SIN / FTM3_EXTCLK	Data	H14	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_A_DATA3 / GPIO2_DAT27 / LPUART3_SOUT /FTM3_CH0	Data	E13	IO	OV_{DD}	---
XSPI1_A_DATA4 / GPIO2_DAT28 / LPUART2_RTS_B / FTM2_CH1	Data	F14	IO	OV_{DD}	---
XSPI1_A_DATA5 / GPIO2_DAT29 / LPUART2_CTS_B / FTM2_CH2	Data	D14	IO	OV_{DD}	---
XSPI1_A_DATA6 / GPIO2_DAT30 / LPUART2_SIN / FTM2_EXTCLK	Data	D16	IO	OV_{DD}	---
XSPI1_A_DATA7 / GPIO2_DAT31 / LPUART2_SOUT	Data	G15	IO	OV_{DD}	---
XSPI1_A_DQS / GPIO2_DAT23 / FTM8_EXTCLK	Data Strobe	F10	IO	OV_{DD}	---
XSPI1_A_SCK / GPIO2_DAT22 /FTM8_CH2 / cfg_eng_use0	Clock	H10	O	OV_{DD}	1, 5
XSPI1_B_CS1_B/ **SDHC2_CMD** / GPIO2_DAT19 /SPI2_SOUT	Chip Select	G21	O	OV_{DD}	1
XSPI1_B_DATA0/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / LPUART5_RTS_B / FTM5_CH1 /cfg_gpinput4	Data	E17	IO	OV_{DD}	4
XSPI1_B_DATA1/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / LPUART5_CTS_B / FTM5_CH2 /cfg_gpinput5	Data	D18	IO	OV_{DD}	4
XSPI1_B_DATA2/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / LPUART5_SIN / FTM5_EXTCLK /cfg_gpinput6	Data	H18	IO	OV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
XSPI1_B_DATA3/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / LPUART5_SOUT / FTM5_CH0 /cfg_gpinput7	Data	F18	IO	OV_{DD}	4
XSPI1_B_DATA4/ **SDHC2_DAT4** / GPIO2_DAT15 /IIC7_SDA / LPUART4_RTS_B / FTM4_CH1	Data	G19	IO	OV_{DD}	---
XSPI1_B_DATA5/ **SDHC2_DAT5** / GPIO2_DAT16 /IIC7_SCL / LPUART4_CTS_B / FTM4_CH2	Data	D20	IO	OV_{DD}	---
XSPI1_B_DATA6/ **SDHC2_DAT6** / GPIO2_DAT17 /IIC8_SDA / LPUART4_SIN / FTM4_EXTCLK	Data	H20	IO	OV_{DD}	---
XSPI1_B_DATA7/ **SDHC2_DAT7** / GPIO2_DAT18 /IIC8_SCL / LPUART4_SOUT /FTM4_CH0	Data	H22	IO	OV_{DD}	---
XSPI1_B_DQS/ **SDHC2_DS** / GPIO2_DAT10 /SPI2_PCS3	Data Strobe	B20	IO	OV_{DD}	---
XSPI1_B_SCK/ **SDHC2_CLK** / GPIO2_DAT09 /SPI2_SCK	Clock	F20	O	OV_{DD}	1
eSDHC 1					
SDHC1_CD_B/ **IIC2_SCL** / GPIO1_DAT31 /FTM1_CH0	Card Detect	U1	I	OV_{DD}	1
SDHC1_CLK / GPIO1_DAT16 /SPI1_SCK / SAI2_TX_SYNC / SAI2_RX_SYNC	Host to Card Clock	M6	O	EV_{DD}	1
SDHC1_CLK_SYNC_IN/ **IIC5_SDA** /GPIO1_DAT24 / EVT2_B	Input Synchronous Clock	R1	I	OV_{DD}	1
SDHC1_CLK_SYNC_OUT/ **IIC5_SCL** /GPIO1_DAT25 / EVT1_B	Output Synchronuous Clock	P2	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC1_CMD / GPIO1_DAT21 /SPI1_SOUT / SAI1_TX_BCLK / SAI1_RX_BCLK	Command/Response	N7	IO	EV_{DD}	26
SDHC1_DAT0 / GPIO1_DAT17 /SPI1_SIN / SAI2_TX_DATA / SAI2_RX_DATA /cfg_gpinput0	Data	N3	IO	EV_{DD}	4, 26
SDHC1_DAT1 / GPIO1_DAT18 /SPI1_PCS2 / SAI2_TX_BCLK / SAI2_RX_BCLK /cfg_gpinput1	Data	P4	IO	EV_{DD}	4, 26
SDHC1_DAT2 / GPIO1_DAT19 /SPI1_PCS1 / SAI1_TX_SYNC / SAI1_RX_SYNC / cfg_gpinput2	Data	N1	IO	EV_{DD}	4, 26
SDHC1_DAT3 / GPIO1_DAT20 /SPI1_PCS0 / SAI1_TX_DATA / SAI1_RX_DATA /cfg_gpinput3	Data	L5	IO	EV_{DD}	4, 26
SDHC1_VSEL / GPIO1_DAT15 /SPI1_PCS3	SDHC Voltage Select	M4	O	OV_{DD}	1
SDHC1_WP/ **IIC2_SDA** / GPIO1_DAT30 /FTM2_CH0	Write Protect	T2	I	OV_{DD}	1
eSDHC 2					
SDHC2_CLK / GPIO2_DAT09 /SPI2_SCK / XSPI1_B_SCK	Host to Card Clock	F20	O	OV_{DD}	1
SDHC2_CLK_SYNC_IN/ **IIC6_SDA** /GPIO1_DAT22 / USB2_DRVVBUS /EVT0_B	Input Synchronous Clock	H16	I	OV_{DD}	1
SDHC2_CLK_SYNC_OUT/ **IIC6_SCL** /GPIO1_DAT23 / USB2_PWRFAULT /EVT3_B	Output Synchronuous Clock	F16	O	OV_{DD}	1
SDHC2_CMD / GPIO2_DAT19 /SPI2_SOUT / XSPI1_B_CS1_B	Command/Response	G21	IO	OV_{DD}	26

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SDHC2_DAT0 / GPIO2_DAT11 /SPI2_SIN / LPUART5_RTS_B / FTM5_CH1 / XSPI1_B_DATA0 / cfg_gpinput4	Data	E17	IO	OV_{DD}	4, 26
SDHC2_DAT1 / GPIO2_DAT12 /SPI2_PCS2 / LPUART5_CTS_B / FTM5_CH2 / XSPI1_B_DATA1 / cfg_gpinput5	Data	D18	IO	OV_{DD}	4, 26
SDHC2_DAT2 / GPIO2_DAT13 /SPI2_PCS1 / LPUART5_SIN / FTM5_EXTCLK / XSPI1_B_DATA2 / cfg_gpinput6	Data	H18	IO	OV_{DD}	4, 26
SDHC2_DAT3 / GPIO2_DAT14 /SPI2_PCS0 / LPUART5_SOUT / FTM5_CH0 / XSPI1_B_DATA3 / cfg_gpinput7	Data	F18	IO	OV_{DD}	4, 26
SDHC2_DAT4 / GPIO2_DAT15 /IIC7_SDA / LPUART4_RTS_B / FTM4_CH1 /XSPI1_B_DATA4	Data	G19	IO	OV_{DD}	26
SDHC2_DAT5 / GPIO2_DAT16 /IIC7_SCL / LPUART4_CTS_B / FTM4_CH2 /XSPI1_B_DATA5	Data	D20	IO	OV_{DD}	26
SDHC2_DAT6 / GPIO2_DAT17 /IIC8_SDA / LPUART4_SIN / FTM4_EXTCLK / XSPI1_B_DATA6	Data	H20	IO	OV_{DD}	26
SDHC2_DAT7 / GPIO2_DAT18 /IIC8_SCL / LPUART4_SOUT / FTM4_CH0 /XSPI1_B_DATA7	Data	H22	IO	OV_{DD}	26
SDHC2_DS /GPIO2_DAT10 / SPI2_PCS3 /XSPI1_B_DQS	Data Strobe (eMMC HS400 mode)	B20	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DUART					
UART1_SIN /GPIO1_DAT10 / LPUART6_SIN / FTM6_EXTCLK	Receive Data	AE7	I	OV_{DD}	1
UART1_SOUT / GPIO1_DAT11 / LPUART6_SOUT / FTM6_CH0 /cfg_rcw_src1	Transmit Data	AB6	O	OV_{DD}	1, 4
DUART					
UART2_SIN /GPIO1_DAT06 / LPUART6_CTS_B / FTM6_CH2	Receive Data	AD6	I	OV_{DD}	1
UART2_SOUT / GPIO1_DAT07 / LPUART6_RTS_B / FTM6_CH1 /cfg_rcw_src0	Transmit Data	AC5	O	OV_{DD}	1, 4
Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	AC7	I	$TA_BB_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	AA7	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	AB2	IO	OV_{DD}	27, 7
PORESET_B	Power On Reset	Y6	I	OV_{DD}	21, 23
RESET_REQ_B / GPIO2_DAT08	Reset Request (POR or Hard)	AC1	O	OV_{DD}	5
Clocking					
DIFF_SYSCLK_N	Differential System Clock (negative)	AH8	I	-	---
DIFF_SYSCLK_P	Differential System Clock (positive)	AJ7	I	-	---
Debug					
ASLEEP /GPIO2_DAT06 / EVT9_B /cfg_rcw_src2	Asleep	AA1	O	OV_{DD}	4
CLK_OUT /GPIO2_DAT07 / FTM1_CH1 /EVT4_B / cfg_rcw_src3	Clock Out	AB4	O	OV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EVT0_B/ **IIC6_SDA** / GPIO1_DAT22 / SDHC2_CLK_SYNC_IN / USB2_DRVVBUS	Event 0	H16	O	OV_{DD}	1
EVT1_B/ **IIC5_SCL** / GPIO1_DAT25 / SDHC1_CLK_SYNC_OUT	Event 1	P2	O	OV_{DD}	1
EVT2_B/ **IIC5_SDA** / GPIO1_DAT24 / SDHC1_CLK_SYNC_IN	Event 2	R1	O	OV_{DD}	1
EVT3_B/ **IIC6_SCL** / GPIO1_DAT23 / SDHC2_CLK_SYNC_OUT / USB2_PWRFAULT	Event 3	F16	O	OV_{DD}	1
EVT4_B/ **CLK_OUT** / GPIO2_DAT07 /FTM1_CH1 / cfg_rcw_src3	Event 4	AB4	O	OV_{DD}	1, 4
EVT5_B/ **IIC3_SCL** / GPIO1_DAT29 /CAN1_TX / LPUART1_SOUT /FTM7_CH0	Event 5	V2	IO	OV_{DD}	---
EVT6_B/ **IIC3_SDA** / GPIO1_DAT28 /CAN1_RX / LPUART1_SIN / FTM7_EXTCLK	Event 6	U3	IO	OV_{DD}	---
EVT7_B/ **IIC4_SCL** / GPIO1_DAT27 /CAN2_TX / LPUART1_CTS_B / FTM7_CH2	Event 7	U7	IO	OV_{DD}	---
EVT8_B/ **IIC4_SDA** / GPIO1_DAT26 /CAN2_RX / LPUART1_RTS_B / FTM7_CH1	Event 8	T6	IO	OV_{DD}	---
EVT9_B/ **ASLEEP** / GPIO2_DAT06 /cfg_rcw_src2	Event 9	AA1	O	OV_{DD}	1, 4
DFT					
SCAN_MODE_B	Internal Use Only	AA3	I	OV_{DD}	10 21
TEST_SEL_B	Internal Use Only	Y4	I	OV_{DD}	21 22
JTAG					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
TBSCAN_EN_B	An IEEE 1149.1 JTAG Compliance Enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the Arm core debug.	W5	I	OV_{DD}	19, 21
TCK	Test Clock	W7	I	OV_{DD}	---
TDI	Test Data In	V4	I	OV_{DD}	9
TDO	Test Data Out	W1	O	OV_{DD}	2
TMS	Test Mode Select	V6	I	OV_{DD}	9
TRST_B	Test Reset	Y2	I	OV_{DD}	9
Analog Signals					
D1_MVREF	SSTL Reference Voltage	P24	IO	$G1V_{DD}/2$	---
FA_ANALOG_G_V	Internal Use Only	Y30	IO	-	15
FA_ANALOG_PIN	Internal Use Only	P6	IO	-	15
TD1_ANODE	Thermal diode anode	AD10	IO	-	17
TD1_CATHODE	Thermal diode cathode	AE9	IO	-	17
Serdes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AD14	-	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AD20	-	XV_{DD}	16
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AG9	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AF10	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AJ19	I	SV_{DD}	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AK20	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AJ11	I	SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AK10	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SD1_RX1_N	SerDes Receive Data (negative)	AJ13	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AK12	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AJ15	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AK14	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AJ17	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AK16	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AG13	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AF12	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AG15	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AF14	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AG17	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AF16	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AG19	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AF18	O	XV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK / GPIO3_DAT07 / SAI4_TX_SYNC / SAI4_RX_SYNC / FTM1_EXTCLK / SWITCH_1588_DAT0	Transmit Clock Out	AH4	O	OV_{DD}	1
EC1_GTX_CLK125 / GPIO3_DAT06 / EC1_1722_DAT0	125MHz Reference Clock	AK2	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EC1_RXD0 /GPIO3_DAT02 / SAI6_TX_BCLK / SAI6_RX_BCLK	Receive Data	AG1	I	OV_{DD}	1
EC1_RXD1 /GPIO3_DAT03 / SAI3_TX_BCLK / SAI3_RX_BCLK	Receive Data	AF2	I	OV_{DD}	1
EC1_RXD2 /GPIO3_DAT04 / SAI4_TX_BCLK / SAI4_RX_BCLK /FTM1_CH2	Receive Data	AE3	I	OV_{DD}	1
EC1_RXD3 /GPIO3_DAT05 / SAI5_TX_BCLK / SAI5_RX_BCLK /FTM1_CH3 / EC1_1722_DAT1	Receive Data	AE1	I	OV_{DD}	1
EC1_RX_CLK / GPIO3_DAT01 / SAI3_TX_SYNC / SAI3_RX_SYNC / FTM1_QD_PHA / EC1_1588_CLK_IN	Receive Clock	AD2	I	OV_{DD}	1
EC1_RX_DV / GPIO3_DAT00 / SAI6_TX_SYNC / SAI6_RX_SYNC / FTM1_QD_PHB / EC1_1588_TRIG_IN1	Receive Data Valid	AH2	I	OV_{DD}	1
EC1_TXD0 /GPIO3_DAT09 / SAI6_TX_DATA / SAI6_RX_DATA /FTM1_CH4 / EC1_1588_PULSE_OUT2	Transmit Data	AF6	O	OV_{DD}	1
EC1_TXD1 /GPIO3_DAT10 / SAI3_TX_DATA / SAI3_RX_DATA /FTM1_CH5 / EC1_1588_CLK_OUT	Transmit Data	AF4	O	OV_{DD}	1
EC1_TXD2 /GPIO3_DAT11 / SAI4_TX_DATA / SAI4_RX_DATA /FTM1_CH6 / EC1_1588_ALARM_OUT1	Transmit Data	AD4	O	OV_{DD}	1
EC1_TXD3 /GPIO3_DAT12 / SAI5_TX_DATA / SAI5_RX_DATA /FTM1_CH7 / EC1_1588_PULSE_OUT1	Transmit Data	AG5	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EC1_TX_EN /GPIO3_DAT08 / SAI5_TX_SYNC / SAI5_RX_SYNC / FTM1_FAULT / SWITCH_1588_DAT1	Transmit Enable	AJ3	O	OV_{DD}	1 14
Ethernet Management Interface 1					
EMI1_MDC /cfg_dram_type	Management Data Clock	AK6	O	OV_{DD}	4
EMI1_MDIO	Management Data In/Out	AK4	IO	OV_{DD}	---
General Purpose Input/Output					
GPIO1_DAT02/ **IIC1_SDA**	General Purpose Input/Output	T4	IO	OV_{DD}	---
GPIO1_DAT03/ **IIC1_SCL**	General Purpose Input/Output	R5	IO	OV_{DD}	---
GPIO1_DAT06/ **UART2_SIN** / LPUART6_CTS_B / FTM6_CH2	General Purpose Input/Output	AD6	IO	OV_{DD}	---
GPIO1_DAT07/ **UART2_SOUT** / LPUART6_RTS_B / FTM6_CH1 /cfg_rcw_src0	General Purpose Input/Output	AC5	O	OV_{DD}	1, 4
GPIO1_DAT10/ **UART1_SIN** / LPUART6_SIN / FTM6_EXTCLK	General Purpose Input/Output	AE7	IO	OV_{DD}	---
GPIO1_DAT11/ **UART1_SOUT** / LPUART6_SOUT / FTM6_CH0 /cfg_rcw_src1	General Purpose Input/Output	AB6	O	OV_{DD}	1, 4
GPIO1_DAT15/ **SDHC1_VSEL** /SPI1_PCS3	General Purpose Input/Output	M4	IO	OV_{DD}	---
GPIO1_DAT16/ **SDHC1_CLK** /SPI1_SCK / SAI2_TX_SYNC / SAI2_RX_SYNC	General Purpose Input/Output	M6	IO	EV_{DD}	---
GPIO1_DAT17/ **SDHC1_DAT0** /SPI1_SIN / SAI2_TX_DATA / SAI2_RX_DATA /cfg_gpinput0	General Purpose Input/Output	N3	IO	EV_{DD}	4
GPIO1_DAT18/ **SDHC1_DAT1** /SPI1_PCS2 / SAI2_TX_BCLK / SAI2_RX_BCLK /cfg_gpinput1	General Purpose Input/Output	P4	IO	EV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT19/ **SDHC1_DAT2** /SPI1_PCS1 / SAI1_TX_SYNC / SAI1_RX_SYNC / cfg_gpinput2	General Purpose Input/Output	N1	IO	EV_{DD}	4
GPIO1_DAT20/ **SDHC1_DAT3** /SPI1_PCS0 / SAI1_TX_DATA / SAI1_RX_DATA /cfg_gpinput3	General Purpose Input/Output	L5	IO	EV_{DD}	4
GPIO1_DAT21/ **SDHC1_CMD** /SPI1_SOUT / SAI1_TX_BCLK / SAI1_RX_BCLK	General Purpose Input/Output	N7	IO	EV_{DD}	---
GPIO1_DAT22/ **IIC6_SDA** / SDHC2_CLK_SYNC_IN / USB2_DRVVBUS /EVT0_B	General Purpose Input/Output	H16	IO	OV_{DD}	---
GPIO1_DAT23/ **IIC6_SCL** / SDHC2_CLK_SYNC_OUT / USB2_PWRFAULT /EVT3_B	General Purpose Input/Output	F16	IO	OV_{DD}	---
GPIO1_DAT24/ **IIC5_SDA** / SDHC1_CLK_SYNC_IN / EVT2_B	General Purpose Input/Output	R1	IO	OV_{DD}	---
GPIO1_DAT25/ **IIC5_SCL** / SDHC1_CLK_SYNC_OUT / EVT1_B	General Purpose Input/Output	P2	IO	OV_{DD}	---
GPIO1_DAT26/ **IIC4_SDA** / CAN2_RX / LPUART1_RTS_B / FTM7_CH1 /EVT8_B	General Purpose Input/Output	T6	IO	OV_{DD}	---
GPIO1_DAT27/ **IIC4_SCL** / CAN2_TX / LPUART1_CTS_B / FTM7_CH2 /EVT7_B	General Purpose Input/Output	U7	IO	OV_{DD}	---
GPIO1_DAT28/ **IIC3_SDA** / CAN1_RX /LPUART1_SIN / FTM7_EXTCLK /EVT6_B	General Purpose Input/Output	U3	IO	OV_{DD}	---
GPIO1_DAT29/ **IIC3_SCL** / CAN1_TX /LPUART1_SOUT / FTM7_CH0 /EVT5_B	General Purpose Input/Output	V2	IO	OV_{DD}	---
GPIO1_DAT30/ **IIC2_SDA** / FTM2_CH0 /SDHC1_WP	General Purpose Input/Output	T2	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO1_DAT31/ **IIC2_SCL** / FTM1_CH0 /SDHC1_CD_B	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO2_DAT06/ **ASLEEP** / EVT9_B /cfg_rcw_src2	General Purpose Input/Output	AA1	O	OV_{DD}	1, 4
GPIO2_DAT07/ **CLK_OUT** / FTM1_CH1 /EVT4_B / cfg_rcw_src3	General Purpose Input/Output	AB4	O	OV_{DD}	1, 4
GPIO2_DAT08/ **RESET_REQ_B**	General Purpose Input/Output	AC1	O	OV_{DD}	1, 5
GPIO2_DAT09/ **SDHC2_CLK** /SPI2_SCK / XSPI1_B_SCK	General Purpose Input/Output	F20	IO	OV_{DD}	---
GPIO2_DAT10/ **SDHC2_DS** / SPI2_PCS3 /XSPI1_B_DQS	General Purpose Input/Output	B20	IO	OV_{DD}	---
GPIO2_DAT11/ **SDHC2_DAT0** /SPI2_SIN / LPUART5_RTS_B / FTM5_CH1 / XSPI1_B_DATA0 / cfg_gpinput4	General Purpose Input/Output	E17	IO	OV_{DD}	4
GPIO2_DAT12/ **SDHC2_DAT1** /SPI2_PCS2 / LPUART5_CTS_B / FTM5_CH2 / XSPI1_B_DATA1 / cfg_gpinput5	General Purpose Input/Output	D18	IO	OV_{DD}	4
GPIO2_DAT13/ **SDHC2_DAT2** /SPI2_PCS1 / LPUART5_SIN / FTM5_EXTCLK / XSPI1_B_DATA2 / cfg_gpinput6	General Purpose Input/Output	H18	IO	OV_{DD}	4
GPIO2_DAT14/ **SDHC2_DAT3** /SPI2_PCS0 / LPUART5_SOUT / FTM5_CH0 / XSPI1_B_DATA3 / cfg_gpinput7	General Purpose Input/Output	F18	IO	OV_{DD}	4
GPIO2_DAT15/ **SDHC2_DAT4** /IIC7_SDA / LPUART4_RTS_B / FTM4_CH1 /XSPI1_B_DATA4	General Purpose Input/Output	G19	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO2_DAT16/ **SDHC2_DAT5** /IIC7_SCL / LPUART4_CTS_B / FTM4_CH2 /XSPI1_B_DATA5	General Purpose Input/Output	D20	IO	OV_{DD}	---
GPIO2_DAT17/ **SDHC2_DAT6** /IIC8_SDA / LPUART4_SIN / FTM4_EXTCLK / XSPI1_B_DATA6	General Purpose Input/Output	H20	IO	OV_{DD}	---
GPIO2_DAT18/ **SDHC2_DAT7** /IIC8_SCL / LPUART4_SOUT / FTM4_CH0 /XSPI1_B_DATA7	General Purpose Input/Output	H22	IO	OV_{DD}	---
GPIO2_DAT19/ **SDHC2_CMD** /SPI2_SOUT / XSPI1_B_CS1_B	General Purpose Input/Output	G21	IO	OV_{DD}	---
GPIO2_DAT20/ **XSPI1_A_CS1_B** / FTM8_CH0 /cfg_svr1	General Purpose Input/Output	D12	O	OV_{DD}	1, 5
GPIO2_DAT21/ **XSPI1_A_CS0_B** / FTM8_CH1 /cfg_svr0	General Purpose Input/Output	H12	O	OV_{DD}	1, 4
GPIO2_DAT22/ **XSPI1_A_SCK** /FTM8_CH2 / cfg_eng_use0	General Purpose Input/Output	H10	O	OV_{DD}	1, 5
GPIO2_DAT23/ **XSPI1_A_DQS** / FTM8_EXTCLK	General Purpose Input/Output	F10	IO	OV_{DD}	---
GPIO2_DAT24/ **XSPI1_A_DATA0** / LPUART3_RTS_B / FTM3_CH1	General Purpose Input/Output	G11	IO	OV_{DD}	---
GPIO2_DAT25/ **XSPI1_A_DATA1** / LPUART3_CTS_B / FTM3_CH2	General Purpose Input/Output	F12	IO	OV_{DD}	---
GPIO2_DAT26/ **XSPI1_A_DATA2** / LPUART3_SIN / FTM3_EXTCLK	General Purpose Input/Output	H14	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO2_DAT27/ **XSPI1_A_DATA3** / LPUART3_SOUT /FTM3_CH0	General Purpose Input/Output	E13	IO	OV_{DD}	---
GPIO2_DAT28/ **XSPI1_A_DATA4** / LPUART2_RTS_B / FTM2_CH1	General Purpose Input/Output	F14	IO	OV_{DD}	---
GPIO2_DAT29/ **XSPI1_A_DATA5** / LPUART2_CTS_B / FTM2_CH2	General Purpose Input/Output	D14	IO	OV_{DD}	---
GPIO2_DAT30/ **XSPI1_A_DATA6** / LPUART2_SIN / FTM2_EXTCLK	General Purpose Input/Output	D16	IO	OV_{DD}	---
GPIO2_DAT31/ **XSPI1_A_DATA7** / LPUART2_SOUT	General Purpose Input/Output	G15	IO	OV_{DD}	---
GPIO3_DAT00/ **EC1_RX_DV** / SAI6_TX_SYNC / SAI6_RX_SYNC / FTM1_QD_PHB / EC1_1588_TRIG_IN1	General Purpose Input/Output	AH2	IO	OV_{DD}	---
GPIO3_DAT01/ **EC1_RX_CLK** / SAI3_TX_SYNC / SAI3_RX_SYNC / FTM1_QD_PHA / EC1_1588_CLK_IN	General Purpose Input/Output	AD2	IO	OV_{DD}	---
GPIO3_DAT02/ **EC1_RXD0** / SAI6_TX_BCLK / SAI6_RX_BCLK	General Purpose Input/Output	AG1	IO	OV_{DD}	---
GPIO3_DAT03/ **EC1_RXD1** / SAI3_TX_BCLK / SAI3_RX_BCLK	General Purpose Input/Output	AF2	IO	OV_{DD}	---
GPIO3_DAT04/ **EC1_RXD2** / SAI4_TX_BCLK / SAI4_RX_BCLK /FTM1_CH2	General Purpose Input/Output	AE3	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO3_DAT05/ **EC1_RXD3** / SAI5_TX_BCLK / SAI5_RX_BCLK /FTM1_CH3 / EC1_1722_DAT1	General Purpose Input/Output	AE1	IO	OV_{DD}	---
GPIO3_DAT06/ **EC1_GTX_CLK125** / EC1_1722_DAT0	General Purpose Input/Output	AK2	IO	OV_{DD}	---
GPIO3_DAT07/ **EC1_GTX_CLK** / SAI4_TX_SYNC / SAI4_RX_SYNC / FTM1_EXTCLK / SWITCH_1588_DAT0	General Purpose Input/Output	AH4	IO	OV_{DD}	---
GPIO3_DAT08/ **EC1_TX_EN** / SAI5_TX_SYNC / SAI5_RX_SYNC / FTM1_FAULT / SWITCH_1588_DAT1	General Purpose Input/Output	AJ3	IO	OV_{DD}	---
GPIO3_DAT09/ **EC1_TXD0** / SAI6_TX_DATA / SAI6_RX_DATA /FTM1_CH4 / EC1_1588_PULSE_OUT2	General Purpose Input/Output	AF6	IO	OV_{DD}	---
GPIO3_DAT10/ **EC1_TXD1** / SAI3_TX_DATA / SAI3_RX_DATA /FTM1_CH5 / EC1_1588_CLK_OUT	General Purpose Input/Output	AF4	IO	OV_{DD}	---
GPIO3_DAT11/ **EC1_TXD2** / SAI4_TX_DATA / SAI4_RX_DATA /FTM1_CH6 / EC1_1588_ALARM_OUT1	General Purpose Input/Output	AD4	IO	OV_{DD}	---
GPIO3_DAT12/ **EC1_TXD3** / SAI5_TX_DATA / SAI5_RX_DATA /FTM1_CH7 / EC1_1588_PULSE_OUT1	General Purpose Input/Output	AG5	IO	OV_{DD}	---
GPIO3_DAT13/ **SPI3_SIN** / EC1_1722_DAT2	General Purpose Input/Output	K4	IO	OV_{DD}	---
GPIO3_DAT14/ **SPI3_SCK** / EC1_1722_DAT3	General Purpose Input/Output	K6	IO	OV_{DD}	---
GPIO3_DAT15/ **SPI3_PCS0** / EC1_1588_TRIG_IN2 / SWITCH_1588_DAT2	General Purpose Input/Output	H6	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GPIO3_DAT16/ **SPI3_SOUT** / EC1_1588_ALARM_OUT2 / SWITCH_1588_DAT3	General Purpose Input/Output	J5	IO	OV_{DD}	---
GPIO3_DAT17/ **USB_PWRFAULT** / SPI3_PCS1	General Purpose Input/Output	H8	IO	OV_{DD}	---
GPIO3_DAT18/ **USB_DRVVBUS** /SPI3_PCS2	General Purpose Input/Output	G7	IO	OV_{DD}	---
Flex Timer Module					
FTM1_CH0/ **IIC2_SCL** / GPIO1_DAT31 / SDHC1_CD_B	Channel 0	U1	IO	OV_{DD}	---
FTM1_CH1/ **CLK_OUT** / GPIO2_DAT07 /EVT4_B / cfg_rcw_src3	Channel 1	AB4	O	OV_{DD}	1, 4
FTM1_CH2/ **EC1_RXD2** / GPIO3_DAT04 / SAI4_TX_BCLK / SAI4_RX_BCLK	Channel 2	AE3	IO	OV_{DD}	---
FTM1_CH3/ **EC1_RXD3** / GPIO3_DAT05 / SAI5_TX_BCLK / SAI5_RX_BCLK / EC1_1722_DAT1	Channel 3	AE1	IO	OV_{DD}	---
FTM1_CH4/ **EC1_TXD0** / GPIO3_DAT09 / SAI6_TX_DATA / SAI6_RX_DATA / EC1_1588_PULSE_OUT2	Channel 4	AF6	IO	OV_{DD}	---
FTM1_CH5/ **EC1_TXD1** / GPIO3_DAT10 / SAI3_TX_DATA / SAI3_RX_DATA / EC1_1588_CLK_OUT	Channel 5	AF4	IO	OV_{DD}	---
FTM1_CH6/ **EC1_TXD2** / GPIO3_DAT11 / SAI4_TX_DATA / SAI4_RX_DATA / EC1_1588_ALARM_OUT1	Channel 6	AD4	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
FTM1_CH7/ **EC1_TXD3** / GPIO3_DAT12 / SAI5_TX_DATA / SAI5_RX_DATA / EC1_1588_PULSE_OUT1	Channel 7	AG5	IO	OV_{DD}	---
FTM1_EXTCLK/ **EC1_GTX_CLK** / GPIO3_DAT07 / SAI4_TX_SYNC / SAI4_RX_SYNC / SWITCH_1588_DAT0	External Clock	AH4	I	OV_{DD}	1
FTM1_FAULT/ **EC1_TX_EN** / GPIO3_DAT08 / SAI5_TX_SYNC / SAI5_RX_SYNC / SWITCH_1588_DAT1	Fault	AJ3	I	OV_{DD}	1
FTM1_QD_PHA/ **EC1_RX_CLK** / GPIO3_DAT01 / SAI3_TX_SYNC / SAI3_RX_SYNC / EC1_1588_CLK_IN	Phase A	AD2	I	OV_{DD}	1
FTM1_QD_PHB/ **EC1_RX_DV** / GPIO3_DAT00 / SAI6_TX_SYNC / SAI6_RX_SYNC / EC1_1588_TRIG_IN1	Phase B	AH2	I	OV_{DD}	1
FTM2_CH0/ **IIC2_SDA** / GPIO1_DAT30 /SDHC1_WP	Channel 0	T2	IO	OV_{DD}	---
FTM2_CH1/ **XSPI1_A_DATA4** / GPIO2_DAT28 / LPUART2_RTS_B	Channel 1	F14	IO	OV_{DD}	---
FTM2_CH2/ **XSPI1_A_DATA5** / GPIO2_DAT29 / LPUART2_CTS_B	Channel 2	D14	IO	OV_{DD}	---
FTM2_EXTCLK/ **XSPI1_A_DATA6** / GPIO2_DAT30 / LPUART2_SIN	External Clock	D16	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
FTM3_CH0/ **XSPI1_A_DATA3** / GPIO2_DAT27 / LPUART3_SOUT	Channel 0	E13	IO	OV_{DD}	---
FTM3_CH1/ **XSPI1_A_DATA0** / GPIO2_DAT24 / LPUART3_RTS_B	Channel 1	G11	IO	OV_{DD}	---
FTM3_CH2/ **XSPI1_A_DATA1** / GPIO2_DAT25 / LPUART3_CTS_B	Channel 2	F12	IO	OV_{DD}	---
FTM3_EXTCLK/ **XSPI1_A_DATA2** / GPIO2_DAT26 / LPUART3_SIN	External Clock	H14	I	OV_{DD}	1
FTM4_CH0/ **SDHC2_DAT7** / GPIO2_DAT18 /IIC8_SCL / LPUART4_SOUT / XSPI1_B_DATA7	Channel 0	H22	IO	OV_{DD}	---
FTM4_CH1/ **SDHC2_DAT4** / GPIO2_DAT15 /IIC7_SDA / LPUART4_RTS_B / XSPI1_B_DATA4	Channel 1	G19	IO	OV_{DD}	---
FTM4_CH2/ **SDHC2_DAT5** / GPIO2_DAT16 /IIC7_SCL / LPUART4_CTS_B / XSPI1_B_DATA5	Channel 2	D20	IO	OV_{DD}	---
FTM4_EXTCLK/ **SDHC2_DAT6** / GPIO2_DAT17 /IIC8_SDA / LPUART4_SIN / XSPI1_B_DATA6	External Clock	H20	I	OV_{DD}	1
FTM5_CH0/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / LPUART5_SOUT / XSPI1_B_DATA3 / cfg_gpinput7	Channel 0	F18	IO	OV_{DD}	4
FTM5_CH1/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / LPUART5_RTS_B / XSPI1_B_DATA0 / cfg_gpinput4	Channel 1	E17	IO	OV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
FTM5_CH2/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / LPUART5_CTS_B / XSPI1_B_DATA1 / cfg_gpinput5	Channel 2	D18	I	OV_{DD}	1, 4
FTM5_EXTCLK/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / LPUART5_SIN / XSPI1_B_DATA2 / cfg_gpinput6	External Clock	H18	I	OV_{DD}	1, 4
FTM6_CH0/ **UART1_SOUT** / GPIO1_DAT11 / LPUART6_SOUT / cfg_rcw_src1	Channel 0	AB6	O	OV_{DD}	1, 4
FTM6_CH1/ **UART2_SOUT** / GPIO1_DAT07 / LPUART6_RTS_B / cfg_rcw_src0	Channel 1	AC5	O	OV_{DD}	1, 4
FTM6_CH2/ **UART2_SIN** / GPIO1_DAT06 / LPUART6_CTS_B	Channel 2	AD6	IO	OV_{DD}	---
FTM6_EXTCLK/ **UART1_SIN** /GPIO1_DAT10 / LPUART6_SIN	External Clock	AE7	I	OV_{DD}	1
FTM7_CH0/ **IIC3_SCL** / GPIO1_DAT29 /CAN1_TX / LPUART1_SOUT /EVT5_B	Channel 0	V2	IO	OV_{DD}	---
FTM7_CH1/ **IIC4_SDA** / GPIO1_DAT26 /CAN2_RX / LPUART1_RTS_B /EVT8_B	Channel 1	T6	O	OV_{DD}	1
FTM7_CH2/ **IIC4_SCL** / GPIO1_DAT27 /CAN2_TX / LPUART1_CTS_B /EVT7_B	Channel 2	U7	IO	OV_{DD}	---
FTM7_EXTCLK/ **IIC3_SDA** / GPIO1_DAT28 /CAN1_RX / LPUART1_SIN /EVT6_B	External Clock	U3	I	OV_{DD}	1
FTM8_CH0/ **XSPI1_A_CS1_B** / GPIO2_DAT20 /cfg_svr1	Channel 0	D12	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
FTM8_CH1/ **XSPI1_A_CS0_B** / GPIO2_DAT21 /cfg_svr0	Channel 1	H12	O	OV_{DD}	1, 4
FTM8_CH2/ **XSPI1_A_SCK** / GPIO2_DAT22 /cfg_eng_use0	Channel 2	H10	O	OV_{DD}	1, 5
FTM8_EXTCLK/ **XSPI1_A_DQS** / GPIO2_DAT23	External Clock	F10	I	OV_{DD}	1
Controller Area Network					
CAN1_RX/ **IIC3_SDA** / GPIO1_DAT28 / LPUART1_SIN / FTM7_EXTCLK /EVT6_B	Receive Data	U3	I	OV_{DD}	1
CAN1_TX/ **IIC3_SCL** / GPIO1_DAT29 / LPUART1_SOUT / FTM7_CH0 /EVT5_B	Transmit Data	V2	O	OV_{DD}	1
CAN2_RX/ **IIC4_SDA** / GPIO1_DAT26 / LPUART1_RTS_B / FTM7_CH1 /EVT8_B	Receive Data	T6	I	OV_{DD}	1
CAN2_TX/ **IIC4_SCL** / GPIO1_DAT27 / LPUART1_CTS_B / FTM7_CH2 /EVT7_B	Transmit Data	U7	O	OV_{DD}	1
Power-On-Reset Configuration					
cfg_dram_type/ **EMI1_MDC**	DRAM Select	AK6	I	OV_{DD}	1, 4
cfg_eng_use0/ **XSPI1_A_SCK** / GPIO2_DAT22 /FTM8_CH2	Power-on-Reset Configuration	H10	I	OV_{DD}	1, 5
cfg_gpinput0/ **SDHC1_DAT0** / GPIO1_DAT17 /SPI1_SIN / SAI2_TX_DATA / SAI2_RX_DATA	General Input	N3	I	EV_{DD}	1, 4
cfg_gpinput1/ **SDHC1_DAT1** / GPIO1_DAT18 /SPI1_PCS2 / SAI2_TX_BCLK / SAI2_RX_BCLK	General Input	P4	I	EV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
cfg_gpinput2/ **SDHC1_DAT2** / GPIO1_DAT19 /SPI1_PCS1 / SAI1_TX_SYNC / SAI1_RX_SYNC	General Input	N1	I	EV_{DD}	1, 4
cfg_gpinput3/ **SDHC1_DAT3** / GPIO1_DAT20 /SPI1_PCS0 / SAI1_TX_DATA / SAI1_RX_DATA	General Input	L5	I	EV_{DD}	1, 4
cfg_gpinput4/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / LPUART5_RTS_B / FTM5_CH1 /XSPI1_B_DATA0	General Input	E17	I	OV_{DD}	1, 4
cfg_gpinput5/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / LPUART5_CTS_B / FTM5_CH2 /XSPI1_B_DATA1	General Input	D18	I	OV_{DD}	1, 4
cfg_gpinput6/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / LPUART5_SIN / FTM5_EXTCLK / XSPI1_B_DATA2	General Input	H18	I	OV_{DD}	1, 4
cfg_gpinput7/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / LPUART5_SOUT / FTM5_CH0 /XSPI1_B_DATA3	General Input	F18	I	OV_{DD}	1, 4
cfg_rcw_src0/ **UART2_SOUT** / GPIO1_DAT07 / LPUART6_RTS_B / FTM6_CH1	Reset Configuration Word	AC5	I	OV_{DD}	1, 4
cfg_rcw_src1/ **UART1_SOUT** / GPIO1_DAT11 / LPUART6_SOUT /FTM6_CH0	Reset Configuration Word	AB6	I	OV_{DD}	1, 4
cfg_rcw_src2/ **ASLEEP** / GPIO2_DAT06 /EVT9_B	Reset Configuration Word	AA1	I	OV_{DD}	1, 4
cfg_rcw_src3/ **CLK_OUT** / GPIO2_DAT07 /FTM1_CH1 / EVT4_B	Reset Configuration Word	AB4	I	OV_{DD}	1, 4
cfg_svr0/ **XSPI1_A_CS0_B** / GPIO2_DAT21 /FTM8_CH1	Power-on-Reset Configuration	H12	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
cfg_svr1/ **XSPI1_A_CS1_B** / GPIO2_DAT20 /FTM8_CH0	Power-on-Reset Configuration	D12	I	OV_{DD}	1, 5
SPI1					
SPI1_PCS0/ **SDHC1_DAT3** / GPIO1_DAT20 / SAI1_TX_DATA / SAI1_RX_DATA /cfg_gpinput3	SPI Chip Select	L5	IO	EV_{DD}	4
SPI1_PCS1/ **SDHC1_DAT2** / GPIO1_DAT19 / SAI1_TX_SYNC / SAI1_RX_SYNC / cfg_gpinput2	SPI Chip Select	N1	O	EV_{DD}	1, 4
SPI1_PCS2/ **SDHC1_DAT1** / GPIO1_DAT18 / SAI2_TX_BCLK / SAI2_RX_BCLK /cfg_gpinput1	SPI Chip Select	P4	O	EV_{DD}	1, 4
SPI1_PCS3/ **SDHC1_VSEL** / GPIO1_DAT15	SPI Chip Select	M4	O	OV_{DD}	1
SPI1_SCK/ **SDHC1_CLK** / GPIO1_DAT16 / SAI2_TX_SYNC / SAI2_RX_SYNC	Serial Clock	M6	IO	EV_{DD}	---
SPI1_SIN/ **SDHC1_DAT0** / GPIO1_DAT17 / SAI2_TX_DATA / SAI2_RX_DATA /cfg_gpinput0	Serial Data Input	N3	I	EV_{DD}	1, 4
SPI1_SOUT/ **SDHC1_CMD** / GPIO1_DAT21 / SAI1_TX_BCLK / SAI1_RX_BCLK	Serial Data Output	N7	O	EV_{DD}	1
SPI2					
SPI2_PCS0/ **SDHC2_DAT3** / GPIO2_DAT14 / LPUART5_SOUT / FTM5_CH0 / XSPI1_B_DATA3 / cfg_gpinput7	SPI Chip Select	F18	IO	OV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI2_PCS1/ **SDHC2_DAT2** / GPIO2_DAT13 / LPUART5_SIN / FTM5_EXTCLK / XSPI1_B_DATA2 / cfg_gpinput6	SPI Chip Select	H18	O	OV_{DD}	1, 4
SPI2_PCS2/ **SDHC2_DAT1** / GPIO2_DAT12 / LPUART5_CTS_B / FTM5_CH2 / XSPI1_B_DATA1 / cfg_gpinput5	SPI Chip Select	D18	O	OV_{DD}	1, 4
SPI2_PCS3/ **SDHC2_DS** / GPIO2_DAT10 / XSPI1_B_DQS	SPI Chip Select	B20	O	OV_{DD}	1
SPI2_SCK/ **SDHC2_CLK** / GPIO2_DAT09 / XSPI1_B_SCK	Serial Clock	F20	IO	OV_{DD}	---
SPI2_SIN/ **SDHC2_DAT0** / GPIO2_DAT11 / LPUART5_RTS_B / FTM5_CH1 / XSPI1_B_DATA0 / cfg_gpinput4	Serial Data Input	E17	I	OV_{DD}	1, 4
SPI2_SOUT/ **SDHC2_CMD** / GPIO2_DAT19 / XSPI1_B_CS1_B	Serial Data Output	G21	O	OV_{DD}	1
SPI 3					
SPI3_PCS0 /GPIO3_DAT15 / EC1_1588_TRIG_IN2 / SWITCH_1588_DAT2	SPI Chip Select	H6	O	OV_{DD}	1
SPI3_PCS1/ **USB_PWRFAULT** / GPIO3_DAT17	SPI Chip Select	H8	O	OV_{DD}	1
SPI3_PCS2/ **USB_DRVVBUS** / GPIO3_DAT18	SPI Chip Select	G7	O	OV_{DD}	1
SPI3_SCK /GPIO3_DAT14 / EC1_1722_DAT3	Serial Clock	K6	O	OV_{DD}	1
SPI3_SIN /GPIO3_DAT13 / EC1_1722_DAT2	Serial Data Input	K4	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SPI3_SOUT /GPIO3_DAT16 / EC1_1588_ALARM_OUT2 / SWITCH_1588_DAT3	Serial Data Output	J5	O	OV_{DD}	1
Ethernet Controller with 1588 Controller					
EC1_1588_ALARM_OUT1/ **EC1_TXD2** /GPIO3_DAT11 / SAI4_TX_DATA / SAI4_RX_DATA /FTM1_CH6	Alarm Out	AD4	O	OV_{DD}	1
EC1_1588_ALARM_OUT2/ **SPI3_SOUT** /GPIO3_DAT16 / SWITCH_1588_DAT3	Alarm Out	J5	O	OV_{DD}	1
EC1_1588_CLK_IN/ **EC1_RX_CLK** / GPIO3_DAT01 / SAI3_TX_SYNC / SAI3_RX_SYNC / FTM1_QD_PHA	Clock Input	AD2	I	OV_{DD}	1
EC1_1588_CLK_OUT/ **EC1_TXD1** /GPIO3_DAT10 / SAI3_TX_DATA / SAI3_RX_DATA /FTM1_CH5	Clock Out	AF4	O	OV_{DD}	1
EC1_1588_PULSE_OUT1/ **EC1_TXD3** /GPIO3_DAT12 / SAI5_TX_DATA / SAI5_RX_DATA /FTM1_CH7	Pulse Out	AG5	O	OV_{DD}	1
EC1_1588_PULSE_OUT2/ **EC1_TXD0** /GPIO3_DAT09 / SAI6_TX_DATA / SAI6_RX_DATA /FTM1_CH4	Pulse Out	AF6	O	OV_{DD}	1
EC1_1588_TRIG_IN1/ **EC1_RX_DV** / GPIO3_DAT00 / SAI6_TX_SYNC / SAI6_RX_SYNC / FTM1_QD_PHB	Trigger In	AH2	I	OV_{DD}	1
EC1_1588_TRIG_IN2/ **SPI3_PCS0** /GPIO3_DAT15 / SWITCH_1588_DAT2	Trigger In	H6	I	OV_{DD}	1
LPUART					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LPUART1_CTS_B/ **IIC4_SCL** /GPIO1_DAT27 / CAN2_TX /FTM7_CH2 / EVT7_B	Clear To Send	U7	I	OV_{DD}	1
LPUART1_RTS_B/ **IIC4_SDA** /GPIO1_DAT26 / CAN2_RX /FTM7_CH1 / EVT8_B	Request To Send	T6	O	OV_{DD}	1
LPUART1_SIN/ **IIC3_SDA** / GPIO1_DAT28 /CAN1_RX / FTM7_EXTCLK /EVT6_B	Receive Data	U3	I	OV_{DD}	1
LPUART1_SOUT/ **IIC3_SCL** / GPIO1_DAT29 /CAN1_TX / FTM7_CH0 /EVT5_B	Transmit Data	V2	IO	OV_{DD}	---
LPUART2_CTS_B/ **XSPI1_A_DATA5** / GPIO2_DAT29 /FTM2_CH2	Clear To Send	D14	I	OV_{DD}	1
LPUART2_RTS_B/ **XSPI1_A_DATA4** / GPIO2_DAT28 /FTM2_CH1	Request To Send	F14	O	OV_{DD}	1
LPUART2_SIN/ **XSPI1_A_DATA6** / GPIO2_DAT30 / FTM2_EXTCLK	Receive Data	D16	I	OV_{DD}	1
LPUART2_SOUT/ **XSPI1_A_DATA7** / GPIO2_DAT31	Transmit Data	G15	IO	OV_{DD}	---
LPUART3_CTS_B/ **XSPI1_A_DATA1** / GPIO2_DAT25 /FTM3_CH2	Clear To Send	F12	I	OV_{DD}	1
LPUART3_RTS_B/ **XSPI1_A_DATA0** / GPIO2_DAT24 /FTM3_CH1	Request To Send	G11	O	OV_{DD}	1
LPUART3_SIN/ **XSPI1_A_DATA2** / GPIO2_DAT26 / FTM3_EXTCLK	Receive Data	H14	I	OV_{DD}	1
LPUART3_SOUT/ **XSPI1_A_DATA3** / GPIO2_DAT27 /FTM3_CH0	Transmit Data	E13	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LPUART4_CTS_B/ **SDHC2_DAT5** / GPIO2_DAT16 /IIC7_SCL / FTM4_CH2 /XSPI1_B_DATA5	Clear To Send	D20	I	OV_{DD}	1
LPUART4_RTS_B/ **SDHC2_DAT4** / GPIO2_DAT15 /IIC7_SDA / FTM4_CH1 /XSPI1_B_DATA4	Request To Send	G19	O	OV_{DD}	1
LPUART4_SIN/ **SDHC2_DAT6** / GPIO2_DAT17 /IIC8_SDA / FTM4_EXTCLK / XSPI1_B_DATA6	Receive Data	H20	I	OV_{DD}	1
LPUART4_SOUT/ **SDHC2_DAT7** / GPIO2_DAT18 /IIC8_SCL / FTM4_CH0 /XSPI1_B_DATA7	Transmit Data	H22	IO	OV_{DD}	---
LPUART5_CTS_B/ **SDHC2_DAT1** / GPIO2_DAT12 /SPI2_PCS2 / FTM5_CH2 / XSPI1_B_DATA1 / cfg_gpinput5	Clear To Send	D18	I	OV_{DD}	1, 4
LPUART5_RTS_B/ **SDHC2_DAT0** / GPIO2_DAT11 /SPI2_SIN / FTM5_CH1 / XSPI1_B_DATA0 / cfg_gpinput4	Request To Send	E17	O	OV_{DD}	1, 4
LPUART5_SIN/ **SDHC2_DAT2** / GPIO2_DAT13 /SPI2_PCS1 / FTM5_EXTCLK / XSPI1_B_DATA2 / cfg_gpinput6	Receive Data	H18	I	OV_{DD}	1, 4
LPUART5_SOUT/ **SDHC2_DAT3** / GPIO2_DAT14 /SPI2_PCS0 / FTM5_CH0 / XSPI1_B_DATA3 / cfg_gpinput7	Transmit Data	F18	IO	OV_{DD}	4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
LPUART6_CTS_B/ **UART2_SIN** /GPIO1_DAT06 / FTM6_CH2	Clear To Send	AD6	I	OV_{DD}	1
LPUART6_RTS_B/ **UART2_SOUT** / GPIO1_DAT07 /FTM6_CH1 / cfg_rcw_src0	Request To Send	AC5	O	OV_{DD}	1, 4
LPUART6_SIN/ **UART1_SIN** / GPIO1_DAT10 / FTM6_EXTCLK	Receive Data	AE7	I	OV_{DD}	1
LPUART6_SOUT/ **UART1_SOUT** / GPIO1_DAT11 /FTM6_CH0 / cfg_rcw_src1	Transmit Data	AB6	O	OV_{DD}	1, 4
USB					
USB2_DRVVBUS/ **IIC6_SDA** / GPIO1_DAT22 / SDHC2_CLK_SYNC_IN / EVT0_B	DR VBUS	H16	O	OV_{DD}	1
USB2_PWRFAULT/ **IIC6_SCL** /GPIO1_DAT23 / SDHC2_CLK_SYNC_OUT / EVT3_B	Power Fault	F16	I	OV_{DD}	1
Synchronous Audio Interfaces					
SAI1_RX_BCLK/ **SDHC1_CMD** / GPIO1_DAT21 /SPI1_SOUT / SAI1_TX_BCLK	Receive Clock	N7	I	EV_{DD}	1
SAI1_RX_DATA/ **SDHC1_DAT3** / GPIO1_DAT20 /SPI1_PCS0 / SAI1_TX_DATA /cfg_gpinput3	Receiev Data	L5	I	EV_{DD}	1, 4
SAI1_RX_SYNC/ **SDHC1_DAT2** / GPIO1_DAT19 /SPI1_PCS1 / SAI1_TX_SYNC /cfg_gpinput2	Receive Sync	N1	IO	EV_{DD}	4
SAI1_TX_BCLK/ **SDHC1_CMD** / GPIO1_DAT21 /SPI1_SOUT / SAI1_RX_BCLK	Transmit Clock	N7	I	EV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SAI1_TX_DATA/ **SDHC1_DAT3** / GPIO1_DAT20 /SPI1_PCS0 / SAI1_RX_DATA /cfg_gpinput3	Transmit Data	L5	O	EV_{DD}	1, 4
SAI1_TX_SYNC/ **SDHC1_DAT2** / GPIO1_DAT19 /SPI1_PCS1 / SAI1_RX_SYNC / cfg_gpinput2	Transmit Sync	N1	IO	EV_{DD}	4
SAI2_RX_BCLK/ **SDHC1_DAT1** / GPIO1_DAT18 /SPI1_PCS2 / SAI2_TX_BCLK /cfg_gpinput1	Receive Clock	P4	I	EV_{DD}	1, 4
SAI2_RX_DATA/ **SDHC1_DAT0** / GPIO1_DAT17 /SPI1_SIN / SAI2_TX_DATA /cfg_gpinput0	Receiev Data	N3	I	EV_{DD}	1, 4
SAI2_RX_SYNC/ **SDHC1_CLK** / GPIO1_DAT16 /SPI1_SCK / SAI2_TX_SYNC	Receive Sync	M6	IO	EV_{DD}	---
SAI2_TX_BCLK/ **SDHC1_DAT1** / GPIO1_DAT18 /SPI1_PCS2 / SAI2_RX_BCLK /cfg_gpinput1	Transmit Clock	P4	I	EV_{DD}	1, 4
SAI2_TX_DATA/ **SDHC1_DAT0** / GPIO1_DAT17 /SPI1_SIN / SAI2_RX_DATA /cfg_gpinput0	Transmit Data	N3	O	EV_{DD}	1, 4
SAI2_TX_SYNC/ **SDHC1_CLK** / GPIO1_DAT16 /SPI1_SCK / SAI2_RX_SYNC	Transmit Sync	M6	IO	EV_{DD}	---
SAI3_RX_BCLK/ **EC1_RXD1** / GPIO3_DAT03 / SAI3_TX_BCLK	Receive Clock	AF2	I	OV_{DD}	1
SAI3_RX_DATA/ **EC1_TXD1** / GPIO3_DAT10 / SAI3_TX_DATA /FTM1_CH5 / EC1_1588_CLK_OUT	Receiev Data	AF4	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SAI3_RX_SYNC/ **EC1_RX_CLK** / GPIO3_DAT01 / SAI3_TX_SYNC / FTM1_QD_PHA / EC1_1588_CLK_IN	Receive Sync	AD2	IO	OV_{DD}	---
SAI3_TX_BCLK/ **EC1_RXD1** / GPIO3_DAT03 / SAI3_RX_BCLK	Transmit Clock	AF2	I	OV_{DD}	1
SAI3_TX_DATA/ **EC1_TXD1** / GPIO3_DAT10 / SAI3_RX_DATA /FTM1_CH5 / EC1_1588_CLK_OUT	Transmit Data	AF4	O	OV_{DD}	1
SAI3_TX_SYNC/ **EC1_RX_CLK** / GPIO3_DAT01 / SAI3_RX_SYNC / FTM1_QD_PHA / EC1_1588_CLK_IN	Transmit Sync	AD2	IO	OV_{DD}	---
SAI4_RX_BCLK/ **EC1_RXD2** / GPIO3_DAT04 / SAI4_TX_BCLK /FTM1_CH2	Receive Clock	AE3	I	OV_{DD}	1
SAI4_RX_DATA/ **EC1_TXD2** / GPIO3_DAT11 / SAI4_TX_DATA /FTM1_CH6 / EC1_1588_ALARM_OUT1	Receiev Data	AD4	I	OV_{DD}	1
SAI4_RX_SYNC/ **EC1_GTX_CLK** / GPIO3_DAT07 / SAI4_TX_SYNC / FTM1_EXTCLK / SWITCH_1588_DAT0	Receive Sync	AH4	IO	OV_{DD}	---
SAI4_TX_BCLK/ **EC1_RXD2** / GPIO3_DAT04 / SAI4_RX_BCLK /FTM1_CH2	Transmit Clock	AE3	I	OV_{DD}	1
SAI4_TX_DATA/ **EC1_TXD2** / GPIO3_DAT11 / SAI4_RX_DATA /FTM1_CH6 / EC1_1588_ALARM_OUT1	Transmit Data	AD4	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SAI4_TX_SYNC/ **EC1_GTX_CLK** / GPIO3_DAT07 / SAI4_RX_SYNC / FTM1_EXTCLK / SWITCH_1588_DAT0	Transmit Sync	AH4	IO	OV_{DD}	---
SAI5_RX_BCLK/ **EC1_RXD3** / GPIO3_DAT05 / SAI5_TX_BCLK /FTM1_CH3 / EC1_1722_DAT1	Receive Clock	AE1	I	OV_{DD}	1
SAI5_RX_DATA/ **EC1_TXD3** / GPIO3_DAT12 / SAI5_TX_DATA /FTM1_CH7 / EC1_1588_PULSE_OUT1	Receiev Data	AG5	I	OV_{DD}	1
SAI5_RX_SYNC/ **EC1_TX_EN** /GPIO3_DAT08 / SAI5_TX_SYNC / FTM1_FAULT / SWITCH_1588_DAT1	Receive Sync	AJ3	IO	OV_{DD}	---
SAI5_TX_BCLK/ **EC1_RXD3** / GPIO3_DAT05 / SAI5_RX_BCLK /FTM1_CH3 / EC1_1722_DAT1	Transmit Clock	AE1	I	OV_{DD}	1
SAI5_TX_DATA/ **EC1_TXD3** / GPIO3_DAT12 / SAI5_RX_DATA /FTM1_CH7 / EC1_1588_PULSE_OUT1	Transmit Data	AG5	O	OV_{DD}	1
SAI5_TX_SYNC/ **EC1_TX_EN** /GPIO3_DAT08 / SAI5_RX_SYNC / FTM1_FAULT / SWITCH_1588_DAT1	Transmit Sync	AJ3	IO	OV_{DD}	---
SAI6_RX_BCLK/ **EC1_RXD0** / GPIO3_DAT02 / SAI6_TX_BCLK	Receive Clock	AG1	I	OV_{DD}	1
SAI6_RX_DATA/ **EC1_TXD0** / GPIO3_DAT09 / SAI6_TX_DATA /FTM1_CH4 / EC1_1588_PULSE_OUT2	Receiev Data	AF6	I	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
SAI6_RX_SYNC/ **EC1_RX_DV** / GPIO3_DAT00 / SAI6_TX_SYNC / FTM1_QD_PHB / EC1_1588_TRIG_IN1	Receive Sync	AH2	IO	OV_{DD}	---
SAI6_TX_BCLK/ **EC1_RXD0** / GPIO3_DAT02 / SAI6_RX_BCLK	Transmit Clock	AG1	I	OV_{DD}	1
SAI6_TX_DATA/ **EC1_TXD0** / GPIO3_DAT09 / SAI6_RX_DATA /FTM1_CH4 / EC1_1588_PULSE_OUT2	Transmit Data	AF6	O	OV_{DD}	1
SAI6_TX_SYNC/ **EC1_RX_DV** / GPIO3_DAT00 / SAI6_RX_SYNC / FTM1_QD_PHB / EC1_1588_TRIG_IN1	Transmit Sync	AH2	IO	OV_{DD}	---
USB PHY 1 and 2					
USB1_D_M	USB PHY Data Minus	D2	IO	-	---
USB1_D_P	USB PHY Data Plus	E1	IO	-	---
USB1_ID	USB PHY ID Detect	D4	I	-	---
USB1_RESREF	USB PHY Impedance Calibration	F4	IO	-	18
USB1_RX_M	USB PHY 3.0 Receive Data (negative)	K2	I	-	---
USB1_RX_P	USB PHY 3.0 Receive Data (positive)	L1	I	-	---
USB1_TX_M	USB PHY 3.0 Transmit Data (negative)	G1	O	-	---
USB1_TX_P	USB PHY 3.0 Transmit Data (positive)	H2	O	-	---
USB1_VBUS	USB PHY VBUS	H4	I	-	---
USB2_D_M	USB PHY Data Minus	B8	IO	-	---
USB2_D_P	USB PHY Data Plus	A7	IO	-	---
USB2_ID	USB PHY ID Detect	E5	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
USB2_RESREF	USB PHY Impedance Calibration	F6	IO	-	18
USB2_RX_M	USB PHY 3.0 Receive Data (negative)	A3	I	-	---
USB2_RX_P	USB PHY 3.0 Receive Data (positive)	B2	I	-	---
USB2_TX_M	USB PHY 3.0 Transmit Data (negative)	B6	O	-	---
USB2_TX_P	USB PHY 3.0 Transmit Data (positive)	A5	O	-	---
USB2_VBUS	USB PHY VBUS	D6	I	-	---
USB_DRVVBUS / GPIO3_DAT18 /SPI3_PCS2	USB PHY Digital signal - Drive VBUS	G7	O	OV_{DD}	1
USB_PWRFAULT / GPIO3_DAT17 /SPI3_PCS1	USB PHY Digital signal - Power Fault	H8	I	OV_{DD}	1
IEEE 1588 signals					
SWITCH_1588_DAT0/ **EC1_GTX_CLK** / GPIO3_DAT07 / SAI4_TX_SYNC / SAI4_RX_SYNC / FTM1_EXTCLK	IEEE 1588 signals	AH4	IO	OV_{DD}	---
SWITCH_1588_DAT1/ **EC1_TX_EN** /GPIO3_DAT08 / SAI5_TX_SYNC / SAI5_RX_SYNC / FTM1_FAULT	IEEE 1588 signals	AJ3	IO	OV_{DD}	---
SWITCH_1588_DAT2/ **SPI3_PCS0** /GPIO3_DAT15 / EC1_1588_TRIG_IN2	IEEE 1588 signals	H6	IO	OV_{DD}	---
SWITCH_1588_DAT3/ **SPI3_SOUT** /GPIO3_DAT16 / EC1_1588_ALARM_OUT2	IEEE 1588 signals	J5	IO	OV_{DD}	---
IEEE 1722 signals					
EC1_1722_DAT0/ **EC1_GTX_CLK125** / GPIO3_DAT06	IEEE 1722 signals	AK2	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
EC1_1722_DAT1/ **EC1_RXD3** /GPIO3_DAT05 / SAI5_TX_BCLK / SAI5_RX_BCLK /FTM1_CH3	IEEE 1722 signals	AE1	IO	OV_{DD}	---
EC1_1722_DAT2/ **SPI3_SIN** / GPIO3_DAT13	IEEE 1722 signals	K4	IO	OV_{DD}	---
EC1_1722_DAT3/ **SPI3_SCK** /GPIO3_DAT14	IEEE 1722 signals	K6	IO	OV_{DD}	---
Display					
DP_AUX_N	Auxillary port (negative)	A19	IO	DP_SV_{DD}	---
DP_AUX_P	Auxillary port (positive)	B18	IO	DP_SV_{DD}	---
DP_HPD	Hot plug detect	F8	I	DP_OV_{DD}	24
DP_LANE0_N	Data lane (negative)	A11	O	DP_SV_{DD}	---
DP_LANE0_P	Data lane (positive)	B10	O	DP_SV_{DD}	---
DP_LANE1_N	Data lane (negative)	A13	O	DP_SV_{DD}	---
DP_LANE1_P	Data lane (positive)	B12	O	DP_SV_{DD}	---
DP_LANE2_N	Data lane (negative)	A15	O	DP_SV_{DD}	---
DP_LANE2_P	Data lane (positive)	B14	O	DP_SV_{DD}	---
DP_LANE3_N	Data lane (negative)	A17	O	DP_SV_{DD}	---
DP_LANE3_P	Data lane (positive)	B16	O	DP_SV_{DD}	---
DP_REFCLK_N	27MHz HCSL reference clock in(negative)	D10	I	DP_SV_{DD}	---
DP_REFCLK_P	27MHz HCSL reference clock in(positive)	E9	I	DP_SV_{DD}	---
DP_REXT	Calibration resistor	D8	I	DP_OV_{DD}	25
Power and Ground Signals					
GND001	Core, Platform and PLL Ground	A9	---	---	---
GND002	Core, Platform and PLL Ground	A21	---	---	---
GND003	Core, Platform and PLL Ground	A25	---	---	---
GND004	Core, Platform and PLL Ground	B4	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND005	Core, Platform and PLL Ground	B30	---	---	---
GND006	Core, Platform and PLL Ground	C1	---	---	---
GND007	Core, Platform and PLL Ground	C3	---	---	---
GND008	Core, Platform and PLL Ground	C5	---	---	---
GND009	Core, Platform and PLL Ground	C7	---	---	---
GND010	Core, Platform and PLL Ground	C9	---	---	---
GND011	Core, Platform and PLL Ground	C11	---	---	---
GND012	Core, Platform and PLL Ground	C13	---	---	---
GND013	Core, Platform and PLL Ground	C15	---	---	---
GND014	Core, Platform and PLL Ground	C17	---	---	---
GND015	Core, Platform and PLL Ground	C19	---	---	---
GND016	Core, Platform and PLL Ground	C23	---	---	---
GND017	Core, Platform and PLL Ground	C27	---	---	---
GND018	Core, Platform and PLL Ground	E3	---	---	---
GND019	Core, Platform and PLL Ground	E7	---	---	---
GND020	Core, Platform and PLL Ground	E11	---	---	---
GND021	Core, Platform and PLL Ground	E15	---	---	---
GND022	Core, Platform and PLL Ground	E19	---	---	---
GND023	Core, Platform and PLL Ground	E21	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND024	Core, Platform and PLL Ground	E25	---	---	---
GND025	Core, Platform and PLL Ground	E29	---	---	---
GND026	Core, Platform and PLL Ground	F2	---	---	---
GND027	Core, Platform and PLL Ground	G3	---	---	---
GND028	Core, Platform and PLL Ground	G5	---	---	---
GND029	Core, Platform and PLL Ground	G9	---	---	---
GND030	Core, Platform and PLL Ground	G13	---	---	---
GND031	Core, Platform and PLL Ground	G17	---	---	---
GND032	Core, Platform and PLL Ground	G23	---	---	---
GND033	Core, Platform and PLL Ground	G27	---	---	---
GND034	Core, Platform and PLL Ground	J1	---	---	---
GND035	Core, Platform and PLL Ground	J3	---	---	---
GND036	Core, Platform and PLL Ground	J21	---	---	---
GND037	Core, Platform and PLL Ground	J25	---	---	---
GND038	Core, Platform and PLL Ground	J29	---	---	---
GND039	Core, Platform and PLL Ground	K16	---	---	---
GND040	Core, Platform and PLL Ground	L3	---	---	---
GND041	Core, Platform and PLL Ground	L7	---	---	---
GND042	Core, Platform and PLL Ground	L9	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND043	Core, Platform and PLL Ground	L11	---	---	---
GND044	Core, Platform and PLL Ground	L15	---	---	---
GND045	Core, Platform and PLL Ground	L19	---	---	---
GND046	Core, Platform and PLL Ground	L27	---	---	---
GND047	Core, Platform and PLL Ground	M2	---	---	---
GND048	Core, Platform and PLL Ground	M14	---	---	---
GND049	Core, Platform and PLL Ground	M18	---	---	---
GND050	Core, Platform and PLL Ground	M22	---	---	---
GND051	Core, Platform and PLL Ground	N5	---	---	---
GND052	Core, Platform and PLL Ground	N9	---	---	---
GND053	Core, Platform and PLL Ground	N13	---	---	---
GND054	Core, Platform and PLL Ground	N17	---	---	---
GND055	Core, Platform and PLL Ground	N25	---	---	---
GND056	Core, Platform and PLL Ground	N29	---	---	---
GND057	Core, Platform and PLL Ground	P12	---	---	---
GND058	Core, Platform and PLL Ground	P16	---	---	---
GND059	Core, Platform and PLL Ground	P20	---	---	---
GND060	Core, Platform and PLL Ground	P22	---	---	---
GND061	Core, Platform and PLL Ground	R3	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND062	Core, Platform and PLL Ground	R11	---	---	---
GND063	Core, Platform and PLL Ground	R15	---	---	---
GND064	Core, Platform and PLL Ground	R19	---	---	---
GND065	Core, Platform and PLL Ground	R27	---	---	---
GND066	Core, Platform and PLL Ground	T10	---	---	---
GND067	Core, Platform and PLL Ground	T14	---	---	---
GND068	Core, Platform and PLL Ground	T18	---	---	---
GND069	Core, Platform and PLL Ground	T22	---	---	---
GND070	Core, Platform and PLL Ground	U5	---	---	---
GND071	Core, Platform and PLL Ground	U9	---	---	---
GND072	Core, Platform and PLL Ground	U13	---	---	---
GND073	Core, Platform and PLL Ground	U17	---	---	---
GND074	Core, Platform and PLL Ground	U25	---	---	---
GND075	Core, Platform and PLL Ground	U29	---	---	---
GND076	Core, Platform and PLL Ground	V12	---	---	---
GND077	Core, Platform and PLL Ground	V16	---	---	---
GND078	Core, Platform and PLL Ground	V20	---	---	---
GND079	Core, Platform and PLL Ground	V22	---	---	---
GND080	Core, Platform and PLL Ground	W3	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND081	Core, Platform and PLL Ground	W11	---	---	---
GND082	Core, Platform and PLL Ground	W15	---	---	---
GND083	Core, Platform and PLL Ground	W19	---	---	---
GND084	Core, Platform and PLL Ground	W27	---	---	---
GND085	Core, Platform and PLL Ground	Y10	---	---	---
GND086	Core, Platform and PLL Ground	Y14	---	---	---
GND087	Core, Platform and PLL Ground	Y18	---	---	---
GND088	Core, Platform and PLL Ground	Y22	---	---	---
GND089	Core, Platform and PLL Ground	AA5	---	---	---
GND090	Core, Platform and PLL Ground	AA9	---	---	---
GND091	Core, Platform and PLL Ground	AA13	---	---	---
GND092	Core, Platform and PLL Ground	AB12	---	---	---
GND093	Core, Platform and PLL Ground	AB22	---	---	---
GND094	Core, Platform and PLL Ground	AC3	---	---	---
GND095	Core, Platform and PLL Ground	AC11	---	---	---
GND096	Core, Platform and PLL Ground	AD8	---	---	---
GND097	Core, Platform and PLL Ground	AE5	---	---	---
GND098	Core, Platform and PLL Ground	AG3	---	---	---
GND099	Core, Platform and PLL Ground	AH6	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
GND100	Core, Platform and PLL Ground	AJ1	---	---	---
GND101	Core, Platform and PLL Ground	AJ5	---	---	---
GND102	Core, Platform and PLL Ground	AK8	---	---	---
SD_GND01	SerDes1 core logic ground	AB16	---	---	20
SD_GND02	SerDes1 core logic ground	AB18	---	---	20
SD_GND03	SerDes1 core logic ground	AB20	---	---	20
SD_GND04	SerDes1 core logic ground	AC21	---	---	20
SD_GND05	SerDes1 core logic ground	AE11	---	---	20
SD_GND06	SerDes1 core logic ground	AE13	---	---	20
SD_GND07	SerDes1 core logic ground	AE15	---	---	20
SD_GND08	SerDes1 core logic ground	AE17	---	---	20
SD_GND09	SerDes1 core logic ground	AE19	---	---	20
SD_GND10	SerDes1 core logic ground	AF20	---	---	20
SD_GND11	SerDes1 core logic ground	AG11	---	---	20
SD_GND12	SerDes1 core logic ground	AH10	---	---	20
SD_GND13	SerDes1 core logic ground	AH12	---	---	20
SD_GND14	SerDes1 core logic ground	AH14	---	---	20
SD_GND15	SerDes1 core logic ground	AH16	---	---	20
SD_GND16	SerDes1 core logic ground	AH18	---	---	20
SD_GND17	SerDes1 core logic ground	AH20	---	---	20
SD_GND18	SerDes1 core logic ground	AJ9	---	---	20
SD_GND19	SerDes1 core logic ground	AK18	---	---	20
SENSEGND	Ground Sense pin	AG7	---	---	---
OVDD1	General I/O supply	J17	---	OV_{DD}	---
OVDD2	General I/O supply	K18	---	OV_{DD}	---
OVDD3	General I/O supply	T8	---	OV_{DD}	---
OVDD4	General I/O supply	V8	---	OV_{DD}	---
G1VDD01	DDR supply	K24	---	$G1V_{DD}$	---
G1VDD02	DDR supply	M24	---	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
G1VDD03	DDR supply	N23	---	$G1V_{DD}$	---
G1VDD04	DDR supply	R23	---	$G1V_{DD}$	---
G1VDD05	DDR supply	U23	---	$G1V_{DD}$	---
G1VDD06	DDR supply	V24	---	$G1V_{DD}$	---
G1VDD07	DDR supply	W23	---	$G1V_{DD}$	---
G1VDD08	DDR supply	AA25	---	$G1V_{DD}$	---
G1VDD09	DDR supply	AA29	---	$G1V_{DD}$	---
G1VDD10	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD11	DDR supply	AE21	---	$G1V_{DD}$	---
G1VDD12	DDR supply	AE25	---	$G1V_{DD}$	---
G1VDD13	DDR supply	AE29	---	$G1V_{DD}$	---
G1VDD14	DDR supply	AG23	---	$G1V_{DD}$	---
G1VDD15	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD16	DDR supply	AH30	---	$G1V_{DD}$	---
G1VDD17	DDR supply	AJ21	---	$G1V_{DD}$	---
G1VDD18	DDR supply	AJ25	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AK28	---	$G1V_{DD}$	---
EVDD	eSDHC supply - switchable	P8	---	EV_{DD}	---
SVDD1	SerDes core logic supply	AA15	---	SV_{DD}	---
SVDD2	SerDes core logic supply	AA17	---	SV_{DD}	---
SVDD3	SerDes core logic supply	AA19	---	SV_{DD}	---
SVDD4	SerDes core logic supply	AB14	---	SV_{DD}	---
XVDD1	SerDes transceiver supply	AC15	---	XV_{DD}	---
XVDD2	SerDes transceiver supply	AC17	---	XV_{DD}	---
XVDD3	SerDes transceiver supply	AC19	---	XV_{DD}	---
FA_VL	Internal Use Only	A29	---	FA_VL	15
PROG_MTR	Internal Use Only	J13	---	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	J15	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	R7	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD02	Supply for cores and platform	L13	---	V_{DD}	---
VDD03	Supply for cores and platform	L17	---	V_{DD}	---
VDD04	Supply for cores and platform	L21	---	V_{DD}	---
VDD05	Supply for cores and platform	L23	---	V_{DD}	---
VDD06	Supply for cores and platform	M8	---	V_{DD}	---
VDD07	Supply for cores and platform	M10	---	V_{DD}	---
VDD08	Supply for cores and platform	M12	---	V_{DD}	---
VDD09	Supply for cores and platform	M16	---	V_{DD}	---
VDD10	Supply for cores and platform	N11	---	V_{DD}	---
VDD11	Supply for cores and platform	N15	---	V_{DD}	---
VDD12	Supply for cores and platform	N19	---	V_{DD}	---
VDD13	Supply for cores and platform	N21	---	V_{DD}	---
VDD14	Supply for cores and platform	P10	---	V_{DD}	---
VDD15	Supply for cores and platform	P14	---	V_{DD}	---
VDD16	Supply for cores and platform	P18	---	V_{DD}	---
VDD17	Supply for cores and platform	R9	---	V_{DD}	---
VDD18	Supply for cores and platform	R13	---	V_{DD}	---
VDD19	Supply for cores and platform	R17	---	V_{DD}	---
VDD20	Supply for cores and platform	R21	---	V_{DD}	---
VDD21	Supply for cores and platform	T12	---	V_{DD}	---
VDD22	Supply for cores and platform	T16	---	V_{DD}	---
VDD23	Supply for cores and platform	T20	---	V_{DD}	---
VDD24	Supply for cores and platform	U11	---	V_{DD}	---
VDD25	Supply for cores and platform	U15	---	V_{DD}	---
VDD26	Supply for cores and platform	U19	---	V_{DD}	---
VDD27	Supply for cores and platform	U21	---	V_{DD}	---
VDD28	Supply for cores and platform	V10	---	V_{DD}	---
VDD29	Supply for cores and platform	V14	---	V_{DD}	---
VDD30	Supply for cores and platform	V18	---	V_{DD}	---
VDD31	Supply for cores and platform	W9	---	V_{DD}	---
VDD32	Supply for cores and platform	W13	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
VDD33	Supply for cores and platform	W17	---	V_{DD}	---
VDD34	Supply for cores and platform	W21	---	V_{DD}	---
VDD35	Supply for cores and platform	Y8	---	V_{DD}	---
VDD36	Supply for cores and platform	Y12	---	V_{DD}	---
VDD37	Supply for cores and platform	Y16	---	V_{DD}	---
VDD38	Supply for cores and platform	Y20	---	V_{DD}	---
VDD39	Supply for cores and platform	AA11	---	V_{DD}	---
VDD40	Supply for cores and platform	AA21	---	V_{DD}	---
TA_BB_VDD	Low Power Security Monitor supply	AD12	---	$TA_BB_V_{DD}$	---
PIXEL_DVDD	Pixel Clock PLL digital supply	M20	---	$PIXEL_DV_{DD}$	---
AVDD_CGA1	A72 Core Cluster Group A PLL1 supply	AC9	---	AVDD_CGA1	---
AVDD_CGA2	A72 Core Cluster Group A PLL2 supply	AB10	---	AVDD_CGA2	---
AVDD_PLAT	Platform PLL supply	AB8	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	T24	---	AVDD_D1	---
AVDD_PIXEL	Pixel Clock PLL analog supply	AC13	---	AVDD_PIXEL	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AD16	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AD18	---	AVDD_SD1_PLL2	---
USB_HVDD1	USB PHY 3.3V Analog and Digital supply HS	J9	---	USB_HV_{DD}	---
USB_HVDD2	USB PHY 3.3V Analog and Digital supply HS	J11	---	USB_HV_{DD}	---
USB_SDVDD1	USB PHY 1.0/0.9V Analog and Digital HS	J7	---	USB_SDV_{DD}	---
USB_SDVDD2	USB PHY 1.0/0.9V Analog and Digital HS	K8	---	USB_SDV_{DD}	---
USB_SVDD1	USB PHY 1.0/0.9V Analog and Digital SS	K10	---	USB_SV_{DD}	---
USB_SVDD2	USB PHY 1.0/0.9V Analog and Digital SS	K12	---	USB_SV_{DD}	---
DP_OVDD	PMA 1.8V common I/O supply	J19	---	DP_OV_{DD}	---
DP_SVDD	PMA transmit core supply	K22	---	DP_SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DP_AVDD	PMA common core supply	K20	---	DP_AV_{DD}	---
SENSEVDD	VDD Sense pin	AF8	---	$SENSEV_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. 2. This output is actively driven during reset rather than being tri-stated during reset. 3. MDIC[0] is grounded through an 237Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 237Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 237Ω. Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3/DDR3L IOs. The MDIC[0:1] pins must be connected to 237Ω precision 1% resistors. MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors. 4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed. 5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset. 6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply. 7. This pin is an open-drain signal. 8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply. 9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. 10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation. 11. This pin requires a 200Ω ± 1% pull-up to respective power-supply. 14.This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. 15. These pins must be pulled to ground (GND). 16. This pin requires a 698Ω ± 1% pull-up to respective power-supply. 17. These pins should be tied to ground if the diode is not utilized for temperature monitoring. 18. This pin should be grounded through a 200Ω ± 1% 100-ppm/ ^{0}C precision resistor. 19. In normal operation, this pin must be pulled high to OV_{DD} with 1 kΩ. 20. SD_GND must be directly connected to GND. 21. This pin will not be tested using JTAG Boundary Scan operation. 22. This pin must be pulled to OVDD through a 100Ω to 1kΩ resistor. 23. PORESET_B should be asserted zero during the JTAG Boundary Scan Operation, and is required to be controllable on board.					

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
24. This pin requires an external 1-MΩ pull-down resistor.					
25. This pin requires an external 499Ω ± 1% pull-down resistor.					
26. Recommend that a weak pull-up resistor (10-100 kΩ) be placed on this pin to the respective power supply.					
27. This pin requires a pull-up to the respective power supply so as to meet the timing requirements in Table 13. RESET initialization timing specifications on page 75.					

Warning

See **"Connection Recommendations"**in QorIQ LS1028A Design Checklist (AN12028)" for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings

Table 2. Absolute maximum ratings [6, 7]

Characteristic	Symbol	Min	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3	1.08	V	1
Core PLL supply voltage	AV_{DD}_CGA1	-0.3	1.98	V	-
Core PLL supply voltage	AV_{DD}_CGA2	-0.3	1.98	V	-
Platform PLL supply voltage	AV_{DD}_PLAT	-0.3	1.98	V	-
DDR PLL supply voltage	AV_{DD}_D1	-0.3	1.98	V	-
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD1_PLL1	-0.3	1.48	V	-
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD1_PLL2	-0.3	1.48	V	-
SFP fuse programming	TA_PROG_SFP	-0.3	1.98	V	-

Table continues on the next page...

Table 2. Absolute maximum ratings [6, 7] (continued)

Characteristic	Symbol	Min	Max Value	Unit	Notes
Thermal monitor unity supply	TH_V_{DD}	-0.3	1.98	V	-
SPI2/3, FlexSPI, Tamper_Detect, System control, GPIO1/2/3, I2C, eSDHC2, SDHC1_VSEL, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, DUART, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN, LPUART	OV_{DD}	-0.3	1.98	V	-
DDR3L DRAM I/O voltage	$G1V_{DD}$	-0.3	1.42	V	-
DDR4 DRAM I/O voltage	$G1V_{DD}$	-0.3	1.26	V	-
Pixel clock PLL digital supply	$PIXEL_DV_{DD}$	-0.3	1.08	V	-
Pixel clock PLL analog supply	AV_{DD}_PIXEL	-0.3	1.98	V	-
PMA common I/O supply	DP_OV_{DD}	-0.3	1.98	V	-
PMA transmit supply	DP_SV_{DD}	-0.3	1.08	V	-
PMA common core supply	DP_AV_{DD}	-0.3	1.08	V	-
eSDHC1	EV_{DD}	-0.3	3.63	V	8
eSDHC1, SPI1, SAI1/2	EV_{DD}	-0.3	1.98	V	9
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK	SV_{DD}	-0.3	1.08	V	-
Pad power supply for SerDes transmitter	XV_{DD}	-0.3	1.48	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	-0.3	3.63	V	2
USB PHY analog and digital HS supply	USB_SDV_{DD}	-0.3	1.08	V	-
USB PHY analog and digital SS supply voltage	USB_SV_{DD}	-0.3	1.08	V	-
Battery Backed Security Monitor supply	$TA_BB_V_{DD}$	-0.3	1.08	V	-
Input voltage for DDR4 and DDR3L DRAM signals	GV_{IN}	-0.3	G1VDD x 1.05	V	3, 4
Input voltage for DDR3L DRAM reference	MV_{REF}	-0.3	G1VDD/2 x 1.05	V	3, 5

Table continues on the next page...

Table 2. Absolute maximum ratings [6, 7] (continued)

Characteristic	Symbol	Min	Max Value	Unit	Notes
SPI2/3, FlexSPI, Tamper_Detect, System control, GPIO1/2/3, I2C, eSDHC2, SDHC1_VSEL, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, DUART, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN, LPUART	OV_{IN}	-0.3	OV_{DD} x 1.1	V	3, 5
eSDHC1, SPI1, SAI1/2	EV_{IN}	-0.3	EV_{DD} x 1.1	V	3, 5
Input voltage for main power supply for internal circuitry of SerDes and DIFF_SYSCLK	SV_{IN}	-0.3	SV_{DD} x 1.05	V	5
PHY transceiver signals: USB transceiver supply for USB PHY	USB_HV_{IN}	-0.3	USB_HV_{DD} x 1.05	V	-
PHY transceiver signals: USB PHY Analog and Digital SS supply voltage	USB_SV_{IN}	-0.3	USB_SV_{DD} x 1.1	V	-
PHY transceiver signals: USB PHY Analog and Digital HS supply voltage	USB_SDV_{IN}	-0.3	USB_SDV_{DD} x 1.1	V	-
Storage temperature range	T_{STG}	-55	150	°C	-

1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

2. Transceiver supply for USB PHY.

3. **Caution:** The input voltage level of the signals must not exceed corresponding Max value. For example DDR4 must not exceed 5% of G1VDD.

4. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/Undershoot period should comply with JEDEC standards.

5. (G1, O, S, E)V_{IN}, USB_S*VIN and USB_HV_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in the Overshoot/undershoot voltage figure at the end of this section.

6. Functional operating conditions are given in Recommended operating conditions table. Absolute maximum ratings are stress ratings only, and functional operations at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damange to the device.

7. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.

8. When EV_{DD} is powered with 3.3V supply.

9. When EV_{DD} is powered with 1.8V supply.

3.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this chip.

WARNING

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Core and platform supply voltage	V_{DD}	1.0 V - 30 mV	1.0	1.0 V + 30 mV	V	1, 2, 3, 4
0.9V core and platform supply voltage	V_{DD}	0.9 V - 30 mV	0.9	0.9 V + 30 mV	V	1, 2, 3, 4
Core PLL supply voltage	AV_{DD}_CGA1	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
Core PLL supply voltage	AV_{DD}_CGA2	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
Platform PLL supply voltage	AV_{DD}_PLAT	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
DDR PLL supply voltage	AV_{DD}_D1	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	5
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD1_PLL1	1.35 V - 67 mV	1.35	1.35 V + 67 mV	V	-
PLL supply voltage (SerDes, filtered from XV_{DD})	AV_{DD}_SD1_PLL2	1.35 V - 67 mV	1.35	1.35 V + 67 mV	V	-
SFP fuse programming	TA_PROG_SFP	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	6
Thermal monitor unity supply	TH_V_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
SPI2/3, FlexSPI, Tamper_Detect, System control, GPIO1/2/3, I2C, eSDHC2, SDHC1_VSEL, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, DUART, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN, LPUART	OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
DDR3L DRAM I/O voltage	G1V_{DD}	1.35V - 67 mV	1.35	1.35V + 67 mV	V	-
DDR4 DRAM I/O voltage	G1V_{DD}	1.2V - 60 mV	1.2	1.2V + 60 mV	V	-
Pixel clock PLL digital supply	PIXEL_DV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
Pixel clock PLL digital supply	PIXEL_DV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
Pixel clock PLL analog supply	AV_{DD}_PIXEL	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
PMA common I/O supply	DP_OV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
PMA transmit supply	DP_SV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
PMA transmit supply (at 0.9 V)	DP_SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
PMA common core supply	DP_AV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
PMA common core supply (at 0.9 V)	DP_AV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
eSDHC1	EV_{DD}	3.3 V - 165 mV	3.3	3.3 V + 165 mV	V	-
eSDHC1, SPI1, SAI1/2	EV_{DD}	1.8 V - 90 mV	1.8	1.8 V + 90 mV	V	-
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK	SV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers and DIFF_SYSCLK	SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
Pad power supply for SerDes transmitter	XV_{DD}	1.35 V - 67 mV	1.35	1.35 V + 67 mV	V	-
USB PHY 3.3V high supply voltage	USB_HV_{DD}	3.3 - 165 mV	3.3	3.3 + 165 mV	V	7
USB PHY analog and digital HS supply	USB_SDV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
USB PHY analog and digital HS supply	USB_SDV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
USB PHY analog and digital SS supply voltage	USB_SV_{DD}	1.0 V - 50 mV	1.0	1.0 V + 50 mV	V	3
USB PHY analog and digital SS supply voltage	USB_SV_{DD}	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
Battery Backed Security Monitor supply	$TA_BB_V_{DD}$	1.0 V - 30 mV	1.0	1.0 V + 50 mV	V	3
Battery Backed Security Monitor supply	$TA_BB_V_{DD}$	0.9 V - 30 mV	0.9	0.9 V + 50 mV	V	3
Input voltage for DDR4 and DDR3L DRAM signals	GV_{IN}	GND	-	$G1V_{DD}$	V	8, 9

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

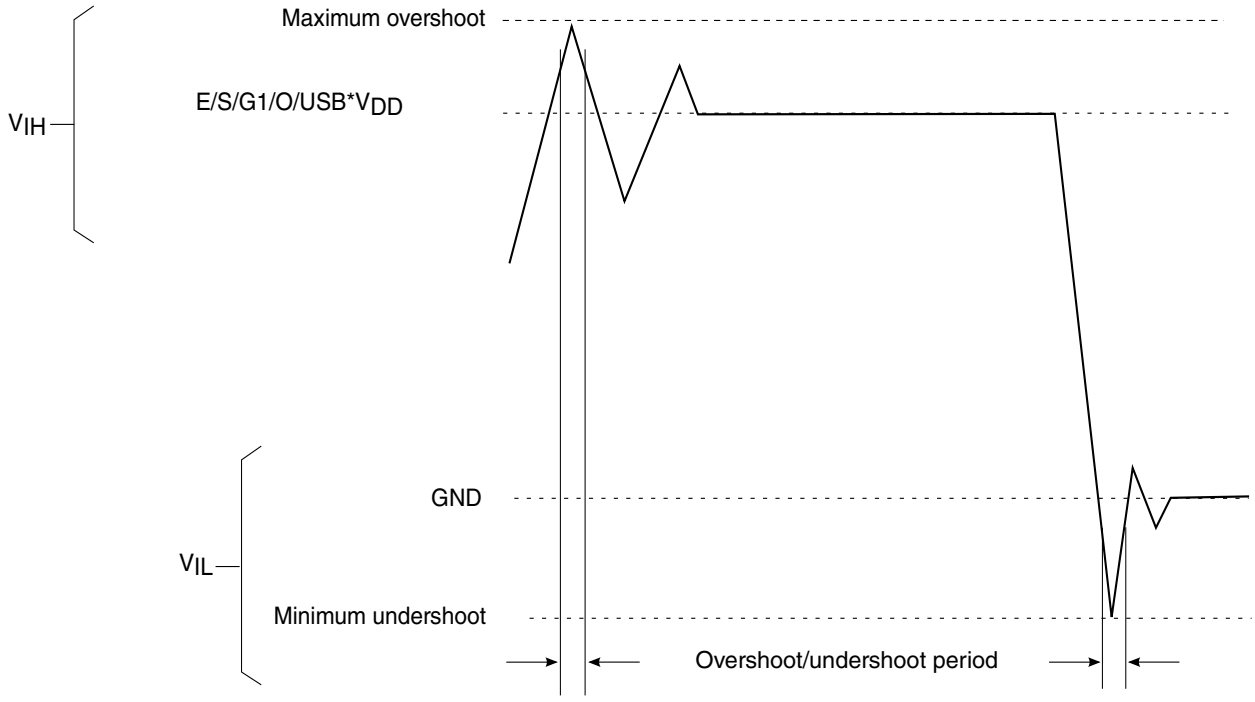
Parameter	Symbol	Min	Typ	Max	Unit	Notes
SPI2/3, FlexSPI, Tamper_Detect, System control, GPIO1/2/3, I2C, eSDHC2, SDHC1_VSEL, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, DUART, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN, LPUART	OV_{IN}	GND	-	OV_{DD}	V	8, 10
eSDHC1, SPI1, SAI1/2	EV_{IN}	GND	-	EV_{DD}	V	8, 10
Input voltage for main power supply for internal circuitry of SerDes and DIFF_SYSCLK	SV_{IN}	GND	-	SV_{DD}	V	10
PHY transceiver signals: USB transceiver supply for USB PHY	USB_HV_{IN}	GND	-	USB_HV_{DD}	V	-
PHY transceiver signals: USB PHY Analog and Digital SS supply voltage	USB_SV_{IN}	GND	-	USB_SV_{DD}	V	-
PHY transceiver signals: USB PHY Analog and Digital HS supply voltage	USB_SDV_{IN}	GND	-	USB_SDV_{DD}	V	-
Normal operating temperature range	T_A/T_J	T_A = 0	-	T_J = 105	°C	-
Extended temperature range	T_A/T_J	T_A = -40	-	T_J = 105	°C	-
High Extended temperature range	T_A/T_J	T_A = -40	-	T_J = 125	°C	-
AEC-Q100 Grade 3 temperature range	T_A/T_J	T_A = -40	-	T_J = 85	°C	11
Secure boot fuse programming operating temperature range	T_A/T_J	T_A = 0	-	T_J = 105	°C	6

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin. 2. Operation at 1.08V is allowable for up to 25 ms at initial power on. 3. For supported voltage requirement for a given part number, see the Orderable part numbers addressed by this document. 4. For additional information, see the Core and platform supply voltage filtering section in the chip design checklist. 5. AVDD_PLAT, AVDD_CGA1, AVDD_CGA2, and AVDD_D1 are measured at the input to the filter and not at the pin of the device. 6. TA_PROG_SFP must be supplied 1.8V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power Sequencing. 7. Transceiver supply for USB PHY. 8. **Caution:** The input voltage level of the signals must not exceed corresponding Max value. For example DDR4 must not exceed 5% of G1VDD. 9. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/Undershoot period should comply with JEDEC standards. 10. (G1, O, S, E)V_{IN}, USB_S*VIN and USB_HV_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in the Overshoot/undershoot voltage figure at the end of this section. 11. The Tj should not exceed 105°C. Proper thermal solution should be applied to meet this requirement.						

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 8. Overshoot/undershoot voltage for GnVDD/OVDD/EVDD/USB_HVDD/USB_S*VDD/SVDD

See the Recommended operating conditions table for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in the Recommended operating conditions table. The input voltage threshold scales with respect to the associated I/O supply voltage. EVDD and OVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D1_MVREF signal (nominally set to G1VDD/2) as is appropriate for the SSTL_1.35 electrical signaling standard and differential receivers referenced by the internally supplied reference signal as is appropriate for the JEDEC DDR4 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output drive capabilities

This chip provides information on the characteristics of the output driver strengths.

NOTE

These are estimated values.

Table 4. Output drive capability [2, 3]

Driver Type	Minimum [2]	Typ	Maximum [3]	Supply_Voltage	Notes
DDR4 signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.2V	1
DDR3L signal	-	18 (full-strength mode) 27 (half-strength mode)	-	$G1V_{DD}$ = 1.35V	1
SPI2/3, FlexSPI, Tamper_Detect, System control, GPIO1/2/3, I2C, eSDHC2, SDHC1_VSEL, Ethernet interface, Ethernet management interface (EMI), TSEC_1588, DUART, Debug, JTAG, POR signals, DFT, USB_PWRFAULT, USB_DRVVBUS, SAI3/4/5/6, Flextimer, CAN, LPUART	30	45	60	OV_{DD} = 1.8V	-
eSDHC1, SPI1, SAI1/2	45	65	90	EV_{DD} = 3.3V	-

1. The drive strength of the DDR4 interface in half-strength mode is at Tj = 105°C and at G1VDD (min).
2. Minimum values reflect estimated numbers based on best-case processed device.
3. Maximum values reflect estimated numbers based on worst-case processed device.

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

Step 1 -

- 1.8V: OV_{DD}, DP_OV_{DD}, AV_{DD}_PIXEL, TH_V_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1
- 3.3V: USB_HV_{DD}
- 1.8V/3.3V: EV_{DD}
  - Drive TA_PROG_SFP = GND
  - PORESET_B should be driven asserted and held during this step.

Step 2 -

- 1.0V / 0.9V: V_{DD}, SV_{DD}, DP_SV_{DD}, DP_AV_{DD}, $PIXEL_DV_{DD}$, USB_SDV_{DD}, USB_SV_{DD}, $TA_BB_V_{DD}$

Step 3-

- System with DDR3L memory (1.35V): $G1V_{DD}$, XV_{DD}, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2
- System with DDR4 memory (1.2V): $G1V_{DD}$ (XV_{DD}, AV_{DD}SD1_PLL1 and AV_{DD}_SD1_PLL2 can be powered up in any step)

Items on the same step have no ordering requirement with respect to one another. Items on separate steps must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time has been met per Table 13. RESET initialization timing specifications on page 75.

NOTE

- While V_{DD} is ramping up, current may be supplied from V_{DD} through LS1028A to $G1V_{DD}$.
- The 3.3V (USB_HV_{DD}) in Step 1 and 1.0V/0.9V (USB_SDV_{DD}, USB_SV_{DD}) in Step 2 supplies should ramp up within 95ms with respect to each other.
- 100us minimum spacing is required between Step 1 (DP_OV_{DD}) and Step2 (DP_SV_{DD}, DP_AV_{DD}) supplies.
- If Trust Architecture Security Monitor battery backed feature is not used, $TA_BB_V_{DD}$ should be connected with V_{DD}.
- If using Trust Architecture Security Monitor battery backed features, prior to VDD ramping up to the 0.5 V level, ensure that SVDD is ramped to recommended operational voltage and DIFF_SYSCLK_P/ DIFF_SYSCLK_N is running. These clocks should have a minimum frequency of 800 Hz and a maximum frequency not greater than the supported system clock frequency for the device.
- Ramp rate requirements should be met per Table 9. Power supply ramp rate on page 72.
- While XVDD is ramping, current may be supplied from XVDD through chip to SVDD.

Differential System clock should meet DC and AC Specifications as per Differential system clock DC electrical characteristics on page 73 and Differential system clock AC timing specifications on page 73 respectively.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

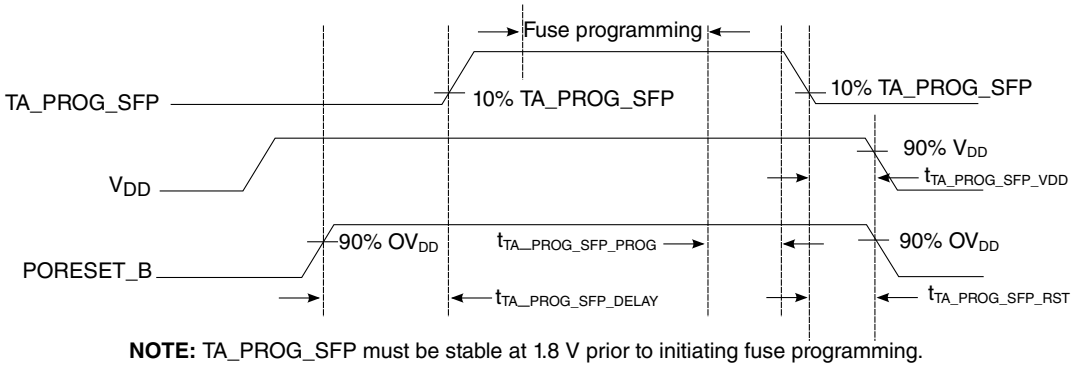
For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive TA_PROG_SFP = 1.8 V after a required minimum delay per Table 5. TA_PROG_SFP timing 5 on page 70.
2. After fuse programming is complete, it is required to return TA_PROG_SFP = GND before the system is power cycled or powered down (V_{DD} ramp down) per the required timing specified in Table 5. TA_PROG_SFP timing 5 on page 70. See Security fuse processor on page 181 for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 9. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 5. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA_PROG_SFP_DELAY}$	10	—	SYSCLKs	1
$t_{TA_PROG_SFP_PROG}$	0	—	us	2
$t_{TA_PROG_SFP_VDD}$	0	—	us	3
$t_{TA_PROG_SFP_RST}$	0	—	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

3. Delay required from TA_PROG_SFP ramp-down complete to V_{DD} ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} reaches 90% V_{DD}.

4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only six secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that all power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing on page 68, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5. TA_PROG_SFP timing 5 on page 70.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.4 Power characteristics

This table shows the thermal power dissipation of the V_{DD} power supply for A72 core/platform/DDR frequency combinations.

Table 6. LS1028A VDD power dissipation for the thermal design at 85^{0}C

Core frequency (MHz)	Platform frequency(MHz)	DDR data rate (MT/s)	GPU and LCD controller frequency (MHz)	V_{DD} (V)	IOV_{DD}[4] (V)	Power (W)		Total Core and Platform Power (W)	Notes
						V_{DD} (W)	IOV_{DD} (W)		
1500	400	1600	700	1.0	1.0	6.25	1.9	8.15	1, 2, 3
1300	400	1600	650	1.0	1.0	5.90	1.9	7.80	1, 2, 3
1000	400	1600	500	1.0	1.0	4.35	1.9	6.25	1, 2, 3
800	300	1300	400	0.9	0.9	2.7	1.8	4.5	1, 2, 3

Notes:

1. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.

2. Thermal power are based on worst-case processed device.

3. Refer to AN12028 "QorIQ LS1028A Design Checklist":

"Maximum VDD Power and IO Power" shows the maximum power dissipation across junction temperature range. This should be used as guide for power supply design and regulator sizing.

"Thermal Power" shows the thermal power across junction temperature range. This data should be used thermal solution design.

4. IOV_{DD} includes SV_{DD}, USB_SDV_{DD}, USB_SV_{DD}, $PIXEL_DV_{DD}$, DP_SV_{DD} and DP_AV_{DD}

Table 7. LS1018A VDD power dissipation for the thermal design at 85^{0}C

Core frequency (MHz)	Platform frequency(MHz)	DDR data rate (MT/s)	GPU and LCD controller frequency (MHz)	V_{DD} (V)	IOV_{DD}[4] (V)	Power (W)		Total Core and Platform Power (W)	Notes
						V_{DD} (W)	IOV_{DD} (W)		
1500	400	1600	700	1.0	1.0	5.25	1.9	7.15	1, 2, 3
1300	400	1600	650	1.0	1.0	5.10	1.9	7.0	1, 2, 3
1000	400	1600	500	1.0	1.0	3.65	1.9	5.55	1, 2, 3

Table continues on the next page...

Table 7. LS1018A VDD power dissipation for the thermal design at 85^{0}C (continued)

Core frequency (MHz)	Platform frequenc y(MHz)	DDR data rate (MT/s)	GPU and LCD controller frequency (MHz)	V_{DD} (V)	IOV_{DD}[4] (V)	Power (W)		Total Core and Platform Power (W)	Notes
						V_{DD} (W)	IOV_{DD} (W)		
800	300	1300	400	0.9	0.9	2.3	1.8	4.1	1, 2, 3

Notes:

1. Thermal power assumes Dhrystone running with activity factor of 90% on core and executing DMA on the platform at 100% activity factor.

2. Thermal power are based on worst-case processed device.

3. Refer to AN12028 "QorIQ LS1028A Design Checklist":

"Maximum VDD Power and IO Power" shows the maximum power dissipation across junction temperature range. This should be used as guide for power supply design and regulator sizing.

"Thermal Power" shows the thermal power across junction temperature range. This data should be used thermal solution design.

4. IOV_{DD} includes SV_{DD}, USB_SDV_{DD}, USB_SV_{DD}, $PIXEL_DV_{DD}$, DP_SV_{DD} and DP_AV_{DD}

This table shows the estimated power dissipation on the TA_BB_VDD supply at allowable voltage levels.

Table 8. TA_BB_VDD power dissipation

Supply	Maximum	Unit	Notes
TA_BB_VDD (SoC off, 40°C)	40	µW	1
TA_BB_VDD (SoC off, 70°C)	55	µW	1

Note: 1. When SoC is off, TA_BB_VDD may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_VDD to battery when SoC is powered down. See the Device reference manual trust architecture chapter for more information.

3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 9. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/$G1V_{DD}$/SV_{DD}/XV_{DD}/ EV_{DD}/$PIXEL_DV_{DD}$, all core and platform V_{DD} supplies and all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for TA_PROG_SFP	—	25	V/ms	1, 2
Required ramp rate for USB_HV_{DD}	—	26.7	V/ms	1, 2

Table continues on the next page...

Table 9. Power supply ramp rate (continued)

Parameter	Min	Max	Unit	Notes
Maximum ramp time for DP_AV_{DD}, DP_SV_{DD}	—	8	V/ms	3
Maximum ramp time for DP_OV_{DD}	—	16	V/ms	3

Notes:

1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Recommended Operating Conditions).
3. From 10% to 90%

3.6 Input clocks

3.6.1 Differential system clock (DIFF_SYSCLK_P/DIFF_SYSCLK_N) timing specifications

The differential system clocking mode requires an on-board oscillator to provide reference clock input to the differential system clock pair (DIFF_SYSCLK_P/DIFF_SYSCLK_N).

This differential clock pair can be configured to provide the clock to core, platform, and USB PLLs.

This figure shows a receiver reference diagram of the differential system clock.

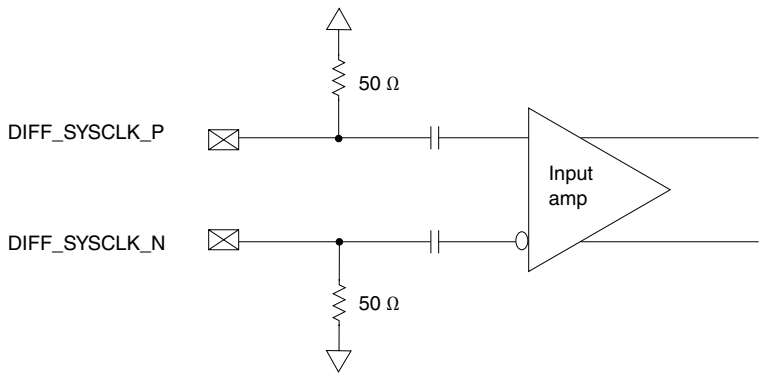


Figure 10. HCSL receiver

This section provides the differential system clock DC and AC timing specifications.

3.6.1.1 Differential system clock DC electrical characteristics

For DC electrical characteristics, see DC-level requirement for SerDes reference clocks on page 126.

The differential system clock receiver's core power supply voltage requirements are specified in Recommended Operating Conditions.

3.6.1.2 Differential system clock AC timing specifications

The DIFF_SYSCLK_P/DIFF_SYSCLK_N input pair supports an input clock frequency of 100 MHz.

For AC timing specifications, see SerDes reference clocks AC timing specifications on page 128.

Spread-spectrum clocking is not supported on differential system clock pair input.

3.6.2 USB reference clock specifications

The reference clock of the USB PHY is the DIFF_SYSCLK_P/DIFF_SYSCLK_N.

Table 10. USB AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency	f_{SYSCLK}	-	100	-	MHz	-
Reference clock frequency-offset	F_{REF_OFFSET}	-300.0	-	300.0	ppm	-
Reference clock random jitter (RMS)	$JRMS_{REF_CLK}$	-	-	3.0	ps	1, 2
Reference clock cycle-to-cycle jitter	DJ_{REF_CLK}		-	150.0	ps	3
Reference clock duty cycle	t_{KHK}/t_{SYSCLK}	40	-	60	%	-

1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.
2. The peak-to-peak Rj specification is calculated at 14.069 times the RJ_{RMS} for 10^{-12} BER.
3. DJ across all frequencies.

3.6.3 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with OV_{DD} = 1.8 V.

Table 11. EC_GTX_CLK125 DC electrical characteristics (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	—	—	V	2
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Recommended Operating Conditions.
3. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended Operating Conditions.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 12. EC_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}		8		ns	—
EC_GTX_CLK125 rise and fall time OV_{DD} = 1.8 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3

Notes:

1. At recommended operating conditions with OV_{DD} = 1.8 V ± 90mV. See Recommended Operating Conditions.

2. Rise times are measured from 20% of OVDD to 80% of OVDD. Fall times are measured from 80% of OVDD to 20% of OVDD.

3. EC_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter.See RGMII AC timing specifications on page 102 for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.6.4 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, see the specific interface section.

3.7 Reset initialization timing specifications

This table provides the RESET initialization timing specifications.

Table 13. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of PORESET_B after all supply rails are stable	1.0	-	ms	1
Required input assertion time of HRESET_B	32.0	-	SYSCLK	2, 3, 7
Maximum rise/fall time of PORESET_B	-	1.0	SYSCLK	4,6
Maximum rise/fall time of HRESET_B	-	10	SYSCLK	4,5
Input setup time for POR configs with respect to negation of PORESET_B	4.0	-	SYSCLK	2
Input hold time for all POR configs with respect to negation of PORESET_B	2.0	-	SYSCLK	2

Table continues on the next page...

Table 13. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5.0	SYSCLK	2

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

2. DIFF_SYSCLK_P/DIFF_SYSCLK_N is the primary clock input for the chip.

3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.

4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

5. For HRESET_B the rise/fall time should not exceed 10 SYSCLKs. Rise time refers to signal transitions from 20% to 70% of OVDD. Fall time refers to transitions from 70% to 20% of OVDD.

6. For PORESET_B the rise/fall time should not exceed 1 SYSCLK. Rise time refers to signal transitions from 20% to 70% of OVDD. Fall time refers to transitions from 70% to 20% of OVDD.

7. See General A-050124 erratum.

3.8 Controller Automatic Network interface (CAN)

3.8.1 CAN DC electrical chracteristics

This table provides the DC electrical characteristics for CAN-FD.

Table 14. DC electrical characteristics for CAN-FD (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (VIN = 0 V or VIN= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, IOH= -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, IOH= -0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.8.2 CAN AC electrical characteristics

This table provides the CAN-FD AC timing specifications.

Table 15. CAN-FD AC timing specifications [1]

Parameter	Min	Max	Unit
Baud rate	10.0	8000.0	kbps
1. See Figure 11. on page 77.			

This figure provides the CAN-FD AC test load.

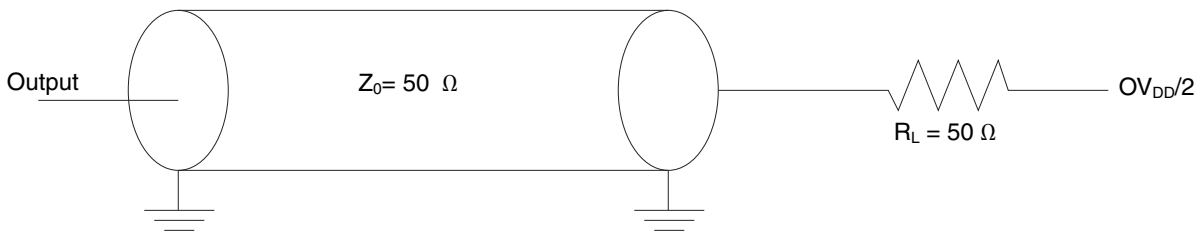


Figure 11. FlexCAN AC test load

3.9 DDR3L and DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3L and DDR4 SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM, and the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.9.1 DDR3L and DDR4 SDRAM controller DC electrical characteristics

This table provides the recommended opearting conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 16. DDR3L SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.35V) [1, 9]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
I/O reference voltage	MVREFn	0.49 * $G1V_{DD}$	0.5 * $G1V_{DD}$	0.51 * $G1V_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	MVREFn + 0.090	-	$G1V_{DD}$	V	5
Input low voltage	V_{IL}	GND	-	MVREFn - 0.090	V	5
I/O leakage current	I_{OZ}	-200.0	-	200.0	µA	6
I/O leakage current at 0.9V VDD and 125^0C	I_{OZ}	-275.0	-	275.0	µA	6

Table continues on the next page...

Table 16. DDR3L SDRAM interface DC electrical characteristics (G1V $_{DD}$ = 1.35V) [1, 9] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high current (V_{OUT} = 0.641 V)	I_{OH}	-	-	-23.3	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	-	-	mA	7, 8

1. For recommended operating conditions, see Recommended Operating Conditions.

2. MVREFn is expected to be equal to 0.5 x $G1V_{DD}$ and to track $G1V_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ± 1% of $G1V_{DD}$ (i.e. ± 13.5 mV).

3. V_{TT} is not applied directly to the device. It is the supply to which fare end signal termination is made, and it is expected to be equal to MVREFn with a min value of MVREFn - 0.04 and a max value of MVREFn + 0.04. V_{TT} should track variations in the DC level of MVREFn.

4. The voltage regulator for MVREFn must meet the specification stated in Table 17. Current draw characteristics for MVREFn (G1V DD = 1.35V) 1 on page 78.

5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.

6. Refer to IBIS model for the complete output IV curve characteristics.

7. IOH and IOL are measured at $G1V_{DD}$ = 1.282V

8. Output leakage is measured with all outputs diabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$

9. $G1V_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.

This tables provides the current draw characteristics for MVREFn.

Table 17. Current draw characteristics for MVREFn (G1V $_{DD}$ = 1.35V) [1]

Parameter	Symbol	Min	Max	Unit
Current draw for MVREFn	I_{MVREFn}	-	500.0	µA

1. For recommended operating conditions, see Recommended Operating Conditions.

This table provides the recommended opearting conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 18. DDR4 SDRAM interface DC electrical characteristics (G1V $_{DD}$ = 1.2V) [1, 7]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * $G1V_{DD}$ + 0.175	-	V	2, 3
Input low voltage	V_{IL}	-	0.7 * $G1V_{DD}$ - 0.175	V	2, 3
I/O leakage current	I_{OZ}	-200.0	200.0	µA	4
I/O leakage current at 0.9V VDD and 125^{0}C	I_{OZ}	-275.0	275.0	µA	6

Table continues on the next page...

Table 18. DDR4 SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.2V) [1, 7] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high current (V_{OUT} = 0.641 V)	I_{OH}	-	-20.7	mA	5, 6
Output low current (V_{OUT} = 0.641 V)	I_{OL}	20.7	-	mA	5, 6

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.

3. Internal Vref for data bus must be set to 0.7 x $G1V_{DD}$

4. Refer to IBIS model for the complete output IV curve characteristics.

5. IOH and IOL are measured at $G1V_{DD}$ = 1.14V

6. Output leakage is measured with all outputs diabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$

7. $G1V_{DD}$ is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source. $G1V_{DD}$ min = 1.14 V, $G1V_{DD}$ max = 1.26 V, and $G1V_{DD}$ typ = 1.2 V.

3.9.2 DDR3L and DDR4 SDRAM controller AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 19. DDR4 SDRAM interface input AC timing specifications

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{ILAC}	-	0.7 * $G1V_{DD}$ - 0.175	V
AC input high voltage	V_{IHAC}	0.7 * $G1V_{DD}$ + 0.175	-	V

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 20. DDR3L SDRAM interface input AC timing specifications [1]

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{ILAC}	-	MVREFn-0.135	V
AC input high voltage	V_{IHAC}	MVREFn+0.135	-	V

1. See Figure 12. on page 83.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM interface input AC timing specifications [3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		-125.0	125.0		1

Table continues on the next page...

Table 21. DDR3L SDRAM interface input AC timing specifications [3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Data Rate of 1600 MT/s in DDR3L		-112.0	112.0		1
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		-250.0	250.0		2
Data Rate of 1600 MT/s in DDR3L		-200.0	200.0		2

1. t_{CISKEW} represents the amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/-(T / 4 - abs(t_{CISKEW})), where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. See Figure 12. on page 83.

This table contains the output AC timing targets for the DDR3L SDRAM interface.

Table 22. DDR3L SDRAM interface output AC timing specifications [6]

Parameter	Symbol	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1250.0	2000.0	ps	1
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		606.0	-		2
Data Rate of 1600 MT/s in DDR3L		495.0	-		2
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		606.0	-		2
Data Rate of 1600 MT/s in DDR3L		495.0	-		2
MCK to MDQS Skew	t_{DDKNMH}	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		-245.0	245.0		3, 4
Data Rate of 1600 MT/s in DDR3L		-150.0	150.0		3, 4
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	-	-	ps	-
Data Rate of 1300 MT/s in DDR3L		500.0	-		5
Data Rate of 1600 MT/s in DDR3L		400.0	-		5

Table continues on the next page...

Table 22. DDR3L SDRAM interface output AC timing specifications [6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
MDQS preamble	t_{DDKHMP}	0.9 * t_{MCK}	-	ps	-
MDQS postamble	t_{DDKHME}	0.4 * t_{MCK}	0.6 * t_{MCK}	ps	-

1. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

2. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, and MDQ/MECC/MDM/MDQS/MDQS_B.

3. Note that tDDKHMH follows the symbol conventions described above. For example, tDDKHMH describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). The timing parameters listed in this table assume that the MCK and MDQS signals are programmed to launch from the controller using the same adjustment value.

4. Note that it is required to program the start value of the DQS adjust for write leveling.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. See Figure 13. on page 83.

NOTE

For the ADDR/CMD setup and hold specifications in Table 22. DDR3L SDRAM interface output AC timing specifications 6 on page 80, it is assumed that the clock control register is set to adjust the memory clockes by 1/2 applied cycle .

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 23. DDR4 SDRAM interface input AC timing specifications [3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-125.0	125.0		1
Data Rate of 1600 MT/s in DDR4		-112.0	112.0		1
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		-250.0	250.0		2
Data Rate of 1600 MT/s in DDR4		-200.0	200.0		2

1. t_{CISKEW} represents the amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = +/-(T / 4 - abs(t_{CISKEW})), where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

3. See Figure 12. on page 83.

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 24. DDR4 SDRAM interface output AC timing specifications [6]

Parameter	Symbol	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1250.0	1538.0	ps	1
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		2
Data Rate of 1600 MT/s in DDR4		495.0	-		2
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		606.0	-		2
Data Rate of 1600 MT/s in DDR4		495.0	-		2
MCK to MDQS Skew	t_{DDKNMH}	-245.0	245.0	ps	3, 4
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	-	-	ps	-
Data Rate of 1300 MT/s in DDR4		500.0	-		5
Data Rate of 1600 MT/s in DDR4		400.0	-		5
MDQS preamble	t_{DDKHMP}	0.9 * t_{MCK}	-	ps	-
MDQS postamble	t_{DDKHME}	0.4 * t_{MCK}	0.6 * t_{MCK}	ps	-

1. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

2. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, and MDQ/MECC/MDM/MDQS/MDQS_B.

3. Note that tDDKHMH follows the symbol conventions described above. For example, tDDKHMH describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). The timing parameters listed in this table assume that the MCK and MDQS signals are programmed to launch from the controller using the same adjustment value.

4. Note that it is required to program the start value of the DQS adjust for write leveling.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. See Figure 13. on page 83.

NOTE

For the ADDR/CMD setup and hold specifications in Table 24. DDR4 SDRAM interface output AC timing specifications 6 on page 82, it is assumed that the clock control register is set to adjust the memory clockes by 1/2 applied cycle .

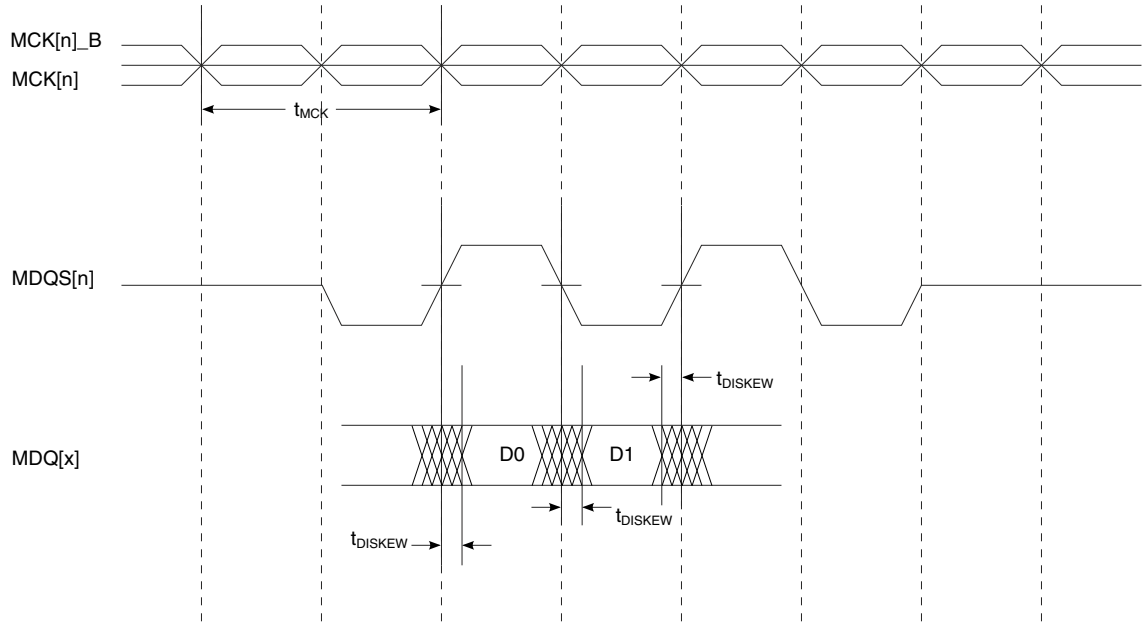


Figure 12. DDR4 SDRAM interface input timing diagram

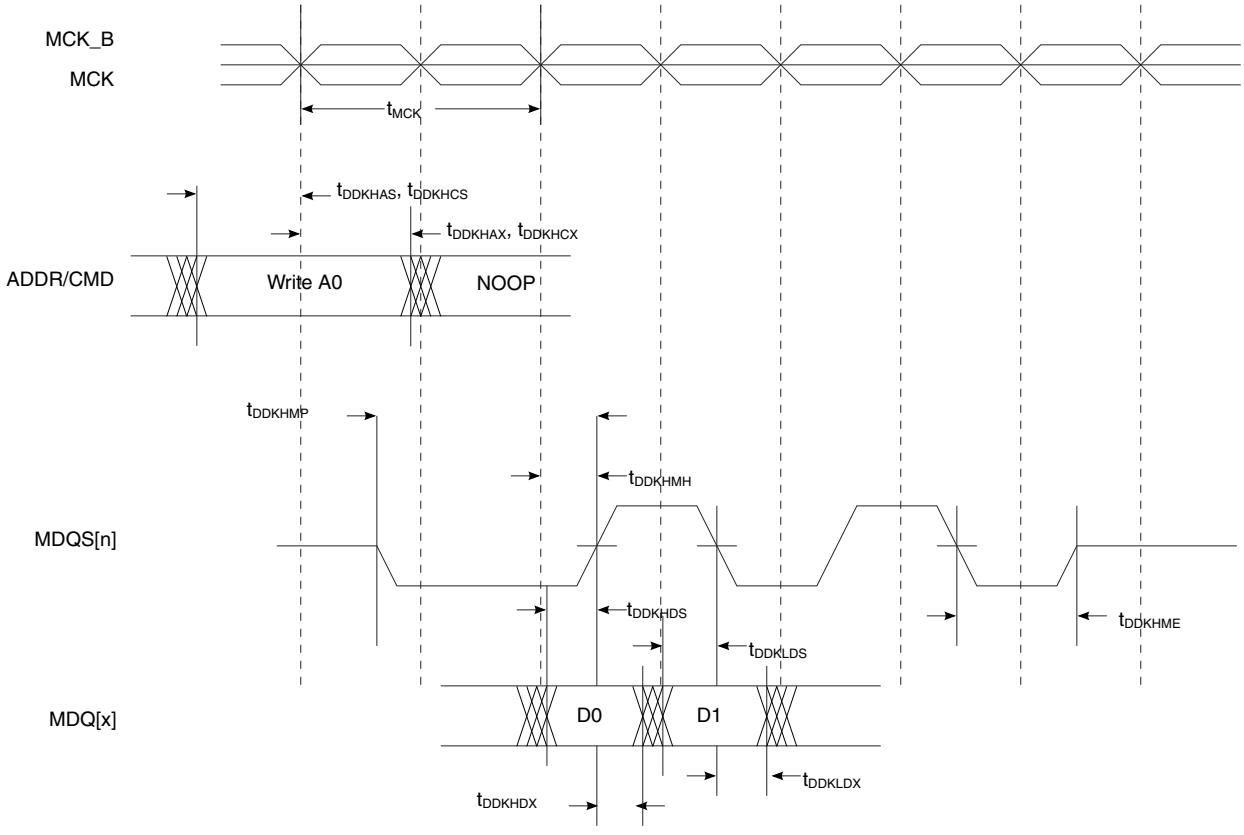


Figure 13. DDR4 SDRAM interface output timing diagram

3.10 Enhanced secure digital host controller (eSDHC)

This table provides the DC electrical characteristics for the eSDHC interface. This device has two eSDHC interfaces. Out of the two, eSDHC2 supports only 1.8 V voltage levels.

3.10.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 25. eSDHC DC electrical characteristics (EV_{DD} = 3.3V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.25 x EV_{DD}	V	2
Input/output leakage current	I_{IN}/I_{OZ}	-	±50	μA	-
Output high voltage (I_{OH} = -100μA at EV_{DD} min)	V_{OH}	0.75 x EV_{DD}	-	V	-
Output low voltage (I_{OL} = 100μA at EV_{DD} min)	V_{OL}	-	0.125 x EV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN} values found in Recommended Operating Conditions.

This table provides the DC electrical characteristics for the eSDHC interface.

Table 26. eSDHC DC electrical characteristics (EV_{DD}/OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}/OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x EV_{DD}/OV_{DD}	V	2
Input/output leakage current	I_{IN}/I_{OZ}	-	±50	μA	-
Output high voltage (I_{OH} = -2mA at EV_{DD}/OV_{DD} min)	V_{OH}	EV_{DD}/OV_{DD} - 0.45	-	V	-
Output low voltage (I_{OL} = 2mA at EV_{DD}/OV_{DD} min)	V_{OL}	-	0.45	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN}/OV_{IN} values found in Recommended Operating Conditions.

3.10.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 27. eSDHC AC timing specifications (full-speed mode) [1, 3, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO mode	f_{SHSCK}	-	-	MHz	-
SD/SDIO full-speed mode		0.0	25.0		1, 2, 3
eMMC full-speed mode		0.0	26.0		1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	10.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	10.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall).

2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an eMMC device.

3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.

4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed eMMC . For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.

5. See Figure 14. on page 86.

6. The AC timing specifications are based on the recommended operating conditions with EVDD =3.3V and OVDD=1.8V, see Recommended Operating Conditions

This figure provides the eSDHC clock input timing diagram as shown here.

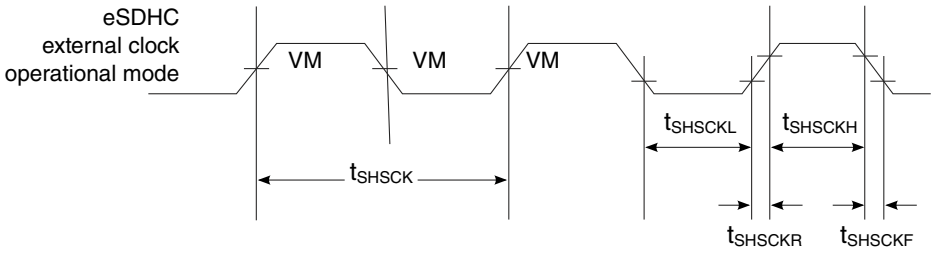


Figure 14. eSDHC clock input timing diagram

This table provides the eSDHC AC timing specifications as defined in the eSDHC clock input timing diagram.

Table 28. eSDHC AC timing specifications (high-speed mode) [1, 3, 5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency SD/SDIO mode	f_{SHSCK}	-	-	MHz	-
SD/SDIO high-speed mode		0.0	50.0		1, 2, 3
eMMC high-speed mode		0.0	52.0		1, 2, 3
SDHC_CLK clock low time	t_{SHSCKL}	7.0	-	ns	3
SDHC_CLK clock high time	t_{SHSCKH}	7.0	-	ns	3
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3.0	ns	3
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIVKH}$	2.5	-	ns	3, 4
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK)	$t_{SHSIXKH}$	2.5	-	ns	3
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	-3.0	-	ns	3
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	3.0	ns	3

Table continues on the next page...

Table 28. eSDHC AC timing specifications (high-speed mode) [1, 3, 5, 6, 7] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall). 2. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an MMC card. 3. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF. 4. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed eMMC . For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns. 5. See Figure 15. on page 87. 6. See Figure 16. on page 88. 7. The AC timing specifications are based on the recommended operating conditions with EVDD =3.3V and OVDD=1.8V, see Recommended Operating Conditions					

This figure provides the input AC timing diagram for high-speed mode.

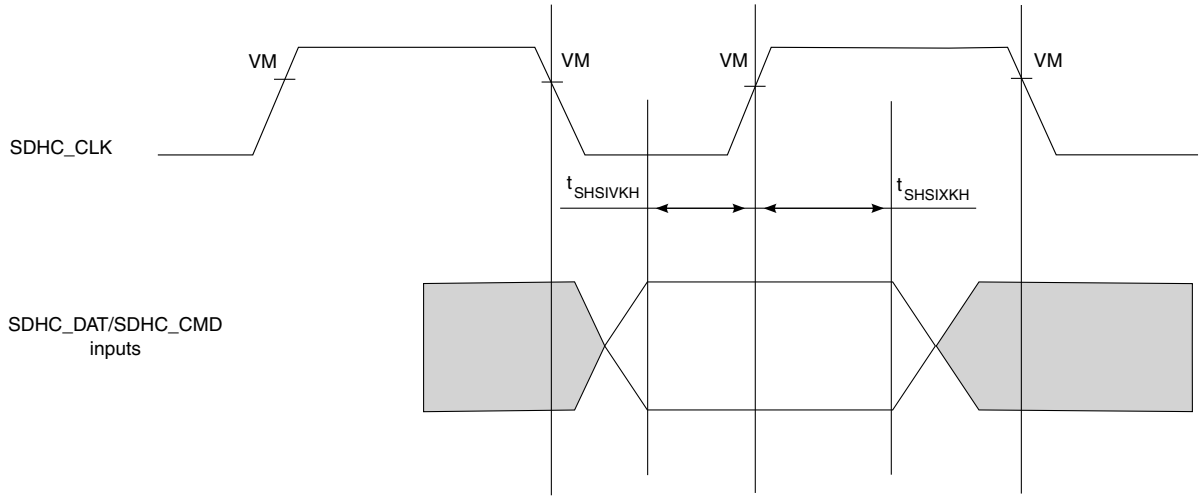
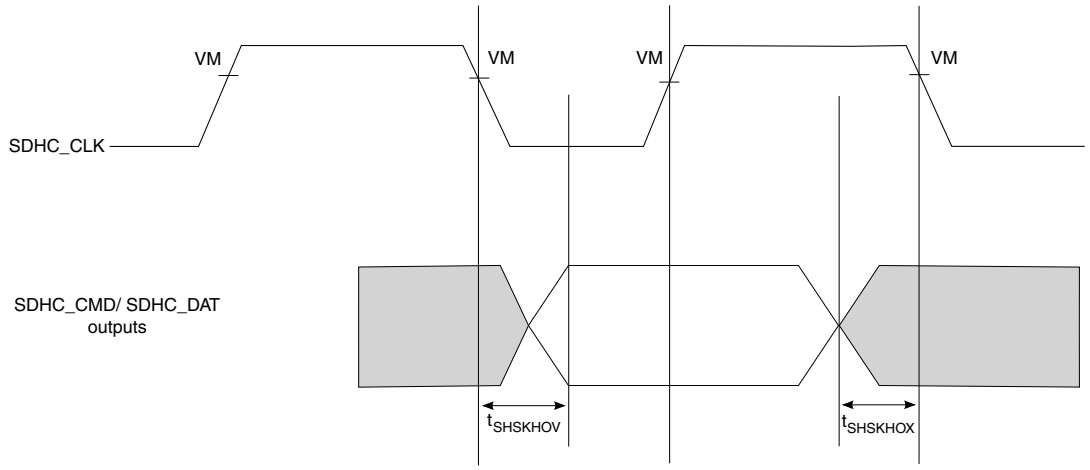


Figure 15. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.



VM = Midpoint Voltage (Respective supply / 2)

Figure 16. eSDHC high-speed mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR50 mode on devices without a voltage translator.

Table 29. eSDHC AC timing specifications (SDR50 mode without voltage translator) [2, 3, 4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHSCK}	0.0	100.0	MHz	-
SDHC_CLK rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	2.0	ns	1
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSKEW}	-0.1	0.1	ns	1
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
Input setup times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHSIVKH}$	2.1	-	ns	1
Input hold times (SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHSIXKH}$	1.1	-	ns	1
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOX}$	1.7	-	ns	1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	$t_{SHSKHOV}$	-	6.1	ns	1

Table continues on the next page...

Table 29. eSDHC AC timing specifications (SDR50 mode without voltage translator) [2, 3, 4, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. C_{CARD} ≤ 10 pF, (1 card), and CL = C_{BUS} + C_{HOST} + C_{CARD} ≤ 30 pF. 2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall). 3. See Figure 17. on page 89. 4. See Figure 18. on page 90. 5. The AC timing specifications are based on the recommended operating conditions with EVDD /OVDD =1.8V, see Recommended Operating Conditions					

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

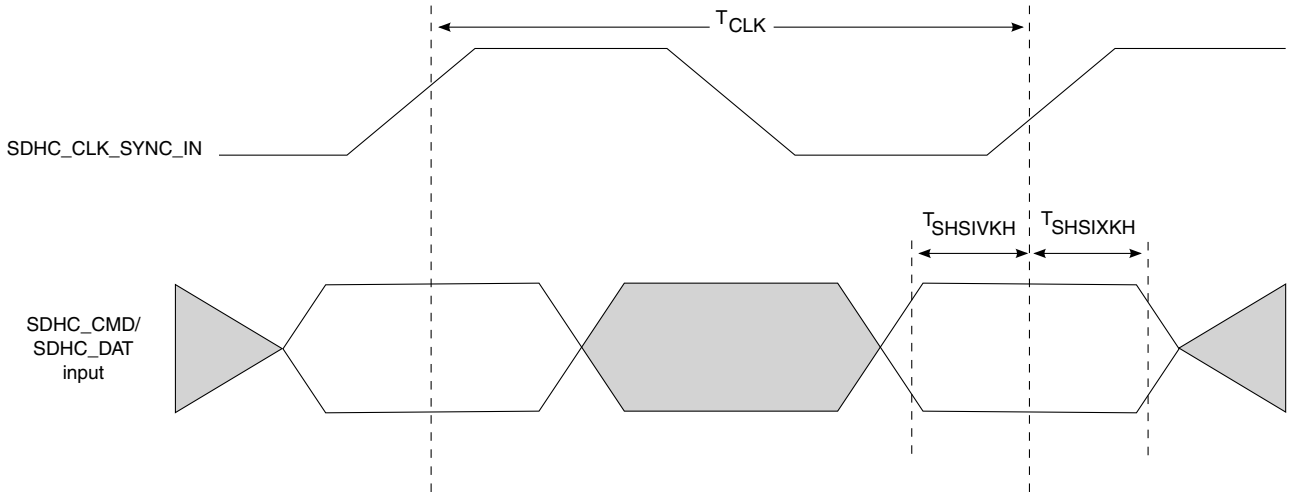


Figure 17. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

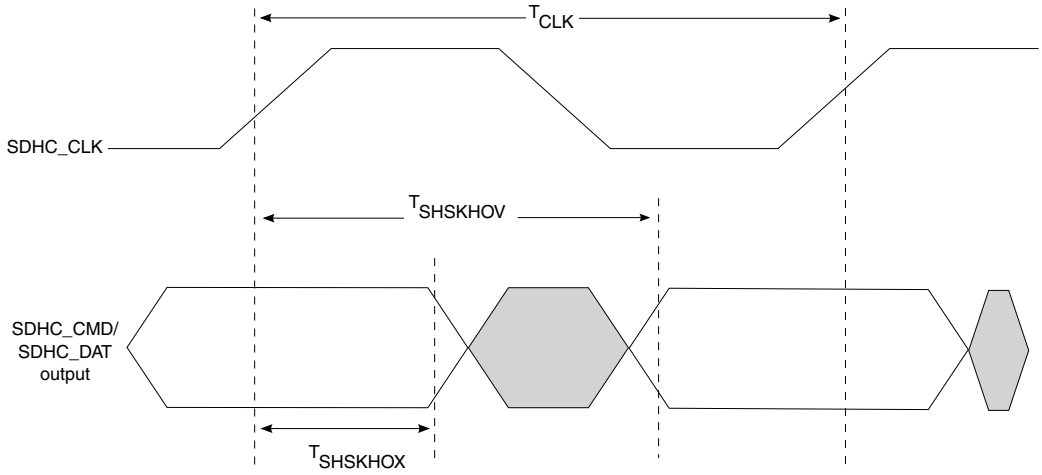


Figure 18. eSDHC SDR50 mode output timing diagram

This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 30. eSDHC AC timing specifications (DDR50/DDR mode without voltage translator) [3, 4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO DDR50 mode		-	45		1
eMMC DDR mode		-	45		2
SDHC_CLK duty cycle	t_{SHSCK}	47.0	53.0	%	-
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	t_{SHSKEW}	-0.65	0.65	ns	-
SDHC_CLK rise and fall times	t_{SHCKR}/ t_{SHCKF}	-	-	ns	-
SD/SDIO DDR50 mode		-	4.0		1
eMMC DDR mode		-	2.0		2
Input setup times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIVKH}$	-	-	ns	-
SD/SDIO DDR50 mode		2.7	-		1
eMMC DDR mode		2.7	-		2
Input hold times (SDHC_DATx to SDHC_CLK_SYNC_IN)	$t_{SHDIXKH}$	0.75	-	ns	1

Table continues on the next page...

Table 30. eSDHC AC timing specifications (DDR50/DDR mode without voltage translator) [3, 4, 5, 6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output hold time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOX}$	-	-	ns	-
SD/SDIO DDR50 mode		1.7	-		1
eMMC DDR mode		3.4	-		2
Output delay time (SDHC_CLK to SDHC_DATx valid)	$t_{SHDKHOV}$	-	-	ns	-
SD/SDIO DDR50 mode		-	7.3		1
eMMC DDR mode		-	7.75		2
Input setup time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIVKH}$	-	-	ns	-
SD/SDIO DDR50 mode		6.9	-		1
eMMC DDR mode		7.1	-		2
Input hold time (SDHC_CMD to SDHC_CLK_SYNC_IN)	$t_{SHCIXKH}$	0.75	-	ns	1
Output hold time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOX}$	-	-	ns	-
SD/SDIO DDR50 mode		1.7	-		1
eMMC DDR mode		3.9	-		2
Output delay time (SDHC_CLK to SDHC_CMD valid)	$t_{SHCKHOV}$	-	-	ns	-
SD/SDIO DDR50 mode		-	15.3		1
eMMC DDR mode		-	18.0		2

Table continues on the next page...

Table 30. eSDHC AC timing specifications (DDR50/DDR mode without voltage translator) [3, 4, 5, 6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. C_{CARD} ≤ 10pF, (1 card). 2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20 pF for MMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50. 3. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall). 4. See Figure 19. on page 92. 5. See Figure 20. on page 93. 6. The AC timing specifications are based on the recommended operating conditions with EVDD /OVDD =1.8V and EVDD=3.3V, see Recommended Operating Conditions					

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

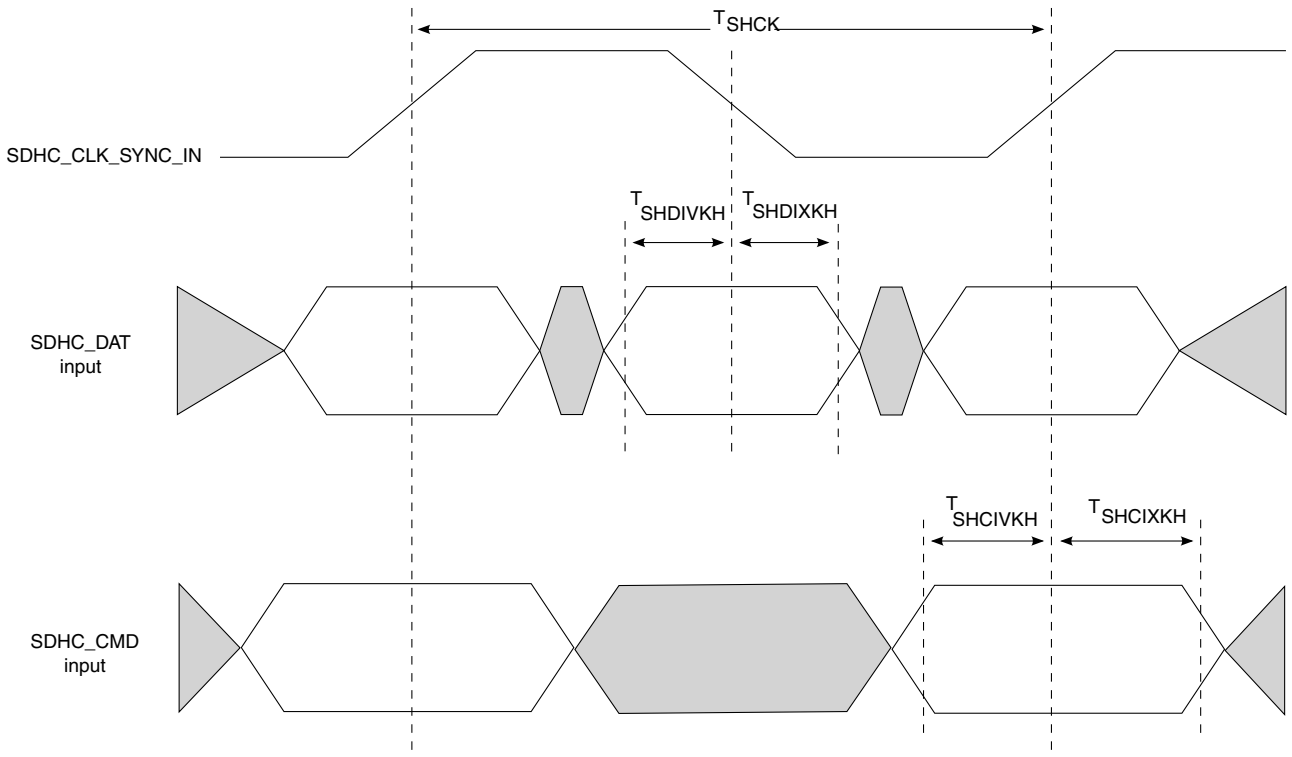


Figure 19. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

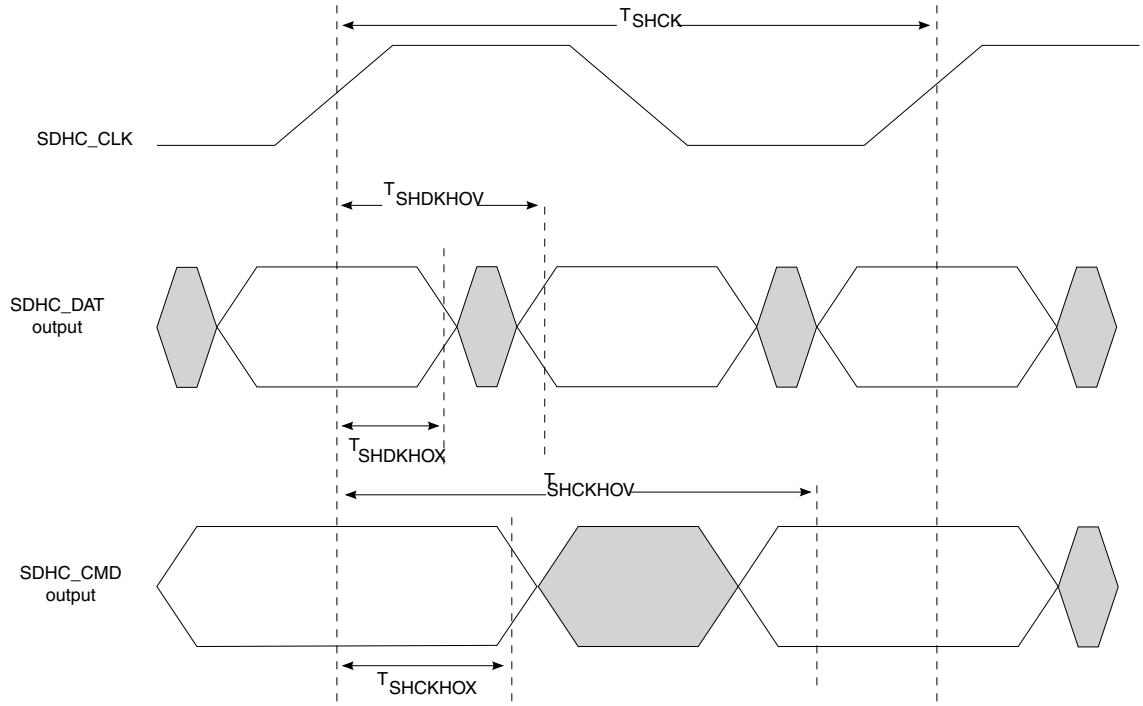


Figure 20. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode (VDD=1.0V)

Table 31. eSDHC AC timing specifications (SDR104/HS200 mode) (VDD=1.0V) [2, 3, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO SDR104 mode		-	200.0		-
eMMC HS200 mode		-	200.0		-
SDHC_CLK duty cycle	t_{SHSCK}	45	55	%	-
SDHC_CLK rise and fall times	t_{SHCKR}/ t_{SHCKF}	-	1.0	ns	1
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	-	-	ns	-
SD/SDIO SDR104 mode		1.58	-		1
eMMC HS200 mode		1.6	-		1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	-	ns	-
SD/SDIO SDR104 mode		-	2.9		1

Table continues on the next page...

Table 31. eSDHC AC timing specifications (SDR104/HS200 mode) (VDD=1.0V) [2, 3, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
eMMC HS200 mode		-	2.9		1
Input data window (UI)	t_{SHIDV}	-	-	Unit interval	-
SD/SDIO SDR104 mode		0.5	-		1
eMMC HS200 mode		0.475	-		1

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall).

3. See Figure 21. on page 96.

4. Board skew between clock and data pins should be less than 100ps

5. The AC timing specifications are based on the recommended operating conditions with EVDD /OVDD =1.8V, see Recommended Operating Conditions

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode (VDD=0.9V)

Table 32. eSDHC AC timing specifications (SDR104/HS200 mode)(VDD=0.9V) [2, 3, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO SDR104 mode		-	166.6		-
eMMC HS200 mode		-	166.6		-
SDHC_CLK duty cycle	t_{SHSCK}	45.0	55.0	%	-
SDHC_CLK rise and fall times	t_{SHCKR}/ t_{SHCKF}	-	1.0	ns	1
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	-	-	ns	-
SD/SDIO SDR104 mode		1.58	-		1
eMMC HS200 mode		1.6	-		1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	-	ns	-
SD/SDIO SDR104 mode		-	4.0		1

Table continues on the next page...

Table 32. eSDHC AC timing specifications (SDR104/HS200 mode)(VDD=0.9V) [2, 3, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
eMMC HS200 mode		-	4.0		1
Input data window (UI)	t_{SHIDV}	-	-	Unit interval	-
SD/SDIO SDR104 mode		0.5	-		1
eMMC HS200 mode		0.475	-		1

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall).

3. See Figure 21. on page 96.

4. Board skew between clock and data pins should be less than 100ps

5. The AC timing specifications are based on the recommended operating conditions with EVDD /OVDD =1.8V, see Recommended Operating Conditions

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

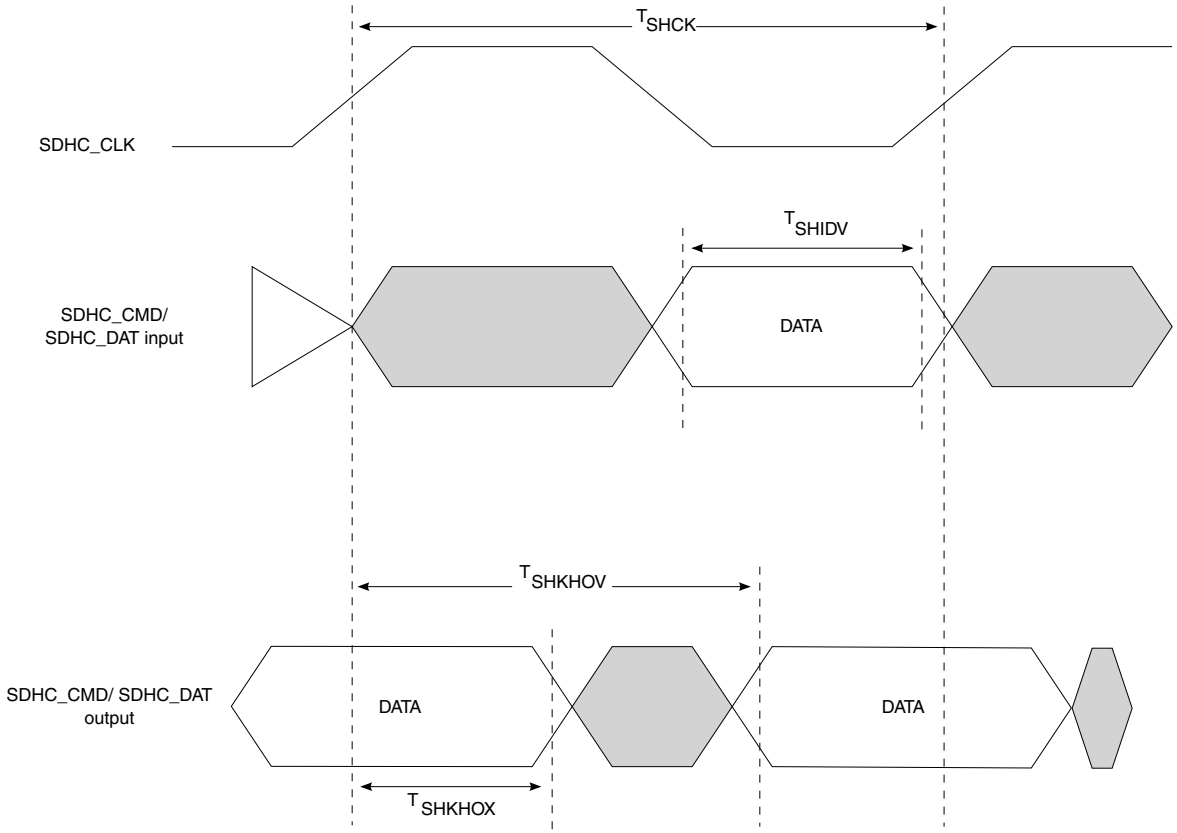


Figure 21. eSDHC SDR104/HS200 mode timing diagram

This table provides the eSDHC AC timing specifications for eMMC HS400 mode (VDD=1.0V).

Table 33. eSDHC AC timing specifications (HS400 mode) (VDD=1.0) [2, 3, 4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	150.0	MHz	-
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	0.75	-	ns	1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	2.58	ns	1
Data valid skew to DQS	T_{SHRQV}	-	0.45	ns	1
Data hold skew to DQS	T_{SHRQHX}	-	0.45	ns	1
Command valid skew to DQS	T_{SHRQV_CMD}	-	0.45	ns	1
Command hold skew to DQS	T_{SHRQHX_CMD}	-	0.45	ns	1

Table continues on the next page...

Table 33. eSDHC AC timing specifications (HS400 mode) (VDD=1.0) [2, 3, 4, 5, 6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
DQS pulse width	$T_{SHDSPWS}$	1.97	-	ns	1
Duty cycle distortion	t_{SHSCK_DIS}	0.0	0.3	ns	1

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.

2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall).

3. See Figure 22. on page 98.

4. See Figure 23. on page 99.

5. The AC timing specifications are based on the recommended operating conditions with OVDD =1.8V, see Recommended Operating Conditions

6. Supoorted on eSDHC2 interface only

This table provides the eSDHC AC timing specifications for eMMC HS400 mode (VDD=0.9V).

Table 34. eSDHC AC timing specifications (HS400 mode)(VDD=0.9V) [2, 3, 4, 5, 6]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK frequency	f_{SHCK}	-	125.0	MHz	-
Output hold time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOX}	0.75	-	ns	1
Output delay time (SDHC_CLK to SDHC_CMD, SDHC_DATx valid)	T_{SHKHOV}	-	3.25	ns	1
Data valid skew to DQS	T_{SHRQV}	-	0.45	ns	1
Data hold skew to DQS	T_{SHRQHX}	-	0.45	ns	1
Command valid skew to DQS	T_{SHRQV_CMD}	-	0.45	ns	1
Command hold skew to DQS	T_{SHRQHX_CMD}	-	0.45	ns	1
DQS pulse width	$T_{SHDSPWS}$	1.97	-	ns	1
Duty cycle distortion	t_{SHSCK_DIS}	0.0	0.3	ns	1

Table continues on the next page...

Table 34. eSDHC AC timing specifications (HS400 mode)(VDD=0.9V) [2, 3, 4, 5, 6] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.					
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC highspeed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (R for rise) or F (F for fall).					
3. See Figure 22. on page 98.					
4. See Figure 23. on page 99.					
5. The AC timing specifications are based on the recommended operating conditions with OVDD =1.8V, see Recommended Operating Conditions					
6. Supoorted on eSDHC2 interface only					

This figure provides the eSDHC HS400 mode input timing diagram.

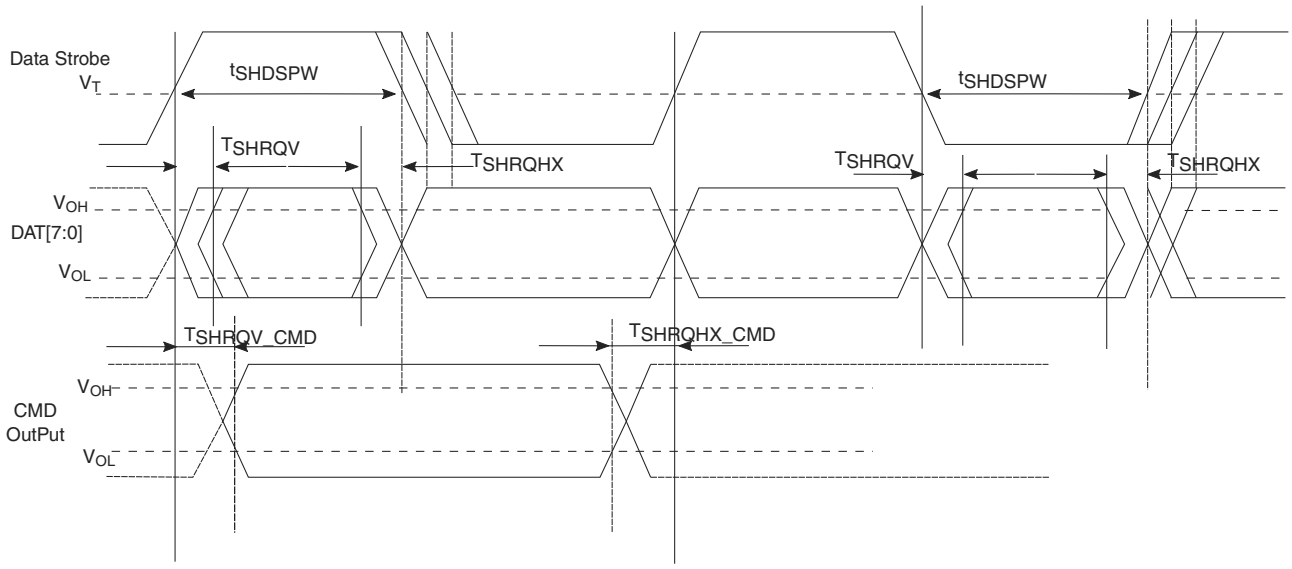


Figure 22. eSDHC HS400 mode input timing diagram

This figure provides the eSDHC HS400 mode output timing diagram.

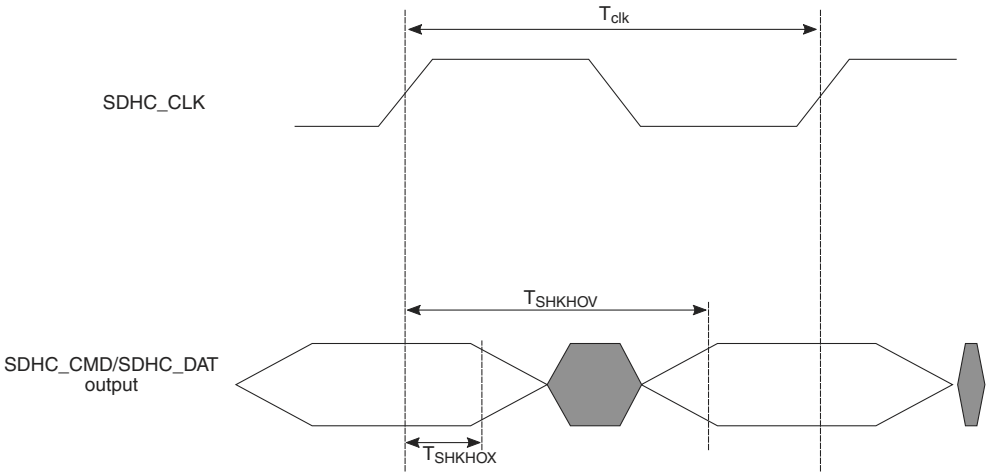


Figure 23. eSDHC HS400 mode output timing diagram

3.11 Ethernet interface (EMI, RGMII and IEEE Std 1588™)

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, and IEEE Std 1588 interfaces.

3.11.1 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet management interface (EMI) interface.

The EMI1 interface timings are compatible with IEEE Std 802.3™ clauses 22 and 45.

3.11.1.1 EMI DC electrical characteristics

This table provides the EMI1 DC electrical characteristics.

Table 35. EMI1 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 35. EMI1 DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.11.1.2 EMI AC timing specifications

This table provides the EMI1 AC timing specifications.

Table 36. EMI1 AC timing specifications [4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	-	2.5	MHz	1
MDC clock pulse width high	t_{MDCH}	160.0	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(Y x t_{enet_clk}) - 3	(Y x t_{enet_clk}) + 3	ns	2, 3, 4
MDIO to MDC setup time	t_{MDDVKH}	8.0	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	0.0	-	ns	-
1. This parameter is dependent on the Ethernet clock frequency. The EMDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EMI1_MDC. 2. t_{enet_clk} is the Ethernet clock period. 3. MDIO timing is configurable by programming EMDIO_CFG register fields. 4. The default value of Y is 5. Y value is determined by EMDIO_CFG[NEG], EMDIO_CFG[MDIO_HOLD] and EMDIO[EHOLD]. It is recommended to use EMDIO_CFG[NEG]=1 for MDIO transactions. 5. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time tMDC from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the tMDC clock reference (K) going to the high (H) state or setup time. 6. See Figure 24. on page 101.					

This figure shows the Ethernet management interface 1 timing diagram.

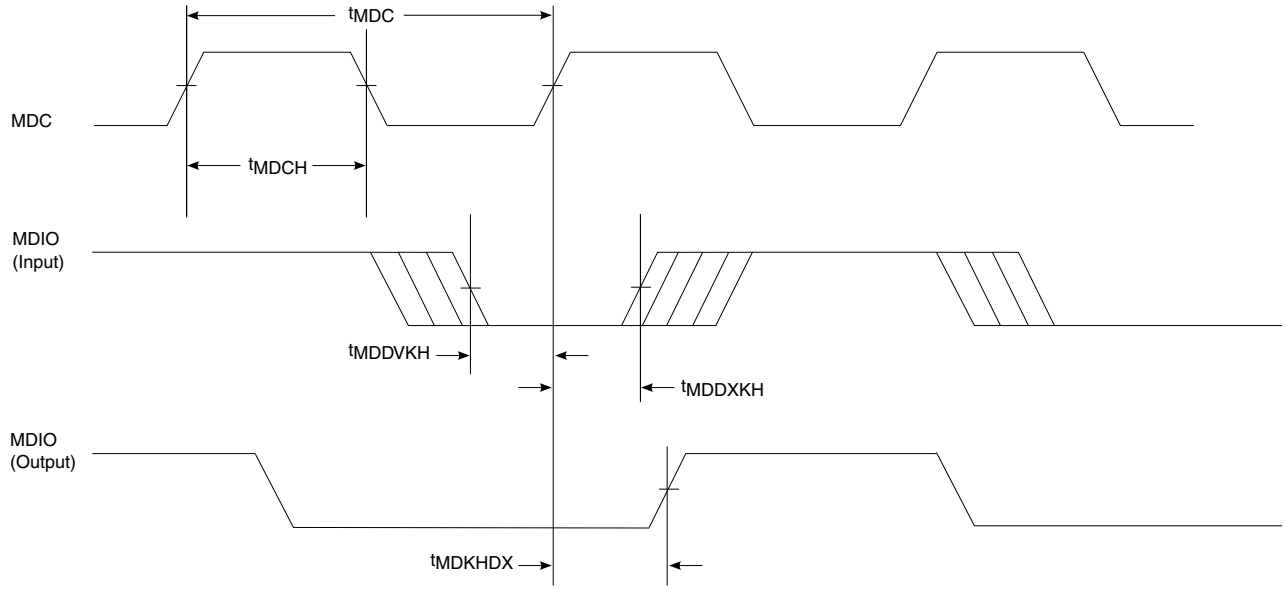


Figure 24. Ethernet management interface 1 timing diagram

3.11.2 Reduced media-independent interface (RGMII)

3.11.2.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface.

Table 37. RGMII DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN}=0 or V_{IN} = OV_{IN})	I_{IN}	-	±50	μA	3, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

4. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.11.2.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 38. RGMII AC timing specifications [8, 9]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500.0	0.0	500.0	ps	1
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2, 3
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/ t_{RGT}	40.0	50.0	60.0	%	4, 5
Duty cycle for Gigabit	t_{RGTH}/ t_{RGT}	45.0	50.0	55.0	%	-
Rise time (20%-80%)	t_{RGTR}	-	-	0.75	ns	6, 7
Fall time (20%-80%)	t_{RGTF}	-	-	0.75	ns	6, 7

1. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10/100 Mbps, the max value is unspecified.

4. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

5. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

6. Applies to inputs and outputs.

7. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

8. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

9. See Figure 25. on page 103.

This figure shows the RGMII AC timing and multiplexing diagrams.

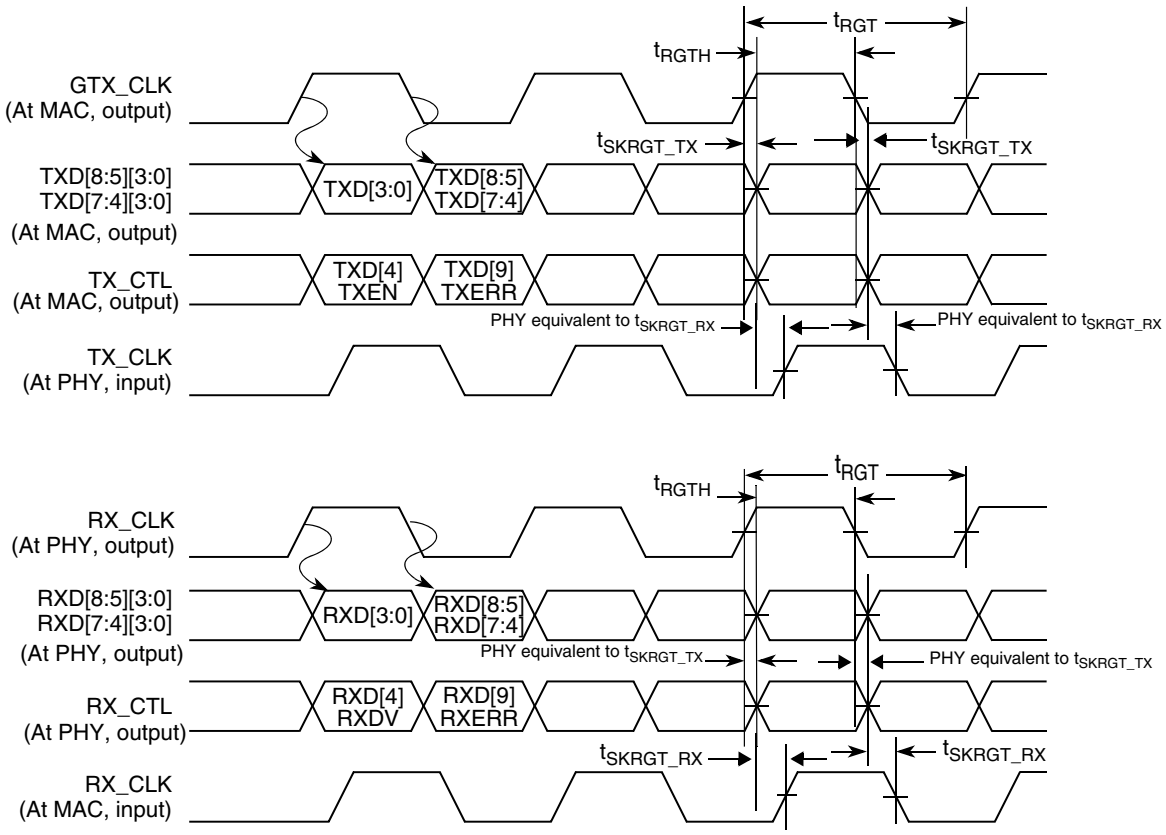


Figure 25. RGMII AC timing and multiplexing diagrams

3.11.3 IEEE 1588

3.11.3.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics.

Table 39. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 39. IEEE 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.11.3.2 IEEE 1588 AC timing specifications

This table provides the AC timing specifications for the IEEE 1588 interface.

Table 40. IEEE 1588 AC timing specifications [5, 6]

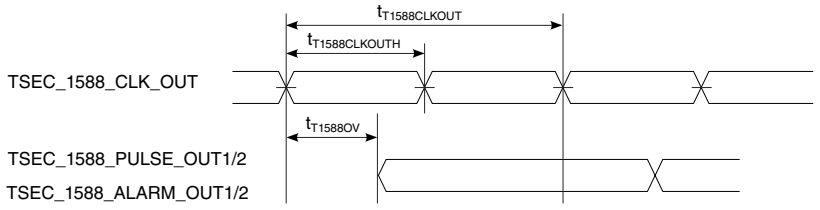
Parameter	Symbol	Min	Typ	Max	Unit	Notes
EC1_1588_CLK_IN clock period	$t_{1588CLK}$	5.0	-	T_{RX_CLK} x 7	ns	1, 2
EC1_1588_CLK_IN duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40.0	50.0	60.0	%	3
EC1_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	-	-	250.0	ps	-
Rise time EC1_1588_CLK_IN (20% to 80%)	$t_{T1588CLKINR}$	1.0	-	2.0	ns	-
Fall time EC1_1588_CLK_IN (80% to 20%)	$t_{T1588CLKINF}$	1.0	-	2.0	ns	-
EC1_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	-	-	ns	4
EC1_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30.0	50.0	70.0	%	-
EC1_1588_PULSE_OUT1/2, EC1_1588_ALARM_OUT1/2	$t_{T1588OV}$	0	-	4.0	ns	-
EC1_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{1588CLK_MAX}$	-	-	ns	1

Table continues on the next page...

Table 40. IEEE 1588 AC timing specifications [5, 6] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of tT1588CLK will be 2800, 280, and 56 ns, respectively. 2. T_{RX_CLK} is the maximum clock period of the ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers. 3. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers. 4. There are two input clock sources: TSEC_1588_CLK_IN and ENETC system clock. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$. 5. See Figure 26. on page 105. 6. See Figure 27. on page 105.						

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 26. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

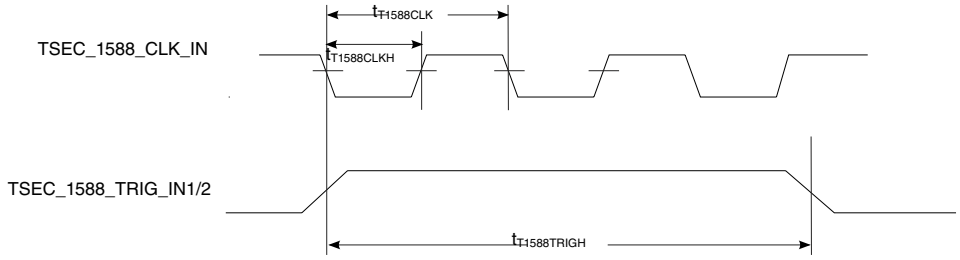


Figure 27. IEEE 1588 input AC timing

3.11.4 TSN SWITCH 1588

3.11.4.1 TSN SWITCH 1588 DC electrical characteristics

This table provides the SWITCH 1588 DC electrical characteristics.

Table 41. SWITCH 1588 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.11.4.2 TSN SWITCH 1588 AC timing specifications

This table provides the AC timing specifications for the SWITCH 1588 interface.

Table 42. SWITCH 1588 AC timing specifications

Parameter	Symbol	Min	Max	Unit
SWITCH_1588_DATn pulse width (configured as input)	$t_{S1588TRIG}$	6.4	-	ns

3.11.5 IEEE 1722

3.11.5.1 IEEE 1722 DC electrical characteristics

This table provides the IEEE 1722 DC electrical characteristics.

Table 43. IEEE 1722 DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0 or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 43. IEEE 1722 DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.11.5.2 IEEE 1722 AC timing specifications

This table provides the AC timing specifications for the IEEE 1722 interface.

Table 44. IEEE 1722 AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
EC1_1722_DATn pulse width (configured as input)	$t_{T1722TRIG}$	5.0	-	ns	Programmed through PTCMRa[TMODE]

3.12 Flex serial peripheral interface (FlexSPI)

3.12.1 FlexSPI DC electrical characteristics

This table provides the DC electrical characteristics for the FlexSPI interface.

Table 45. FlexSPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (0V ≤ V_{IN} ≤ OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -100 μA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OH} = 100 μA)	V_{OL}	-	0.15xOV_{DD}	V	-
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.12.2 FlexSPI AC timing specifications

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0

Table 46. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle distortion	T_{dis}	-0.5	0.5	ns	-
CS output hold time	$t_{FSKHOX2}$	(FLSHxCR1[TCSH]*T)- 0.54	-	ns	1
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5)*T) - 0.74	-	ns	1
Setup time for incoming data-without DQS	t_{FSIVKH}	2.4	-	ns	-
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

1. Refer Flash Control Register 1 (FLSHxyCR1) in QorIQ LS1028ARM for more details, where x: A or B, y: 1 or 2.
2. See Figure 29. on page 110.
3. See Figure 30. on page 111.
4. See Figure 31. on page 111.

This table provides the FlexSPI timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2

Table 47. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2 [2, 3, 4]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	100.0	MHz	-
Duty cycle distortion	T_{dis}	-0.5	0.5	ns	-
CS output hold time	$t_{FSKHOX2}$	(FLSHxCR1[TCSH]*T) - 0.54	-	ns	1
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5)*T) - 0.74	-	ns	1
Setup time for incoming data-without DQS	t_{FSIVKH}	2.4	-	ns	-
Hold time for incoming data without DQS	t_{FSIXKH}	1.05	-	ns	-
Output data delay	t_{FSKHOV}		2.35	ns	-
Output data hold	t_{FSKHOX}	-1.35	-	ns	-

Table continues on the next page...

Table 47. SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1 or 0x2 [2, 3, 4] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. Refer Flash Control Register 1 (FLSHxyCR1) in QorIQ LS1028ARM for more details, where x: A or B, y: 1 or 2. 2. See Figure 29. on page 110. 3. See Figure 30. on page 111. 4. See Figure 31. on page 111.					

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x1 or 0x2

Table 48. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x1, or 0x2 [3, 4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	75.0	MHz	-
Duty cycle distortion	T_{dis}	-0.5	0.5	ns	-
CS output hold time	$t_{FSKHOX2}$	((FLSHxCR1[TCSH]+0.5)* T/2) - 0.54	-	ns	1
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5)* T/2) - 0.74	-	ns	1
Data Valid Window	t_{FSIDVW}	0.3	-	UI	2
Output data delay	t_{FSKHOV}/ t_{FSKLOV}	-	3.96	ns	-
Output data hold	t_{FSKHOX}/ t_{FSKLOX}	2.85	-	ns	-
1. Refer Flash Control Register 1 (FLSHxyCR1) in QorIQ LS1028ARM for more details, where x: A or B, y: 1 or 2. 2. For DDR, Unit Internval (UI) is half of period. For example, 5 ns for 100 MHz 3. See Figure 29. on page 110. 4. See Figure 30. on page 111. 5. See Figure 32. on page 112.					

This table provides the FlexSPI timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] =0x3

Table 49. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3 [2, 3, 4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	-	125.0	MHz	-
Duty cycle distortion	T_{dis}	-0.5	0.5	ns	-
CS output hold time	$t_{FSKHOX2}$	((FLSHxCR1[TCSH]+0.5)* T/2) - 0.54	-	ns	1

Table continues on the next page...

Table 49. DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3 [2, 3, 4, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
CS output delay	$t_{FSKHOV2}$	((FLSHxCR1[TCSS]+0.5)* T/2) - 0.74	-	ns	1
DQS to data valid	t_{FSIVKH}/ t_{FSIVKL}	-0.7	0.7	ns	-
DQS to data invalid	$t_{FSIIVKH}$/ $t_{FSIIVKL}$	-0.7	0.9	ns	-
Output data delay	t_{FSKHOV}/ t_{FSKLOV}	-	2.57	ns	-
Output data hold	t_{FSKHOX}/ t_{FSKLOX}	1.4	-	ns	-

1. Refer Flash Control Register 1 (FLSHxyCR1) in QorIQ LS1028ARM for more details, where x: A or B, y: 1 or 2.
2. See Figure 29. on page 110.
3. See Figure 30. on page 111.
4. See Figure 32. on page 112.
5. See Figure 28. on page 110.

This figure shows the FlexSPI data input timing in DDR mode with an external DQS.

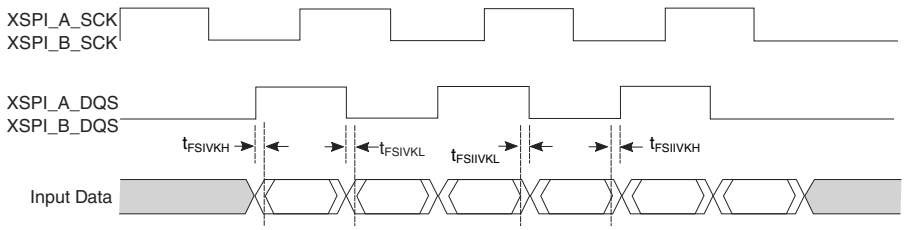


Figure 28. FlexSPI input AC timing - DDR mode with an external DQS

This figure shows the AC test load for the FlexSPI interface.

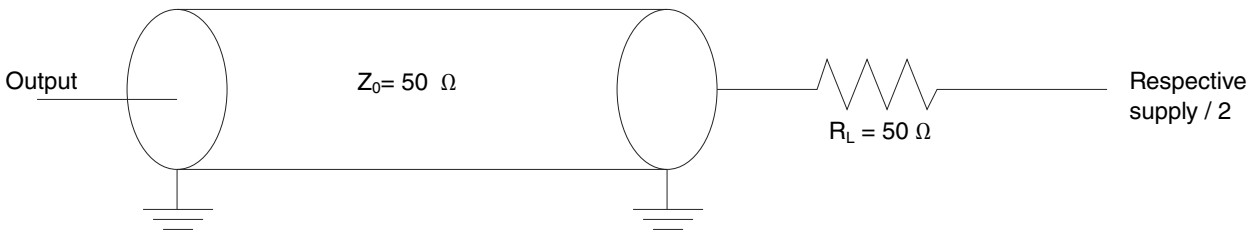


Figure 29. AC test load for FlexSPI

This figure shows the FlexSPI clock input timing diagram.

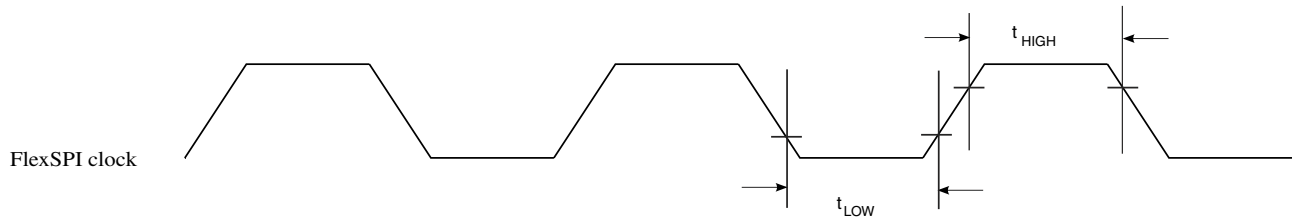


Figure 30. FlexSPI clock input timing diagram

This figure shows the FlexSPI AC timing diagram for SDR mode.

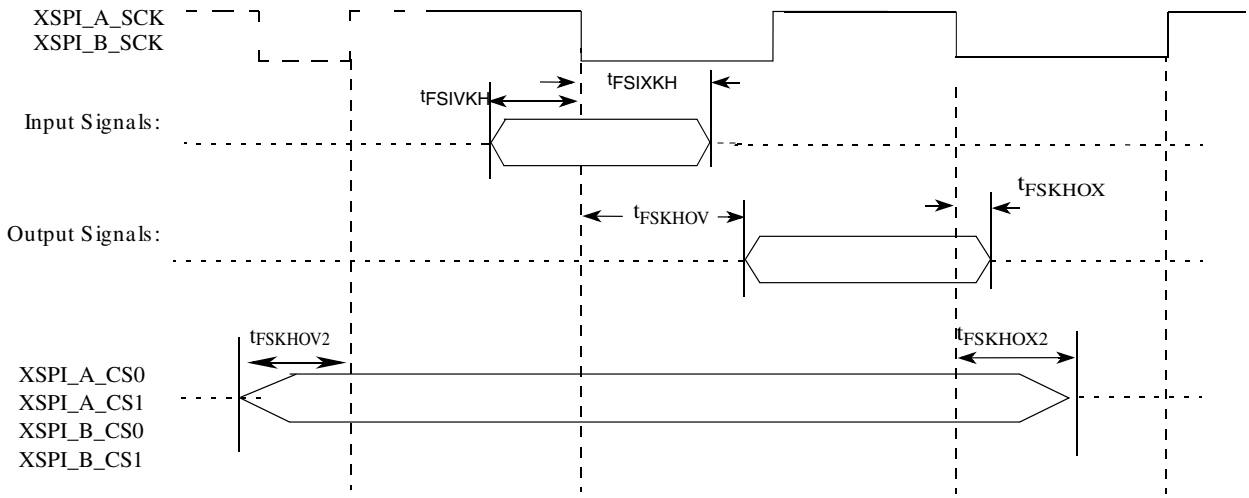


Figure 31. FlexSPI SDR mode AC timing diagram

This figure shows the FlexSPI AC timing diagram for DDR mode 1 and 2.

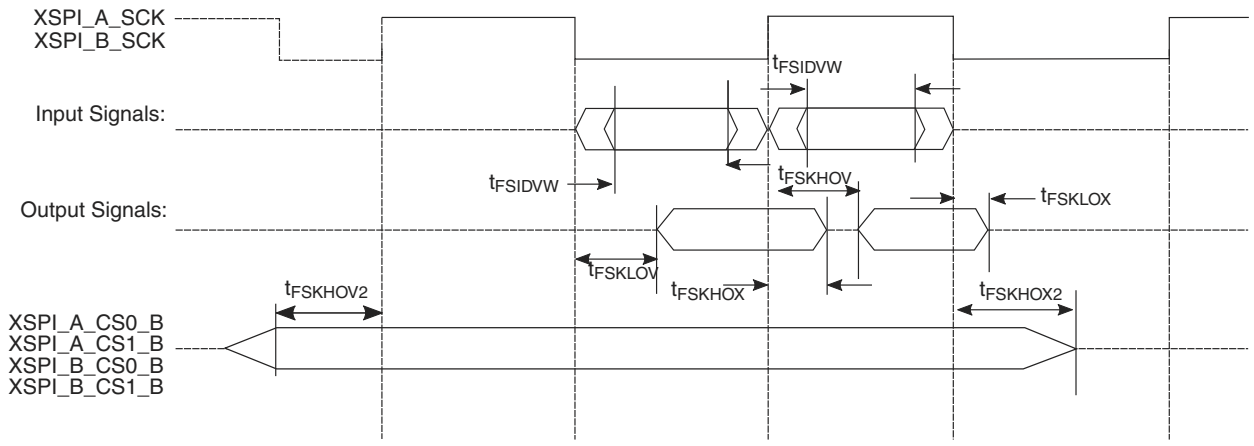


Figure 32. FlexSPI DDR mode 1 and 2 AC timing diagram

3.13 Flextimer interface

This section describes the DC and AC electrical characteristics for the Flextimer interface. There are Flextimer pins on various power supplies in this device.

3.13.1 FlexTimer DC electrical characteristics

This table provides the DC electrical characteristics for Flextimer.

Table 50. FlexTimer DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.13.2 FlexTimer AC timing specifications

This table provides theAC timing specifications for Flextimer.

Table 51. FlexTimer AC timing specifications [2]

Parameter	Symbol	Min	Max	Unit	Notes
Flextimer inputs - minimum pulse width	t_{PIWID}	20.0	-	ns	1

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs should be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

2. See Figure 33. on page 113.

This figure provides the AC test load for the Flextimer.

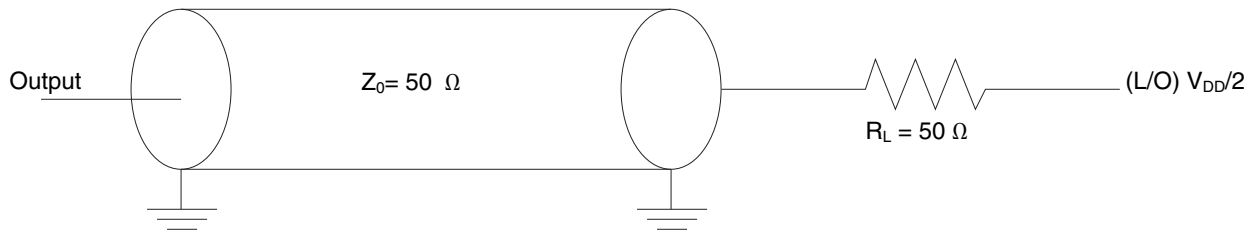


Figure 33. Flextimer AC test load

3.14 General purpose input/output (GPIO)

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface.

Table 52. GPIO DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN}= OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.14.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 53. GPIO AC timing specifications [2]

Parameter	Symbol	Min	Max	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20.0	-	ns	1

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

2. See Figure 34. on page 114.

The figure below provides the AC test load for the GPIO.

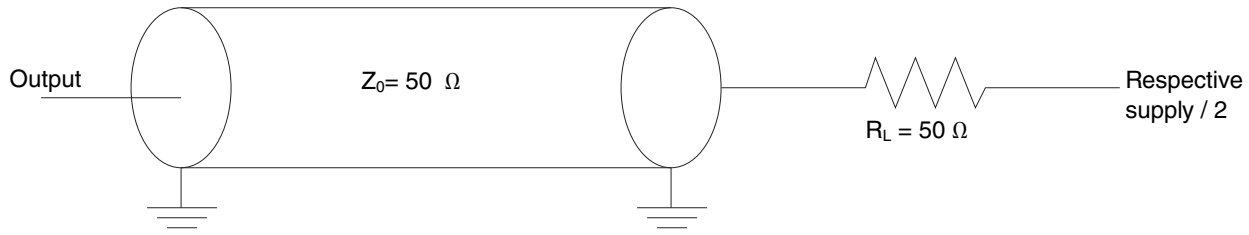


Figure 34. GPIO AC test load

3.15 Display Port/eDP interface (DP/eDP)

This section describes the AC and DC electrical characteristics for the Display Port/eDP interface.

3.15.1 eDP/DP DC electrical characteristics

This table provides the DC electrical characteristics for eDP transmitter module.

Table 54. eDP transmitter DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential Peak-to-peak Output Voltage Swing Level 0	$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	180.0	200.0	220.0	mV	2, 3
Differential Peak-to-peak Output Voltage Swing Level 1	$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	225.0	250.0	275.0	mV	2, 3
Differential Peak-to-peak Output Voltage Swing Level 2	$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	270.0	300.0	330.0	mV	2, 3
Differential Peak-to-peak Output Voltage Swing Level 3	$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3}$	315.0	350.0	385.0	mV	2, 3

Table continues on the next page...

Table 54. eDP transmitter DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential Peak-to-peak Output Voltage Swing Level 4	$V_{TX-DIFFp-p-Level4}$	360.0	400.0	440.0	mV	2, 3
Differential Peak-to-peak Output Voltage Swing Level 5	$V_{TX-DIFFp-p-Level5}$	405.0	450.0	495.0	mV	2, 3
Maximum allowed Differential Peak-to- Peak Output Voltage	$V_{TX-DIFFP-P-MAX}$	-	-	1380.0	mV	4
Transmit lane short-circuit current	$I_{TX-SHORT}$	-	-	50.0	mA	5
AC coupling capacitor	C_{TX}	75.0	-	265.0	nF	5, 6

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Steps between $V_{TX-DIFF-p-p}$ voltages must be monotonic.

3. Specified at the package pins.

4. Allows eDP Source devices to support differential signal voltages compatible with eDP v1.3 (and lower) devices and designs.

5. From DP1.3

6. Use 100nF typical value

This table provides the DC electrical characteristics for DP transmitter module.

Table 55. DP transmitter DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential Peak-to-peak Output Voltage Swing Level 0	$V_{TX-DIFFp-p-Level0}$	340.0	400.0	460.0	mV	2, 3, 4
Differential Peak-to-peak Output Voltage Swing Level 1	$V_{TX-DIFFp-p-Level1}$	510.0	600.0	680.0	mV	2, 3, 4
Differential Peak-to-peak Output Voltage Swing Level 2	$V_{TX-DIFFp-p-Level2}$	690.0	800.0	920.0	mV	2, 3, 4
Differential Peak-to-peak Output Voltage Swing Level 3	$V_{TX-DIFFp-p-Level3}$	850.0	1200.0	1380.0	mV	2, 3, 4
Transmit lane short-circuit current	$I_{TX-SHORT}$	-	-	50.0	mA	5
Pre-emphasis Level 0	$V_{TX-PREEMP-RATIO-Level0}$	-	0.0	-	dB	6

Table continues on the next page...

Table 55. DP transmitter DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Pre-emphasis Level 1	$V_{TX-PREEMP-RATIO-Level1}$	2.8	3.5	4.2	dB	6
Pre-emphasis Level 2	$V_{TX-PREEMP-RATIO-Level2}$	4.8	6.0	7.2	dB	6
Pre-emphasis Level 3	$V_{TX-PREEMP-RATIO-Level3}$	7.5	9.5	11.4	dB	7
Pre-emphasis Post Cursor2 Level 0	$V_{TX-PREEMP-POST2-RATIO-Level0}$	-	0.0	-	dB	8
Pre-emphasis Post Cursor2 Level 1	$V_{TX-PREEMP-POST2-RATIO-Level1}$	-1.1	-0.9	-0.7	dB	8
Pre-emphasis Post Cursor2 Level 2	$V_{TX-PREEMP-POST2-RATIO-Level2}$	-2.3	-1.9	-1.5	dB	8
Pre-emphasis Post Cursor2 Level 3	$V_{TX-PREEMP-POST2-RATIO-Level3}$	-3.7	-3.1	-2.5	dB	8
AC coupling capacitor	C_{TX}	75.0	-	265.0	nF	5, 9
TX DC Common Mode Voltage	$V_{TX-DC-CM}$	0.0	-	2.0	V	10
TX AC Common Mode Voltage for HBR and RBR	$V_{TX-AC-CM}$	-	-	20.0	mV rms	-
TX AC Common Mode Voltage for HBR2	$V_{TX-AC-CM}$	-	-	30.0	mV rms	-

Table continues on the next page...

Table 55. DP transmitter DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Steps between $V_{TX-DIFF-p-p}$ voltages must be monotonic. 3. Specified at the package pins. 4. Voltage Swing Level 3 for RBR and HBR is optional. 5. From DP1.3 6. Support for Pre-emphasis Levels 0, 1, and 2 is required. 7. Support for Pre-emphasis Level 3 is optional. 8. At TP1 (refer eDP spec 1.4) 9. Use 100nF typical value 10. Common mode voltage is equal to Vbias_TX voltage.						

This table provides the DP_HPD DC electrical characteristics.

Table 56. DP_HPD DC electrical characteristics (DP_OV $_{DD}$ = 1.8V) [1]

Parameter	Min	Typ	Max	Unit
DP_HPD Voltage	2.25	-	3.6	V
Hot plug detection threshold	2.0	-	-	V
Hot unplug detection threshold	-	-	0.8	V
Input leakage current	-	2.4	3.8	uA
1. For recommended operating conditions, see Recommended Operating Conditions.				

This table lists the eDP/DPAUXchannel electrical specifications.

Table 57. eDP/DP AUX channel electrical specifications (DP_OV $_{DD}$ = 1.8V) [1, 3, 4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Manchester transaction unit interval	UI_{MAN}	0.4	-	0.6	us	2, 3, 4
Number of pre-charge pulses	Pre-charge Pulses	10.0	-	16.0	-	5
AUX CH bus park time	$T_{AUX-BUS-PARK}$	10.0	-	-	ns	6
AUX Peak-to-peak differential voltage at TX package pins (TP1) for eDP1.4	$V_{AUX-DIFFP-P}$	0.18	0.2	1.38	V	7

Table continues on the next page...

Table 57. eDP/DP AUX channel electrical specifications (DP_OV_{DD} = 1.8V) [1, 3, 4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Peak-to-peak differential voltage at TX package pins (TP1) when transmitting for DP 1.3 specification	$V_{TX_AUX-DIFFP-P}$	0.29	-	0.4	V	7
AUX Peak-to-peak differential voltage at TX package pins (TP1) when receiving for DP 1.3 specification	$V_{RX_AUX-DIFFP-P}$	0.29	-	1.38	V	7
AUX channel DC common mode voltage for eDP 1.4 specification	$V_{AUX-DC-CM-eDP}$	0.0	-	1.2	V	-
AUX channel DC common mode voltage for DP 1.3 specification	$V_{AUX-DC-CM-DP}$	0.0	-	2.0	V	-
AUX AC-coupling capacitor	C_{TX}	75.0	-	200.0	nF	8
AUX short circuit current limit	I_{AUX_SHORT}	-	-	90.0	mA	-
AUX turn around common mode voltage	$V_{AUX-TURN-CM}$	-	-	0.3	V	9
AUX CH termination DC resistance	$V_{AUX_TERM_R}$	-	100.0	-	ohm	-
Maximum allowable UI variation within a single transaction of a transmitting device	$T_{cycle-to-cycle\ jitter}$	-	-	0.08	UI	10, 11
Maximum allowable variation for adjacent bit times within a single transaction of a transmitting device	$T_{cycle-to-cycle\ jitter}$	-	-	0.04	UI	12, 11
Maximum allowable UI variation within a single transaction of a receiving device	$T_{cycle-to-cycle\ jitter}$	-	-	0.1	UI	13, 11
Maximum allowable variation for adjacent bit times within a single transaction of a receiving device	$T_{cycle-to-cycle\ jitter}$	-	-	0.05	UI	14, 11

Table continues on the next page...

Table 57. eDP/DP AUX channel electrical specifications (DP_OV_{DD} = 1.8V) [1, 3, 4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Results in the bit rate of 1Mbps including the overhead of Manchester-II coding.

3. See Figure 35. on page 119.

4. See Figure 36. on page 120.

5. Each pulse is a 0 in Manchester-II code.

6. Period after the AUX CH STOP condition for which the bus is parked.

7. $V_{AUX\text{-}DIFFP\text{-}P} = 2 \times | V_{DP_AUX_P} - V_{DP_AUX_M} |$

8. Use 100nF typical value

9. Steady state common mode voltage shift between transmit and receive modes of operation

10. Equal to 48ns maximum. The transmitting device is an upstream device for a Request transaction and a downstream device for a Reply transaction.

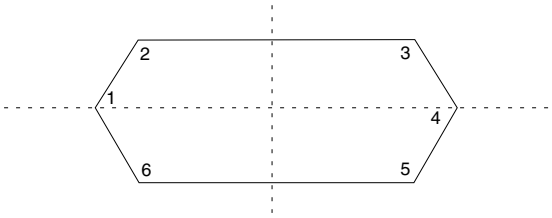
11. At TP2 (refer eDP spec 1.4)

12. Equal to 24ns maximum. The transmitting device is an upstream device for a Request transaction and a downstream device for a Reply Transaction.

13. Equal to 60ns maximum. The transmitting device is an upstream device for a Request transaction and a downstream device for a Reply Transaction.

14. Equal to 30ns maximum. The transmitting device is an upstream device for a Request transaction and a downstream device for a Reply Transaction.

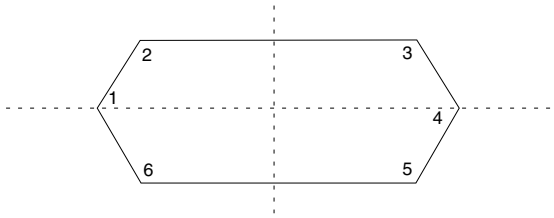
This figure illustrates the Aux CH EYE mask at the transmitting device's package pins and vertices values



Point	Time (UI)	Minimum Voltage Value at Six Vertices (mV)
1	0.01	0
2	0.11	90
3	0.89	90
4	0.99	0
5	0.89	-90
6	0.11	-90
Note: For eDP 1.4 at TP1		

Figure 35. Aux CH EYE mask for manchester-II transactions at transmitting device's package

This figure illustrates mask vertices for Aux CH EYE at connector pins of TX device



Point	Time (from Eye Center) (ns)	Minimum Voltage Value at Six Vertices (mV)
1	-185	0
2	-135	145
3	135	145
4	185	0
5	135	-145
6	-135	-145
Note: For DP 1.3 at TP2		

Figure 36. Aux CH EYE mask at connector pins of TX device

3.15.2 eDP/DP AC timing specifications

This table provides the DP_HPD AC timing specifications.

Table 58. DP_HPD AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
IRQ_HPD Pulse/glitch detection threshold for Upstream device	t_{HPD_WIDTH}	0.25	-	ms	1
IRQ_HPD Pulse /Hot Unplug event detection threshold for Upstream device	$t_{HPD_UNPLUG_WIDTH}$	2.0	-	ms	2
IRQ_HPD minimum spacing	$t_{HPD_MIN_SPACING}$	2.0	-	ms	3
1. When the pulse width is narrower than this threshold, the upstream device must ignore the pulse as a glitch. 2. When the pulse width is narrower than this threshold, the upstream device must read the Link/Sink Device Status field and take corrective action. When the pulse width is wider than this threshold, it is likely to be actual cable unplug/re-plug event. Upon detecting HPD high, the upstream device must read the Link/Sink Device Status field, and if the link is unstable, read the Link/Sink Capability field of the DPCD before initiating Link Training. 3. Minimum Time after asserting HPD at the end of IRQ_HPD before de-asserting HPD at the start of the following IRQ_HPD.					

This table provides the eDP/DP transmitter output AC timing specifications.

Table 59. eDP/DP transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit interval for BR1	U_{IBR1}	-	617.3	-	ps	1

Table continues on the next page...

Table 59. eDP/DP transmitter AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit interval for BR2	U_{IBR2}	-	463.0	-	ps	1
Unit interval for BR3	U_{IBR3}	-	411.5	-	ps	1
Unit interval for BR4	U_{IBR4}	-	370.4	-	ps	1
Unit interval for BR5	U_{IBR5}	-	308.6	-	ps	1
Unit interval for BR6	U_{IBR6}	-	231.5	-	ps	1
Unit interval for BR7	U_{IBR7}	-	185.0	-	ps	1
Deterministic jitter	D_{JMAX}	-	-	0.17 x UI	ps	2, 3
Total jitter	T_{JMAX}	-	-	0.27 x UI	ps	2, 3
Lane Intra-pair output skew	$L_{TX-SKEWINTRA_PAIR_CHIP}$	-	-	20.0	ps	4, 5
Lane Intra-pair Rise-fall Time Mismatch	$T_{TX-RISE_FALL_MISMATCH_DIFF}$	-	-	5.0	%	6, 4
D+/D- TX Output Rise/Fall Time	$T_{TX-RISE}/T_{TX-FALL}$	50.0	-	130.0	ps	7, 4
Minimum TX EYE Width at TP1	T_{TXEYE_RBR}	0.82	-	-	UI	8
Minimum TX EYE Width at TP1	T_{TXEYE_HBR}	0.72	-	-	UI	9
Minimum TX EYE Width at TP1	T_{TXEYE_HBR2}	0.73	-	-	UI	10
Maximum time between the jitter median and maximum deviation from the median at TP1	$T_{TX-EYE-MEDIANto-MAX-JITTER_RBR}$	-	-	0.09	UI	8
Maximum time between the jitter median and maximum deviation from the median at TP1	$T_{TX-EYE-MEDIANto-MAX-JITTER_HBR}$	-	-	0.147	UI	9

Table continues on the next page...

Table 59. eDP/DP transmitter AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum time between the jitter median and maximum deviation from the median at TP1	$T_{TX-EYE-MEDIANto-MAX-JITTER_HBR2}$	-	-	0.135	UI	10
Differential Return Loss at 0.675GHz	$R_{LTX-DIFF}$	12.0	-	-	dB	4, 11
Differential Return Loss at 1.35GHz	$R_{LTX-DIFF}$	9.0	-	-	dB	4, 11
Clock Jitter Rejection Bandwidth	$F_{TX-REJECTION BW}$	-	-	4.0	MHz	12

1. High Limit= +300ppm; Low Limit= -5300ppm. For constant (non-SSC) Frequency

2. Based on D10.2 pattern

3. The EYE diagram must be measured with a Compliance Test Load and a signal analyzer that includes a Link CDR emulation function matching the DisplayPort receiver Jitter Tolerance Mask specifications

4. At TP1 (refer eDP spec 1.4)

5. Applies to all supported lanes.

6. D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.

7. 20% to 80%

8. For RBR

9. For HBR

10. For HBR2

11. Straight loss line between 0.675 GHz and 1.35 GHz

12. Transmitter jitter must be measured at source connector pins using a signal analyzer that has a second-order PLL with closed-loop tracking bandwidth of 20MHz (for D10.2 pattern) and damping factor of 1.428.

This table provides the AC requirements for eDP reference clocks.

Table 60. DP_REFCLK_P and DP_REFCLK_N input clock requirements. [8]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DP_REFCLK_P and DP_REFCLK_N frequency	t_{DP_REFCLK}	-	27.0	-	MHz	1
DP_REFCLK_P and DP_REFCLK_N clock frequency tolerance	$t_{DP_REFCLK_TOL}$	-300.0	-	300.0	ppm	-

Table continues on the next page...

Table 60. DP_REFCLK_P and DP_REFCLK_N input clock requirements. [8] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak amplitude		0.5	-	2.2	V	2
External AC coupling capacitor	C_{TX}	100.0	-	-	nF	3
DP_REFCLK_P and DP_REFCLK_N reference clock duty cycle	$t_{DP_REFCLK_DUTY}$	45.0	-	55.0	%	-
DP_REFCLK_P and DP_REFCLK_N rise and fall time	t_R/t_F	-	-	400.0	ps	4
Input deterministic Jitter	$t_{DP_REFCLK_DJ}$	-	-	9.0	ps	5
Input Phase Noise	$t_{DP_REFCLK_PN}$	-	-	-125 dBc/Hz max @ 10 kHz -130 dBc/Hz max @ 100 kHz -140 dBc/Hz max @ 1 MHz -140 dBc/Hz max @ 10 MHz	dBC/Hz	6
Input Random Jitter	$t_{DP_REFCLK_RJ}$	-	-	2.963	ps	7

1. Non-SSC pure tone clock
2. At Package pin
3. Place before receiver pins
4. 20% to 80%
5. Over a band of 10KHz to 10MHz
6. The noise floor density range is from 10 KHz to 10 MHz
7. The integrated jitter range is from 10 KHz to 10 MHz
8. HCSL clock receiver

3.16 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, 1000Base-KX, USXGMII and serial ATA (SATA) data transfers.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.16.1 Signal terms definitions

The SerDes uses differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

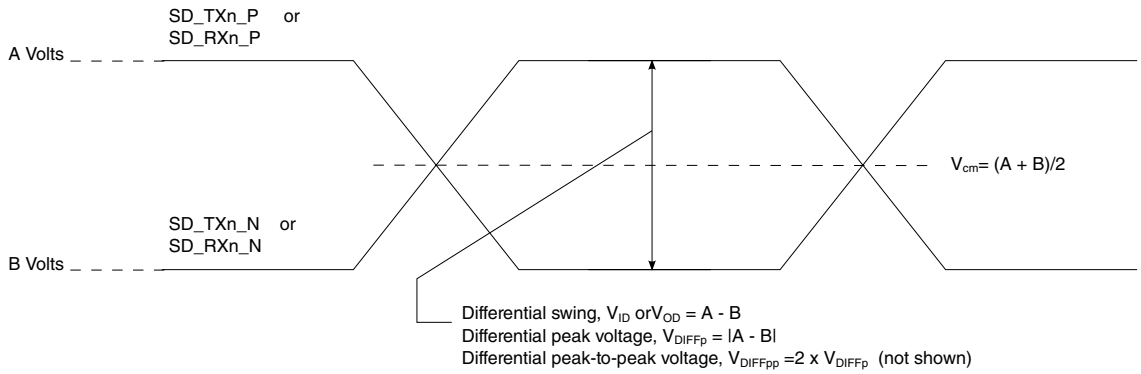


Figure 37. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing — The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing) — The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TX\ n_}P$ - $V_{SD_TXn_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing) — The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD_RXn_P}$- $V_{SD_RXn_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp} — The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$ — Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 x |V_{OD}|.

Differential Waveform — The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 42. on page 130 as an example for differential waveform.

Common Mode Voltage, V_{cm} — The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = ($V_{SD_TXn_P}$ + $V_{SD_TXn_N}$) ÷ 2 = (A + B) ÷ 2, which is the arithmetic mean of the two complementary output voltages

within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.16.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbps), QSGMII (5 Gbps)
- PCIe (2.5 GT/s, 5 GT/s and 8 GT/s)
- SATA (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.16.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 61. SerDes spread-spectrum clock source recommendations 1 on page 125. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 61. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Recommended Operating Conditions.

2. Only down-spreading is allowed.

3.16.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

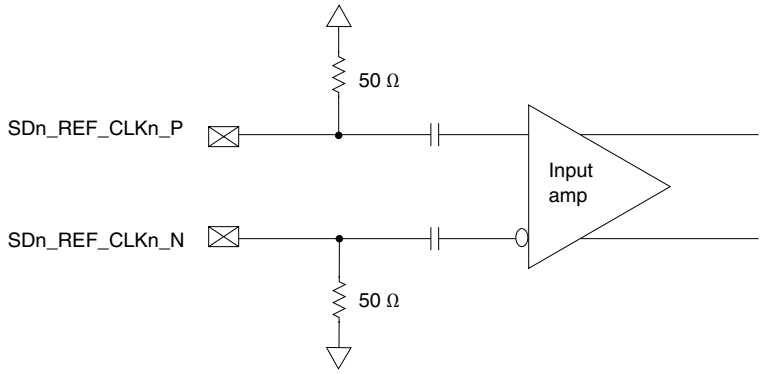


Figure 38. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceiver's core power supply voltage requirements (SV_{DD}) are as specified in Recommended Operating Conditions.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 38. on page 126. Each differential clock input (SD*n*_REF_CLK*n*_P or SD*n*_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions on page 124 for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.16.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below.

Differential mode:

- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics on page 125, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 39. on page 127 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

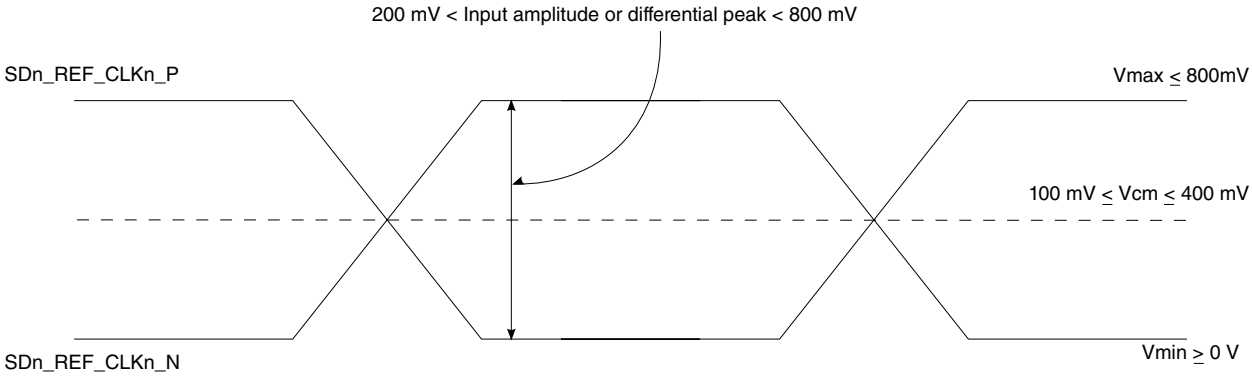


Figure 39. Differential reference clock input DC requirements (external DC-coupled)

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (GND). Figure 40. on page 127 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

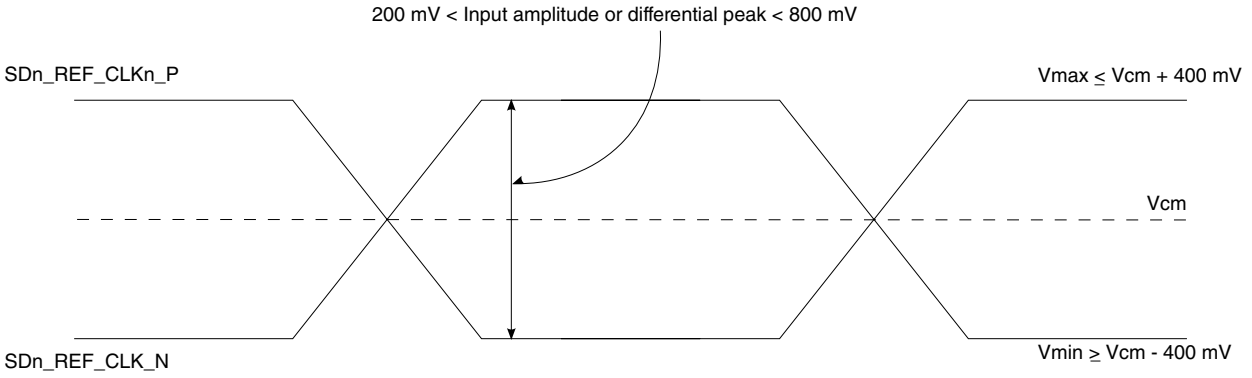


Figure 40. Differential reference clock input DC requirements (external AC-coupled)

Single-ended mode:

- The reference clock can also be single-ended. The SDn_REF_CLKn_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SDn_REF_CLKn_N either left unconnected or tied to ground.
- The SDn_REF_CLKn_P input average voltage must be between 200 and 400 mV. Figure 41. on page 128 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SDn_REF_CLKn_N) through the same source impedance as the clock input (SDn_REF_CLKn_P) in use.

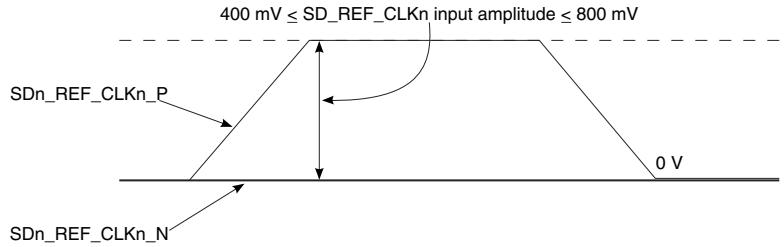


Figure 41. Single-ended reference clock input DC requirements

3.16.2.4 SerDes reference clocks AC timing specifications

For protocols with data rates up to 5 Gb/s where there is no reference clock jitter specification (ex: SGMII), use the PCIe 2.5G clock jitter requirements.

For protocols with data rates greater than 5 Gb/s and less than 8 Gb/s where there is no reference clock jitter specification, use the PCIe 5G clock jitter requirements.

For protocols with data rates greater than 8 Gb/s and less than 16 Gb/s where there is no reference clock jitter specification (ex: USXGMII-10.3125G), use the PCIe 8G or XFI clock jitter requirements.

Use the protocol's reference clock frequency tolerance specification (ex: +/-100 ppm for SGMII/USXGMII/1000Base-KX, +/-300 ppm for PCIe and +/-350 ppm for SATA).

This table defines the AC requirements for SerDes reference clocks for PCI Express. SerDes reference clocks need to be verified by the customer's application design.

Table 62. SD1_REF_CLKn_P and SD1_REF_CLKn_N input clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	1
PCI Express SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-300.0	-	300.0	ppm	2
SGMII SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100.0	-	100.0	ppm	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40.0	50.0	60.0	%	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42.0	ps	-

Table continues on the next page...

Table 62. SD1_REF_CLKn_P and SD1_REF_CLKn_N input clock requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	-	-	86.0	ps	5
PCI Express 5 GT/s SD1_REF_CLKn_P/ SD1_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK-LF-RMS}$	-	-	3.0	ps RMS	6
PCI Express 5 GT/s SD1_REF_CLKn_P/ SD1_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK-HF-RMS}$	-	-	3.1	ps RMS	6
SD1_REF_CLKn_P/ SD1_REF_CLKn_N rising/falling edge rate	t_{CLKRR}/ t_{CLKFR}	0.6	-	4.0	V/ns	7, 8
PCI Express 8 GT/s SD1_REF_CLKn_P/ SD1_REF_CLKn_N RMS reference clock jitter	$t_{REFCLK-RMS-DC}$	-	-	1.0	ps RMS	9
Differential input high voltage	V_{IH}	150.0	-	-	mV	4
Differential input low voltage	V_{IL}	-	-	-150.0	mV	4
Rising edge rate (SD1_REF_CLKn_P) to falling edge rate (SD1_REF_CLKn_N) matching	Rise-Fall matching	-	-	20.0	%	10, 11, 12

Table continues on the next page...

Table 62. SD1_REF_CLKn_P and SD1_REF_CLKn_N input clock requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Caution: Only 100, 125, and 156.25 have been tested. In-between values do not work correctly with the rest of the system. 2. For PCI Express (2.5, 5 and 8 GT/s). 3. For SGMII, 2.5G SGMII and QSGMII. 4. Measurement taken from differential waveform. 5. Limits from PCI Express CEM Rev 2.0. 6. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0. 7. Measured from -150 mV to +150 mV on the differential waveform (derived from SD1_REF_CLKn_P minus SD1_REF_CLKn_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. 8. See Figure 42. on page 130. 9. For PCI Express 8 GT/s, per PCI Express base specification Rev. 3.0. 10. Measurement taken from single-ended waveform. 11. Matching applies to rising edge for SD1_REF_CLKn_P and falling edge rate for SD1_REF_CLKn_N. It is measured using a ±75 mV window centered on the median cross point where SD1_REF_CLKn_P rising meets SD1_REF_CLKn_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD1_REF_CLKn_P must be compared to the fall edge rate of SD1_REF_CLKn_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. 12. See Figure 43. on page 131.						

This figure shows the differential measurement points for rise and fall time.

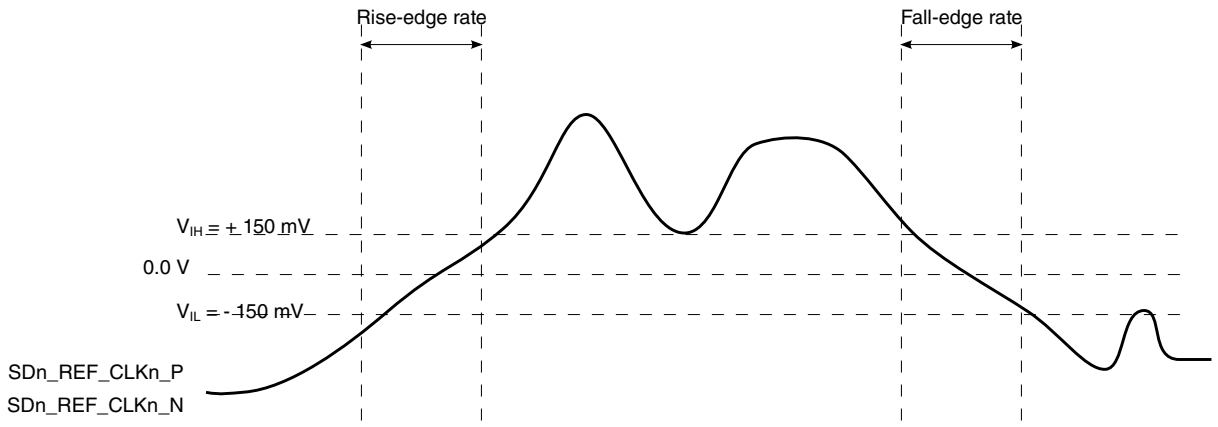


Figure 42. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

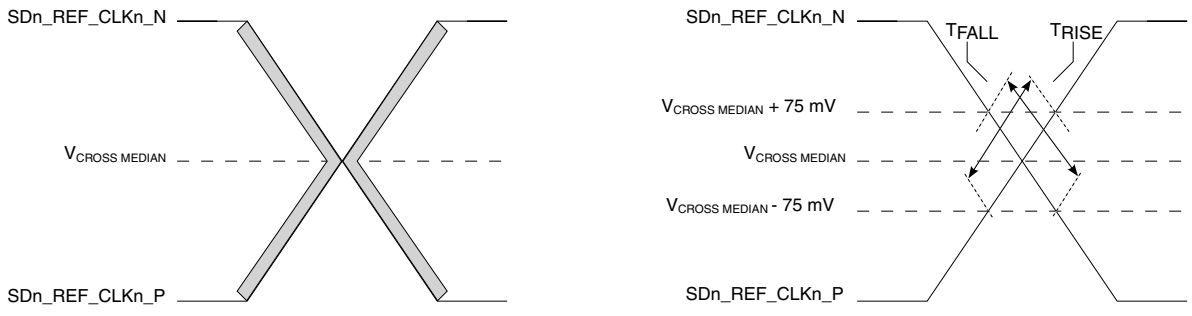


Figure 43. Single-ended measurement points for rise and fall time matching

For protocols with data rates greater than 8 Gb/s where there is no reference clock jitter specification (ex:USXGMII-10.3125G), use the PCIe 8G clock jitter requirements.

This table defines the AC requirements for SerDes reference clocks for USXGMII-10.3125G SerDes reference clocks need to be verified by the customer's application design.

Table 63. SD1_REF_CLKn_P and SD1_REF_CLKn_N input clock requirements for USXGMII

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	t_{CLK_REF}	-	156.25	-	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
Reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	2
Single side band noise at 1 kHz	at 1 kHz	-	-	-85	dBC/Hz	3
Single side band noise at 10 kHz	at 10 kHz	-	-	-108	dBC/Hz	3
Single side band noise at 100 kHz	at 100 kHz	-	-	-128	dBC/Hz	3
Single side band noise at 1 MHz	at 1 MHz	-	-	-138	dBC/Hz	3
Single side band noise at 10 MHz	at 10 MHz	-	-	-138	dBC/Hz	3
Random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
Total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
Spurious noise (1.2 MHz to 15 MHz)	NA	-	-	-75	dBC	-

Table continues on the next page...

Table 63. SD1_REF_CLKn_P and SD1_REF_CLKn_N input clock requirements for USXGMII (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Caution: Only 156.25 have been tested. Inbetween values do not work correctly with the rest of the system. 2. Measurement taken from differential waveform. 3. Per XFP specification, Rev 4.5, the Module Jitter Generation spec at XFI optical output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode, the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.						

3.16.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

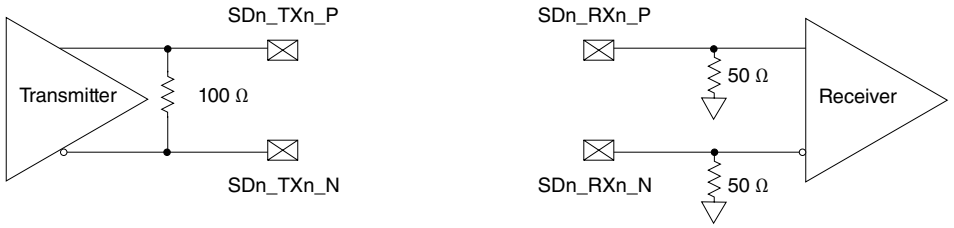


Figure 44. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- SATA
- SGMII
- USXGMII

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.16.4 PCI Express

3.16.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.16.4.2 PCI Express clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

SD1_REF_CLK1_N / SD1_REF_CLK1_P and SD1_REF_CLK2_N / SD1_REF_CLK2_P may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks on page 125.

3.16.4.3 PCI Express DC electrical characteristics

This section describes the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s. This table defines the PCI Express 2.0 (2.5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 64. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFP-P}$	800.0	1000.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	3
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	5

1. For recommended operating conditions, see Recommended Operating Conditions.
2. $V_{TX_DIFFp-p} = 2 \times | V_{TX-D+} - V_{TX-D-} |$
3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
4. Transmitter DC differential mode low impedance
5. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (2.5 GT/s) differential receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	175.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

Table continues on the next page...

Table 65. PCI Express 2.0 (2.5 GT/s) differential receiver input DC electrical characteristics [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. $V_{RX_DIFFp\text{-}p}$ = 2 x | $V_{RX\text{-}D+}$ - $V_{RX\text{-}D-}$ | 3. Measured at the package pins with a test load of 50Ω to GND on each pin. 4. Receiver DC differential mode impedance. 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port. 6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance). 7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power. 8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground. 9. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ = 2 x | $V_{RX\text{-}D+}$ - $V_{RX\text{-}D-}$ |						

This table defines the PCI Express 2.0 (5 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 66. PCI Express 2.0 (5 GT/s) differential transmitter output DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFP\text{-}P}$	800.0	1000.0	1200.0	mV	2
Low power differential peak-peak output voltage	$V_{TX\text{-}DIFFP\text{-}P\text{-}LOW}$	400.0	500.0	1200.0	mV	2
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	3
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80.0	100.0	120.0	Ω	4
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40.0	50.0	60.0	Ω	5
1. For recommended operating conditions, see Recommended Operating Conditions. 2. $V_{TX_DIFFp\text{-}p}$ = 2 x | $V_{TX\text{-}D+}$ - $V_{TX\text{-}D-}$ | 3. Ratio of $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. 4. Transmitter DC differential mode low impedance 5. Required transmitter D+ as well as D- DC Impedance during all states.						

This table defines the DC electrical characteristics for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 67. PCI Express 2.0 (5 GT/s) differential receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential peak-to-peak voltage	$V_{RX-DIFFP-P}$	120.0	1000.0	1200.0	mV	2, 3
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	4, 5
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	6, 3, 5
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	7, 8
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	9, 3

1. For recommended operating conditions, see Recommended Operating Conditions.

2. $V_{RX_DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

3. Measured at the package pins with a test load of 50Ω to GND on each pin.

4. Receiver DC differential mode impedance.

5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

6. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

7. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

8. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

9. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

This table defines the PCI Express 3.0 (8 GT/s) DC electrical characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 68. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800.0	-	1300.0	mVp-p	2
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400.0	-	1300.0	mV	2

Table continues on the next page...

Table 68. PCI Express 3.0 (8 GT/s) differential transmitter output DC electrical characteristics [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	3
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	3
Minimum swing during EIEOS for full swing	$Z_{TX-EIEOS-FS}$	250.0	-	-	mVp-p	4
Minimum swing during EIEOS for reduced swing	$Z_{TX-EIEOS-RS}$	232.0	-	-	mVp-p	4
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80.0	100.0	120.0	Ω	5
Transmitter DC impedance	Z_{TX-DC}	40.0	50.0	60.0	Ω	6

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

3. Ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

4. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

5. Transmitter DC differential mode low impedance

6. Required transmitter D+ as well as D- DC Impedance during all states.

This table defines the DC electrical characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 69. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80.0	100.0	120.0	Ω	2, 3
DC input impedance	Z_{RX-DC}	40.0	50.0	60.0	Ω	4, 5, 3
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50.0	-	-	kΩ	6, 7

Table continues on the next page...

Table 69. PCI Express 3.0 (8 GT/s) differential receiver input DC electrical characteristics [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65.0	-	175.0	mV	8, 5
Generator launch voltage	$V_{RX-LAUNCH-8G}$	-	800.0	-	mV	9
Eye height (-20dB channel)	$V_{RX-SV-8G}$	25.0	-	-	mV	10
Eye height (-12dB channel)	$V_{RX-SV-8G}$	50.0	-	-	mV	10
Eye height (-3dB channel)	$V_{RX-SV-8G}$	200.0	-	-	mV	10

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Receiver DC differential mode impedance.

3. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all configured lanes on a port.

4. Required receiver D+ as well as D- DC impedance (50 ± 20% tolerance).

5. Measured at the package pins with a test load of 50Ω to GND on each pin.

6. Required receiver D+ as well as D- DC impedance when the receiver terminations do not have power.

7. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300mV above the receiver ground.

8. $V_{RX-IDLE-DET-DIFFp-p} = 2 \times | V_{RX-D+} - V_{RX-D-} |$

9. Measured at TP1 per PCI Express base specification Rev 3.0.

10. Measured at TP2 per PCI Express base specification Rev 3.0. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. In the parameter names, "SV" refers to stressed voltage. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2.

3.16.4.4 PCI Express AC timing specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 70. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5

Table continues on the next page...

Table 70. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	6, 3, 4, 5
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.

2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 -T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}.

3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis.

4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

5. See Figure 46. on page 143.

6. Jiiter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI.

7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the AC timing specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timingspecifications do not include RefClk jitter.

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	399.88	400.0	400.12	ps	1
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	3, 4, 5

Table continues on the next page...

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. 2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE} = 0.6 UI. 3. Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. 4. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram. 5. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 72. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	2, 3, 4, 5
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	6
AC coupling capacitor	C_{TX}	75.0	-	200.0	nF	7, 8

Table continues on the next page...

Table 72. PCI Express 2.0 (5 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. 2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 -T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or REFCLK jitter. Includes devices random jitter at 10^{-12}. 3. Specified at the measurement point into a timing and voltage test load and measured over any 250 consecutive transmitter Uis. 4. A T_{TX-EYE} - 0.75 UI provides for a a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter Uis. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 5. See Figure 46. on page 143. 6. Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps. 7. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. 8. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.						

This table defines the AC timing specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 73. PCI Express 2.0 (5 GT/s) differential receiver input AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	-
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.3	UI	-
1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.						

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1
AC coupling capacitor	C_{TX}	176.0	-	265.0	nF	2, 3
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-

Table continues on the next page...

Table 74. PCI Express 3.0 (8 GT/s) differential transmitter output AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12.0	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24.0	ps p-p	4, 5
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10.0	ps p-p	4, 5
Data-dependent jitter	T_{TX-DDJ}	-	-	18.0	ps p-p	4
1. Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. 2. All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. 3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 4. Measured with optimized preset value after de-embedding to transmitter pin. 5. PWJ parameters shall be measured after data-dependent jitter (DDJ) separation.						

This table defines the AC timing specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timingspecifications do not include RefClk jitter.

Table 75. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications [5]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	124.9625	125.0	125.0375	ps	1, 2
Eye width at TP2P	$T_{RX-SV-8G}$	0.3	-	0.35	UI	2
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14.0	-	-	mV	3
Sinusoidal jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	-	-	0.1	UI p-p	4, 5
Random jitter	$T_{RX-SV-RJ-8G}$	-	-	2.0	ps RMS	6, 5

Table continues on the next page...

Table 75. PCI Express 3.0 (8 GT/s) differential receiver input AC timing specifications [5] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Each UI is 125 ps ± 300 ppm. UI does not account for spreadspectrum clock dictated variations. 2. $T_{RX-SV-8G}$ is referenced to TP2P and is obtained after post-processing data is captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization. 3. Frequency = 2.1GHz. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels. 4. Fixed at 100 MHz. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency. 5. See Figure 45. on page 142. 6. Random jitter spectrally flat before filtering. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.						

This figure shows the swept sinusoidal jitter mask.

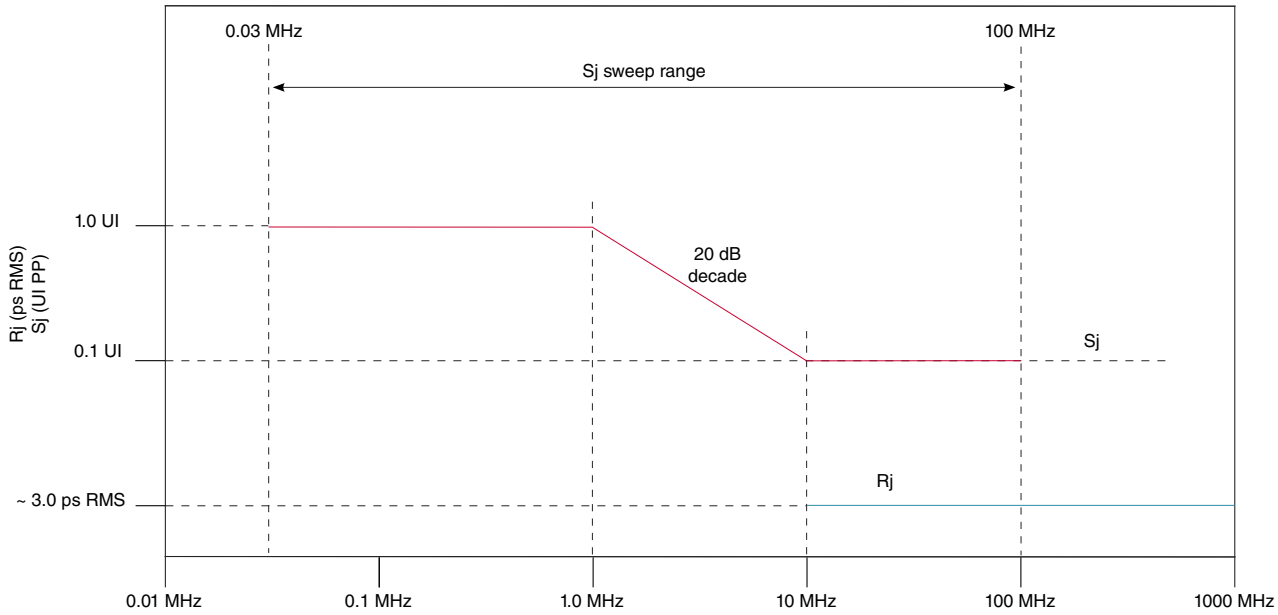


Figure 45. Swept sinusoidal jitter mask

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure. Note that the allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and Dpackage pins.

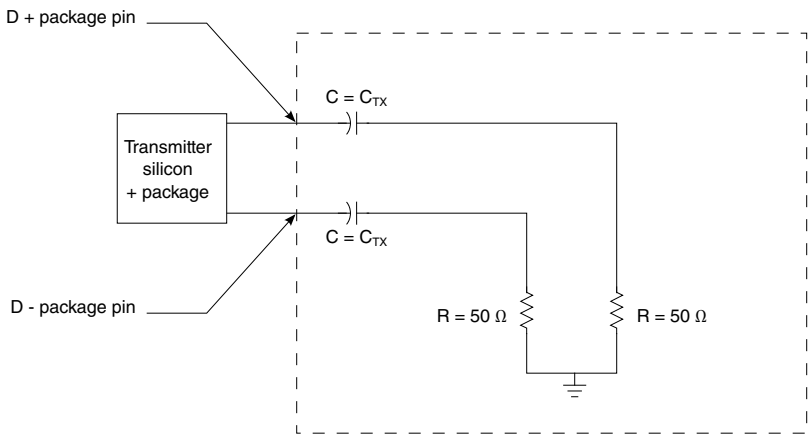


Figure 46. Test and measurement load

3.16.5 Serial ATA (SATA)

3.16.5.1 SATA DC electrical characteristics

This table provides the differential transmitter output DC characteristics for the SATAinterface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 76. SATA Gen 1i/1m 1.5G transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA_TX\ DIFF}$	400.0	500.0	600.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA_TX\ DIFFIM}$	85.0	100.0	115.0	Ω	DC impedance.
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Terminated by a 50Ω load. 3. DC impedance.						

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 77. SATA Gen 1i/1m 1.5G receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA_RX\ DIFF}$	240.0	500.0	600.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA_RX\ SEIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	50.0	120.0	240.0	mV p-p	-

Table continues on the next page...

Table 77. SATA Gen 1i/1m 1.5G receiver input DC electrical characteristics [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Voltage relative to common of either signal comprising a differential pair. 3. DC impedance.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 78. SATA Gen 2i/2m 3G transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA_TX\ DIFF}$	400.0	-	700.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA_TX\ DIFFIM}$	85.0	100.0	115.0	Ω	DC impedance.
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Terminated by a 50Ω load. 3. DC impedance.						

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 79. SATA Gen 2i/2m 3G receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA_RX\ DIFF}$	240.0	-	750.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA_RX\ SEIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	75.0	120.0	240.0	mV p-p	-
1. For recommended operating conditions, see Recommended Operating Conditions. 2. Voltage relative to common of either signal comprising a differential pair. 3. DC impedance.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 80. SATA Gen 3i transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter differential output voltage	$V_{SATA_TX\ DIFF}$	240.0	-	900.0	mV p-p	Terminated by a 50Ω load.
Transmitter differential pair impedance	$Z_{SATA_TX\ DIFFIM}$	85.0	100.0	115.0	Ω	DC impedance.

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Terminated by a 50Ω load.
3. DC impedance.

This table provides the Gen 3i differential receiver input DC characteristics for the SATAinterface.

Table 81. SATA Gen 3i receiver input DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	$V_{SATA_RX\ DIFF}$	240.0	-	1000.0	mV p-p	2
Differential receiver input impedance	$Z_{SATA_RX\ SEIM}$	85.0	100.0	115.0	Ω	3
OOB signal detection threshold	V_{SATA_OOB}	75.0	120.0	200.0	mV p-p	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Voltage relative to common of either signal comprising a differential pair.
3. DC impedance.

3.16.5.2 SATA AC timing specifications

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 82. SATA reference clock input requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn_P/ SDn_REF_CLKn_N frequency range	t_{CLK_REF}	-	100 / 125	-	MHz	1
SDn_REF_CLKn_P/ SDn_REF_CLKn_N frequency tolerance	t_{CLK_TOL}	-350.0	-	350.0	ppm	-

Table continues on the next page...

Table 82. SATA reference clock input requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn_P/ SDn_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	2
SDn_REF_CLKn_P/ SDn_REF_CLKn_N cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	-	-	100.0	ps	3
SDn_REF_CLKn_P/ SDn_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50.0	-	50.0	-	3, 4, 5

1. **Caution:** Only 100 MHz and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. Measurement taken from differential waveform.
3. At RefClk input.
4. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
5. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 83. Gen 1i/1m 1.5 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Total jitter, data-data 5 UI	$U_{SATA_TXTJ5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	-	-	0.22	UI p-p	1

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 84. Gen 1i/1m 1.5 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	666.4333	666.6667	670.2333	-	-
Total jitter, data-data 5 UI	$U_{SATA_RX\ TJ5UI}$	-	-	0.43	UI p-p	Measured at the receiver.
Total jitter, data-data 250 UI	$U_{SATA_RX\ TJ250UI}$	-	-	0.6	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 5 UI	$U_{SATA_RX\ DJ5UI}$	-	-	0.25	UI p-p	Measured at the receiver.
Deterministic jitter, data-data 250 UI	$U_{SATA_RX\ DJ250UI}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 85. Gen 2i/2m 3 G transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA_TX\ TJfB/500}$	-	-	0.37	UI p-p	1
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA_TX\ TJfB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA_TX\ TJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA_TX\ TJfB/1667}$	-	-	0.35	UI p-p	1
1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.						

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 2i/2m 3 G receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	333.2167	333.3333	335.1167	-	-

Table continues on the next page...

Table 86. Gen 2i/2m 3 G receiver AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA_RX\ TJfB/500}$	-	-	0.6	UI p-p	Measured at the receiver.
Total jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA_RX\ TJfB/1667}$	-	-	0.65	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 500$	$U_{SATA_RX\ TJfB/500}$	-	-	0.42	UI p-p	Measured at the receiver.
Deterministic jitter, $f_{C3DB} = f_{BAUD} \div 1667$	$U_{SATA_RX\ TJfB/1667}$	-	-	0.35	UI p-p	Measured at the receiver.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 3i transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Channel speed	t_{CH_SPEED}	-	6.0	-	Gbps
Total jitter before and after compliance interconnect channel	J_T	-	-	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 88. Gen 3i receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	166.6083	167.6667	167.5583	-
Total jitter before and after compliance interconnect channel	J_T	-	-	0.6	UI p-p
Random jitter before compliance interconnect channel	J_R	-	-	0.18	UI p-p

3.16.6 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 47. on page 150, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 44. on page 132.

3.16.6.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, a SerDes reference clock is required on SDn_REF_CLK[1:2]_P and SDn_REF_CLK[1:2]_N pins.

For more information on these specifications, see SerDes reference clocks on page 125.

3.16.6.2 SGMII and SGMII 2.5G DC electrical characteristics

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N), as provided in the SGMII transmitter DC measurement circuit figure as shown below.

Table 89. SGMII DC transmitter electrical characteristics [1, 12, 13]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\|V_{OD}\|_{-max}$	mV	2
Output low voltage	V_{OL}	$\|V_{OD}\|_{-min}/2$	-	-	mV	2
Output differential voltage	$\|V_{OD}\|$	320.0	500.0	725.0	mV	3, 4, 5
Output differential voltage	$\|V_{OD}\|$	293.8	459.0	665.6	mV	3, 4, 6
Output differential voltage	$\|V_{OD}\|$	266.9	417.0	604.7	mV	3, 4, 7
Output differential voltage	$\|V_{OD}\|$	240.6	376.0	545.2	mV	3, 4, 8
Output differential voltage	$\|V_{OD}\|$	213.1	333.0	482.9	mV	3, 4, 9
Output differential voltage	$\|V_{OD}\|$	186.9	292.0	423.4	mV	3, 4, 10
Output differential voltage	$\|V_{OD}\|$	160.0	250.0	362.5	mV	3, 4, 11
Output impedance (differential)	R_O	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. This does not align to DC-coupled SGMII.
3. $|V_{OD}| = |V_{SD_TXn_P} - V_{SD_TXn_N}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
4. The $|V_{OD}|$ value shown in Typ column is based on the condition of XnVDD-Typ, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn_TXn_P and SDn_TXn_N.
5. LNmTECR0[AMP_RED]=0b000000
6. LNmTECR0[AMP_RED]=0b000001
7. LNmTECR0[AMP_RED]=0b000011
8. LNmTECR0[AMP_RED]=0b000010
9. LNmTECR0[AMP_RED]=0b000110 (default)
10. LNmTECR0[AMP_RED]=0b000111
11. LNmTECR0[AMP_RED]=0b010000
12. See Figure 47. on page 150.
13. See Figure 48. on page 151.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

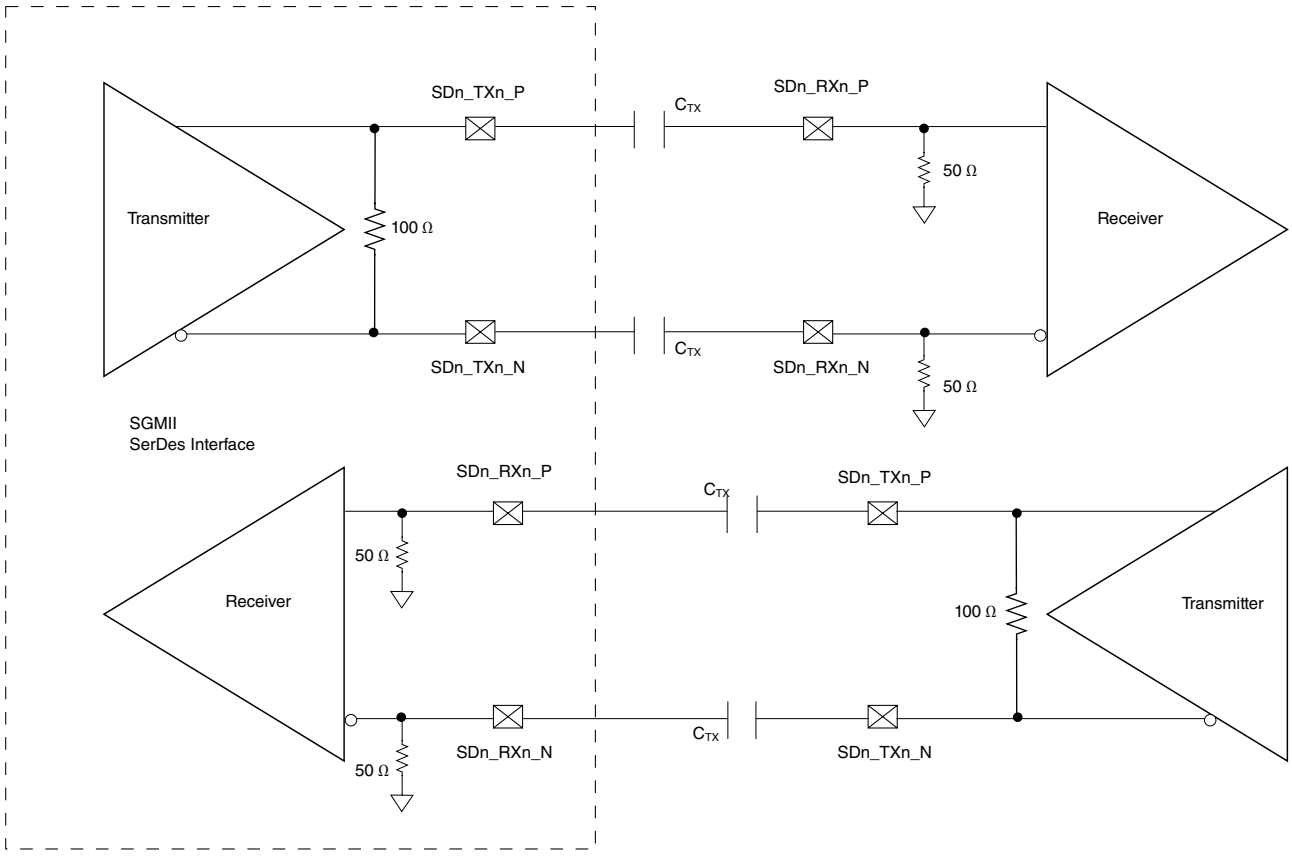


Figure 47. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

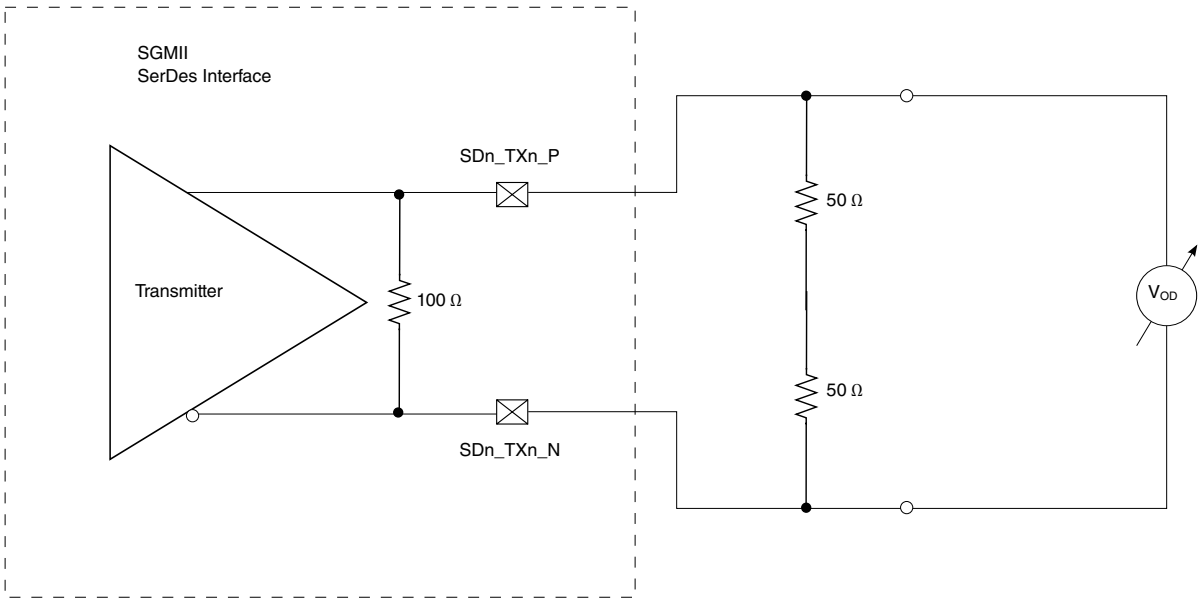


Figure 48. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 90. SGMII 2.5G transmitter DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	-
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 91. SGMII DC receiver electrical characteristics [1]

Parameter	Symbol	Min	Max	Unit	Notes
DC input voltage range	V_{IN}	N/A	N/A	-	2
Input differential voltage (REIDL_TH = 001, default)	$V_{RX_DIFFp\text{-}p}$	100.0	1200.0	mV	3, 4
Input differential voltage (REIDL_TH = 100)	$V_{RX_DIFFp\text{-}p}$	175.0	1200.0	mV	3, 4
Loss of signal threshold (REIDL_TH = 001, default)	V_{LOS}	30.0	100.0	mV	5, 4

Table continues on the next page...

Table 91. SGMII DC receiver electrical characteristics [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Loss of signal threshold (REIDL_TH = 100)	V_{LOS}	65.0	175.0	mV	5, 4
Receiver differential input impedance	Z_{RX_DIFF}	80.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. Input must be externally AC coupled.
3. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The REIDL_TH shown in the table referes to the chip's LNmGCR1[REIDL_TH] bit field.
5. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express.

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 92. SGMII 2.5G receiver DC electrical characteristics [1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX_DIFFp\text{-}p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. For recommended operating conditions, see Recommended Operating Conditions.

3.16.6.3 SGMII and SGMII 2.5G AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 93. SGMII transmitter AC timing specifications [4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	-	-	0.17	UI p-p	-
Total jitter	J_T	-	-	0.35	UI p-p	1
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	2
Unit interval: 3.125 GBaud (2.5G SGMII)	UI	320-100ppm	320.0	320+100ppm	ps	2
AC coupling capacitor	C_{TX}	10.0	-	200.0	nF	3

Table continues on the next page...

Table 93. SGMII transmitter AC timing specifications [4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. See Figure 50. on page 154. 2. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm. 3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output. 4. See Figure 49. on page 153.						

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N) or at the receiver inputs (SDn_RXn_P and SDn_RXn_N) respectively, as shown in this figure.

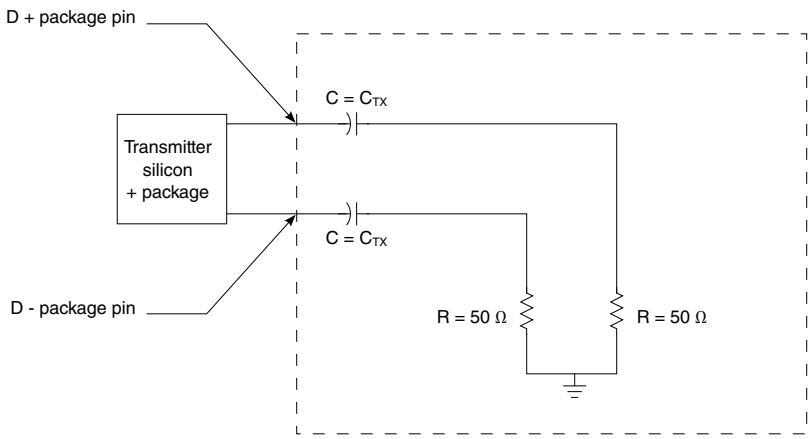


Figure 49. SGMII AC test/measurement load

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. TheAC timing specifications do not include RefClk jitter. Source synchronous clocking is notsupported. Clock is recovered from the data.

Table 94. SGMII receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2, 3
Unit interval: 1.25 GBaud (SGMII)	UI	800-100ppm	800.0	800+100ppm	ps	1
Unit interval: 3.125 GBaud (2.5G SGMII)	UI	320-100ppm	320.0	320+100ppm	ps	1
Bit error ratio	BER	-	-	10^{-12}	-	-

Table continues on the next page...

Table 94. SGMII receiver AC timing specifications [3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1. Measured at receiver. 2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of the Single-frequency sinusoidal jitter limits figure shown below. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects. 3. See Figure 50. on page 154.						

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

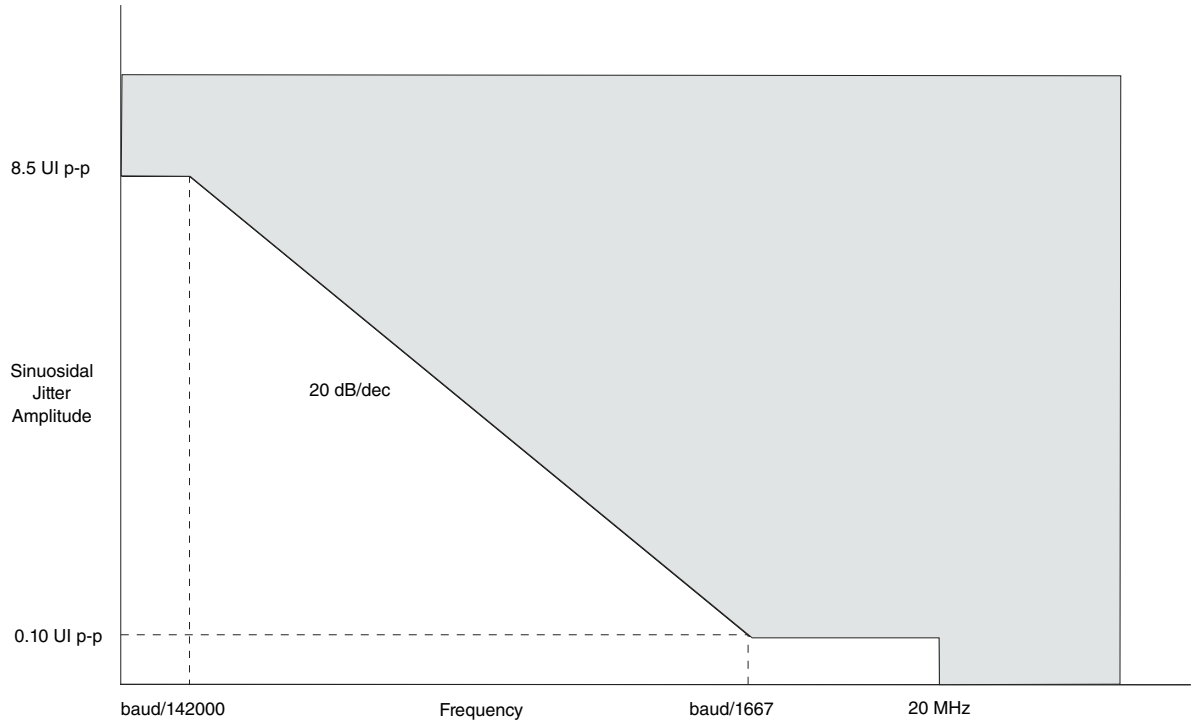


Figure 50. Single-frequency sinusoidal jitter limits

3.16.7 Quad serial media-independent interface (QSGMII)

3.16.7.1 QSGMII clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

For more information on these specifications, see SerDes reference clocks on page 125.

3.16.7.2 QSGMII DC electrical characteristics

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 95. QSGMII transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit
Output differential voltage	V_{DIFF}	400.0	-	900.0	mV
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.					

This table defines the QSGMII receiver DC electrical characteristics.

Table 96. QSGMII receiver DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit
Input differential voltage	V_{DIFF}	100.0	-	900.0	mV
Differential resistance	R_{RDIN}	80.0	100.0	120.0	Ω
1. For recommended operating conditions, see Recommended Operating Conditions.					

3.16.7.3 QSGMII AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 97. QSGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p
Total jitter tolerance	J_T	-	-	0.3	UI p-p

This table provides the QSGMII receiver AC timing specifications.

Table 98. QSGMII receiver AC timing specifications [2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000-100ppm	5.0	5.000+100ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.3	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.0	UI p-p	-

Table continues on the next page...

Table 98. QSGMII receiver AC timing specifications [2] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{TJ}	s -	-	0.6	UI p-p	-

1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. See Figure 51. on page 156.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

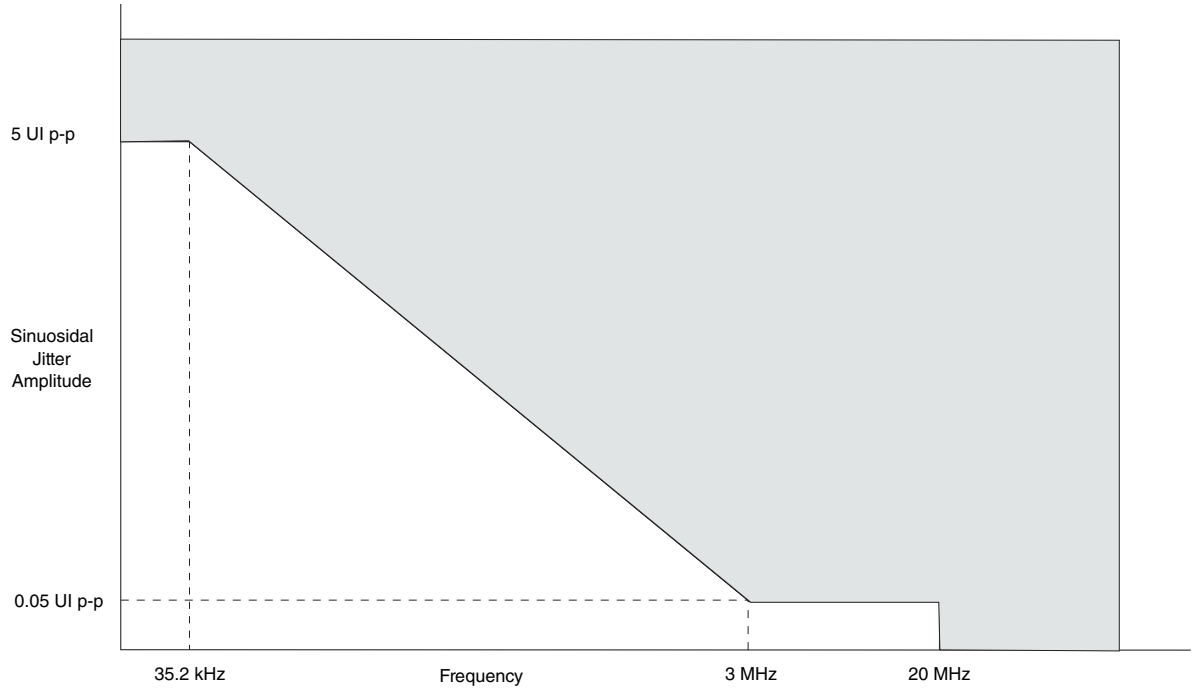


Figure 51. QSGMII single-frequency sinusoidal jitter limits

3.16.8 1000Base-KX

3.16.8.1 1000Base-KX DC electrical characteristics

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SDn_TXn_P and SDn_TXn_N).

Table 99. 1000Base-KX transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800.0	-	1600.0	mV	SRDSxLNmTECR0[AMP_RED]=00_0000
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. SRDSxLNmTECR0[AMP_RED]=00_0000

This tableprovides the 1000Base-KX receiver DC electrical characteristics

Table 100. 1000Base-KX receiver DC electrical characteristics [1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFFp-p}$	-	1600.0	mV
Differential resistance	T_{RDIN}	80.0	120.0	Ω

1. For recommended operating conditions, see Recommended Operating Conditions.

3.16.8.2 1000Base-KX AC timing specifications

This table defines the 1000Base-KX transmitter AC timing specifications.

Table 101. 1000Base-KX transmitter AC timing specifications [2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gbaud	-
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ} / T_{RJ}	-	-	0.15	UI p-p	-
Deterministic jitter tolerance	T_{DJ}	-	-	0.1	UI p-p	-
Total jitter	T_{TJ}	-	-	0.25	UI p-p	1

1. Total jitter is specified at a BER of 10^{-12}.
2. The AC specifications do not include Refclk jitter.

This table defines the 1000Base-KX receiver AC timing specifications.

Table 102. 1000Base-KX receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Baud rate	R_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gbaud	-
Total jitter tolerance	R_{TJ}	-	-	Per IEEE 802.3ap-clause 70.	UI p-p	1
Random jitter	R_{RJ}	-	-	0.15	UI p-p	2
Sinusoidal jitter (maximum)	R_{SJ-max}	-	-	0.1	UI p-p	1

1. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.

2. Random jitter is specified at a BER of 10^{-12}.

3. The AC specifications do not include Refclk jitter.

3.16.9 USXGMII interface (10G-SXGMII and 10G-QXGMII)

3.16.9.1 USXGMII DC electrical characteristics

This table defines the 10G-SXGMII transmitter DC electrical characteristics.

Table 103. 10G-SXGMII transmitter DC electrical characteristics [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800.0	-	1200.0	mV	LNmTECR0[EQ_AMP_RED]= 000000
De-emphasized differential output voltage (ratio at 1.14dB)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	LNmTECR0[EQ_POST1Q]= 00011
De-emphasized differential output voltage (ratio at 3.5dB)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	LNmTECR0[EQ_POST1Q]= 01000
De-emphasized differential output voltage (ratio at 4.66dB)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	LNmTECR0[EQ_POST1Q]= 01010
De-emphasized differential output voltage (ratio at 6.0dB)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	LNmTECR0[EQ_POST1Q]= 01100

Table continues on the next page...

Table 103. 10G-SXGMII transmitter DC electrical characteristics [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
De-emphasized differential output voltage (ratio at 9.5dB)	$V_{TX-DE-RATIO-9.5dB}$	9.0	9.5	10.0	dB	LNmTECR0[EQ_POST1Q]= 10000
Differential resistance	T_{RD}	80.0	100.0	120.0	Ω	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. LNmTECR0[EQ_AMP_RED]= 000000
3. LNmTECR0[EQ_POST1Q]= 00011
4. LNmTECR0[EQ_POST1Q]= 01000
5. LNmTECR0[EQ_POST1Q]= 01010
6. LNmTECR0[EQ_POST1Q]= 01100
7. LNmTECR0[EQ_POST1Q]= 10000

This table defines the 10G-SXGMII receiver DC electrical characteristics.

Table 104. 10G-SXGMII receiver DC electrical characteristics [1]

Parameter	Symbol	Min	Max	Unit
Input differential voltage	$V_{RX-DIFF}$	-	1200.0	mV
Differential resistance	R_{RD}	80.0	120.0	Ω

1. For recommended operating conditions, see Recommended Operating Conditions.

3.16.9.2 USXGMII AC timing characteristics

This table defines the 10G-SXGMII transmitter AC timing specifications. RefClk jitter is not included.

Table 105. 10G-SXGMII transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Uncorrelated high probability jitter/ Random Jitter	T_{UHPJ}/T_{RJ}	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.3	UI p-p

This table defines the 10G-SXGMII receiver AC timing specifications. RefClk jitter is not included.

Table 106. 10G-SXGMII receiver AC timing specifications [3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Total jitter	T_J	-	-	1.0	UI p-p	1, 2
Random jitter	R_J	-	-	0.13	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1

1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max, where ISI is jitter due to frequency dependent loss.
3. TX equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

3.17 I2C

3.17.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I ^{2}C interface.

Table 107. I ^{2}C DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Output low voltage (OV_{DD} = min, IOL = 2 mA, $OV_{DD} \le$ 2V)	V_{OL}	0.0	0.36	V	-
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0.0	50.0	ns	3
Input current each I/O pin (input voltage is between 0.1 x OV_{DD} (min) and 0.9 x OV_{DD} (max))	I_I	-	±50	μA	4
Capacitance for each I/O pin	C_I	-	10.0	pF	-

1. For recommended operating conditions, see Recommended Operating Conditions.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if the supply is switched off.

3.17.2 I2C AC timing specifications

This table provides the AC timing specifications for the I ^{2}C interface.

Table 108. I ^{2}C AC timing specifications [3, 4, 5]

Parameter	Symbol	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0.0	400.0	kHz	-
Low period of the SCL clock	t_{I2CL}	1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	µs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	µs	-
Data setup time	t_{I2DVKH}	100.0	-	ns	-
Data input hold time (CBUS compatible masters, I ^{2}C bus devices)	t_{I2DXKL}	0.0	-	µs	1
Data output delay time	t_{I2OVKL}	-	0.9	µs	2
Setup time for STOP condition	t_{I2PVKH}	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	-	µs	-
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x OV_{DD}	-	V	-
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x OV_{DD}	-	V	-
Capacitive load for each bus line	Cb	-	400.0	pF	-

Table continues on the next page...

Table 108. I ^{2}C AC timing specifications [3, 4, 5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I ^{2}C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. 2. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal. 3. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I ^{2}C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. 4. See Figure 52. on page 162. 5. See Figure 53. on page 162.					

This figure shows the AC test load for the I2C.

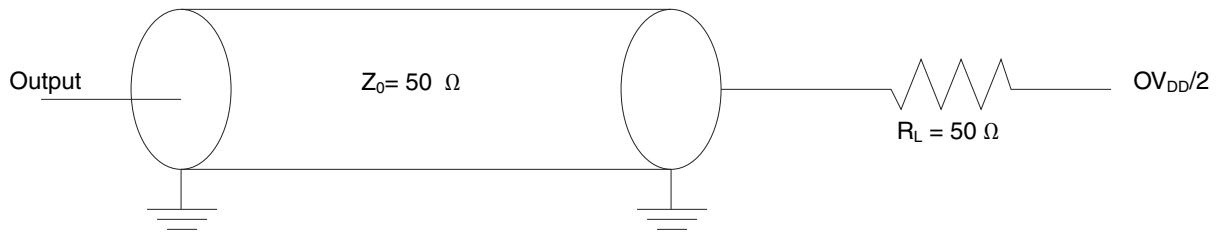


Figure 52. I ^{2}C AC test load

This figure shows the AC timing diagram for the I ^{2}C bus.

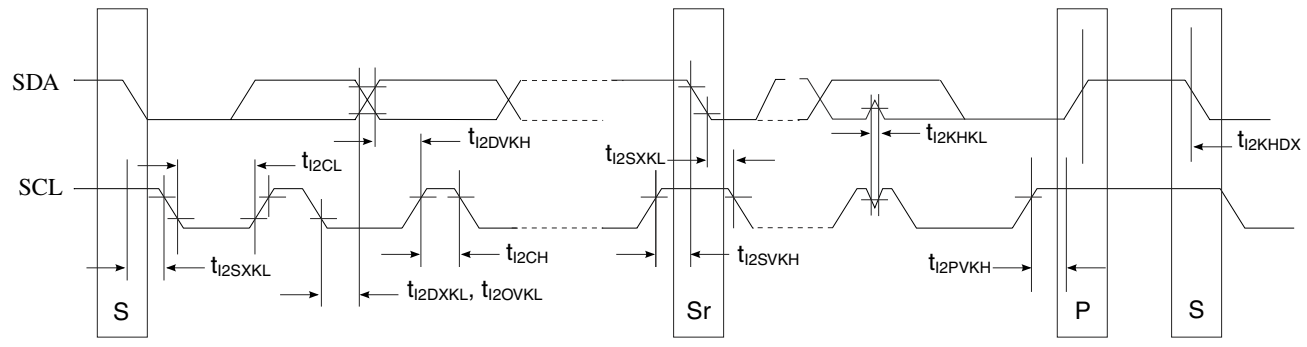


Figure 53. I ^{2}C bus AC timing diagram

3.18 JTAG

This section describes the DC and AC electrical specifications for the JTAG (IEEE 1149.1) interface.

3.18.1 JTAG DC electrical characteristics

This table provides the DC electrical characteristics for the JTAG (IEEE 1149.1) interface.

Table 109. JTAG DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	-100/+50	µA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.18.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 54. on page 164, Figure 55. on page 165, Figure 56. on page 165, and Figure 57. on page 165.

Table 110. JTAG AC timing specifications [3, 4, 5, 6, 7]

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	F_{JTG}	0.0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30.0	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15.0	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0.0	2.0	ns	-
TRST_B assert time	t_{TRST}	25.0	-	ns	1
Input setup times	t_{JTDVKH}	4.0	-	ns	-

Table continues on the next page...

Table 110. JTAG AC timing specifications [3, 4, 5, 6, 7] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input hold times	t_{JTDXKH}	10.0	-	ns	-
Output valid times: boundary-scan data	t_{JTKLDV}	-	15.0	ns	2
Output valid times: TDO	t_{JTKLDV}	-	10.0	ns	2
Output hold times	t_{JTKLDX}	0.0	-	ns	2

1. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

2. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

3. The symbols used for timing specifications follow these patterns: t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, tJTDXKH symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

4. See Figure 54. on page 164.

5. See Figure 55. on page 165.

6. See Figure 56. on page 165.

7. See Figure 57. on page 165.

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

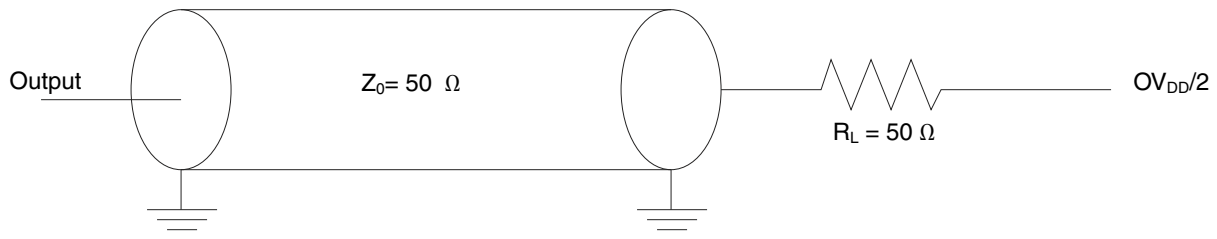


Figure 54. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

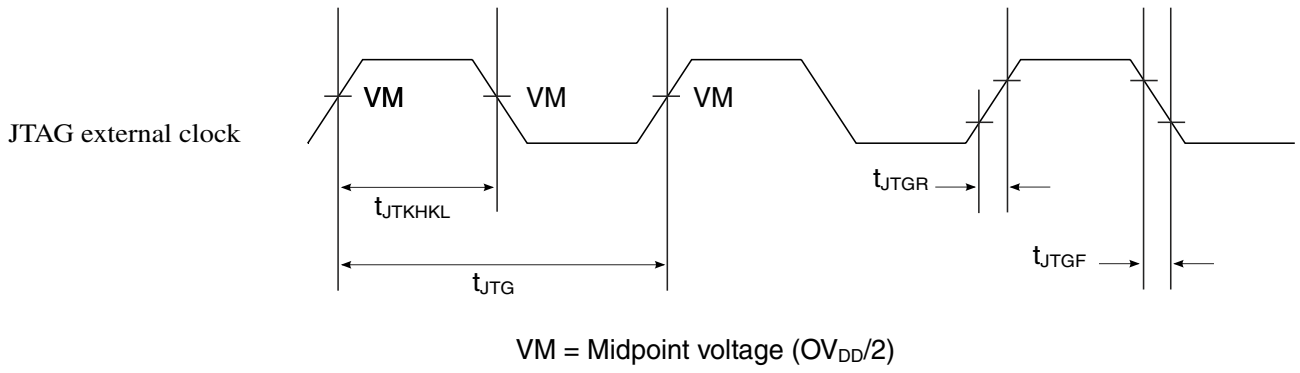


Figure 55. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

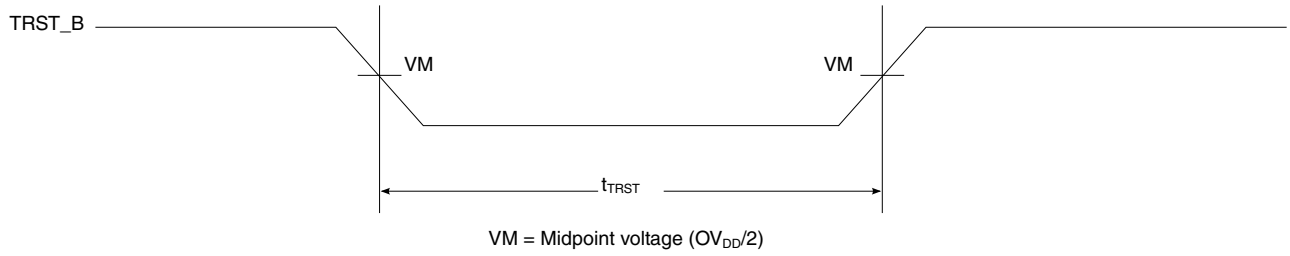


Figure 56. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

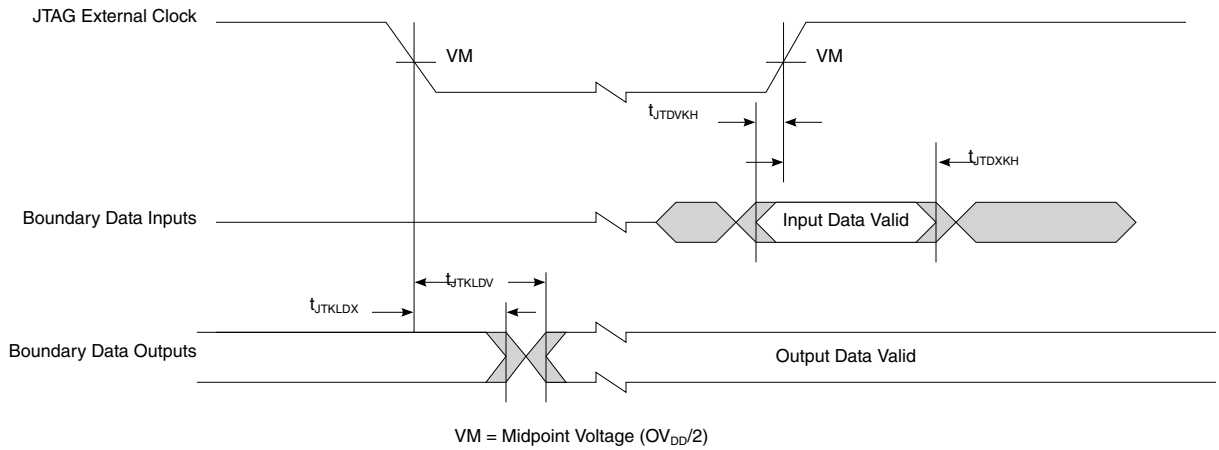


Figure 57. Boundary-scan timing diagram

3.19 Synchronous Audio Interface (SAI)

This section describes the DC and AC electrical specifications for the SAI interface.

3.19.1 SAI DC electrical characteristics

This table provides the DC electrical characteristics for the SAI/I ^{2}S interface.

Table 111. SAI/I ^{2}S DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current ($L1V_{IN}$ = 0V or $L1V_{IN}$ = OV_{DD})	I_{IN}	-	±50	μA	3, 4
Output high voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	1.35	-	V	4
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	4

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

4. The symbol OV_{DD} represents the recommended operating voltage of the supply referenced in Recommended Operating Conditions.

3.19.2 SAI AC timing specifications

This table provides the SAI/I^{2}S timing in slave mode (clocks input).

Table 112. Slave mode SAI/I^{2}S timing [1]

Parameter	Symbol	Min	Max	Unit
SAIn_TX_BCLK/SAIn_RX_BCLK cycle time (input)	t_{SAIC}	20.0	-	ns
SAIn_TX_BCLK/SAIn_RX_BCLK pulse width high/low (input)	$t_{SAIL/tSAIH}$	35%	65%	BCLK period
SAIn_TX_BCLK to SAIn_TX_DATA / SAIn_TX_SYNC output valid	$t_{SAISLOV}$	-	20.0	ns
SAIn_TX_BCLK to SAIn_TX_DATA/ SAIn_TX_SYNC output invalid	$t_{SAISLOX}$	0.0	-	ns

Table continues on the next page...

Table 112. Slave mode SAI/I²S timing [1] (continued)

Parameter	Symbol	Min	Max	Unit
SAIn_RX_DATA setup before SAIn_RX_BCLK	$t_{SAIMVKH}$	10.0	-	ns
SAIn_RX_DATA hold after SAIn_RX_BCLK	$t_{SAISXKH}$	2.1	-	ns
SAIn_RX_SYNC input setup before SAIn_RX_BCLK	$t_{SAISFSVKH}$	10.0	-	ns
SAIn_RX_SYNC input hold after SAIn_RX_BCLK	$t_{SAISFSXKH}$	2.1	-	ns

1. See Figure 58. on page 167.

This figure shows the SAI timing in slave modes.

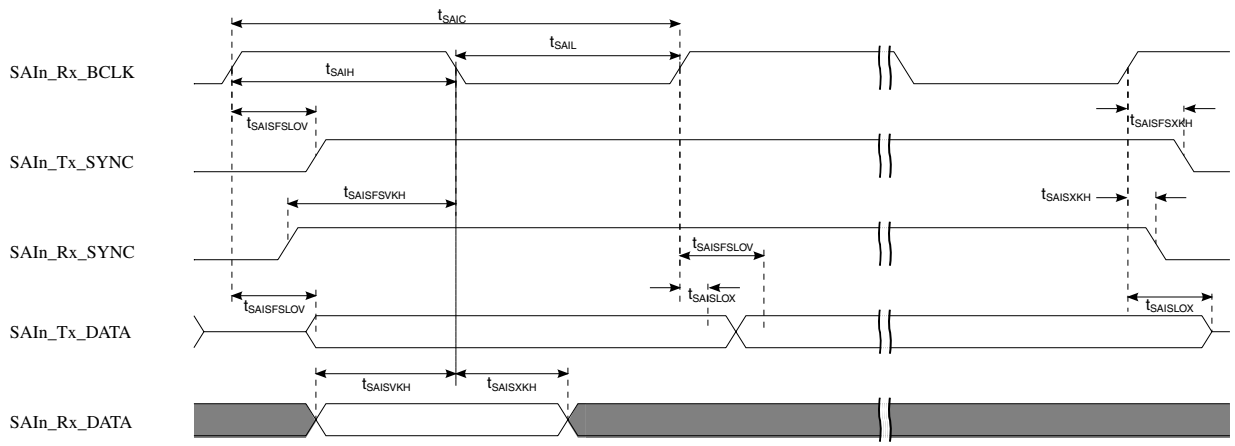


Figure 58. SAI timing - slave modes

3.20 Serial peripheral interface (SPI)

3.20.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface.

Table 113. SPI DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3

Table continues on the next page...

Table 113. SPI DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (I_{OH} = -100 µA)	V_{OH}	0.85xOV_{DD}	-	V	-
Output low voltage (I_{OH} = 100 µA)	V_{OL}	-	0.15xOV_{DD}	V	-

1. For recommended operating conditions, see Recommended Operating Conditions.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions.

3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.

3.20.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 114. SPI AC timing specifications [5, 6, 7, 8]

Parameter	Symbol	Min	Max	Unit	Notes
SCK cycle time	t_{SCK}	t_{SYS} x 2	-	ns	-
SCK clock pulse width	t_{SDC}	40.0	60.0	%	-
CS to SCK delay	t_{CSC}	tp*2 - 2.51	-	ns	1, 2, 3
After SCK delay	t_{ASC}	tp*2 - 0.23	-	ns	1, 2, 3
Slave access time (SS active to SOUT driven)	t_A	-	15.0	ns	4
Slave disable time (SS inactive to SOUT High-Z or invalid)	t_{DI}	-	10.0	ns	4
Data setup time for inputs	t_{NIIVKH}	9.0	-	ns	1
Data setup time for inputs	t_{NEIVKH}	4.0	-	ns	4
Data hold time for inputs	t_{NIIXKH}	0.0	-	ns	1
Data hold time for inputs	t_{NEIXKH}	2.0	-	ns	4
Data valid (after SCK edge) for outputs	t_{NIKHOV}	-	5.0	ns	1
Data valid (after SCK edge) for outputs	t_{NEKHOV}	-	10.0	ns	4
Data hold time for outputs	t_{NIKHOX}	0.0	-	ns	1
Data hold time for outputs	t_{NEKHOX}	0.0	-	ns	4

Table continues on the next page...

Table 114. SPI AC timing specifications [5, 6, 7, 8] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. Master mode					
2. Refer the CTARx register in QorIQ LS1028ARM for more details					
3. tp is the input clock period for the SPI controller.					
4. Slave mode					
5. See Figure 59. on page 169.					
6. See Figure 60. on page 170.					
7. See Figure 61. on page 171.					
8. See Figure 62. on page 172.					

This figure shows the SPI timing master when CPHA = 0.

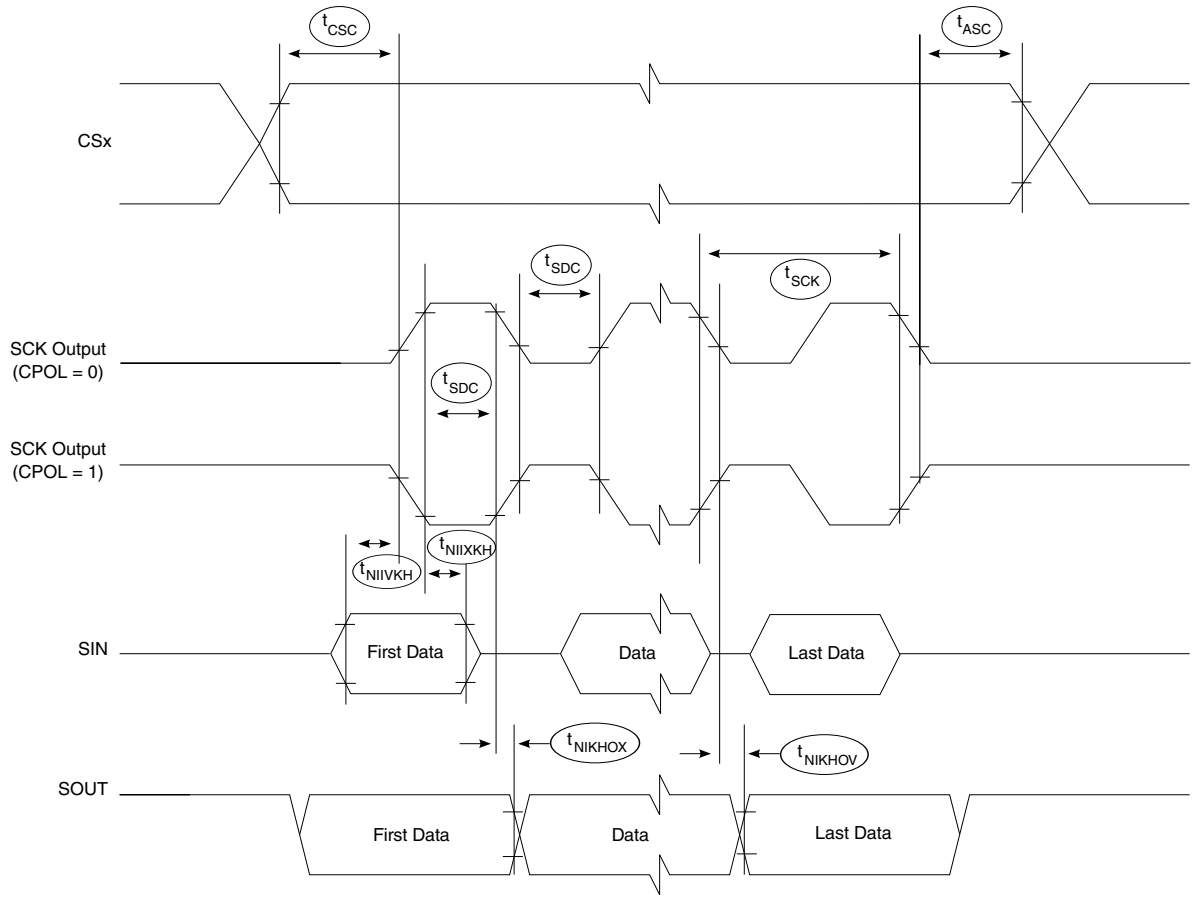


Figure 59. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

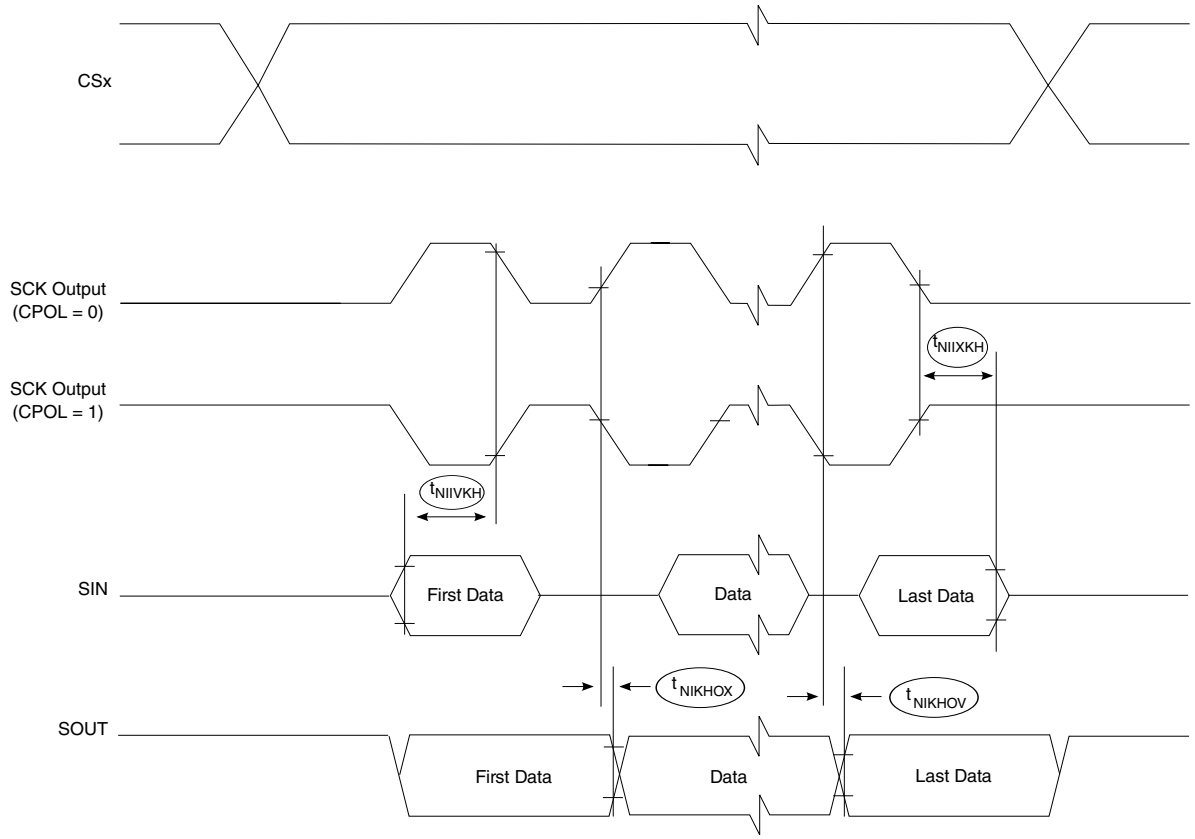


Figure 60. SPI timing master, CPHA = 1

This figure shows the SPI timing slave when CPHA = 0.

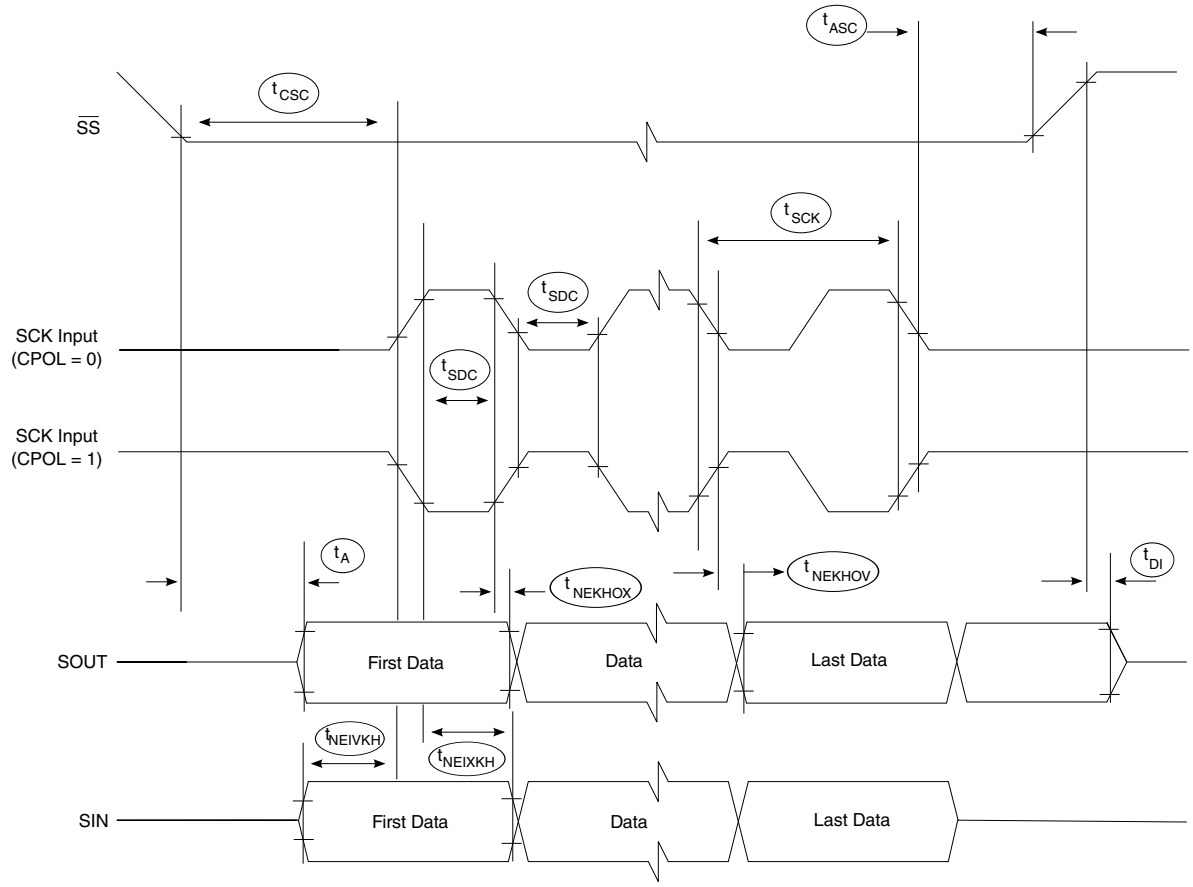


Figure 61. SPI timing slave, CPHA = 0

This figure shows the SPI timing slave when CPHA = 1.

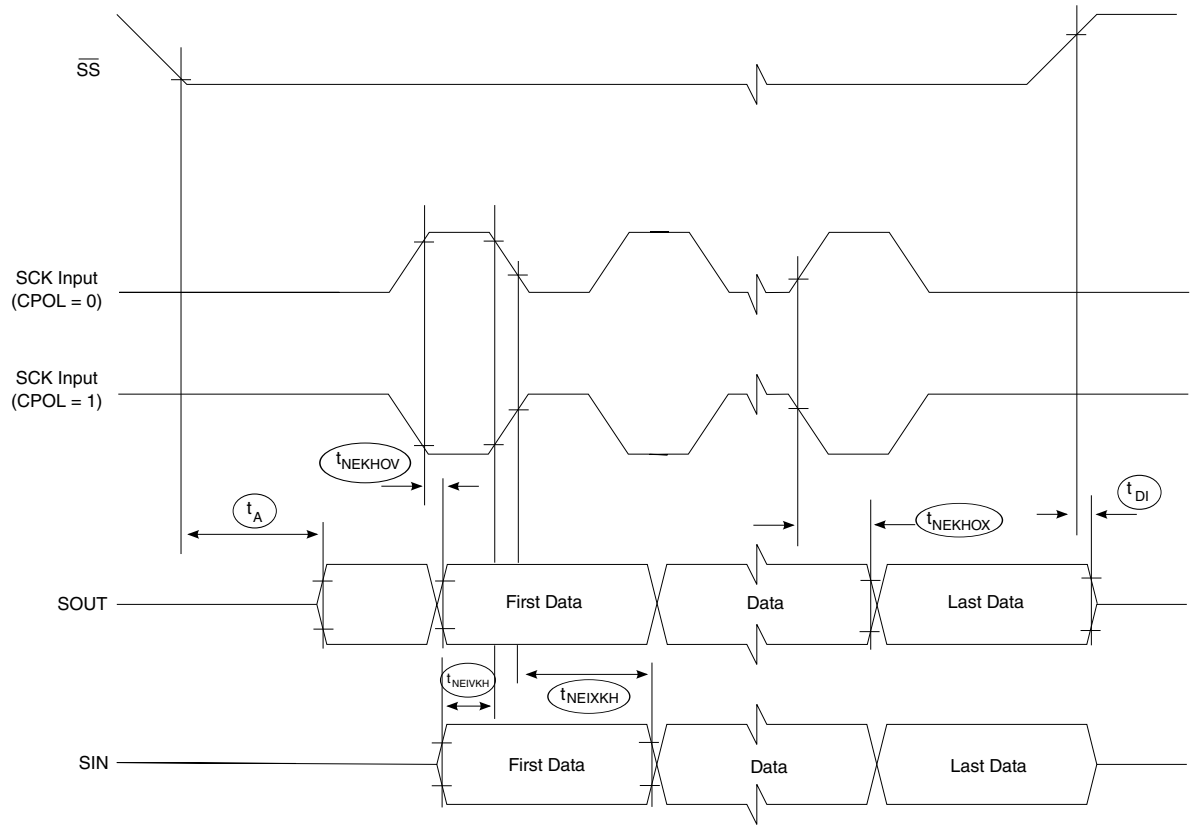


Figure 62. SPI timing slave, CPHA = 1

3.21 Universal asynchronous receiver/transmitter (UART)

3.21.1 UART DC electrical characteristics

The table below provides the DC electrical characteristics for the DUART interface.

Table 115. DUART DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (I_{OL} = 0.5 mA)	V_{OL}	-	0.45	V	-

Table continues on the next page...

Table 115. DUART DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.21.2 UART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 116. DUART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Minimum baud rate	baud	f_{PLAT}/(2 x 1,048,576)	-	baud	1, 2
Maximum baud rate	baud	-	f_{PLAT}/(2 x 16)	baud	1, 3
1. f_{PLAT} refers to the internal platform clock. 2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample. 3. The actual attainable baud rate is limited by the latency of interrupt processing.					

3.22 Low power Universal asynchronous receiver/transmitter (LPUART)

3.22.1 LPUART DC electrical characteristics

This table provides the DC electrical characteristics for the LPUART interface.

Table 117. LPUART DC electrical characteristics (OV_{DD} = 1.8V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	2
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-	±50	μA	3
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 117. LPUART DC electrical characteristics (OV_{DD} = 1.8V) [1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Recommended Operating Conditions. 3. The symbol OV_{IN} represents the input voltage of the supply referenced in Recommended Operating Conditions.					

3.22.2 LPUART AC timing specifications

This table provides the AC timing specifications for the LPUART interface.

Table 118. LPUART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Minimum baud rate	baud	f_{PLAT}/(2 x 32 x 8192)	-	baud	1, 2, 3
Maximum baud rate	baud	-	f_{PLAT}/(2 x 16)	baud	1, 4, 3
1. f_{PLAT} refers to the internal platform clock. 2. Every bit can be over sampled with a sample clock rate of 8 and 64 times (software configurable) and each bit is the majority of the values sampled at the sample rate divided by two, (sample rate/2)+1 and (sample rate/2)+2. 3. The 1-to-0 transition during a data word can cause a resynchronization of the sample point. 4. The actual attainable baud rate is limited by the latency of interrupt processing.					

3.23 Universal serial bus 3.0 (USB)

3.23.1 USB 3.0 DC electrical characteristics

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at respective supply = 3.3 V.

Table 119. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	2
Input low voltage	V_{IL}	-	0.8	V	2
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2mA)	V_{OH}	2.8	-	V	-
Output low voltage (USB_HV_{DD} = min, I_{OH} = 2mA)	V_{OL}	-	0.3	V	-
1. For recommended operating conditions, see Recommended Operating Conditions. 2. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Recommended Operating Conditions.					

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 120. USB 3.0 transmitter DC electrical characteristics (USB_HV $_{DD}$ = 3.3V) [1]

Parameter	Symbol	Min	Typ	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800.0	1000.0	1200.0	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400.0	-	1200.0	$mV_{p\text{-}p}$
Transmit de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3.0	-	4.0	dB
Differential impedance	Z_{diffTX}	72.0	100.0	120.0	Ω
Transmit common mode impedance	$R_{TX\text{-}DC}$	18.0	-	30.0	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	-	-	200.0	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0.0	-	10.0	mV

1. For recommended operating conditions, see Recommended Operating Conditions.

This table provides the USB 3.0 receiver DC electrical characteristics at the Rx package pins.

Table 121. USB 3.0 receiver DC electrical characteristics (USB_HV $_{DD}$ = 3.3V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential receiver input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72.0	100.0	120.0	Ω	-
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18.0	-	30.0	Ω	-
DC input CM input impedance for V > 0 during reset or power down	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	25000.0	-	-	Ω	-
LFPS detect threshold	$V_{TRX\text{-}IDLE\text{-}DET\text{-}DC\text{-}DIFFpp}$	100.0	-	300.0	mV	2

1. For recommended operating conditions, see Recommended Operating Conditions.

2. Below the minimum is noise. Must wake up above the maximum.

3.23.2 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 122. USB 3.0 transmitter AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Speed	f_{USB}	-	5.0	-	Gb/s	-
Transmitter eye	T_{TX-EYE}	0.625	-	-	UI	-
Unit Interval	UI	199.94	200.0	200.06	ps	1
AC coupling capacitor	AC_{CAP}	75.0	-	200.0	nF	-

1. UI does not account for SSC-caused variations.

This table provides the USB 3.0 receiver AC timing specifications at the Rx package pins.

Table 123. USB 3.0 receiver AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	UI	199.94	200.0	200.06	ps	1

1. UI does not account for SSC-caused variations.

This table provides the key LFPS electrical specifications at the transmitter.

Table 124. LFPS electrical specifications at the transmitter [2]

Parameter	Symbol	Min	Max	Unit	Notes
Period	t_{Period}	20.0	100.0	ns	-
Peak-to-peak differential amplitude	$V_{tx-diff-pp-lfps}$	800.0	1200.0	mV	-
Rise/fall time	$t_{rise/fall}$	-	4.0	ns	1
Duty cycle	DC_{LFPS}	40.0	60.0	%	1, 2

1. Measured at compliance TP1. See the Transmit normative setup figure below for details.
2. See Figure 63. on page 176.

This figure shows the transmit normative setup with reference channel as per USB 3.0 specifications.

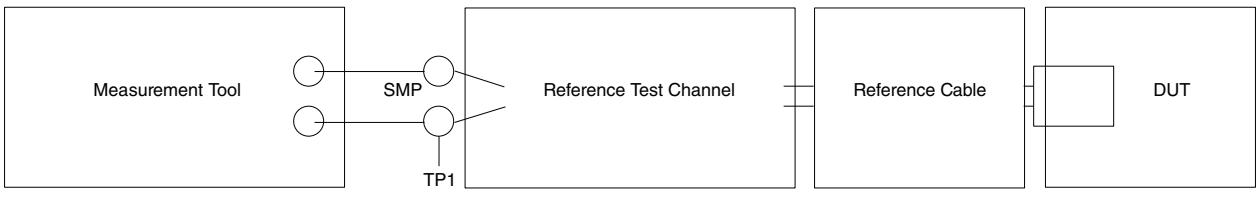


Figure 63. Transmit normative setup

4 Hardware design considerations

4.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, ENETC and GPU & LCD controller.

Table 125. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency								Unit	Notes
	800 MHz		1000 MHz		1300 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	600	800	600	1000	600	1300	600	1500	MHz	1, 3, 4
Core frequency	300	800	300	1000	300	1300	300	1500	MHz	1, 3, 4
Platform clock frequency	300	300	300	400	300	400	300	400	MHz	1
GPU and LCD controller frequency	400	400	400	500	400	650	400	700	MHz	5
Memory bus clock frequency	650	650	650	800	650	800	650	800	MHz	1, 2
ENETC frequency	400	400	400	400	400	400	400	400	MHz	6

Notes:

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

2. The memory bus clock speed is half the DDR3L/DDR4 data rate.

3. For supported voltage/frequency options, see the orderable part list of QorIQ LS1028A Multicore Communications Processors at www.nxp.com.

4. The core cluster can run at cluster group PLL/1, PLL/2 and PLL/4. For the PLL/1 case, the minimum frequency is 600 MHz. For PLL/2 case, the minimum frequency is 400 MHz. The minimum frequency provided to the core cluster after any dividers must always be greater than or equal to the platform frequency. For the case of the minimum platform frequency = 300 MHz, the minimum core cluster frequency is 300 MHz.

5. GPU will run on CGA_PLL2 for 700MHz.

6. For the case of the minimum platform frequency = 300 MHz, ENETC frequency will be a divide by option of CGA PLLn

5 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates.

Table 126. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to Case Thermal Resistance	—	$R_{\Theta JC}$	0.54	°C/W	1

Notes:

1. Junction-to-Case thermal resistance is determined using an isothermal cold plate heat extraction model. Case temperature is the surface temperature at the package lid top side centre.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature by using some external temperature monitoring devices (such as ADT7481A™).

The following are the specifications of the chip temperature diodes:

- Operating range: 10 - 230 µA
- Ideality factor over temperature range 85°C - 125°C, n = 1.006 ± 0.003, with approximate error ± 1°C and error under ± 3°C for temperature range 0°C - 85°C.

5.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 64. on page 178. The heat sink should be attached to the printed-circuit board with the spring force centered over the lid.

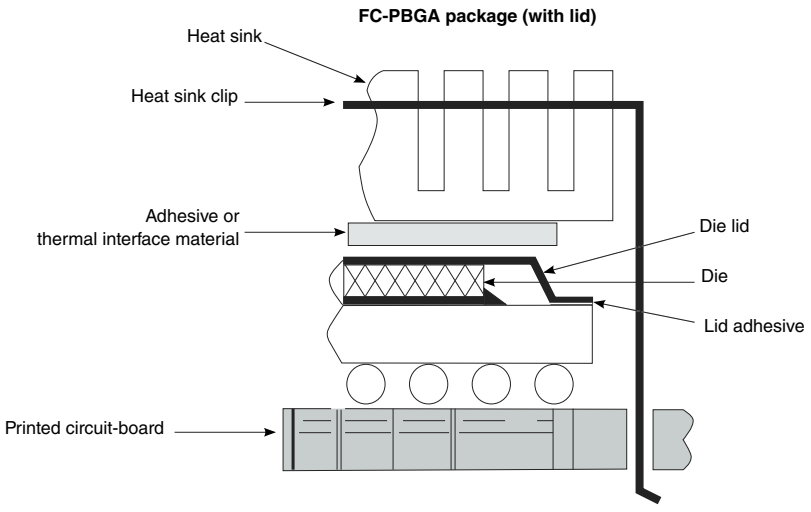


Figure 64. Package exploded, cross-sectional view-FC-PBGA (w/ Lid)

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6 Package information

6.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 17mm x 17mm, 448 flip-chip, plastic-ball grid array.

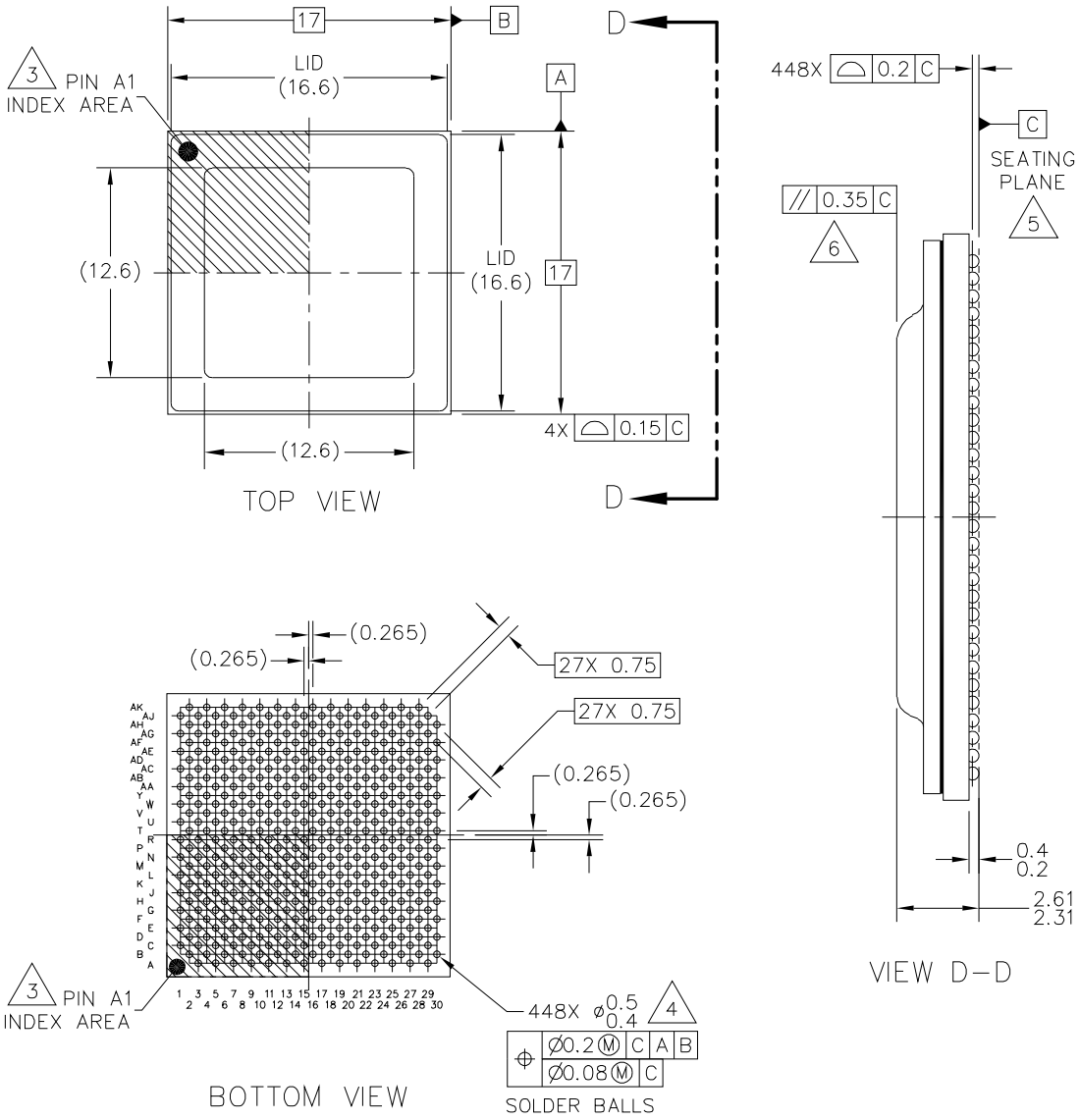
- Package outline - 17 mm x 17 mm
- Interconnects - 448
- Ball Pitch - 0.75 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, and 0.5% Cu
- Module height (typical) - 2.31 (minimum), 2.46 mm (typical), 2.61 mm (maximum)

6.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

H-FC-PBGA-448 I/O
17 X 17 X 2.46 PKG, 0.75 PITCH

SOT1908-1



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DATE: 04 JUN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01058D	REVISION: B	PAGE: 1

Figure 65. Mechanical dimensions of the FC-PBGA (with lid)

Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M - 1994.
3. Pin A1 feature shape, size and location may vary.
4. Maximum solder ball diameter measured parallel to datum C.
5. Datum C, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Lid overhang on substrate not allowed.

7 Security fuse processor

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.80 V to the TA_PROG_SFP pin per Power sequencing on page 68. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of six fuse programming cycles. All other times TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 9. on page 70. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Recommended Operating Conditions.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

8.1 Part numbering nomenclature

This table provides the NXP QorIQ platform part numbering nomenclature.

Table 127. Part numbering nomenclature

p	ls	n	nn	n	x	t	e	n	c	d	r
Qual Status	Generation	Performance Level	Number of Virtual cores	Unique ID	Core Type	Temperature Range	Encryption	Package Type	CPU Speed[1]	DDR Data Rate	Die Revision
P="Pre-qual" Blank="Qualified"	LS = Layerscape	1	02 = Two Cores 01 = One Core	8 = GPU	A = ARM	S = Standard temp X = Extended temp Y = High Extended temp C = AEC Q100 Grade 3 Stresses	E = Export controlled crypto hardware enabled N = Export controlled crypto hardware disabled	7 = FCPBGA C4 PbFree	H = 800 MHz K = 1000 MHz N = 1300 MHz P = 1500 MHz	N = 1300 MT/s Q = 1600 MT/s	A = Rev 1.0

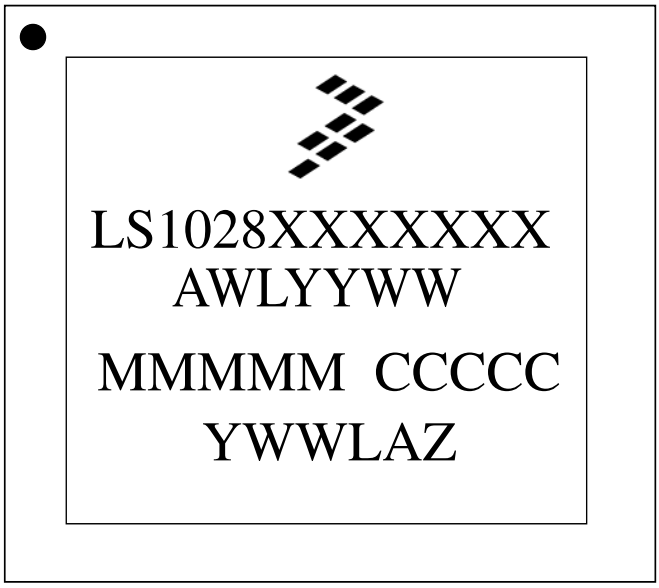
1. For the LS1028A family of devices, parts marked with "H" require 0.9 V operating voltage.

2. For the LS1028A family of devices, parts marked with "Y" are available with CPU speed 800MHz only.

3. For the LS1028A family of devices, parts marked with "C" require 1.0 V operating voltage.

8.1.1 Part marking

Parts are marked as in the example shown in this figure.



Legend:
LS1028XXXXXXX is the orderable part number
AWLYYWW is the test traceability code
MMMMM is the mask number
CCCCC is the country code
YWWLAZ is the assembly traceability code

Figure 66. Part marking for FC-PBGA chip LS1028A

9 Revision history

This table summarizes revisions to this document.

Table 128. Revision history

Revision	Date	Description
0	12/2019	Initial release

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