THE DATASHEET OF

MP3418GJ-Z

www.win-source.net 0086-755-83957316

MP3418

400mA, 1.2MHz, Synchronous, Step-up Converter with Output Disconnect

The Future of Analog IC Technology

DESCRIPTION

The MP3418 is a high-efficiency, synchronous, current–mode, step-up converter with output disconnect.

The MP3418 can start up from an input voltage as low as 0.8V to provide inrush current limiting, and output short-circuit protection. The integrated, P-channel, synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The PMOS disconnects the output from the input when the part shuts down. This output disconnect feature allows the output to be completely discharged, thus allowing the part to draw less than 1μA in shutdown mode.

The 1.2MHz switching frequency allows for smaller external components, while the internal compensation and the soft-start minimize the external component count: these feature help to produce a compact solution for a wide current load range.

The MP3418 is available in a small 8-pin TSOT23 package.

FEATURES

- Up to 96% Efficiency
- 0.8V Low Voltage Start-Up
- 0.6V-to-4V Input Range
- 1.8V-to-4V Output Range
- Internal Synchronous Rectifier
- 1.2MHz Fixed-Frequency Switching
- Typical 38μA Quiescent Current
- Typical 0.1μA Shutdown Current
- Current-Mode Control with Internal Compensation
- True Output Disconnect from Input
- V_{IN}>V_{OUT} Down Mode Operation
- High Efficiency under Light-Load Conditions
- Very Small External Components
- Inrush Current Limiting and Internal Soft-Start
- Over-Voltage Protection
- Short-Circuit Protection
- TSOT23-8 Package

APPLICATIONS

- Battery-Powered Products
- Personal Medical Devices
- Portable Media Players
- Wireless Peripherals
- Handheld Computers and Smartphones

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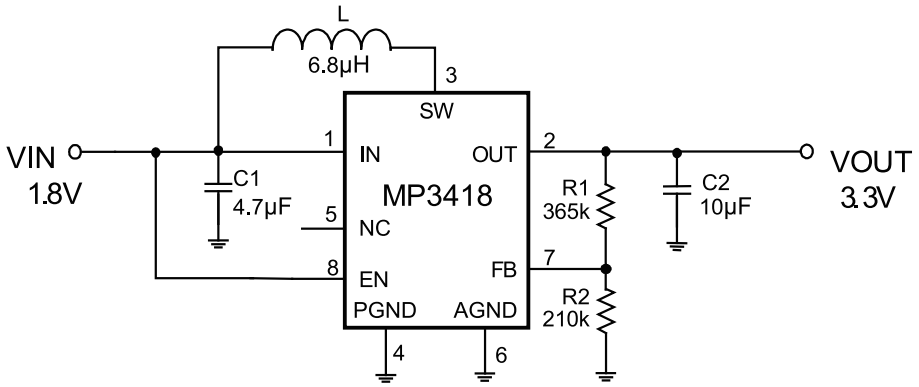
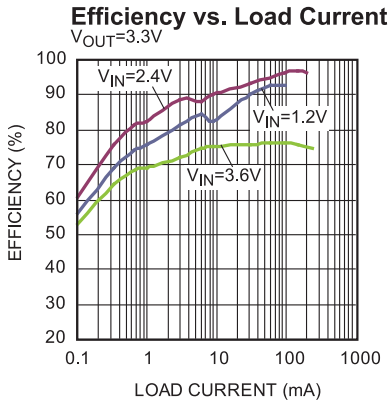
TYPICAL APPLICATION CIRCUIT





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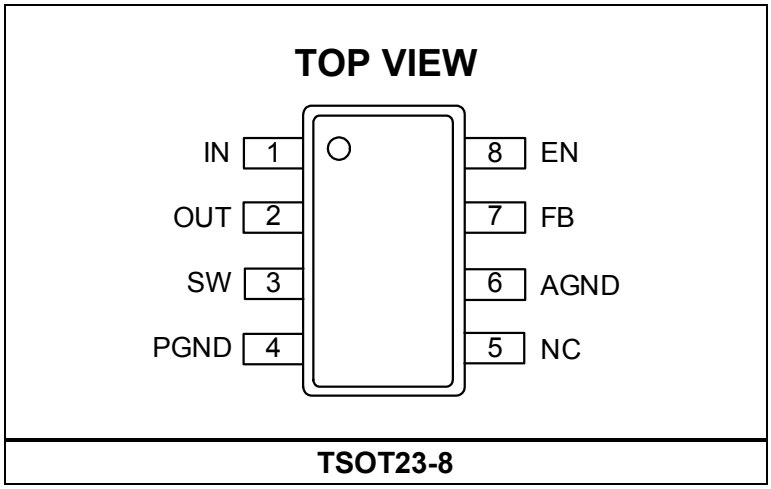
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3418GJ	TSOT23-8	AET

* For Tape & Reel, add suffix –Z (e.g. MP3418GJ–Z);

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

SW Pin, OUT Pin ..... -0.5V to +6.5V
All other Pins ..... -0.5V to +6V
Continuous Power Dissipation (T_A = 25°C) (2) 1.25W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Start-up Voltage V_{ST} ..... 0.8V to 4V
Supply Voltage V_{IN} ..... 0.6V to 4V
V_{OUT} ..... 1.8V to 4V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8 ..... 100 ..... 55 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 1.8V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Minimum Startup Voltage	V_{ST}			0.8	1.0	V
Operating Input Voltage	V_{IN}		0.6		4	V
Output Voltage Adjust Range	V_{OUT}		1.8		4.0	V
Quiescent Current	I_{QNS}	V_{EN}=V_{IN}=1.8V, V_{OUT}=3.3V, no load, Measured on OUT pin		38	50	μA
Shutdown Current	I_{SD}	V_{EN}=V_{OUT}=0V, Measured on IN pin		0.1	1	μA
IN Under-Voltage Lockout	V_{UVLO}	V_{IN} Rising	0.4	0.5	0.6	V
Operation Frequency	f_{SW}		1.0	1.2	1.4	MHz
Feedback Voltage	V_{FB}		1.19	1.21	1.23	V
Feedback Input Current	I_{FB}	V_{FB}=1.25V		1	50	nA
NMOS On-Resistance	R_{NDS_ON}			110		mΩ
NMOS Leakage Current	I_{N_LK}	V_{SW}=6.5V		0.1	1	μA
PMOS On-Resistance	R_{PDS_ON}			120		mΩ
PMOS Leakage Current	I_{P_LK}	V_{SW}=6.5V, V_{OUT}=0V		0.1	1	μA
Maximum Duty Cycle	D_{MAX}		85	90		%
Startup Current Limit	I_{ST_LIMIT}			200		mA
NMOS Current Limit	I_{SW_LIMIT}		300	400	500	mA
EN Input High Level	V_{EN_H}		0.7			V
EN Input Low Level	V_{EN_L}				0.1	V
EN Input Current	I_{EN}	Connect to V_{IN}	0.6	1.2	2	uA
Thermal Shutdown(5)				150		°C
Over Temperature Hysteresis(5)				20		°C

Notes:

5）Guaranteed by design, not tested

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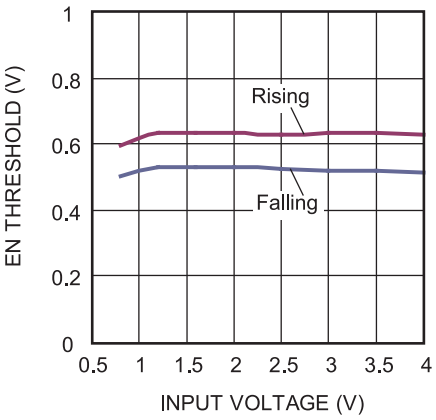
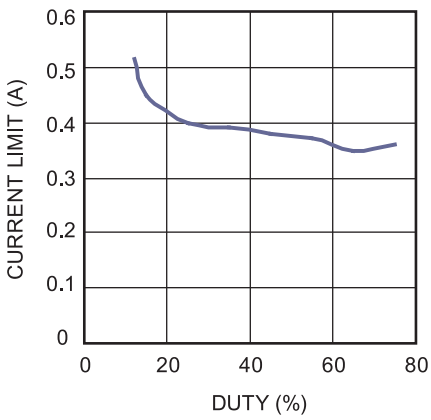
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 2.4V, V_{OUT} = 3.3V, L = 6.8µH, C_{OUT}=10uF, T_A = 25°C, unless otherwise noted.

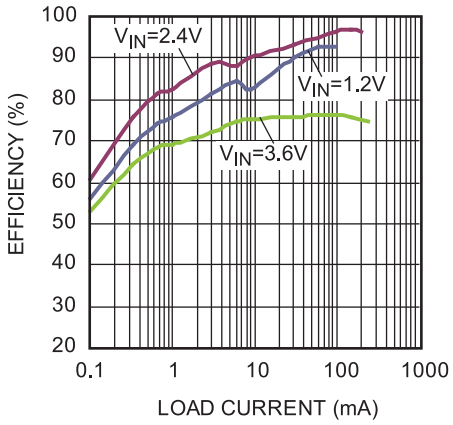
EN Threshold vs. Input Voltage



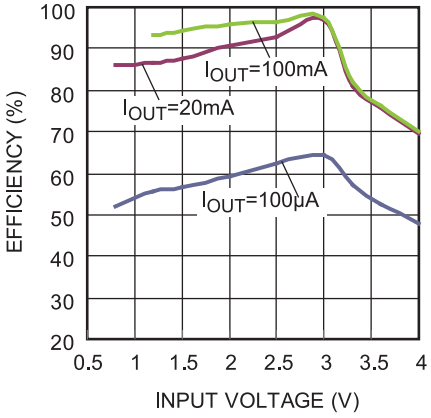
Current Limit vs. Duty



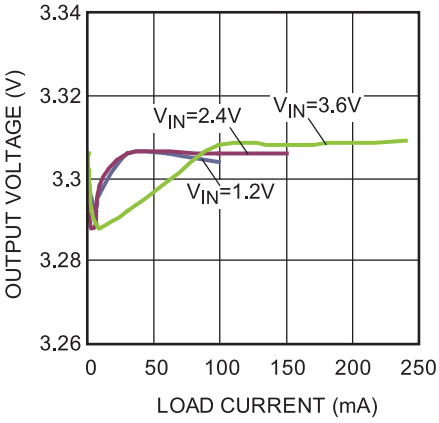
Efficiency vs. Load Current



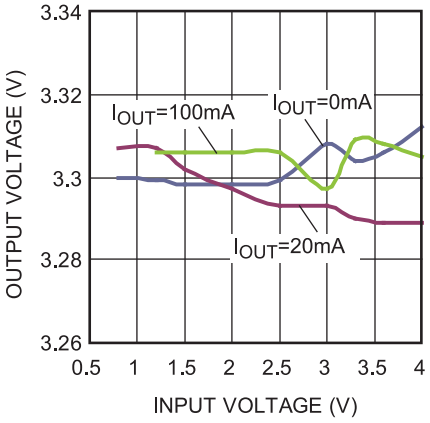
Efficiency vs. Input Voltage



Load Regulation



Line Regulation



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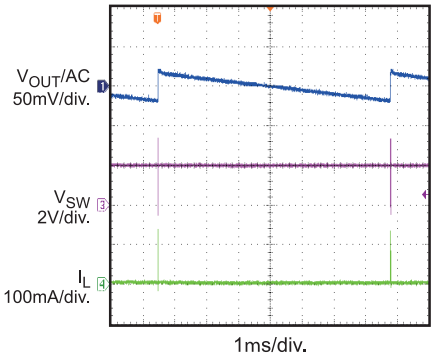
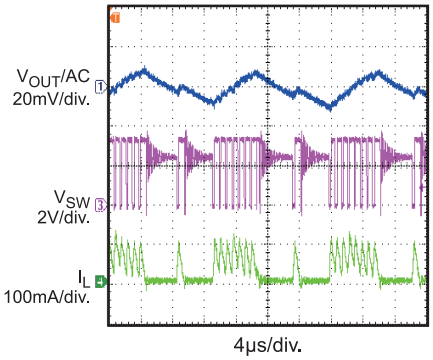
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 2.4V, V_{OUT} = 3.3V, L = 6.8µH, C_{OUT}=10uF, T_A = 25°C, unless otherwise noted.

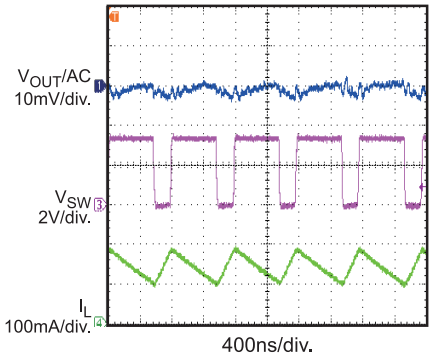
Output Voltage Ripple
I_{OUT} = 0mA



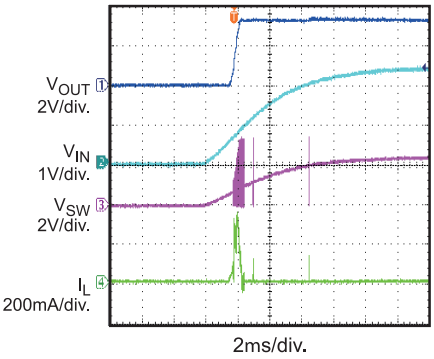
Output Voltage Ripple
I_{OUT} = 20mA



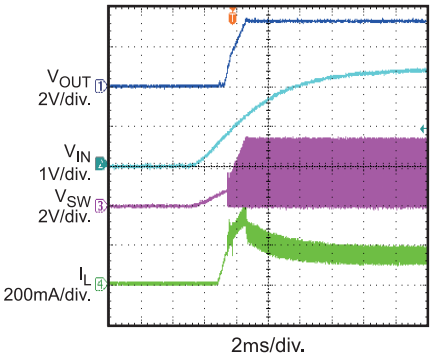
Output Voltage Ripple
I_{OUT} = 100mA



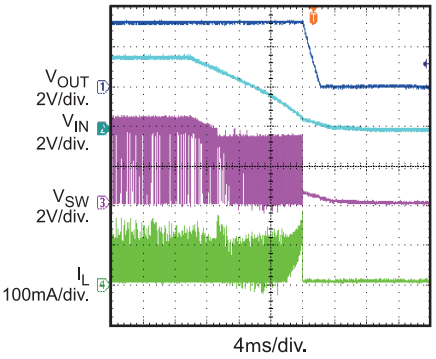
V_{IN} Startup
I_{OUT} = 0mA



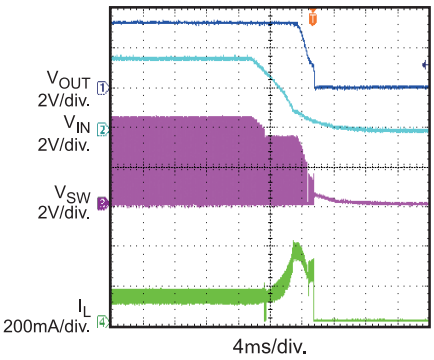
V_{IN} Startup
I_{OUT} = 100mA



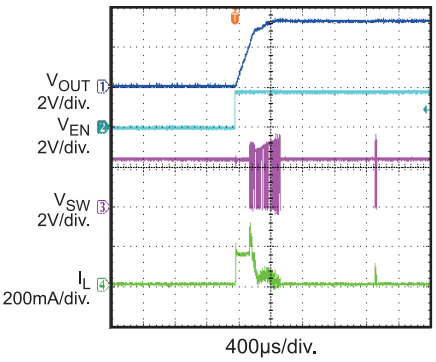
V_{IN} Shutdown
V_{IN} = 3.6V, I_{OUT} = 20mA



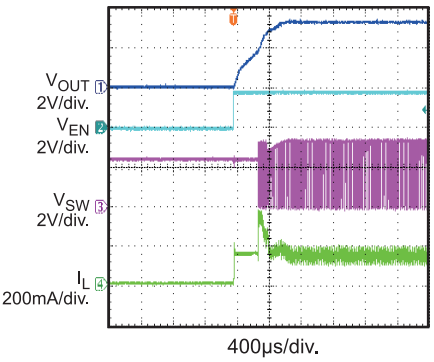
V_{IN} Shutdown
V_{IN} = 3.6V, I_{OUT} = 100mA



EN Startup
I_{OUT} = 0mA



EN Startup
I_{OUT} = 100mA



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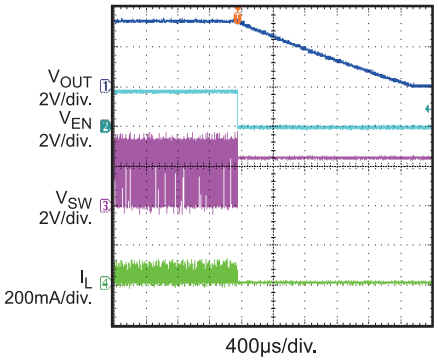
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

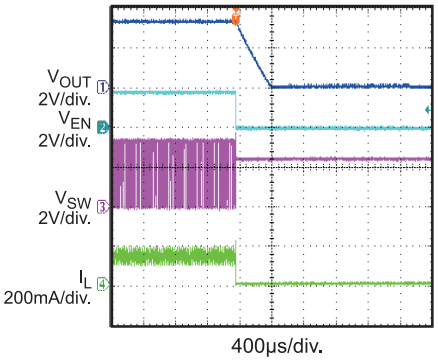
Performance waveforms are tested on the evaluation board in the Design Example section.

V_{IN} = 2.4V, V_{OUT} = 3.3V, L = 6.8µH, C_{OUT}=10uF, T_A = 25°C, unless otherwise noted.

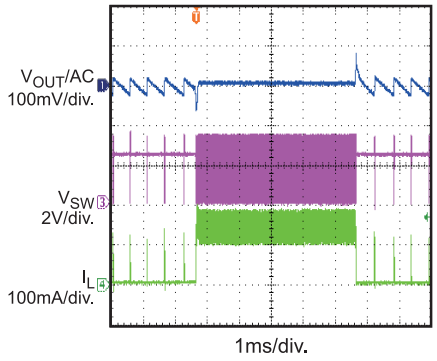
EN Shutdown
I_{OUT} = 20mA



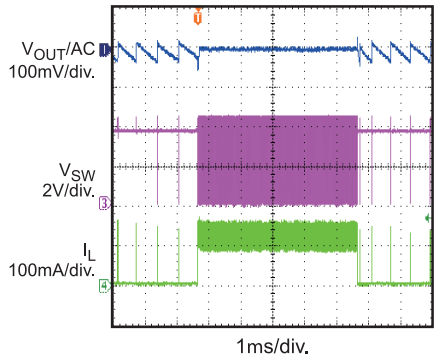
EN Shutdown
I_{OUT} = 100mA



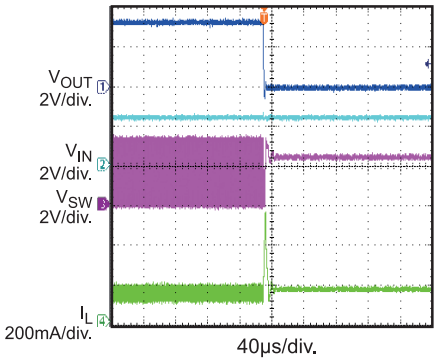
Load Transient
V_{IN}=2.4V, I_{OUT}=0 to 100mA@250mA/µs



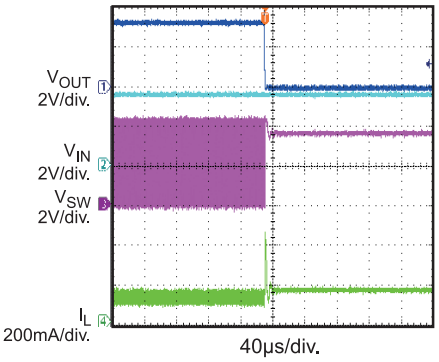
Load Transient
V_{IN}=3.6V, I_{OUT}=0 to 100mA@250mA/µs



Short Circuit Protection
V_{IN}=2.4V, I_{OUT}=100mA before Short



Short Circuit Protection
V_{IN}=3.6V, I_{OUT}=100mA before Short



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PIN FUNCTIONS

Pin #	Name	Pin Function
1	IN	Input Supply. Requires bypass capacitor.
2	OUT	Output Node. Source of the internal synchronous rectifier. Place the output capacitor as close as possible between OUT and PGND.
3	SW	Output Switch Node. Connect the inductor to SW to complete the step-up converter.
4	PGND	Power Ground. Reference ground of the regulated output voltage.
5	NC	No Connection.
6	AGND	Analog Ground.
7	FB	Feedback. Connect to the tap of an external resistive voltage divider from the output to FB to set the output voltage.
8	EN	Enable input. Turns regulator on (V_{EN}>0.7V) or off (V_{EN}<0.1V). Don't apply a voltage greater than 6.5V to this pin.

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BLOCK DIAGRAM

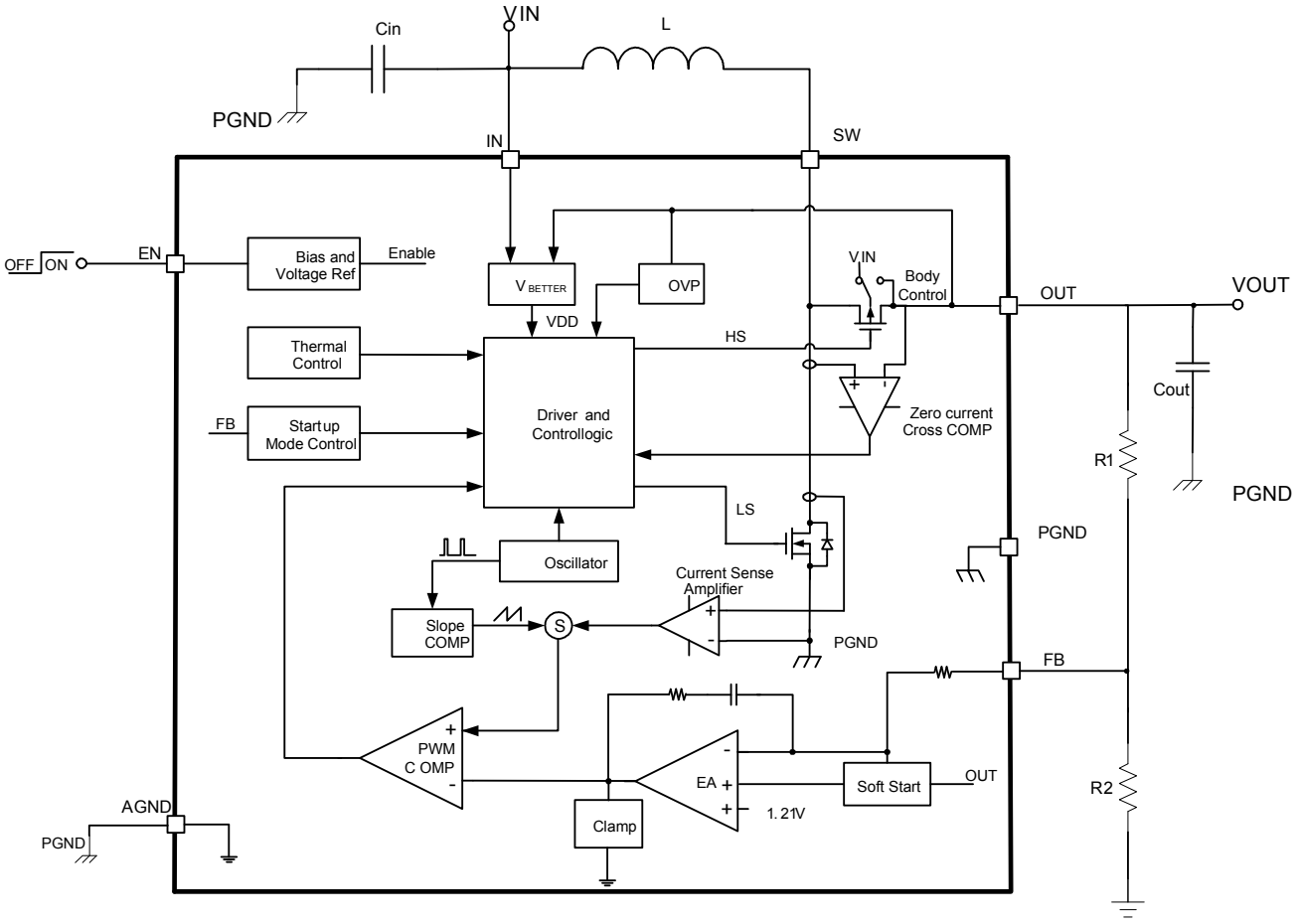

Figure 1: Functional Block Diagram

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OPERATION

The MP3418 is a 1.2MHz, synchronous, step-up converter housed in a compact TSOT23 package with true output disconnect. Able to operate at low-input voltages of less than 0.8V, the device features fixed-frequency current-mode PWM control for exceptional line and load regulation. Internal soft-start and loop compensation simplify the design process and minimize the external components. The internal low-$R_{DS(ON)}$ MOSFETs combined with Power Save Mode operation enable the device to maintain high efficiency over a wide current-load range.

Synchronous Rectifier

The MP3418 integrates an N-channel and a P-channel MOSFET to realize a synchronous rectifier. Replacing the traditional Schottky diode with a low-$R_{DS(ON)}$ PMOS improves efficiency. In a conventional synchronous rectifier, the PMOS body diode is forward-biased, and the current flows from V_{IN} to V_{OUT}. The MP3418 allows for true output disconnect by eliminating the body diode, and prevents battery depletion when the converter shuts down. To prevent excessive inductor current, the PMOS synchronous rectifier only functions when V_{OUT} > (V_{IN} +200mV).

Start-Up

When EN is on, the MP3418 starts up with a linear charge period. During this linear charge period, the rectifier PMOS turns on until the output capacitor charges to V_{IN}–200mV; the PMOS current is limited during this period to around 200mA to avoid inrush current. This circuit also helps to limit the output current under short circuit conditions.

After the linear charging period, the device starts switching. If V_{OUT} remains below 1.7V, the part then works in free-running mode; in this mode, the device works in open loop first at a variable frequency then at a fixed 500kHz switching frequency, the duty cycle depends on the input-output ratio, and the switching current is limited to 400mA to avoid the start-up current inrush.

The internal soft-start (SS) does not take charge and continues to rise following the FB voltage during the linear charging and free-running period. Once the output voltage reaches 1.7V, the normal closed-loop operation initiates, V_{OUT} starts to rise under the control of SS. It then works either in boost mode or down mode depending on V_{IN} and V_{OUT}. Table 1 lists the operation modes during start up.

Table 1: Operation Mode during Start-Up Sequence

V_{OUT} <Vin-200mV & V_{OUT} <1.7V	Linear Charge
V_{OUT} ≥Vin-200mV & V_{OUT} <1.7V	Free Running
V_{OUT} <Vin+200mV & V_{OUT} ≥1.7V	Down mode
V_{OUT} >Vin+200mV & V_{OUT} ≥1.7V	Boost Mode

In normal mode, when V_{OUT}>V_{IN}+200mV, the MP3418 powers itself from V_{OUT} instead of V_{IN}. This allows the battery voltage to drop to as low as 0.6V without affecting the circuit operation. The battery supplies sufficient energy to the output and becomes the only limiting factor in the application.

Device Enable

The device operates when EN is high (>0.7V). It enters shutdown mode when EN is set to low (<0.1V). In shutdown mode, the regulator stops switching and halts all internal control circuitry and eliminate body-diode conduction of the internal PMOS rectifier. This isolates the load from the input, and means that the output voltage can drop below the input voltage during shutdown.

Power-Save Mode

The MP3418 automatically enters power-save mode (PSM) when the load decreases, and resumes PWM mode when the load increases. In PSM, the converter only operates when the output voltage falls below the set threshold, and ramps up by several pulses with the same switching frequency as PWM mode. It resumes power-save mode once the output voltage exceeds the high threshold. PSM requires fewer circuit resources than PWM mode. All unused circuitry is disabled, so as to reduce quiescent power dissipation as well as switching power loss. The OUT pin voltage-

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monitoring circuit and error amplifier with loop compensation for peak-current– mode control remain active.

The output ripple, which is usually around 1% peak to peak, can be reduced by increasing the output capacitance and also by adding a small feed-forward capacitance (around 5.6pF).

The MP3418 operates from PSM to PWM mode depending on the load, which varies with the input voltage, inductor value, and the output capacitor value.

Under-Voltage Lockout

Under-voltage lockout prevents device startup when V_{IN} falls below 0.5V while in operation and the battery is being discharged.

Error Amplifier

The error amplifier (EA) is an internally-compensated amplifier. The EA compares the internal 1.21V reference voltage against V_{FB} to generate an error signal. The output voltage of MP3418 could be adjusted from 1.8V to 4V by connecting FB to the tap of an external voltage divider from V_{OUT} to ground, as per the following equation:

$$V_{OUT} = 1.21V \times (1 + \frac{R1}{R2}) \quad (1)$$

Set R1 and R2 as large as possible to achieve a low quiescent current. Usually, select an R1 value larger than 300k for good stability and transient balance.

Current Sensing

Lossless current sensing converts the NMOS switch current signal to a voltage that can be summed with the internal slope compensator. The difference between this summed signal and the error amplifier output provides control over the peak current through the PWM. Peak switch current is limited to approximately 400mA, independent of input or output voltage. The switching current signal is blanked for 60ns to enhance noise rejection.

Thermal Protection

The device has an internal temperature monitor If the die temperature exceeds 150°C, the switches turn off. Once the output drops below 1.7V, it will turn on..

Output Disconnect and Inrush Limiting

The MP3418 is designed to allow true output disconnect by eliminating the internal PMOS rectifier's body diode conduction. This feature allows V_{OUT} to go to 0V during shutdown and draw 0A from the input source. It also allows for inrush current limiting at start-up, which minimizes surge currents at the input supply. Note that to optimize output disconnect, exclude the external Schottky diode between SW and V_{OUT}.

To minimize voltage overshoot on the SW pin due to stray inductance, keep the output filter capacitor as close as possible to the V_{OUT} pin and use very low ESR/ESL ceramic capacitors tied to a clean ground plane.

Short-Circuit Protection

Unlike most step-up converters, the MP3418 allows for short circuits on the output. In the event of a short circuit, the device first turns off the NMOS when the sensed current reaches the current limit. The device then enters a linear charge period with the current limited as with the start-up period. In addition, the thermal regulation circuit further controls the input current if the die temperature rises above 150°C.

Down Mode (V_{IN}>V_{OUT}) Operation

The MP3418 will continue to regulate the output voltage even when the input voltage exceeds the output voltage. This is achieved by terminating the switching at the synchronous PMOS and applying V_{IN} statically on its gate. This ensures that the slope of the inductor current will reverse while current flows to the output. Since the PMOS no longer acts as a low-impedance switch in this mode, power dissipation increases within the IC to cause a sharp drop in efficiency. Limit the maximum output current to maintain an acceptable junction temperature.

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APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. Add a ceramic capacitor larger than 4.7μF in parallel with a 100nF ceramic capacitor close to the IC.

Output Capacitor Selection

The output capacitor requires a minimum capacitance value of 10μF at the programmed output voltage to ensure stability over the full operating range. A higher capacitance value may be required to lower the output ripple and also the transient response. Low ESR capacitors, such as X5R- or X7R-type ceramic capacitors, are recommended. Assuming that the ESR is zero, estimate the minimum output capacitance to support the ripple in the PWM mode as.

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V} \quad (2)$$

Where,

$V_{OUT(MAX)}$ = Maximum output voltage

$V_{IN(MIN)}$ = Minimum Input voltage

I_O=Output current

f_S = Switching frequency

ΔV= Acceptable output ripple

Additional output capacitance may also be required for applications where $V_{IN} \approx V_{OUT}$ to reduce ripple in PSM mode and to ensure stability in PWM mode, especially at higher output load currents.

Inductor Selection

The MP3418 can use small surface-mount inductors due to its 1.2MHz switching frequency. Inductor values between 4.7μH and 10μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability (and lower the PSM threshold) by reducing the inductor ripple current. Increasing the inductance above 10μH will increase component size while providing little improvement in output current capability. The minimum inductance value is given by:

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{2 \times V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

Where ΔI_L is the acceptable inductor current ripple

The inductor current ripple is typically set at 30% to 40% of the maximum inductor current. High-frequency ferrite-core inductor materials reduce frequency-dependent power losses and improve efficiency compared to cheaper powdered-iron cores. The inductor should have low DCR (inductor series resistance without saturated windings) to reduce the resistive power loss; further reducing the DCR will significantly improve efficiency when DCR<<R_{DS-ON}. Select a large-enough saturation current (I_{SAT}) to support the current peak.

The device enters PSM at a load that borders continuous and discontinuous PWM operation, which means the averaged inductor current (I_{AVG}) is equal to half of the inductor current ripple (ΔI_L). So a larger inductor may lead to a lower PSM enter level.

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PCB Layout Considerations

Layout is important, especially for switching power supplies with high switching frequencies; poor layout results in reduced performance, EMI problems, resistive loss, and even system instability.

Following the rules below can help ensure a stable layout design:

1. Place a decoupling capacitor (>100nF) as close as possible from V_{OUT} to PGND. Avoid placing vias between the OUT pin and the output capacitor to reduce spikes on the SW node and improve EMI performance.
2. Place the input capacitor, output capacitor, and inductor as close to the IC as possible with a short and wide trace.
3. Place the feedback divider resistors as close as possible to the control GND (AGND) pin.
4. Use a large copper GND area to lower the die temperature.

Figure 2 shows the recommended component placement for the MP3418.

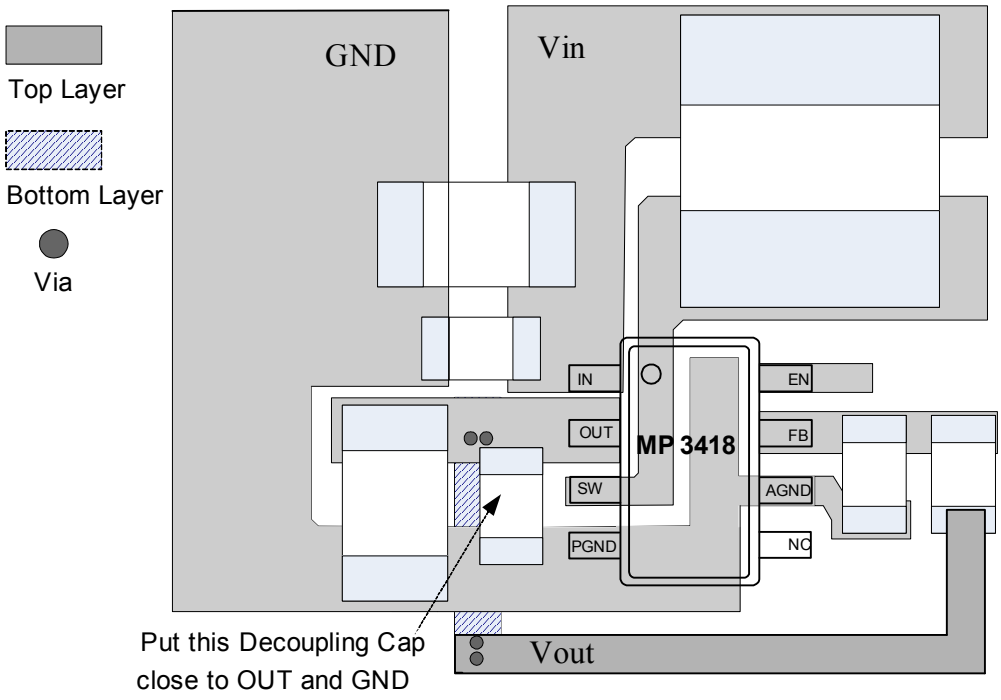

Figure 2: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

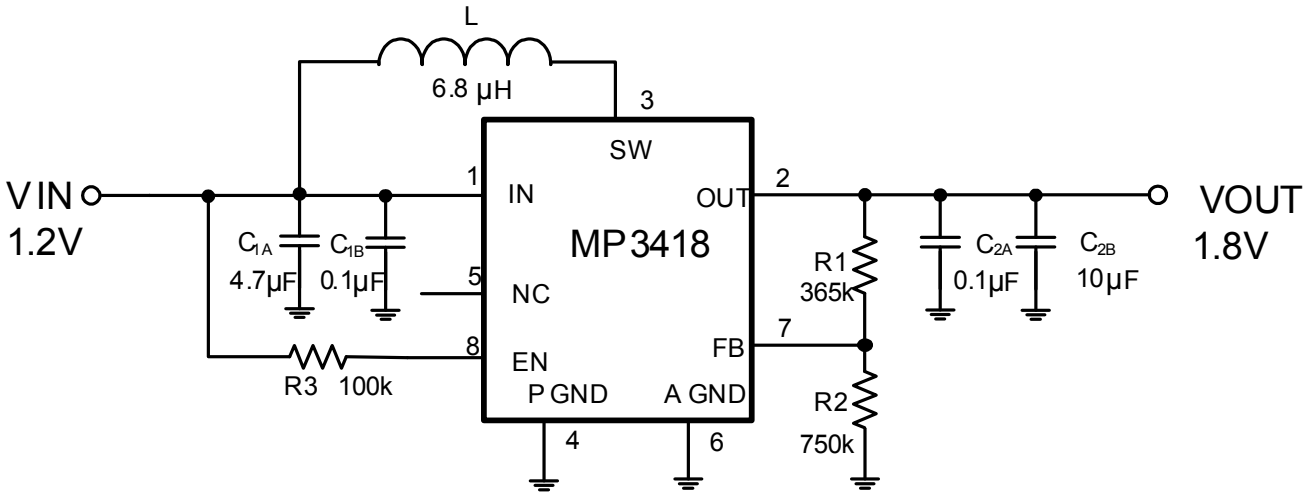

Figure 3: Boost Circuit. V_{IN}=1.2V, V_{OUT}=1.8V.

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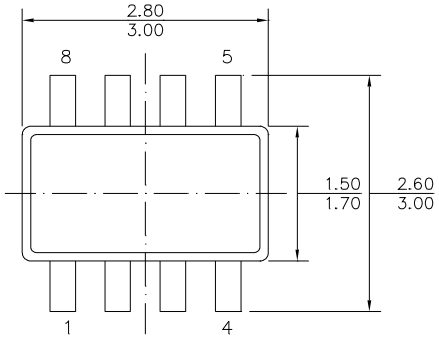
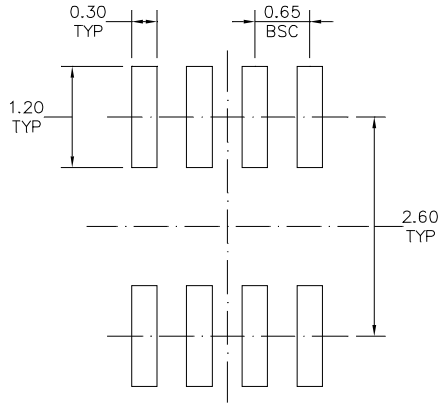
PACKAGE INFORMATION

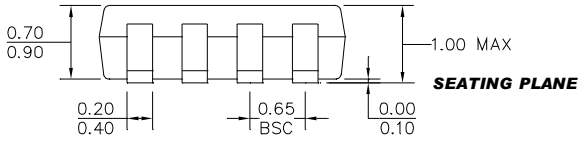
TSOT23-8



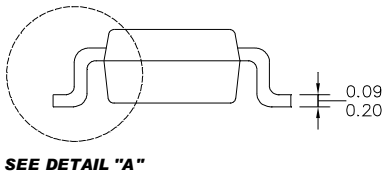
TOP VIEW



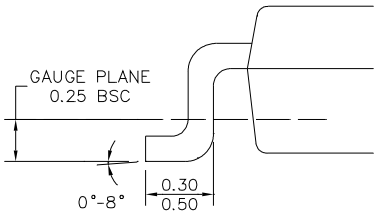
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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