THE DATASHEET OF

MP20051DN-LF

www.win-source.net 0086-755-83957316

MP1470B

High Efficiency, 2A, 16V, 500kHz Synchronous, Step-Down Converter in a 6-Pin TSOT23

The Future of Analog IC Technology

DESCRIPTION

The MP1470B is a high frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input supply range with excellent load and line regulation. The MP1470B has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Protection features include over-current protection and thermal shutdown.

The MP1470B requires a minimal number of readily available, standard, external components and is available in a compact 6-pin TSOT23 package.

FEATURES

- Wide 4.7V to 16V Operating Input Range
- 163mΩ/86mΩ Low-$R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- High-Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Forced PWM
- Internal Soft Start
- Over-Current Protection and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a 6-Pin TSOT23 Package

APPLICATIONS

- Game Consoles
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

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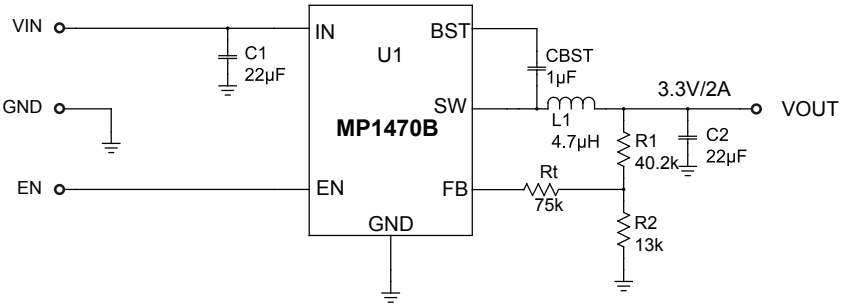
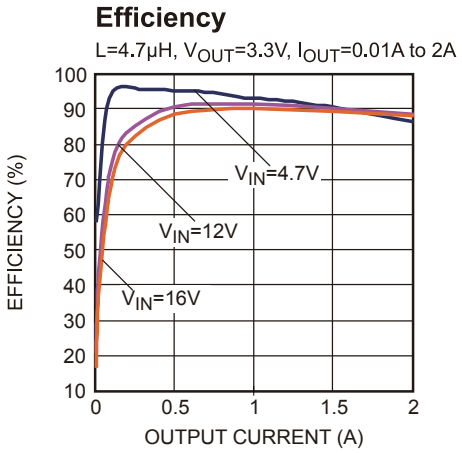
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1470BGJ	TSOT23-6	*See Below*

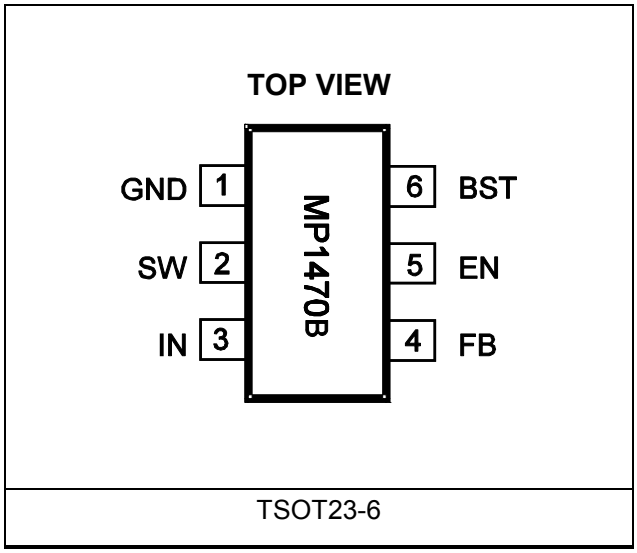
* For Tape & Reel, add suffix –Z (e.g. MP1470BGJ–Z)

TOP MARKING

|APMY

APM: Product code of MP1470BGJ
Y: Year code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 17V
V_{SW} .....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BS} ..... V_{SW}+6V
All other pins(2) ..... –0.3V to 6V
Continuous power dissipation (T_A = +25°C) (3)
.....1.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.7V to 16V
Output voltage (V_{OUT})..... 0.8V to VIN*D_{MAX}
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSOT23-6	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For the ABS voltage of EN, please refer to page11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply current (quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		0.83		mA
HS switch-on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		163		mΩ
LS switch-on resistance	LS_{RDS-ON}	Vcc = 5V		86		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit	I_{LIMIT}	V_{IN} = 12V, D = 40%	3	3.7		A
Oscillator frequency	f_{SW}	V_{FB} = 0.75V	400	490	580	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 700mV	88	92		%
Minimum on time[6]	T_{ON_MIN}			90		ns
Feedback voltage	V_{FB}		776	800	824	mV
EN rising threshold	V_{EN_RISING}		1.4	1.5	1.6	V
EN falling threshold	$V_{EN_FALLING}$		1.23	1.32	1.41	V
EN input current	I_{EN}	V_{EN} = 2V		1.6		μA
		V_{EN} = 0		0		μA
V_{IN} under-voltage lockout threshold—rising	$INUV_{Vth}$		3.85	4.2	4.55	V
V_{IN} under-voltage lockout threshold—hysteresis	$INUV_{HYS}$			340		mV
Soft-start period	T_{SS}	V_{OUT} from 0% to 100%		1		ms
Thermal shutdown[6]	T_{SD}			150		°C
Thermal hysteresis[6]	T_{SD_HYS}			20		°C

NOTE:

6) Not tested in production. Guaranteed by engineering sample characterization.

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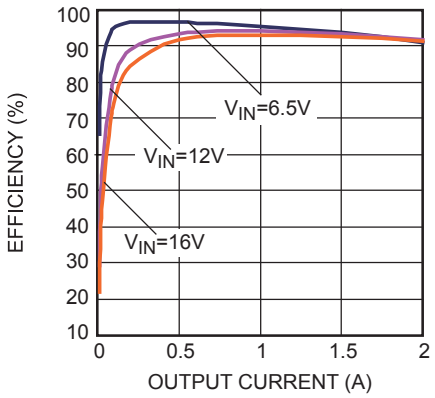
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

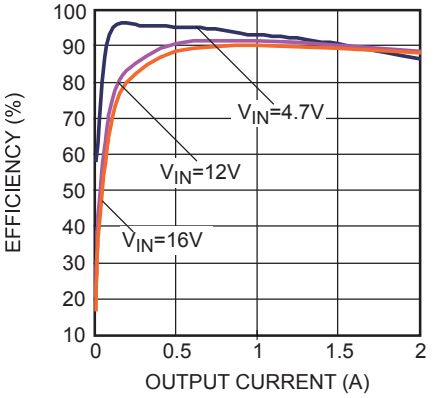
Efficiency

L=6.5µH, V_{OUT}=5V, I_{OUT}=0.01A to 2A



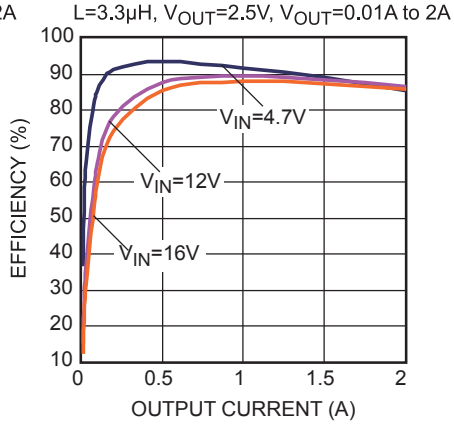
Efficiency

L=4.7µH, V_{OUT}=3.3V, I_{OUT}=0.01A to 2A



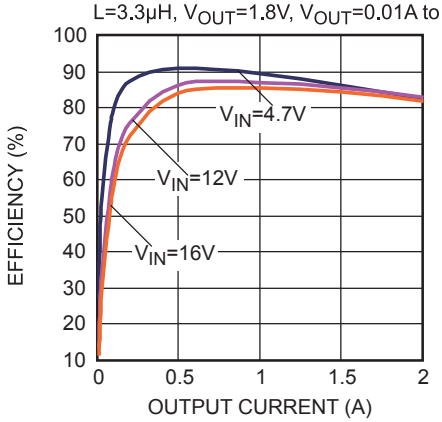
Efficiency

L=3.3µH, V_{OUT}=2.5V, V_{OUT}=0.01A to 2A



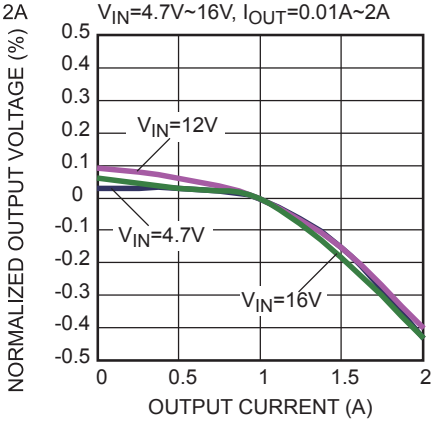
Efficiency

L=3.3µH, V_{OUT}=1.8V, V_{OUT}=0.01A to 2A



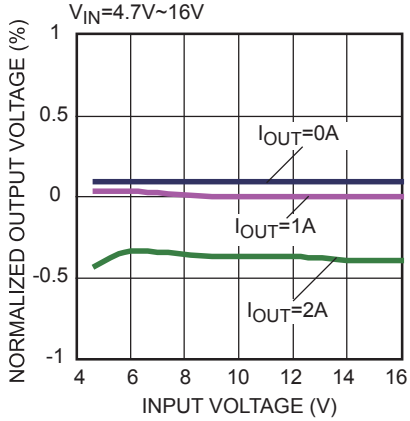
Load Regulation

V_{IN}=4.7V~16V, I_{OUT}=0.01A~2A

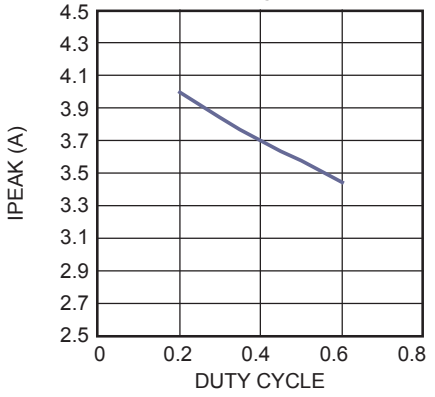


Line Regulation

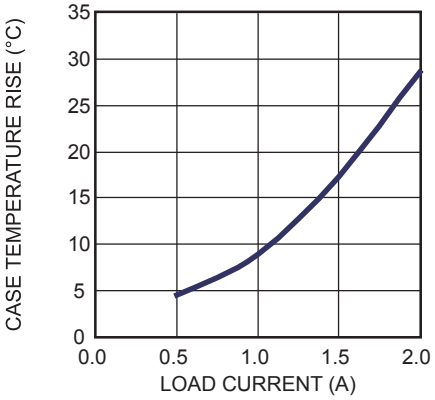
V_{IN}=4.7V~16V



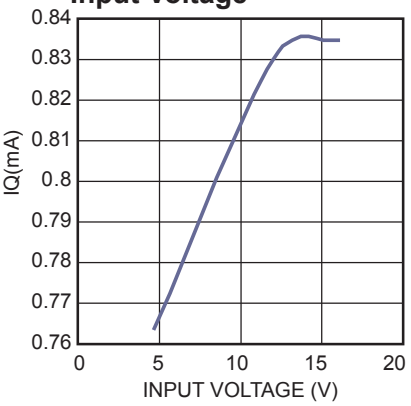
Inductor Peak Current Limit vs. Duty



Case Temperature Rise vs. Load Current



Quiescent Current vs. Input Voltage



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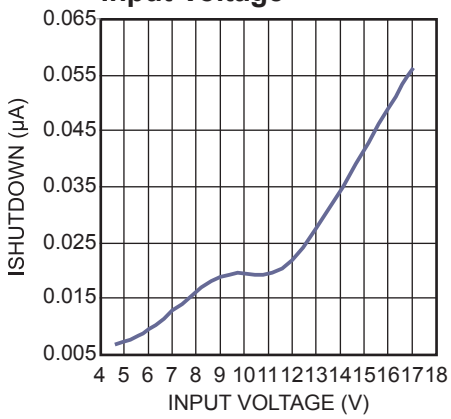
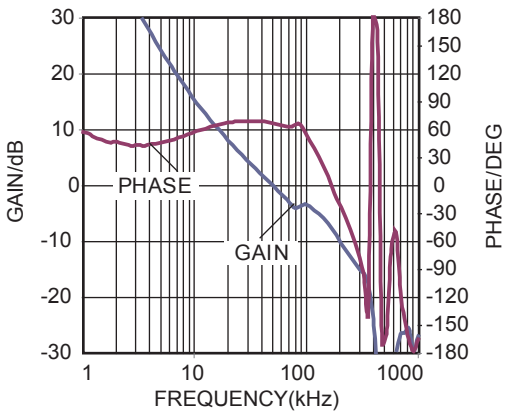
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

Shutdown Current vs. Input Voltage



Bode Plot



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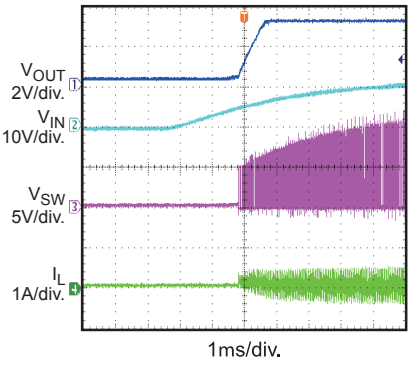
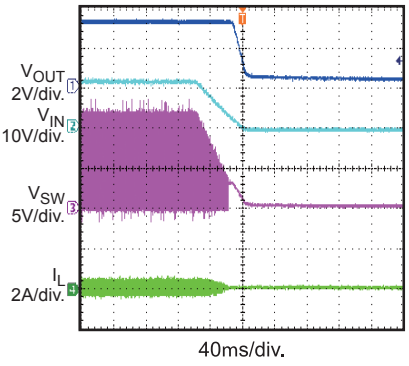
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

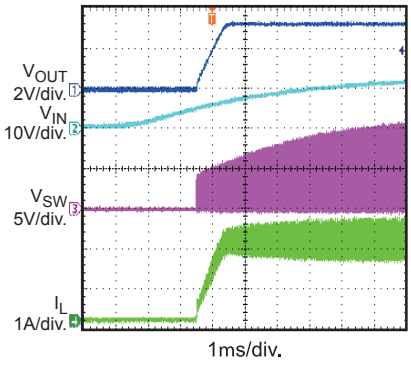
Startup through Input Voltage
I_{OUT} = 0A



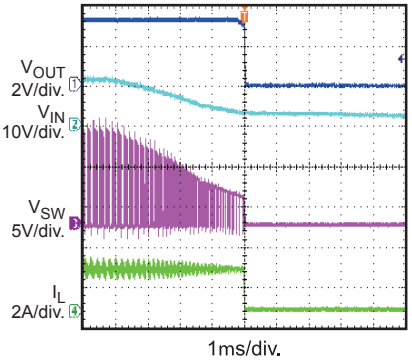
Shutdown through Input Voltage
I_{OUT} = 0A



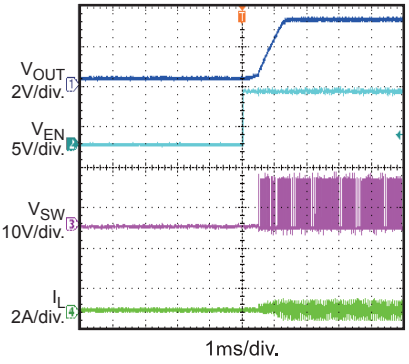
Start-Up through Input Voltage
I_{OUT} = 2A



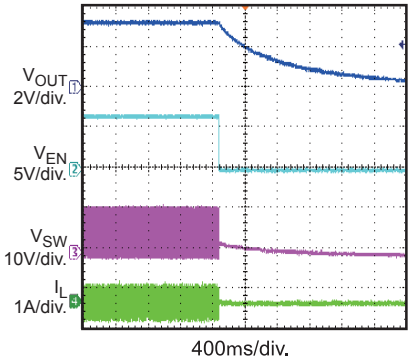
Shutdown through Input Voltage
I_{OUT} = 2A



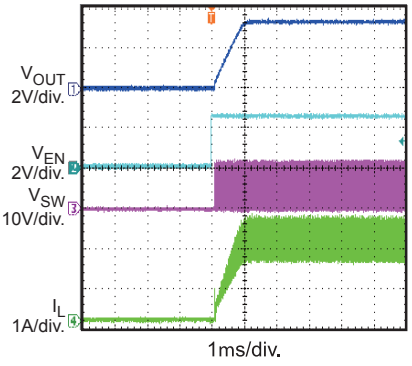
Start-Up through Enable
I_{OUT} = 0A



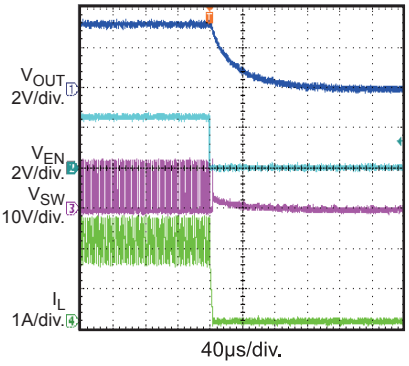
Shutdown through Enable
I_{OUT} = 0A



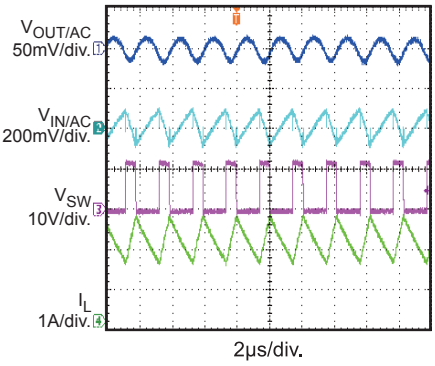
Startup through Enable
I_{OUT} = 2A



Shutdown through Enable
I_{OUT} = 2A



Input/Output Ripple
I_{OUT} = 2A



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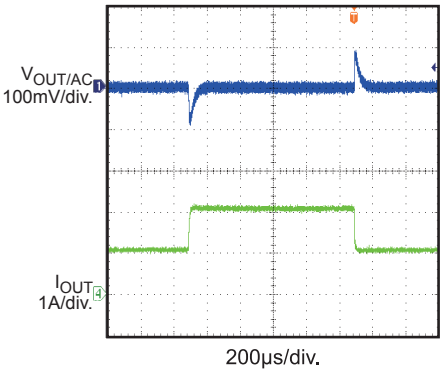
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = +25°C, unless otherwise noted.

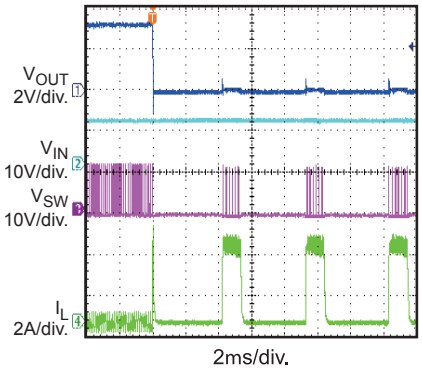
Transient Response

I_{OUT} = 1A to 2A, 2.5A/µs



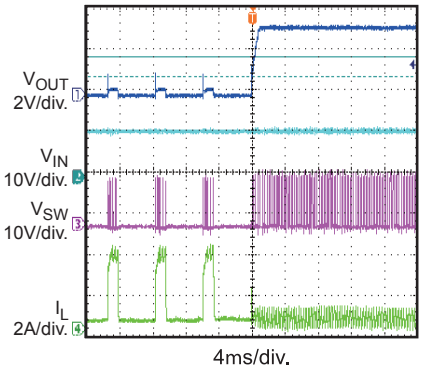
Short-Circuit Entry

I_{OUT} = 0A



Short-Circuit Recovery

I_{OUT} = 0A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	GND	**System ground.** GND is the reference ground of the regulated output voltage: it requires extra care during PCB layout. Connect to GND with copper traces and vias.
2	SW	**Switch output.** Connect using a wide PCB trace.
3	IN	**Supply voltage.** The MP1470B operates from a 4.7V to 16V input rail. IN requires C1 to decouple the input rail. Connect using a wide PCB trace.
4	FB	**Feedback.** Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 140mV to prevent current-limit runaway during a short-circuit fault.
5	EN	**EN = high to enable the MP1470B.** For automatic start-up, connect EN to V_{IN} using a 100kΩ resistor.
6	BST	**Bootstrap.** Connect a capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver. Use a 1μF BST capacitor.

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FUNCTIONAL BLOCK DIAGRAM

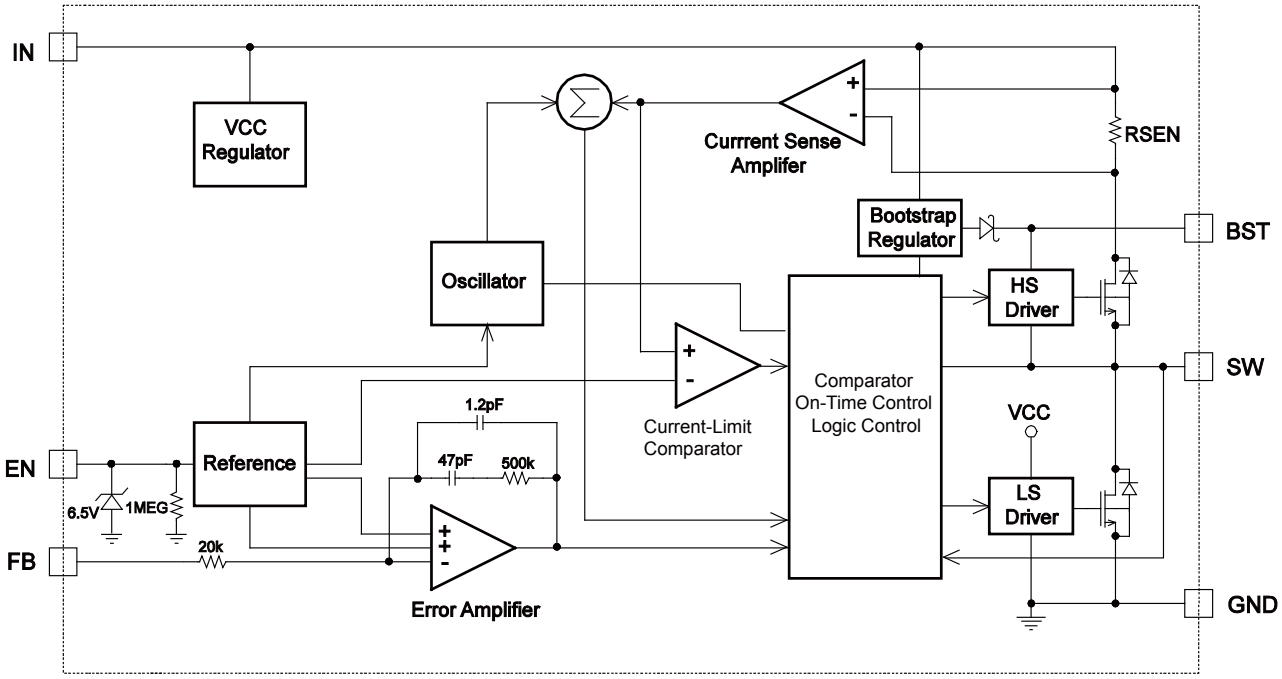

Figure 1: Functional Block Diagram

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OPERATION

The MP1470B is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input supply range with excellent load and line regulation.

The MP1470B operates in a fixed frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates the PWM cycle to turn on the integrated high-side power MOSFET. This MOSFET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP set current value within 92% of one PWM period, the power MOSFET is forced to turn off.

Internal Regulator

The 5V internal regulator powers most of the internal circuits. This regulator takes V_{IN} and operates in the full V_{IN} range.

Error Amplifier

The error amplifier compares the FB voltage against the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current charges or discharges the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to float to shut down the chip.

EN is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to V_{IN} limits the EN input current to less than 100μA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V-6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

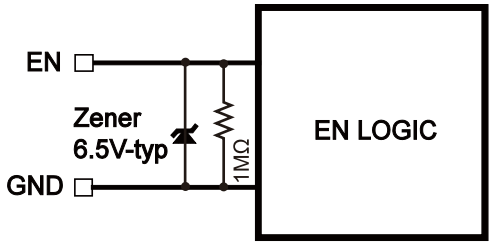

Figure 2: 6.5V Zener Diode

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1470B UVLO comparator monitors the output voltage of the internal regulator (VCC). The typical value of the UVLO rising threshold is about 4.2V while its falling threshold is about 3.86V.

Pre-Bias Start-Up

The MP1470B is designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is charged by V_{IN}. If the BST voltage exceeds its rising threshold voltage, the internal soft-start voltage ramps up. When the internal soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Internal Soft Start (SS)

A soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuit generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS falls below the internal reference (REF), SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier resumes using REF as its reference. The SS time is set internally to 1ms.

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Over-Current Protection and Hiccup Mode

The MP1470B has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current limit threshold. When the output voltage drops to trigger a UV event (FB falls below the under-voltage (UV) threshold (typically 140mV)), the MP1470B enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator. The MP1470B exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the whole chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, L1, and C2 (see Figure 3). If V_{IN}-V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4.

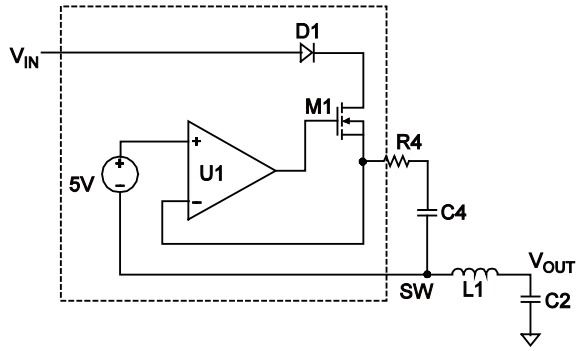

Figure 3: Internal Bootstrap Charger Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Also, the feedback resistor (R1) sets the feedback loop bandwidth through the internal compensation capacitor (see the Typical Application circuits). Refer to Table 1 to choose R1 and R2 using Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (1)$$

Use a T-type network (see Figure 4).

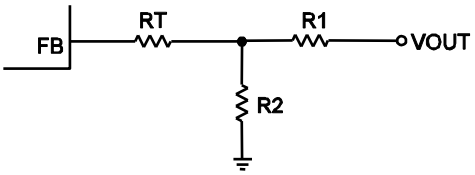

Figure 4: T-Type Network

Table 1 lists the recommended T-type resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.05	10 (1%)	32.4 (1%)	300 (1%)
1.2	20.5 (1%)	41.2 (1%)	249 (1%)
1.8	40.2 (1%)	32.4 (1%)	120 (1%)
2.5	40.2 (1%)	19.1 (1%)	100 (1%)
3.3	40.2 (1%)	13 (1%)	75 (1%)
5	40.2 (1%)	7.68 (1%)	75 (1%)

Selecting the Inductor

Use a 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. For best performance, use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectrics, and small temperature coefficients. A 22μF capacitor is sufficient for most applications.

The input capacitor (C1) requires an adequate ripple-current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, as shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality ceramic capacitor (0.1μF) as close to the IC as possible when using electrolytic or tantalum capacitors. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low

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ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP1470B can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap (BST) diode can enhance the efficiency of the regulator given the following applicable conditions:

- V_{OUT} is 5V or 3.3V;
- the duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

Connect the external BST diode from the output voltage regulator to BST (see Figure 5).

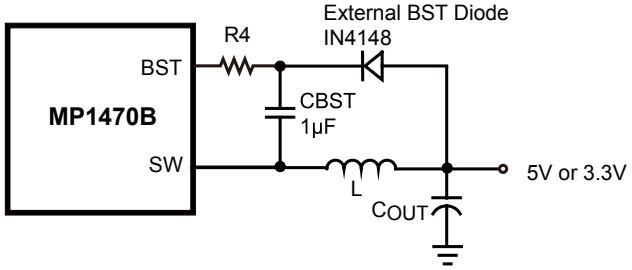

Figure 5: Optional External Bootstrap Diode

For most applications, use an IN4148 for the external BST diode and a 1µF capacitor for the BST capacitor.

PCB Layout Guidelines

Efficient PCB layout is critical to achieve stable operation. For best results, refer to Figure 6 and follow the guidelines below:

1. Keep the connection between the input ground and GND as short and wide as possible.
2. Keep the connection between the input capacitor and IN as short and wide as possible.
3. Use short and direct feedback connections.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas such as FB.

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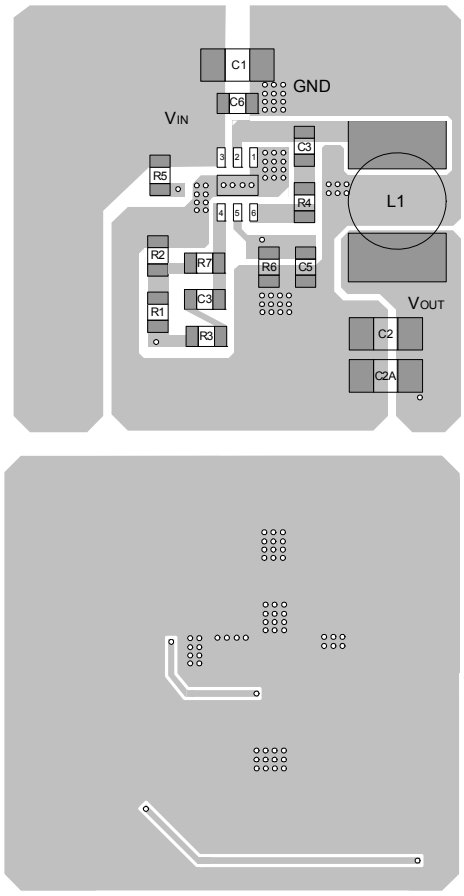

Figure 6: Recommended PCB Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_O	2A

The detailed application schematics are shown in Figures 7 through 11. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

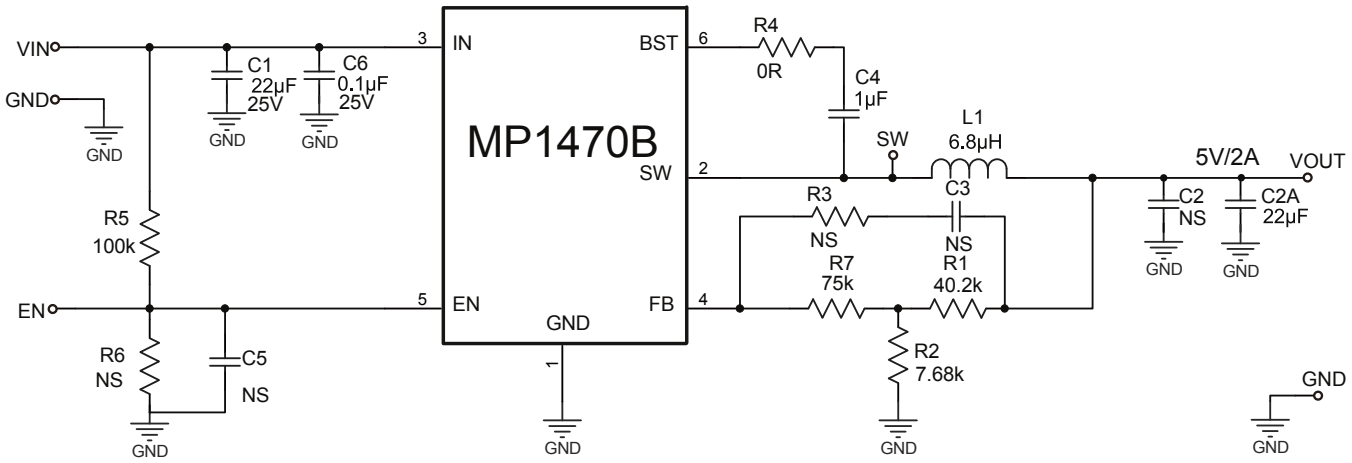

Figure 7: 12Vin, 5V/2A

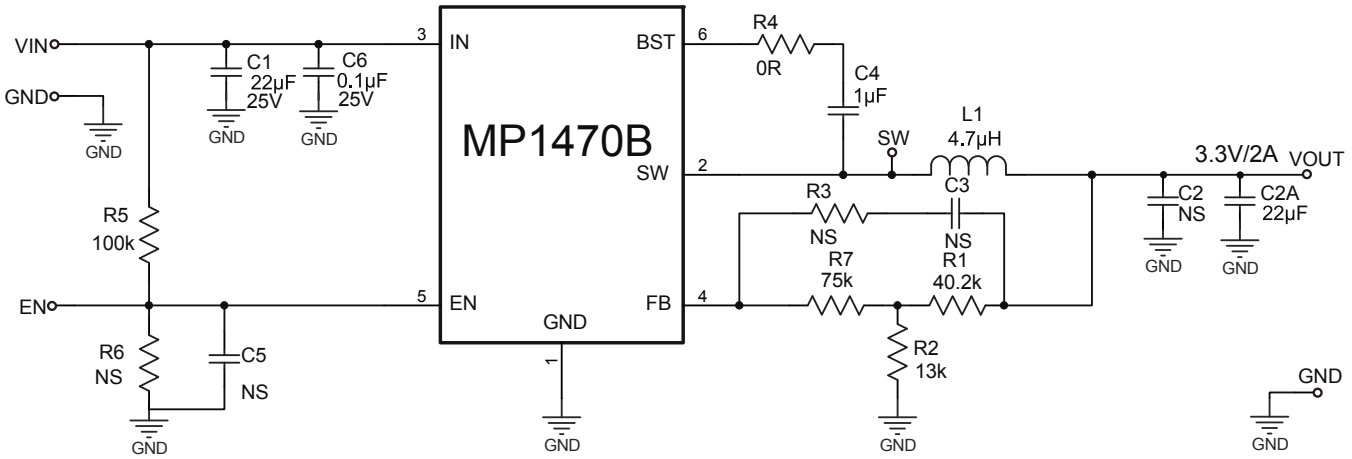

Figure 8: 12Vin, 3.3V/2A

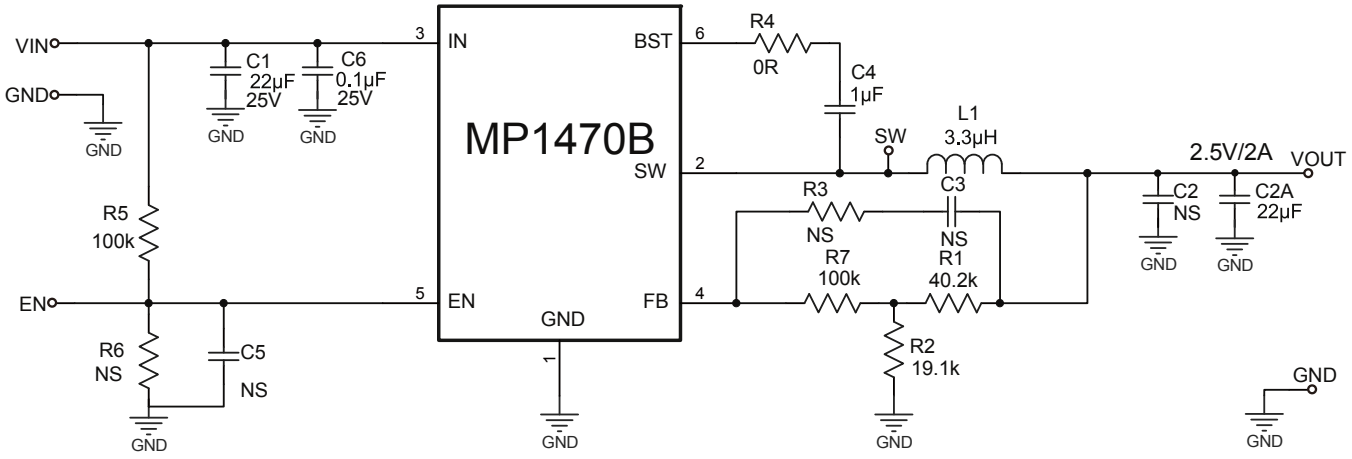

Figure 9: 12Vin, 2.5V/2A

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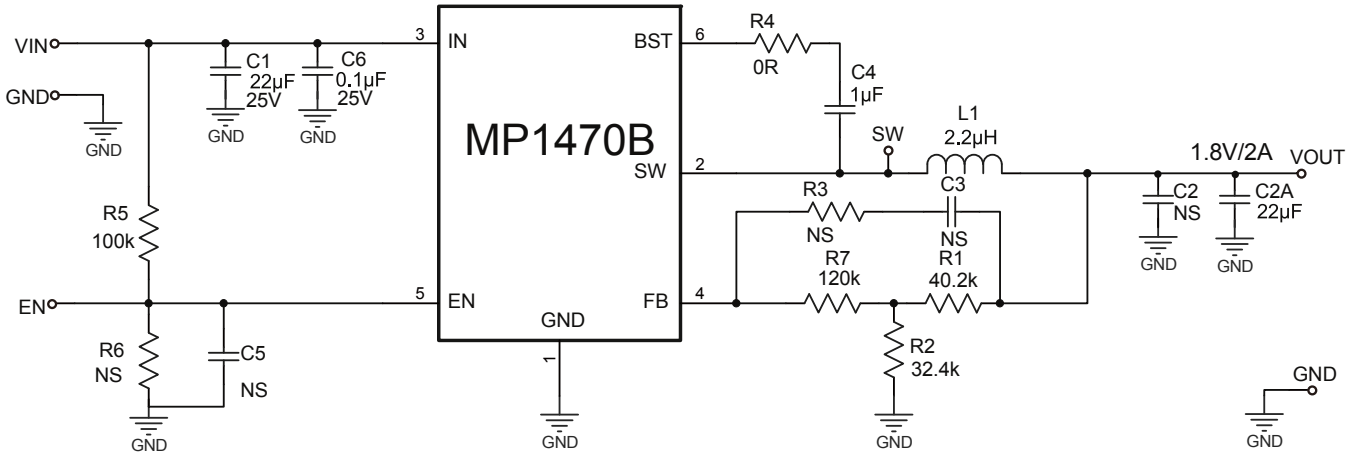

Figure 10: 12Vin, 1.8V/2A

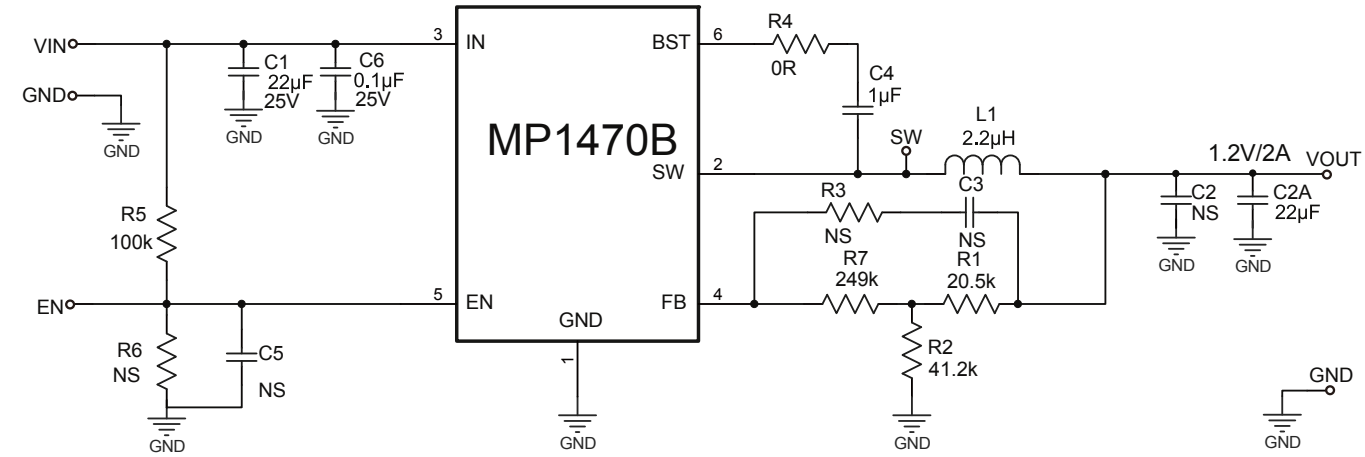

Figure 11: 12Vin, 1.2V/2A

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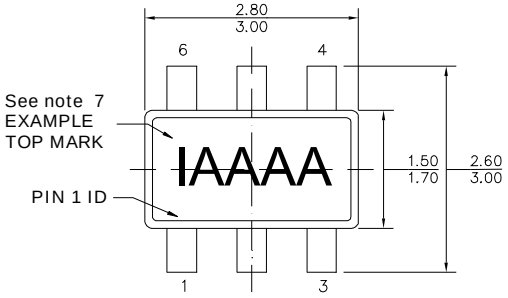
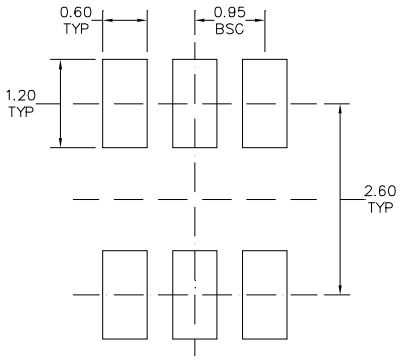
PACKAGE INFORMATION

TSOT23-6



TOP VIEW



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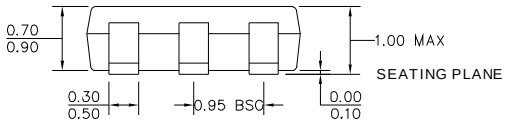
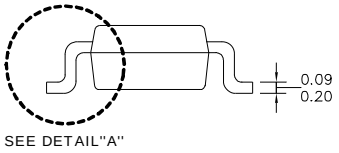
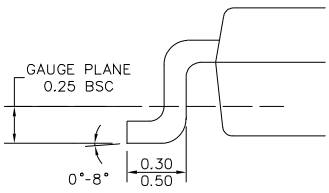


FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK).

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