Features

- Three Input Channels for 3D Antennas
- 2.8 mV_{PP} Sensitivity Typically
- Ultra Low Current Operation Consumption
- 2 µA Standby Current Typically
- 4 µA Active Current Typically
- Power Supply 2 V to 4.2 V
- Carrier Frequency Range from 100 kHz to 150 kHz
- Wake-up Function for a Microcontroller
- Header Detection
- Baud Rate up to 4 kbps (ASK Modulation)
- Bi-directional Two-wire Interface
- ESD According to Automotive Requirements

Benefits

- Digital RSSI for Field Strength Measurement
- Coils Input Range from 2.8 mV_{PP} to 2.8 V_{PP} Typically
- High Sensitivity

Applications

- Passive Entry Go (PEG)/Car Access
- Position Indicator
- Home Access Control
- RFID Systems

Description

The ATA5282 is a 125-kHz ultra low power receiver IC with three input channels for Passive Entry Go applications. It includes all circuits for an LF wake-up channel. The three sensitive input stages of the IC amplifier demodulate and measure the input signal from the antenna coils. The microcontroller interface of the IC outputs the data signal as well as the measured RSSI values. During standby mode, the header detection unit monitors the incoming signal and generates a wake-up signal for the microcontroller if the IC receives a valid 125-kHz carrier signal.

By combining the IC with an antenna coil, a microcontroller, an RF transmitter/transceiver and a battery, it is possible to design a complete hands-free key for Passive Entry Go applications.

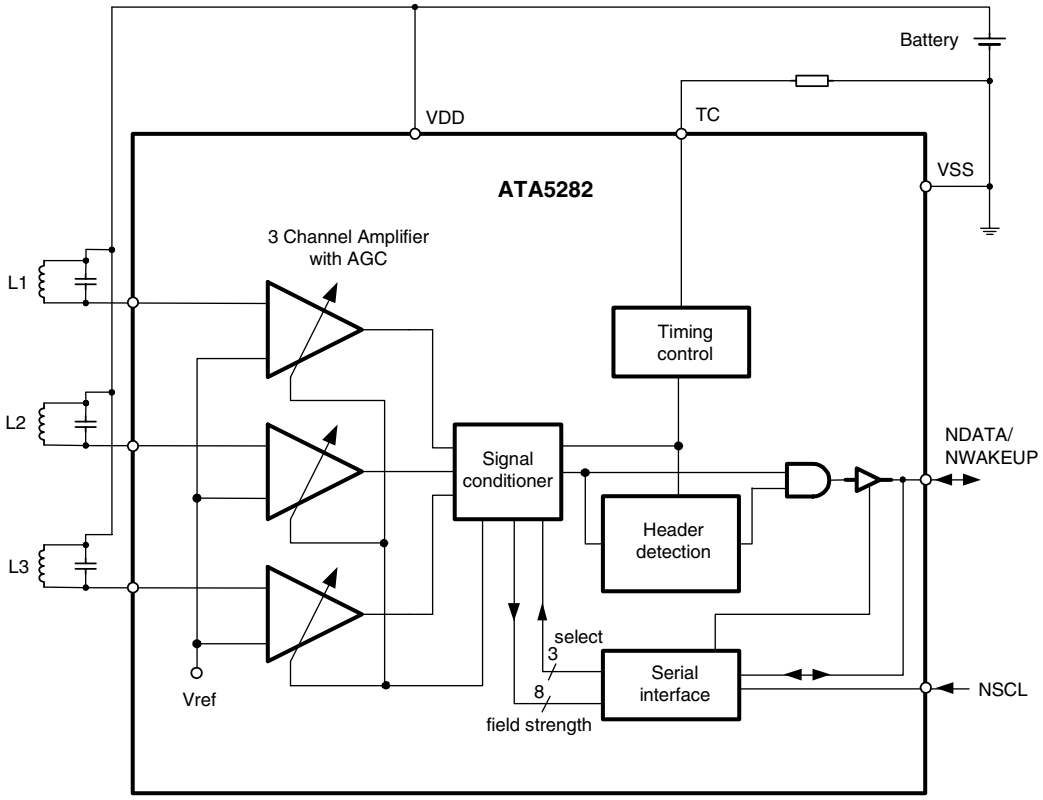
Ultra Low Power 125 kHz 3D - Wake-up Receiver with RSSI

ATA5282

Preliminary

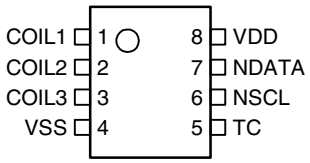
Rev. 4694B–AUTO–06/04

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning TSSOP 8L



Pin Description

Pin	Symbol	Function
1	COIL1	Input: Coil channel X
2	COIL2	Input: Coil channel Y
3	COIL3	Input: Coil channel Z
4	VSS	Circuit ground
5	TC	Output: Current output for oscillator adjustment
6	NSCL	Input: Clock for serial interface (default high)
7	NDATA	Input/Output: I/O data for serial interface and field strength measurement/ Wake-up function (default high)
8	VDD	Battery voltage

Functional Description

The ATA5282 is a 3-channel ASK receiver for 125-kHz carrier signals. Its three active input stages with very low power consumption and high input sensitivity allow to connect up to 3 antennas for direction-independent wake-up function and data transfer.

Without a carrier signal the ATA5282 operates in standby listen mode. In this mode, it monitors the 3 Coil inputs with a very low current consumption. To activate the IC and the connected control unit, the transmitting end must send a preamble carrier burst and the header code. When a preamble has been detected, the IC activates the internal oscillator and the header check. The last gap at the end of a valid header enables the NDATA output.

During data transfer, the NDATA pin outputs the demodulated and merged signal of the 3 input stages.

To achieve data rates up to 4 kbps for input signals from 2.8 mV_{PP} to 3.1 V_{PP} it is necessary to control the gain of the amplifiers. Each of the 3 input stages contain an amplifier with Automatic Gain Control (AGC). It is used to adapt the gain to the incoming signal strength, and is also used as RSSI for field strength measurements.

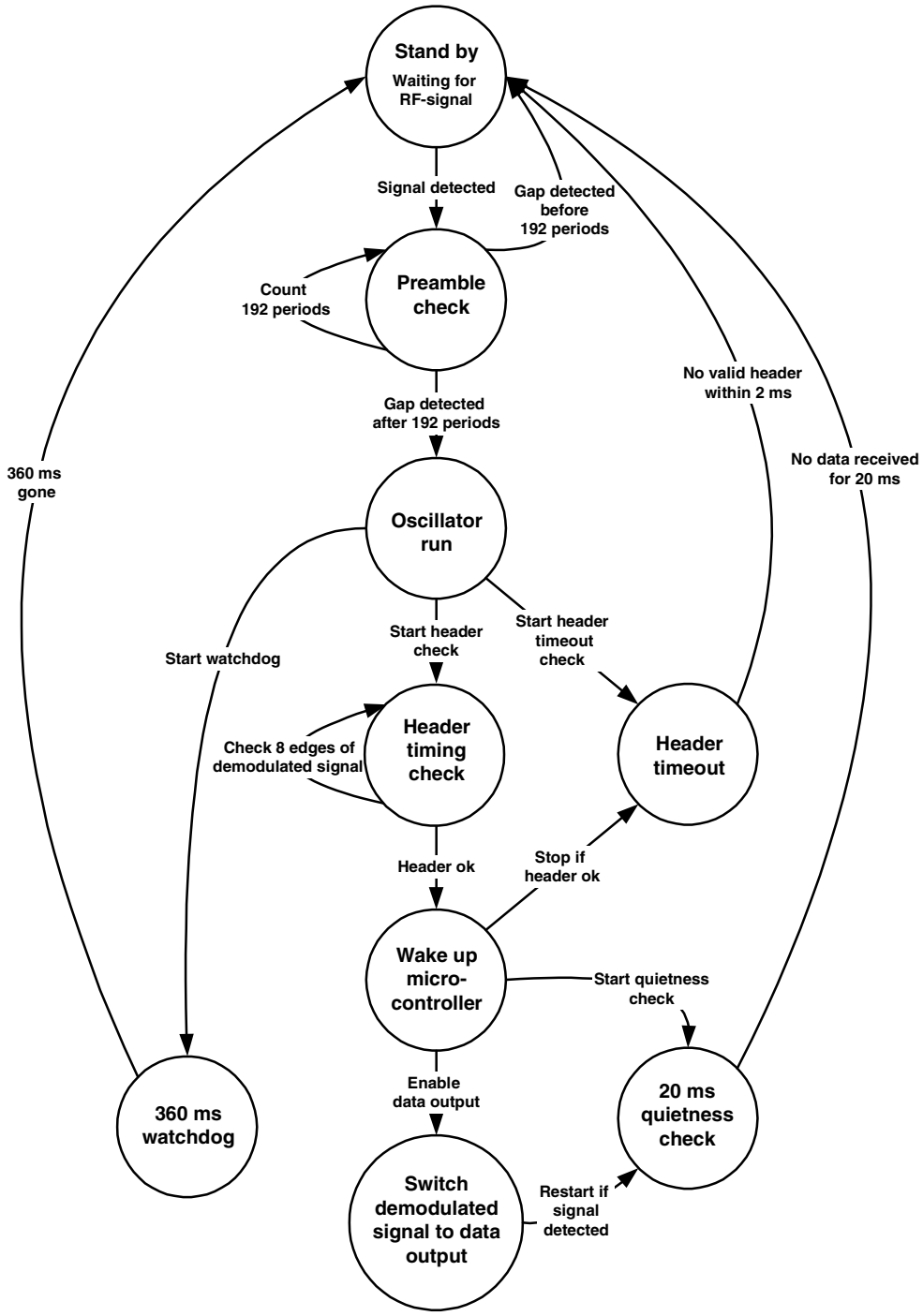
The integrated synchronous serial interface uses the NSCL together with the NDATA pin as clock and data line. It allows to control several functions as well as read out the received signal field strength. Enabling only single coil inputs, freezing the actual status of the automatic gain control or resetting the complete circuit to the initial state at any time are built-in features.

When communication is finished or a time out event occurs, the internal watchdog timer or reset command via the serial interface sets the IC to standby listen mode.

Functional State Diagram

This diagram gives an overview of the major tasks performed by the ATA5282. The detailed function of the automatic gain control that is active during preamble check, header check and data transfer is not shown here.

Figure 3. ATA5282 State Diagram



AGC Amplifier

Each of the three input stages contain an AGC amplifier to amplify the input signal from the Coil. The gain is adjusted by the automatic gain control circuit if a preamble signal is detected. The high dynamic range of the AGC amplifier enables the IC to work with input signals from 2.8 mV_{PP} to 3.1 V_{PP}. After the AGC settling time has elapsed, the amplifier output delivers a 125-kHz signal with an amplitude adjusted for the following evaluation circuits (preamble detection, signal conditioner, wake-up).

Automatic Gain Control

For correct demodulation, the signal conditioner needs an appropriate internal signal amplitude. To control the input signal, the ATA5282 has a built-in digital AGC for each input channel. This gain control circuit regulates the internal signal amplitude to the reference level (Ref2, Figure 4 on page 6). The gain control uses the signal of the input channel with the highest amplitude for the regulation as well as signal for the signal conditioner.

During the preamble, each period of the carrier signal decreases the gain if the internal signal exceeds the reference level. If the signal does not achieve the reference level, each period increases the gain. After 192 preamble periods, the standard gain control mode is activated. In this mode, the gain is decreased every two periods if the internal signal exceeds the reference level and increased every eight periods if the reference level is not achieved. These measures assure that the input signal's envelope deformation will be minimized.

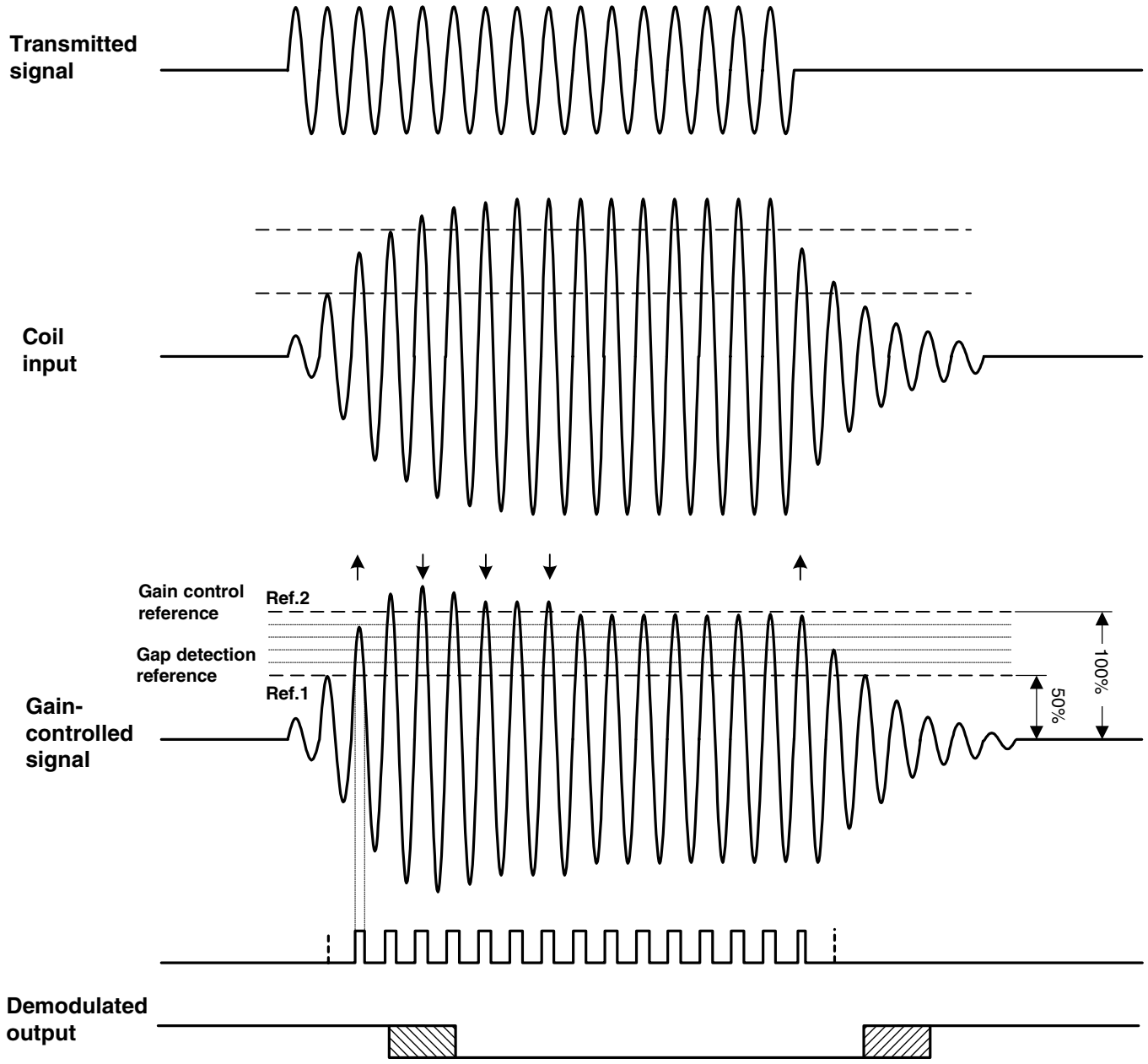
During the gaps between signal bursts, the gain control is frozen to avoid that the gain be modified by noise signals.

The tuning range of the AGC is subdivided into 256 regulator steps. The settling time for the full tuning range requires 320 periods (192 + (2 $\times$ 64) periods) during a preamble phase. To accelerate the settling time, fast gain control mode can be activated via the serial interface. In this mode, the tuning range is subdivided into 128 steps and the settling time is two times faster.

In standby listen mode, the gain is reset to the maximum value. A proper carrier signal activates the automatic gain control.

The preamble (Figure 9 on page 10) with up to 320 periods of the 125 kHz magnetic field is used to control the gain of the input amplifiers. To detect the starting point of the header, the start gap should not exceed 256 µs (32 periods of 125 kHz).

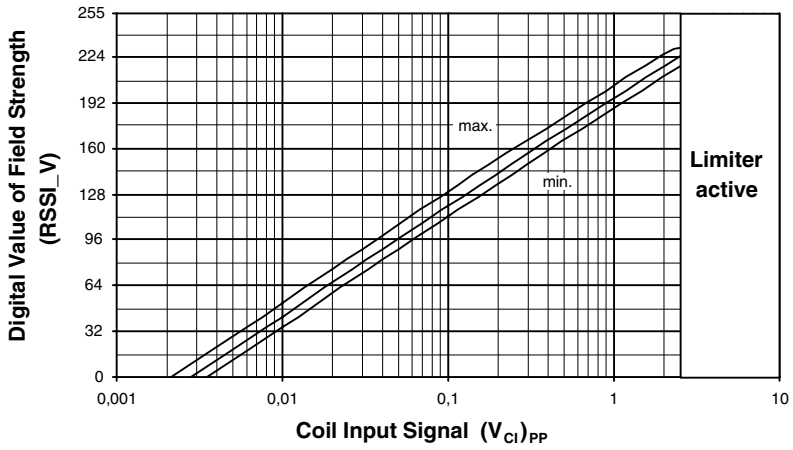
Figure 4. Automatic Gain Control



Field Strength RSSI (Received Signal Strength Indicator)

The digital value of the AGC counter is used as an indicator for the corresponding field strength of the input signal. The digital value can be accessed by the microcontroller via the serial interface.

Figure 5. Field Strength as a Function of Coil Input Signal



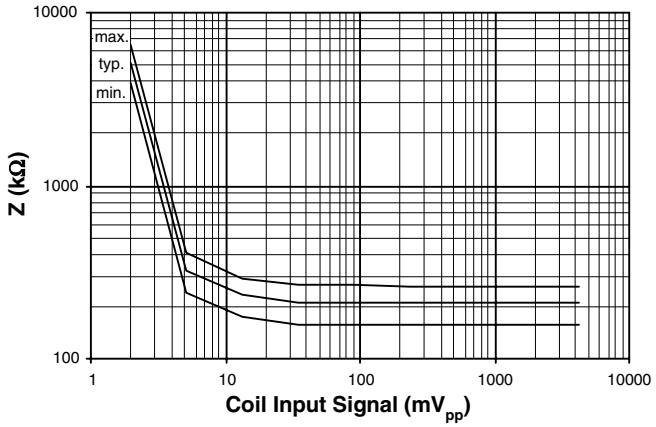
The characteristic gain control value versus the coil input signal (see Figure 5) can be calculated by using the following equation:

$$RSSI_V = ROUND\ (32.36 \times Ln(V_{CI})_{PP} + 192.7)$$

RSSI_V: Digital value of field strength
Ln(): Natural logarithm function
V_{CI}: Coil input voltage

With the variation of the gain the coil input impedance changes from high impedance to minimal 143 kΩ (Figure 6). This impedance variation is an insignificant influence to the quality factor of the resonant circuits.

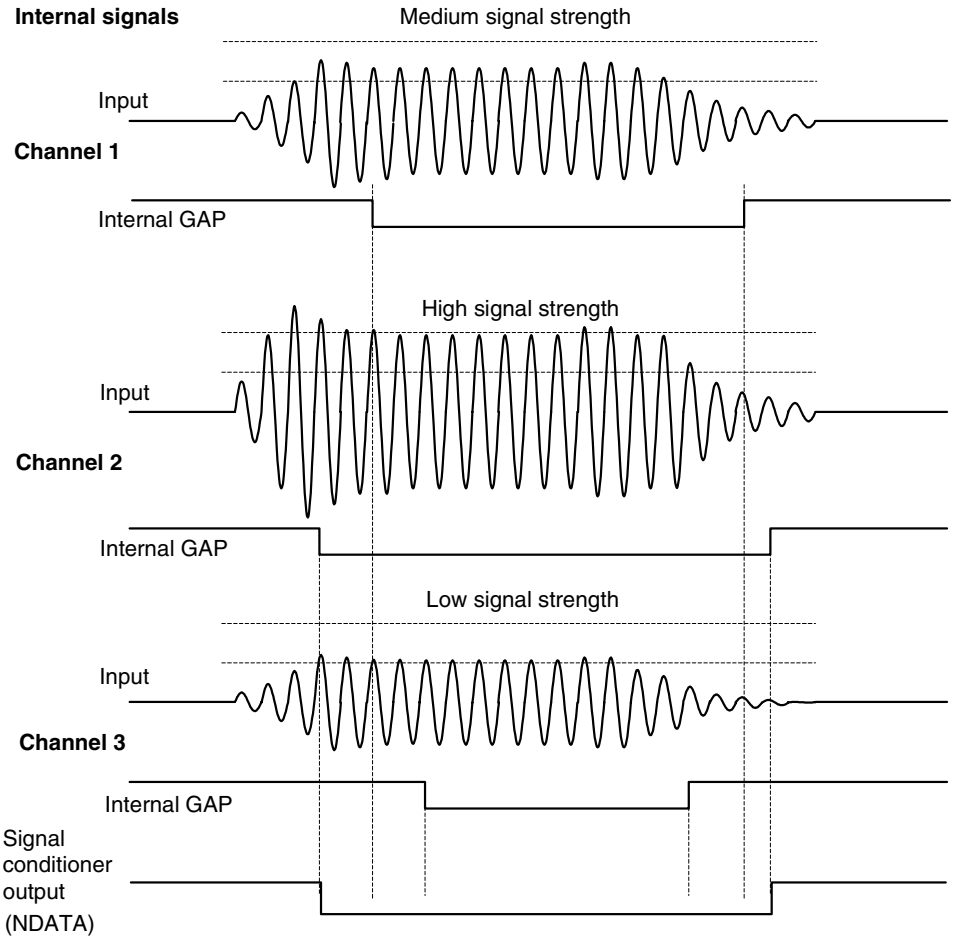
Figure 6. Coil Input Impedance



Signal Conditioner

The signal conditioner operates on the demodulated output signal of all three channels.

Figure 7. Function of Signal Conditioner



The AGC reduces the gain of all 3 channels with reference to the signal with the highest amplitude. This automatically reduces the gain of channels with medium or low input signal amplitudes which results in the suppression of further process of these channels. The logical combination of the 3 demodulated output signals mostly represents the signal with the highest input amplitude.

Preamble Detection

To prevent the circuit from unintended operations in a noisy environment, the preamble is checked to consist of 192 periods minimum. Three consecutive periods missing do not disturb counting. With this check passed, the circuit starts the internal oscillator at the end of the preamble (Figure 11 on page 12). The AGC needs a maximum of 256 steps for full range tuning of amplifiers.

Before data transmission occurs the IC remains in standby listen mode. To prevent the circuit from unintended operations in a noisy environment, the preamble detection circuit checks the input signal. A valid signal is detected by a counter circuit after 192 carrier periods without interrupts. Short interrupts which are suppressed by the signal conditioner are tolerated. If a valid carrier (preamble) has been found, the circuit starts the automatic gain control. It requires up to 256 carrier periods for settling. The complete preamble should have at least 320 carrier periods.

Internal Oscillator

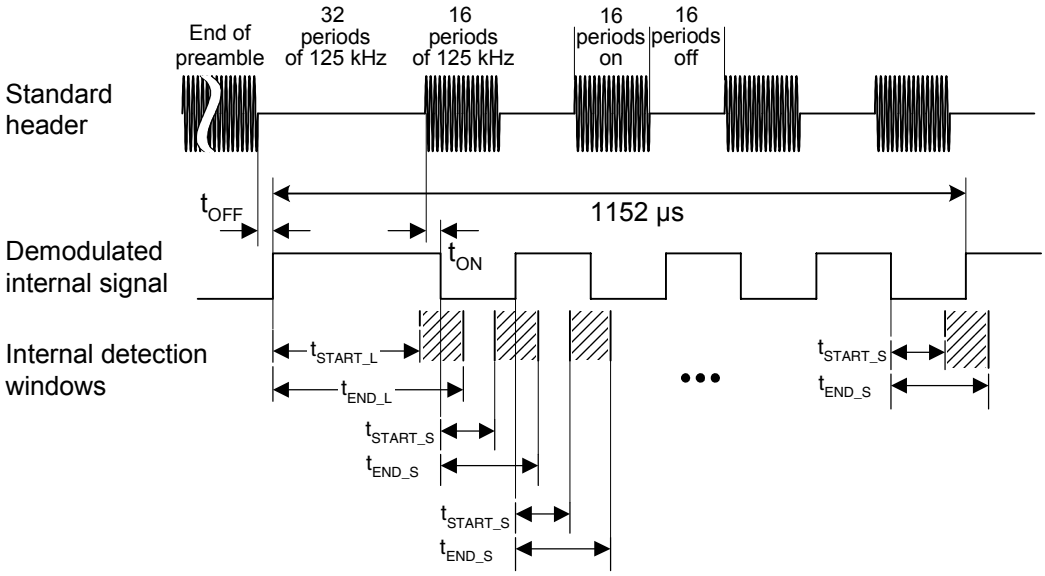
If the end of the preamble is detected, the internal oscillator starts operating. It works as a time base to generate the time windows for the header detection, the header time-out check, the 20-ms-no-signal check and the data transmission duration watchdog. An external resistor connected to TC selects the oscillators frequency and defines all internal timings.

Header Detection and Wake-up

The preamble needs to be followed by the specific header. This header ensures that the built-in header detection wakes up the controller only with a valid signal. One possible protocol used for wake-up and data transmission is shown in Figure 9 on page 10 and Figure 11 on page 12.

The standard header information must be transferred in OOK-mode (On-Off-Keying) with a duty cycle of 50%. The header detection starts with the start gap. A valid header requires 8 consecutive samples of rising and falling edges before the NDATA pin switches from high to low.

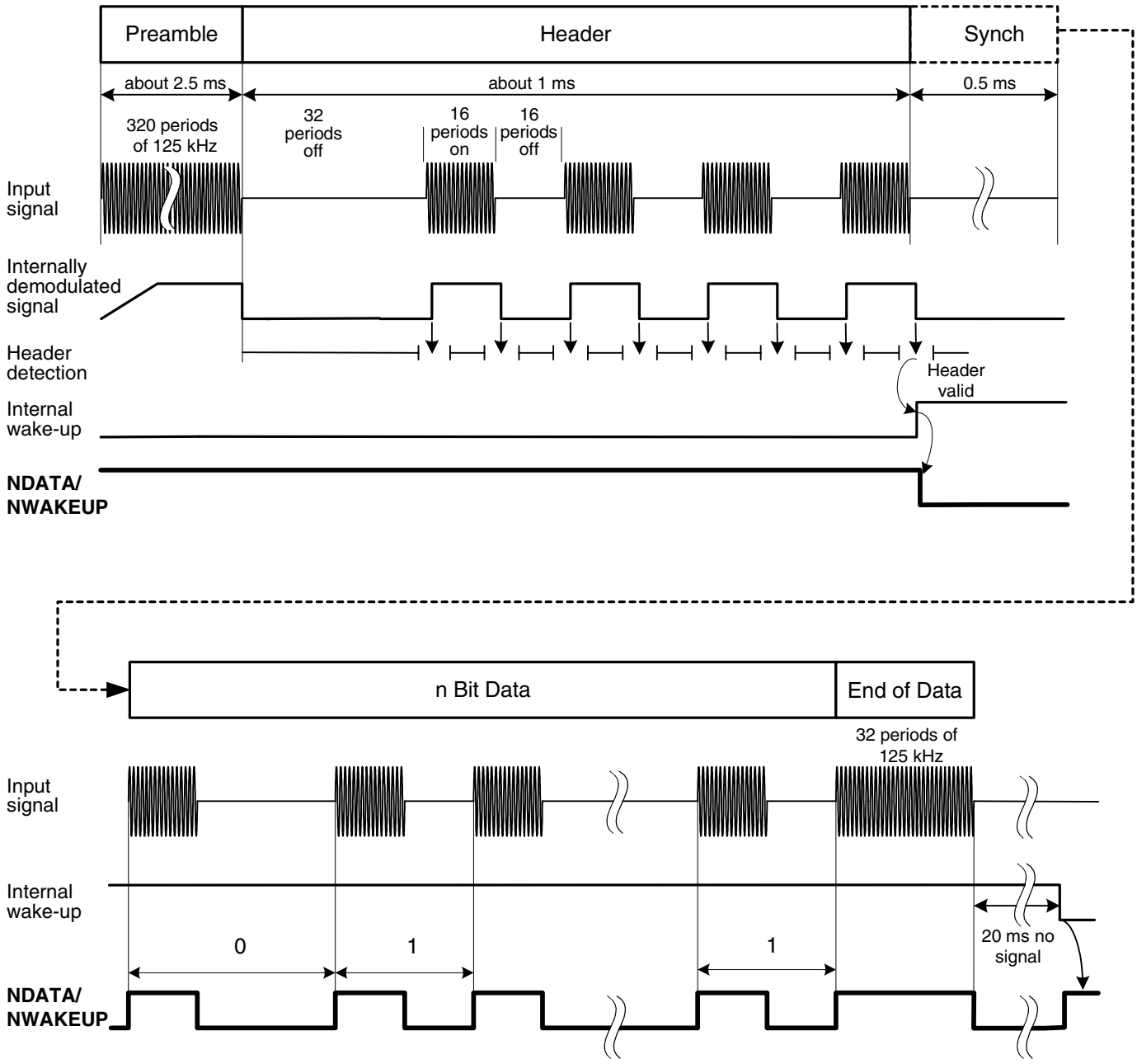
Figure 8. Standard Header



If no valid header has been detected within 2 ms, beginning at the end of the preamble, the header time-out check stops the oscillator and resets the gain control as well as the header detection circuit to their initial state. The circuit then waits for the next preamble.

In case of corrupted data or in a noisy environment, the controller also may use the serial interface to reset the ATA5282 to the initial state. This is performed by shifting a specific command into the internal command register.

Figure 9. Wake-up Protocol for 125-kHz ASK Modulation

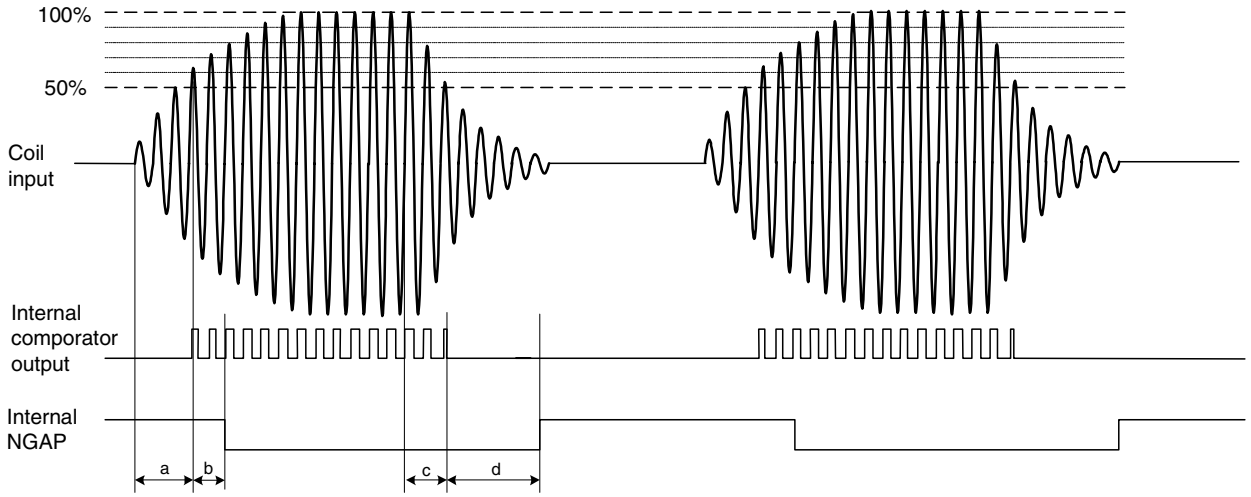


Data Output

The wake-up signal enables the data pin that delivers the received and demodulated data stream to the controller. Sampling and decoding has to be performed by the controller. An example for data coding is given in the "n Bit Data" field (Figure 9 on page 10). This kind of modulation requires an indication of the end of data, for example, by a burst that differs from the other transmitted bits. As the circuit does not check the received data (except the header), it is up to the base station which kind of modulation (pulse distance, Manchester, bi-phase...) is used.

The data output signal is derived from the internal GAP detection. Table 1 describes how the timing depends on different conditions of the applied input signal. The Q-factor of the external LC-tank as well as the signal strength influence the pulse width of the output signal.

Figure 10. Output Timing Conditons



a + b = Data delay time t_{ON}

c + d = Data delay time t_{OFF}

Table 1. Typical Output Timing versus Signal Strength at 3.2 V Supply Voltage

Input Signal	a, c (Figure 10)	b (Periods)			d (Periods)		
		no Q	Q ≤14	Q ≤20	no Q	Q ≤14	Q ≤20
Minimum, 2.8 mV_{PP}	Depends on Q-factor	2 to 4	3 to 5	4 to 6	2 to 4	3 to 5	3 to 5
Medium, V_{CI} < 3.2 V_{PP}		2 to 4	3 to 5	4 to 6	2 to 4	3 to 5	3 to 5
Strong, V_{CI} ≥ 3.2 V_{PP}		2 to 4	2 to 4	2 to 4	2 to 4	3 to 5	3 to 5

Current Profile and Reset Function

As long as the ATA5282 does not receive and recognize a valid preamble, it stays in a low-current listen mode with the gain control and the header detection reset to their initial state. After the circuit has passed the preamble check, the internal oscillator and the watchdog (for a 360 ms interval) starts. This results in an increased current consumption. The target of the different reset sources is to reduce the current consumption as fast as possible back to the initial value.

This can take place at the end of the header time-out check at the earliest. If no valid header has been detected within 2 ms, the circuit switches back to the initial state.

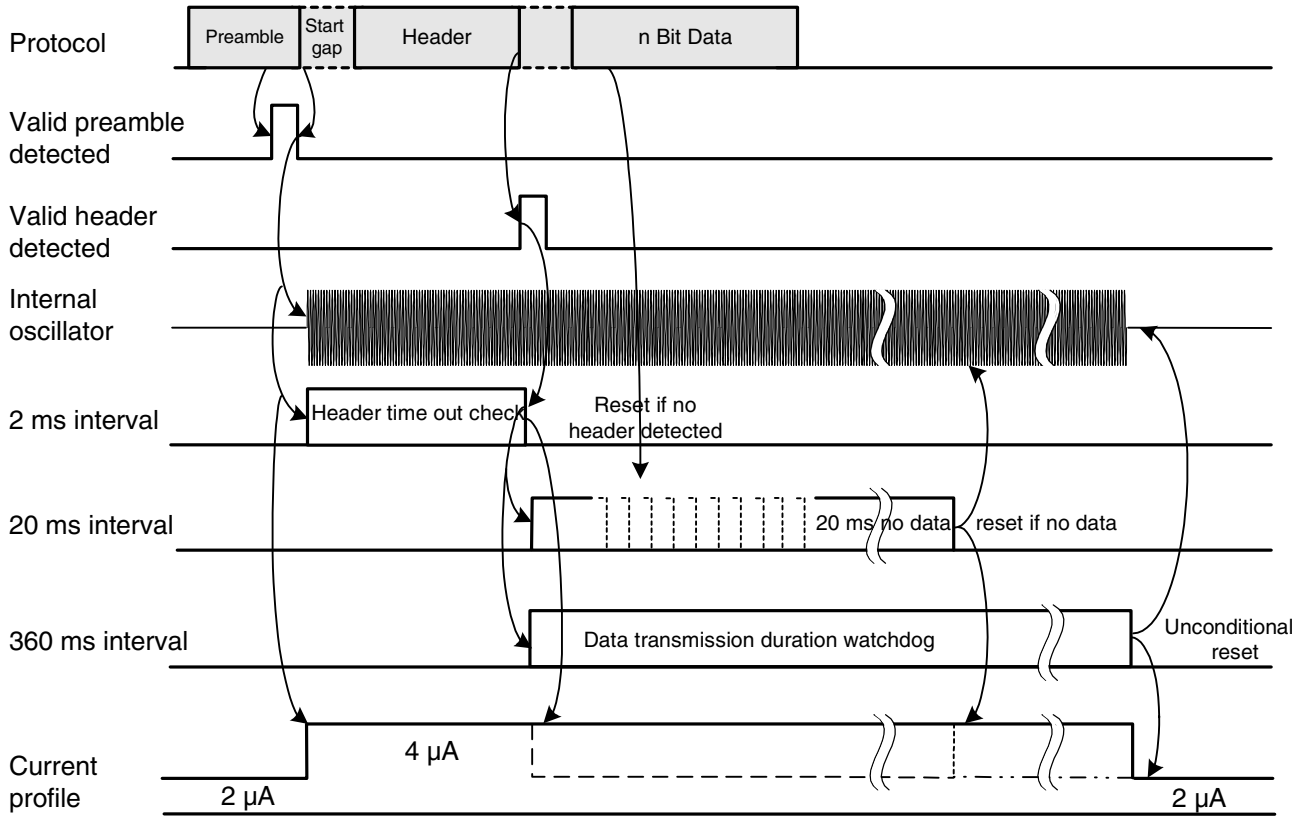
With wake-up activated, three further mechanism are available to control the reset. One under control of the connected microcontroller, one if no signal is received and one unconditional after a fixed time.

The controller may shift the SOFTRES-command into the internal command register to force the circuit into the reset state. This may be useful if the controller detects that the received data are corrupted.

The ATA5282 itself permanently checks for incoming signals. An interval of 20 ms (no signal received) also leads to the reset state.

If there is no valid signal within 20 ms, for example, in a noisy environment or due to customer protocol requirements, the watchdog forces the circuit into the reset state after a fixed time of 360 ms at the latest.

Figure 11. Current Profile and Reset Timing

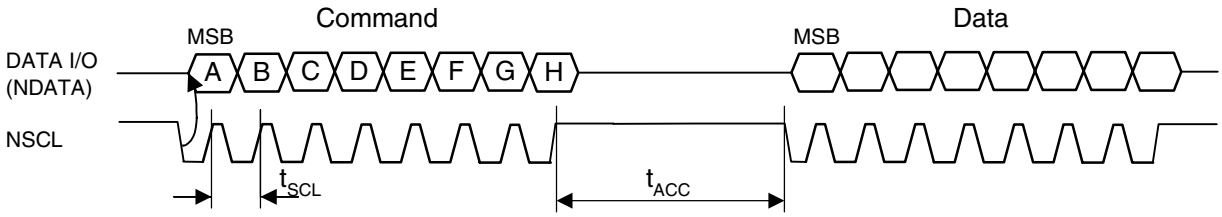


Serial Interface

General Description

The serial interface is an easy-to-handle 8-bit 2-wire interface. It always operates as a slave. The controller uses the NSCL input to shift a command into and data out of the internal shift register. The interface starts working with the first falling edge of NSCL. NDATA/NWAKEUP serves as bi-directional DATA I/O for command input and data output. The rising edge of NSCL is used to clock the command into the register of the ATA5282, while the falling edge is used to shift out the data. Data changes are always derived from the falling edge of NSCL. Two operating modes are implemented. One is the command mode that only requires an 8-bit input and does not prepare a data output. This mode is useful to control different operating modes of the ATA5282, as described on the following pages. The second mode is used to read out the current value of the AGC-counter that is related to the field strength of the input signal. The READ_FS command starts an internal sequence to store the value of the AGC into the shift register and switches the DATA I/O to output mode. After t_{ACC}, the controller must deliver another 8 shift clocks to clock out the information.

Figure 12. Serial Interface



Command and Data Register

The 8-bit command register is organized as follows:

Table 2. Command Register

MSB	Command						LSB	Function
FREEZE	CH_SEL 1	CH_SEL 2	READ_FS	SOFT_RES	FGC	not used	TEST MOD	Default value after reset: 00 hex
							0	Application mode active
							1	Test mode active
						X	For future use	
					0	Standard gain control active (AGC full range: 256 steps)		
					1	Fast gain control active (AGC full range: 128 steps)		
				0	No effect			
				1	Reset circuit to initial state			
			0	No effect				
			1	Read AGC-counter (field strength)				
	0	0	Coil input 1, 2, 3 active					
	0	1	Select Coil input 1 (disable 2 and 3)					
	1	0	Select Coil input 2 (disable 1 and 3)					
	1	1	Select Coil input 3 (disable 1 and 2)					
0	Automatic Gain Control (AGC) active							
1	AGC stopped with actual value							

Note: These commands, except FREEZE- and READ_FS, cause a reset of AGC to initial state.

Table 3. Data Register

MSB	Data						LSB	Function
AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0	Default value ’00’hex

Note: The content of the data register is updated every time a READ_FS command is given via the interface.

Command Description

Note: Every command except FREEZE- and READ_FS causes a reset of the AGC to its initial state.

TEST_MOD

Not for customer use, this mode is only used for production tests.

FGC

With FGC set to 1, the time for a full-range control cycle of the AGC is 128 steps instead of 256 steps as in standard mode. This divides the AGC settling time by 2, compared to the standard mode.

SOFT_RES

In addition to the internal hardware reset and watchdog functions, this bit allows the connected microcontroller to switch the circuit into the initial low-power state. All internal registers including the serial interface and the gain control counter are reset by this command.

READ_FS

As long as this bit is kept at 0, the interface is in write mode and accepts 8-bit commands only. Setting Read_FS to 1 enables to read out the digital 8-bit value of the gain control counter (RSSI), thus requiring two 8-bit accesses. The distance between the two accesses (t_{ACC}) must be >50 µs to allow proper operating and updating of the internal data register.

CH_SEL0,1

These two bits define the operation mode of the three channels. After reset, all channels are active. With the CH_SEL-bits, one of the three channels can be selected to be active, while the other two are disabled. The gain control is reset to the initial value if these bits are modified and operates only with the selected channel. This feature can be used for three-dimensional field strenght measurements or to suppress the influence of noise from disturbing channels.

FREEZE

When set to 1, this bit disables the automatic gain control and maintains the actual value for the gain of the input amplifiers. Even when changing the input amplitudes (for example, modulation through noise or movement), the gain is kept constant.

Example

The example shows how to program the circuit to operate on channel 1 only and to measure the field strength of the Coil 1 input signal.

Figure 13 shows the command entry which activates Coil 1 input only and also the fast gain control (FGC). The gain control counter is set to zero (highest sensitivity) by this command. The information is shifted into the ATA5282 with the rising edge of the shift clock.

Figure 13. Select Coil Input 1 + FGC

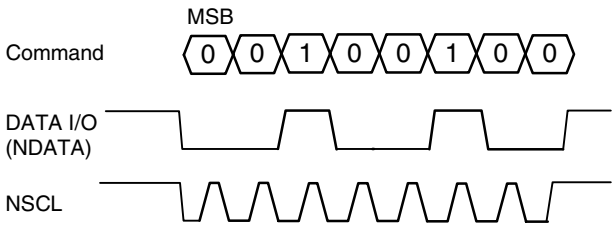
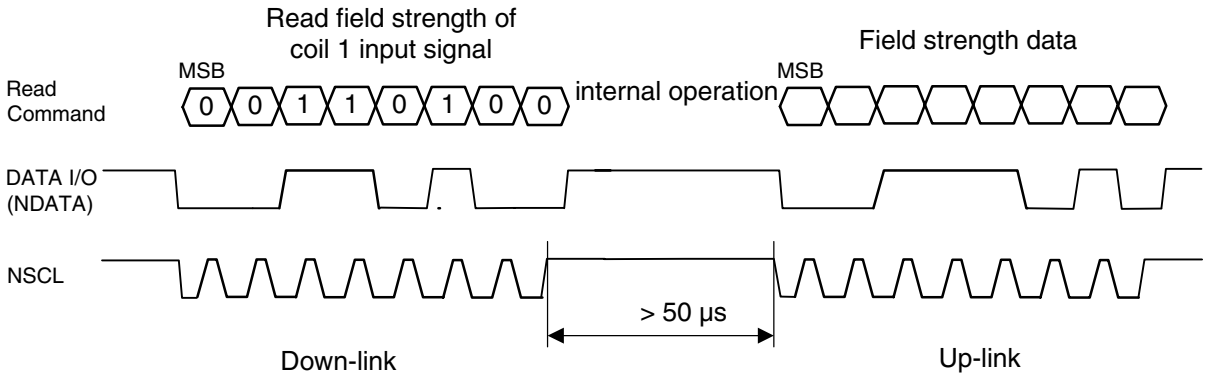


Figure 14 shows the second step, the read-out of the actual field strength of the signal applied to Coil 1.

When 128 steps have been passed, the gain control is finished and the value can be read out. This is performed by providing the command READ_FS with the information of the selected channel. 50 µs later, the ATA5282 has updated and stored the information into the internal shift register. Now the microcontroller can read the actual information by generating the next 8 shift clock pulses. The information changes on the falling edge of the clock pulse.

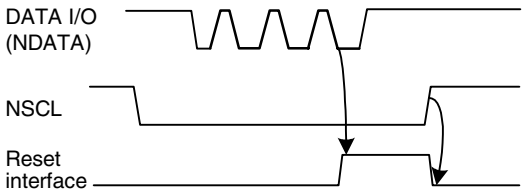
Figure 14. Read Field Strength of Channel 1



Reset Interface

To prevent the system from hanging or running into a deadlock condition due to disturbances on the NSCL line (hardware or software), a special function is provided to reset, the interface.

Figure 15. Reset Interface



Setting the NSCL to a low level and generating 4 clock pulses at the NDATA pin resets all interface-relevant registers and flip-flops, thus cancelling the deadlock condition and resynchronizing the interface.

Application

Figure 16 shows an application of the ATA5282. Combined with the antenna resonant circuit, the ATA5282 is used as wake-up receiver for the microcontroller. Additional to the antenna circuits the blocking filter - consisting of a RC element (R_1 = 100 Ω, C_1 = 10 nF) - is neccessary for the ATA5282. An additional resistor (R_2 = 2 MΩ/1%) should be placed at TC for oscillator tuning (optional: a parallel capacitor C_2 with maximum 10 pF).

Figure 16. Application Circuit

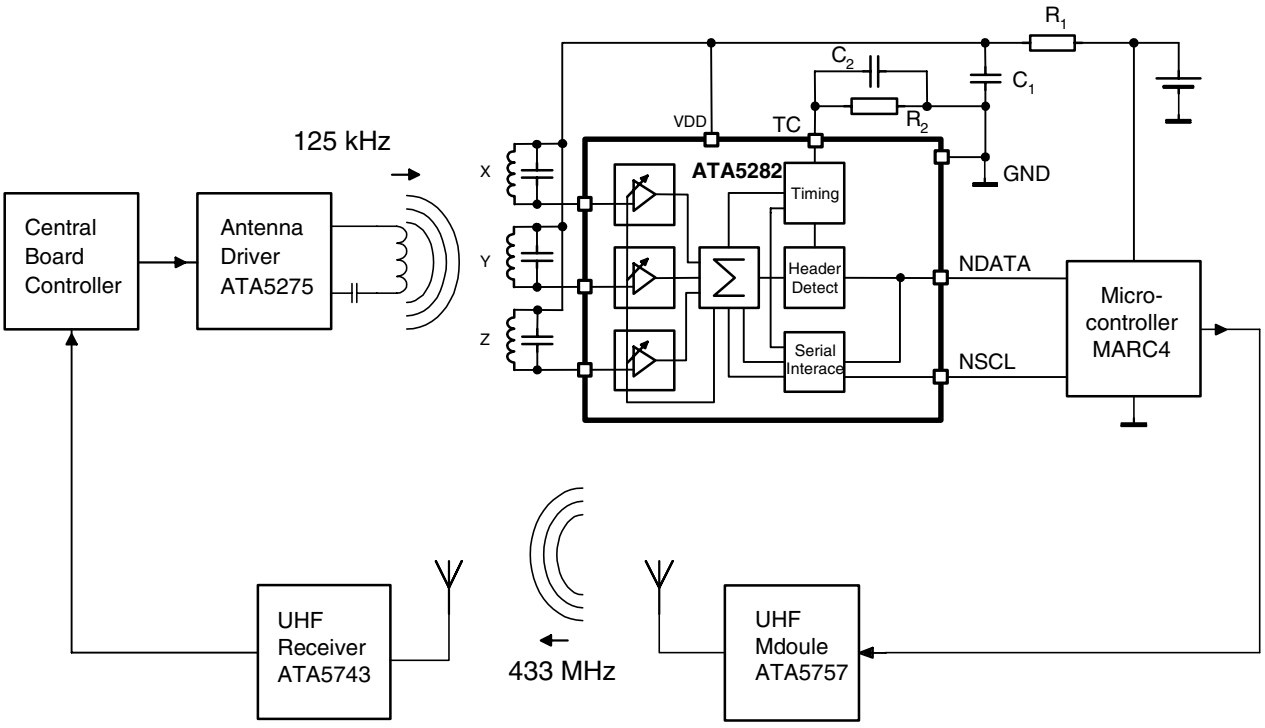
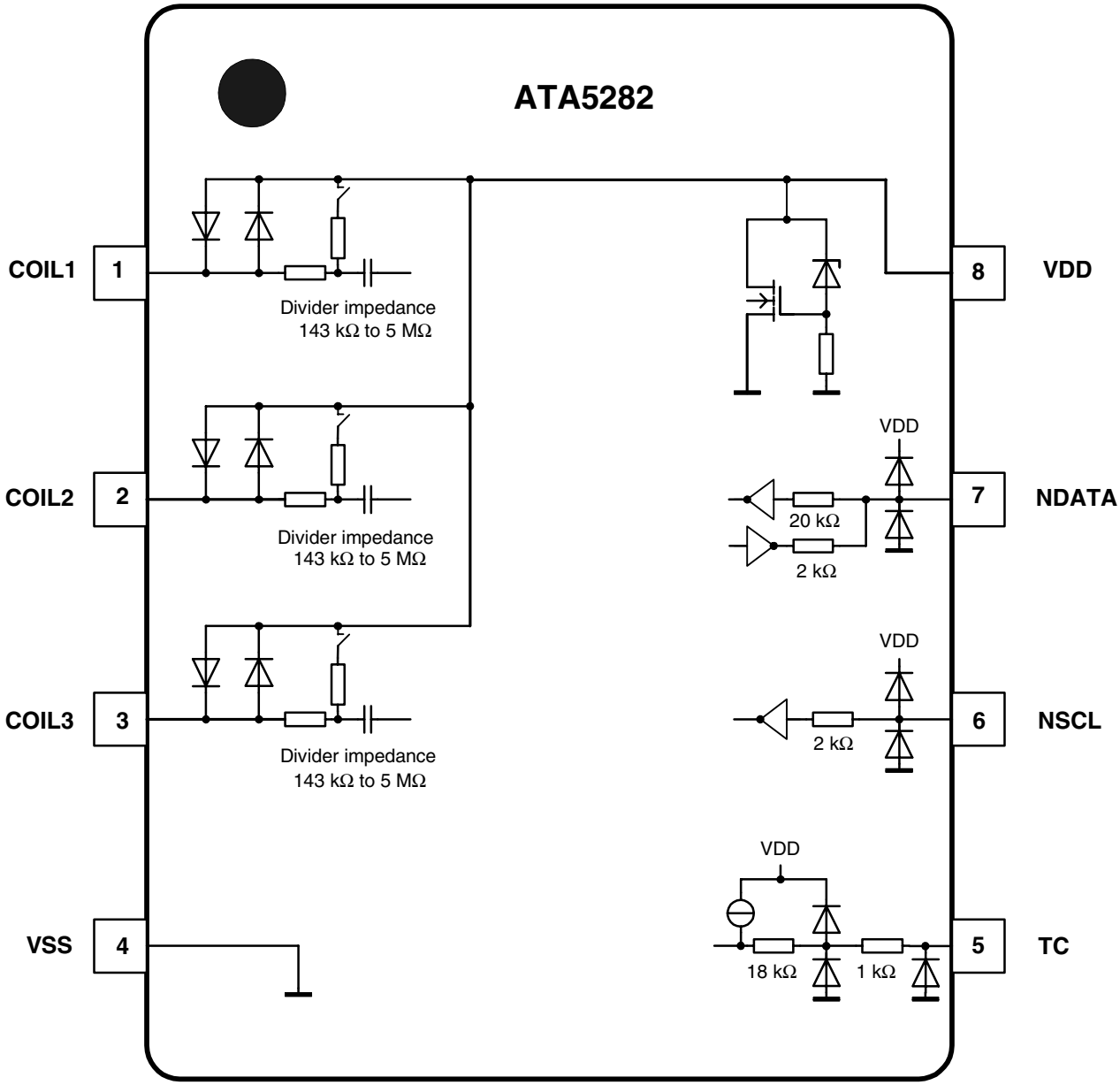


Figure 17. Pin Connection and Pin Protection



Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Power supply	V_{DD}	-0.3 to +6.5	V
Input voltage (except coil inputs)	V_{IN}	V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3	V
Input current coil	I_{CI}	±10	mA
Input voltage coil	V_{CI}	V_{DD} - 3.5 < V_{CI} < V_{DD} + 3.5	V
ESD protection (human body)	V_{ESD}	4	kV
Operating temperature range	T_{amb}	-40 to +85	°C
Storage temperature range	T_{stg}	-40 to +130	°C
Soldering temperatur	T_{sld}	260	°C
Thermal resistance (TSSOP 8L)	R_{thJA}	240	k/W

Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction-case	R_{thJC}	260	°C
Thermal resistance junction-ambient	R_{thJC}	240	°C

Operating Range

Parameters	Symbol	Value	Unit
Power supply range	V_{DD}	2 to 4.2	V
Operating temperature range	T_{OP}	-40 to +85	°C

Electrical Characteristics

V_{SS} = 0 V, V_{DD} = 3.2 V, T_{amb} = 25°C unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply and Coil Limiter**								
1.1	Power supply		8	V_{DD}	2	3.2	4.2	V	A
1.2	Supply current (initial state, AGC off)		8	I_{DD}		2	4	µA	A
1.3	Supply current (AGC active)		8	I_{DD}		4	6	µA	A
1.4	Power on reset threshold			V_{POR}	1	1.5	1.9	V	A
1.5	Power up time	Switch on V_{DD} to circuit active		V_{PON}			100	ms	C
1.6	RESET reactivation caused by negative spikes on V_{DD}	t_{BDN} = 500 ns	7	t_{RST}	10		100	µs	C
1.71 1.72 1.73	Coil input voltage refered to V_{DD} (Input Coil limiter for channels X, Y, Z)	I_{CI} = ±1 mA V_{DD} = 2.0 V V_{DD} = 3.2 V V_{DD} = 4.2 V	1, 2, 3	V_{CI}		±1.2 ±1.4 ±1.55		V_P V_P V_P	A
1.8	TC low current output	V_{O_TC} at 500 mV	5	I_{TC}	230	250	270	nA	A
1.9	Carrier frequency range		1, 2, 3	f_{CF}	100		150	kHz	D
2	**Amplifiers**								
2.1	Wake-up sensitivity	125-kHz input signal	7	V_{SENS}		2.8	3.6	mV_{PP}	A
2.2	Bandwith	Without Coil		B_W		200		kHz	C
2.3	Upper corner frequency	Without Coil		f_u		230		kHz	C
2.4	Lower corner frequency	Without Coil		f_o		30		kHz	C
2.5	Gain difference	Channel to channel	1, 2, 3	G_{DIFF}			±20	%	A
2.6	Input impedance	$V_{IN} \geq 2.8\ mV_{PP}$ at 125 kHz	1, 2, 3	R_{IN}	143			kΩ	A
2.7	Input capacitance		1, 2, 3	C_{IN}		10		pF	C
2.8	Coils Input Range	$V_{CI} = 2.8\ mV_{PP}$ $V_{CI} = 2.8\ V_{PP}$	1, 2, 3			60		dB	A
3	**Digital**								
3.1	Oscillator frequency	R_{EXT} = 2 MΩ and C_{EXT} maximum 10 pF		f_{OSC}	80	90	100	kHz	A
3.2	Preamble periods (not FGC)	$V_{CI} \geq 3.2V_{PP}$	1, 2, 3	n_{PAM}	320				A
3.3	Header detection windows (L = long, S = short) see Figure 8 on page 9	Tolerance included oscillator tolerance		t_{START_L}	160	182	205	µs	A
3.4				t_{END_L}	315	357	400	µs	A
3.5				t_{START_S}	40	50	60	µs	A
3.6				t_{END_S}	200	225	255	µs	A
3.7	Shift clock period		6	t_{NSCL}	10			µs	C
3.8	Data access time			t_{ACC}	50			µs	A
3.9	Data rate (Q < 20)	125 kHz ASK		D_{RATE}		4		kbps	A
3.10	Delay time RF signal to data	125 kHz ASK		t_{ON}		40		µs	A
3.11	Delay time RF signal to data	125 kHz ASK		t_{OFF}		40		µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics (Continued)

V_{SS} = 0 V, V_{DD} = 3.2 V, T_{amb} = 25°C unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	**Interface**								
4.1	NSCL input level LOW		6	V_{IL_NSCL}	V_{SS}		$0.2 \times V_{DD}$	V	A
4.2	NSCL input level HIGH		6	V_{IH_NSCL}	$0.8 \times V_{DD}$		V_{DD}	V	A
4.3	NSCL input leakage current LOW	$V_{NSCL} = V_{SS}$	6	I_{IL_NSCL}	-200		0	nA	A
4.4	NSCL input leakage current HIGH	$V_{NSCL} = V_{DD}$	6	I_{IH_NSCL}	0		+200	nA	A
4.5	NDATA input level LOW	$V_{NSCL} = V_{SS}$	7	V_{IL_NDAT}	V_{SS}		$0.2 \times V_{DD}$	V	A
4.6	NDATA input level HIGH	$V_{NSCL} = V_{SS}$	7	V_{IH_NDAT}	$0.8 \times V_{DD}$		V_{DD}	V	A
4.7	NDATA input leakage current LOW	$V_{NDAT} = V_{SS}$ $V_{NSCL} = V_{SS}$	7	I_{IL_NDAT}	-200		0	nA	A
4.8	NDATA input leakage current HIGH	$V_{NDAT} = V_{DD}$ $V_{NSCL} = V_{SS}$	7	I_{IH_NDAT}	0		+200	nA	A
4.9	NDATA output level LOW	I_{NDAT} = +100 µA $V_{NSCL} = V_{DD}$	7	V_{OL_NDAT}	V_{SS}		$0.2 \times V_{DD}$	V	A
4.10	NDATA output level HIGH	I_{NDAT} = -100 µA $V_{NSCL} = V_{DD}$	7	V_{OL_NDAT}	$0.8 \times V_{DD}$		V_{DD}	V	A

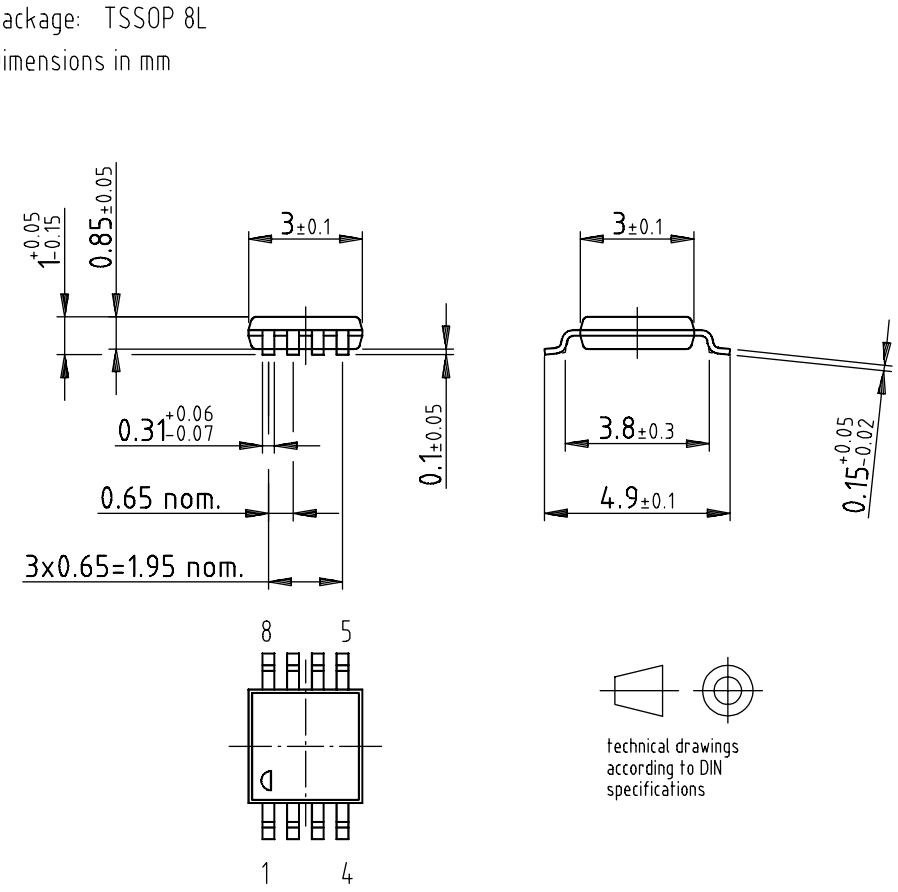
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Ordering Information

Extended Type Number	Package	Remarks
ATA5282	TSSOP 8L	–

Package Information

Figure 18. Package TSSOP 8L



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