THE DATASHEET OF

LTC1148CS#PBF

www.win-source.net 0086-755-83957316

High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Ultrahigh Efficiency: Over 95% Possible**
- Current-Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Three Decades of Output Current
- Low 160μA Standby Current at Light Loads
- Logic Controlled Micropower Shutdown: I_Q < 20μA
- Wide V_{IN} Range: 3.5V* to 20V
- Short-Circuit Protection
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Adaptive Nonoverlap Gate Drives
- Output Can Be Externally Held High in Shutdown
- Available in 14-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC®1148 series is a family of synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture providing constant ripple current in the inductor.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V* to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited by only the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1148 series combines synchronous switching for maximum efficiency at high currents with an automatic low current operating mode, called Burst Mode operation, which reduces switching losses. Standby power is reduced to only 2mW at V_{IN} = 10V (at I_{OUT} = 0). Load currents in Burst Mode operation are typically 0mA to 300mA.

For operation up to 48V input, see the LTC1149 and LTC1159 data sheets and Application Note 54.

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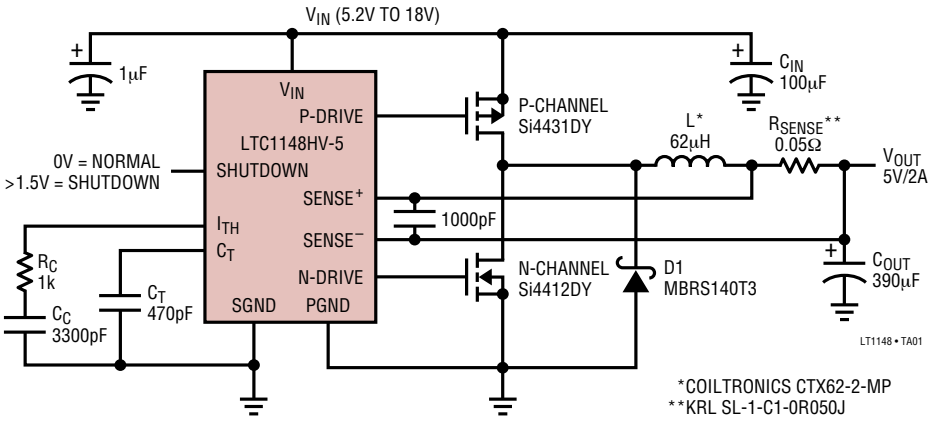
Burst Mode is a trademark of Linear Technology Corporation.
* LTC1148L and LTC1148L-3.3 only.
Protected by U.S. Patents, including 6580258, 5481178.

TYPICAL APPLICATION



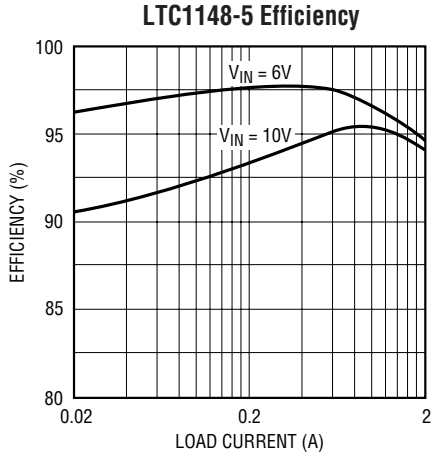


Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (Pin 3)
- LTC1148 and LTC1148L Series ..... 16V to –0.3V
- LTC1148HV Series ..... 20V to –0.3V

Continuous Output Current (Pins 1, 14) 50mA

Sense Voltages (Pins 7, 8)
- LTC1148HV (Adjustable Only)
  - $V_{IN} \geq 12.7V$ ..... 13V to –0.3V
  - $V_{IN} < 12.7V$ ..... (V_{IN} + 0.3V) to –0.3V

Operating Ambient Temperature Range ..... 0°C to 70°C

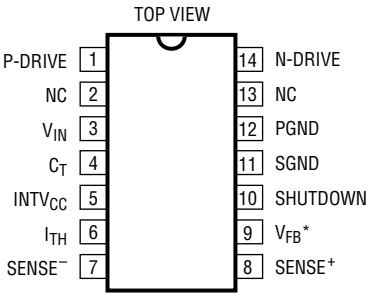
Extended Commercial and Industrial Temperature Range ..... –40°C to 85°C

Junction Temperature (Note 2) ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
14-LEAD PDIP

S PACKAGE
14-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS = NC

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1148CN
LTC1148HVCN
LTC1148CN-3.3
LTC1148HVCN-3.3
LTC1148CN-5
LTC1148HVCN-5
LTC1148CS
LTC1148HVCS
LTC1148LCS
LTC1148CS-3.3
LTC1148HVCS-3.3
LTC1148LCS-3.3
LTC1148CS-5
LTC1148HVCS-5
LTC1148HVIS-5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_9	Feedback Voltage (LTC1148, LTC1148L, LTC1148HV)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_9	Feedback Current (LTC1148, LTC1148L, LTC1148HV)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage V_{IN} = 9V						
	LTC1148-3.3, LTC1148HV-3.3, LTC1148L-3.3	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	LTC1148-5, LTC1148HV-5	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation						
	LTC1148-3.3, LTC1148HV-3.3, LTC1148L-3.3	5mA < I_{LOAD} < 2A	●		40	65	mV
	LTC1148-5, LTC1148HV-5	5mA < I_{LOAD} < 2A	●		60	100	mV
	Output Ripple (Burst Mode)	I_{LOAD} = 0A			50		mV_{P-P}
I_Q	Input DC Supply Current (Note 3)	(Note 7)					
	LTC1148 Series						
	Normal Mode	4V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	4V < V_{IN} < 12V			160	230	µA
	Sleep Mode (LTC1148-5)	6V < V_{IN} < 12V			160	230	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 12V			10	20	µA
	LTC1148HV Series						
	Normal Mode	4V < V_{IN} < 18V			1.6	2.3	mA
	Sleep Mode	4V < V_{IN} < 18V			160	250	µA
	Sleep Mode (LTC1148HV-5)	6V < V_{IN} < 18V			160	250	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 18V			10	22	µA
	LTC1148L Series						
	Normal Mode	3.5V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	3.5V < V_{IN} < 12V			160	230	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 3.5V < V_{IN} < 12V			10	20	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_8 - V_7$	Current Sense Threshold Voltage LTC1148, LTC1148HV, LTC1148L	 V_{SENSE}^- = 5V, $V_9 = V_{OUT}/4 + 25mV$ (Forced) V_{SENSE}^- = 5V, $V_9 = V_{OUT}/4 - 25mV$ (Forced)	 ●	 130	 25 150	 170	 mV mV
	LTC1148-3.3, LTC1148HV-3.3 LTC1148L-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)	 ●	 130	25 150	 170	mV mV
	LTC1148-5, LTC1148HV-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)	 ●	 130	25 150	 170	mV mV
V_{10}	Shutdown Pin Threshold			0.5	0.8	2	V
I_{10}	Shutdown Pin Input Current	0V < $V_{SHUTDOWN}$ < 8V, V_{IN} = 16V			1.2	5	µA
I_4	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT} V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off Time (Note 5)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_R, t_F	Driver Output Transition Times	C_L = 3000pF (Pins 1, 14), V_{IN} = 6V			100	200	ns

–40°C ≤ T_A ≤ 85°C (Note 5), V_{IN} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_9	Feedback Voltage (LTC1148, LTC1148HV LTC1148L)	V_{IN} = 9V		1.20	1.25	1.30	V
ΔV_{OUT}	Regulated Output Voltage LTC1148-3.3, LTC1148HV-3.3, LTC1148L-3.3 LTC1148-5, LTC1148HV-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA		 3.17 4.85	 3.33 5.05	 3.43 5.20	 V V
I_Q	Input DC Supply Current (Note 3) LTC1148 Series Normal Mode Sleep Mode Sleep Mode Shutdown LTC1148HV Series Normal Mode Sleep Mode Sleep Mode Shutdown LTC1148L Series Normal Mode Sleep Mode Shutdown	(Note 7) 4V < V_{IN} < 12V 4V < V_{IN} < 12V 6V < V_{IN} < 12V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 12V 4V < V_{IN} < 18V 4V < V_{IN} < 18V 6V < V_{IN} < 18V $V_{SHUTDOWN}$ = 2.1V, 4V < V_{IN} < 18V 3.5V < V_{IN} < 12V 3.5V < V_{IN} < 12V $V_{SHUTDOWN}$ = 2.1V, 3.5V < V_{IN} < 12V		 	 1.6 160 160 10 1.6 160 160 10 1.6 160 10	 2.4 260 260 22 2.6 280 280 24 2.4 260 22	 mA µA µA µA mA µA µA µA mA µA µA
$V_8 - V_7$	Current Sense Threshold Voltage LTC1148, LTC1148HV, LTC1148L (Note 4)	 V_{SENSE}^- = 5V, $V_9 = V_{OUT}/4 - 25mV$ (Forced) V_{SENSE}^- = 5V, $V_9 = V_{OUT}/4 + 25mV$ (Forced)	 	 125	 25 150	 175	 mV mV
	LTC1148-3.3, LTC1148HV-3.3, LTC1148L-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)	 	 125	25 150	 175	mV mV
	LTC1148-5, LTC1148HV-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced) V_{SENSE}^- = V_{OUT} – 100mV (Forced)	 	 125	25 150	 175	mV mV
V_{10}	Shutdown Pin Threshold			0.55	0.8	2	V
t_{OFF}	Off Time (Note 5)	C_T = 390pF, I_{LOAD} = 700mA		3.8	5	6	µs

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC1148CN, LTC1148CN-3.3, LTC1148CN-5: $T_J = T_A + (P_D \times 70°C/W)$

LTC1148CS, LTC1148CS-3.3, LTC1148CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 4: The LTC1148 and LTC1148HV versions are tested with external feedback resistors resulting in a nominal output voltage of 5V. The LTC1148L version is tested with external feedback resistors resulting in a nominal output voltage of 2.5V.

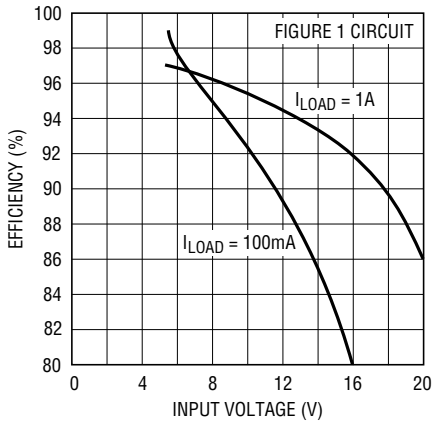
Note 5: In applications where R_{SENSE} is placed at ground potential, the off time increases approximately 40%.

Note 6: The LTC1148, LTC1148HV and LTC1148L series are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation. The LTC1148HVI-5 is guaranteed over the full –40°C to 85°C operating temperature range.

Note 7: The LTC1148L and LTC1148L-3.3 allow operation to V_{IN} = 3.5V.

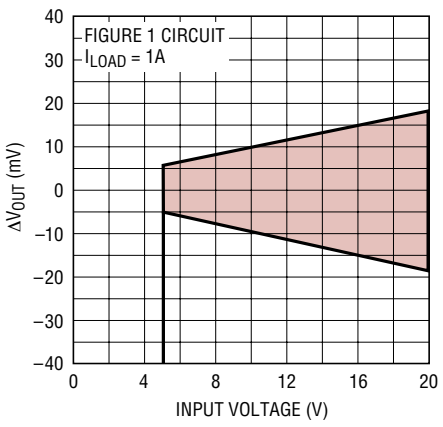
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



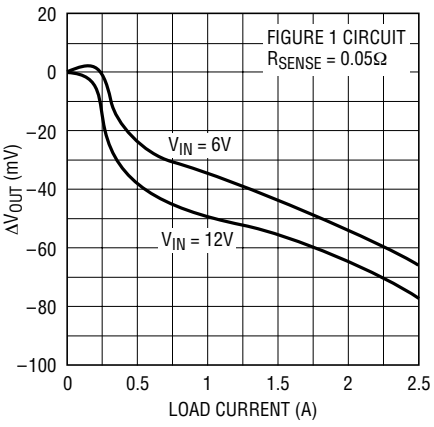
LTC1148 • TPC01

Line Regulation



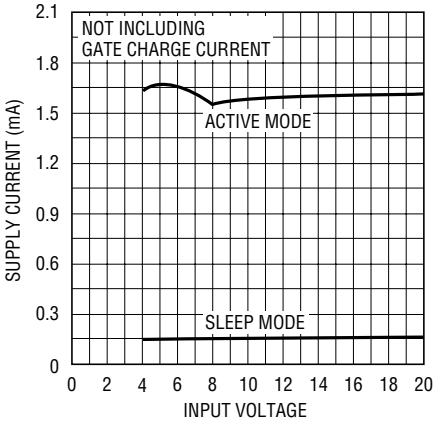
LTC1148 • TPC02

Load Regulation



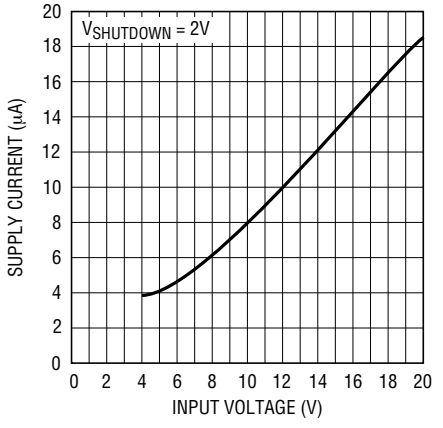
LTC1148 • TPC03

DC Supply Current



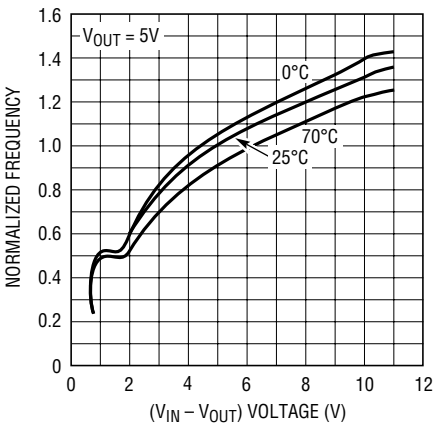
LTC1148 • TPC04

Supply Current in Shutdown



LTC1148 • TPC05

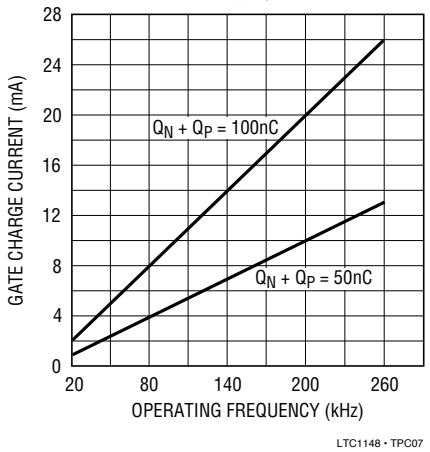
Operating Frequency vs ($V_{IN} – V_{OUT}$)



LTC1148 • TPC06

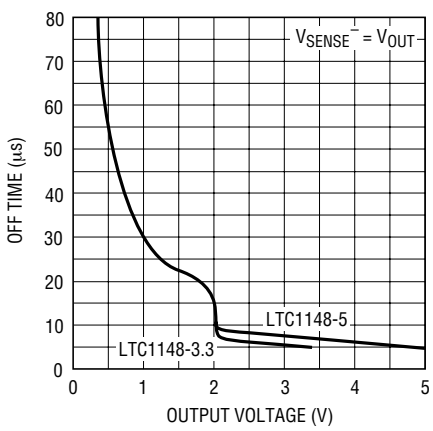
TYPICAL PERFORMANCE CHARACTERISTICS

Gate Charge Supply Current



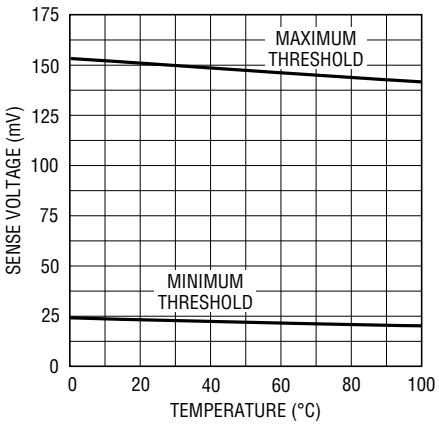
LTC1148 • TPC07

Off Time vs V_{OUT}



LTC1148 • TPC08

Current Sense Threshold Voltage



LTC1148 • TPC09

PIN FUNCTIONS

P-DRIVE (Pin 1): High Current Drive for Top P-Channel MOSFET. Voltage swing at this pin is from V_{IN} to ground.

NC (Pin 2): No Connection. Can connect to power ground.

V_{IN} (Pin 3): Main Supply Pin. Must be closely decoupled to power ground Pin 12.

C_T (Pin 4): External capacitor C_T from Pin 4 to ground sets the operating frequency. The actual frequency is also dependent upon the input voltage.

$INTV_{CC}$ (Pin 5): Internal Supply Voltage, Nominally 3.3V. Can be decoupled to signal ground. Do not externally load this pin.

I_{TH} (Pin 6): Gain Amplifier Decoupling Point. The current comparator threshold increases with the Pin 6 voltage.

$SENSE^-$ (Pin 7): Connects to internal resistive divider which sets the output voltage in LTC1148-3.3 and LTC1148-5 versions. Pin 7 is also the (–) input for the current comparator.

$SENSE^+$ (Pin 8): The (+) Input to the Current Comparator. A built-in offset between Pins 7 and 8 in conjunction with R_{SENSE} sets the current trip threshold.

V_{FB} (Pin 9): For the LTC1148 adjustable version, Pin 9 serves as the feedback pin from an external resistive divider used to set the output voltage. On LTC1148-3.3 and LTC1148-5 versions this pin is not used.

SHUTDOWN (Pin 10): When grounded, the LTC1148 series operates normally. Pulling Pin 10 high holds both MOSFETs off and puts the LTC1148 series in micropower shutdown mode. Requires CMOS logic signal with t_R, $t_F < 1\mu s$, should not be left floating.

SGND (Pin 11): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

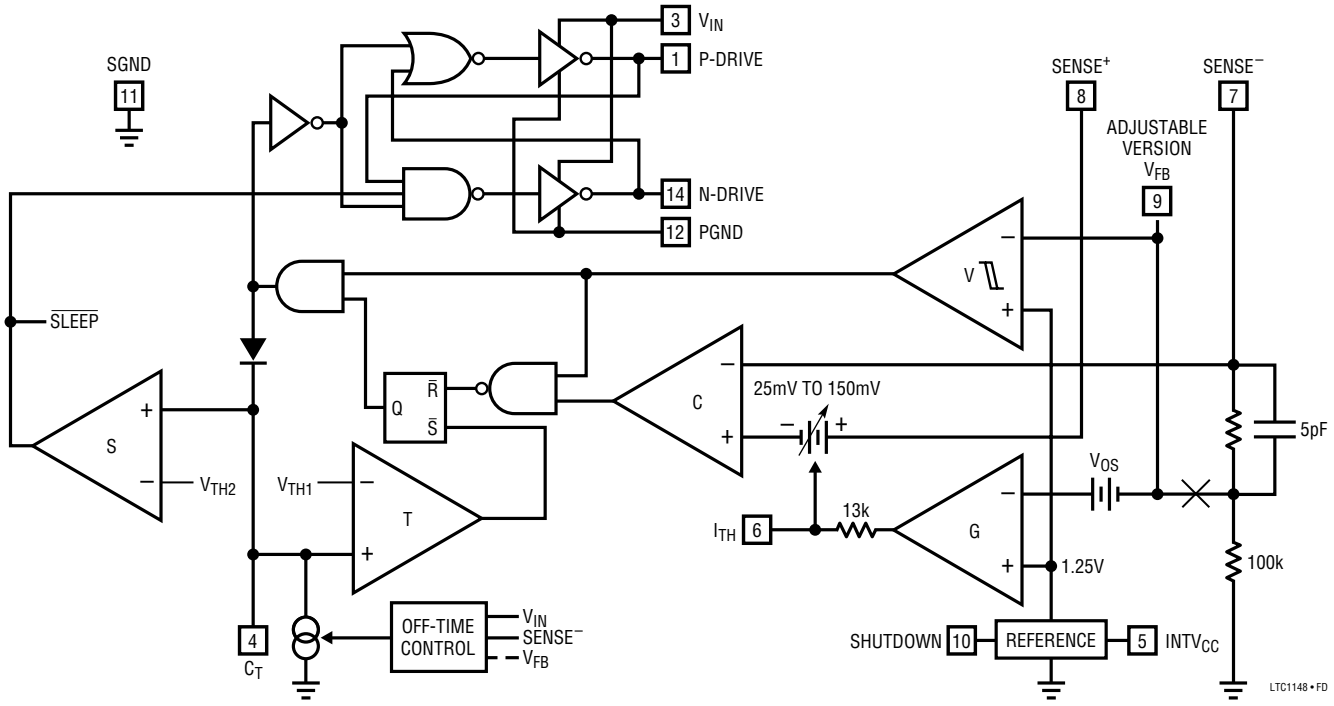
PGND (Pin 12): Driver Power Ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

NC (Pin 13): No Connection. Can connect to power ground.

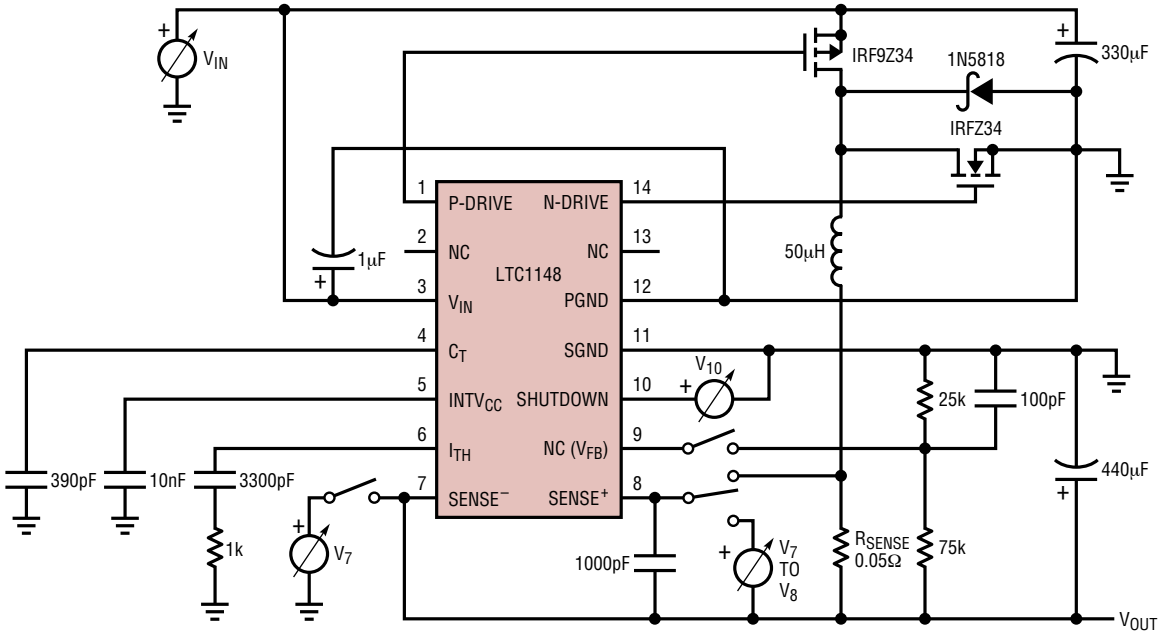
N-DRIVE (Pin 14): High Current Drive for Bottom N-Channel MOSFET. Voltage swing at Pin 14 is from ground to V_{IN}.

FUNCTIONAL DIAGRAM

Pin 9 connection shown for LTC1148-3.3 and LTC1148-5; changes create LTC1148.



TEST CIRCUIT



OPERATION

The LTC1148 series uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the timing capacitor Pin 4.

The output voltage is sensed by an internal voltage divider connected to SENSE$^-$ Pin 7 (LTC1148-3.3 and LTC1148-5) or external divider returned to V_{FB} Pin 9 (LTC1148). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1148 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Pins 7 and 8 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to Pin 4 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by Pin 7) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-drive output goes to V_{IN}, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-drive output to go low (turning off the N-channel MOSFET) and the P-drive output to also go low (turning the P-channel MOSFET back on). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (Pin 6) to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{sleep}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160μA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and the process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset (V_{OS}) is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-drive output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low while the N-drive output is high.

Using constant off-time architecture, the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing extremely low dropout operation.

APPLICATIONS INFORMATION

The basic LTC1148 series application circuit (fixed output versions) is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 20V. If the application requires higher input voltage, then the LTC1149 or LTC1159 should be used.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1148 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (See C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1148 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

The load current below which Burst Mode operation commences (I_{BURST}) and the peak short-circuit current ($I_{SC(PK)}$) both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

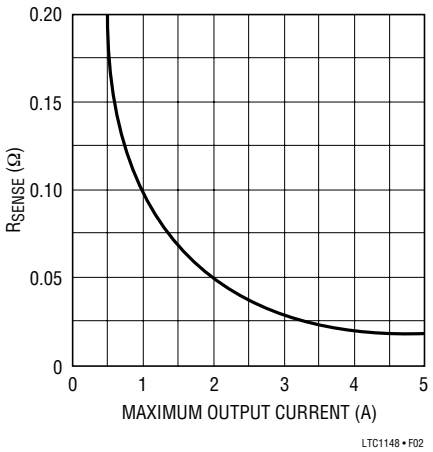


Figure 2. Selecting R_{SENSE}

The LTC1148 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1148 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{1}{2.6(10^4)f}$$

Assumes $V_{IN} = 2V_{OUT}$, Figure 1 circuit.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

APPLICATIONS INFORMATION

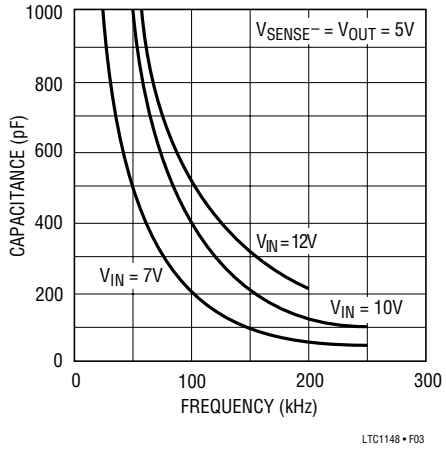


Figure 3. Timing Capacitor Value

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3(10^4)C_T\left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus V_{REG}/V_{OUT} = 1 in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V, the LTC1148 series reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1(10^5)R_{SENSE}(C_T)V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1148 series may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, Kool Mμ® on molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids, with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequencies, but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1148 series: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4V) may be used. If V_{IN} is expected to drop below 8V, logic-

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level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are strongly recommended. The LTC1148/LTC1148HV series supply voltage must always be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1148 series is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN}(P_P)}{V_{OUT}(I_{MAX}^2)(1 + \delta_P)}$$

$$\text{N-Ch } R_{DS(ON)} = \frac{V_{IN}(P_N)}{(V_{IN} - V_{OUT})(I_{MAX}^2)(1 + \delta_N)}$$

where P_P and P_N are the allowable power dissipations and d_P and d_N are the temperature dependencies of $R_{DS(ON)}$. P_P and P_N will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). (1 + d) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but d = 0.007/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diode D1 shown in Figure 1 only conducts during the dead-time between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question. An additional 0.1μF to 1μF ceramic capacitor is also required on V_{IN} Pin 3 for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1148 series:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

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In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1148 series would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

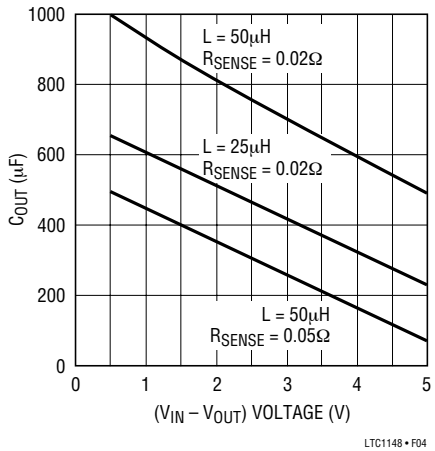

Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 6 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power).

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1148 series circuits: 1) LTC1148 DC bias current, 2) MOSFET gate charge current, and 3) I^2R losses.

1. The DC supply current is the current which flows into V_{IN} Pin 3 less the gate charge current. For V_{IN} = 10V the

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LTC1148 DC supply current is 160μA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1148 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f (Q_N + Q_P)$. The typical gate charge for a 0.1Ω N-channel power MOSFET is 25nC, and for a P-channel about twice that value. This results in $I_{GATECHG}$ = 7.5mA in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.

   Figure 5 shows how the efficiency losses in a typical LTC1148 series regulator end up being apportioned.

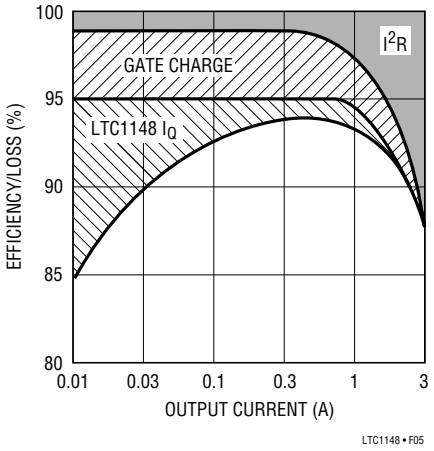

Figure 5. Efficiency Loss

   The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during dead time, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{OUT} = 5V, I_{MAX} = 2A, and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/2 = 0.05\Omega$

$t_{OFF} = (1/200kHz)[1 – (5/12)] = 2.92\mu s$

$C_T = 2.92\mu s/[(1.3)(10^4)] = 220pF$

$L_{MIN} = 5.1(10^5)0.05\Omega(220pF)5V = 28\mu H$

Assume that the MOSFET dissipations are to be limited to $P_N = P_P$ = 250mW.

If T_A = 50°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 63°C

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and $\delta_P = \delta_N = 0.007(63 - 25) = 0.27$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2\,(1.27)} = 0.12\Omega$$

$$\text{N-Ch } R_{DS(ON)} = \frac{12(0.25)}{7(2)^2\,(1.27)} = 0.085\Omega$$

The P-channel requirement can be met by a Si9430DY, while the N-channel requirement is exceeded by a Si9410DY. Note that the most stringent requirement for the N-channel MOSFET is with $V_{OUT} = 0$ (i.e., short circuit). During a continuous short circuit, the worst-case N-channel dissipation rises to:

$$P_N = I_{SC(AVG)}^2(R_{DS(ON)})(1 + \delta_N)$$

With the 0.05Ω sense resistor $I_{SC(AVG)}$ = 2A will result, increasing the 0.085Ω N-channel dissipation to 450mW at a die temperature of 73°C.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time, causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V:

$$f_{MIN} = (1/2.92\mu s)[1 - (5V/7V)] = 98kHz$$

$$P_P = \frac{5V(0.12\Omega)(2A)^2(1.27)}{7V} = 435mW$$

This last step is necessary to assure that the power dissipation and junction temperature of the P-channel are not exceeded.

LTC1148 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1148 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB} Pin 9 (see Figure 9). The regulated voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1148.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

Auxiliary Windings – Suppressing Burst Mode Operation

The LTC1148 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the SENSE⁻ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 6. Two 100Ω resistors are inserted in series with the leads from the sense resistor.

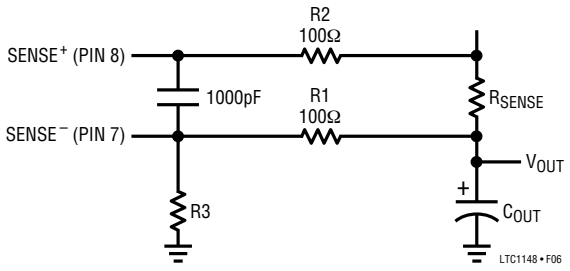

Figure 6. Suppression of Burst Mode Operation

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With the addition of R3, a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the minimum threshold will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Pins 7 and 8.

Output Crowbar

An added feature to using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. Pulling the timing capacitor Pin 4 above 1.5V when the output voltage is greater than the desired regulated value will turn "on" the N-channel MOSFET.

A fault condition which causes the output voltage to go above a maximum allowable value can be detected by external circuitry. Turning on the N-channel MOSFET when this fault is detected will cause large currents to flow and blow the system fuse.

The N-channel MOSFET needs to be sized so it will safely handle this overcurrent condition. The typical delay from pulling the C_T pin high and the N drive Pin 14 going high is 250ns. Note: Under shutdown conditions, the N-channel is held OFF and pulling the C_T pin high will not cause the N-channel MOSFET to crowbar the output.

A simple N-channel FET can be used as an interface between the overvoltage detect circuitry and the LTC1148 as shown in Figure 7.

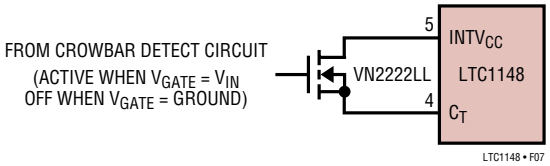

Figure 7. Output Crowbar Interface

Troubleshooting Hints

Since efficiency is critical to LTC1148 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor Pin 4.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 8a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation should occur with the C_T pin waveform periodically falling to ground as shown in Figure 8b.

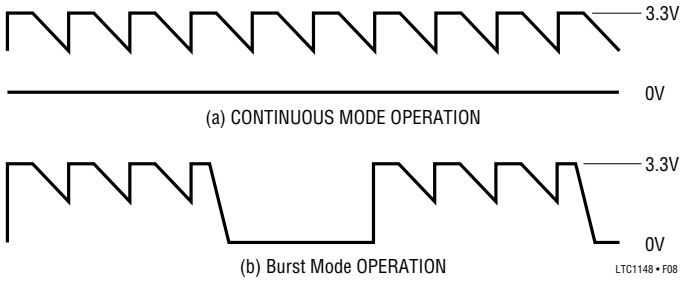

Figure 8. C_T Waveforms

If Pin 4 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

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Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1148 series. These items are also illustrated graphically in the layout diagram of Figure 9. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1148 signal ground Pin 11 must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1148 SENSE$^-$ Pin 7 connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 7 and 8 should be as close as possible to the LTC1148.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.
5. Is the 1µF V_{IN} decoupling capacitor connected closely between Pin 3 and power ground Pin 12? This capacitor carries the MOSFET driver peak currents.
6. Is the Shutdown Pin 10 actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

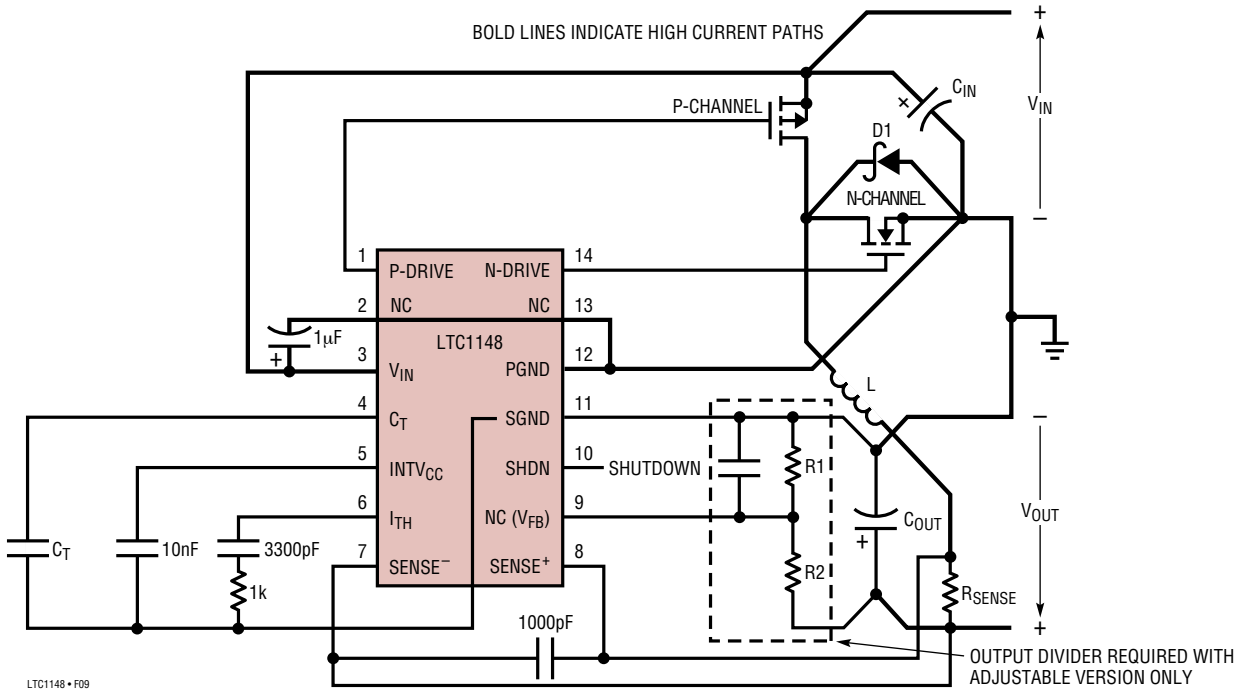


Figure 9. LTC1148 Layout Diagram (See Board Layout Checklist)

TYPICAL APPLICATIONS

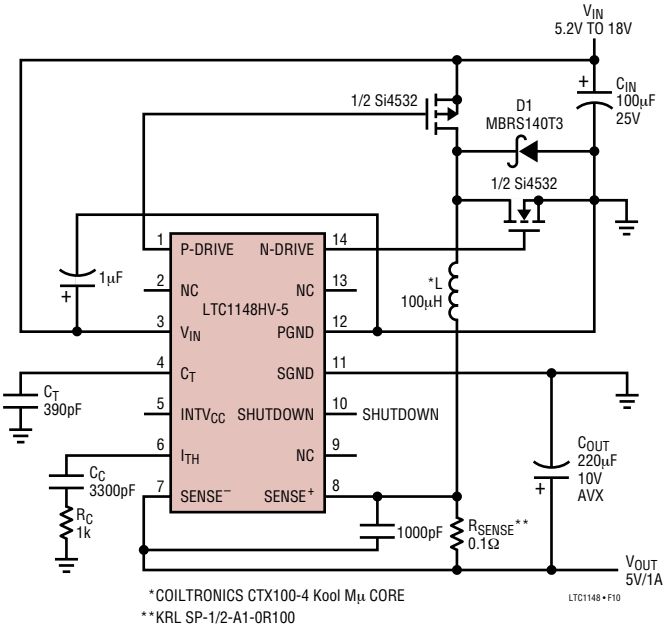


Figure 10. 5V/1A High Efficiency Regulator with Extended Input Voltage Range

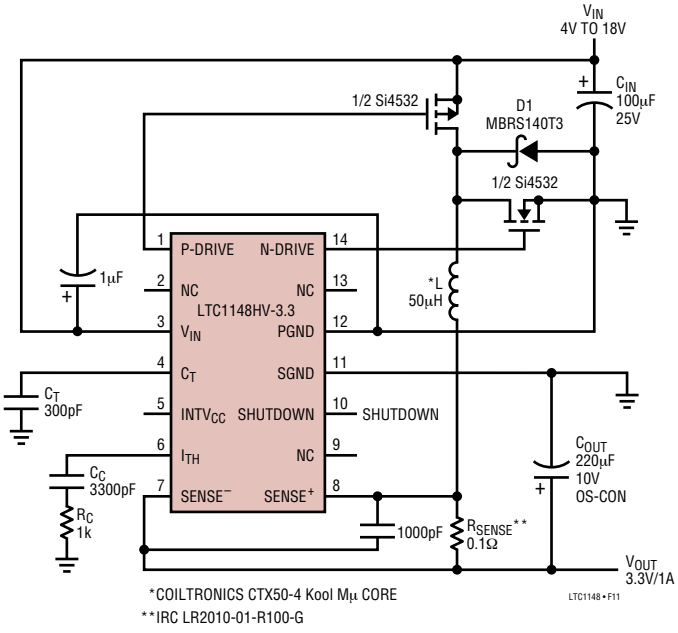


Figure 11. High Efficiency 5V to 3.3V/1A Converter with Extended Input Voltage Range

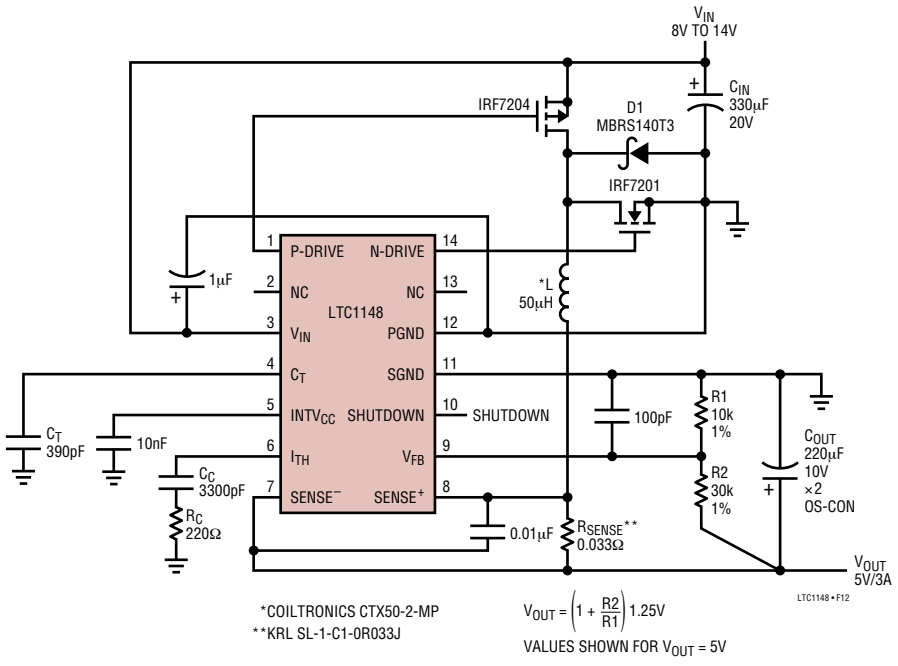


Figure 12. High Efficiency Adjustable 3A Regulator

TYPICAL APPLICATIONS

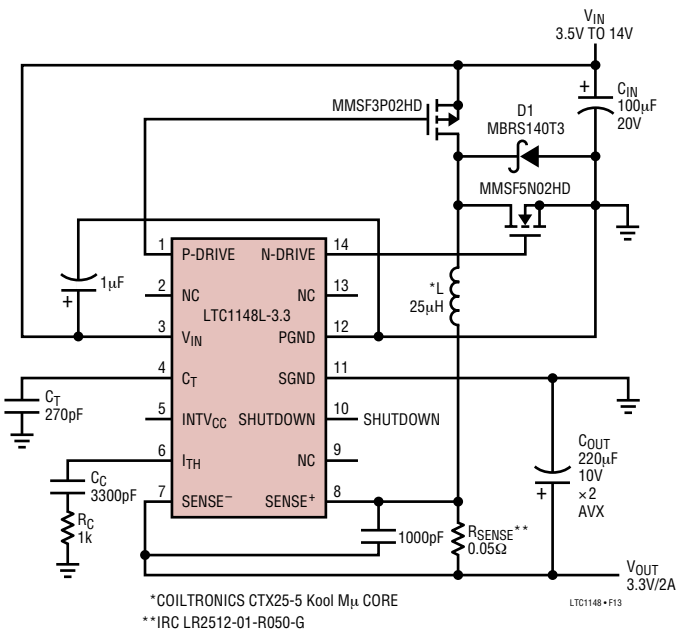


Figure 13. 5V Input Voltage, 3.3V/2A Low Dropout, High Efficiency Regulator

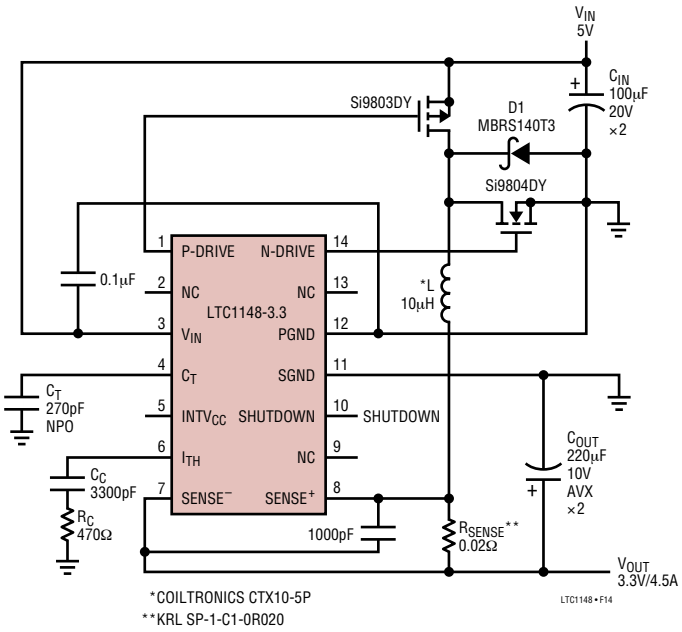


Figure 14. High Efficiency 5V to 3.3V/4.5A Converter

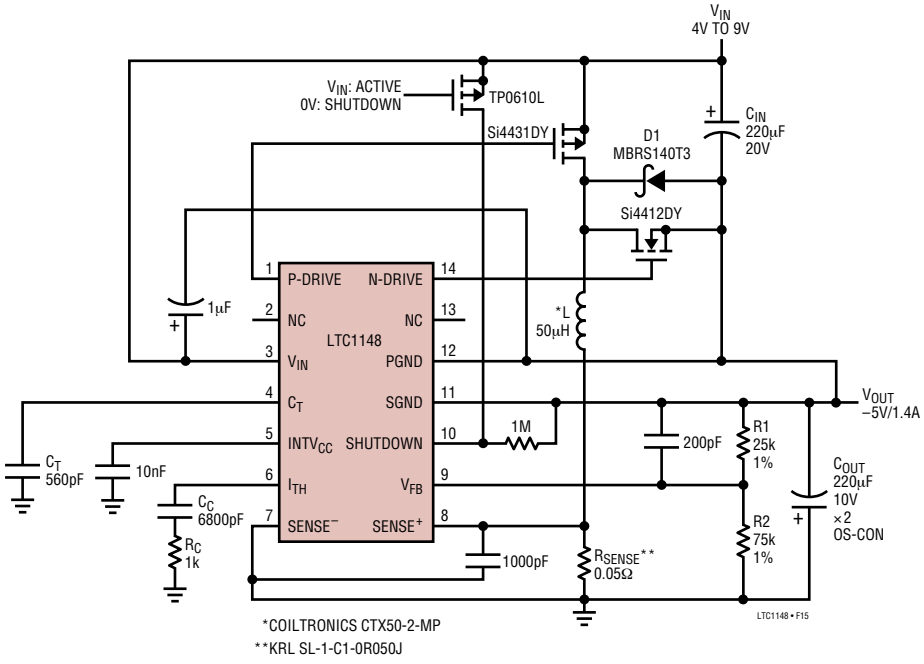


Figure 15. 4V to 9V Input Voltage to –5V/1A Regulator

TYPICAL APPLICATIONS

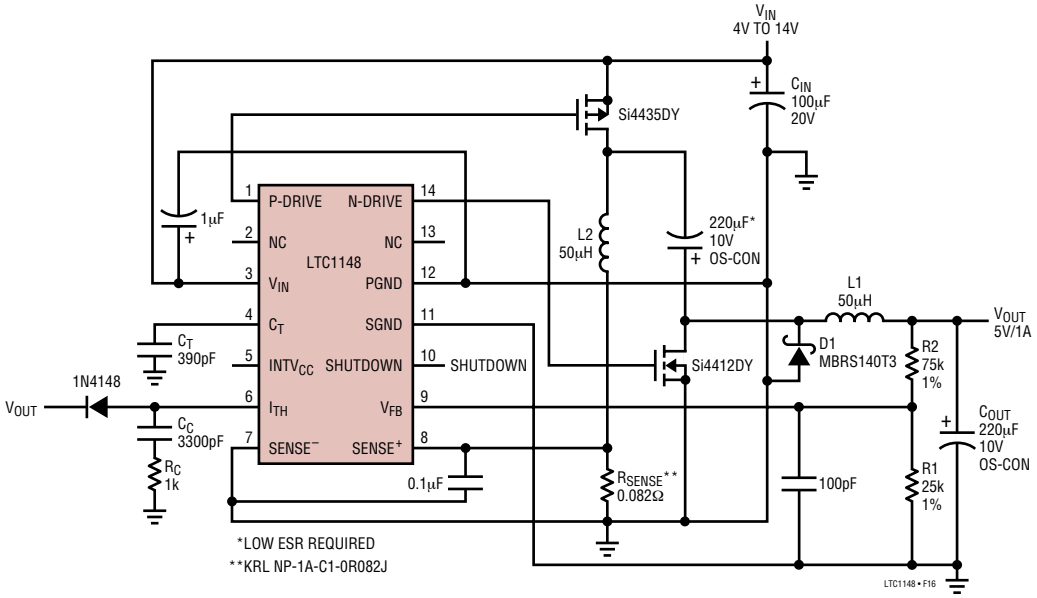


Figure 16. 4V to 14V Input Voltage to 5V/1A Regulator with Current Foldback

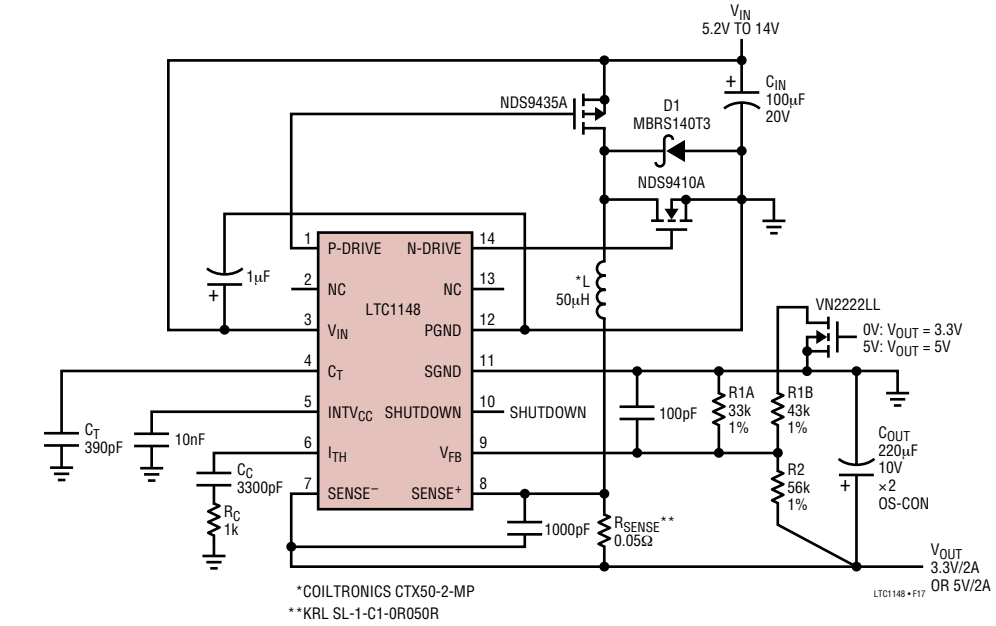
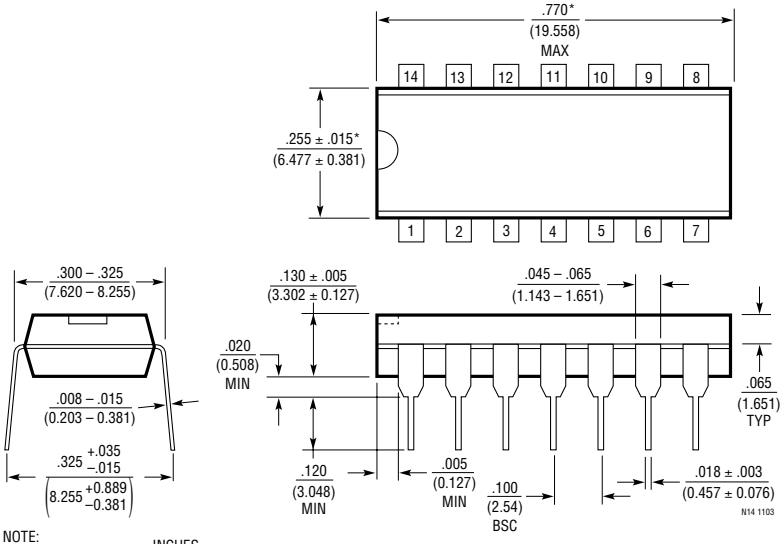


Figure 17. Logic Selectable 5V/1A or 3.3V/1A High Efficiency Regulator

PACKAGE DESCRIPTION

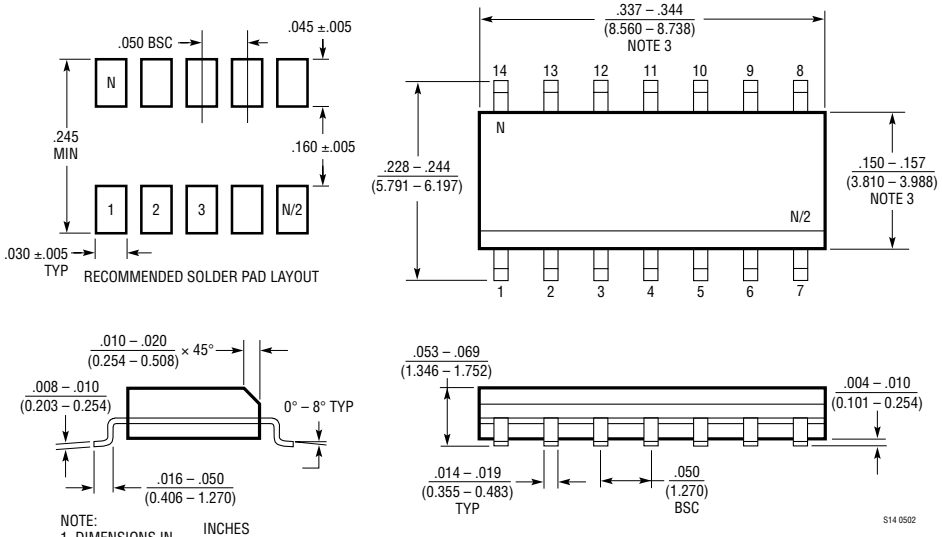
N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

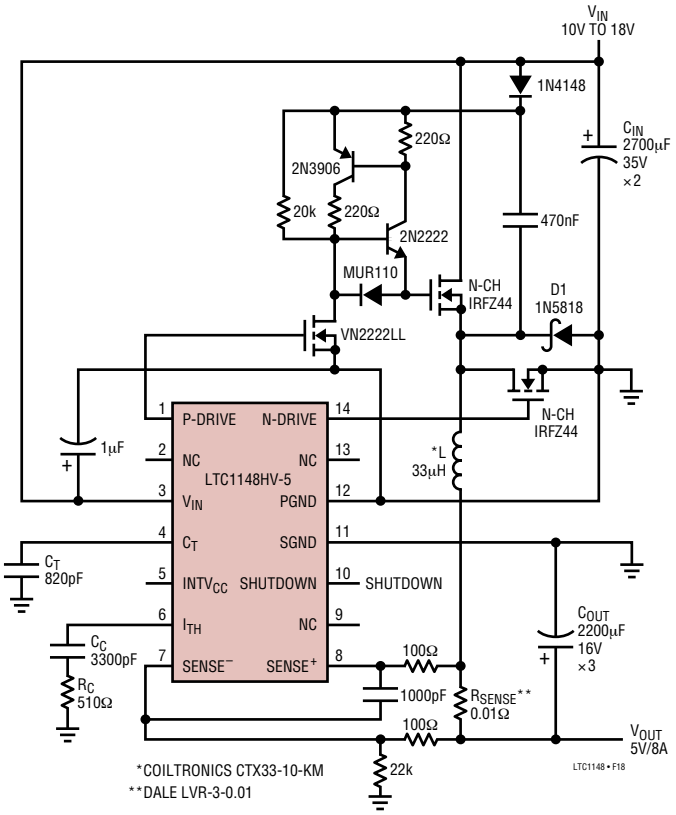


Figure 18. All N-Channel 5V/8A High Efficiency Regulator (Burst Mode Operation Suppressed)

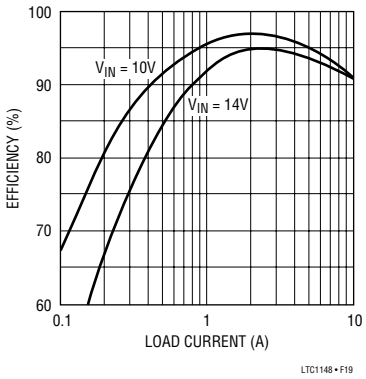


Figure 19. All N-Channel 5V/8A Efficiency

For additional high efficiency application circuits, see Application Notes 54, 58 and 66

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulator	Dual LTC1148
LTC1143	Dual High Efficiency Step-Down Switching Regulator Controller	Nonsynchronous Dual Output
LTC1147	High Efficiency Step-Down Switching Regulator Controller	Nonsynchronous Equivalent to LTC1148, 8-Pin
LTC1149	High Efficiency Synchronous Step-Down Switching Regulator	V_{IN} < 48V, Standard Threshold MOSFETs
LTC1159	High Efficiency Synchronous Step-Down Switching Regulator	V_{IN} < 40V, Logic Level MOSFETs
LTC1174	High Efficiency Step-Down and Inverting DC/DC Converter	Nonsynchronous 8-Pin Internal Switch
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Nonsynchronous Internal Switch
LTC1435A	High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Synchronous N-Channel, Constant Frequency
LTC1538-AUX	Dual High Efficiency, Low Noise, Synchronous Step-Down Switching Regulator	Auxiliary Linear Regulator, 5V Standby in Shutdown

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