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HMC595A

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HMC595A / 595AE

v01.0515

GaAs MMIC 3 WATT T/R SWITCH DC - 3 GHz

Typical Applications

The HMC595A / 595AE is ideal for:

- Cellular/3G Infrastructure
- Private Mobile Radio Handsets
- WLAN, WiMAX & WiBro
- Automotive Telematics
- Test Equipment

Features

Low Insertion Loss: 0.3 dB

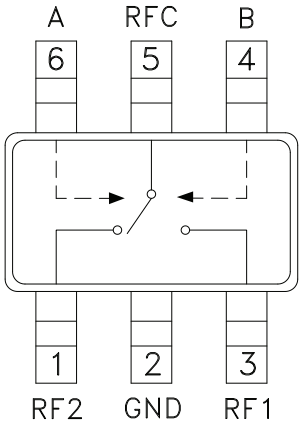
High Input IP3: +63 dBm

Isolation: 30 dB

Positive Control: 0/+3V to 0/+10V

Ultra Small Package: SOT26

Functional Diagram



General Description

The HMC595A & HMC595AE are low-cost SPDT switches in 6-lead SOT26 packages for use in transmit/receive applications which require very low distortion at high incident power levels. The device can control signals from DC to 3 GHz and is especially suited for Cellular/3G infrastructure, WiMAX and WiBro applications with only 0.3 dB typical insertion loss. The design provides a 3 watt power handling and +63 dBm third order intercept at +8 Volt bias. RF1 and RF2 are reflective shorts when "Off". Control inputs A & B are compatible with CMOS and some TTL logic families. These products are form, fit and function replacements for HMC595 & HMC595E while offering superior electrical performance.

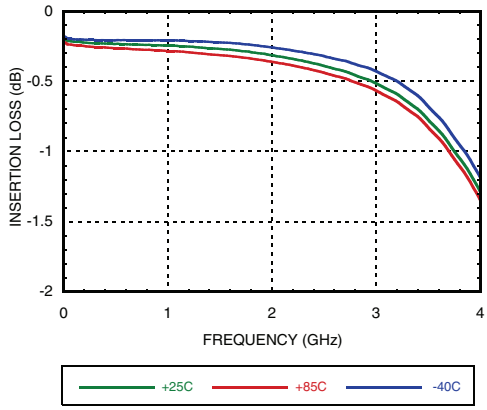
Electrical Specifications, T_A = +25° C, Vctl = 0/+5 Vdc (Unless Otherwise Stated), 50 Ohm System

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.25 0.3 0.4 0.5	0.5 0.6 0.7 0.8	dB dB dB dB
Isolation		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	26 22 18 14	30 26 24 18		dB dB dB dB
Return Loss		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		30 25 22 20		dB dB dB dB
Input Power for 1dB Compression	Vctl = 0/+3V Vctl = 0/+5V Vctl = 0/+8V	0.5 - 3.0 GHz	29 35 37	31 37 39		dBm dBm dBm
Input Third Order Intercept (Two-tone Input Power = +23 dBm Each Tone)	Vctl = 0/+3V Vctl = 0/+5V Vctl = 0/+8V	0.5 - 3.0 GHz		50 64 63		dBm dBm dBm
Switching Characteristics		DC - 3.0 GHz				
tRISE, tFALL (10/90% RF)				50		ns
tON, tOFF (50% CTL to 10/90% RF)				100		ns

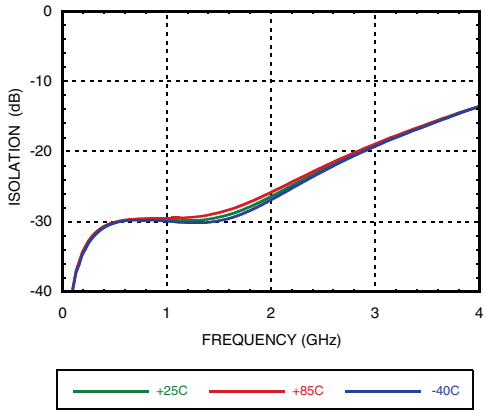
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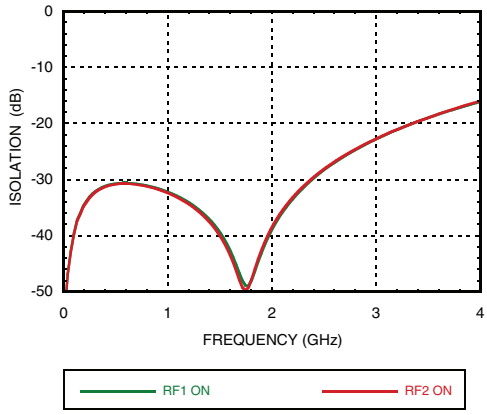
Insertion Loss



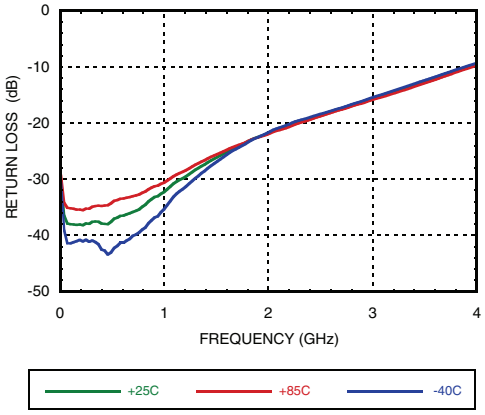
Isolation Between RFC and RF1/RF2



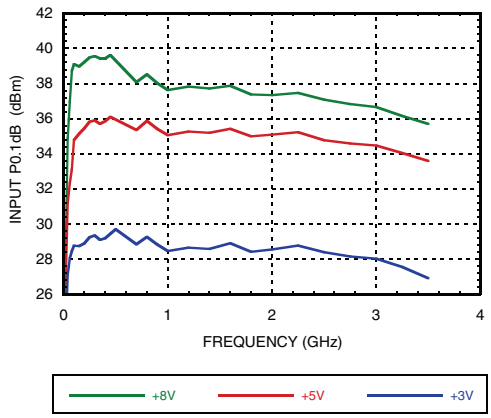
RF1 to RF2 Isolations



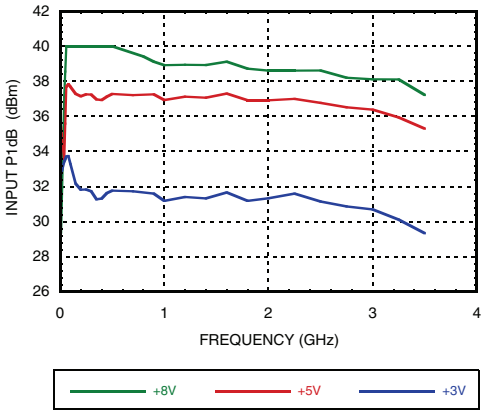
Return Loss



Input P0.1dB vs. Vctl



Input P1dB vs. Vctl

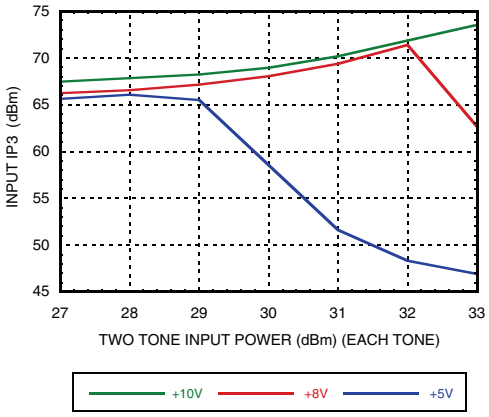


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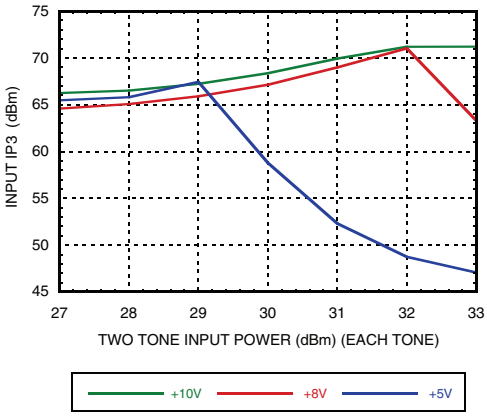
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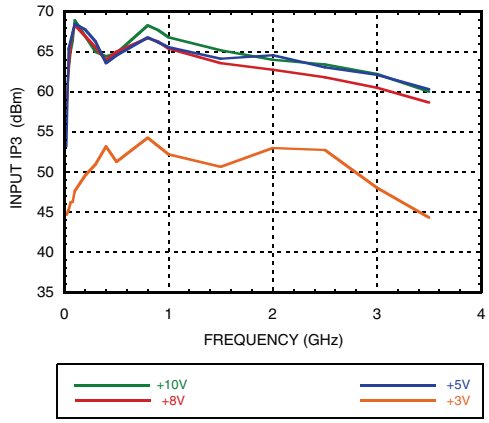
Input IP3 vs. Input Power @ 900 MHz



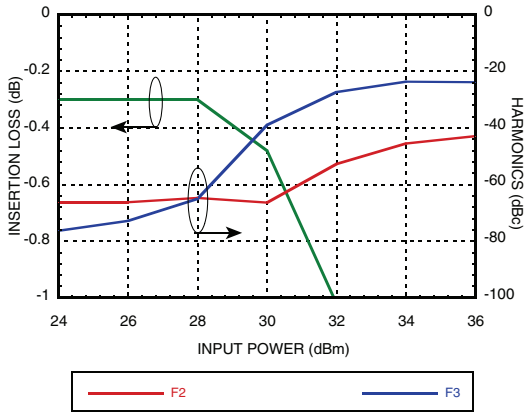
Input IP3 vs. Input Power @ 1900 MHz



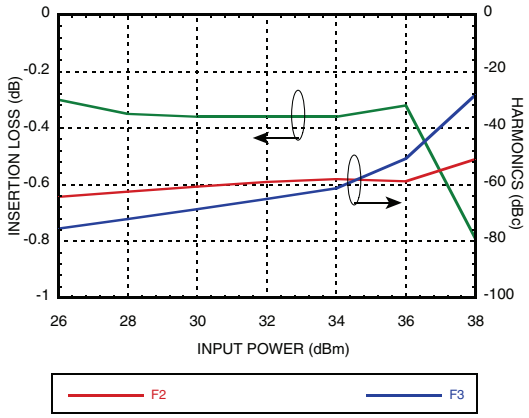
Input Third Order Intercept Point



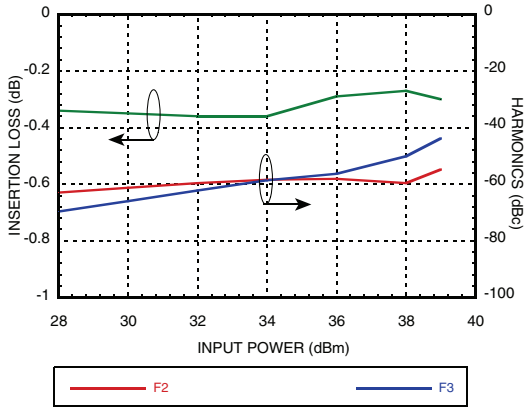
2nd & 3rd Harmonics @ 900 MHz Vctl = +3 Volts



2nd & 3rd Harmonics @ 900 MHz Vctl = +5 Volts



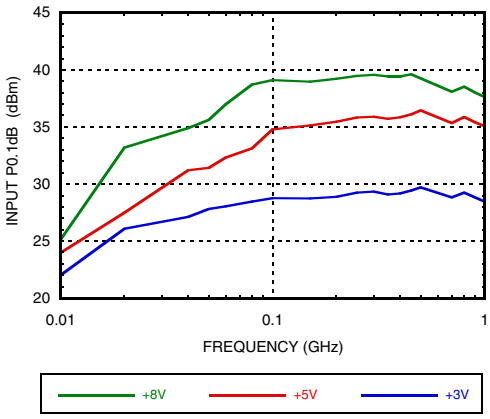
2nd & 3rd Harmonics @ 900 MHz Vctl = +8 Volts



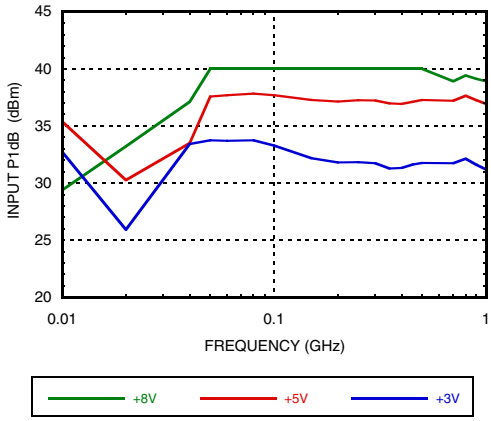
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Input P0.1dB vs. Vctl



Input P1dB vs. Vctl



Absolute Maximum Ratings

Max. Input Power V_{ctl} = 0/+8V	0.5 - 2.5 GHz	39 dBm
Control Voltage Range (A & B)		-0.2 to +12 Vdc
Channel Temperature		150 °C
Continuous Pdiss (T= + 85 °C) (derate 9.2 mW/°C above 85 °C)		0.597W
Thermal Resistance		109 °C/W
Storage Temperature		-65 to +150 °C
Operating Temperature		-40 to +85 °C
ESD Sensitivity (HBM)		Class 1A

DC Blocks are required at ports RFC, RF1 and RF2

Control Voltages

State	Bias Condition
Low	0 to +0.2 Vdc @ 10 µA Typical
High	+3 Vdc @ 2µA Typical to +8 Vdc @ 100 µA Typical (± 0.2 Vdc)

Truth Table

Control Input (Vctl)		Signal Path State	
A	B	RFC to RF1	RFC to RF2
High	Low	Off	On
Low	High	On	Off

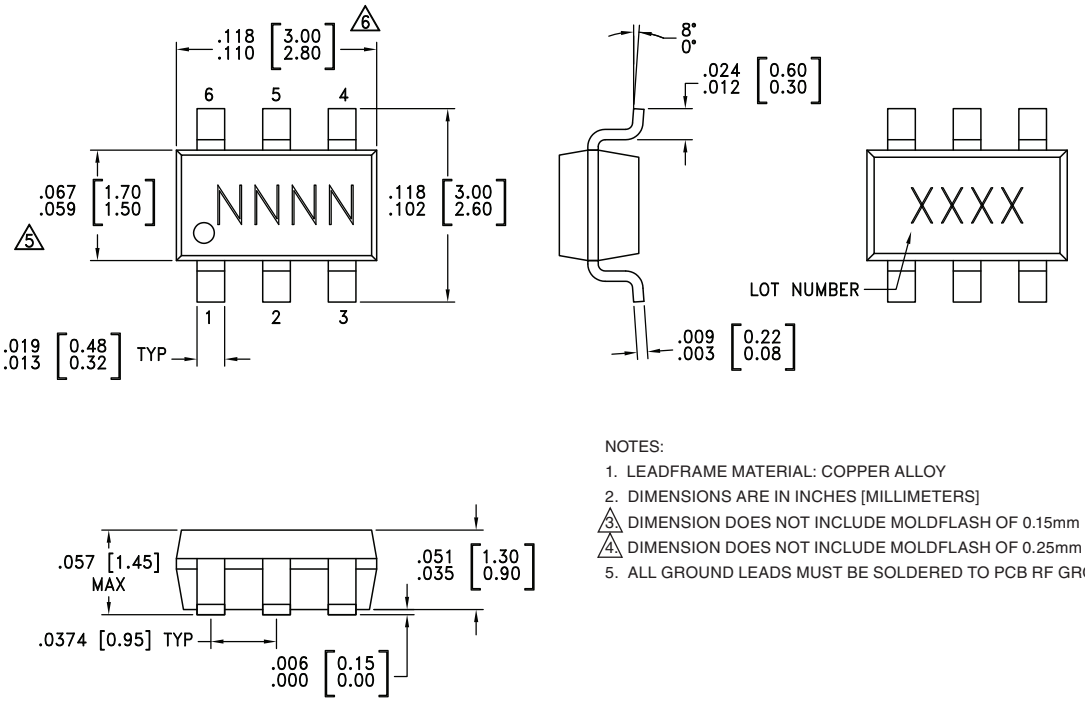
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OBSERVE HANDLING PRECAUTIONS

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Outline Drawing



NOTES:

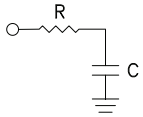
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC595A	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H595A XXXX
HMC595AE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	595AE XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5	RF2, RF1, RFC	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required.	
2	GND	This pin must be connected to RF/DC ground.	
4	B	See truth table and control voltage table.	
6	A	See truth table and control voltage table.	

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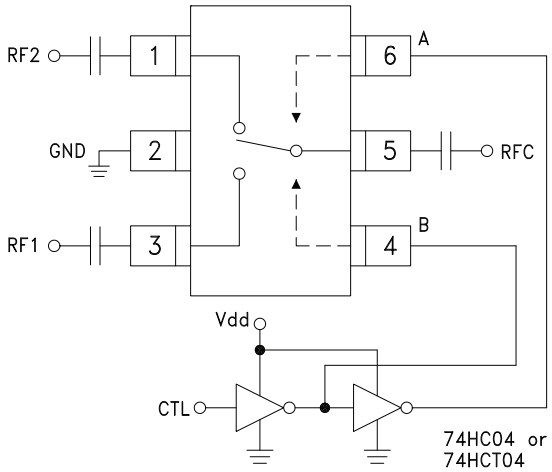
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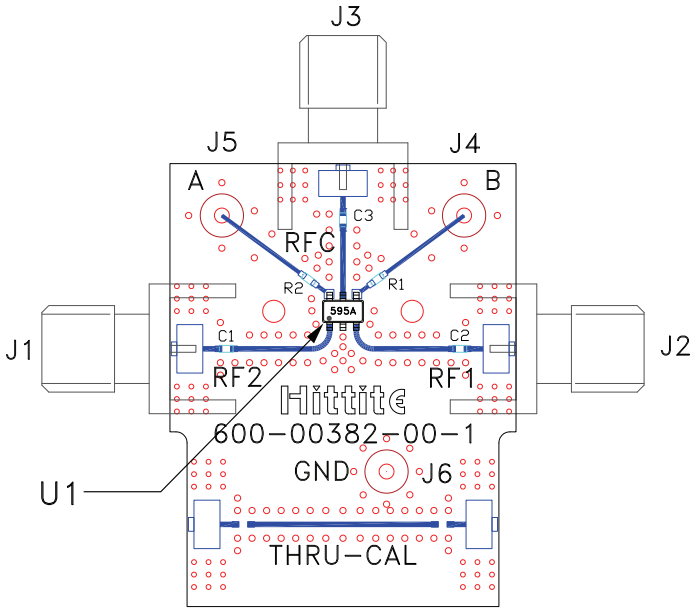
Typical Application Circuit

Notes:

1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3 to +8 Volts applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with V set to +10V. The switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.



Evaluation Circuit Board



List of Materials for Evaluation PCB EV1HMC595A [1]

Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4 - J6	DC Pin
C1 - C3	330 pF capacitor, 0402 Pkg.
R1, R2	1 kOhm Resistor, 0402 Pkg.
U1	HMC595A / 595AE T/R Switch
PCB [2]	101659 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ohm impedance and the package ground leads and package bottom should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Analog Devices upon request.

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