



**THE DATASHEET OF  
TIBPAL16R6-7CFN**

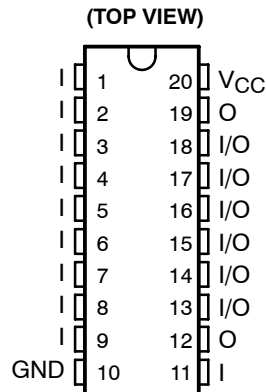


**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C  
TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M  
HIGH-PERFORMANCE IMPACT-X™ PAL® CIRCUITS**

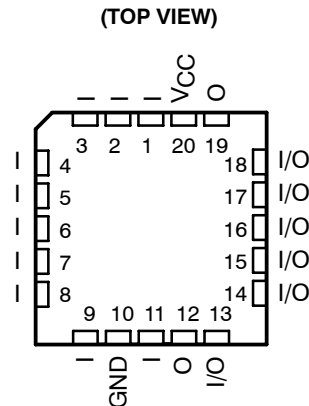
SRPS006E - D3115, MAY 1988 - REVISED DECEMBER 2010

- **High-Performance Operation:**
  - $f_{max}$  (no feedback)
    - TIBPAL16R'-7C Series . . . 100 MHz Min
    - TIBPAL16R'-10M Series . . . 62.5 MHz Min
  - $f_{max}$  (internal feedback)
    - TIBPAL16R'-7C Series . . . 100 MHz Min
    - TIBPAL16R'-10M Series . . . 62.5 MHz Min
  - $f_{max}$  (external feedback)
    - TIBPAL16R'-7C Series . . . 74 MHz Min
    - TIBPAL16R'-10M Series . . . 52.5 MHz Min
  - Propagation Delay
    - TIBPAL16L'-7C Series . . . 7 ns Max
    - TIBPAL16L'-10M Series . . . 10 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

TIBPAL16L8'  
C SUFFIX . . . J OR N PACKAGE  
M SUFFIX . . . J PACKAGE



TIBPAL16L8'  
C SUFFIX . . . FN PACKAGE  
M SUFFIX . . . FK PACKAGE



Pin assignments in operating mode

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

**description**

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

IMPACT-X is a trademark of Texas Instruments Incorporated.  
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



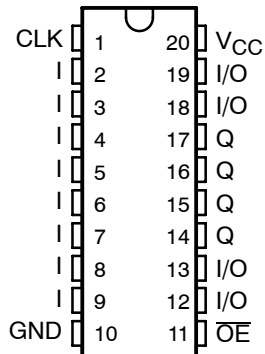
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# TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

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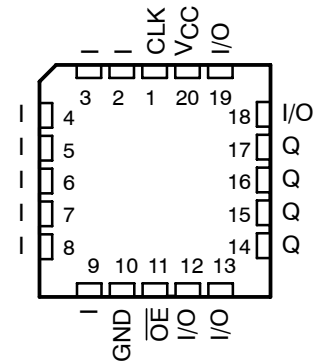
**TIBPAL16R4'**  
C SUFFIX . . . J OR N PACKAGE  
M SUFFIX . . . J PACKAGE

(TOP VIEW)



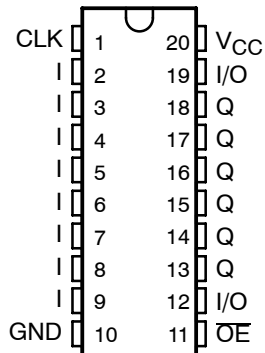
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M SUFFIX . . . FK PACKAGE

(TOP VIEW)



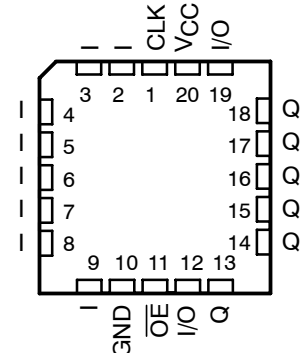
**TIBPAL16R6'**  
C SUFFIX . . . J OR N PACKAGE  
M SUFFIX . . . J PACKAGE

(TOP VIEW)



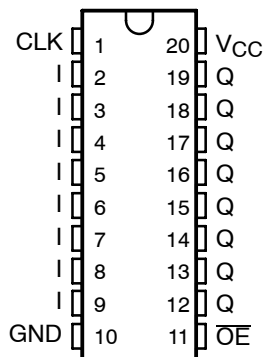
**TIBPAL16R6'**  
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M SUFFIX . . . FK PACKAGE

(TOP VIEW)



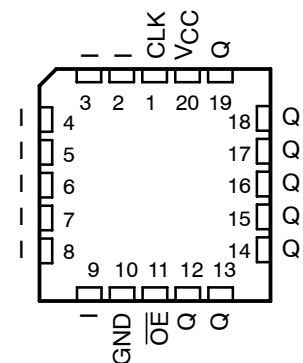
**TIBPAL16R8'**  
C SUFFIX . . . J OR N PACKAGE  
M SUFFIX . . . J PACKAGE

(TOP VIEW)



**TIBPAL16R8'**  
C SUFFIX . . . FN PACKAGE  
M SUFFIX . . . FK PACKAGE

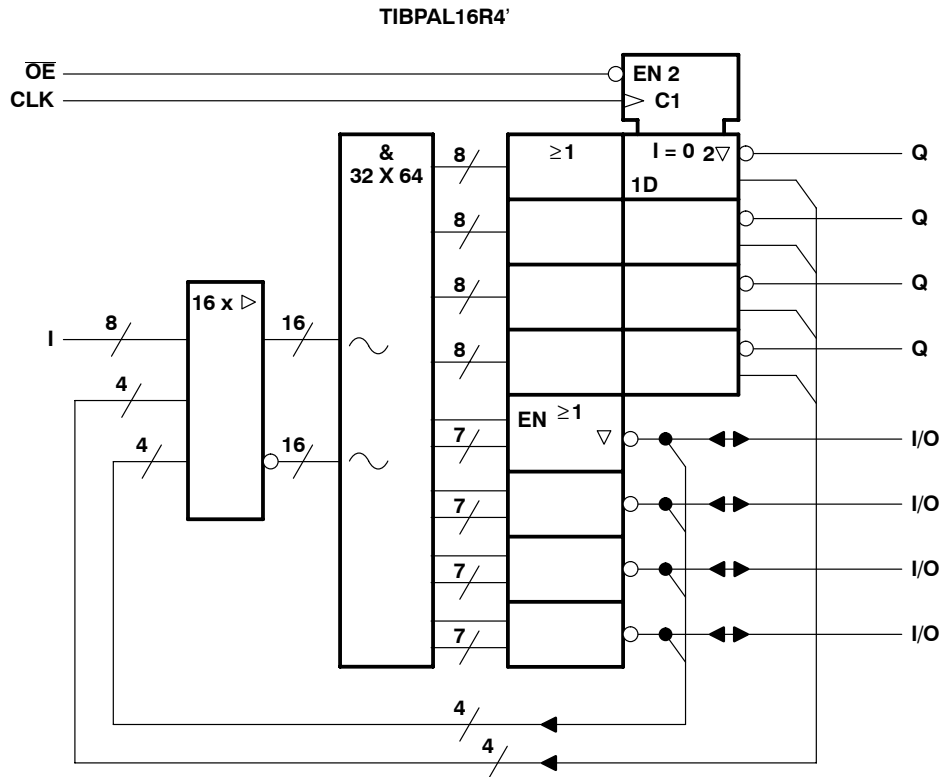
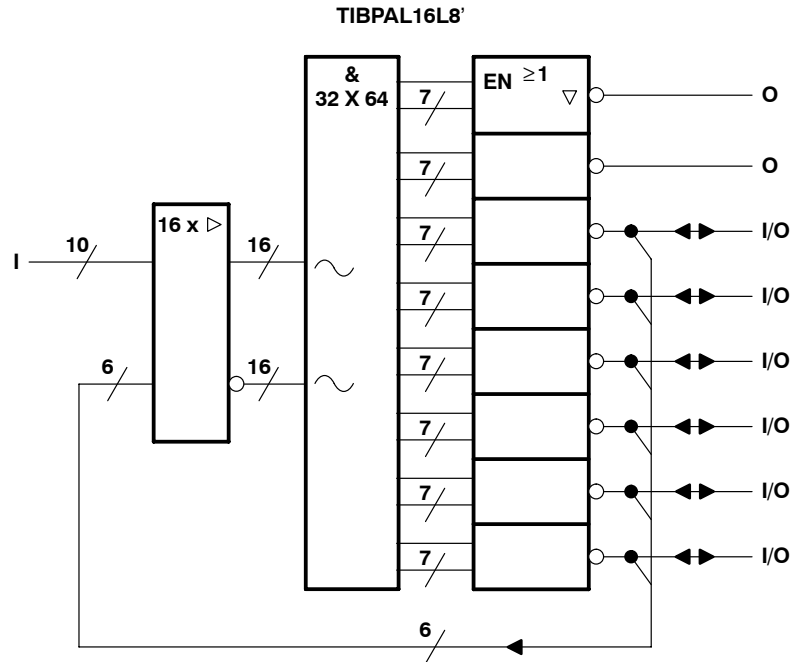
(TOP VIEW)



Pin assignments in operating mode

TIBPAL16L8-7C, TIBPAL16R4-7C  
 TIBPAL16L8-10M, TIBPAL16R4-10M  
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functional block diagrams (positive logic)



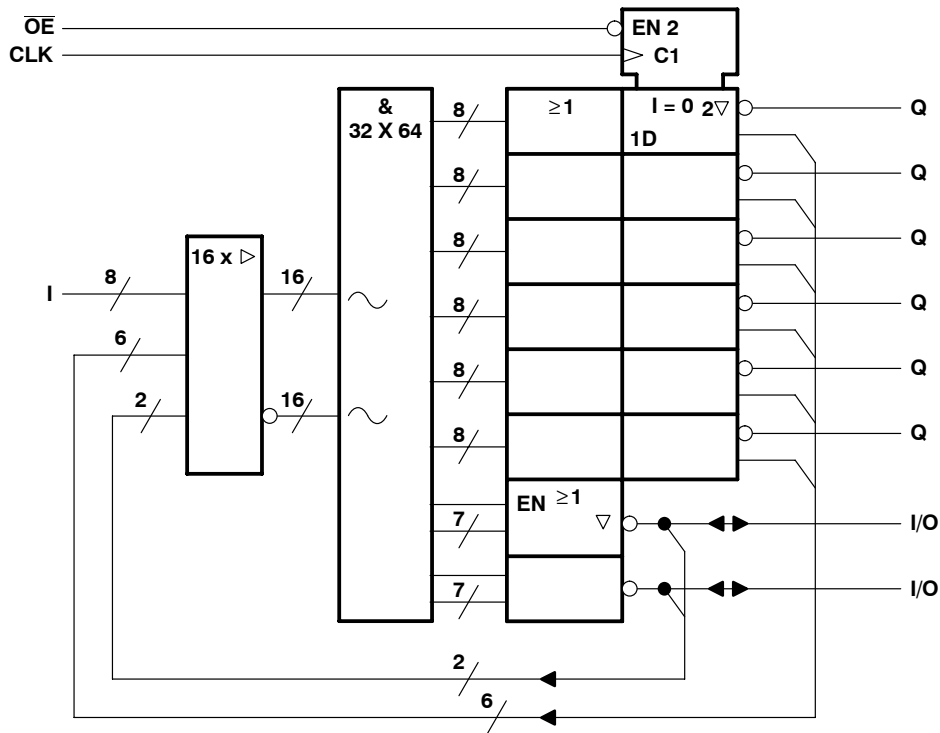
~ denotes fused inputs

**TIBPAL16R6-7C, TIBPAL16R8-7C**  
**TIBPAL16R6-10M, TIBPAL16R8-10M**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**

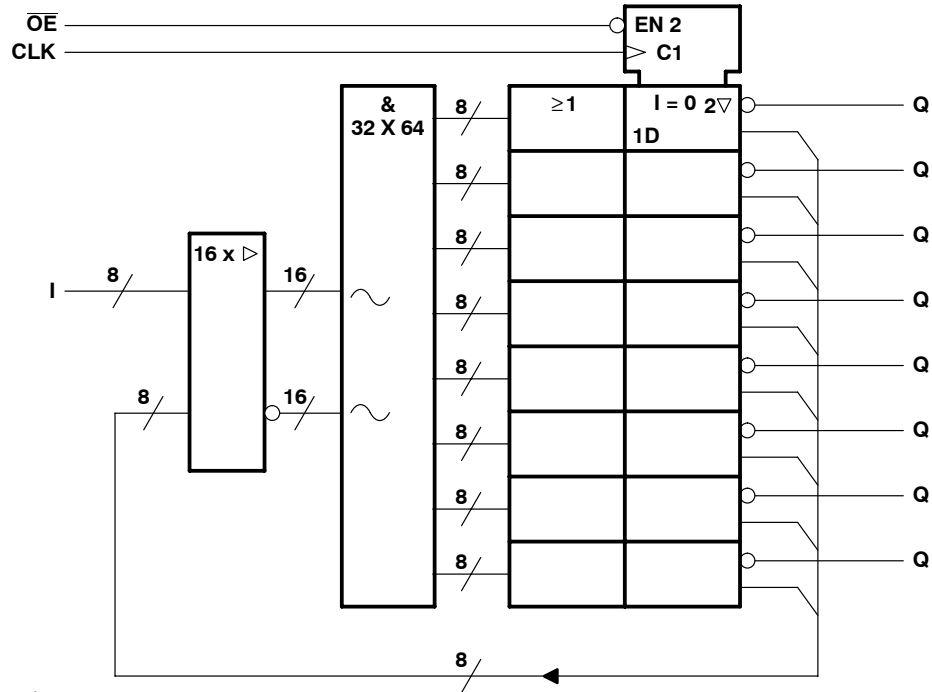
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functional block diagrams (positive logic)

TIBPAL16R6'

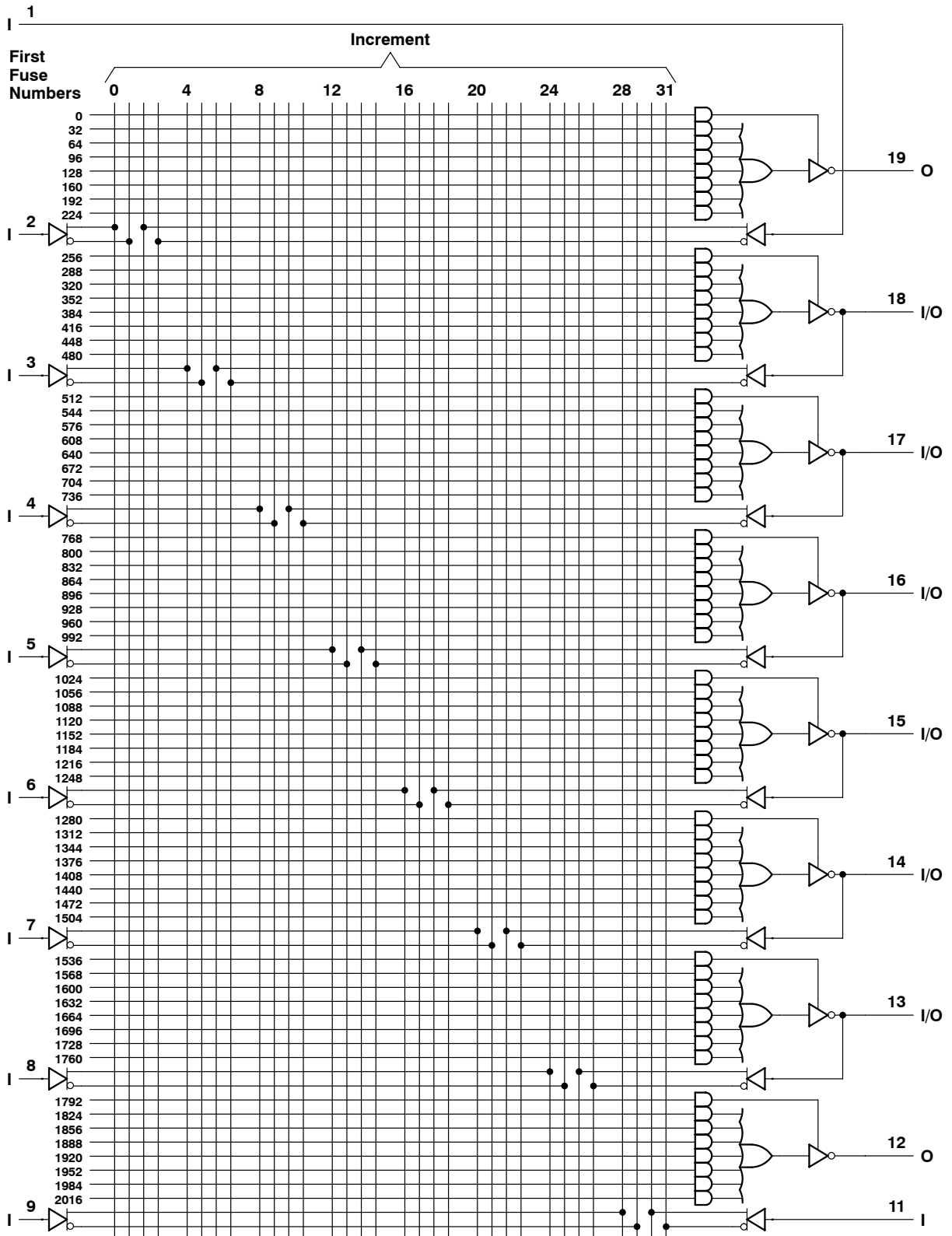


TIBPAL16R8'



~ denotes fused inputs

logic diagram (positive logic)



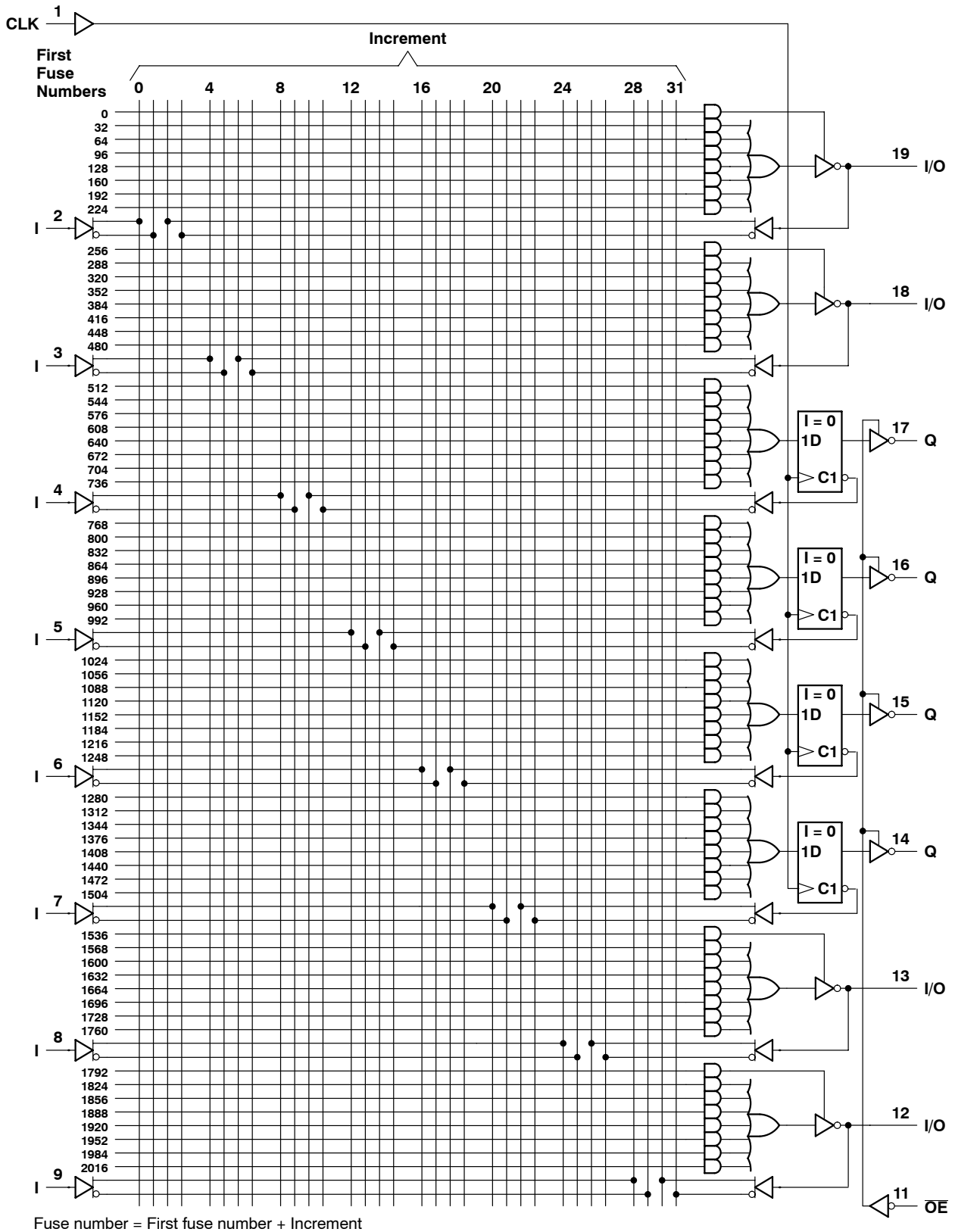
Fuse number = First fuse number + Increment

**TIBPAL16R4-7C**  
**TIBPAL16R4-10M**

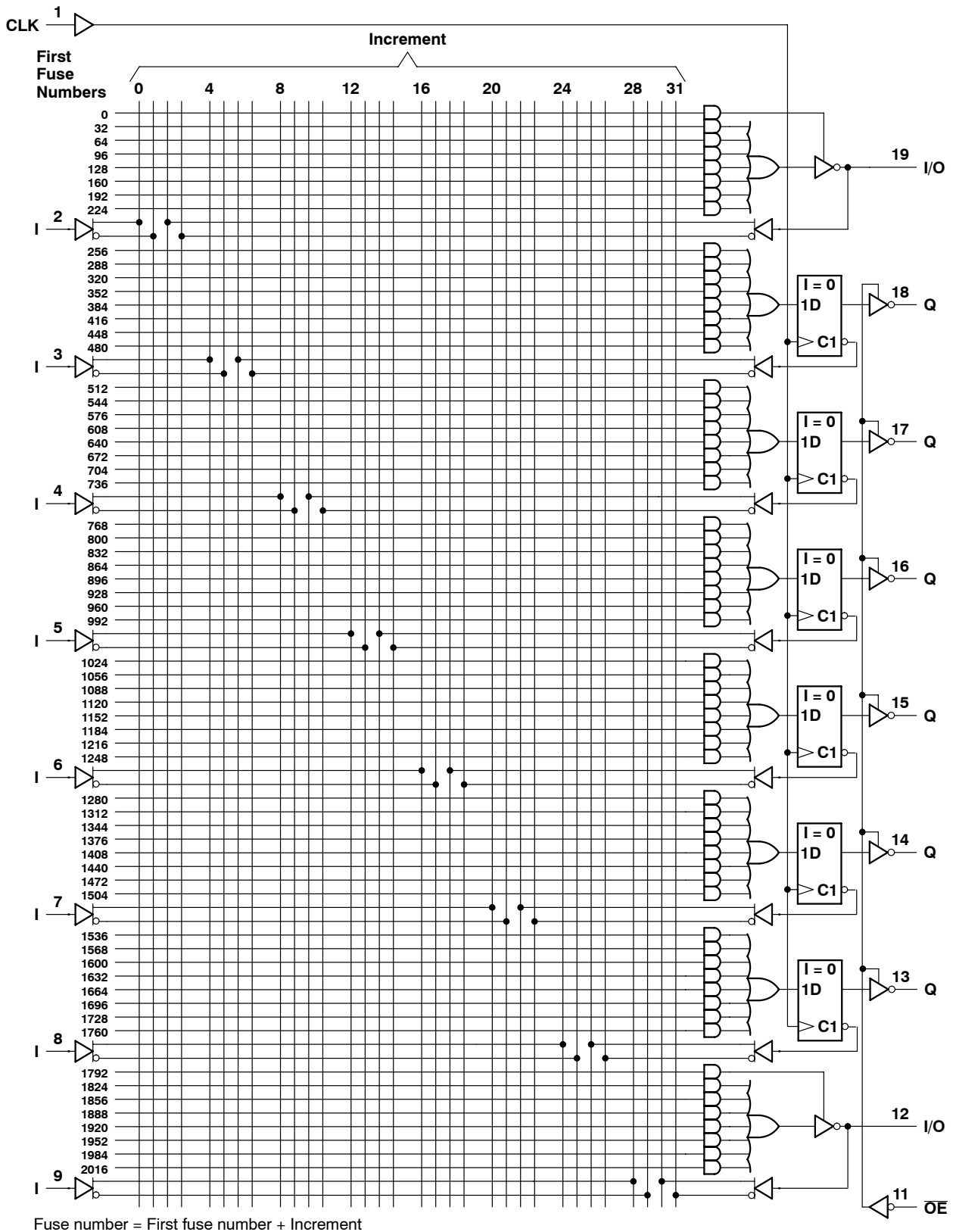
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**logic diagram (positive logic)**



logic diagram (positive logic)

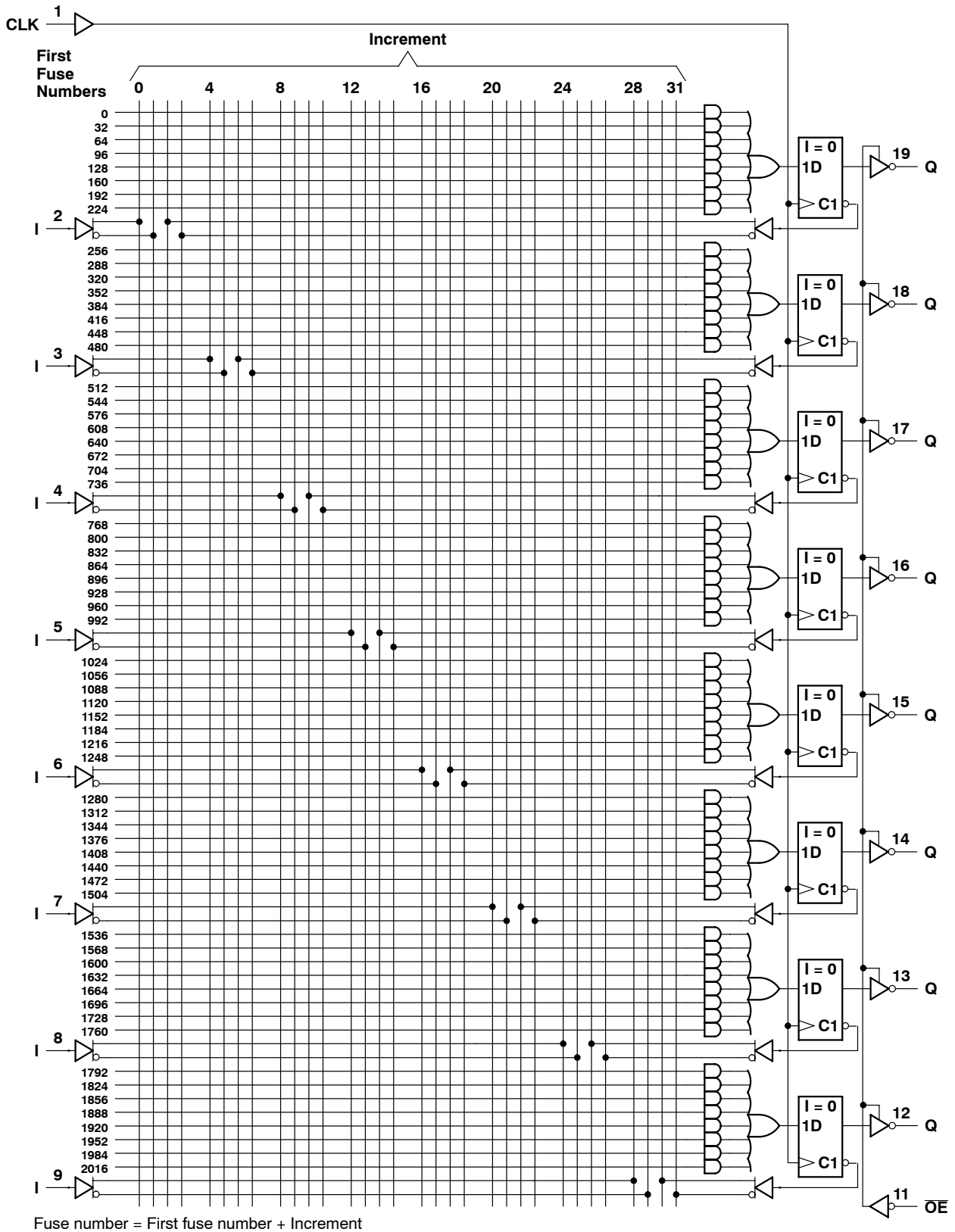


**TIBPAL16R8-7C**  
**TIBPAL16R8-10M**

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**logic diagram (positive logic)**



**OBSOLETE - No Longer Available**  
**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage (see Note 1) .....	5.5 V
Voltage applied to disabled output (see Note 1) .....	5.5 V
Operating free-air temperature range .....	0°C to 75°C
Storage temperature range .....	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage (see Note 2)	2		5.5	V
$V_{IL}$	Low-level input voltage (see Note 2)			0.8	V
$I_{OH}$	High-level output current			–3.2	mA
$I_{OL}$	Low-level output current			24	mA
$f_{clock}$	Clock frequency	0		100	MHz
$t_w$	Pulse duration, clock (see Note 2)	High		5	ns
		Low		5	
$t_{su}$	Setup time, input or feedback before clock↑		7		ns
$t_h$	Hold time, input or feedback after clock↑		0		ns
$T_A$	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

**electrical characteristics over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_I = -18\text{ mA}$		–0.8	–1.5	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3.2\text{ mA}$	2.4	3.2		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 24\text{ mA}$		0.3	0.5	V
$I_{OZH}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.7\text{ V}$			100	μA
$I_{OZL}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.4\text{ V}$			–100	μA
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 5.5\text{ V}$			100	μA
$I_{IH}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 2.7\text{ V}$			25	μA
$I_{IL}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0.4\text{ V}$		–80	–250	μA
$I_{OS}^\S$	$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.5\text{ V}$	–30	–70	–130	mA
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0$ ,		160	180	mA
$C_i$	$f = 1\text{ MHz}$ ,	$V_I = 2\text{ V}$		5		pF
$C_o$	$f = 1\text{ MHz}$ ,	$V_O = 2\text{ V}$		6		pF
$C_{clk}$	$f = 1\text{ MHz}$ ,	$V_{CLK} = 2\text{ V}$		6		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ I/O leakage is the worst case of  $I_{OZL}$  and  $I_{IL}$  or  $I_{OZH}$  and  $I_{IH}$  respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.



**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C**  
**HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS**

SRPS006E – D3115, MAY 1988 – REVISED DECEMBER 2010

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT		
$f_{\max}^{\ddagger}$	without feedback		R1 = 200 $\Omega$ , R2 = 390 $\Omega$ , See Figure 6	100			MHz		
	with internal feedback (counter configuration)			100					
	with external feedback			74					
$t_{pd}$	I, I/O	O, I/O		1 or 2 outputs switching		3	5.5	7	ns
		8 outputs switching		3	6	7.5			
$t_{pd}$	CLK $\uparrow$	Q		2	4	6.5	ns		
$t_{pd}^{\S}$	CLK $\uparrow$	Feedback input		3			ns		
$t_{en}$	OE $\downarrow$	Q		4			7.5	ns	
$t_{dis}$	OE $\uparrow$	Q		4			7.5	ns	
$t_{en}$	I, I/O	O, I/O		6			9	ns	
$t_{dis}$	I, I/O	O, I/O		6			9	ns	
$t_{sk(o)}^{\parallel}$	Skew between registered outputs		0.5				ns		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .‡ See section for  $f_{\max}$  specifications.§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured  $f_{\max}$  with internal feedback in the counter configuration.¶ This parameter is the measurement of the difference between the fastest and slowest  $t_{pd}$  (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

# TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

SRPS006E – D3115, MAY 1988 – REVISED DECEMBER 2010

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2		5.5	V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-2	mA
$I_{OL}$	Low-level output current			12	mA
$f_{clock}^{\dagger}$	Clock frequency	0		62.5	MHz
$t_w$	Pulse duration, clock (see Note 2)	High		8	ns
		Low		8	
$t_{su}^{\dagger}$	Setup time, input or feedback before clock $\uparrow$	10			ns
$t_h^{\dagger}$	Hold time, input or feedback after clock $\uparrow$	0			ns
$T_A$	Operating free-air temperature	-55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP $^{\dagger}$	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5$ V,	$I_I = -18$ mA		-0.8	-1.5	V
$V_{OH}$		$V_{CC} = 4.5$ V,	$I_{OH} = -2$ mA	2.4	3.2		V
$V_{OL}$		$V_{CC} = 4.5$ V,	$I_{OL} = 12$ mA		0.3	0.5	V
$I_{OZH}^{\ddagger}$		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			100	$\mu$ A
$I_{OZL}^{\ddagger}$	0, Q outputs	$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			-0.1	mA
	I/O ports					-0.25	
$I_I$		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V			1	mA
$I_{IH}$	I/O ports	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			100	$\mu$ A
	All others					25	
$I_{IL}^{\ddagger}$		$V_{CC} = 5.5$ V,	$V_I = 0.4$ V		-0.08	-0.25	mA
$I_{OS}^{\S}$		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V	-30	-70	-130	mA
$I_{CC}$		$V_{CC} = 5.5$ V,	$V_I = GND$ , Outputs open		140	200	mA
$C_i$		$f = 1$ MHz,	$V_I = 2$ V		5		pF
$C_o$		$f = 1$ MHz,	$V_O = 2$ V		6		pF
$C_{clk/oe}$		$f = 1$ MHz,	$V_{CLK/OE} = 2$ V		6		pF

 $^{\dagger}$  All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^{\circ}$ C. $^{\ddagger}$  I/O leakage is the worst case of  $I_{OZL}$  and  $I_{IL}$  or  $I_{OZH}$  and  $I_{IH}$  respectively. $^{\S}$  Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

**TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M**  
**HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS**

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
$f_{\max}^{\ddagger}$	without feedback		R1 = 390 $\Omega$ , R2 = 750 $\Omega$ , See Figure 6	62.5			MHz
	with internal feedback (counter configuration)			62.5			
	with external feedback			52.5			
$t_{pd}$	I, I/O	O, I/O		2	6	10	ns
$t_{pd}$	CLK $\uparrow$	Q		1	4	9	ns
$t_{pd}^{\S}$	CLK $\uparrow$	Feedback input		5			ns
$t_{en}$	OE $\downarrow$	Q		1	4	10	ns
$t_{dis}$	OE $\uparrow$	Q		1	4	10	ns
$t_{en}$	I, I/O	O, I/O		2	6	12	ns
$t_{dis}$	I, I/O	O, I/O	1	6	10	ns	

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .‡ See section for  $f_{\max}$  specifications.  $f_{\max}$  with external feedback is not production tested but is calculated from the equation found in the  $f_{\max}$  section.§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured  $f_{\max}$  with internal feedback in the counter configuration.

**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C**  
**TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**

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## programming information

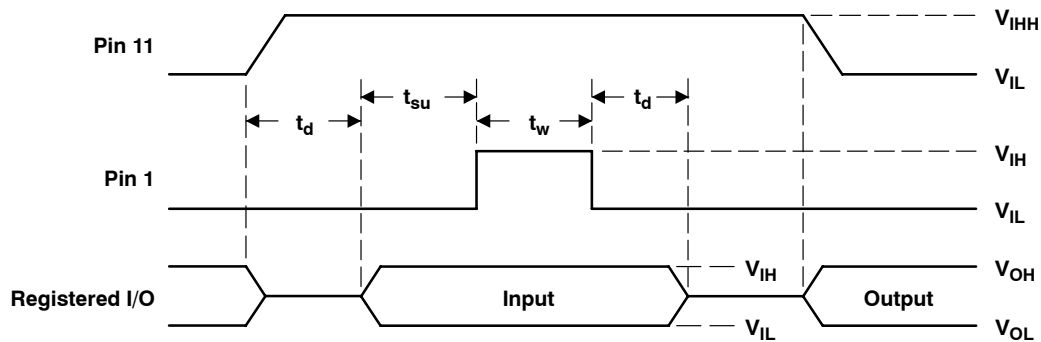
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

## preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With  $V_{CC}$  at 5 volts and Pin 1 at  $V_{IL}$ , raise Pin 11 to  $V_{IHH}$ .
- Step 2. Apply either  $V_{IL}$  or  $V_{IH}$  to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to  $V_{IL}$ . Preload can be verified by observing the voltage level at the output pin.



**Figure 1. Preload Waveforms**

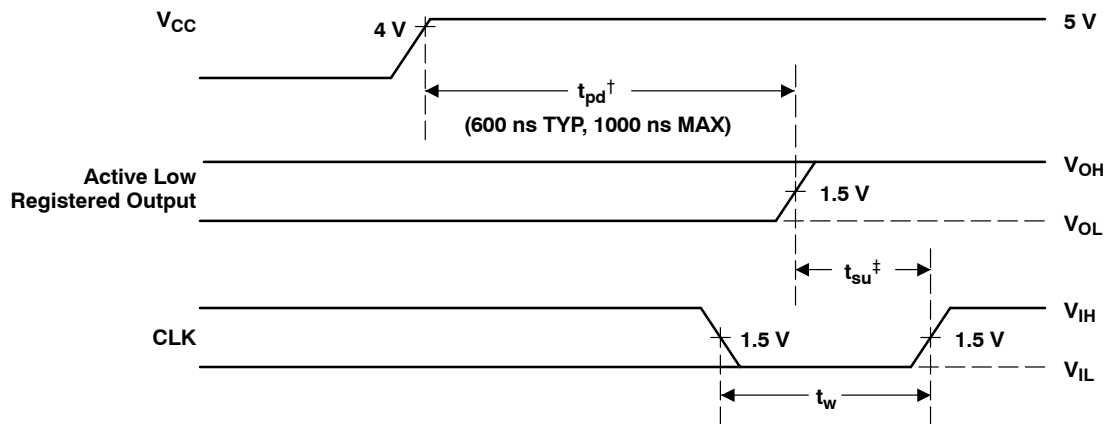
NOTE 3:  $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns}$   $V_{IHH} = 10.25 \text{ V to } 10.75 \text{ v}$

**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C**  
**TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**

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**power-up reset (see Figure 2)**

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of  $V_{CC}$  be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



<sup>†</sup> This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

<sup>‡</sup> This is the setup time for input or feedback.

**Figure 2. Power-Up Reset Waveforms**

## $f_{\max}$ SPECIFICATIONS

### $f_{\max}$ without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ( $t_{su} + t_h$ ). However, the minimum  $f_{\max}$  is determined by the minimum clock period ( $t_w$  high +  $t_w$  low).

$$\text{Thus, } f_{\max} \text{ without feedback} = \frac{1}{(t_{w\text{high}} + t_{w\text{low}})} \text{ or } \frac{1}{(t_{su} + t_h)}$$

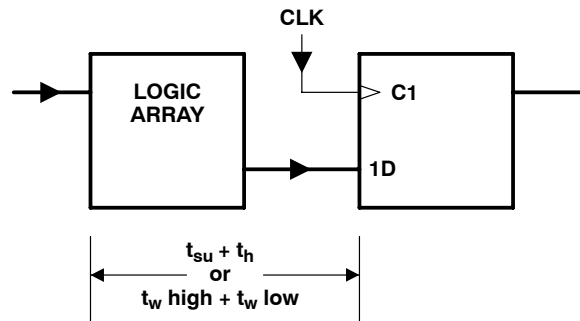


Figure 3.  $f_{\max}$  Without Feedback

### $f_{\max}$ with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, } f_{\max} \text{ with internal feedback} = \frac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}$$

Where  $t_{pd}$  CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

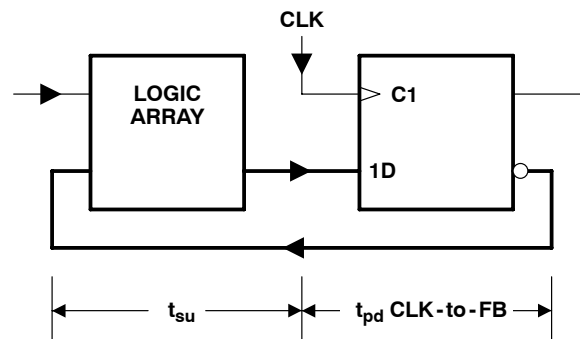


Figure 4.  $f_{\max}$  With Internal Feedback

TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C  
 TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M  
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## $f_{\max}$ SPECIFICATIONS

### $f_{\max}$ with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ( $t_{su} + t_{pd}$  CLK-to-Q).

$$\text{Thus, } f_{\max} \text{ with external feedback} = \frac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$$

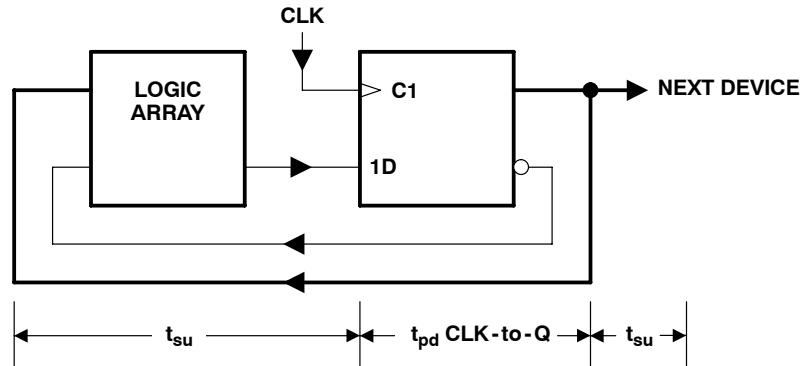
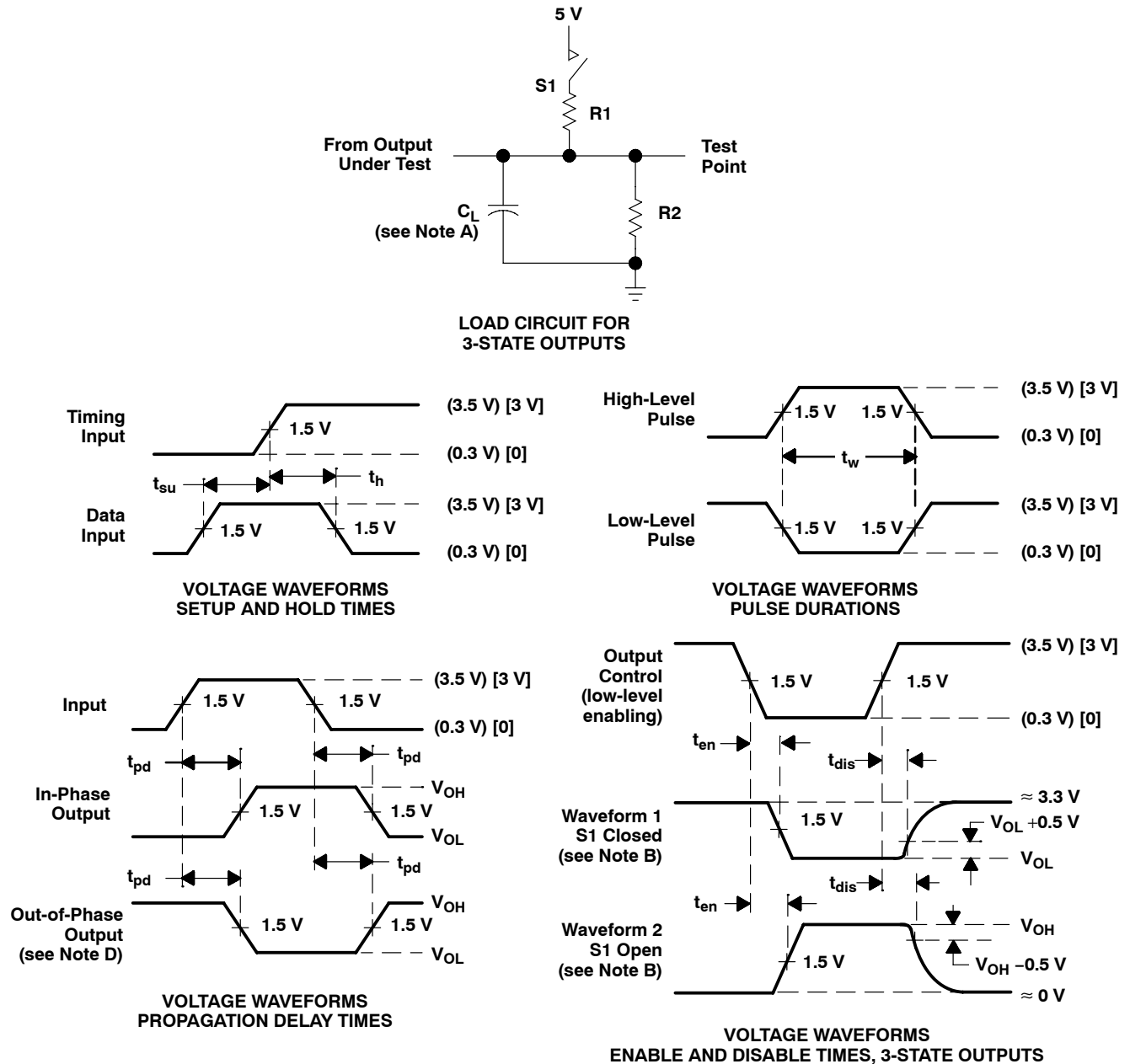


Figure 5.  $f_{\max}$  With External Feedback

TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C  
 TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M  
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## PARAMETER MEASUREMENT INFORMATION



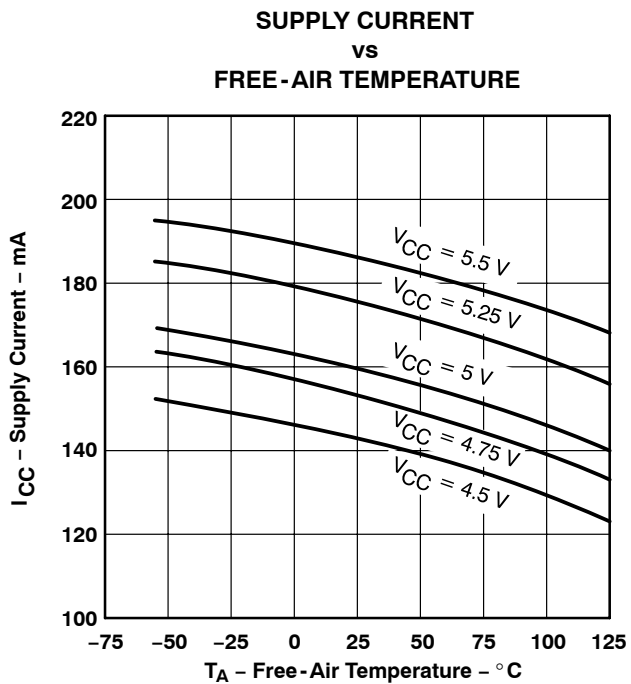
- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ), PRR  $\leq$  1 MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%; For M suffix, use the voltage levels indicated in brackets [ ], PRR  $\leq$  10 MHz,  $t_r$  and  $t_f \leq 2$  ns, duty cycle = 50%.  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
 E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

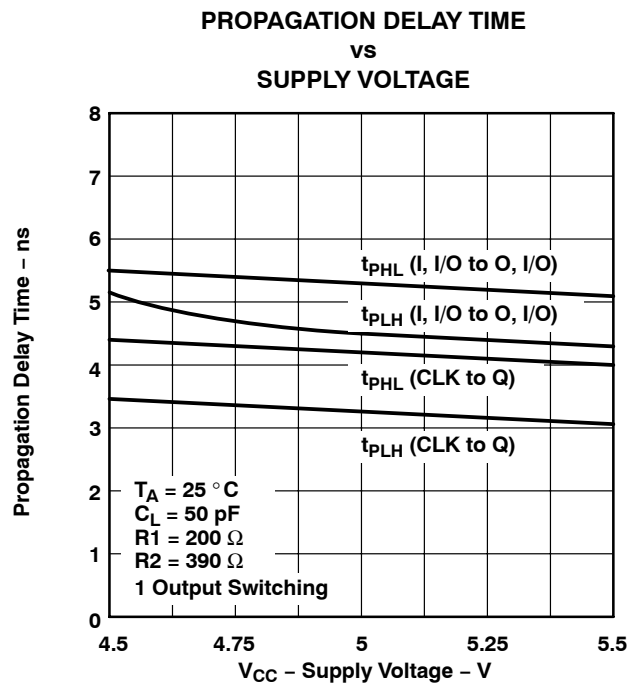
**TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C**  
**TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M**  
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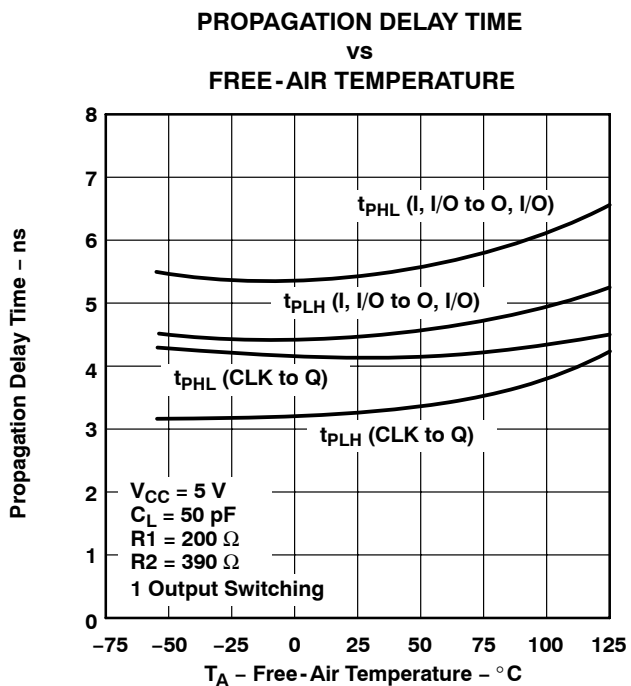
**TYPICAL CHARACTERISTICS**



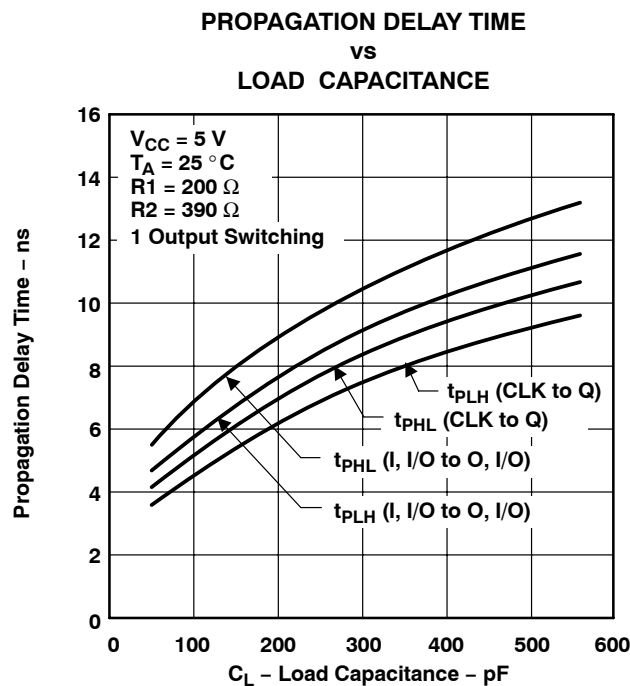
**Figure 7**



**Figure 8**



**Figure 9**



**Figure 10**

TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C  
 TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M  
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TYPICAL CHARACTERISTICS

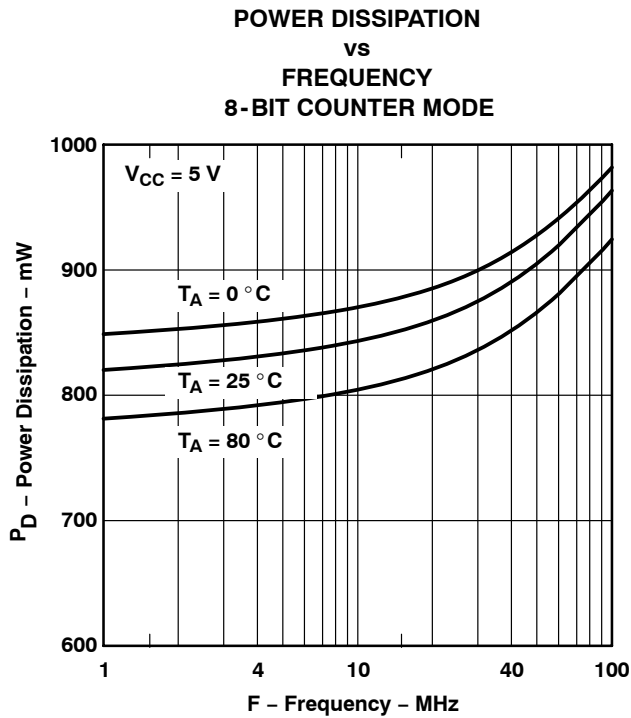


Figure 11

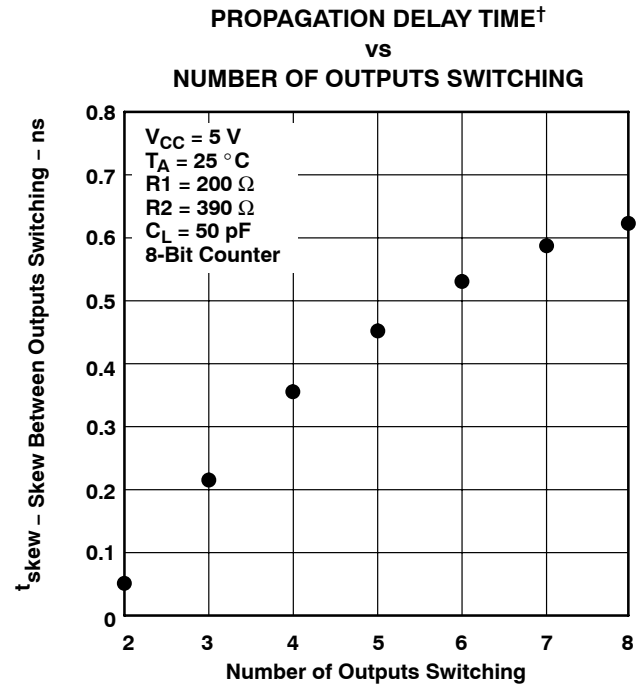


Figure 12

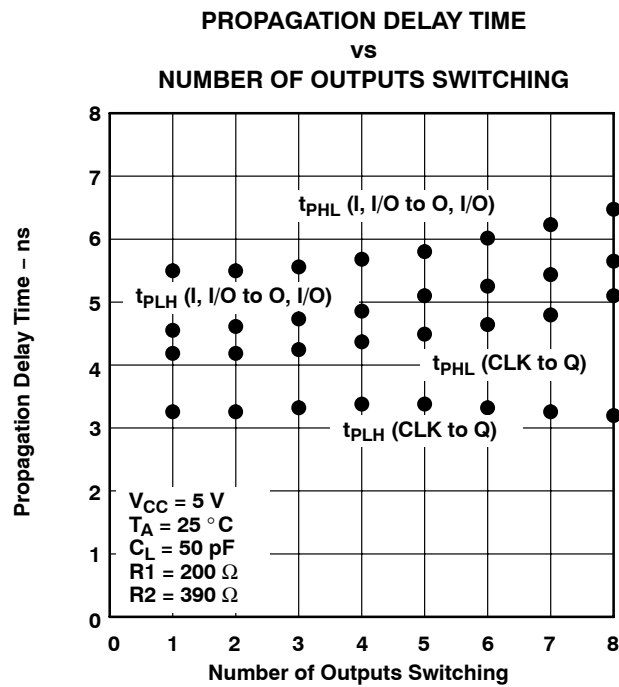


Figure 13

†Outputs switching in the same direction ( $t_{PLH}$  compared to  $t_{PLH}/t_{PHL}$  to  $t_{PHL}$ )

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D0892

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-85155172A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515517RA	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515517SA	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
5962-85155182A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155182A TIBPAL16 R8-10MFKB	
5962-8515518RA	NRND	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515518RA TIBPAL16R8-10M JB	
5962-8515518SA	NRND	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515518SA TIBPAL16R8-10M WB	
5962-85155192A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515519RA	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515519SA	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
5962-85155202A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515520RA	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
5962-8515520SA	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
TIBPAL16L8-10MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	5962-85155172A TIBPAL16 L8-10MFKB	
TIBPAL16L8-10MJB	OBSOLETE	CDIP	J	20		TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515517RA TIBPAL16L8-10M JB	
TIBPAL16L8-10MWB	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125	5962-8515517SA TIBPAL16L8-10M WB	
TIBPAL16L8-7CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	0 to 75	16L8-7	<a href="#">Samples</a>
TIBPAL16L8-7CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 75	TIBPAL16L8-7CN	<a href="#">Samples</a>
TIBPAL16R4-10MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TIBPAL16R4-10MJB	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
TIBPAL16R4-10MWB	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125		
TIBPAL16R4-7CFN	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	0 to 75		
TIBPAL16R4-7CN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 75		
TIBPAL16R6-10MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	5962-85155192A TIBPAL16 R6-10MFKB	
TIBPAL16R6-10MJB	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125	5962-8515519RA TIBPAL16R6-10M JB	
TIBPAL16R6-10MWB	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	-55 to 125	5962-8515519SA TIBPAL16R6-10M WB	
TIBPAL16R6-7CFN	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	0 to 75	16R6-7	
TIBPAL16R6-7CN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 75	TIBPAL16R6-7CN	
TIBPAL16R8-10MFKB	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-85155182A TIBPAL16 R8-10MFKB	
TIBPAL16R8-10MJB	NRND	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515518RA TIBPAL16R8-10M JB	
TIBPAL16R8-10MWB	NRND	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8515518SA TIBPAL16R8-10M WB	
TIBPAL16R8-7CFN	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	0 to 75		
TIBPAL16R8-7CN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 75		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

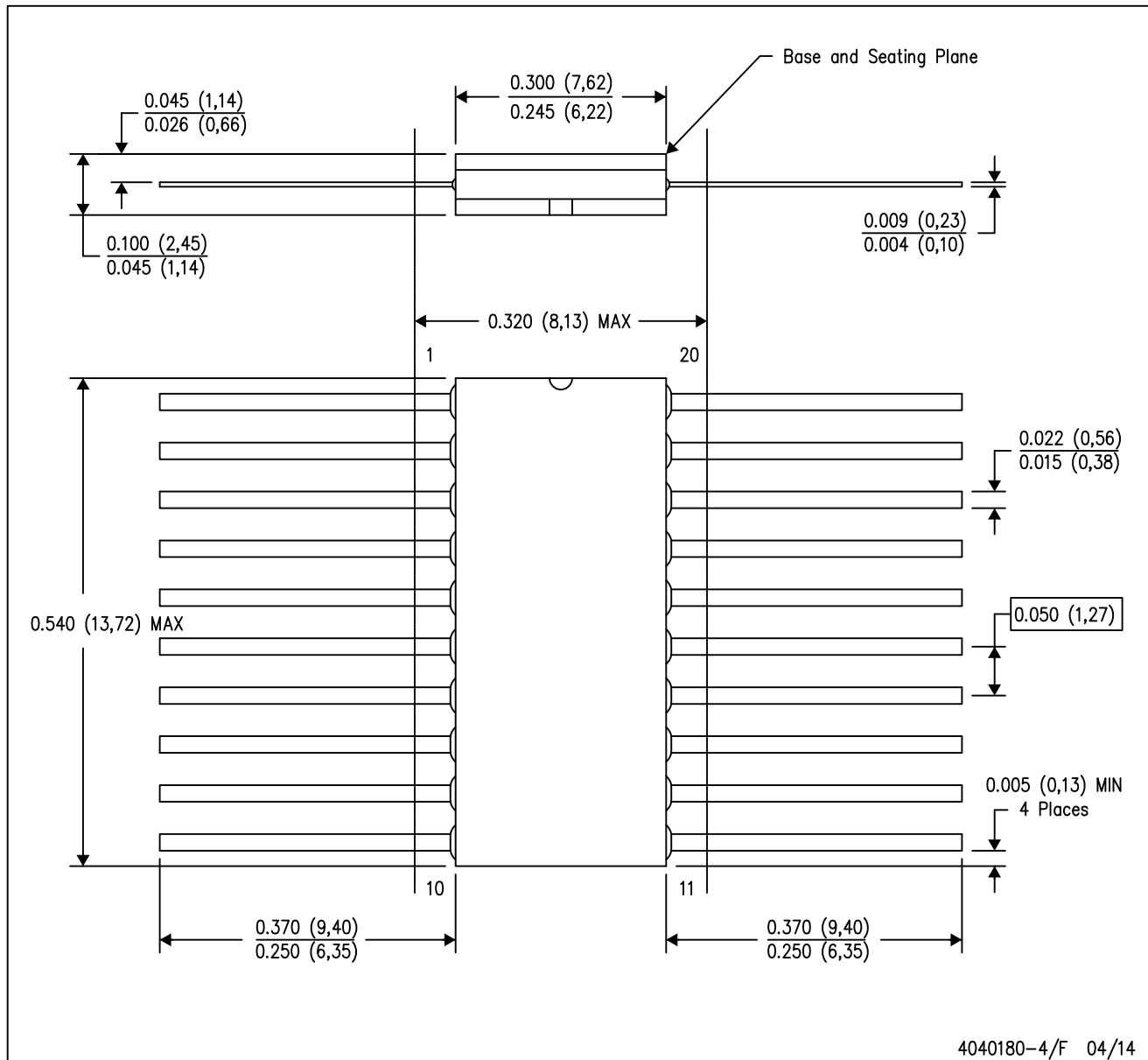


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

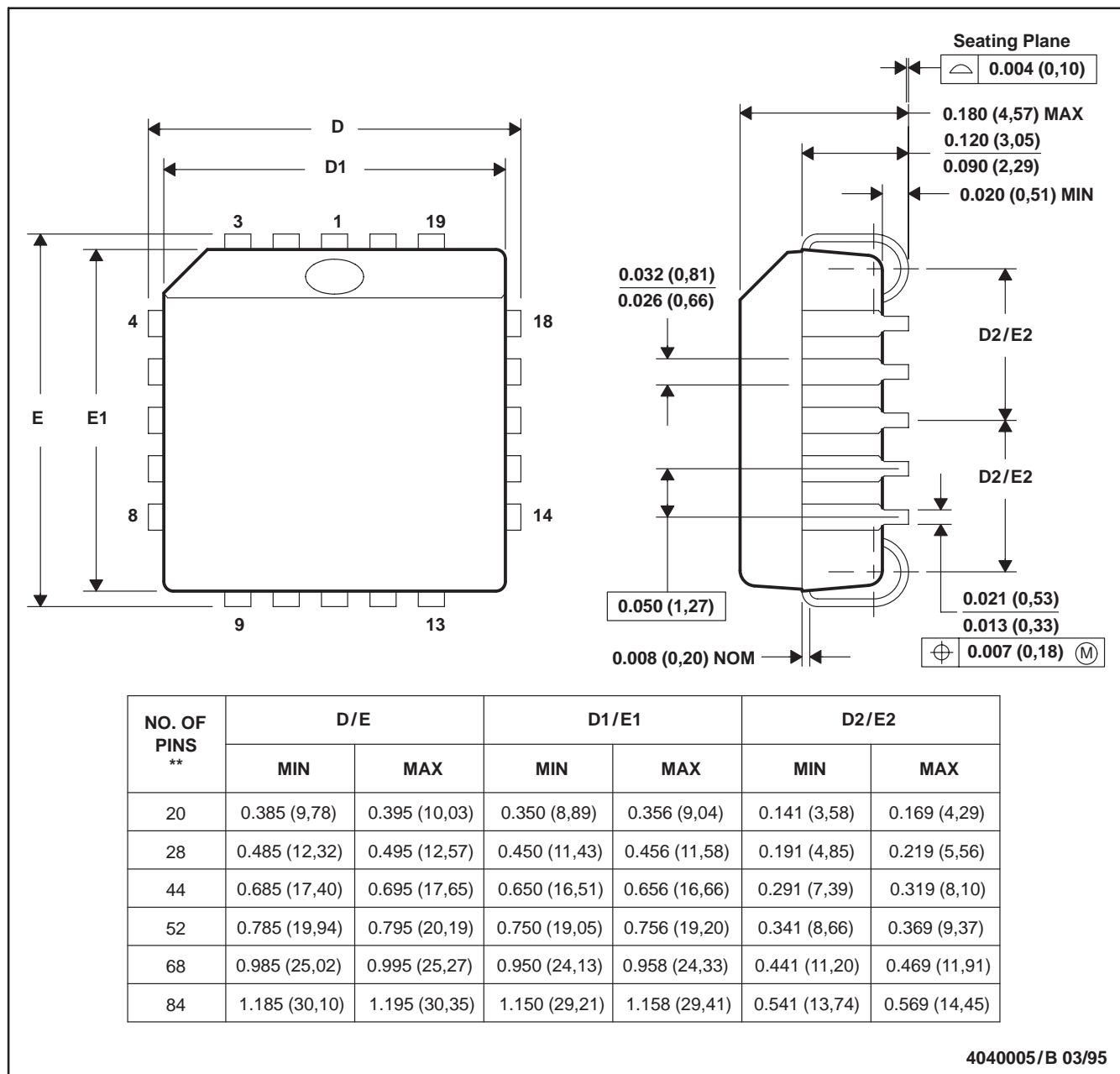


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

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