



**THE DATASHEET OF
ESD217B102ELE6327XTMA1**



Protection Device

TVS (Transient Voltage Suppressor)

ESD217-B1-02EL

Bi-directional, +14 / -8 V, 9 pF, 0402, RoHS and Halogen Free compliant

ESD217-B1-02EL

Data Sheet

Revision 1.1, 2014-11-11
Final

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1 Product Overview

1.1 Features

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 30 kV (air), ± 25 kV (contact)
 - IEC61000-4-4 (EFT): ± 3 kV / ± 60 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 3 A (8/20 μ s)
- Asymmetrical, bi-directional working voltage up to $V_{RWM} = +14$ V / -8 V
- Low capacitance: $C_L = 9$ pF (typical)
- Low clamping voltage: $V_{CL} = 26$ V (typical) at $I_{TLP} = 16$ A
- Very low reverse current: $I_R < 1$ nA (typical)
- Ultra low dynamic resistance: $R_{DYN} = 0.2$ Ω (typical)
- Pb-free (RoHS compliant) and halogen free package



1.2 Application Examples

- USB 2.0, 10/100 Ethernet, Firewire, DVI
- Mobile communication
- Consumer products (STD, MP3, DVD, DSC...)
- LCD display, camera
- Notebooks and desktop computers, peripherals

1.3 Product Description

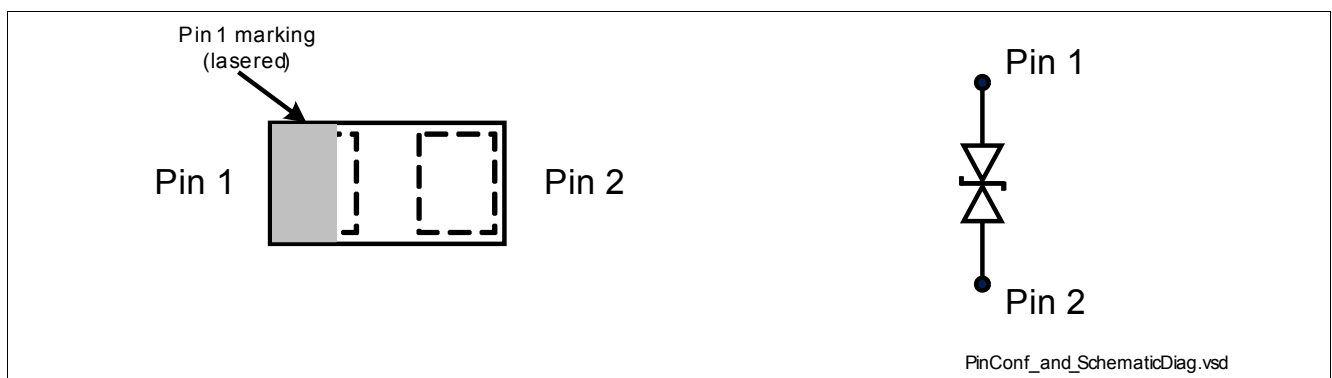


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD217-B1-02EL	TSLP-2-19	1 line, bi-directional	B

2 Characteristics

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values	Unit
ESD air discharge ¹⁾	V_{ESD}	± 30	kV
ESD contact discharge ¹⁾		± 25	
Peak pulse power ²⁾	P_{PK}	85	W
Peak pulse current ²⁾	I_{PP}	± 3	A
Operating temperature range	T_{OP}	-55 to 125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2

2) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

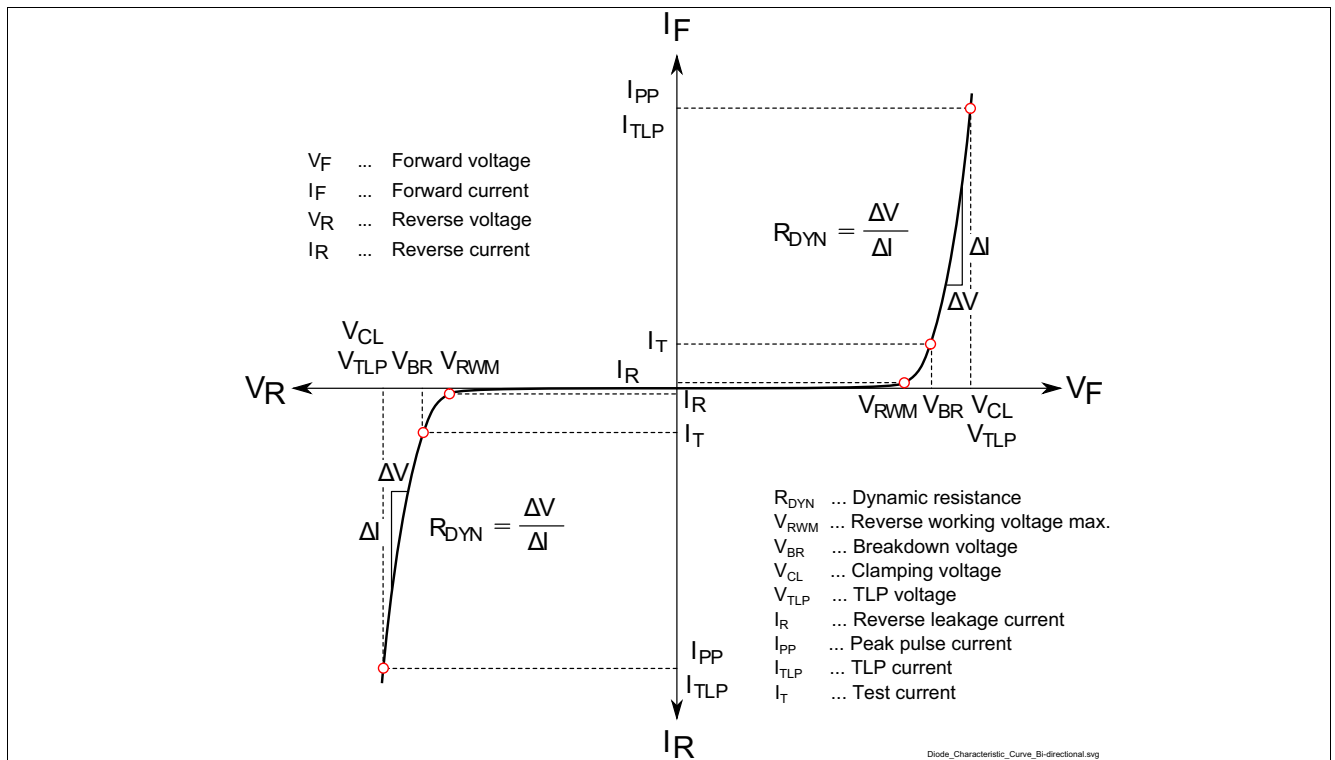


Figure 2-1 Definitions of electrical characteristics

Characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-8	–	14	V	Pin 2 to Pin1
Breakdown voltage	V_{BR}	14.5	17	20	V	$I_R = 1\text{ mA}$ Pin2 to Pin1 Pin1 to Pin2
		8.5	11.5	14		
Reverse current	I_R	–	<1	50	nA	$V_R = 3.3\text{ V}$

Table 2-3 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	9	13	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
Series inductance	L_S	–	0.4	–	nH	

Table 2-4 ESD and Surge Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾	V_{CL}	–	26	–	V	$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$
		–	29	–		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$
Clamping voltage ²⁾		–	25.5	–		$I_{PP} = 3\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin2 to Pin1
		–	24	–		$I_{PP} = 3\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin1 to Pin2
Dynamic resistance ¹⁾	R_{DYN}	–	0.2	–	Ω	$t_p = 100\text{ ns}$, Pin2 to Pin1
		–	0.4	–		$t_p = 100\text{ ns}$, Pin1 to Pin2

1) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$.

2) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

3 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25^\circ\text{C}$, unless otherwise specified

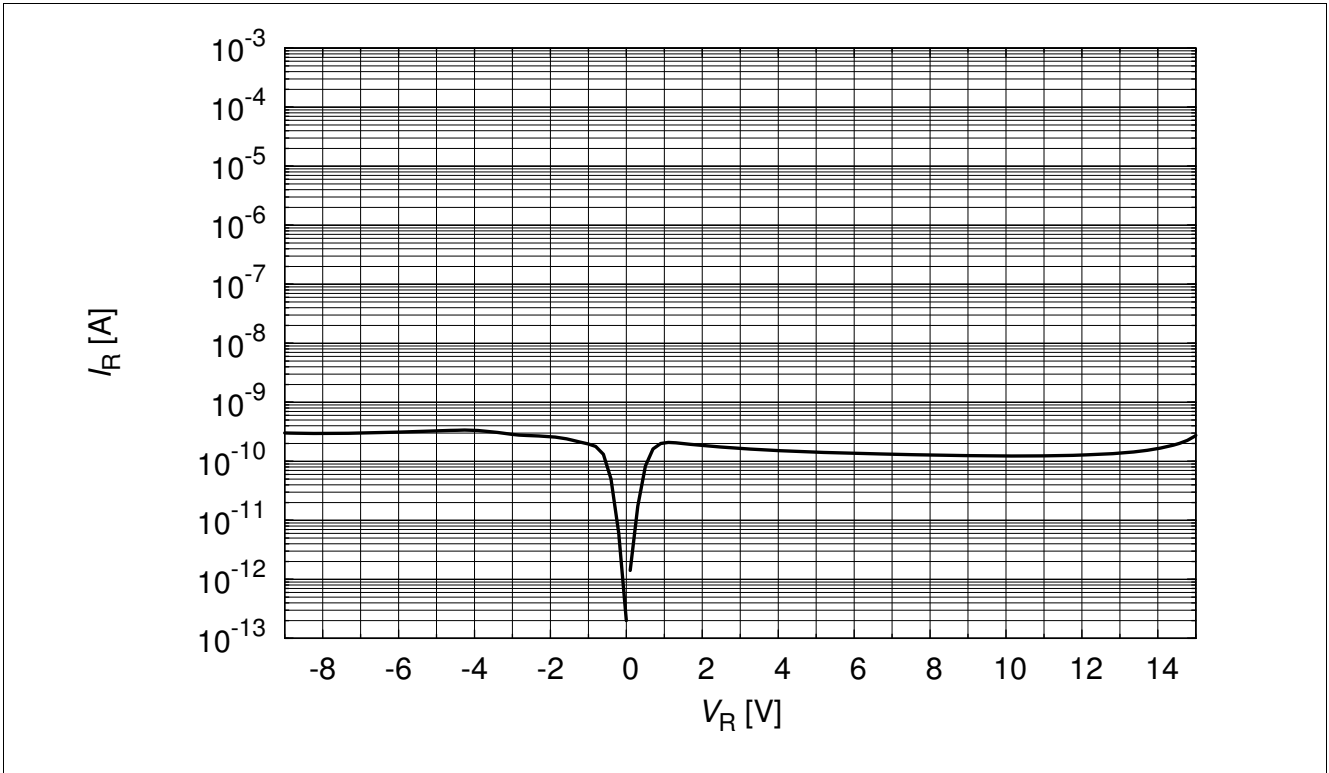


Figure 3-1 Reverse leakage current: $I_R = f(V_R)$, pin 2 to pin 1

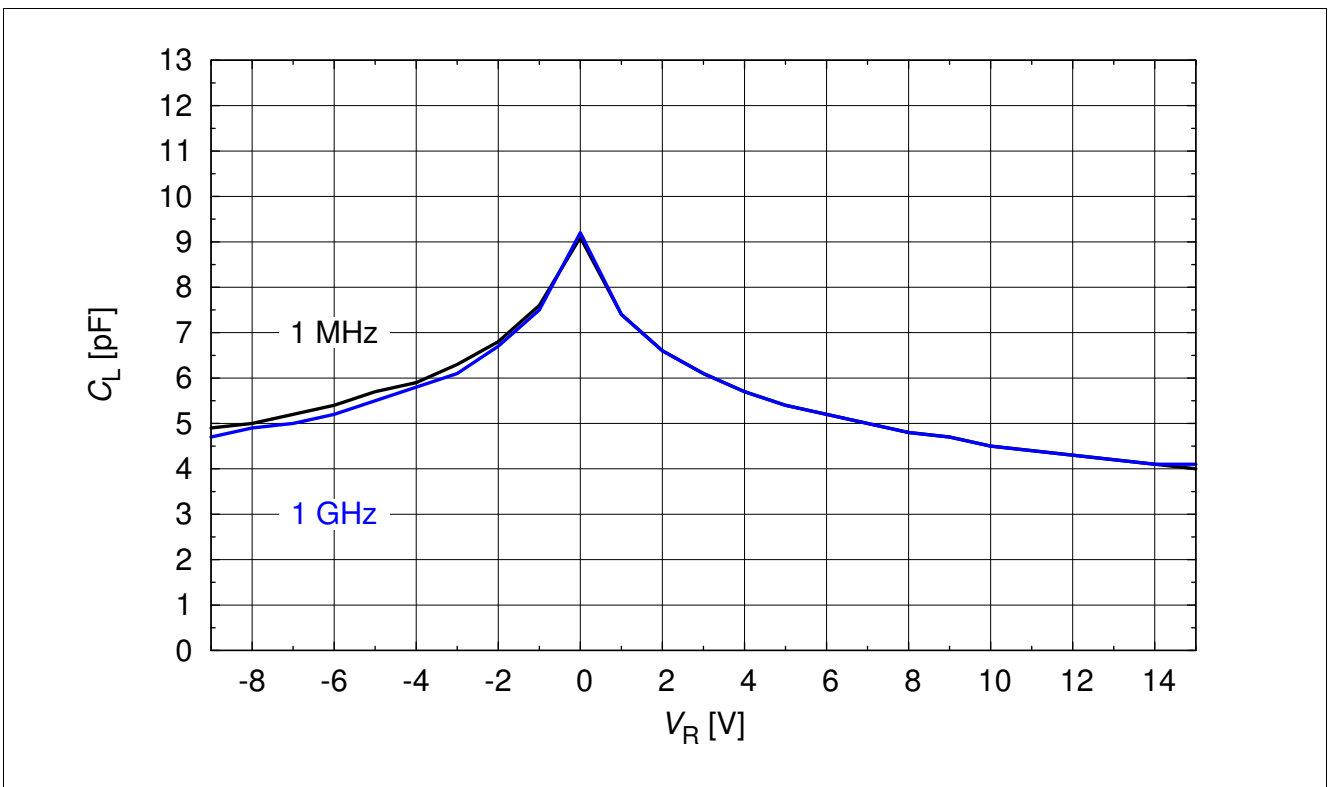


Figure 3-2 Line capacitance: $C_L = f(V_R)$, pin 2 to pin 1

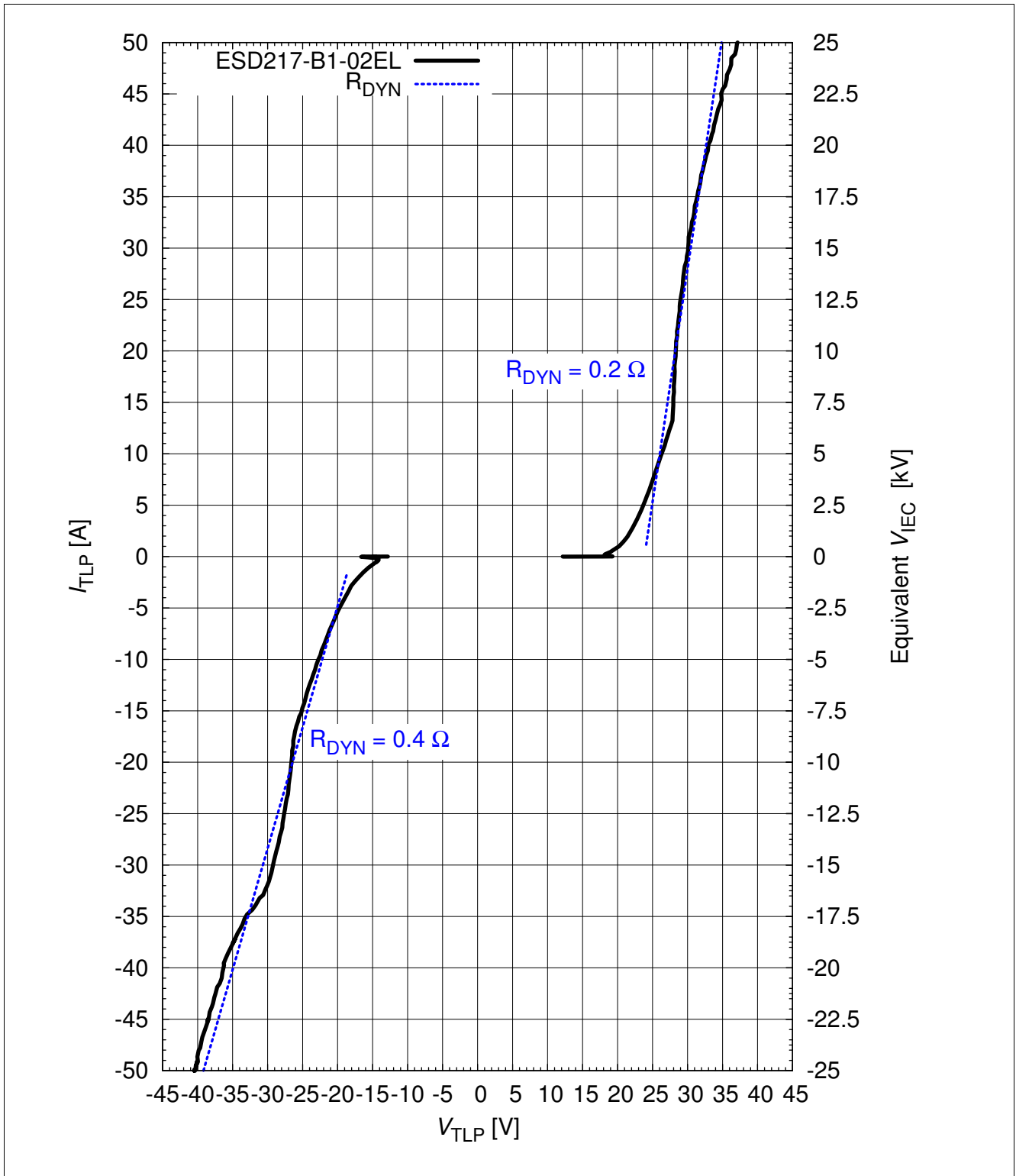


Figure 3-3 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 2 to pin 1

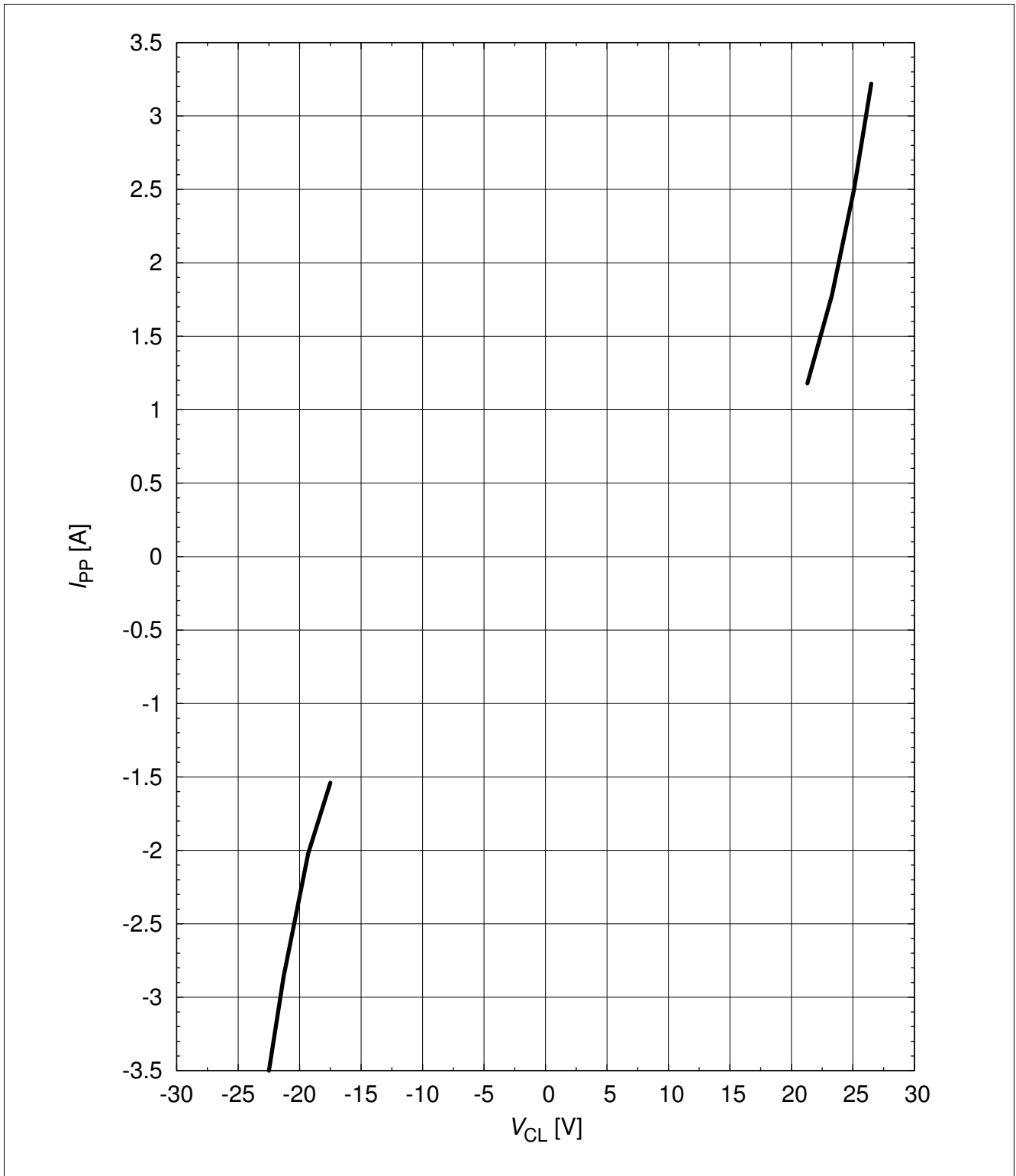


Figure 3-4 Clamping voltage(Surge): $I_{PP} = f(V_{CL})$ [1], pin 2 to pin 1

Typical Characteristics Diagrams

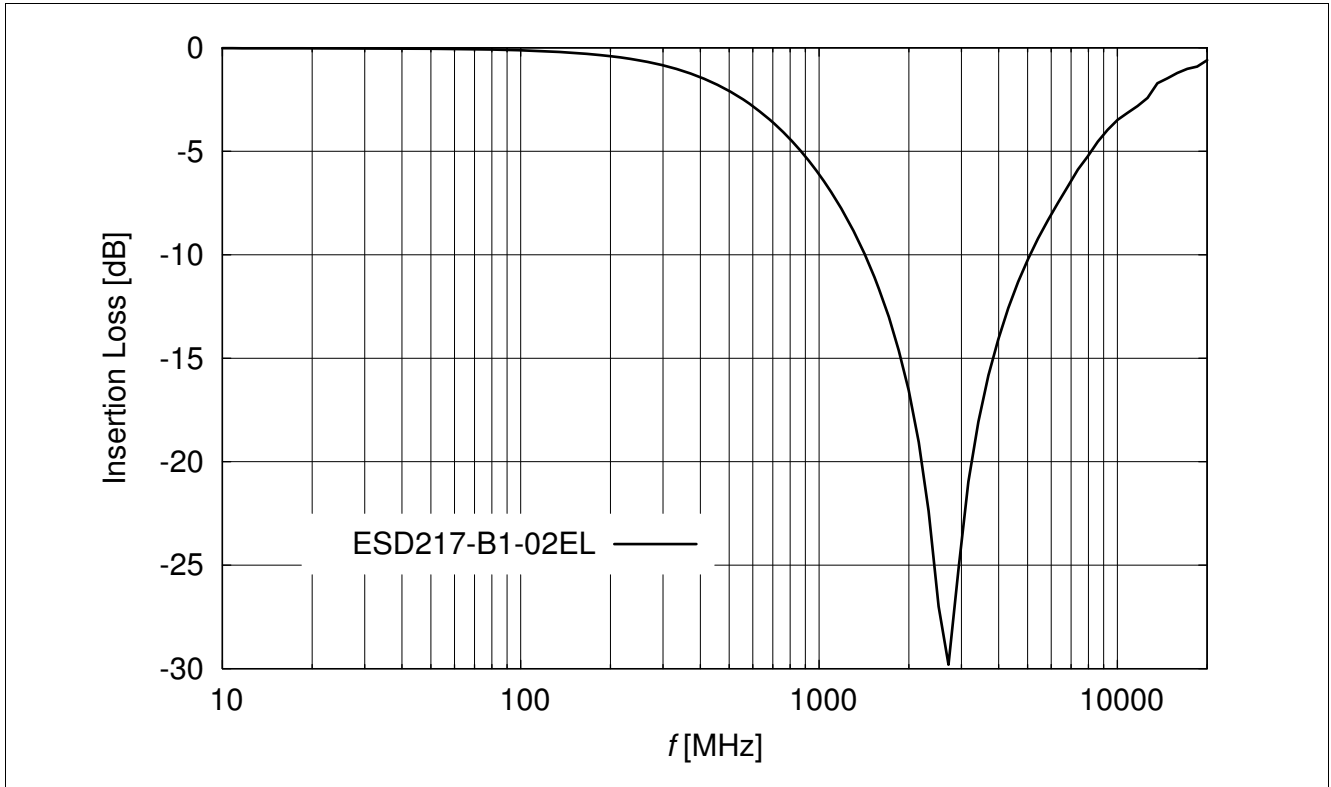


Figure 3-5 Insertion loss vs. frequency in a 50 Ω system

4 Package Information

4.1 TSLP-2-19

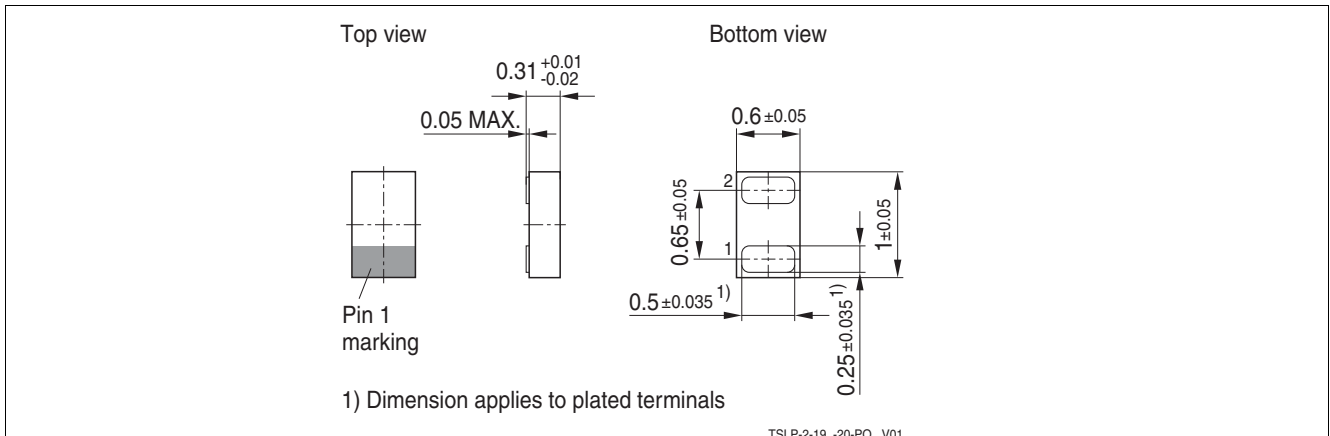


Figure 4-1 TSLP-2-19 Package outline

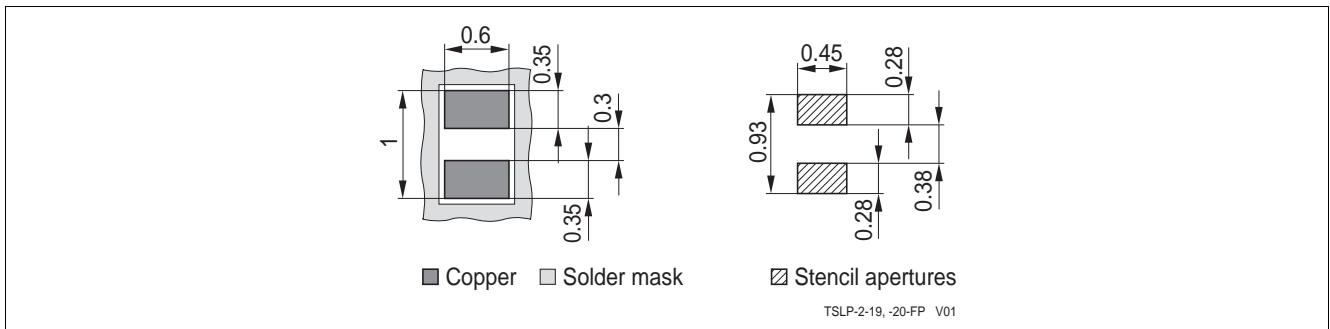


Figure 4-2 TSLP-2-19 Footprint

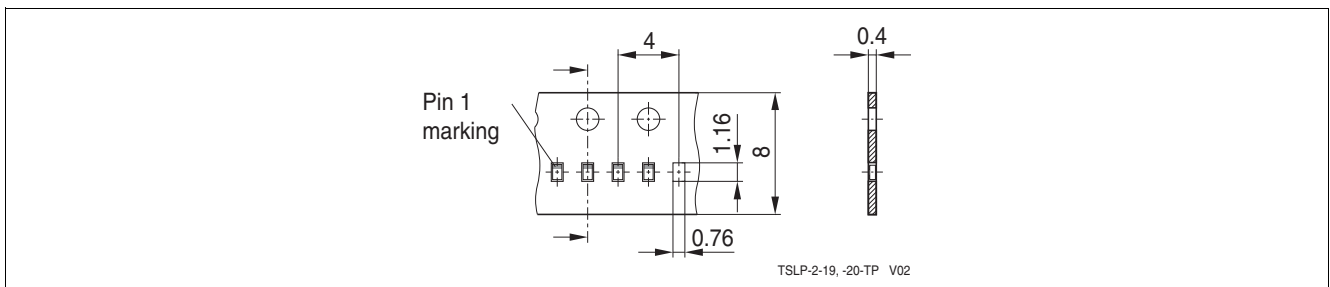


Figure 4-3 TSLP-2-19 Packing

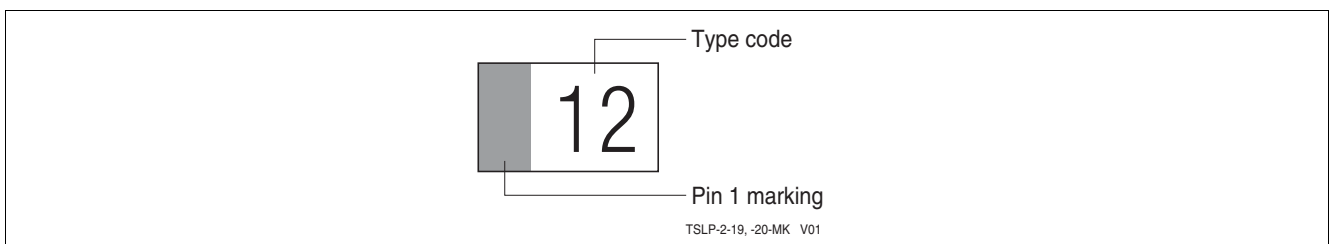


Figure 4-4 TSLP-2-19 Marking example, Type code see: [Table 1-1 “Part Information” on Page 3](#)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

Revision History Rev. 1.0, 2014-05-16

Page or Item	Subjects (major changes since previous revision)
Revision 1.1, 2014-11-11	
3	Table 1-1) updated

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