# THE DATASHEET OF

# PL123-05NSC-R

# PL123-05N/-09N

## Low Skew Fanout Buffer

### FEATURES

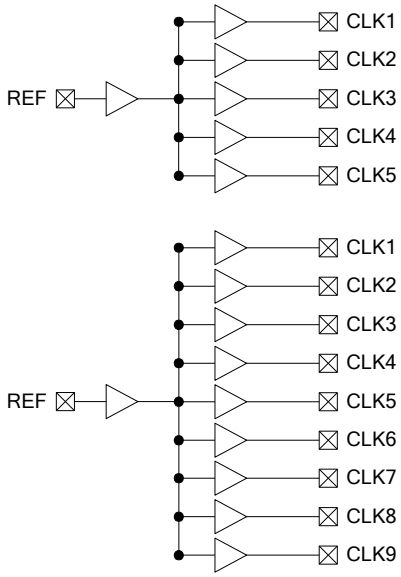
- Output fanout buffer for DC to 134MHz
- Output Options:
  - 1:5 output fanout with *PL123-05*
  - 1:9 output fanout with *PL123-09*
- Low power consumption for portable applications
- Low input-output delay
- Output-Output skew less than 250ps
- Low Additive Phase Jitter of 60fs RMS
- 2.5V to 3.3V, ±10% operation
- 1.8V ±10% operation up to 67MHz
- Operating temperature range from -40°C to 85°C
- Available in 16-Pin SOP (PL123-09) and 8-Pin SOP (PL123-05). Both are GREEN/RoHS packages.

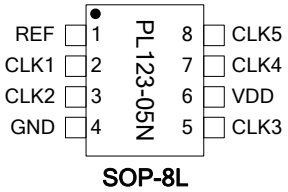
### DESCRIPTION

The PL123-05N and PL123-09N are a low-cost fanout buffers for distributing high-speed clocks with low output to output skew and preserving low noise properties. The fanout buffers accept an input from DC to 134MHz and provide 5 or 9 outputs of the same frequency. A typical PL123-09N application for driving SDRAM in PC systems would use eight outputs to drive two DIMMs, or four SO-DIMMs, with the remaining output used for driving an external feedback to a PLL. A typical PL123-05N application is to fanout a low noise CMOS clock oscillator to 5 low noise CMOS clocks.

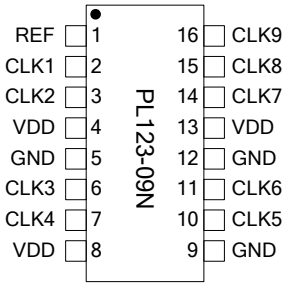
These parts are not intended for 5V input-tolerant applications.

### BLOCK DIAGRAM AND PACKAGE PINOUT




SOP-8L




SOP-16L

## PIN DESCRIPTIONS

| Name | PL123-09N SOP-16L | PL123-05N SOP-8L | Type | Description |
|---|---|---|---|---|
| REF | 1 | 1 | I | Input reference frequency. |
| CLK1 | 2 | 2 | O | Buffered clock output |
| CLK2 | 3 | 3 | O | Buffered clock output |
| VDD | 4, 8, 13 | 6 | P | VDD connection |
| GND | 5, 9, 12 | 4 | P | GND connection |
| CLK3 | 6 | 5 | O | Buffered clock output |
| CLK4 | 7 | 7 | O | Buffered clock output |
| CLK5 | 10 | 8 | O | Buffered clock output |
| CLK6 | 11 | - | O | Buffered clock output |
| CLK7 | 14 | - | O | Buffered clock output |
| CLK8 | 15 | - | O | Buffered clock output |
| CLK9 | 16 | - | O | Buffered clock output |

## LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

### Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections ( looks like ringing ).
- Design long traces (> 1 inch) as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

### Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

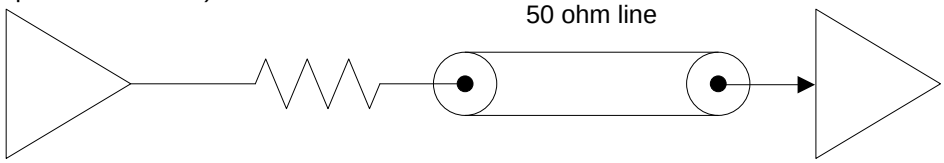
### Typical CMOS termination

Place Series Resistor as close as possible to CMOS output

CMOS Output Buffer

( Typical buffer impedance 20 ohm)

To CMOS Input




Connect a 33 ohm series resistor at each of the output clocks to enhance the stability of the output signal

## ABSOLUTE MAXIMUM CONDITIONS

Supply Voltage to Ground Potential ..... –0.5V to 4.6V
DC Input Voltage ..... $V_{SS}$ – 0.5V to 4.6V
Storage Temperature ..... –65°C to 150°C

Junction Temperature..... 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015).....> 2000V

## OPERATING CONDITIONS

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.62 | 3.63 | V |
| $T_A$ | Commercial Operating Temperature (ambient temperature) | 0 | 70 | °C |
| | Industrial Operating Temperature (ambient temperature) | -40 | 85 | °C |
| $C_L$ | Load Capacitance, below 100 MHz, $V_{DD}$ > 2.25V | – | 30 | pF |
| | Load Capacitance, above 100 MHz, $V_{DD}$ > 2.25V | – | 10 | pF |
| | Load Capacitance, below 67MHz, 1.62V < $V_{DD}$ < 2.25V | – | 15 | pF |
| $C_{IN}$ | Input Capacitance | – | 7 | pF |
| REF, CLK[1:9] | Operating Frequency, Input=Output, $V_{DD}$ > 2.25V | DC | 134 | MHz |
| | Operating Frequency, Input=Output, 1.62V < $V_{DD}$ < 2.25V | DC | 67 | MHz |
| $t_{PU}$ | Power-up time for all $V_{DD}$s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

## ELECTRICAL CHARACTERISTICS (Commercial and Industrial Temperature Devices)

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage [1] | $V_{DD}$ > 2.25V | – | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage [1] | $V_{DD}$ > 2.25V | 2.0 | – | V |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | – | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | – | 100 | µA |
| $V_{OL}$ | Output LOW Voltage [2] | $I_{OL}$ = 8 mA , $V_{DD}$ > 2.97V | – | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage [2] | $I_{OH}$ = –8 mA , $V_{DD}$ > 2.97V | 2.4 | – | V |
| $I_{DD}$ | Supply Current | 66.67MHz with unloaded outputs | – | 32 | mA |

## SWITCHING CHARACTERISTICS (Commercial and Industrial Temperature Devices) [3]

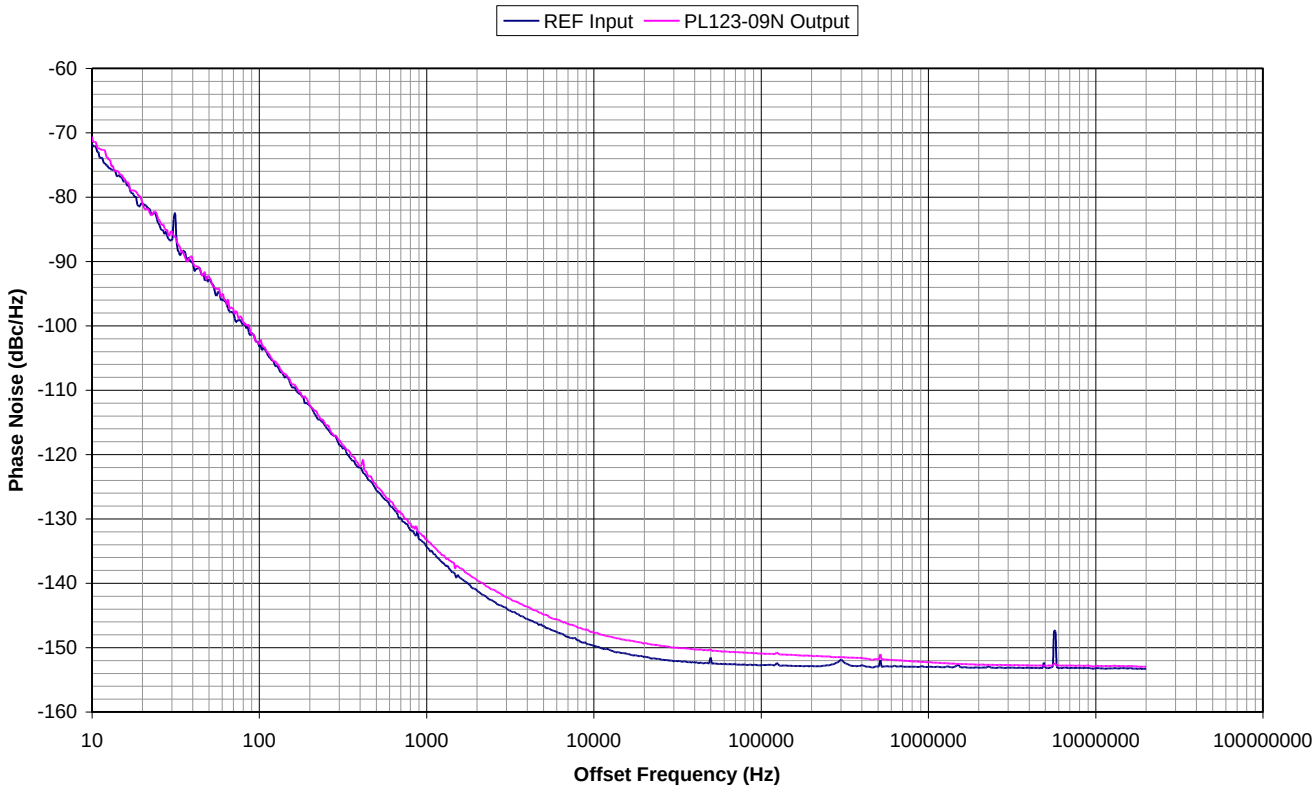
| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Duty Cycle [2] = t2 ÷ t1 | Measured at 1.4V, $V_{DD}$=3.3V, Input=50% | 40 | 50 | 60 | % |
| | | Measured at $V_{DD}$/2 , Input = 50% | 40 | 50 | 60 | % |
| $t_3$ | Rise Time [2] | 0.8V ➔ 2.0V , $V_{DD}$=3.3V , 30pF Load | – | – | 1.5 | ns |
| | | 10% ➔ 90% , $V_{DD}$=2.5V , 15pF Load | – | – | 2.5 | ns |
| | | 10% ➔ 90% , $V_{DD}$=1.8V , 15pF Load | – | – | 4.5 | ns |
| $t_4$ | Fall Time [2] | 2.0V ➔ 0.8V , $V_{DD}$=3.3V , 30pF Load | – | – | 1.5 | ns |
| | | 90% ➔ 10% , $V_{DD}$=2.5V , 15pF Load | – | – | 2.5 | ns |
| | | 90% ➔ 10% , $V_{DD}$=1.8V , 15pF Load | – | – | 4.5 | ns |
| $t_5$ | Output to Output Skew [2] | All outputs equally loaded | – | – | 250 | ps |
| $t_6$ | Propagation Delay, REF Rising Edge to CLKX Rising Edge [2] | Measured at $V_{DD}$/2 | 1 | 5 | 9.2 | ns |

**Notes:**
1. REF input has a threshold voltage of $V_{DD}$/2
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.
3. All parameters are specified with loaded outputs.

**NOISE CHARACTERISTICS** (Commercial and Industrial Temperature Devices)

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Additive Phase Jitter | $V_{DD}$=3.3V, Frequency=100MHz<br>Offset=12KHz ~ 20MHz | | 60 | | fs |

**PL123-09N Additive Phase Jitter:**
**VDD=3.3V, CLK=100MHz, Integration Range 12KHz to 20MHz: 0.059ps typical.**

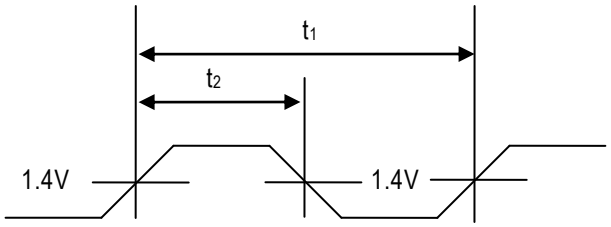



When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

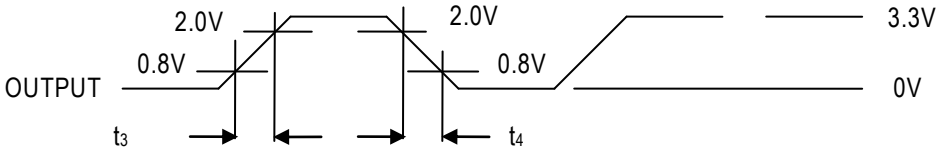
$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

## SWITCHING WAVEFORMS

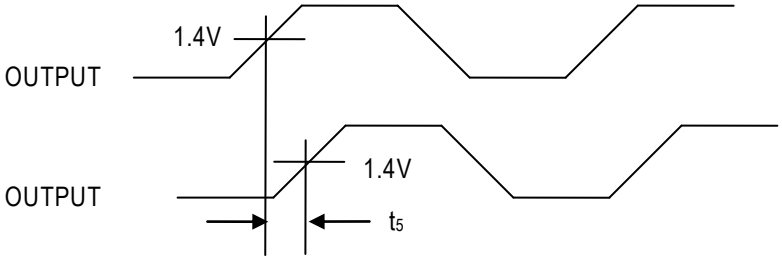
### Duty Cycle Timing



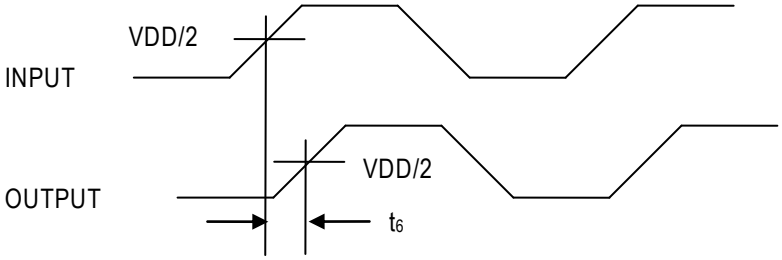

### All Outputs Rise/Fall Time



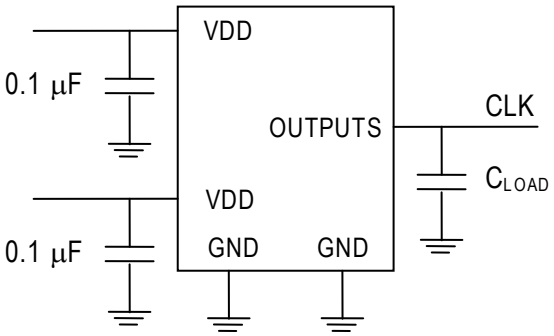

### Output-Output Skew




### Input-Output Propagation Delay



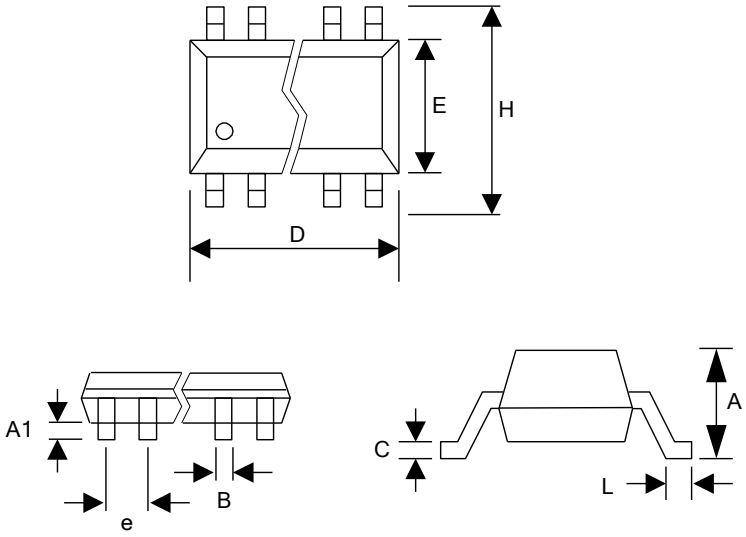

## TEST CIRCUIT



## PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)

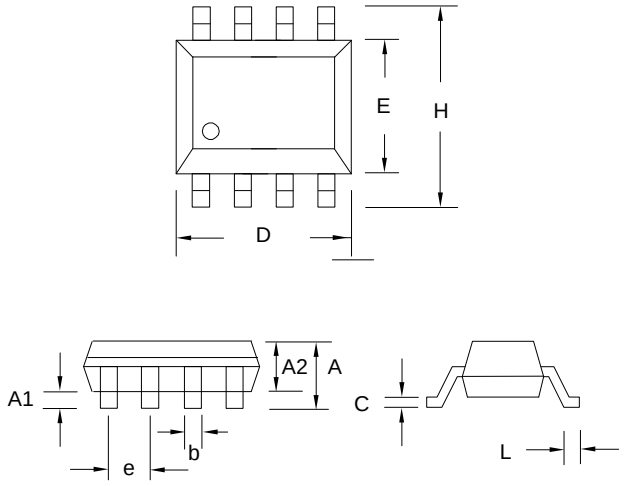
### SOP-16L ( mm )

| Symbol | Min. | Max. |
|---|---|---|
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 9.80 | 10.00 |
| E | 3.80 | 4.00 |
| H | 5.80 | 6.20 |
| L | 0.40 | 1.27 |
| e | 1.27 BSC | |




### SOP-8L (mm)

| Symbol | Min. | Max. |
|---|---|---|
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | 1.50 |
| B | 0.33 | 0.53 |
| C | 0.19 | 0.27 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| H | 5.80 | 6.20 |
| L | 0.40 | 0.89 |
| e | 1.27 BSC | |

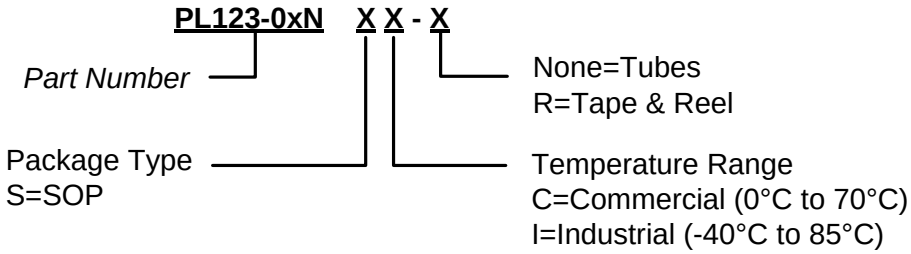


## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

**PART NUMBER**

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range




| Part/Order Number | Marking | Package Option |
|---|---|---|
| Green (Lead-Free) Package | | |
| PL123-09NSC | P12309N<br>SC<br>LLLLL | 16-Pin SOP Tube |
| PL123-09NSC-R | | 16-Pin SOP (Tape and Reel) |
| PL123-09NSI | P12309N<br>SI<br>LLLLL | 16-Pin SOP Tube |
| PL123-09NSI-R | | 16-Pin SOP (Tape and Reel) |
| PL123-05NSC | P12305N<br>SC<br>LLLLL | 8-Pin SOP Tube |
| PL123-05NSC-R | | 8-Pin SOP (Tape and Reel) |
| PL123-05NSI | P12305N<br>SI<br>LLLLL | 8-Pin SOP Tube |
| PL123-05NSI-R | | 8-Pin SOP (Tape and Reel) |

***Note: LLLLL designates lot number**

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