



**THE DATASHEET OF  
CDC318ADLRG4**



# CDC318A

## 1-LINE TO 18-LINE CLOCK DRIVER WITH I<sup>2</sup>C CONTROL INTERFACE

SCAS614A – SEPTEMBER 1998 – REVISED JUNE 2002

- **High-Speed, Low-Skew 1-to-18 Clock Buffer for Synchronous DRAM (SDRAM) Clock Buffering Applications**
- **Output Skew,  $t_{sk(o)}$ , Less Than 250 ps**
- **Pulse Skew,  $t_{sk(p)}$ , Less Than 500 ps**
- **Supports up to Four Unbuffered SDRAM Dual Inline Memory Modules (DIMMs)**
- **I<sup>2</sup>C Serial Interface Provides Individual Enable Control for Each Output**
- **Operates at 3.3 V**
- **Distributed V<sub>CC</sub> and Ground Pins Reduce Switching Noise**
- **100-MHz Operation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Packaged in 48-Pin Shrink Small Outline (DL) Package**

### description

The CDC318A is a high-performance clock buffer designed to distribute high-speed clocks in PC applications. This device distributes one input (A) to 18 outputs (Y) with minimum skew for clock distribution. The CDC318A operates from a 3.3-V power supply. It is characterized for operation from 0°C to 70°C.

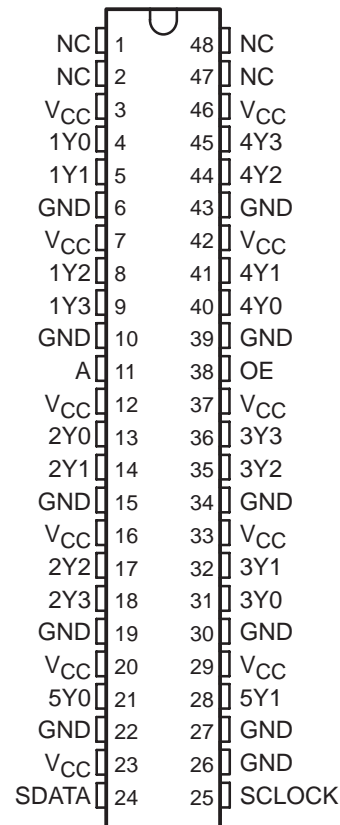
This device has been designed with consideration for optimized EMI performance. Depending on the application layout, damping resistors in series to the clock outputs (like proposed in the PC100 specification) may not be needed in most cases.

The device provides a standard mode (100K-bits/s) I<sup>2</sup>C serial interface for device control. The implementation is as a slave/receiver. The device address is specified in the I<sup>2</sup>C device address table. Both of the I<sup>2</sup>C inputs (SDATA and SCLOCK) are 5-V tolerant and provide integrated pullup resistors (typically 140 kΩ).

Three 8-bit I<sup>2</sup>C registers provide individual enable control for each of the outputs. All outputs default to enabled at powerup. Each output can be placed in a disabled mode with a low-level output when a low-level control bit is written to the control register. The registers are write only and must be accessed in sequential order (i.e., random access of the registers is not supported).

The CDC318A provides 3-state outputs for testing and debugging purposes. The outputs can be placed in a high-impedance state via the output-enable (OE) input. When OE is high, all outputs are in the operational state. When OE is low, the outputs are placed in a high-impedance state. OE provides an integrated pullup resistor.

**DL PACKAGE  
(TOP VIEW)**



NC – No internal connection



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**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# CDC318A

## 1-LINE TO 18-LINE CLOCK DRIVER

### WITH I<sup>2</sup>C CONTROL INTERFACE

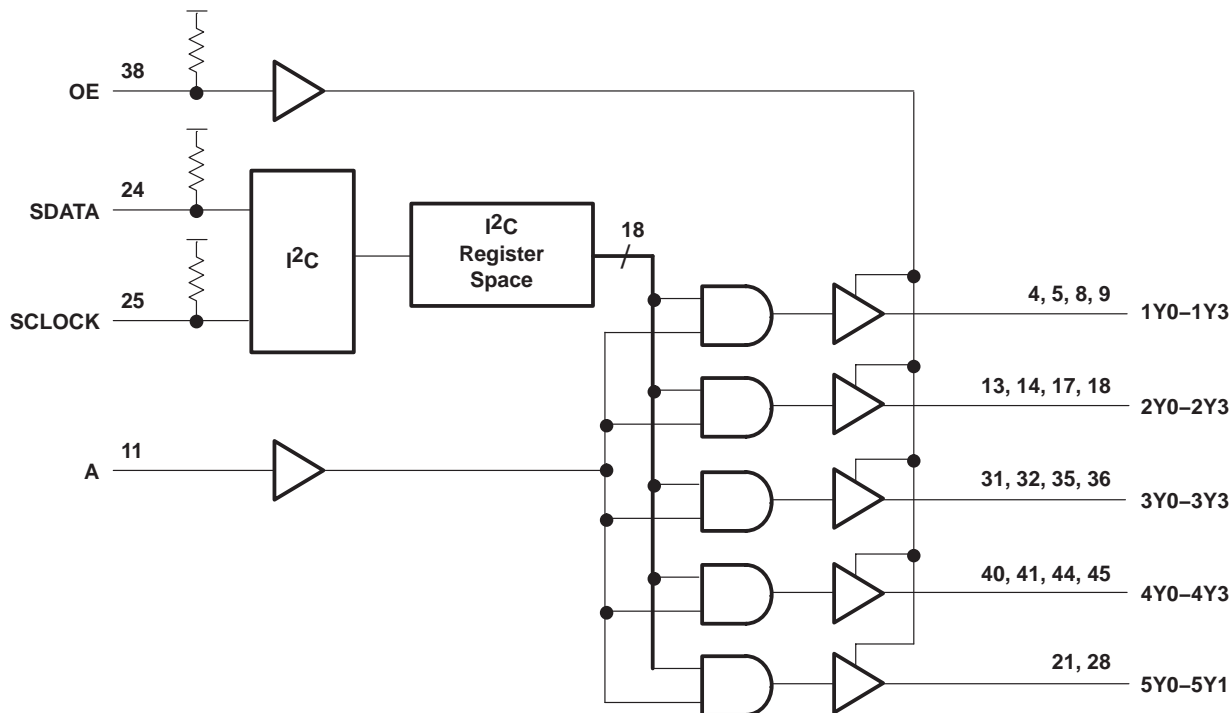
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FUNCTION TABLE

INPUTS		OUTPUTS				
OE	A	1Y0-1Y3	2Y0-2Y3	3Y0-3Y3	4Y0-4Y3	5Y0-5Y1
L	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
H	L	L	L	L	L	L
H	H	H†	H†	H†	H†	H†

† The function table assumes that all outputs are enabled via the appropriate I<sup>2</sup>C configuration register bit. If the output is disabled via the appropriate configuration bit, then the output is driven to a low state, regardless of the state of the A input.

### logic diagram (positive logic)



### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
1Y0–1Y3	4, 5, 8, 9	O	3.3-V SDRAM byte 0 clock outputs
2Y0–2Y3	13, 14, 17, 18	O	3.3-V SDRAM byte 1 clock outputs
3Y0–3Y3	31, 32, 35, 36	O	3.3-V SDRAM byte 2 clock outputs
4Y0–4Y3	40, 41, 44, 45	O	3.3-V SDRAM byte 3 clock outputs
5Y0–5Y1	21, 28	O	3.3-V clock outputs provided for feedback control of external phase-locked loops (PLLs)
A	11	I	Clock input
OE	38	I	Output enable. When asserted, OE puts all outputs in a high-impedance state. A nominal 140-k $\Omega$ pullup resistor is internally integrated.
SCLOCK	25	I	I <sup>2</sup> C serial clock input. A nominal 140-k $\Omega$ pullup resistor is internally integrated.
SDATA	24	I/O	Bidirectional I <sup>2</sup> C serial data input/output. A nominal 140-k $\Omega$ pullup resistor is internally integrated.
GND	6, 10, 15, 19, 22, 26, 27, 30, 34, 39, 43		Ground
NC	1, 2, 47, 48		No internal connection. Reserved for future use.
V <sub>CC</sub>	3, 7, 12, 16, 20, 23, 29, 33, 37, 42, 46		3.3-V power supply

#### I<sup>2</sup>C DEVICE ADDRESS

A7	A6	A5	A4	A3	A2	A1	A0 (R/W)
H	H	L	H	L	L	H	—

#### I<sup>2</sup>C BYTE 0-BIT DEFINITION<sup>†</sup>

BIT	DEFINITION	DEFAULT VALUE
7	2Y3 enable (pin 18)	H
6	2Y2 enable (pin 17)	H
5	2Y1 enable (pin 14)	H
4	2Y0 enable (pin 13)	H
3	1Y3 enable (pin 9)	H
2	1Y2 enable (pin 8)	H
1	1Y1 enable (pin 5)	H
0	1Y0 enable (pin 4)	H

<sup>†</sup> When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

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### I<sup>2</sup>C BYTE 1-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	4Y3 enable (pin 45)	H
6	4Y2 enable (pin 44)	H
5	4Y1 enable (pin 41)	H
4	4Y0 enable (pin 40)	H
3	3Y3 enable (pin 36)	H
2	3Y2 enable (pin 35)	H
1	3Y1 enable (pin 32)	H
0	3Y0 enable (pin 31)	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

### I<sup>2</sup>C BYTE 2-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	5Y1 enable (pin 28)	H
6	5Y0 enable (pin 21)	H
5	Reserved	H
4	Reserved	H
3	Reserved	H
2	Reserved	H
1	Reserved	H
0	Reserved	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (SCLOCK, SDATA) (see Note 1) .....	-0.5 V to 6.5 V
Output voltage range, $V_O$ (SDATA) (see Note 1) .....	-0.5 V to 6.5 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state (except SDATA), $I_O$ .....	48 mA
Current into SDATA in the low state, $I_O$ .....	12 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) (SCLOCK) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) (SDATA) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3) .....	84°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero. The absolute maximum power dissipation allowed at  $T_A = 55^\circ\text{C}$  (in still air) is 1.2 W.  
 3. Thermal impedance ( $\theta_{JA}$ ) can be considerably lower if the device is soldered on the PCB board with a copper layer underneath the package. A simulation on a PCB board (3 in.  $\times$  3 in.) with two internal copper planes (1 oz. cu, 0.036 mm thick) and 0.071 mm cu (202) in area underneath the package, resulted in  $\theta_{JA} = 60^\circ\text{C/W}$ . This would allow 1.2 W total power dissipation at  $T_A = 70^\circ\text{C}$ .

**recommended operating conditions (see Note 4)**

		MIN	TYP	MAX	UNIT
$V_{CC}$	3.3-V core supply voltage	3.135		3.465	V
$V_{IH}$	High-level input voltage	A, OE	2	$V_{CC} + 0.3$	V
		SDATA, SCLOCK (see Note 3)	2.2	5.5	V
$V_{IL}$	Low-level input voltage	A, OE	-0.3	0.8	V
		SDATA, SCLOCK (see Note 3)	0	1.04	V
$I_{OH}$	High-level output current			-36	mA
$I_{OL}$	Low-level output current			24	mA
$r_i$	Input resistance to $V_{CC}$		140		k $\Omega$
$f(\text{SCL})$	SCLOCK frequency			100	kHz
$t(\text{BUS})$	Bus free time	4.7			$\mu\text{s}$
$t_{su}(\text{START})$	START setup time	4.7			$\mu\text{s}$
$t_h(\text{START})$	START hold time	4			$\mu\text{s}$
$t_w(\text{SCLL})$	SCLOCK low pulse duration	4.7			$\mu\text{s}$
$t_w(\text{SCLH})$	SCLOCK high pulse duration	4			$\mu\text{s}$
$t_r(\text{SDATA})$	SDATA input rise time			1000	ns
$t_f(\text{SDATA})$	SDATA input fall time			300	ns
$t_{su}(\text{SDATA})$	SDATA setup time	250			ns
$t_h(\text{SDATA})$	SDATA hold time	20			ns
$t_{su}(\text{STOP})$	STOP setup time	4			$\mu\text{s}$
$T_A$	Operating free-air temperature	0		70	$^\circ\text{C}$

NOTE 4: The CMOS-level inputs fall within these limits:  $V_{IH} \text{ min} = 0.7 \times V_{CC}$  and  $V_{IL} \text{ max} = 0.3 \times V_{CC}$ .



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 3.135 V, I <sub>I</sub> = -18 mA				-1.2	V	
V <sub>OH</sub>	High-level output voltage	Y outputs	V <sub>CC</sub> = Min to Max, I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.1 V			V	
			V <sub>CC</sub> = 3.135 V, I <sub>OH</sub> = -36 mA	2.4				
V <sub>OL</sub>	Low-level output voltage	Y outputs	V <sub>CC</sub> = Min to Max, I <sub>OL</sub> = 1 mA	0.1			V	
			V <sub>CC</sub> = 3.135 V, I <sub>OL</sub> = 24 mA	0.4				
		SDATA	V <sub>CC</sub> = 3.135 V	I <sub>OL</sub> = 3 mA	0.4			
				I <sub>OL</sub> = 6 mA	0.6			
I <sub>OH</sub>	High-level output current	SDATA	V <sub>CC</sub> = 3.135 V, V <sub>O</sub> = V <sub>CC</sub> MAX	20			μA	
		Y outputs	V <sub>CC</sub> = 3.135 V, V <sub>O</sub> = 2 V	-54	-126		mA	
			V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 1.65 V	-92				
			V <sub>CC</sub> = 3.465 V, V <sub>O</sub> = 3.135 V	-21	-46			
I <sub>OL</sub>	Low-level output current	Y outputs	V <sub>CC</sub> = 3.135 V, V <sub>O</sub> = 1 V	49	118		mA	
			V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = 1.65 V	93				
			V <sub>CC</sub> = 3.465 V, V <sub>O</sub> = 0.4 V	24	53			
I <sub>IH</sub>	High-level input current	A	V <sub>CC</sub> = 3.465 V, V <sub>I</sub> = V <sub>CC</sub>	5			μA	
		OE		20				
		SCLOCK, SDATA		20				
I <sub>IL</sub>	Low-level input current	A	V <sub>CC</sub> = 3.465 V, V <sub>I</sub> = GND	-5			μA	
		OE		-10	-50			
		SCLOCK, SDATA		-10	-50			
I <sub>OZ</sub>	High-impedance-state output current	V <sub>CC</sub> = 3.465 V, V <sub>O</sub> = 3.465 V or 0		±10			μA	
I <sub>off</sub>	Off-state current	SCLOCK, SDATA	V <sub>CC</sub> = 0, V <sub>I</sub> = 0 V to 5.5 V		50			μA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 3.465 V, I <sub>O</sub> = 0		0.2	0.5		mA	
ΔI <sub>CC</sub>	Change in supply current	V <sub>CC</sub> = 3.135 V to 3.465 V, One input at V <sub>CC</sub> - 0.6 V, All other inputs at V <sub>CC</sub> or GND		500			μA	
		Dynamic I <sub>CC</sub> at 100 MHz		V <sub>CC</sub> = 3.465 V, C <sub>L</sub> = 20 pF,	230			mA
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 3.3 V		4			pF	
C <sub>O</sub>	Output capacitance	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 3.3 V		6			pF	
C <sub>I/O</sub>	SDATA I/O capacitance	V <sub>I/O</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 3.3 V		7			pF	

**switching characteristics over recommended operating conditions**

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub>	Low-to-high level propagation delay time	A	Y		1.2	4.5	ns
		SCLOCK↓	SDATA valid	V <sub>CC</sub> = 3.3 V ±0.165 V, See Figure 3		2	μs
t <sub>PLH</sub>	Low-to-high level propagation delay time	SDATA↑	Y	V <sub>CC</sub> = 3.3 V ±0.165 V, See Figure 3		150	ns
t <sub>PHL</sub>	High-to-low level propagation delay time	A	Y		1.2	4.5	ns
		SCLOCK↓	SDATA valid	V <sub>CC</sub> = 3.3 V ±0.165 V, See Figure 3		2	μs
t <sub>PHL</sub>	High-to-low level propagation delay time	SDATA↑	Y	V <sub>CC</sub> = 3.3 V ±0.165 V, See Figure 3		150	ns
t <sub>PZH</sub>	Enable time to the high level	OE	Y		1	7	ns
t <sub>PZL</sub>	Enable time to the low level				1	7	
t <sub>PHZ</sub>	Disable time from the high level	OE	Y		1	7	ns
t <sub>PLZ</sub>	Disable time from the low level				1	7	
t <sub>sk(o)</sub>	Skew time	A	Y			250	ps
t <sub>sk(p)</sub>	Skew time	A	Y			500	ps
t <sub>sk(pr)</sub>	Skew time	A	Y			1	ns
t <sub>r</sub>	Rise time		Y		0.5	2.2	ns
t <sub>r</sub>	Rise time (see Note 5 and Figure 3)	SDATA		C <sub>L</sub> = 10 pF	6		ns
				C <sub>L</sub> = 400 pF		950	
t <sub>f</sub>	Fall time		Y		0.5	2.3	ns
t <sub>f</sub>	Fall time (see Note 5 and Figure 3)	SDATA		C <sub>L</sub> = 10 pF	20		ns
				C <sub>L</sub> = 400 pF		250	

NOTE 5: This parameter has a lower limit than BUS specification. This allows use of series resistors for current spike protection.

**ESD information**

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	200 V
Charge Device Model (CDM)	2.0 kV

**thermal information**

CDC318A 48-PIN SSOP			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
R <sub>θJA</sub>	High K		62	56	54	51	°C/W
R <sub>θJA</sub>	Low K		95	71	65	58	°C/W
R <sub>θJC</sub>	High K	36					°C/W
R <sub>θJC</sub>	Low K	38					°C/W

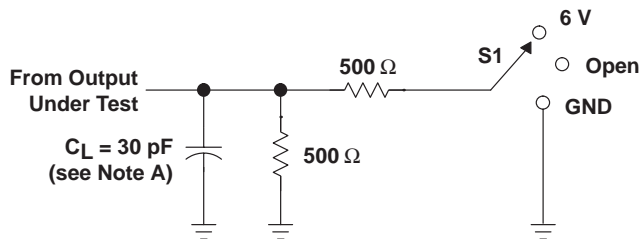
# CDC318A

## 1-LINE TO 18-LINE CLOCK DRIVER

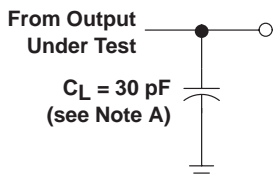
### WITH I<sup>2</sup>C CONTROL INTERFACE

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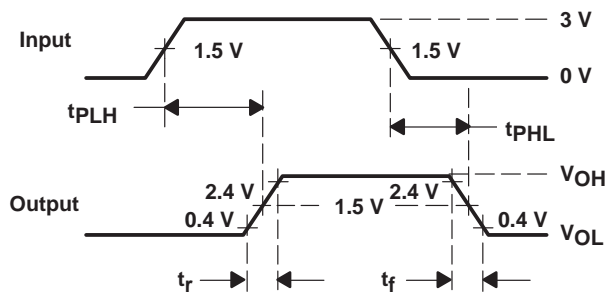
#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR  $t_{pd}$  AND  $t_{sk}$

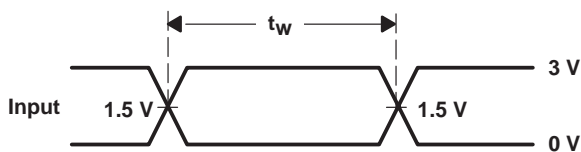


LOAD CIRCUIT FOR  $t_r$  AND  $t_f$

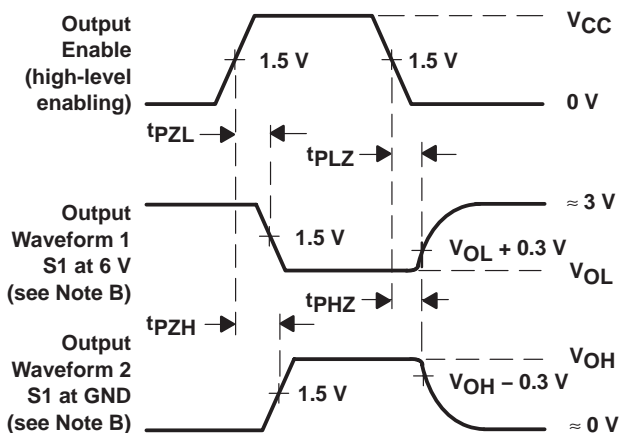


VOLTAGE WAVEFORMS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS

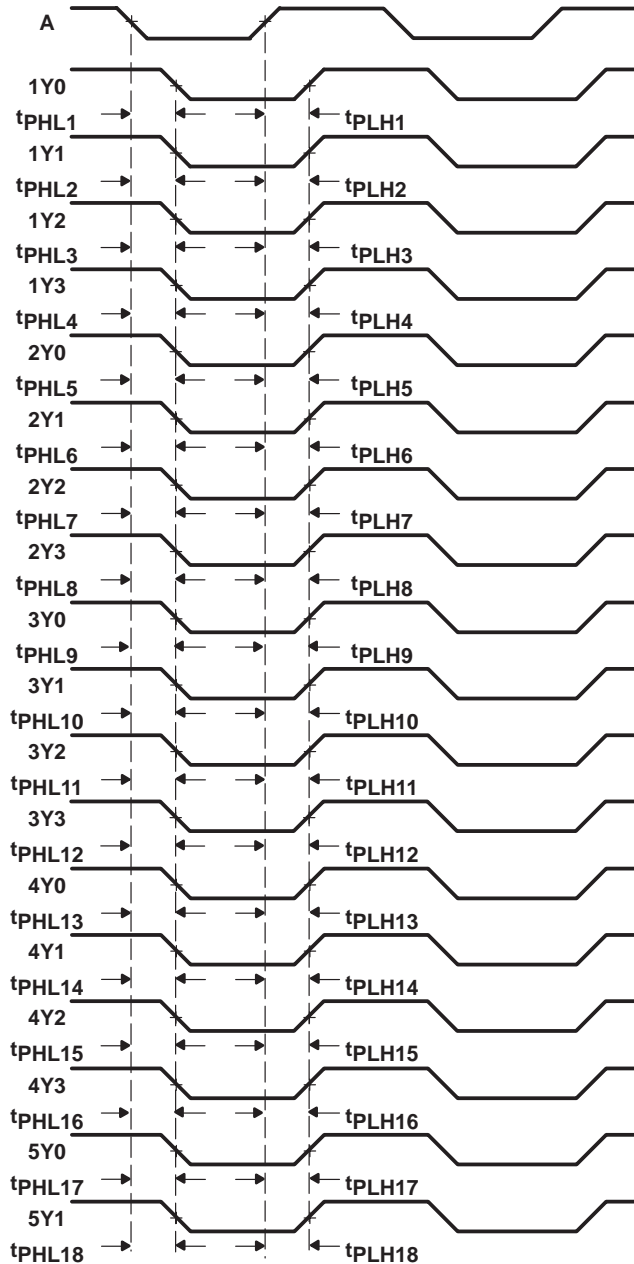


VOLTAGE WAVEFORMS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**



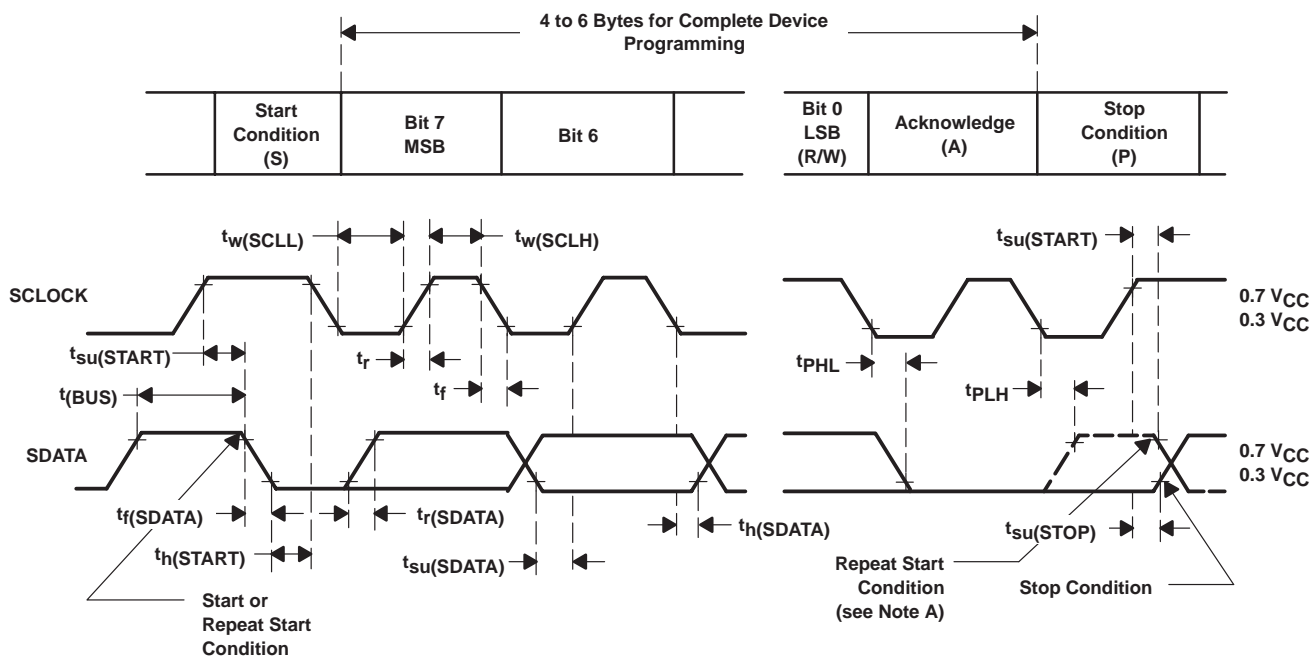
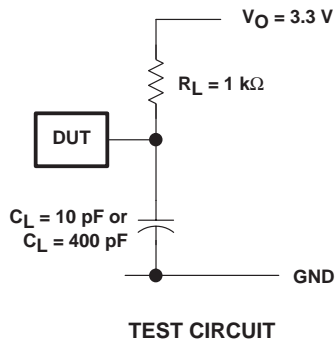
- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1:18$ )
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1:18$ )
- B. Pulse skew,  $t_{sk(p)}$ , is calculated as the greater of  $|t_{PLHn} - t_{PHLn}|$  ( $n = 1:18$ )
- C. Process skew,  $t_{sk(pr)}$ , is calculated as the greater of:
- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1:18$ ) across multiple devices under identical operating conditions
  - The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1:18$ ) across multiple devices under identical operating conditions

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$ ,  $t_{sk(p)}$ ,  $t_{sk(pr)}$**

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**PARAMETER MEASUREMENT INFORMATION**



BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2	Command (dummy value, ignored)
3	Byte count (dummy value, ignored)
4	I <sup>2</sup> C data byte 0
5	I <sup>2</sup> C data byte 1
6	I <sup>2</sup> C data byte 2

NOTES: A. The repeat start condition is not supported.  
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 kHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≥ 10 ns, t<sub>f</sub> ≥ 10 ns.

**Figure 3. Propagation Delay Times, t<sub>r</sub> and t<sub>f</sub>**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC318ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A	<a href="#">Samples</a>
CDC318ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A	<a href="#">Samples</a>
CDC318ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A	<a href="#">Samples</a>
CDC318ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	CDC318A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

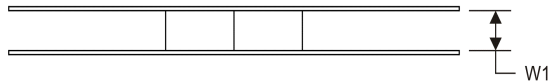
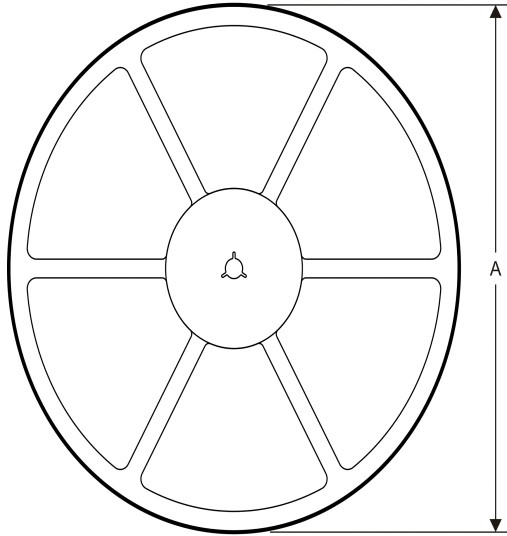
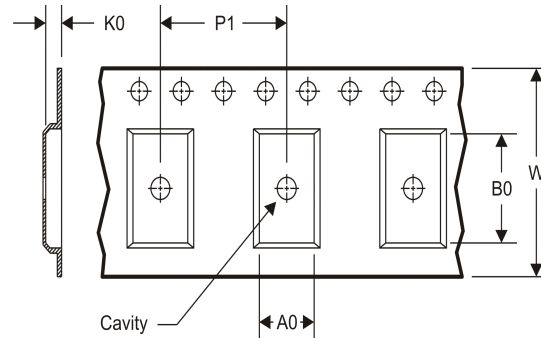
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC318ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC318ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

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