

NX3DV3899

Dual double-pole double-throw analog switch

Rev. 3.2 — 21 June 2024

Product data sheet

1 General description

The NX3DV3899 is a dual double-pole double-throw analog data-switch suitable for use as an analog or digital multiplexer/demultiplexer. It consists of four switches, each with two independent input/outputs (nY0 and nY1) and a common input/output (nZ). The two digital inputs (1S and 2S) are used to select the switch position. Schmitt trigger action at the select input (nS) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 1.4 V to 4.3 V.

A low input voltage threshold allows pin nS to be driven by lower level logic signals without a significant increase in supply current I_{CC} . This makes it possible for the NX3DV3899 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3DV3899 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ.

2 Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
 - 7.2 Ω (typical) at $V_{CC} = 1.4$ V
 - 5.4 Ω (typical) at $V_{CC} = 1.65$ V
 - 2.9 Ω (typical) at $V_{CC} = 2.5$ V
 - 2.4 Ω (typical) at $V_{CC} = 3.0$ V
 - 2.3 Ω (typical) at $V_{CC} = 3.6$ V
 - 2.2 Ω (typical) at $V_{CC} = 4.3$ V
- Break-before-make switching
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 2A exceeds 2000 V (all pins)
 - HBM JESD22-A114F Class 3A exceeds 5000 V (I/O pins to GND)
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- 1.8 V control logic at $V_{CC} = 3.6$ V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3 Applications

- Data switch
- Cell phone



- PDA
- Portable media player

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		Version
		Name	Description	
NX3DV3899HR	x99	HXQFN16(U)	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 mm x 3 mm x 0.5 mm	SOT1039-2
NX3DV3899GU	x9	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm	SOT1161-1

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
NX3DV3899HR	NX3DV3899HR,115	HXQFN16(U)	REEL 7" Q1 NDP ^[1]	1500	-40°C to +125°C
	NX3DV3899HRZ	HXQFN16(U)	REEL 7" Q1 NDP SSB ^[2]	1500	-40°C to +125°C
NX3DV3899GU	NX3DV3899GU,115	XQFN16	REEL 7" Q1 NDP	4000	-40°C to +125°C

[1] Will go EOL - migrate to new leadframe NX3DV3899HRZ orderable part number.

[2] This packing method uses a Static Shielding Bag (SSB) solution. Material is to be kept in the sealed bag between uses.

5 Functional diagram

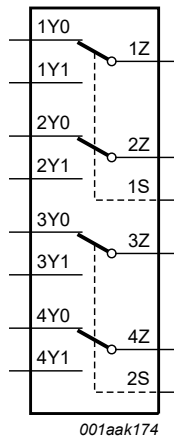


Figure 1. Logic symbol

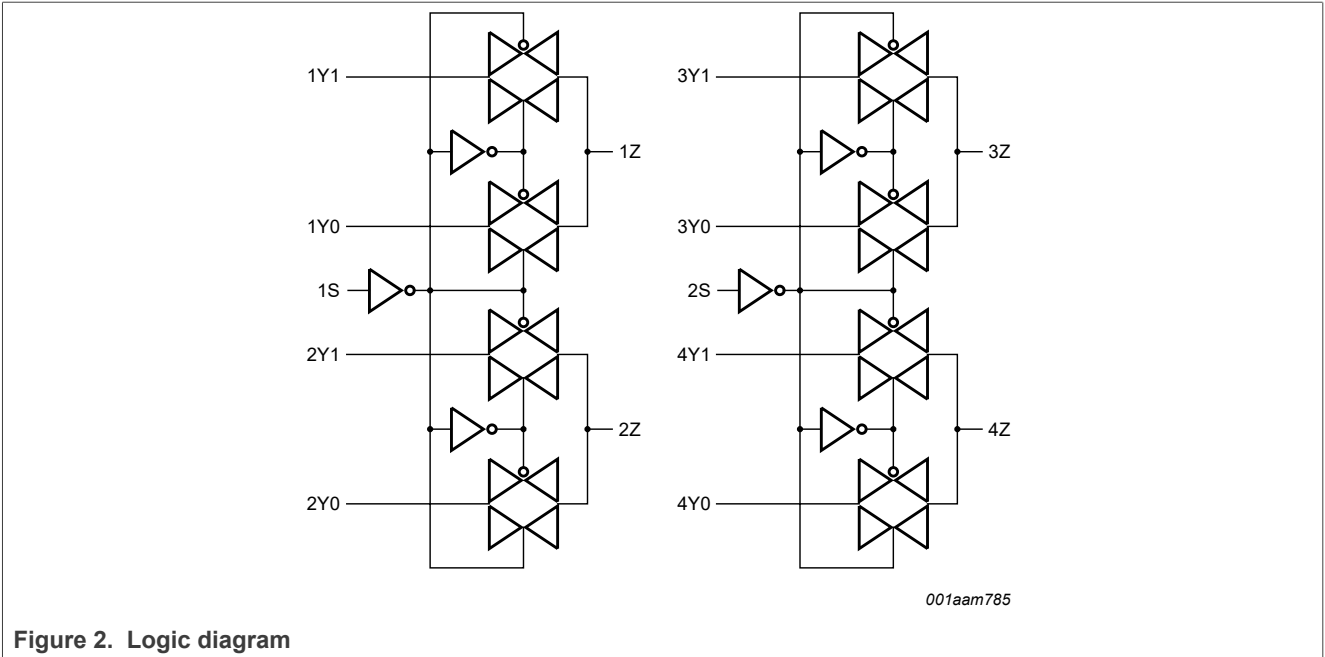


Figure 2. Logic diagram

6 Pinning information

6.1 Pinning

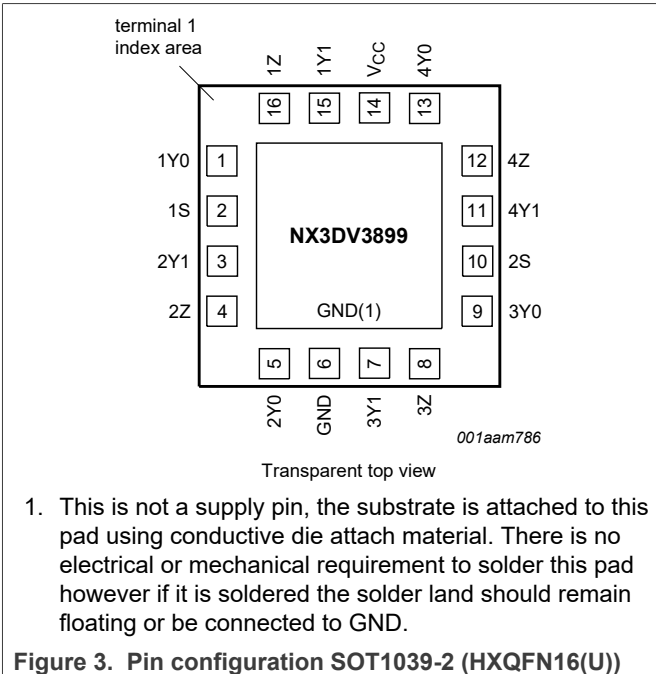


Figure 3. Pin configuration SOT1039-2 (HXQFN16(U))

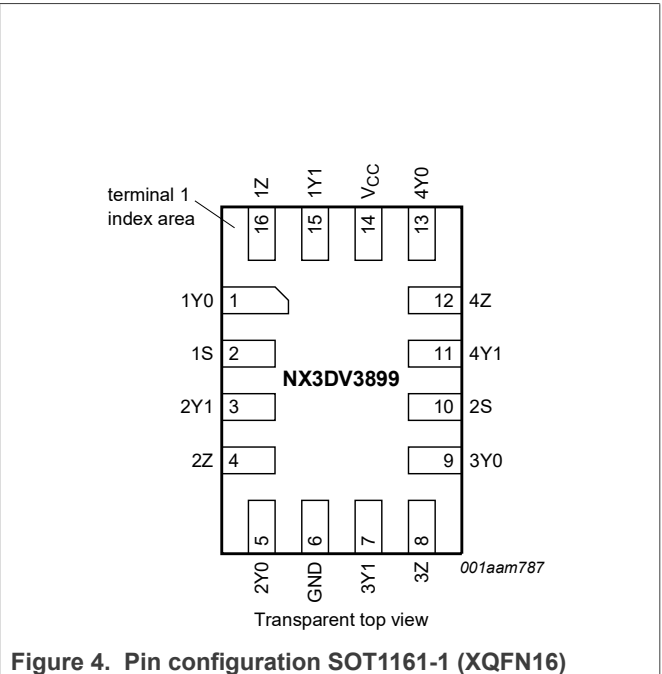


Figure 4. Pin configuration SOT1161-1 (XQFN16)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1Y0, 2Y0, 3Y0, 4Y0	1, 5, 9, 13	independent input or output
1S, 2S	2, 10	select input
1Y1, 2Y1, 3Y1, 4Y1	15, 3, 7, 11	independent input or output
1Z, 2Z, 3Z, 4Z	16, 4, 8, 12	common output or input
GND	6	ground (0 V)
V _{CC}	14	supply voltage

7 Functional description

Table 4. Function table^[1]

Input nS	Channel on
L	nY0
H	nY1

[1] H = HIGH voltage level; L = LOW voltage level.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	select input nS	^[1] -0.5	+4.6	V
V _{SW}	switch voltage		^[2] -0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±50	mA
I _{SW}	switch current	V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; source or sink current	-	±350	mA
		V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±500	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		HXQFN16(U)	^[3] -	250	mW
		XQFN16	^[4] -	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.

[3] For HXQFN16(U) package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.

[4] For XQFN16 package: above 133 °C the value of P_{tot} derates linearly with 14.5 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.4	4.3	V
V_I	input voltage	select input nS	0	4.3	V
V_{SW}	switch voltage		^[1] 0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.4\text{ V to }4.3\text{ V}$	^[2] -	200	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

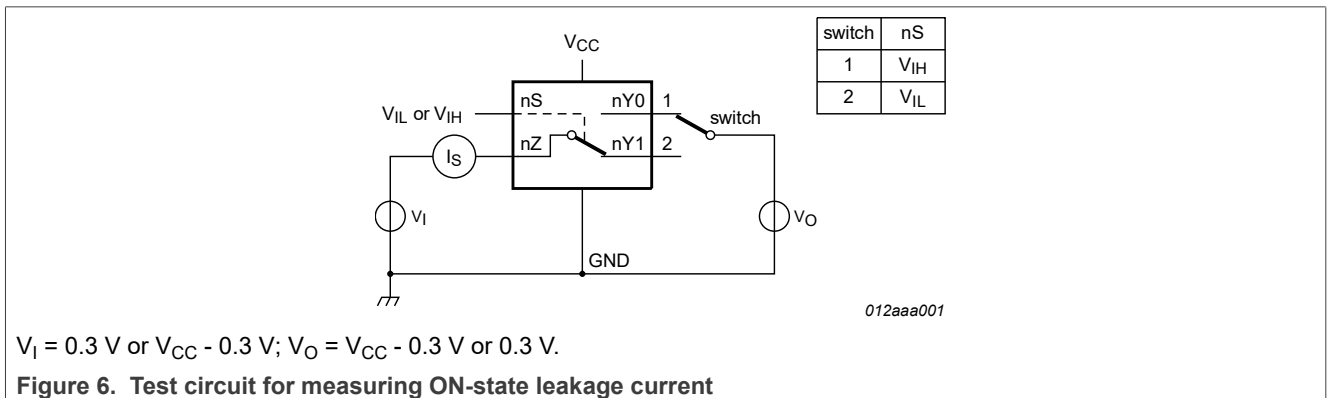
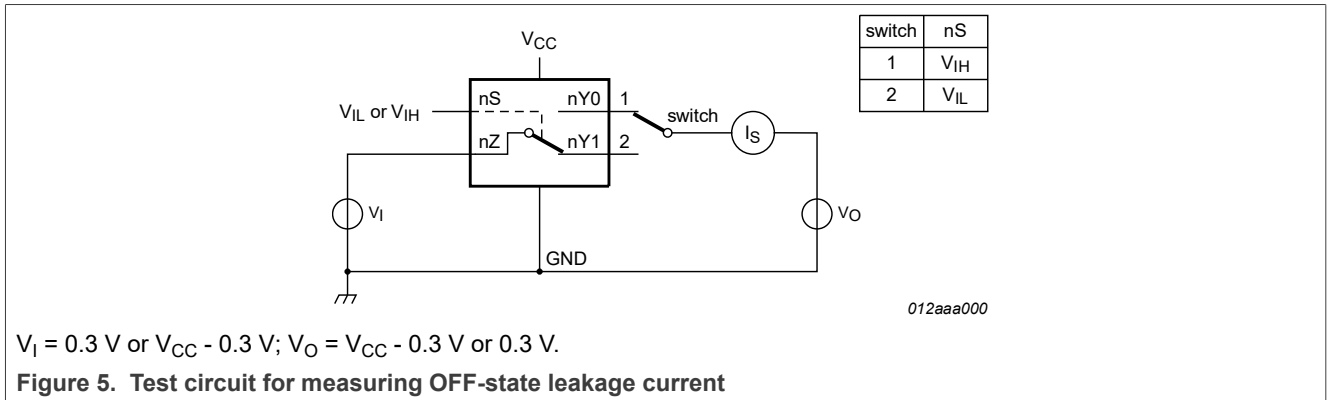
Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	0.9	-	-	0.9	-	-	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	0.9	-	-	0.9	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.1	-	-	1.1	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	1.3	-	-	1.3	-	-	V
		$V_{CC} = 3.6\text{ V to }4.3\text{ V}$	1.4	-	-	1.4	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	-	-	0.3	-	0.3	0.3	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	0.4	-	0.4	0.3	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.4	-	0.4	0.4	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.5	-	0.5	0.5	V
		$V_{CC} = 3.6\text{ V to }4.3\text{ V}$	-	-	0.6	-	0.6	0.6	V
I_I	input leakage current	select input nS; $V_I = \text{GND to }4.3\text{ V}$; $V_{CC} = 1.4\text{ V to }4.3\text{ V}$	-	-	-	-	± 0.5	± 1	μA
$I_{S(OFF)}$	OFF-state leakage current	nY0 and nY1 port; see Figure 5							
		$V_{CC} = 1.4\text{ V to }4.3\text{ V}$	-	-	± 5	-	± 50	± 500	nA
$I_{S(ON)}$	ON-state leakage current	nZ port; see Figure 6							
		$V_{CC} = 1.4\text{ V to }4.3\text{ V}$	-	-	± 5	-	± 50	± 500	nA
I_{CC}	supply current	$V_I = V_{CC}\text{ or GND}$; $V_{SW} = \text{GND or }V_{CC}$							
		$V_{CC} = 3.6\text{ V}$	-	-	100	-	500	5000	nA

Table 7. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
		V _{CC} = 4.3 V	-	-	150	-	800	6000	nA
ΔI _{CC}	additional supply current	V _{SW} = GND or V _{CC}							
		V _I = 2.6 V; V _{CC} = 4.3 V	-	2.0	4.0	-	7	7	μA
		V _I = 2.6 V; V _{CC} = 3.6 V	-	0.35	0.7	-	1	1	μA
		V _I = 1.8 V; V _{CC} = 4.3 V	-	7.0	10.0	-	15	15	μA
		V _I = 1.8 V; V _{CC} = 3.6 V	-	2.5	4.0	-	5	5	μA
		V _I = 1.8 V; V _{CC} = 2.5 V	-	50	200	-	300	500	nA
C _I	input capacitance		-	1.0	-	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	8	-	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	30	-	-	-	-	pF

10.1 Test circuits



10.2 ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 8](#) to [Figure 14](#).

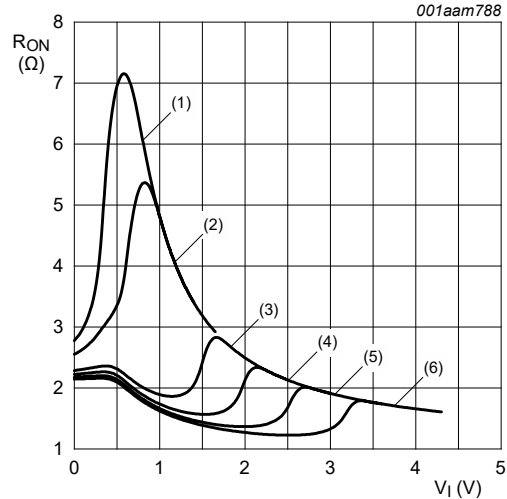
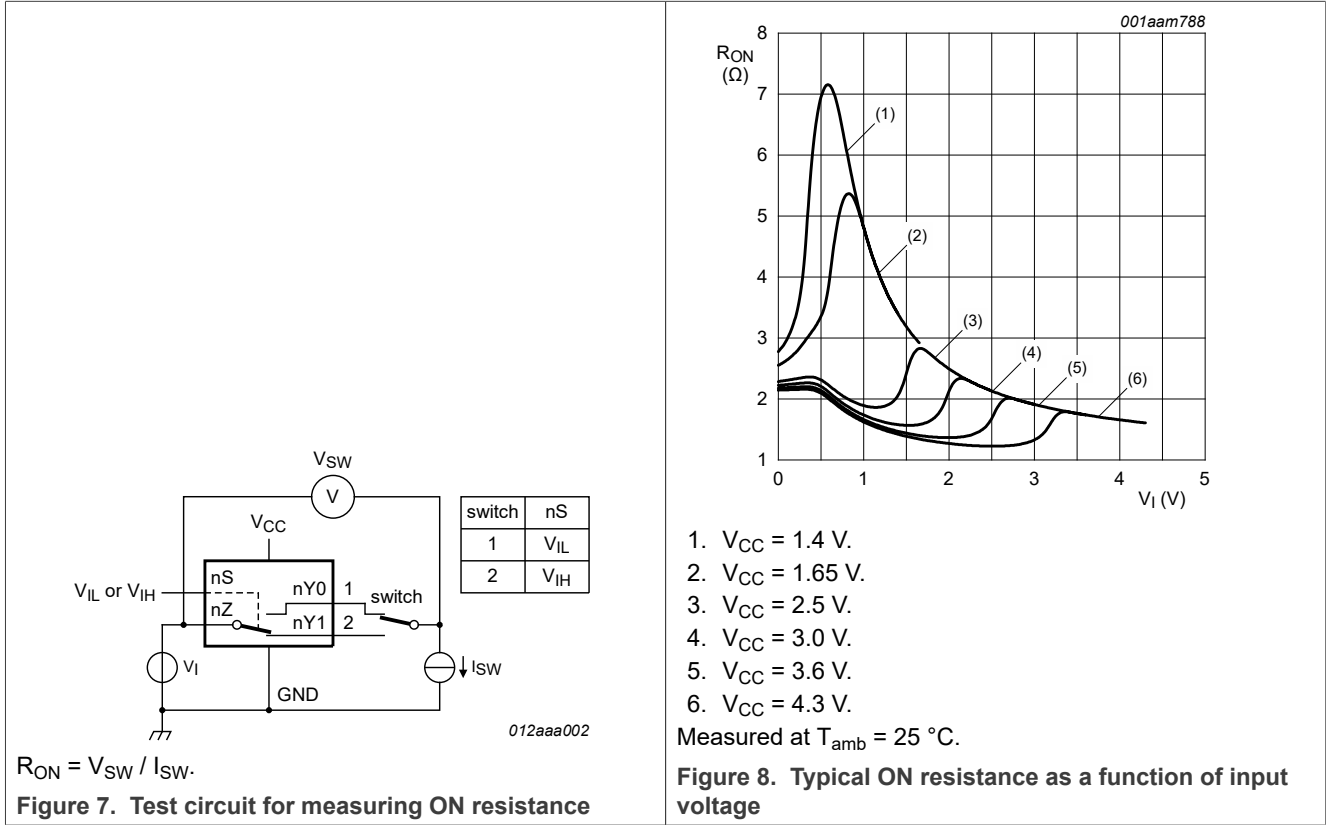
Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; I _{SW} = 100 mA; see Figure 7						
		V _{CC} = 1.4 V	-	7.2	9.3	-	10	Ω
		V _{CC} = 1.65 V	-	5.4	7.3	-	8	Ω
		V _{CC} = 2.5 V	-	2.9	3.9	-	4.5	Ω
		V _{CC} = 3.0 V	-	2.4	3.4	-	4.5	Ω
		V _{CC} = 3.6 V	-	2.3	3.3	-	4.2	Ω
		V _{CC} = 4.3 V	-	2.2	3.3	-	4.2	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = GND to V _{CC} ; I _{SW} = 100 mA ^[2]						
		V _{CC} = 3.0 V	-	0.8	-	-	-	Ω
		V _{CC} = 4.3 V	-	0.7	-	-	-	Ω
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} ; I _{SW} = 100 mA ^[3]						
		V _{CC} = 1.4 V	-	4.4	-	-	-	Ω
		V _{CC} = 1.65 V	-	2.8	-	-	-	Ω
		V _{CC} = 2.5 V	-	1.0	-	-	-	Ω
		V _{CC} = 3.0 V	-	0.8	-	-	-	Ω
		V _{CC} = 3.6 V	-	0.9	-	-	-	Ω
		V _{CC} = 4.3 V	-	1.0	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

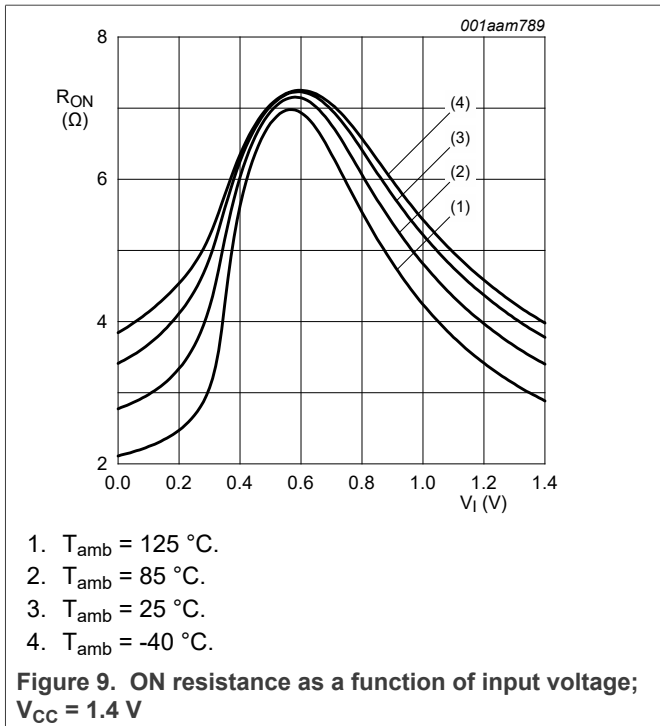
[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs



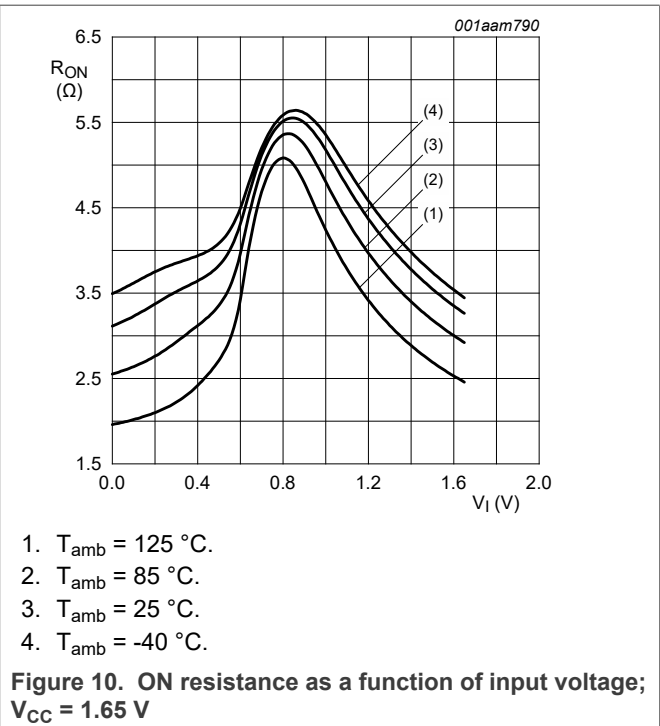
1. V_{CC} = 1.4 V.
 2. V_{CC} = 1.65 V.
 3. V_{CC} = 2.5 V.
 4. V_{CC} = 3.0 V.
 5. V_{CC} = 3.6 V.
 6. V_{CC} = 4.3 V.
- Measured at T_{amb} = 25 °C.

Figure 8. Typical ON resistance as a function of input voltage



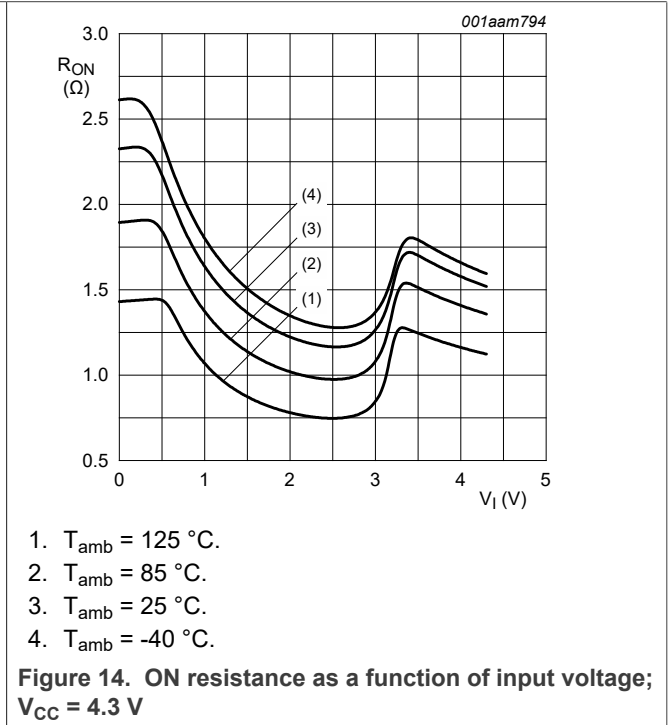
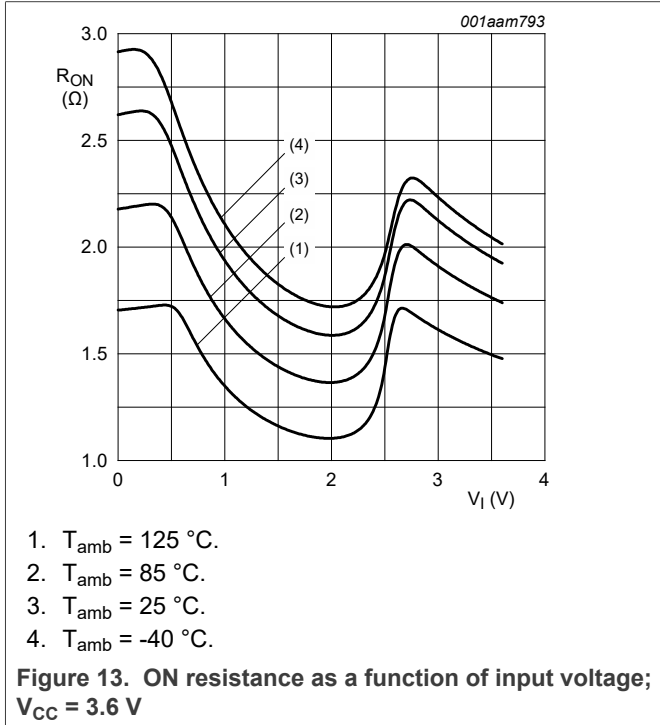
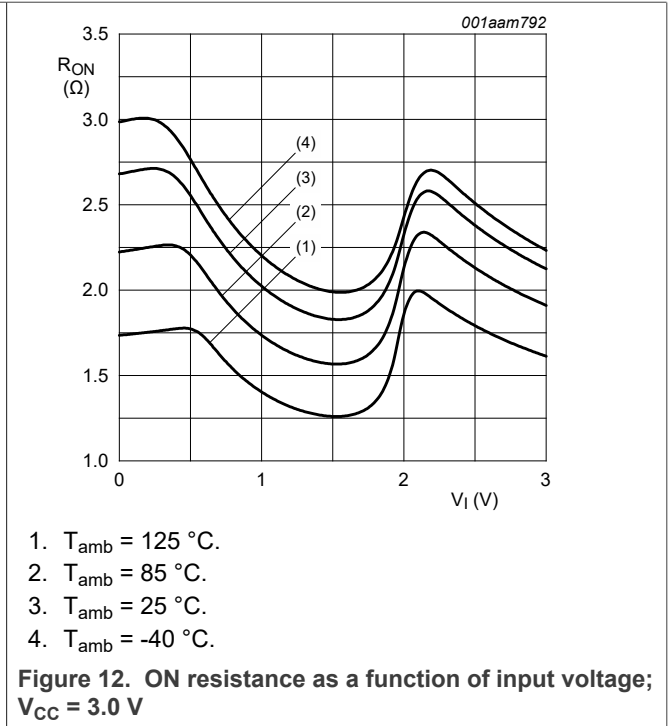
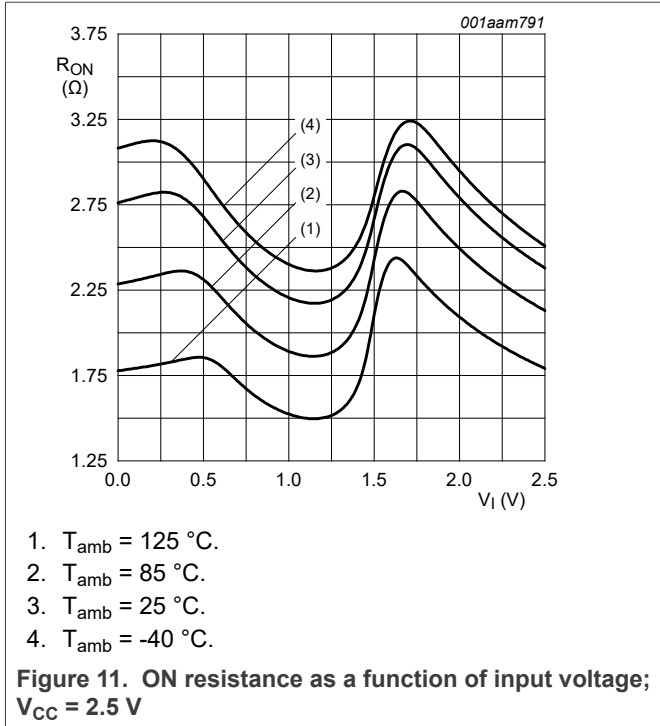
1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 9. ON resistance as a function of input voltage; V_{CC} = 1.4 V



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 10. ON resistance as a function of input voltage; V_{CC} = 1.65 V



11 Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 17](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{en}	enable time	nS to nZ or nYn; see Figure 15							
		V _{CC} = 1.4 V to 1.6 V	-	41	90	-	120	120	ns
		V _{CC} = 1.65 V to 1.95 V	-	30	70	-	80	90	ns
		V _{CC} = 2.3 V to 2.7 V	-	20	45	-	50	55	ns
		V _{CC} = 2.7 V to 3.6 V	-	19	40	-	45	50	ns
		V _{CC} = 3.6 V to 4.3 V	-	19	40	-	45	50	ns
t _{dis}	disable time	nS to nZ or nYn; see Figure 15							
		V _{CC} = 1.4 V to 1.6 V	-	24	70	-	80	90	ns
		V _{CC} = 1.65 V to 1.95 V	-	15	55	-	60	65	ns
		V _{CC} = 2.3 V to 2.7 V	-	9	25	-	30	35	ns
		V _{CC} = 2.7 V to 3.6 V	-	8	20	-	25	30	ns
		V _{CC} = 3.6 V to 4.3 V	-	8	20	-	25	30	ns
t _{b-m}	break-before-make time	see Figure 16	[2]						
		V _{CC} = 1.4 V to 1.6 V	-	20	-	9	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	17	-	7	-	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	13	-	4	-	-	ns
		V _{CC} = 2.7 V to 3.6 V	-	11	-	3	-	-	ns
		V _{CC} = 3.6 V to 4.3 V	-	11	-	2	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

11.1 Waveform and test circuits

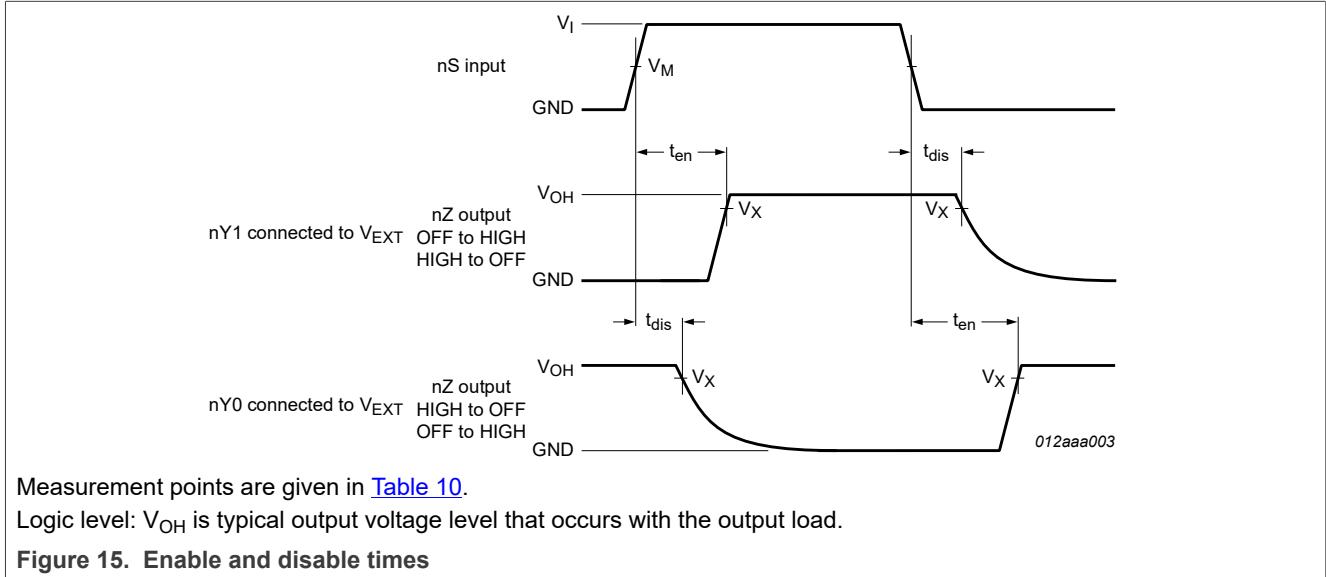


Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

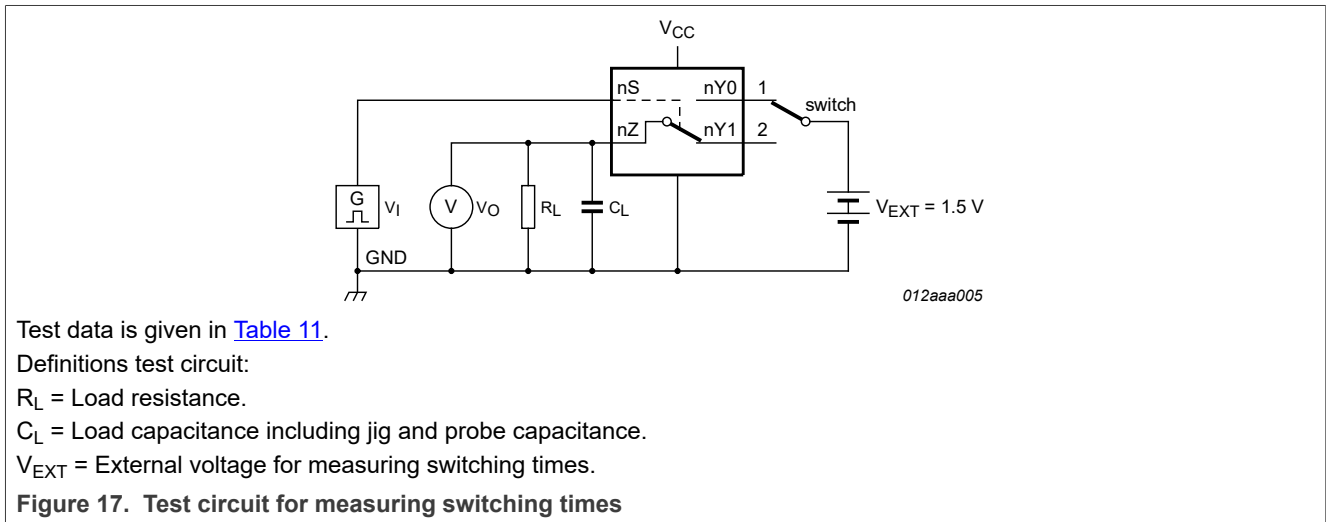
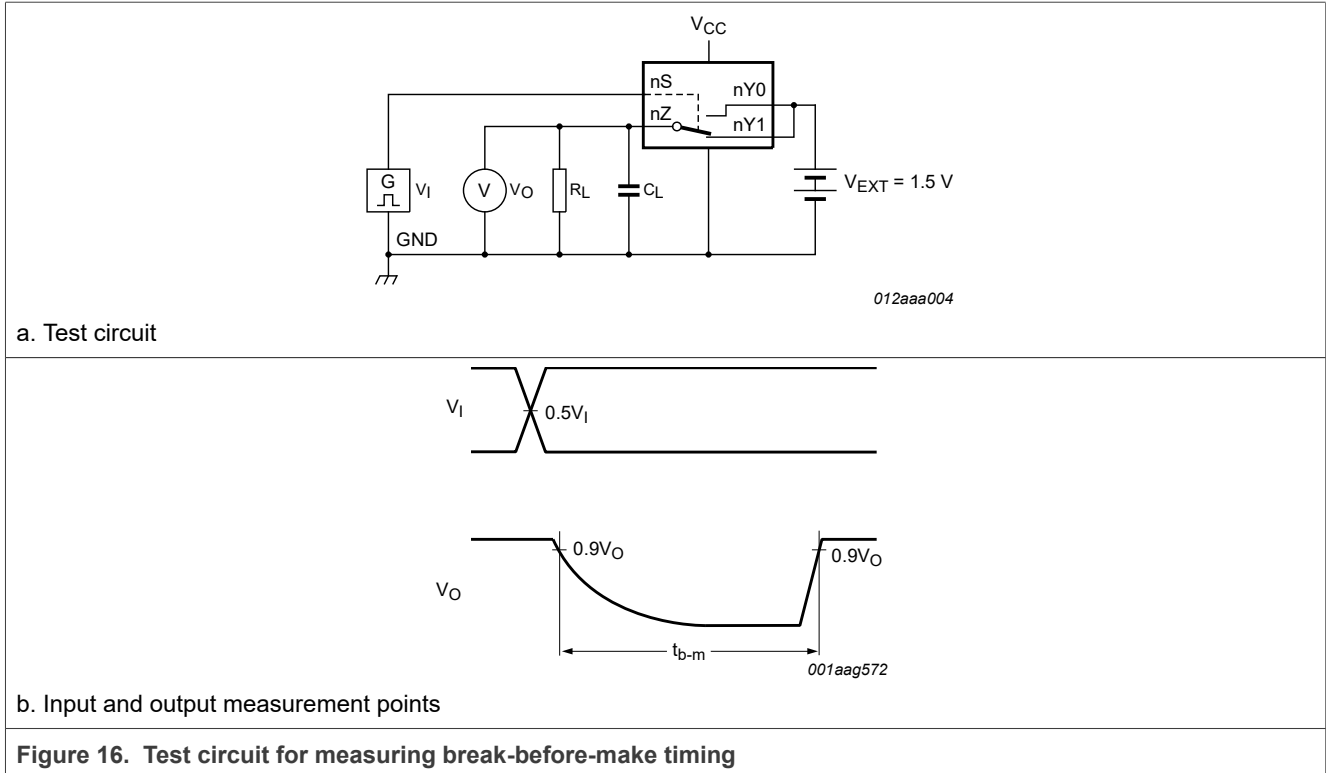


Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = GND$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
THD	total harmonic distortion	$f_i = 20$ Hz to 20 kHz; $R_L = 600$ Ω; see Figure 18	[1]				
		$V_{CC} = 1.4$ V; $V_I = 1$ V (p-p)		-	0.05	-	%
		$V_{CC} = 1.65$ V; $V_I = 1.2$ V (p-p)		-	0.02	-	%
		$V_{CC} = 2.3$ V; $V_I = 1.5$ V (p-p)		-	0.01	-	%
		$V_{CC} = 2.7$ V; $V_I = 2$ V (p-p)		-	0.01	-	%
		$V_{CC} = 3.6$ V; $V_I = 2$ V (p-p)		-	0.01	-	%
		$V_{CC} = 4.3$ V; $V_I = 2$ V (p-p)		-	0.01	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50$ Ω; see Figure 19	[1]				
		$V_{CC} = 1.4$ V to 4.3 V		-	200	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 1$ MHz; $R_L = 50$ Ω; see Figure 20	[1]				
		$V_{CC} = 1.4$ V to 4.3 V		-	-70	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1$ MHz; $C_L = 50$ pF; $R_L = 50$ Ω; see Figure 21					
		$V_{CC} = 1.4$ V to 3.6 V		-	210	-	V
		$V_{CC} = 3.6$ V to 4.3 V		-	300	-	V
Xtalk	crosstalk	between switches; $f_i = 1$ MHz; $R_L = 50$ Ω; see Figure 22	[1]				
		$V_{CC} = 1.4$ V to 4.3 V		-	-90	-	dB
Q_{inj}	charge injection	$f_i = 1$ MHz; $C_L = 0.1$ nF; $R_L = 1$ MΩ; $V_{gen} = 0$ V; $R_{gen} = 0$ Ω; see Figure 23					
		$V_{CC} = 1.4$ V		-	0.5	-	pC
		$V_{CC} = 1.65$ V		-	0.7	-	pC
		$V_{CC} = 2.5$ V		-	1.6	-	pC
		$V_{CC} = 3.0$ V		-	2.1	-	pC
		$V_{CC} = 3.6$ V		-	2.9	-	pC
		$V_{CC} = 4.3$ V		-	4.0	-	pC

[1] f_i is biased at $0.5V_{CC}$.

11.3 Test circuits

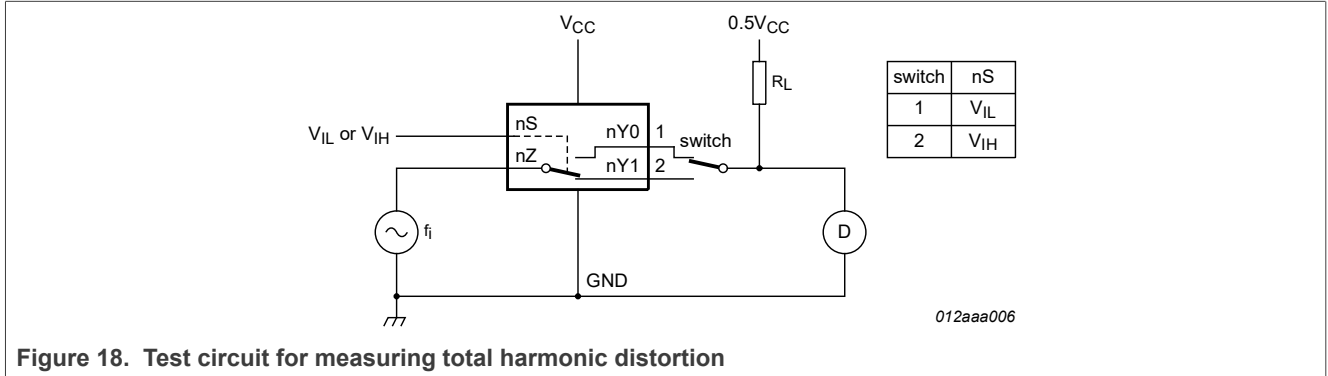


Figure 18. Test circuit for measuring total harmonic distortion

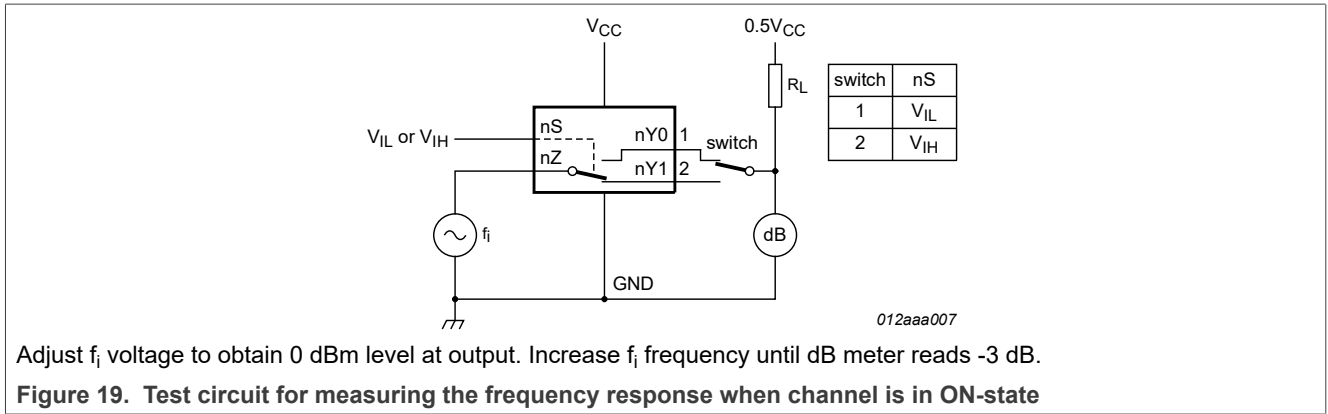


Figure 19. Test circuit for measuring the frequency response when channel is in ON-state

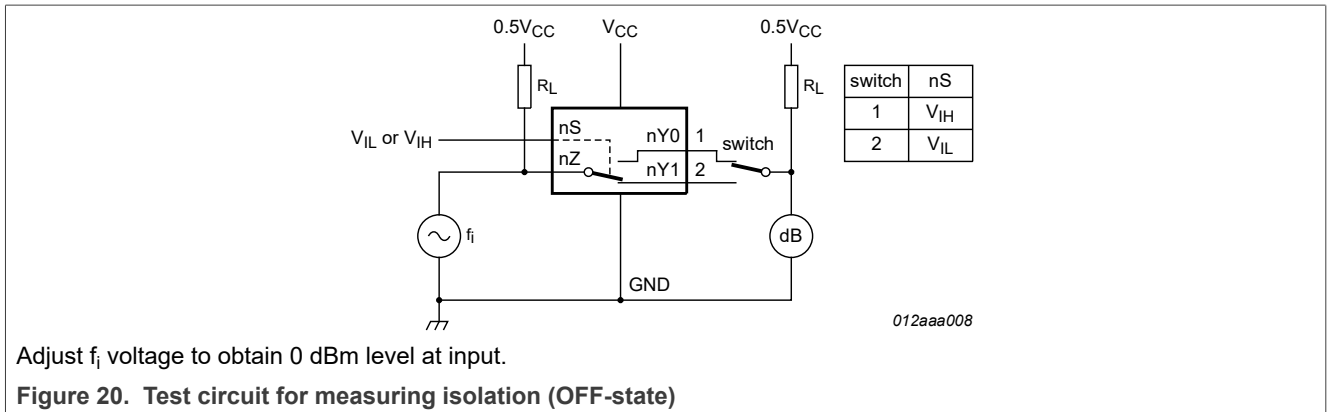


Figure 20. Test circuit for measuring isolation (OFF-state)

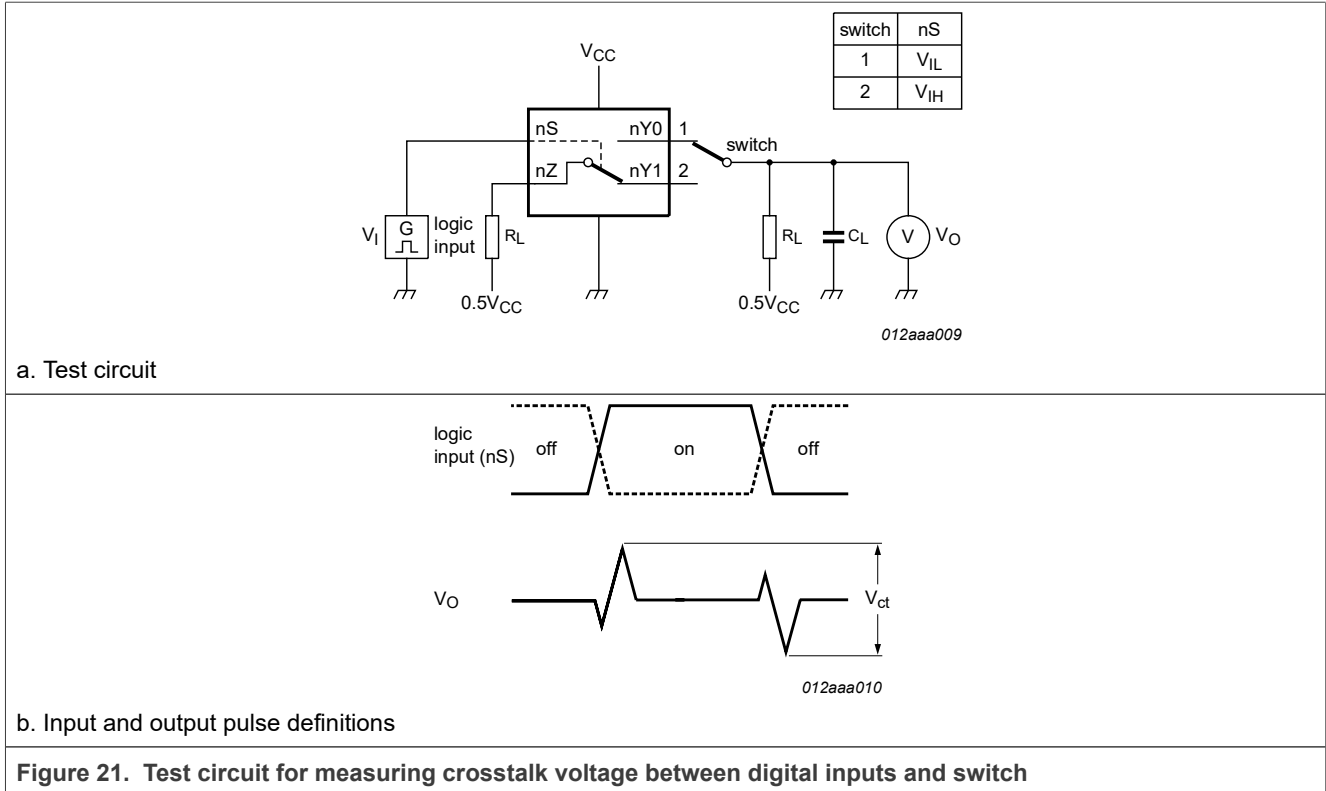
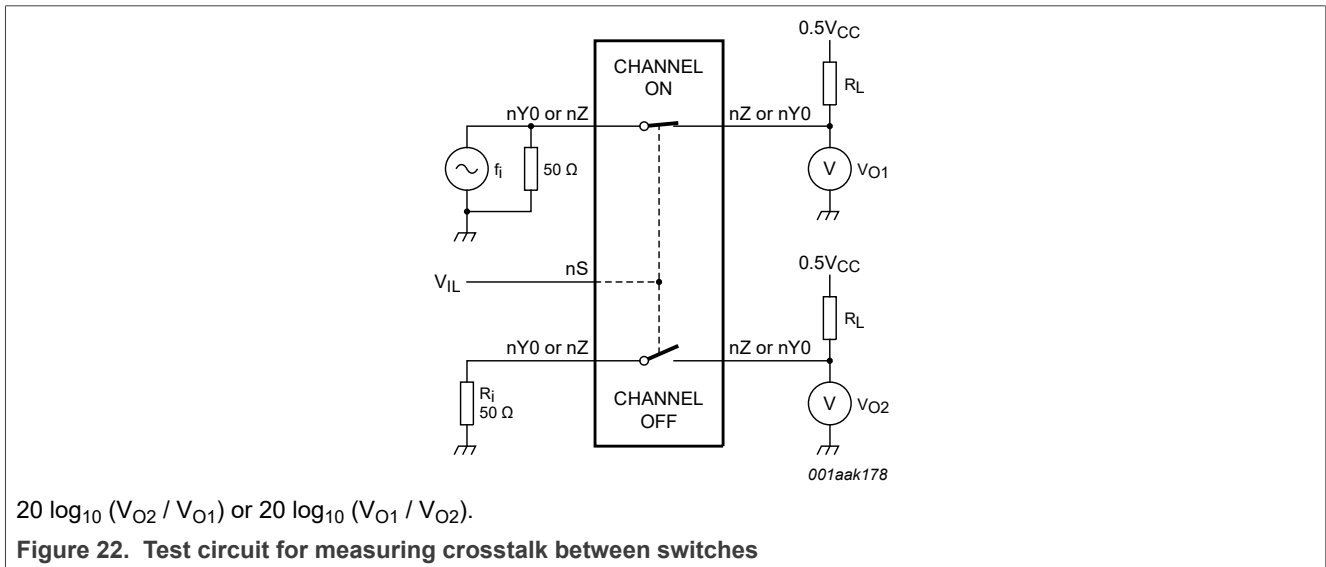
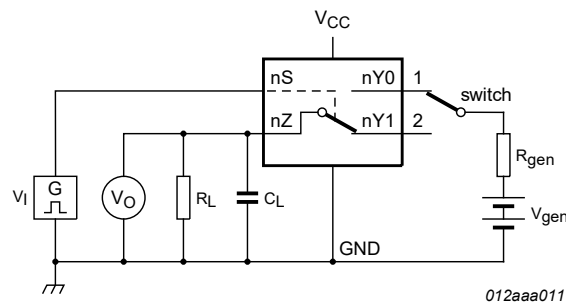
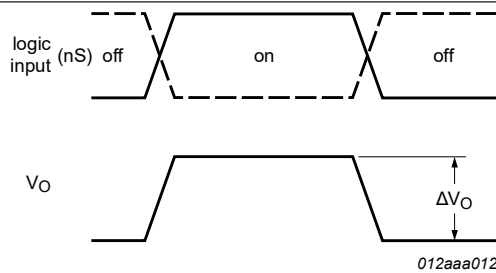


Figure 21. Test circuit for measuring crosstalk voltage between digital inputs and switch





a. Test circuit



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Figure 23. Test circuit for measuring charge injection

12 Package outline

HXQFN16(U): plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.5 mm

SOT1039-2

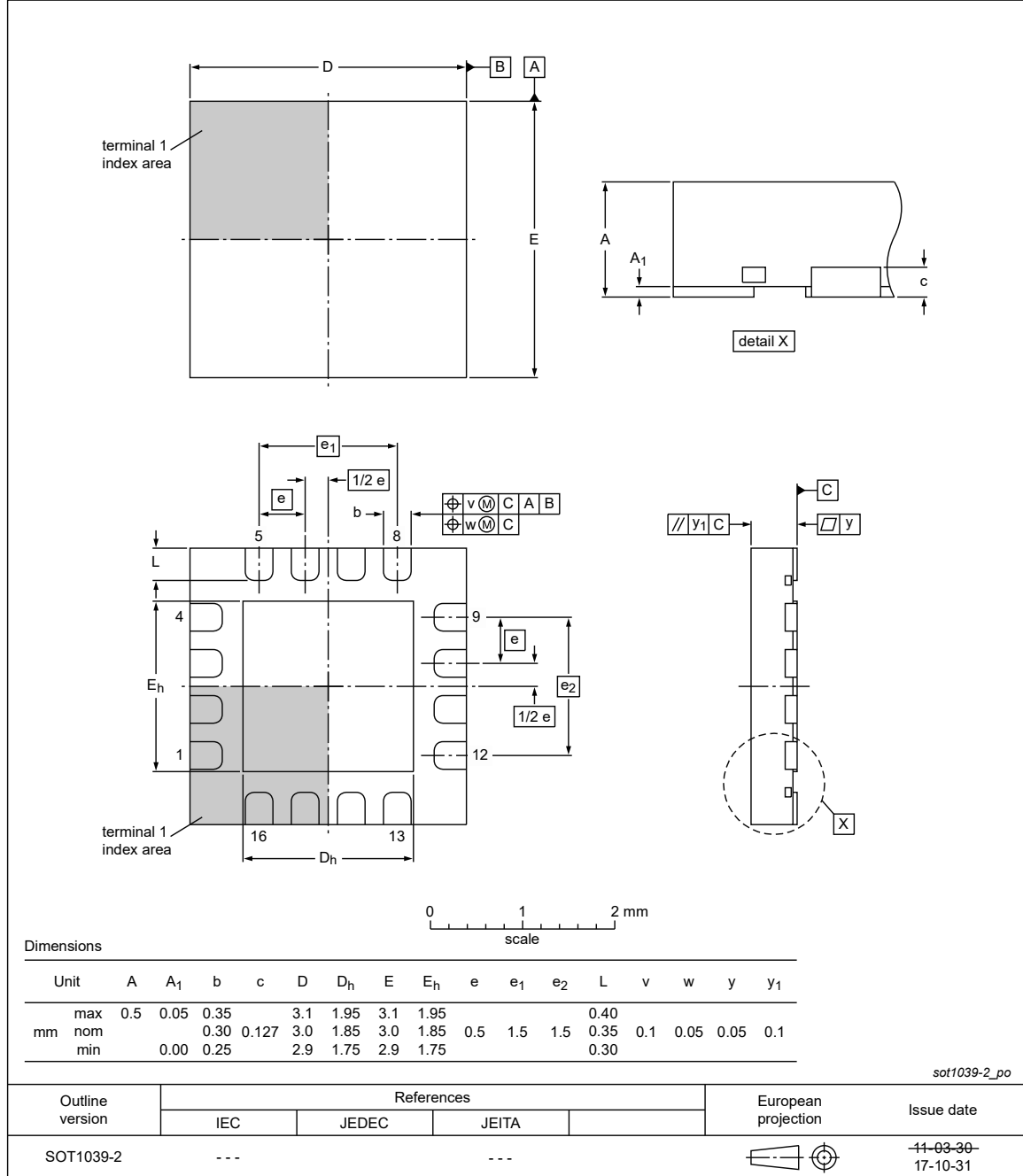
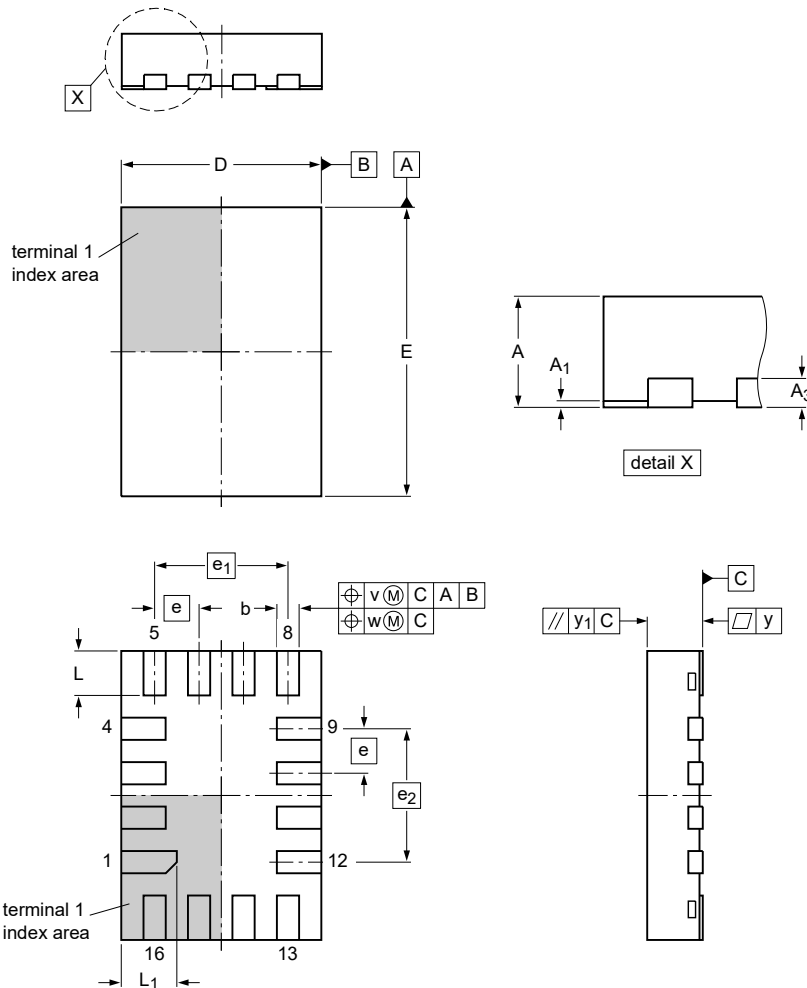


Figure 24. Package outline SOT1039-2 (HXQFN16(U))

XQFN16: plastic, extremely thin quad flat package; no leads;
16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1



Dimensions

Unit ⁽¹⁾	A	A ₁	A ₃	b	D	E	e	e ₁	e ₂	L	L ₁	v	w	y	y ₁
max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
mm nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
min		0.00		0.15	1.7	2.5				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	---	---	---			-09-12-28- 09-12-29

Figure 25. Package outline SOT1161-1 (XQFN16)

13 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

14 Revision history

Table 14. Revision history

Document ID	Release date	Description
NX3DV3899 v.3.2	21 June 2024	Updated per CIN 202405025I: <ul style="list-style-type: none">• Corrected package outline from SOT1039-1 to SOT1039-2.
NX3DV3899 v.3.1	25 June 2021	Updated Section 4.
NX3DV3899 v.3	9 November 2011	Product data sheet; v.3
NX3DV3899 v.2	23 November 2010	Product data sheet; v.2
NX3DV3899 v.1	21 October 2010	Product data sheet; v.1

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	2	Tab. 8.	ON resistance	7
Tab. 2.	Ordering options	2	Tab. 9.	Dynamic characteristics	10
Tab. 3.	Pin description	4	Tab. 10.	Measurement points	11
Tab. 4.	Function table	4	Tab. 11.	Test data	12
Tab. 5.	Limiting values	4	Tab. 12.	Additional dynamic characteristics	13
Tab. 6.	Recommended operating conditions	5	Tab. 13.	Abbreviations	19
Tab. 7.	Static characteristics	5	Tab. 14.	Revision history	19

Figures

Fig. 1.	Logic symbol	2	Fig. 14.	ON resistance as a function of input voltage; VCC = 4.3 V	9
Fig. 2.	Logic diagram	3	Fig. 15.	Enable and disable times	11
Fig. 3.	Pin configuration SOT1039-2 (HXQFN16(U))	3	Fig. 16.	Test circuit for measuring break-before-make timing	12
Fig. 4.	Pin configuration SOT1161-1 (XQFN16)	3	Fig. 17.	Test circuit for measuring switching times	12
Fig. 5.	Test circuit for measuring OFF-state leakage current	6	Fig. 18.	Test circuit for measuring total harmonic distortion	14
Fig. 6.	Test circuit for measuring ON-state leakage current	6	Fig. 19.	Test circuit for measuring the frequency response when channel is in ON-state	14
Fig. 7.	Test circuit for measuring ON resistance	8	Fig. 20.	Test circuit for measuring isolation (OFF-state)	14
Fig. 8.	Typical ON resistance as a function of input voltage	8	Fig. 21.	Test circuit for measuring crosstalk voltage between digital inputs and switch	15
Fig. 9.	ON resistance as a function of input voltage; VCC = 1.4 V	8	Fig. 22.	Test circuit for measuring crosstalk between switches	15
Fig. 10.	ON resistance as a function of input voltage; VCC = 1.65 V	8	Fig. 23.	Test circuit for measuring charge injection	16
Fig. 11.	ON resistance as a function of input voltage; VCC = 2.5 V	9	Fig. 24.	Package outline SOT1039-2 (HXQFN16(U))	17
Fig. 12.	ON resistance as a function of input voltage; VCC = 3.0 V	9	Fig. 25.	Package outline SOT1161-1 (XQFN16)	18
Fig. 13.	ON resistance as a function of input voltage; VCC = 3.6 V	9			



Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	4
8	Limiting values	4
9	Recommended operating conditions	5
10	Static characteristics	5
10.1	Test circuits	6
10.2	ON resistance	7
10.3	ON resistance test circuit and graphs	8
11	Dynamic characteristics	10
11.1	Waveform and test circuits	11
11.2	Additional dynamic characteristics	13
11.3	Test circuits	14
12	Package outline	17
13	Abbreviations	19
14	Revision history	19
	Legal information	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View NX3DV3899HRZ on WIN SOURCE](#)
-  [NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management