



THE DATASHEET OF CDC208DW

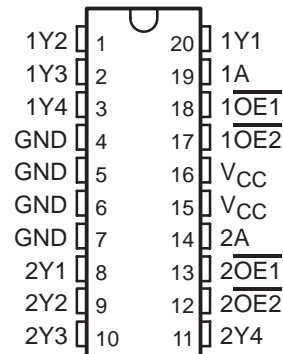


CDC208 DUAL 1-LINE TO 4-LINE CLOCK DRIVER WITH 3-STATE OUTPUTS

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- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW)

DW PACKAGE
(TOP VIEW)



description

The CDC208 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC208 is characterized for operation from -40°C to 85°C .

FUNCTION TABLES

| INPUTS | | | OUTPUTS | | | |
|-------------------|-------------------|----|---------|-----|-----|-----|
| $\overline{1OE1}$ | $\overline{1OE2}$ | 1A | 1Y1 | 1Y2 | 1Y3 | 1Y4 |
| L | L | L | L | L | L | L |
| L | L | H | H | H | H | H |
| L | H | X | L | L | L | L |
| H | L | X | H | H | H | H |
| H | H | X | Z | Z | Z | Z |

| INPUTS | | | OUTPUTS | | | |
|-------------------|-------------------|----|---------|-----|-----|-----|
| $\overline{2OE1}$ | $\overline{2OE2}$ | 2A | 2Y1 | 2Y2 | 2Y3 | 2Y4 |
| L | L | L | L | L | L | L |
| L | L | H | H | H | H | H |
| L | H | X | L | L | L | L |
| H | L | X | H | H | H | H |
| H | H | X | Z | Z | Z | Z |



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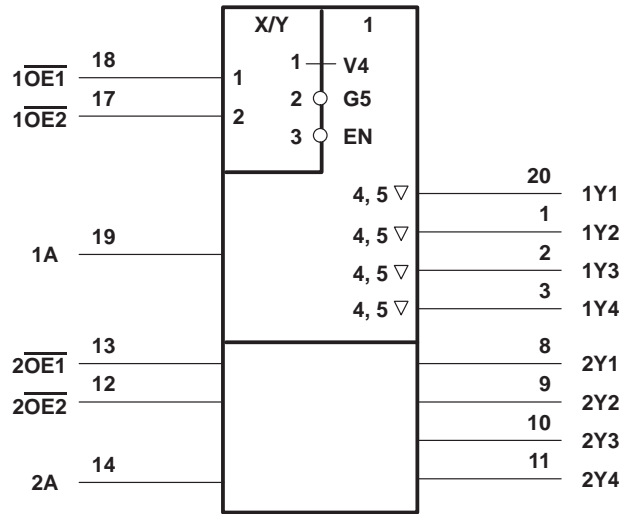
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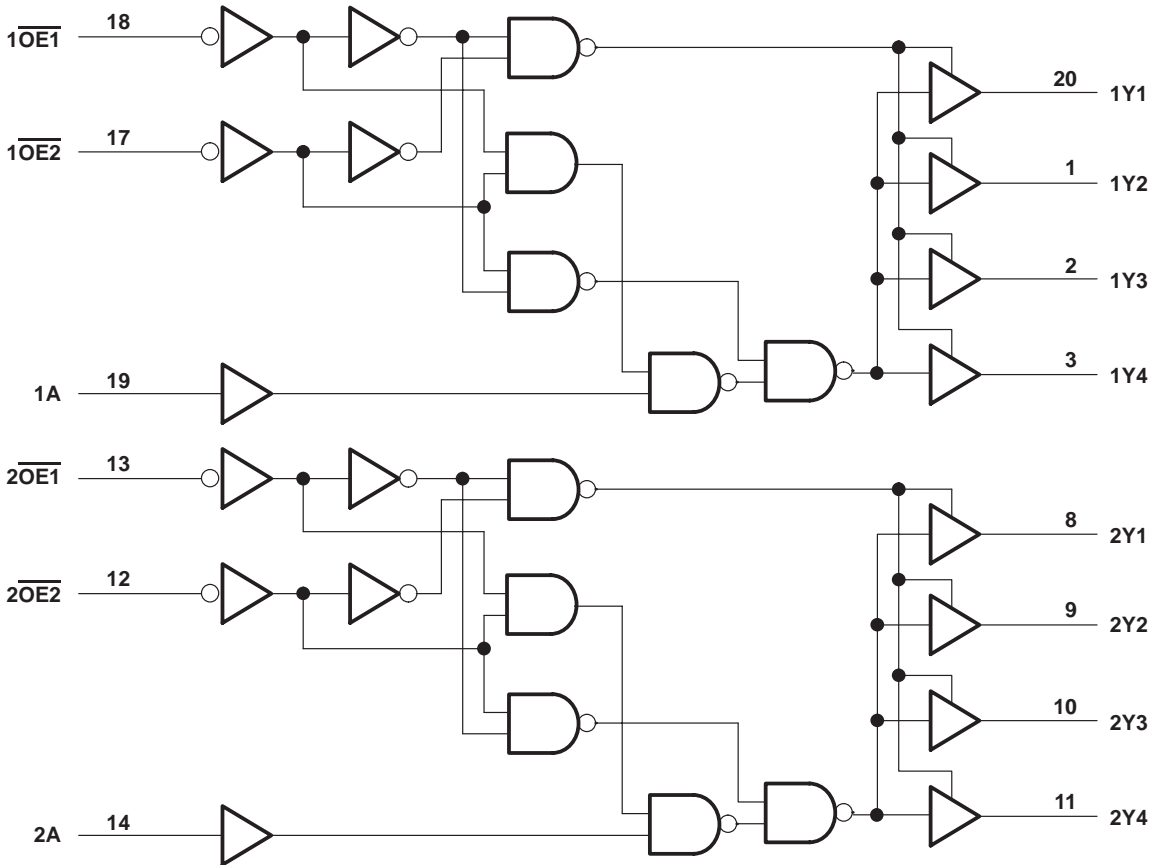
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±200 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2) | 1.6 W |
| Storage temperature range | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------------|------------------------------------|-----|----------|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | | V |
| I_{OH} | High-level output current | | | –24 | mA |
| I_{OL} | Low-level output current | | | 24 | mA |
| $\Delta t / \Delta v$ | Input transition rise or fall rate | 0 | | 10 | ns/V |
| f_{clock} | Input clock frequency | | | 60 | MHz |
| T_A | Operating free-air temperature | –40 | | 85 | °C |



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------------|---|---|-----------------------|-----|-----|------|------|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | |
| | I _{OH} = -75 mA† | 5.5 V | | | | 3.85 | | |
| | V _{OL} | I _{OL} = 50 μA | 4.5 V | | | | 0.1 | |
| 5.5 V | | | | | | 0.1 | | |
| I _{OL} = 24 mA | | 4.5 V | | | | 0.36 | | |
| | | 5.5 V | | | | 0.36 | | |
| I _{OL} = 75 mA† | | 5.5 V | | | | 1.65 | | |
| I _I | | V _I = V _{CC} or GND | 5.5 V | | | | ±0.1 | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | | ±0.5 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | | 8 | | μA |
| ΔI _{CC} ‡ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | | 0.9 | | mA |
| C _i | V _I = V _{CC} or GND | 5 V | | | | 4 | | pF |
| C _o | V _O = V _{CC} or GND | 5 V | | | | 10 | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | MIN | MAX | UNIT |
|-----------|---|-------------|--------------------------|-----|------|-----|------|------|
| | | | MIN | TYP | MAX | | | |
| t_{PLH} | 1A and 2A | Any Y | 5.3 | 8.5 | 10.9 | 5.3 | 11.7 | ns |
| t_{PHL} | | | 3.6 | 7.7 | 11 | 3.6 | 11.5 | |
| t_{PLH} | $\overline{1OE1}$, $\overline{1OE2}$, and $\overline{2OE1}$, $\overline{2OE2}$ | Any Y | 4.7 | 8.5 | 11.7 | 4.7 | 12.8 | ns |
| t_{PHL} | | | 4.4 | 8.4 | 11.3 | 4.4 | 12.4 | |
| t_{PZH} | $\overline{1OE2}$ or $\overline{2OE2}$ | Any Y | 4.4 | 8.1 | 11.3 | 4.4 | 12.4 | ns |
| t_{PZL} | $\overline{1OE1}$ or $\overline{2OE1}$ | | 5 | 9.6 | 13.3 | 5 | 14.9 | |
| t_{PHZ} | $\overline{1OE2}$ or $\overline{2OE2}$ | Any Y | 4.2 | 7.4 | 9.3 | 4.2 | 10.2 | ns |
| t_{PLZ} | $\overline{1OE1}$ or $\overline{2OE1}$ | | 5.4 | 7.5 | 9.2 | 5.4 | 9.9 | |

switching characteristics, $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$, $T_A = 25^\circ\text{C}$ to 70°C (see Note 3 and Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|-------------|--------------|-------------|-----|------|------|
| t_{PLH} | 1A and 2A | Any Y | 6.6 | 10.2 | ns |
| t_{PHL} | | | 6.6 | 9.8 | |
| $t_{sk(o)}$ | 1A and 2A | Any Y | | 1 | ns |

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

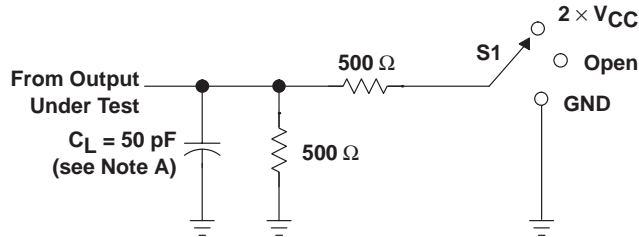
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|--|------------------|-----|------|
| C_{pd} | Power dissipation capacitance per bank | Outputs enabled | 96 | pF |
| | | Outputs disabled | 12 | |

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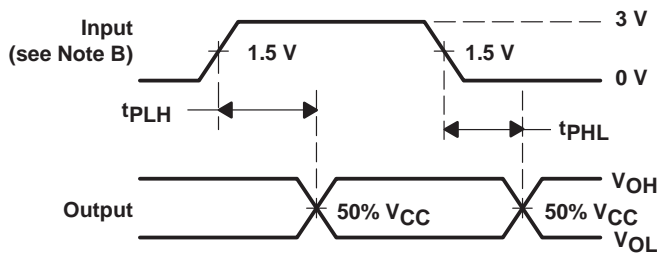
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PARAMETER MEASUREMENT INFORMATION

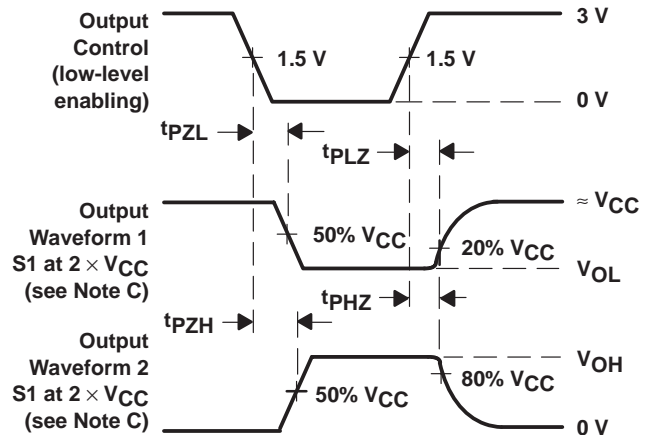


(see Note A) LOAD CIRCUIT FOR OUTPUTS

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

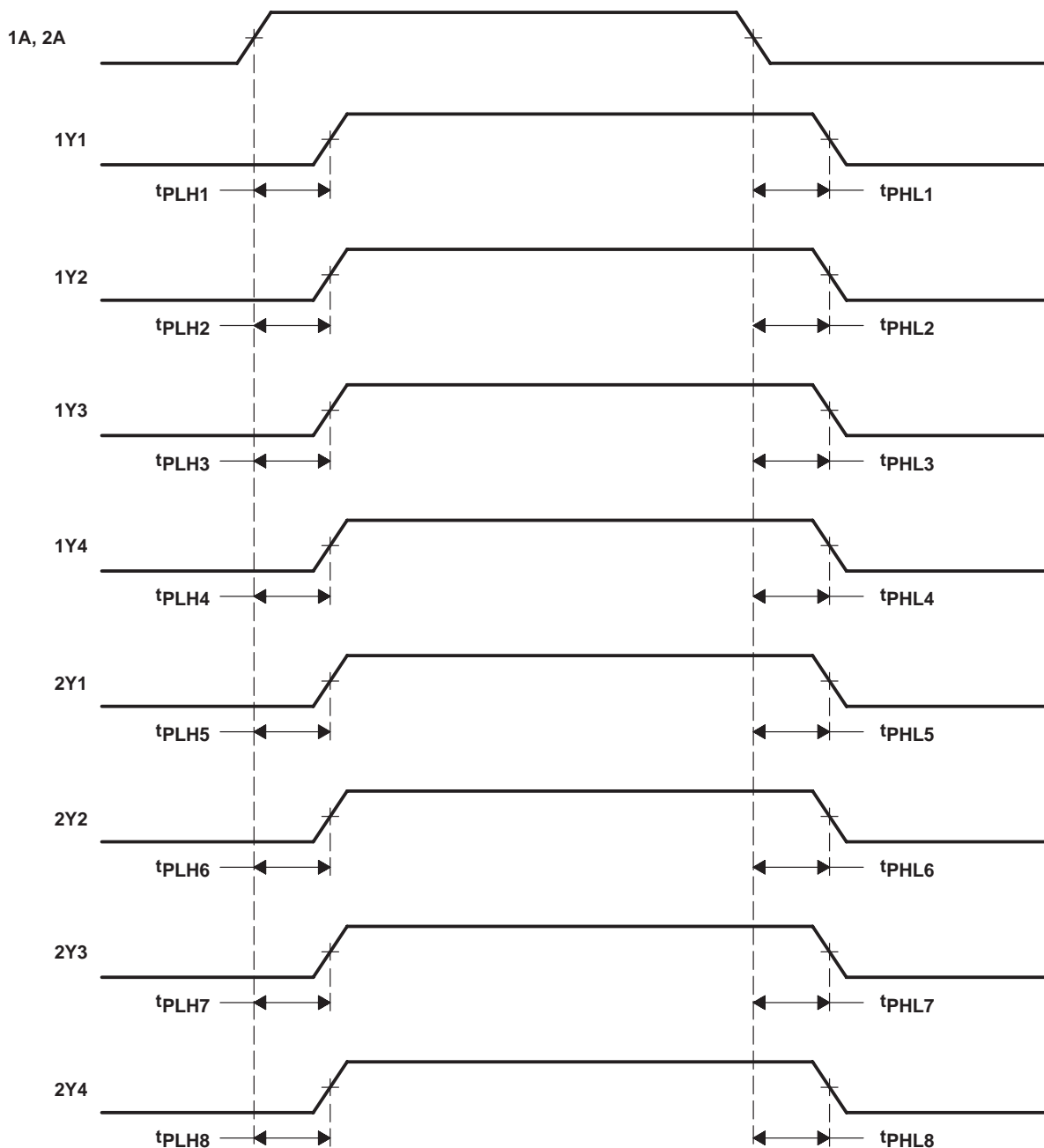


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns. For testing pulse duration: $t_r = t_f = 1$ to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 8$)
- The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, \dots, 8$)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDC208DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | CDC208 | Samples |
| CDC208DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | CDC208 | Samples |
| CDC208DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | CDC208 | Samples |
| CDC208NS | ACTIVE | SO | NS | 20 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC208 | Samples |
| CDC208NSG4 | ACTIVE | SO | NS | 20 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC208 | Samples |
| CDC208NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC208 | Samples |
| CDC208NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC208 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDC208DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CDC208NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDC208DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CDC208NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

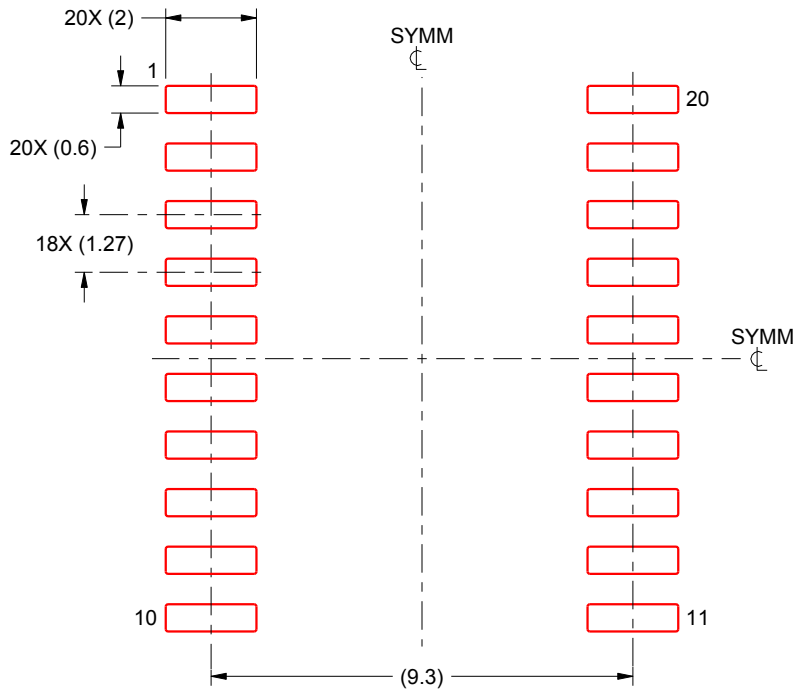
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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