



**THE DATASHEET OF  
CD74HC4024M96**



# CDx4HC4024, CDx4HCT4024 High-Speed CMOS Logic 7-Stage Binary Ripple Counter

## 1 Features

- Fully static operation
- Buffered inputs
- Common reset
- Negative edge clocking
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL Loads
  - Bus driver outputs: 15 LSTTL Loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V (max)}$ ,  $V_{IH} = 2\text{ V (min)}$
  - CMOS input compatibility,  $I_1 \leq 1\mu\text{A}$  at  $V_{OL}, V_{OH}$

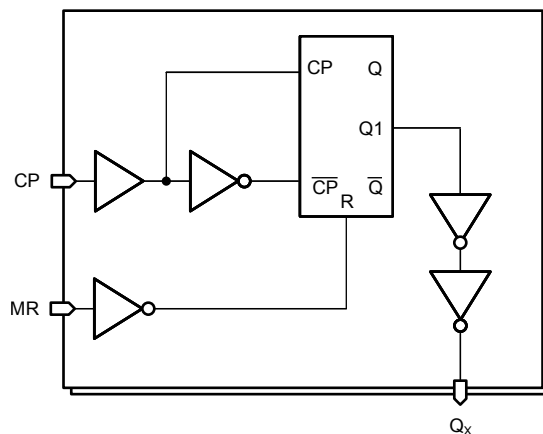
## 2 Description

The 'HC4024 and 'HCT4024 are 7-stage ripple-carry binary counters. All counter stages are flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD74HC4024M	SOIC (14)	8.65 mm × 3.90 mm
CD74HCT4024M	SOIC (14)	8.65 mm × 3.90 mm
CD74HC4024E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT4024E	PDIP (14)	19.31 mm × 6.35 mm
CD74HC4024PW	TSSOP (14)	5.00 mm × 4.40 mm
CD54HC4024F	CDIP (14)	19.55 mm × 6.71 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Functional Block Diagram

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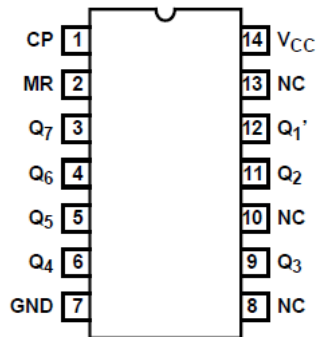
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## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (October 2003) to Revision D (March 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

## 4 Pin Configuration and Functions



**J, N, D or PW Package**  
**14-Pin CDIP, PDIP, SOIC, or TSSOP**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		- 0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		- 65	150	°C
	Lead temperature (soldering 10s) (SOIC - lead tips only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	V
V <sub>I</sub> , V <sub>O</sub>	DC input or output voltage		0	V <sub>CC</sub>	V
t <sub>t</sub>	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T <sub>A</sub>	Temperature range		- 55	125	°C

### 5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	86	80	113	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15			
			6	4.2		4.2		4.2			
V <sub>IL</sub>	Low level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35		
			6		1.8		1.8		1.8		
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 μA	2	1.9		1.9		1.9		V	
		I <sub>OH</sub> = – 20 μA	4.5	4.4		4.4		4.4			
	High level output voltage TTL loads	I <sub>OH</sub> = – 20 μA	6	5.9		5.9		5.9			
		I <sub>OH</sub> = – 4 mA	4.5	3.98		3.84		3.7			
		I <sub>OH</sub> = – 5.2 mA	6	5.48		5.34		5.2			
V <sub>OL</sub>	Low level output voltage CMOS loads	I <sub>OL</sub> = 20 μA	2		0.1		0.1		0.1	V	
		I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1		
	Low level output voltage TTL loads	I <sub>OL</sub> = 20 μA	6		0.1		0.1		0.1		
		I <sub>OL</sub> = 4 mA	4.5		0.26		0.33		0.4		
		I <sub>OL</sub> = 5.2 mA	6		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> or GND	6		±0.1		±1		±1	μA	
I <sub>CC</sub>	Quiescent device current	V <sub>CC</sub> or GND	6		8		80		160	μA	
<b>HCT TYPES</b>											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2		2		2		V	
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 μA	4.5	4.4		4.4		4.4		V	
	High level output voltage TTL loads	I <sub>OH</sub> = – 4 mA	4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1	V	
	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> and GND	5.5		±0.1		±1		±1	μA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> or GND	5.5		8		80		160	μA	
ΔI <sub>CC</sub> <sup>(1)</sup>	Additional supply current per input pin	CP, MR inputs held at V <sub>CC</sub> - 2.1	4.5 to 5.5		100	180		225		245	μA

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Prerequisite for Switching Specifications

PARAMETER		V <sub>CC</sub> (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
f <sub>MAX</sub>	Maximum input pulse frequency	2	6	5	4	MHz			
		4.5	30	24	20	MHz			
		6	35	29	24	MHz			
t <sub>W</sub>	Input pulse width	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
t <sub>REM</sub>	Reset removal time	2	50	65	75	ns			
		4.5	10	13	15	ns			
		6	9	11	13	ns			
t <sub>W</sub>	Reset pulse width	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
<b>HCT TYPES</b>									
f <sub>MAX</sub>	Maximum input pulse frequency	4.5	25	20	16	MHz			
t <sub>W</sub>	Input pulse width	4.5	20	25	30	ns			
t <sub>REC</sub>	Reset recovery time	4.5	10	13	15	ns			
t <sub>W</sub>	Reset pulse width	4.5	20	25	30	ns			

## 5.6 Switching Characteristics

$t_r, t_f = 6$  ns. See (Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
$t_{PLH}, t_{PHL}$	Propagation delay time CP to Q1' output	$C_L = 50$ pF	2		140		175		210	ns	
			4.5		28		35		42	ns	
		$C_L = 15$ pF	5		11					ns	
			6		24		30		36	ns	
$t_{PLH}, t_{PHL}$	Propagation delay time, $Q_n$ to $Q_{n+1}$	$C_L = 50$ pF	2		75		95		110	ns	
			4.5		15		19		22	ns	
		$C_L = 15$ pF	5		6					ns	
			6		13		13		19	ns	
$t_{PLH}, t_{PHL}$	Propagation delay time, MR to $Q_n$	$C_L = 50$ pF	2		170		215		255	ns	
			4.5		34		43		51	ns	
			5		14					ns	
			6		29		27		43	ns	
$t_{TLH}, t_{THL}$	Output transition time	$C_L = 50$ pF	2		75		95		110	ns	
			4.5		15		19		22	ns	
			6		13		16		19	ns	
$C_{IN}$	Input capacitance	$C_L = 50$ pF			10		10		10	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	$C_L = 15$ pF	5		30					pF	
<b>HCT TYPES</b>											
$t_{PLH}, t_{PHL}$	Propagation delay time CP to Q1' output	$C_L = 50$ pF	4.5		40		50		60	ns	
										ns	
$t_{PLH}, t_{PHL}$	Propagation delay time, $Q_n$ to $Q_{n+1}$	$C_L = 15$ pF	5		17					ns	
										ns	
$t_{PLH}, t_{PHL}$	Propagation delay time, MR to $Q_n$	$C_L = 50$ pF	4.5		40		50		60		
			5		17						
$t_{TLH}, t_{THL}$	Output transition time	$C_L = 50$ pF	4.5		15		19		22	ns	
$C_{IN}$	Input capacitance	$C_L = 15$ pF			10		10		10	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	$C_L = 15$ pF	5		30					pF	

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per buffer.

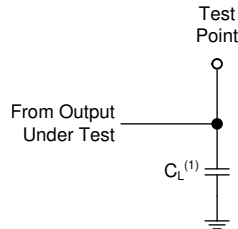
(2)  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$  where:  $M = 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$   $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

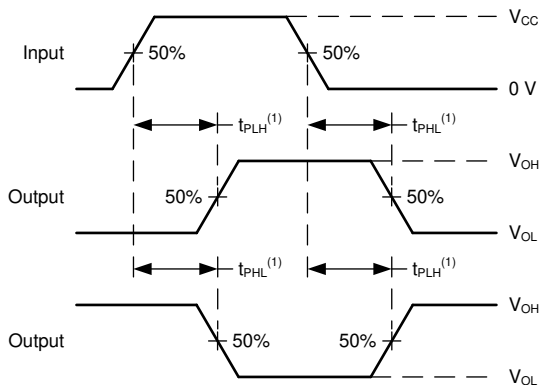
For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



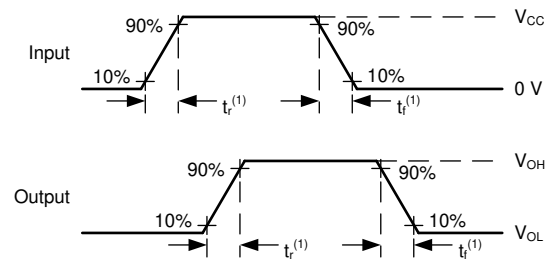
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**



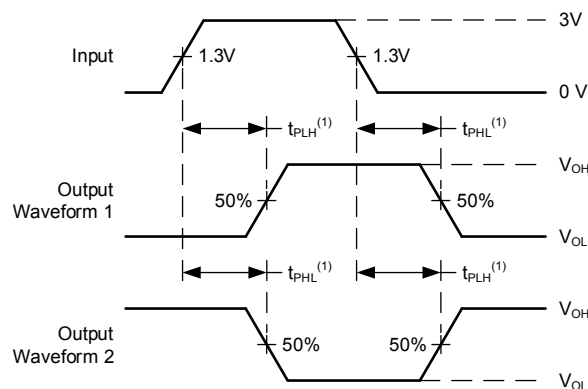
(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

**Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**



(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

**Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC4024F	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC4024F	<a href="#">Samples</a>
CD54HCT4024F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT4024F3A	<a href="#">Samples</a>
CD74HC4024E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4024E	<a href="#">Samples</a>
CD74HC4024M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC4024M	<a href="#">Samples</a>
CD74HC4024PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HJ4024	<a href="#">Samples</a>
CD74HCT4024E	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4024E	<a href="#">Samples</a>
CD74HCT4024EE4	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4024E	<a href="#">Samples</a>
CD74HCT4024M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4024M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4024, CD54HCT4024, CD74HC4024, CD74HCT4024 :**

● Catalog : [CD74HC4024](#), [CD74HCT4024](#)

● Military : [CD54HC4024](#), [CD54HCT4024](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4024M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4024M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4024PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4024PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4024PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4024M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC4024M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC4024PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4024PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4024PWR	TSSOP	PW	14	2000	366.0	364.0	50.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024M	D	SOIC	14	50	506.6	8	3940	4.32

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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