





# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## General Description

The MAX5450–MAX5455 are a family of dual digital potentiometers that perform the same function as a mechanical potentiometer or variable resistor. The MAX5451/MAX5453/MAX5455 have two 3-terminal potentiometers and the MAX5450/MAX5452/MAX5454 have two 2-terminal variable resistors. The MAX5450–MAX5455 operate from a +2.7V to +5.5V single-supply voltage and use an ultra-low supply current of 0.1μA. These devices consist of two fixed resistors each with 256 digitally-controlled wiper contacts. The convenient power-on reset (POR) sets the wiper to midscale position at power-up and the easy-to-use up/down interface allows glitchless switching between resistor taps. Six inputs control the 14-pin MAX5451/MAX5453/MAX5455 potentiometers. Four inputs control the 10-pin MAX5450/MAX5452/MAX5454 variable resistors.

The MAX5450–MAX5455 are ideal for applications requiring digitally-controlled resistors. Three resistance values are available: 10kΩ, 50kΩ, and 100kΩ. An end-to-end resistor temperature coefficient of 35ppm/°C and a ratiometric temperature coefficient of 5ppm/°C make the MAX5450–MAX5455 excellent choices for adjustable gain circuit requiring low-temperature drift.

The MAX5450–MAX5455 are available in 10-pin μMAX® and 14-pin TSSOP packages. Each device is guaranteed over the extended–industrial temperature range (-40°C to +85°C).

## Applications

Mechanical Potentiometer Replacement  
 Low-Drift Programmable-Gain Amplifier (PGA)  
 Volume Control  
 LCD Screen Adjustment  
 Adjustable Voltage References  
 Adjustable Linear Regulators  
 Programmable Filters, Delays, Time Constants  
 Impedance Matching

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## Features

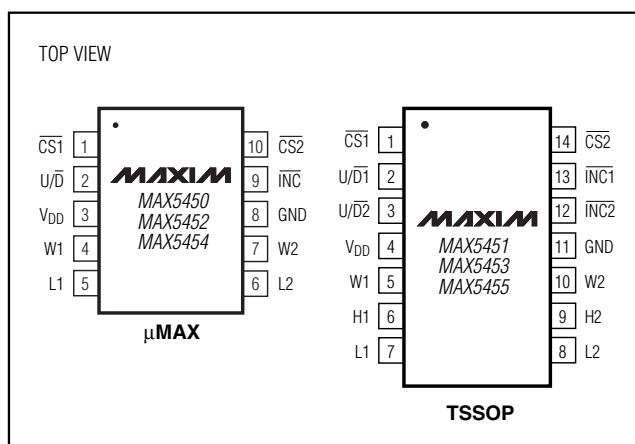
- ◆ Small-Footprint Packages
  - 10-Pin μMAX (MAX5450/MAX5452/MAX5454)
  - 14-Pin TSSOP (MAX5451/MAX5453/MAX5455)
- ◆ 256-Tap Positions
- ◆ Independent Up/Down Potentiometer Controls (MAX5451/MAX5453/MAX5455)
- ◆ Ultra-Low 0.1μA Supply Current
- ◆ +2.7V to +5.5V Single-Supply Operation
- ◆ Low 35ppm/°C End-to-End Temperature Coefficient
- ◆ Power-On Reset Sets Wiper to Midscale (Position 127)
- ◆ Glitchless Switching Between the Resistor Taps
- ◆ 10kΩ, 50kΩ, 100kΩ Resistance Values

## Ordering Information

PART	PIN-PACKAGE	R (kΩ)	PKG CODE
MAX5450EUB	10 μMAX	10	U10C-4
MAX5451EUD	14 TSSOP	10	U14-1
MAX5452EUB	10 μMAX	50	U10C-4
MAX5453EUD	14 TSSOP	50	U14-1
MAX5454EUB	10 μMAX	100	U10C-4
MAX5455EUD	14 TSSOP	100	U14-1

**Note:** All devices specified over the -40°C to +85°C operating range.

## Pin Configurations



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## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND .....	-0.3V to +6V	14-Pin TSSOP (derate 9.1mW/°C above +70°C) .....	727mW
$CS_{-}$ , $INC_{-}$ , and $U/D_{-}$ to GND .....	-0.3V to +6V	Operating Temperature Range .....	-40°C to +85°C
$H_{-}$ , $L_{-}$ , $W_{-}$ to GND .....	-0.3V to ( $V_{DD}$ +0.3V)	Junction Temperature .....	+150°C
Maximum Continuous Current into $H_{-}$ , $L_{-}$ , and $W_{-}$ .....	±1mA	Storage Temperature Range .....	-65°C to +150°C
Continuous Power Dissipation ( $T_A$ = +70°C)		Lead Temperature (soldering, 10s) .....	+300°C
10-Pin $\mu$ MAX (derate 6.94mW/°C above +70°C) .....	555mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{DD}$  = +2.7V to +5.5V,  $V_H$  =  $V_{DD}$ ,  $V_L$  = 0;  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{DD}$  = +5V,  $T_A$  = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>DC PERFORMANCE (Voltage-Divider Mode, MAX5451/MAX5453/MAX5455 Only)</b>							
Resolution	N			8			Bits
Integral Nonlinearity (Notes 1 and 2)	INL	$V_{DD}$ = +5V				±1	LSB
		$V_{DD}$ = +3V				±1	
Differential Nonlinearity (Notes 1 and 2)	DNL	$V_{DD}$ = +5V				±1	LSB
		$V_{DD}$ = +3V				±1	
End-to-End Resistor Tempco	$TC_R$			35			ppm/°C
Ratiometric Resistor Tempco				5			ppm/°C
Full-Scale Error		MAX5451		-8			LSB
		MAX5453		-1.6			
		MAX5455		-0.8			
Zero-Scale Error		MAX5451		+8			LSB
		MAX5453		+1.6			
		MAX5455		+0.8			
<b>DC PERFORMANCE (Variable Resistor Mode)</b>							
Resolution	N			8			Bits
Integral Nonlinearity (Notes 1 and 3)	INL	$V_{DD}$ = +5V	MAX5450, MAX5451			±3	LSB
			MAX5452-MAX5455			±1	
		$V_{DD}$ = +3V	MAX5450, MAX5451			±4.5	
			MAX5452-MAX5455			±2	
Differential Nonlinearity (Notes 1 and 3)	DNL	$V_{DD}$ = +5V				±1	LSB
		$V_{DD}$ = +3V				±1	
<b>DC PERFORMANCE (Resistor Characteristics)</b>							
Wiper Resistance (Note 4)	$R_W$	$V_{DD}$ = +5V, MAX5451/MAX5453/MAX5455		225			$\Omega$
		$V_{DD}$ = +3V, MAX5451/MAX5453/MAX5455		550			
Wiper Capacitance	$C_W$			10			pF
End-To-End Resistance	$R_{HL}$	MAX5450, MAX5451		6.5	10	12.5	k $\Omega$
		MAX5452, MAX5453		32	50	62.5	
		MAX5454, MAX5455		60	100	125	

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MAX5450-MAX5455

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+5.5V$ ,  $V_H = V_{DD}$ ,  $V_L = 0$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS (Note 5)</b>						
Input High Voltage	$V_{IH}$		0.7 x $V_{DD}$			V
Input Low Voltage	$V_{IL}$			0.3 x $V_{DD}$		V
Input Leakage Current				±1.0		μA
Input Capacitance				5		pF
<b>TIMING CHARACTERISTICS (Analog)</b>						
Wiper-Settling Time (Note 6)	$t_{1W}$	MAX5451	0.5		μs	
		MAX5453	1.2			
		MAX5455	1.8			
<b>TIMING CHARACTERISTICS (Digital, Note 7, Figure 1)</b>						
Maximum $\overline{INC}$ Frequency	$f_{MAX}$		7			MHz
$\overline{CS}$ to $\overline{INC}$ Setup Time	$t_{CI}$		25			ns
$\overline{CS}$ to $\overline{INC}$ Hold Time	$t_{IC}$		0			ns
$\overline{INC}$ Low Period	$t_{IL}$		25			ns
$\overline{INC}$ High Period	$t_{IH}$		25			ns
$U/\overline{D}$ to $\overline{INC}$ Setup	$t_{DI}$		50			ns
$U/\overline{D}$ to $\overline{INC}$ Hold	$t_{ID}$		0			ns
<b>POWER SUPPLIES</b>						
Supply Voltage	$V_{DD}$		2.7		5.5	V
Supply Current	$I_{DD}$	$\overline{CS} = \overline{INC} = U/\overline{D} = V_{DD}$ or GND	$V_{DD} = +5V$	0.7	2	μA
			$V_{DD} = +2.7V$	0.1		

**Note 1:** Linearity is defined in terms of the  $H_-$  to  $L_-$  code-dependent resistance.

**Note 2:** The DNL and INL are measured with the potentiometer configured as a voltage divider with  $H_- = V_{DD}$  and  $L_- = GND$ . The wiper terminal is unloaded and measured with an ideal voltmeter.

**Note 3:** The DNL and INL are measured with the potentiometer configured as a variable resistor. For the 3-terminal potentiometers (MAX5451/MAX5453/MAX5455),  $H_-$  is unconnected and  $L_- = GND$ . For the 2-terminal potentiometers (MAX5450/MAX5452/MAX5454),  $L_- = GND$ . At  $V_{DD} = +5V$ , the wiper terminal is driven with a source current of 400μA for the 10kΩ configuration, 80μA for the 50kΩ configuration, and 40μA for the 100kΩ configuration. At  $V_{DD} = +3V$ , 200μA/40μA/20μA for 10kΩ/50kΩ/100kΩ configuration, respectively.

**Note 4:** The wiper resistance is the worst value measured by injecting the currents given in Note 3 into  $W_-$  with  $L_- = GND$ .  $R_{W_-} = (V_{W_-} - V_{H_-}) / I_{W_-}$ .

**Note 5:** Device draws higher supply current when digital inputs are driven with voltages between  $(V_{DD} - 0.5V)$  and  $(GND + 0.5V)$ . (See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.)

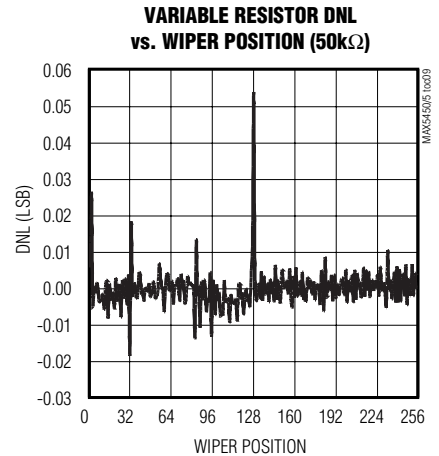
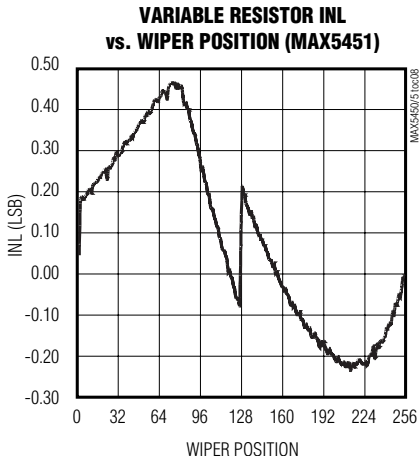
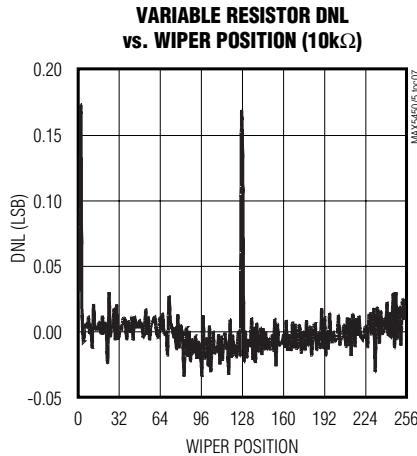
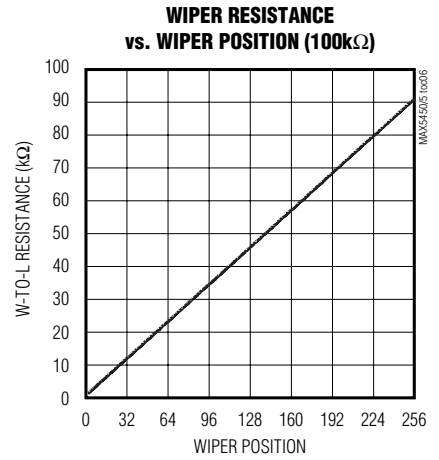
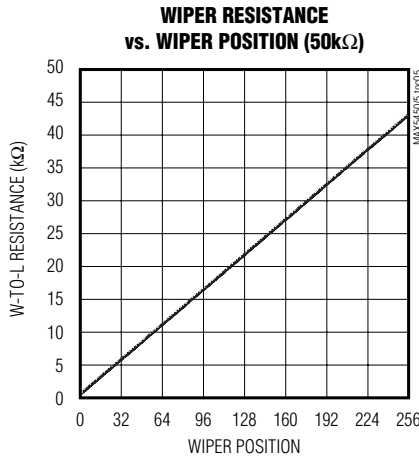
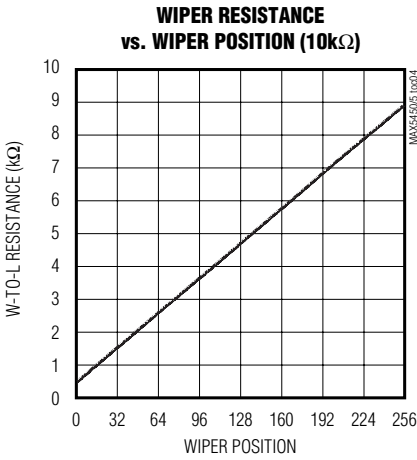
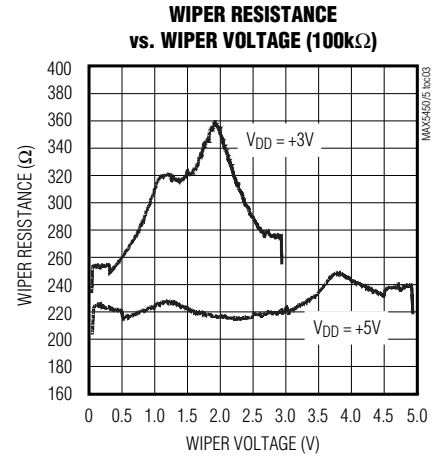
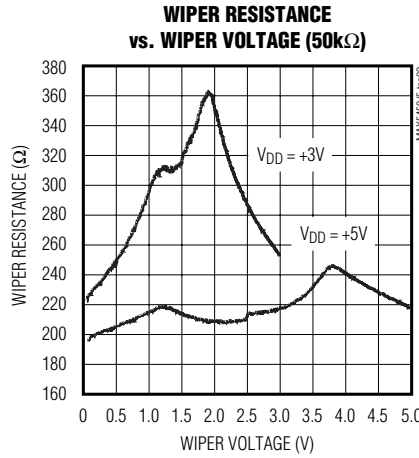
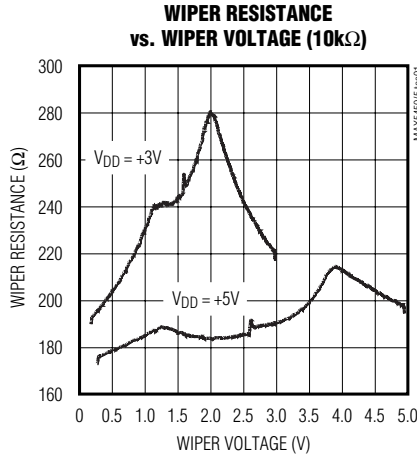
**Note 6:** Wiper-Settling Time is the worst case 0% to 50% rise-time measured between consecutive wiper positions.  $H_- = V_{DD}$ ,  $L_- = GND$ , and the wiper terminal is unloaded and measured with a 10pF oscilloscope probe (see Tap-To-Tap Switching Transient in the *Typical Operating Characteristics*).

**Note 7:** Digital timing is guaranteed by design.

# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Typical Operating Characteristics

( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

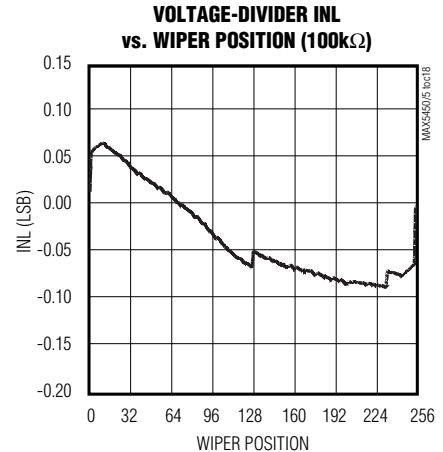
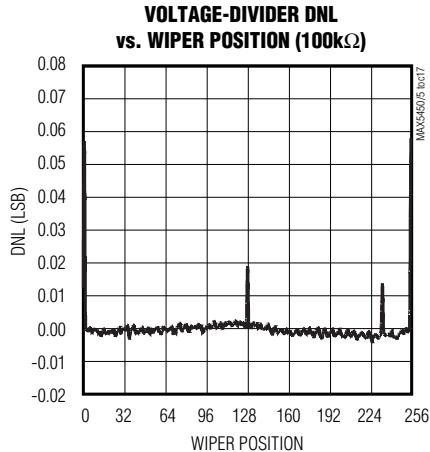
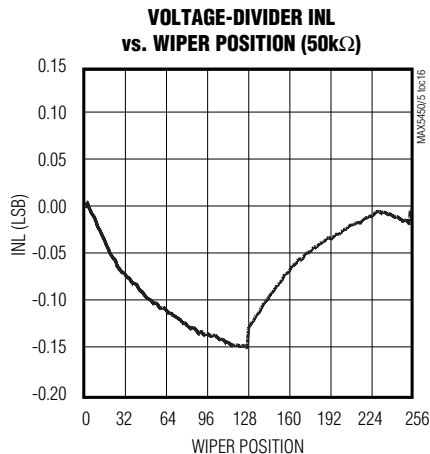
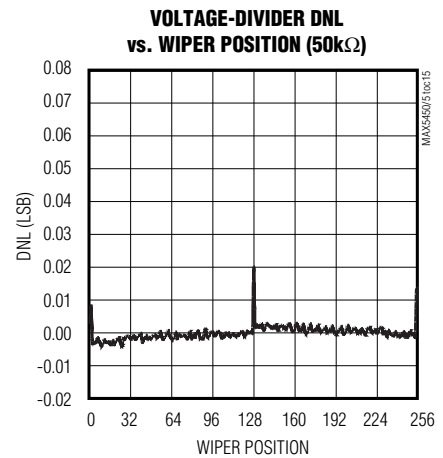
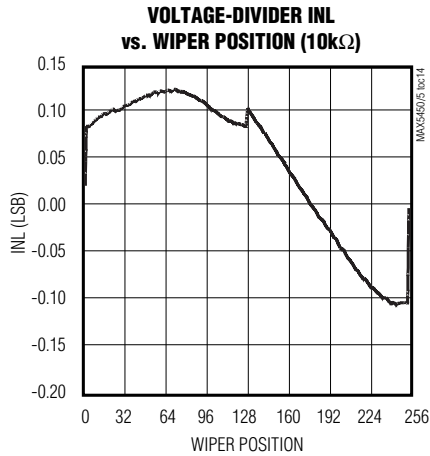
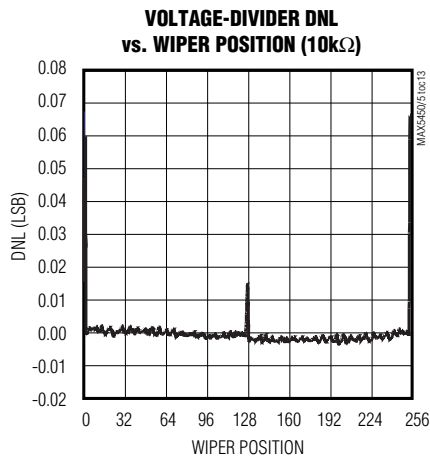
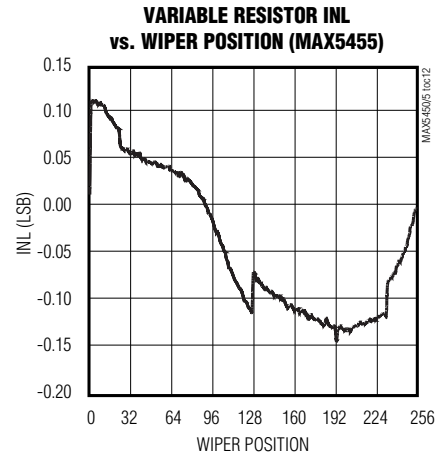
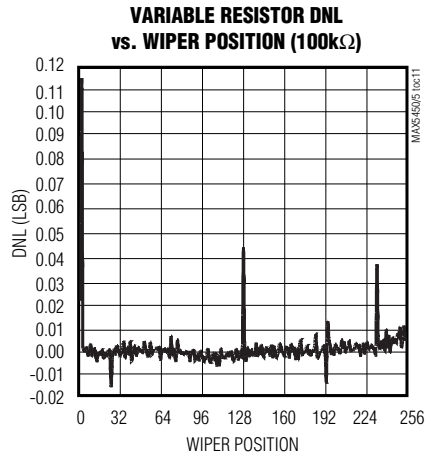
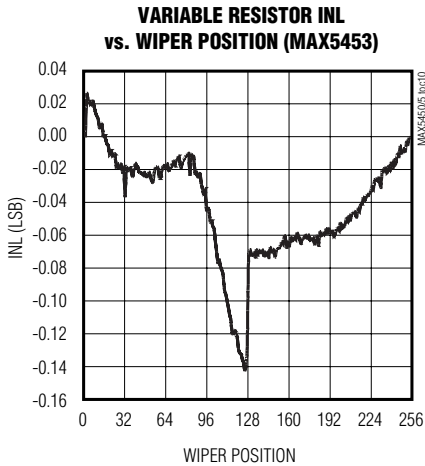


# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

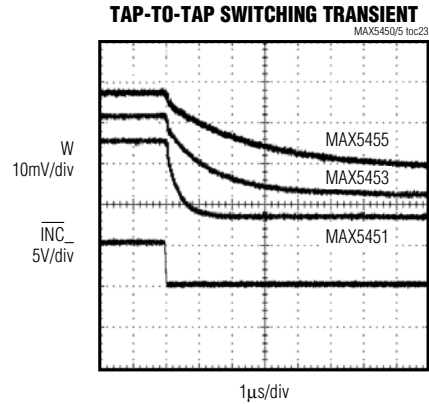
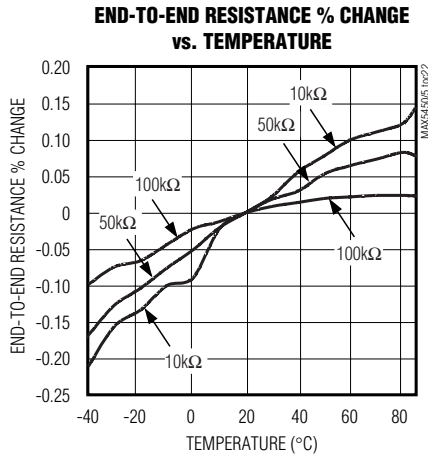
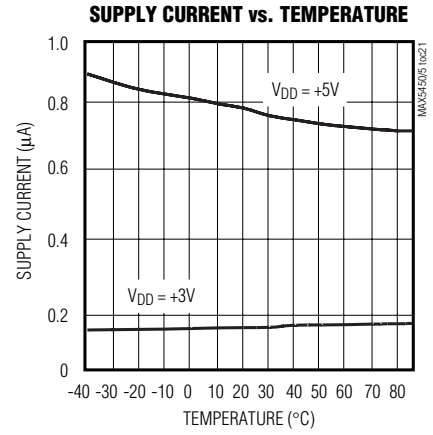
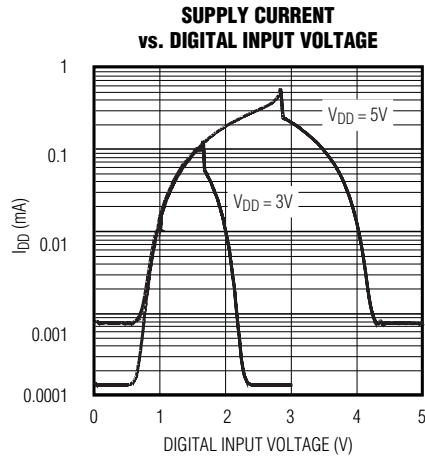
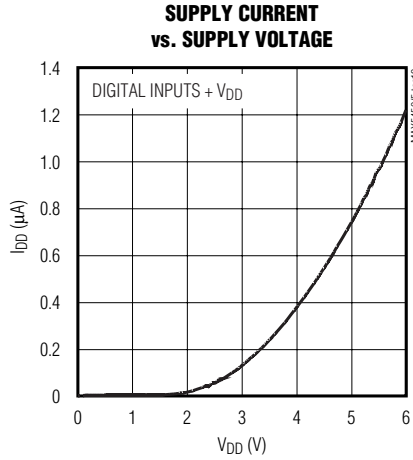
MAX5450-MAX5455



# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Pin Description

MAX5450-MAX5455

PIN		NAME	FUNCTION
MAX5451 MAX5453 MAX5455	MAX5450 MAX5452 MAX5454		
1	1	$\overline{CS1}$	Chip-Select Input of Resistor 1. Drive low to change wiper position W1 through $\overline{INC}$ and U/D.
—	2	U/D	Up/Down Control Input. With U/D low, a high-to-low $\overline{INC}$ transition decrements wiper position. With U/D high, a high-to-low $\overline{INC}$ transition increments wiper position.
2	—	U/D1	Up/Down Control Input of Resistor 1. With U/D1 low, a high-to-low $\overline{INC1}$ transition decrements wiper position W1. With U/D1 high, a high-to-low $\overline{INC1}$ transition increments wiper position W1.
3	—	U/D2	Up/Down Control Input of Resistor 2. With U/D2 low, a high-to-low $\overline{INC2}$ transition decrements wiper position W2. With U/D2 high, a high-to-low $\overline{INC2}$ transition increments wiper position W2.
4	3	V <sub>DD</sub>	Power Supply
5	4	W1	Wiper Terminal of Resistor 1
6	—	H1	High Terminal of Resistor 1
7	5	L1	Low Terminal of Resistor 1
8	6	L2	Low Terminal of Resistor 2
9	—	H2	High Terminal of Resistor 2
10	7	W2	Wiper Terminal of Resistor 2
11	8	GND	Ground
—	9	$\overline{INC}$	Wiper Increment Control Input. With $\overline{CS1}$ low, a high-to-low transition increments (U/D high) or decrements (U/D low) wiper position W1. This applies similarly for $\overline{CS2}$ and W2.
12	—	$\overline{INC2}$	Wiper Increment Control Input. With $\overline{CS2}$ low, a high-to-low transition increments (U/D2 high) or decrements (U/D2 low) wiper position W2.
13	—	$\overline{INC1}$	Wiper Increment Control Input. With $\overline{CS1}$ low, a high-to-low transition increments (U/D1 high) or decrements (U/D1 low) wiper position W1.
14	10	$\overline{CS2}$	Chip-Select Input of Resistor 2. Drive low to change wiper position W2 through $\overline{INC}$ and U/D.

# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

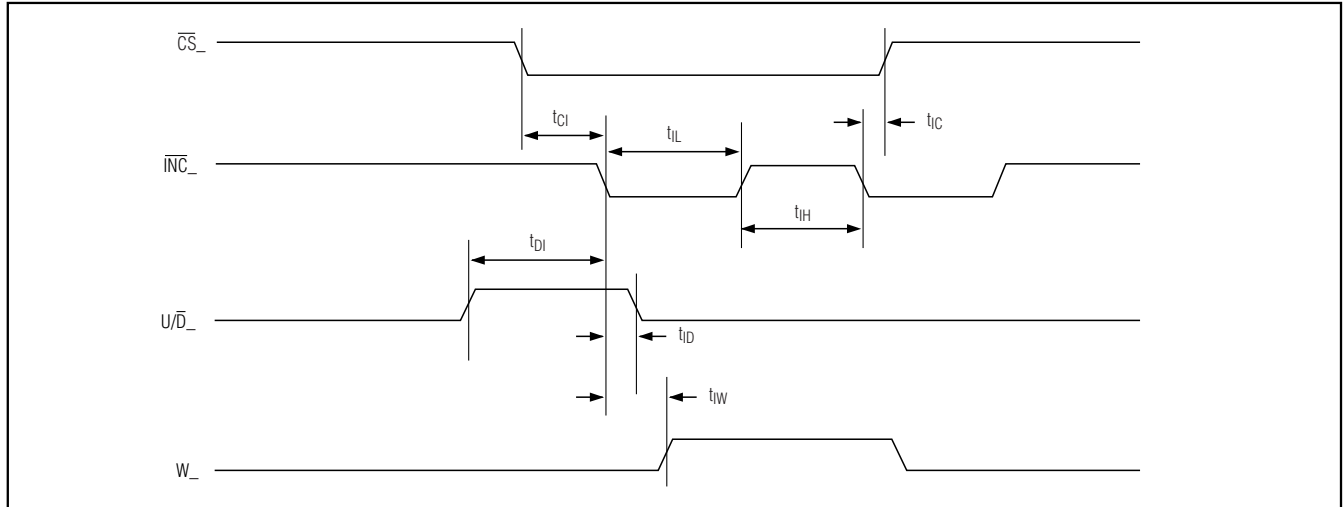


Figure 1. Digital Interface and Timing diagram

## Detailed Description

The MAX5450–MAX5455 contain two independent resistor arrays each with 255-resistive elements. 256-tap points are accessible to the wiper along the resistor arrays between H and L (Figure 2). Power-on reset circuitry sets the wiper to midscale (position 127) at power-up.

Logic inputs  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$  determine the wiper position of the MAX5450–MAX5455. With  $\overline{CS}$  low and  $U/\overline{D}$  high, a high-to-low (falling edge) transition on  $\overline{INC}$ , increments the internal counter, which increases the resistance between W and L. When both  $\overline{CS}$  and  $U/\overline{D}$  are low, a high-to-low  $\overline{INC}$  transition decrements the internal counter, decreasing the resistance between W and L (Figure 1). The wiper performs a make-before-break transition ensuring that there is never an open circuit during a transition from one resistor tap to another. When the wiper is at either end (max/min) of the resistor array, additional transitions in the direction of the endpoint will not change the counter value (the counter will not wrap around).

The MAX5450/MAX5452/MAX5454 are similar to the MAX5451/MAX5453/MAX5455 except for internal connections. The MAX5450/MAX5452/MAX5454 internally connect  $\overline{INC1}$  to  $\overline{INC2}$ ,  $U/\overline{D1}$  to  $U/\overline{D2}$ ,  $W1$  to  $H1$ , and  $W2$  to  $H2$  (Figures 3 and 4). The internal connections configure the MAX5450/MAX5452/MAX5454 to be variable resistors.

## Applications Information

The MAX5450–MAX5455 are ideal for adjustable voltage or adjustable gain circuits where accurate adjustable resistances are required.

### Adjustable Current to Voltage Converter

Figure 5 shows the MAX5450/MAX5452/MAX5454 with a MAX4250 low-noise op amp to fine-tune a current to voltage converter. The physical sizes of both devices minimize circuit space.

### Adjustable Gain Amplifier

Figures 6a and 6b shows the MAX5450–MAX5455 digitally adjusting the gain of the MAX4493 general-purpose, dual supply op amp. Figure 6a shows the MAX5450/MAX5452/MAX5454 variable resistor in series with a resistor to ground to form the adjustable gain control. Figure 6b shows the MAX5451/MAX5453/MAX5455 as a 3-terminal potentiometer. In these applications the low 5ppm/°C ratiometric tempco allows for a very stable adjustable gain over temperature.

### Adjustable Linear Regulator

In Figure 7, the MAX5450/MAX5452/MAX5454 is shown digitally adjusting the output voltage of the MAX8866 dual linear regulator. In this circuit, the MAX5450/MAX5452/MAX5454 is connected in series with a resistor to ground to form the adjustable feedback stage. The 8-bit MAX5450/MAX5452/MAX5454 allows precise tuning of the output voltage.

# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

**MAX5450-MAX5455**

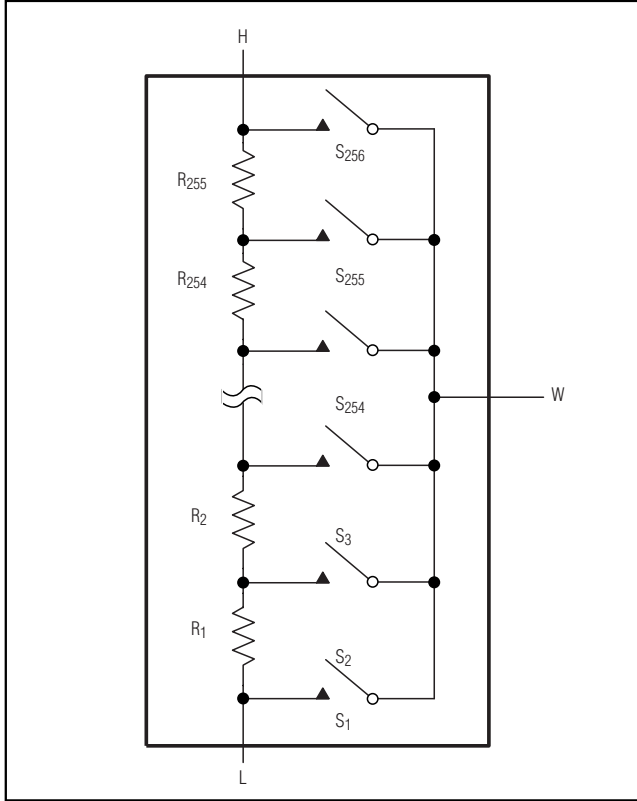


Figure 2. Simplified Digital Potentiometer Resistor Array

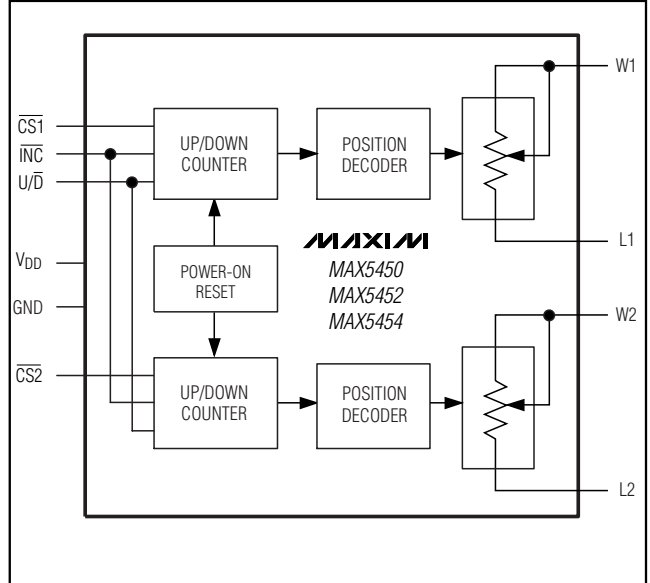


Figure 3. MAX5450/MAX5452/MAX5454 Simplified Functional Diagram

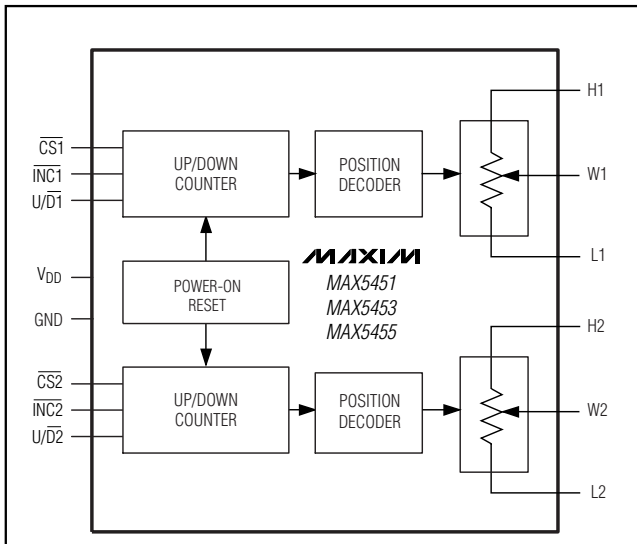


Figure 4. MAX5451/MAX5453/MAX5455 Simplified Functional Diagram

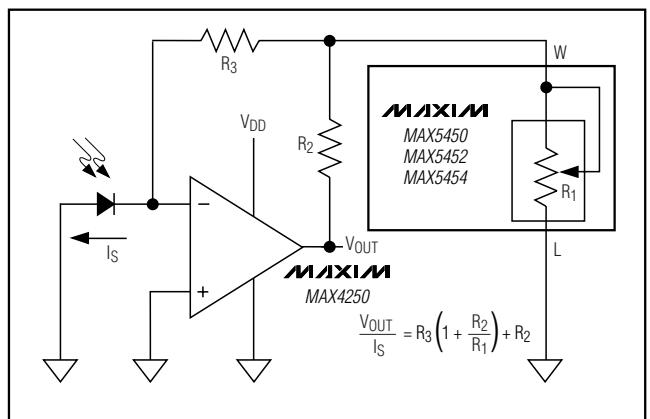


Figure 5. Adjustable Current to Voltage Converter

$$\frac{V_{OUT}}{I_S} = R_3 \left( 1 + \frac{R_2}{R_1} \right) + R_2$$

# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

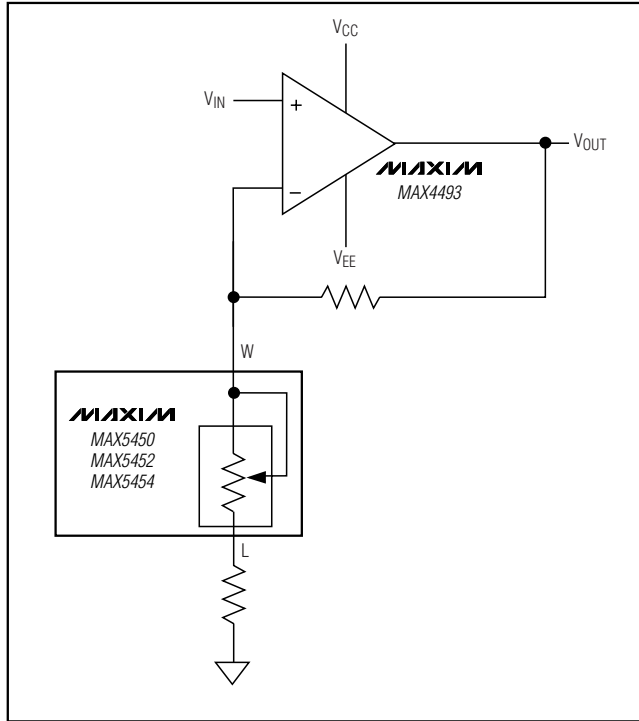


Figure 6a. Variable Resistor Adjustable-Gain Amplifier

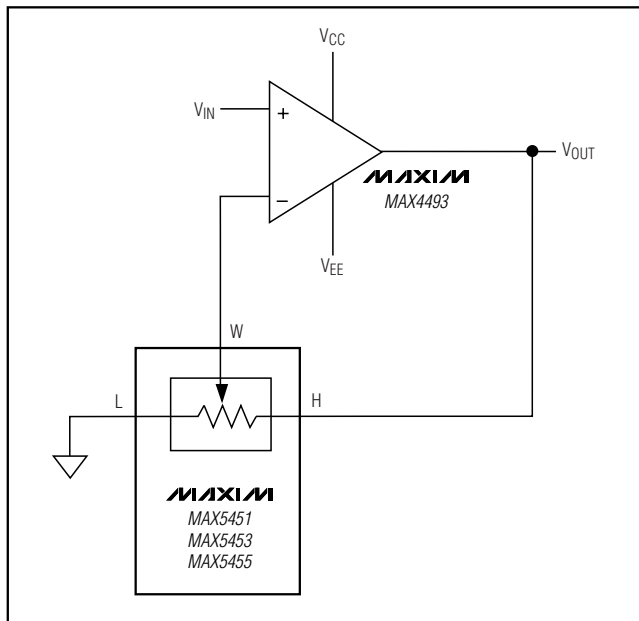


Figure 6b. Potentiometer Adjustable-Gain Amplifier

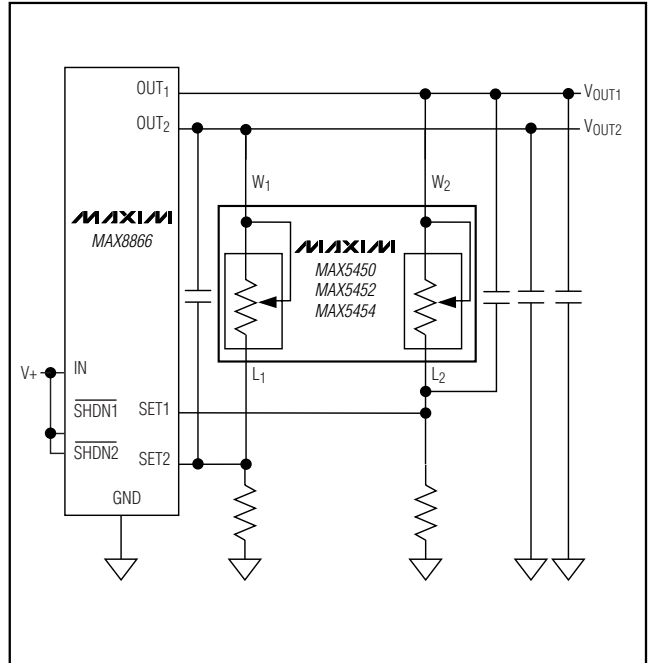


Figure 7. Adjustable Dual Linear Regulator

## Truth Table

$\overline{CS}$	$U/\overline{D}$	$\overline{INC}$	$W$
H	X	X	O
L	L	↑	O
L	H	↑	O
L	L	↓	-
L	H	↓	+

*X = Don't care*                      *O = Previous State*  
*↓ = High-to-Low Transition*      *- = Decrement*  
*↑ = Low-to-High Transition*      *+ = Increment*

## Chip Information

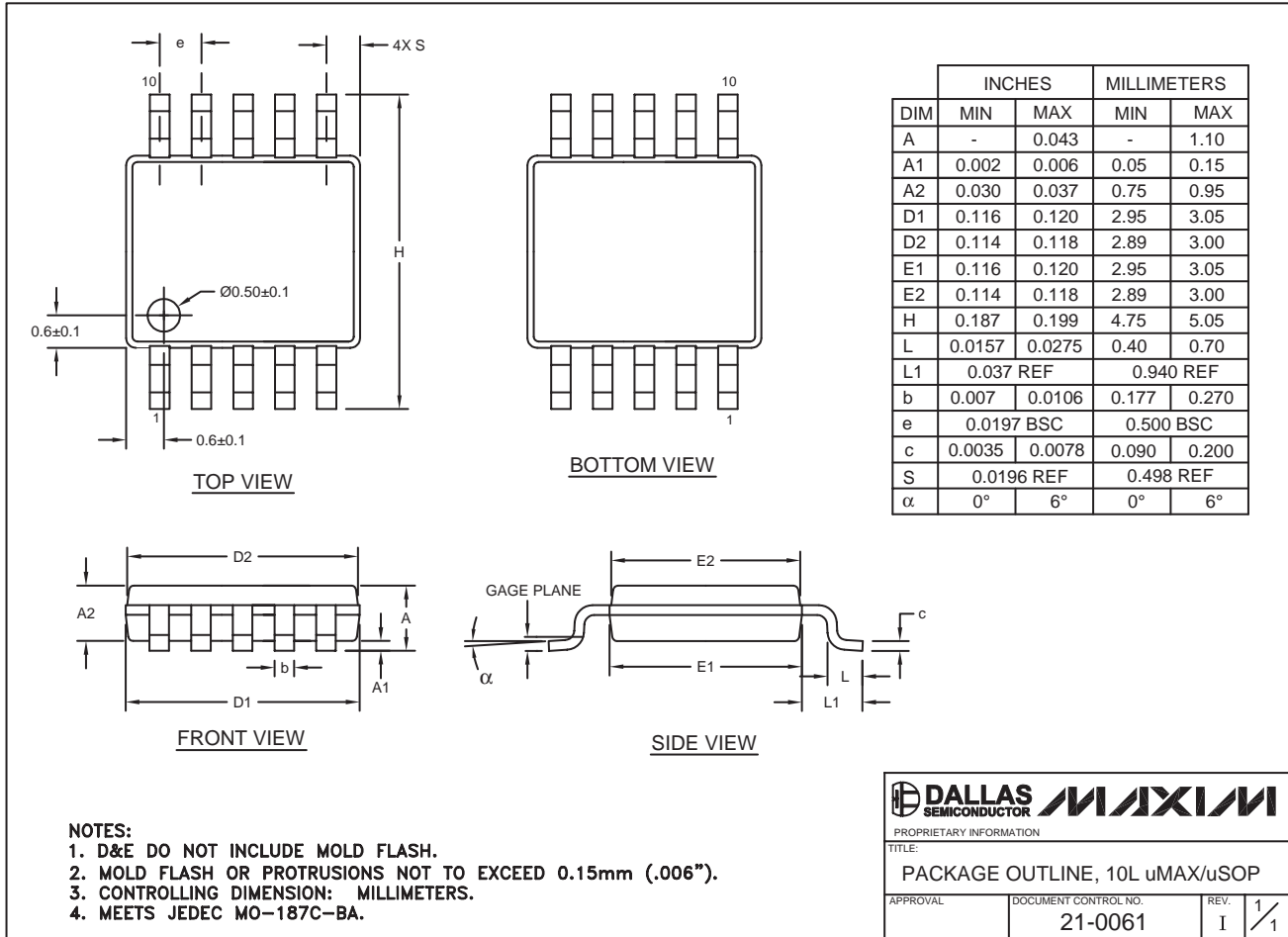
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 PROCESS: CMOS

# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Package Information

MAX5450-MAX5455

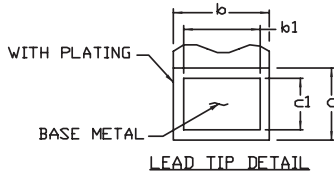
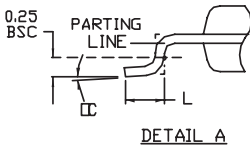
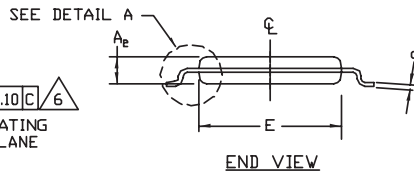
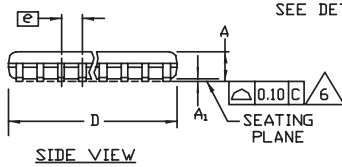
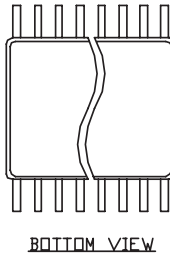
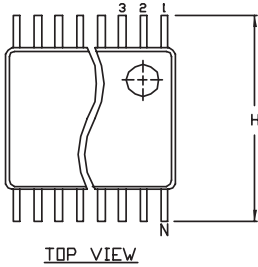
10LUMAX.EPS



# Dual, 256-Tap, Up/Down Interface, Digital Potentiometers

## Package Information (continued)

TSSOP4.40mm.EPS



	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	.043	
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>2</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c <sub>1</sub>	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC	N		VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

**NOTES:**

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. 'N' REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-



TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY	
APPROVAL	DOCUMENT CONTROL NO. 21-0066
REV. G	1/1

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