THE DATASHEET OF

MAX4566EEE+

ANALOG DEVICES

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Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

MAX4565/MAX4566/MAX4567

General Description

The MAX4565/MAX4566/MAX4567 are low-voltage T-switches designed for switching RF and video signals from DC to 350MHz in 50Ω and 75Ω systems. The MAX4565 contains four normally open single-pole/single-throw (SPST) switches. The MAX4566 contains two dual SPST switches (one normally open, one normally closed.) The MAX4567 contains two single-pole/double-throw (SPDT) switches.

Each switch is constructed in a "T" configuration, ensuring excellent high-frequency off isolation and crosstalk of -83dB at 10MHz. They can handle rail-to-rail analog signals in either direction. On-resistance (60Ω max) is matched between switches to 2.5Ω max and is flat (2Ω max) over the specified signal range, using ±5V supplies. The off leakage current is less than 5nA at +25°C and 50nA at +85°C.

These CMOS switches can operate with dual power supplies ranging from ±2.7V to ±6V or a single supply between +2.7V and +12V. All digital inputs have 0.8V/2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

- RF Switching
- Video Signal Routing
- High-Speed Data Acquisition
- Test Equipment
- ATE Equipment
- Networking

Features

- High 50Ω Off Isolation: -83dB at 10MHz
- Low 50Ω Crosstalk: -87dB at 10MHz
- DC to 350MHz -3dB Signal Bandwidth
- 60Ω Signal Paths with ±5V Supplies
- 2.5Ω Signal-Path Matching with ±5V Supplies
- 2Ω Signal-Path Flatness with ±5V Supplies
- Low 50Ω Insertion Loss: 2.5dB at 100MHz
- ±2.7V to ±6V Dual Supplies
  +2.7V to +12V Single Supply
- Low Power Consumption: <1µW
- Rail-to-Rail Bidirectional Signal Handling
- Pin Compatible with Industry-Standard DG540, DG542, DG643
- >2kV ESD Protection per Method 3015.7
- TTL/CMOS-Compatible Inputs
  with Single +5V or ±5V

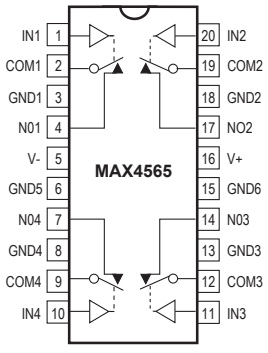
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4565CPP	0°C to +70°C	20 Plastic DIP
MAX4565CWP	0°C to +70°C	20 Wide SO

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

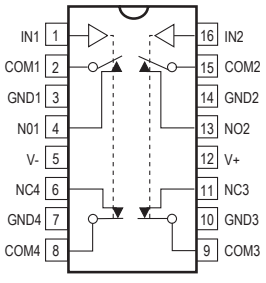


DIP/SO/SSOP

MAX4565	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

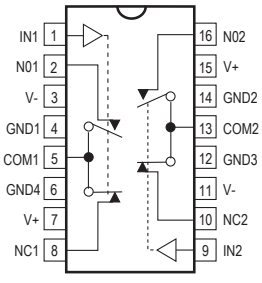
MAX4566



DIP/SO/QSOP

MAX4566		
LOGIC	1, 2	3, 4
0	OFF	ON
1	ON	OFF

MAX4567



DIP/SO/QSOP

MAX4567		
LOGIC	NO-COM	NC-COM
0	OFF	ON
1	ON	OFF

19-1252; Rev 1; 2/21

Absolute Maximum Ratings

(Voltages Referenced to GND)
V+ ..... -0.3V, +13.0V
V- ..... -13.0V, +0.3V
V+ to V- ..... -0.3V, +13.0V
All Other Pins (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal ..... ±25mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle) ..... ±50mA
ESD per Method 3015.7 ..... >2000V
Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP
(derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO
(derate 8.70mW/°C above +70°C) 696mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
20-Pin Plastic DIP (derate 8.0mW/°C above +70°C) 640mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ... 800mW
20-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX456_C_ E ..... 0°C to +70°C
MAX456_E_ E ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Voltages on all other pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND\_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)	C, E	V-		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM\_}$ = ±2V, $I_{COM\_}$ = 10mA	+25°C		46	60	Ω
			C, E			80	
Signal-Path On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM\_}$ = ±2V, $I_{COM\_}$ = 10mA	+25°C		1	2.5	Ω
			C, E			3	
Signal-Path On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V; V- = -5V; $V_{COM\_}$ = 1V, 0V, -1V; I_{COM} = 10mA	+25°C		0.3	2	Ω
NO_, NC_ Off Leakage Current (Note 6)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{N\_}$ = ± 4.5V	+25°C	-1	0.02	1	nA
			C, E	-10		10	
COM_ Off Leakage Current (Note 6)	$I_{COM\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{N\_}$ = ± 4.5V	+25°C	-1	0.02	1	nA
			C, E	-10		10	
COM_ On Leakage Current (Note 6)	$I_{COM\_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V	+25°C	-2	0.04	2	nA
			C, E	-20		20	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA

Electrical Characteristics—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND\_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{COM\_}$ = ±3V, V+ = 5V, V- = -5V, Figure 3		+25°C		75	150	ns
				C, E			200	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = ±3V, V+ = 5V, V- = -5V, Figure 3		+25°C		30	100	ns
				C, E			120	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM\_}$ = ±3V, V+ = 5V, V- = -5V, Figure 4		+25°C	5	30		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, $V_{NO\_}$ = 0V, R_S = 0Ω, Figure 5		+25°C		25	60	pC
NO_, NC_ Off Capacitance	$C_{N\_(OFF)}$	$V_{NO\_}$ = GND, f = 1MHz, Figure 7		+25°C		2.5		pF
COM_ Off Capacitance	$C_{COM\_(OFF)}$	$V_{COM\_}$ = 0V, f = 1MHz, Figure 7	MAX4565	+25°C		2.5		pF
			MAX4566					
COM_ On Capacitance	$C_{COM\_(ON)}$	$V_{COM\_}$ = $V_{NO\_}$ = 0V, f = 1MHz, Figure 7	MAX4565	+25°C		6		pF
			MAX4566			6		
			MAX4567			7		
Off Isolation (Note 7)	V_{ISO}	R_L = 50Ω, $V_{COM\_}$ = $1V_{RMS}$, f = 10MHz, Figure 6	MAX4565	+25°C		-83		dB
			MAX4566			-82		
			MAX4567			-83		
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, $V_{COM\_}$ = $1V_{RMS}$, f = 10MHz, Figure 6	MAX4565	+25°C		-92		dB
			MAX4566			-85		
			MAX4567			-87		
-3dB Bandwidth (Note 9)	BW	Figure 6, R_L = 50Ω		+25°C		350		MHz
Distortion	THD+N	V_{IN} = 5Vp-p, f < 20kHz, 600Ω in and out		+25°C		0.02		%
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E	-6		+6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN\_}$ = 0V or V+		+25°C	-1	0.05	1	µA
				C, E	-10		10	
V - Supply Current	I-	V- = -5.5V		+25°C	-1	0.05	1	µA
				C, E	-10		10	

Electrical Characteristics—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND\_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER_	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM\_}$ = 3.5V, $I_{COM\_}$ = 1mA	+25°C		68	120	Ω
			C, E			150	
Signal-Path On-Resistance Match	ΔR_{ON}	V+ = 4.5V, $V_{COM\_}$ = 3.5V, $I_{COM\_}$ = 1mA	+25°C		2	5	Ω
			C, E			6	
NO_, NC_ Off Leakage Current (Notes 6, 10)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V, $V_{COM\_}$ = 1V, $V_{N\_}$ = 4.5V	+25°C	-1		1	nA
			C, E	-10		10	
COM_ Off Leakage Current (Notes 6, 10)	$I_{COM\_(OFF)}$	V+ = 5.5V, $V_{COM\_}$ = 1V, $V_{N\_}$ = 4.5V	+25°C	-1		1	nA
			C, E	-10		10	
COM_ On Leakage Current (Notes 6, 10)	$I_{COM\_(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V	+25°C	-2		2	nA
			C, E	-20		20	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V	C, E	-1	0.001	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 3V, V+ = 5V, Figure 3	+25°C		130	200	ns
			C, E			250	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 3V, V+ = 5V, Figure 3	+25°C		30	120	ns
			C, E			150	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM\_}$ = 3V, V+ = 5V, Figure 4	+25°C	10	90		ns
Charge Injection	Q	C_L = 1.0nF, V_{NO} = 2.5V, R_S = 0Ω, Figure 5	+25°C		7	25	pC
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, f = 10MHz, $V_{COM\_}$ = $1V_{RMS}$, Figure 6	+25°C		-81		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, f = 10MHz, $V_{COM\_}$ = $1V_{RMS}$, Figure 6	+25°C		-86		dB
-3dB Bandwidth (Note 9)	BW	R_L = 50Ω, Figure 6	+25°C		320		MHz
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN\_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

Electrical Characteristics—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND\_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

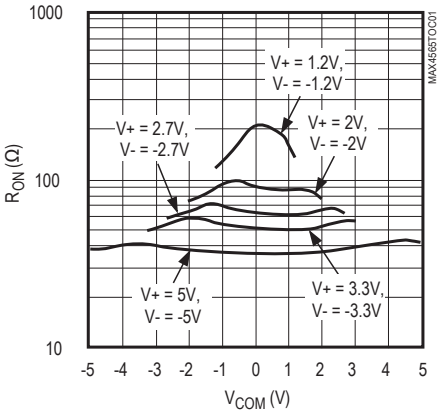
PARAMETER_	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM\_}$ = 1V, $I_{COM\_}$ = 1mA	+25°C		150	350	Ω
			C, E			450	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}	(Note 3)	C, E		1.0	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}	(Note 3)	C, E	0.8	1.0		V
IN_ Input Current Logic High or Low	$I_{INH\_}$, $I_{INL\_}$	$V_{IN\_}$ = 0.8V or 2.4V (Note 3)	C, E	-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 3)							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 1.5V, V+ = 2.7V, Figure 3 (Note 3)	+25°C		270	500	ns
			C, E			600	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 1.5V, V+ = 2.7V, Figure 3 (Note 3)	+25°C		40	100	ns
			C, E			120	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM\_}$ = 1.5V, V+ = 2.7V, Figure 4 (Note 3)	+25°C	10	120		ns
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN\_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.
Note 9: -3dB bandwidth is measured relative to 100kHz.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

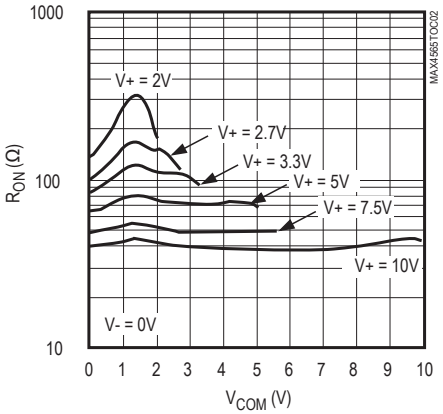
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

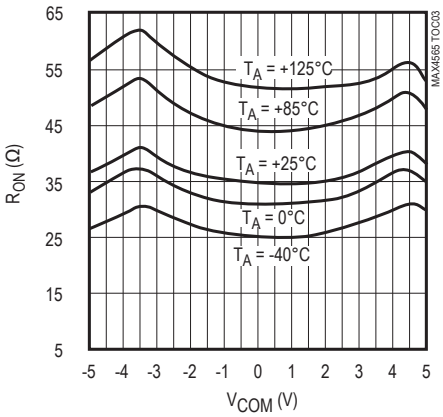
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



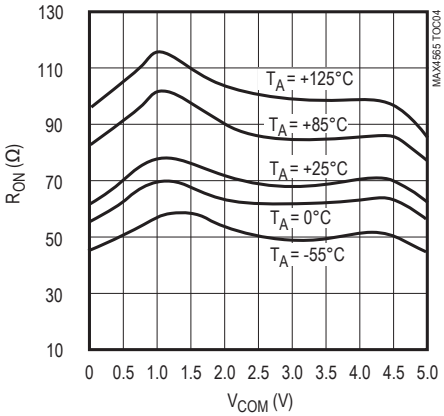
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



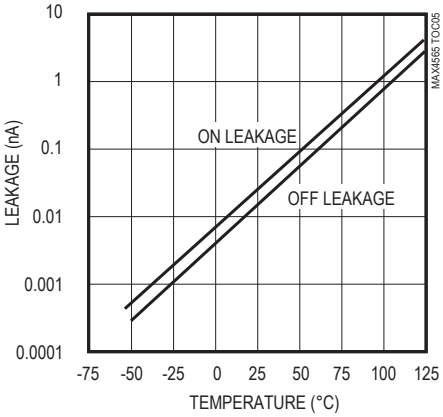
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



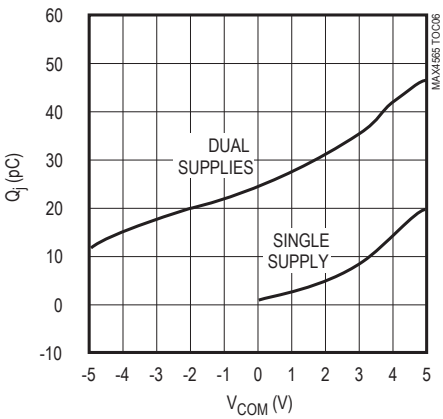
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



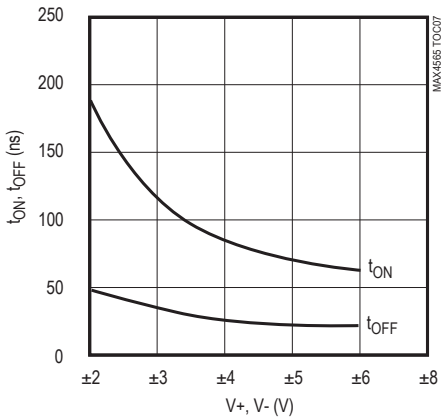
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



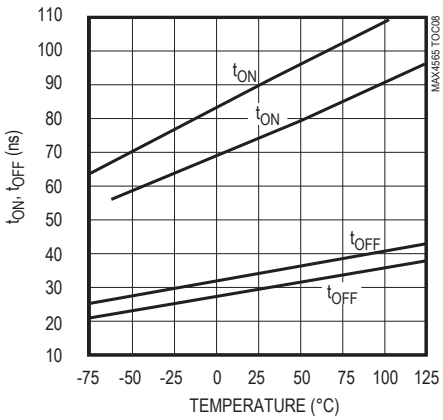
CHARGE INJECTION vs. V_{COM}



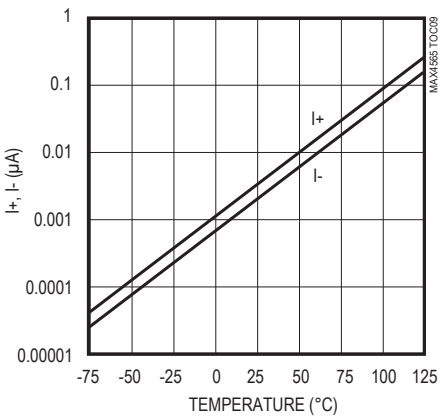
ON/OFF TIME vs. SUPPLY VOLTAGE



ON/OFF TIME vs. TEMPERATURE



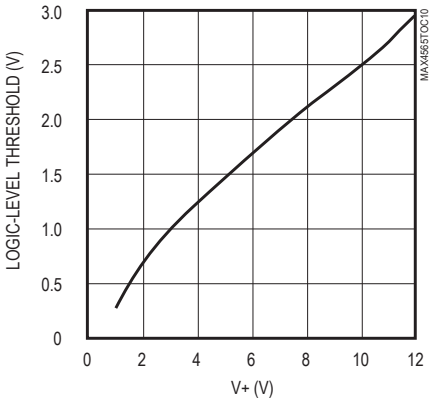
POWER-SUPPLY CURRENT vs. TEMPERATURE



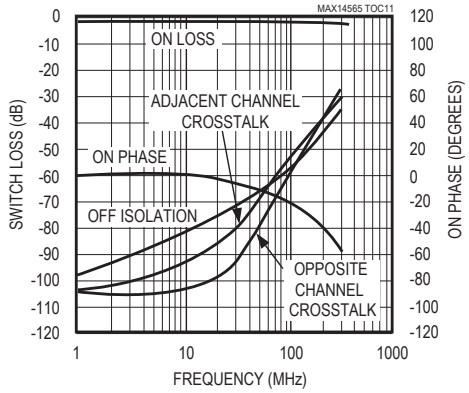
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

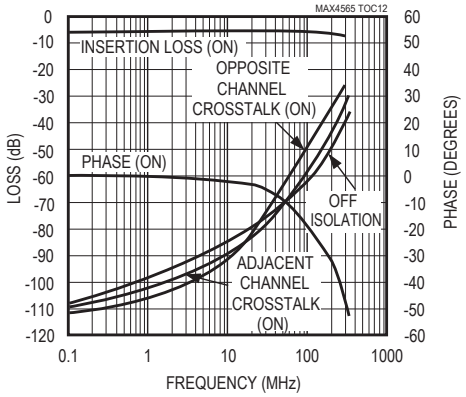
LOGIC-LEVEL THRESHOLD VOLTAGE vs. V+ SUPPLY VOLTAGE



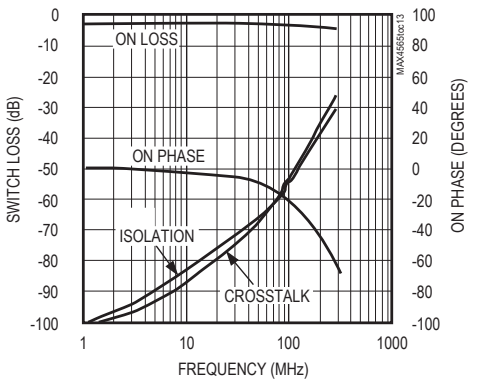
MAX4565 FREQUENCY RESPONSE



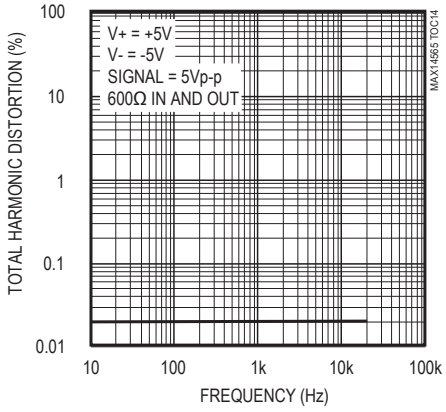
MAX4566 FREQUENCY RESPONSE



MAX4567 FREQUENCY RESPONSE



MAX4567 TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN			NAME	FUNCTION*
MAX4565	MAX4566	MAX4567		
1, 10, 11, 20	1, 16	1, 9	IN_	Digital Control Input
3, 6, 8, 13, 15, 18	3, 7, 10, 14	4, 6, 12, 14	GND_	RF and Logic Ground. Grounds are not internally connected to each other, and should all be connected to a ground plane (see *Grounding* section).
16	12	7, 15	V+	Positive Supply-Voltage Input (analog and digital)
5	5	3, 11	V-	Negative Supply-Voltage Input. Connect to ground plane for single-supply operation.
4, 7, 14, 17	4, 13	2, 16	NO_	Analog Switch Normally Open** Terminals
—	6, 11	8, 10	NC_	Analog Switch Normally Closed** Terminals
2, 9, 12, 19	2, 8, 9, 15	5, 13	COM_	Analog Switch Common** Terminals

* *All pins have ESD diodes to V- and V+.*

** *NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.*

Theory of Operation

The MAX4565/MAX4566/MAX4567 are high-frequency "T" switches. Each "T" switch consists of two series CMOS switches, with a third N-channel switch at the junction that shunts capacitively-coupled signals to ground when the series switches are off. This produces superior high-frequency signal isolation when the switch is turned off.

Logic-Level Translators

The MAX4565/MAX4566/MAX4567 are constructed as high-frequency "T" switches, as shown in Figure 1. The logic-level input, IN_, is translated by amplifier A1 into a V+ to V- logic signal that drives amplifier A2. (Amplifier A2 is an inverter for normally closed switches.) Amplifier A2 drives the gates of N-channel MOSFETs N1 and N2 from V+ to V-, turning them fully on or off. The same signal drives inverter A3 (which drives the P-channel MOSFETs P1 and P2) from V+ to V-, turning them fully on or off, and drives the N-channel MOSFET N3 off and on.

The logic-level threshold is determined by V+ and GND_. The voltage on GND_ is usually at ground potential, but it may be set to any voltage between (V+ - 2V) and V-. When the voltage between V+ and GND_ is less than 2V, the level translators become very slow and unreliable. Since individual switches in each package have individual GND_ pins, they may be set to different voltages. Normally, however, they should all be connected to the ground plane.

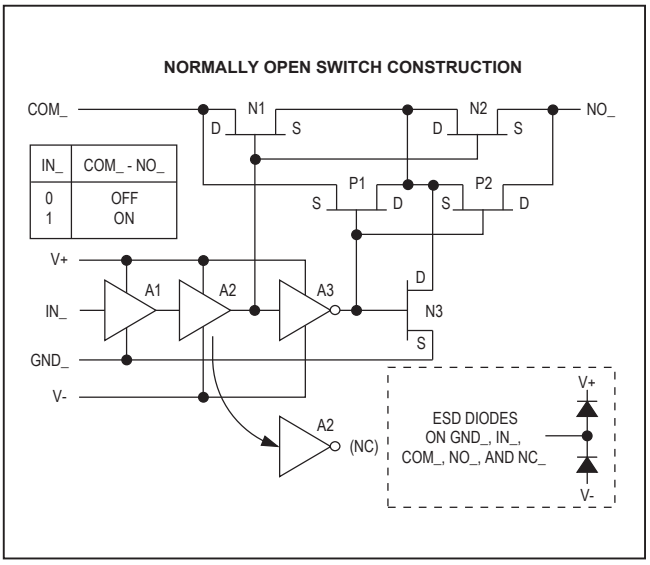


Figure 1. T-Switch Construction

Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off. The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical (i.e., signals may pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small

amount of capacitance to GND_. The four on MOSFETs also have capacitance to ground that, together with the series resistance, forms a lowpass filter. All of these capacitances are distributed evenly along the series resistance, so they act as a transmission line rather than a simple R-C filter. This helps to explain the exceptional 350MHz bandwidth when the switches are on.

Typical attenuation in 50Ω systems is -2.5dB and is reasonably flat up to 300MHz. Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's internal resistance.

The MAX4565/MAX4566/MAX4567 are optimized for ±5V operation. Using lower supply voltages or a single supply increases switching time, increases on-resistance (and therefore on-state attenuation), and increases nonlinearity.

Switch Off Condition

When the switch is off, MOSFETs N1, N2, P1, and P2 are off and MOSFET N3 is on. The signal path is through the off-capacitances of the series MOSFETs, but it is shunted to ground by N3. This forms a highpass filter whose exact characteristics are dependent on the source and load impedances. In 50Ω systems, and below 10MHz, the attenuation can exceed 80dB. This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout have a major role in determining overall performance.

Applications Information

Power-Supply Considerations

Overview

The MAX4565/MAX4566/MAX4567 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. All pins have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog signal voltage.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly; when V+ reaches +12V, the level threshold is about 3.1V, which is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar-Supply Operation

The MAX4565/MAX4566/MAX4567 operate with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4565/MAX4566/MAX4567 V+ pin to +3V and connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs can exceed the absolute maximum ratings, causing damage to the part and/or external circuits.**

CAUTION:

The absolute maximum V+ to V- differential voltage is 13.0V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4565/MAX4566/MAX4567. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single-Supply Operation

The MAX4565/MAX4566/MAX4567 operate from a single supply between +2.7V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. Note, however, that these parts are optimized for ±5V operation, and most AC and DC characteristics are degraded significantly when departing from ±5V. As the overall supply voltage (V+ to V-) is lowered, switching speed, on-resistance, off isolation, and distortion are degraded. (See *Typical Operating Characteristics*.)

Single-supply operation also limits signal levels and interferes with grounded signals. When V- = 0V, AC signals are limited to -0.3V. Voltages below -0.3V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

Power Off

When power to the MAX4565/MAX4566/MAX4567 is off (i.e., V+ = 0V and V- = 0V), the *Absolute Maximum Ratings* still apply. This means that neither logic-level inputs on IN_ nor signals on COM_, NO_, or NC_ can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, and the parts can be damaged if excessive current flows.

Grounding

DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. **For most applications, a ground plane is strongly recommended, and all GND_ pins should be connected to it with solid copper.** While the V+ and V- power-supply pins are common to all switches in a given package, each switch has separate ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance and provides added flexibility in some applications, but it can cause problems if it is overlooked. All the GND_ pins have ESD diodes to V+ and V-.

In systems that have separate digital and analog (signal) grounds, connect these switch GND_ pins to analog ground. Preserving a good signal ground is much more important than preserving a digital ground.

The logic-level inputs, IN_, have voltage thresholds determined by V+ and GND_. (V- does not influence the logic-level threshold.) With +5V and 0V applied to V+ and GND_, the threshold is about 1.6V, ensuring compatibility with TTL- and CMOS-logic drivers.

The various GND_ pins can be connected to separate voltage potentials if any or all of the logic-level inputs is not a normal logic signal. (The GND_ voltages cannot exceed (V+ - 2V) or V-.) Elevating GND_ reduces off isolation. For example, using the MAX4565, if GND2–GND6 are connected to 0V and GND1 is connected to V-, then switches 2, 3, and 4 would be TTL/CMOS compatible, but switch 1 (IN1) could be driven with the rail-to-rail output of an op amp operating from V+ and V-. Note, however, that IN_ can be driven more negative than GND_, as far as V-. GND_ does not have to be removed from 0V when IN_ is driven from bipolar sources, but the voltage on IN_ should never exceed V-. GND_ should be separated from 0V only if the logic-level threshold has to be changed.

Any GND_ pin not connected to 0V should be bypassed to the ground plane with a surface-mount 10nF capacitor to maintain good RF grounding. DC current in the IN_ and GND_ pins is less than 1nA, but increases with switching frequency.

On the MAX4565 only, two extra ground pins—GND5 and GND6—are provided to improve isolation and crosstalk. They are not connected to the logic-level circuit. These pins should always be connected to the ground plane with solid copper.

AC Ground and Bypassing

A ground plane is mandatory for satisfactory high-frequency operation. (Prototyping using hand wiring or wire-wrap boards is strongly discouraged.) Connect all 0V GND_ pins to the ground plane with solid copper. (The GND_ pins extend the high-frequency ground through the package wire-frame, into the silicon itself, thus improving isolation.) The ground plane should be solid metal underneath the device, without interruptions. There should be no traces under the device itself. **For DIP packages, this applies to both sides of a two-sided board.** Failure to observe this will have a minimal effect on the “on” characteristics of the switch at high frequencies, but it will degrade the off isolation and crosstalk.

Bypass all V+ and V- pins to the ground plane with surface-mount 10nF capacitors. For DIP packages, mount the capacitors as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors.

For surface-mount packages, bypass capacitors should be mounted on the opposite side of the board from the device. In this case, use short feedthroughs or vias, directly under the V+ and V- pins. Any GND_ pin not connected to 0V should be similarly bypassed. If V is 0V, connect it directly to the ground plane with solid copper. Keep all leads short.

The MAX4567 has two V+ and two V- pins. Make DC connections to only one of each to minimize crosstalk. Do not route DC current into one of the V+ or V- pins and out the other V+ or V- pin to other devices. The second set of V+ and V- pins is for AC bypassing only.

For dual-supply operation, the MAX4567 should have four 10nF bypass capacitors connected to each V+ and V- pin as close to the package as possible. For single-supply operation, the MAX4567 should have two 10nF bypass capacitors connected (one to each V+ pin) as close to the package as possible.

On the MAX4565, GND5 and GND6 should always be connected to the ground plane with solid copper to improve isolation and crosstalk.

Signal Routing

Keep all signal leads as short as possible. Separate all signal leads from each other and other traces with the ground plane on both sides of the board. Where possible, use coaxial cable instead of printed circuit board traces.

Board Layout

IC sockets degrade high-frequency performance and should not be used if signal bandwidth exceeds 5MHz. Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Such grounds tend to be wedge-shaped as they get closer to the device. Use vias to connect the ground planes on each side of the board, and place the vias in the apex of the wedge-shaped grounds that separate signal leads. Logic-level signal lead placement is not critical.

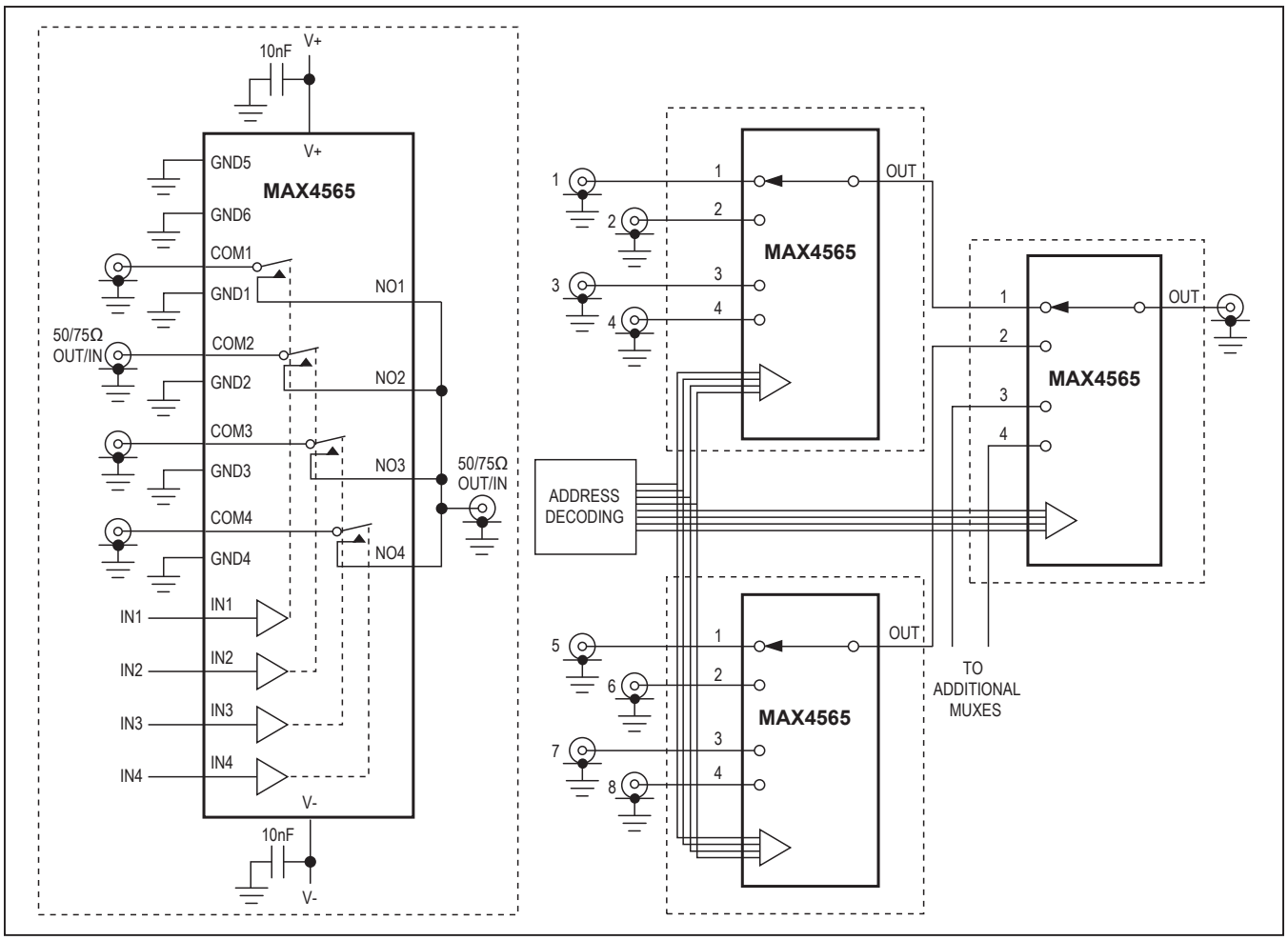


Figure 2. 4-Channel Multiplexer

Multiplexer

With its excellent off isolation, the MAX4565 is ideal for use in high-frequency video multiplexers. Figure 2 shows such an application for switching any one of four video inputs to a single output. The same circuit may be used as a demultiplexer by simply reversing the signal direction.

Stray capacitance of traces and the output capacitance of switches placed in parallel reduces bandwidth, so the outputs of no more than four individual switches should be placed in parallel to maintain a high bandwidth. If more than four mux channels are needed, the 4-channel circuit should be duplicated and cascaded.

Test Circuits/Timing Diagrams

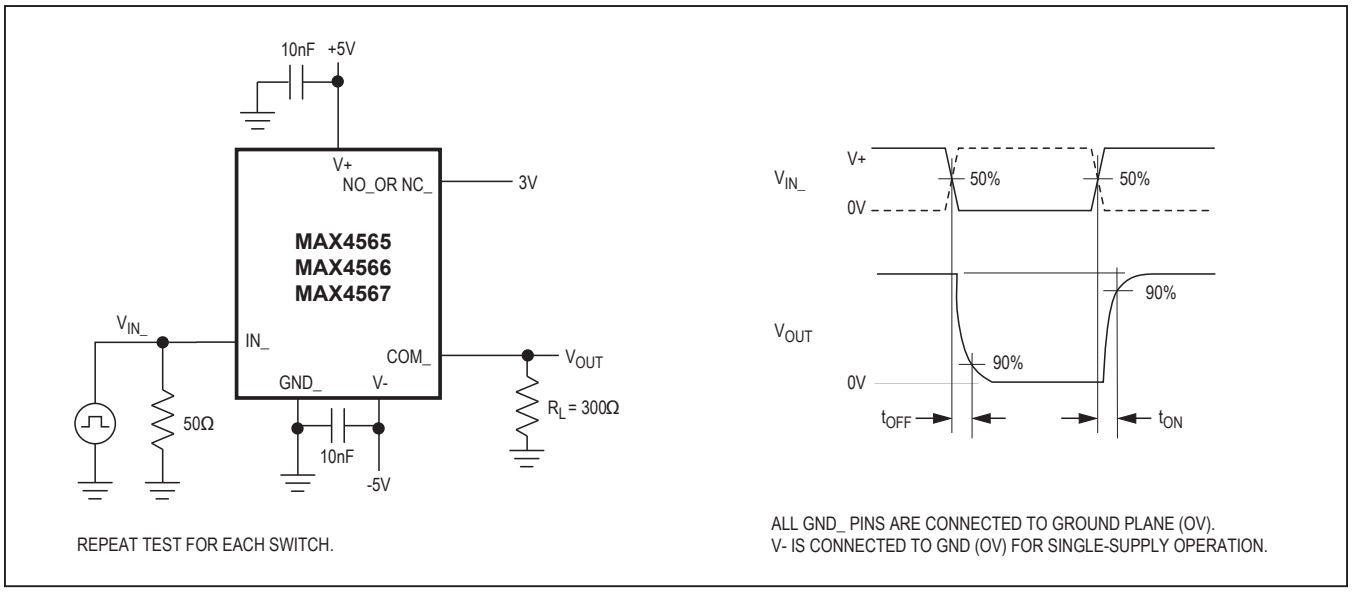


Figure 3. Switching Time

Test Circuits/Timing Diagrams (continued)

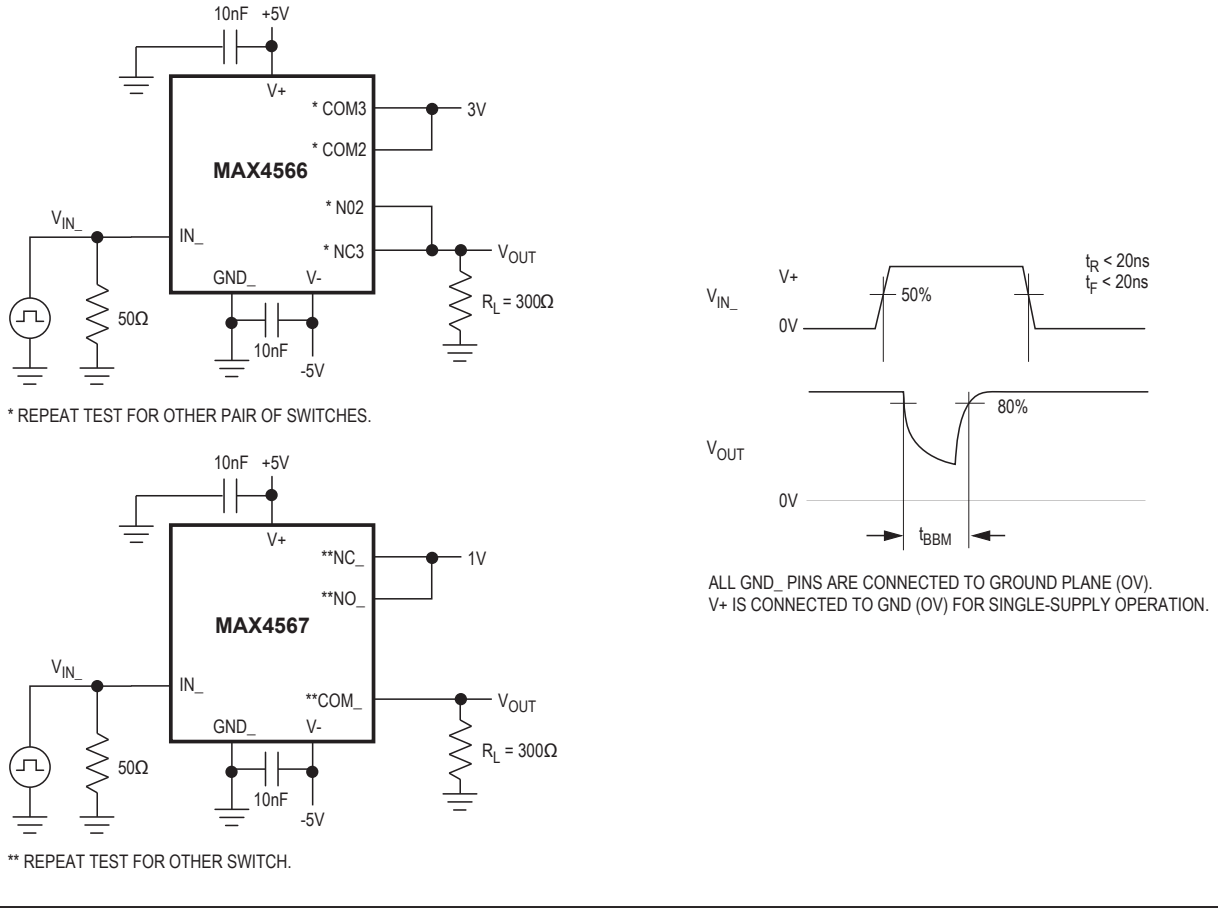


Figure 4. Break-Before-Make Interval (MAX4566/MAX4567 only)

Test Circuits/Timing Diagrams (continued)

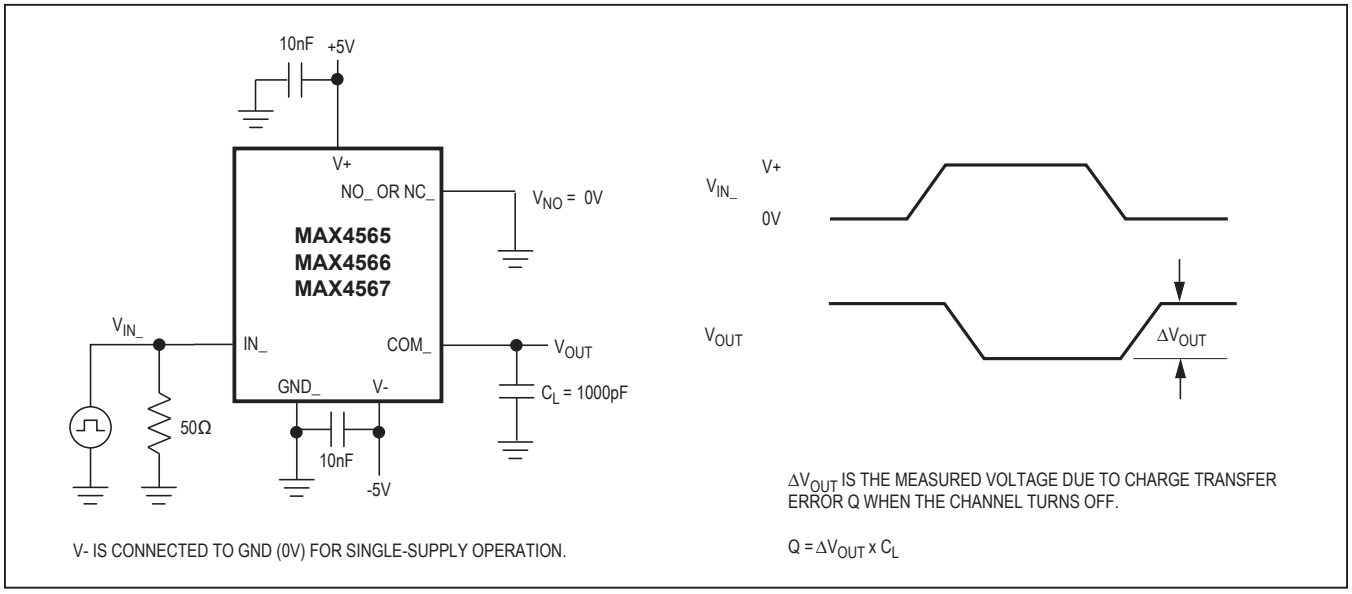


Figure 5. Charge Injection

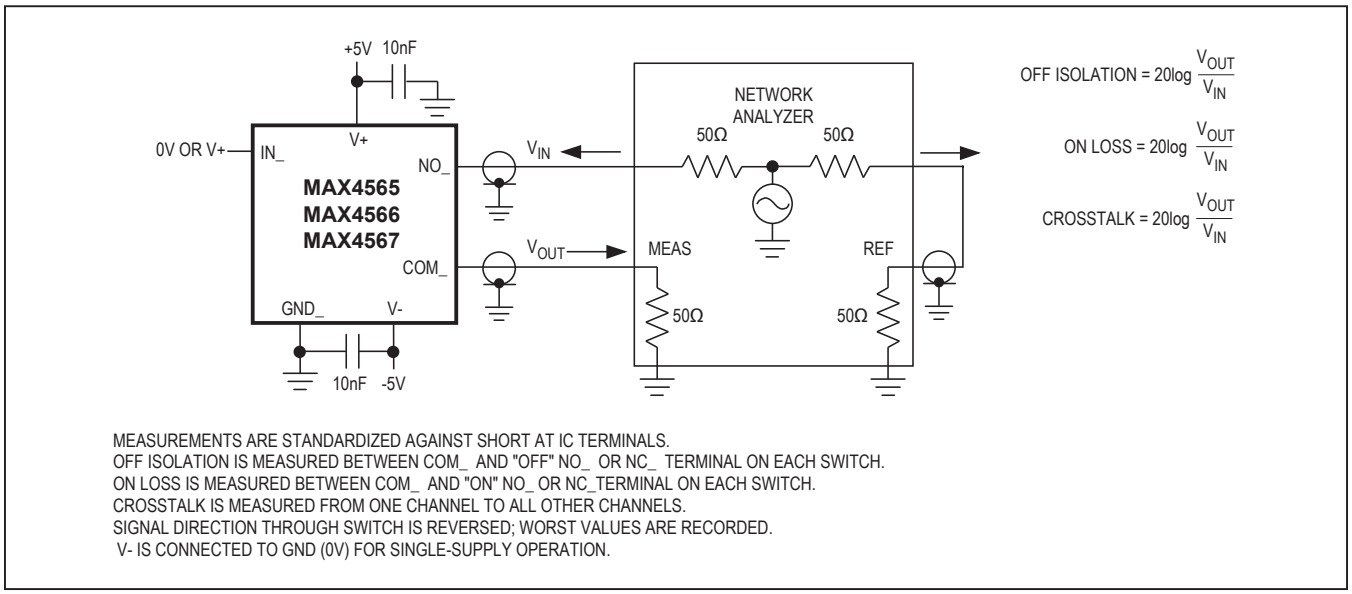


Figure 6. On Loss, Off Isolation, and Crosstalk

Test Circuits/Timing Diagrams (continued)

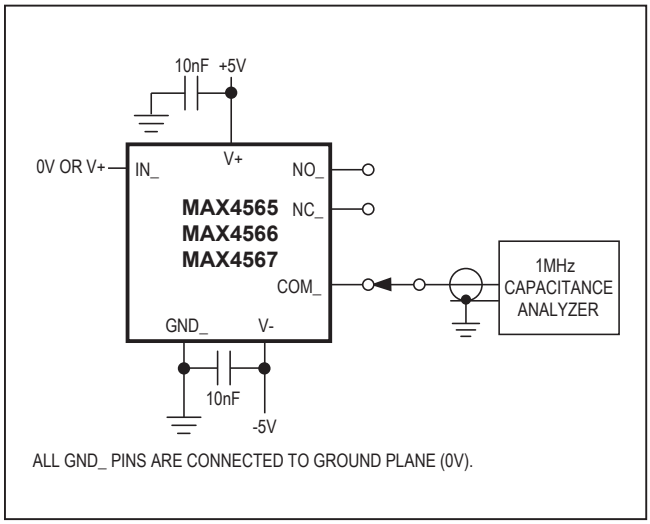
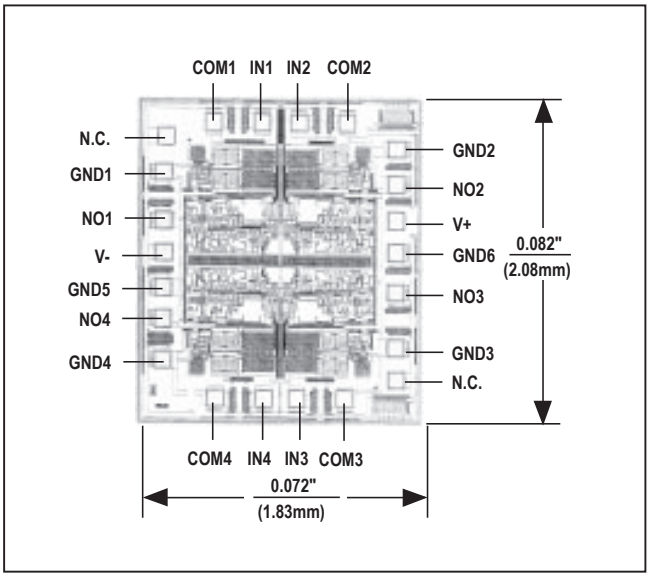


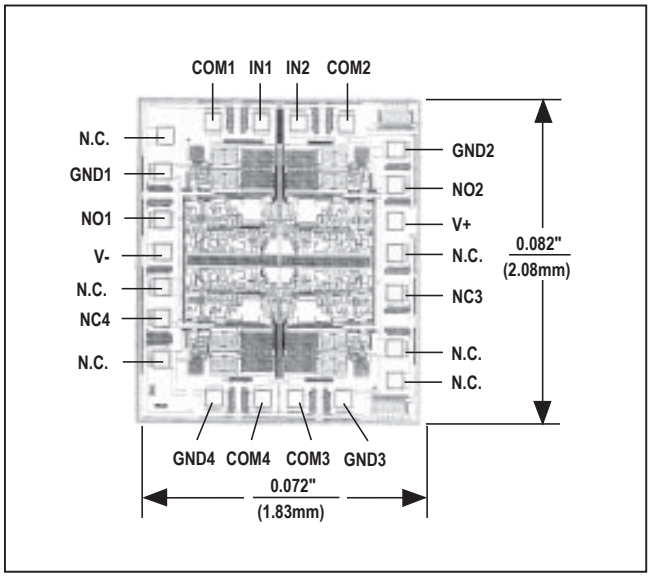
Figure 7. NO_, NC_, COM_ Capacitance

Chip Topographies

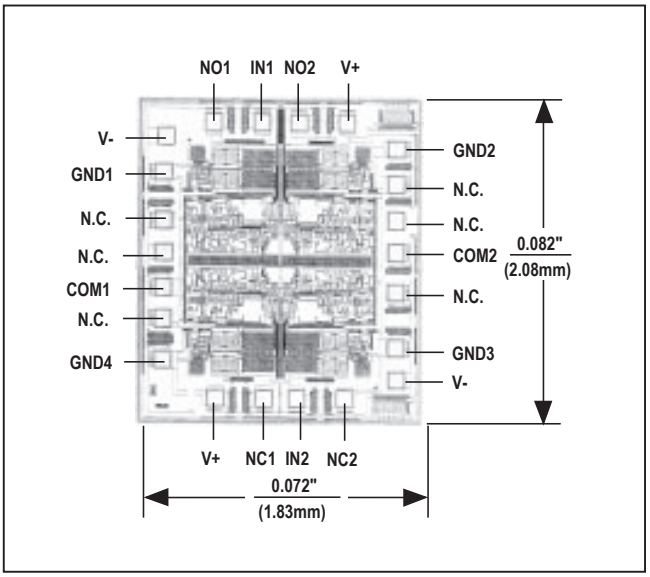
MAX4565



MAX4566



MAX4567



TRANSISTOR COUNT: 257
SUBSTRATE INTERNALLY CONNECTED TO V+

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4565CAP	0°C to +70°C	20 SSOP
MAX4565C/D	0°C to +70°C	Dice*
MAX4565EPP	-40°C to +85°C	20 Plastic DIP
MAX4565EWP	-40°C to +85°C	20 Wide SO
MAX4565EAP	-40°C to +85°C	20 SSOP
MAX4566CPE	0°C to +70°C	16 Plastic DIP
MAX4566CSE	0°C to +70°C	16 Narrow SO
MAX4566CEE	0°C to +70°C	16 QSOP
MAX4566C/D	0°C to +70°C	Dice*
MAX4566EPE	-40°C to +85°C	16 Plastic DIP
MAX4566ESE	-40°C to +85°C	16 Narrow SO
MAX4566EEE	-40°C to +85°C	16 QSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX4567CPE	0°C to +70°C	16 Plastic DIP
MAX4567CSE	0°C to +70°C	16 Narrow SO
MAX4567CEE	0°C to +70°C	16 QSOP
MAX4567C/D	0°C to +70°C	Dice*
MAX4567EPE	-40°C to +85°C	16 Plastic DIP
MAX4567ESE	-40°C to +85°C	16 Narrow SO
MAX4567EEE	-40°C to +85°C	16 QSOP
MAX4565CWP+	0°C to +70°C	20 Wide SO
MAX4565CWP+T	0°C to +70°C	20 Wide SO
MAX4565EWP+	-40°C to +85°C	20 Wide SO
MAX4565EWP+T	-40°C to +85°C	20 Wide SO
MAX4565ESE+T	-40°C to +85°C	16 Narrow SO

**Contact factory for dice specifications.*

Package Information

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 SSOP	A20+5	21-0056	90-0094
20 SOIC (W)	W20+2	21-0042	90-0108
20 PDIP	P20+4	21-0043	NOT AVAILABLE
16 SOIC (N)	S16+1	21-0041	90-0097
16 QSOP	E16+1	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/97	Initial Release.	—
1	2/21	Added new packages to *Ordering Information*, added *Package Information* and *Revision History*.	1, 16

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