THE DATASHEET OF

MAX32630IWG+

MAX32630/MAX32631

Ultra-Low Power, High-Performance Cortex-M4F Microcontroller for Wearables

General Description

The MAX32630/MAX32631 is an ARM® Cortex® -M4F 32-bit microcontroller with a floating point unit, ideal for the emerging category of wearable medical and fitness applications. The architecture combines ultra-low power high-efficiency signal processing functionality with significantly reduced power consumption and ease of use. The device features four powerful and flexible power modes. A peripheral management unit (PMU) enables intelligent peripheral control with up to six channels to significantly reduce power consumption. Built-in dynamic clock gating and firmware-controlled power gating allows the user to optimize power for the specific application. Multiple SPI, UART and I2C serial interfaces, as well as 1-Wire® master and USB, allow for interconnection to a wide variety of external sensors. A four-input, 10-bit ADC with selectable references is available to monitor analog input from external sensors and meters. The small 100-ball WLP package provides a tiny, 4.37mm x 4.37mm footprint.

The MAX32630/MAX32631 include a hardware AES engine. The MAX32631 is a secure version of the MAX32630. It incorporates a trust protection unit (TPU) with encryption and advanced security features. These features include a modular arithmetic accelerator (MAA) for fast ECDSA, a hardware PRNG entropy generator, and a secure boot loader.

Applications

- Sports Watches
- Fitness Monitors
- Wearable Medical Patches
- Portable Medical Devices
- Sensor Hubs

Ordering Information appears at end of data sheet.

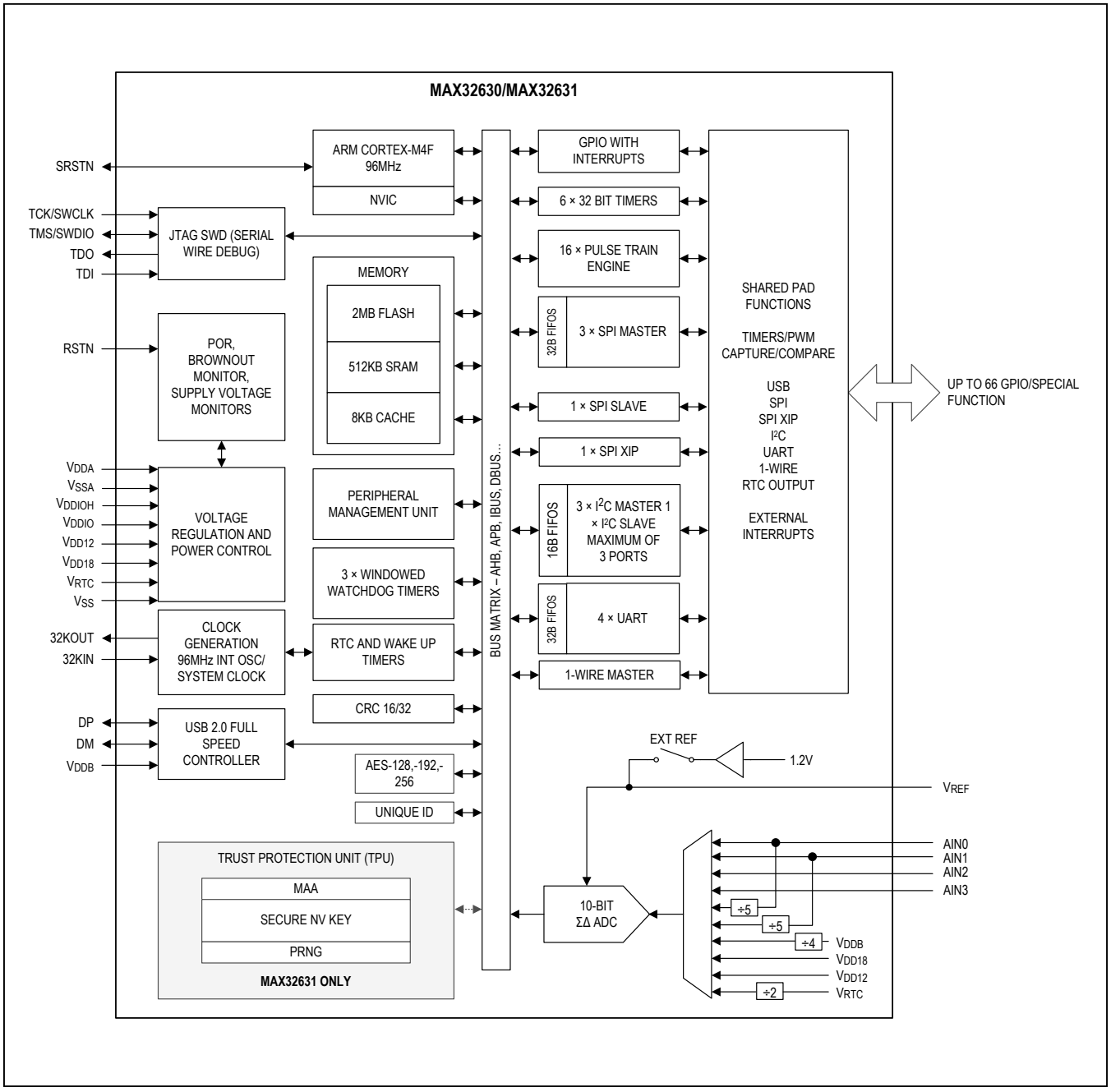
Benefits and Features

- High-Efficiency Microcontroller for Wearable Devices
  - Internal Oscillator Operates Up to 96MHz
  - Low Power 4MHz Oscillator System Clock Option for Always-On Monitoring Applications
  - 2MB Flash Memory
  - 512KB SRAM
  - 8KB Instruction Cache
  - 1.2V Core Supply Voltage
  - 1.8V to 3.3V I/O
  - Optional 3.3V ±5% USB Supply Voltage
- Power Management Maximizes Uptime for Battery Applications
  - 106µA/MHz Active Current Executing from Cache
  - Wakeup to 96MHz Clock or 4MHz Clock
  - 600nA Low Power Mode (LP0) Current with RTC Enabled
  - 3.5µW Ultra-Low Power Data Retention Sleep Mode (LP1) with Fast 5µs Wakeup to 96MHz
- Optimal Peripheral Mix Provides Platform Scalability
  - SPIX Execute in Place (XIP) Engine for Memory Expansion with Minimal Footprint
  - Three SPI Masters, One SPI Slave
  - Four UARTs
  - Three I2C Masters, One I2C Slave
  - 1-Wire Master
  - Full-Speed USB 2.0 Engine with Internal Transceiver
  - Sixteen Pulse Train (PWM) Engines
  - Six 32-Bit Timers and 3 Watchdog Timers
  - Up to 66 General-Purpose I/O Pins
  - One 10-Bit Delta-Sigma ADC Operating at 7.8ksps
  - AES-64, -128, -256
  - CMOS-Level 32kHz RTC Output
- Secure Valuable IP and Data with Robust Internal Hardware Security (MAX32631 Only)
  - Trust Protection Unit (TPU) Including MAA Supports ECDSA and Modular Arithmetic
  - PRNG Seed Generator
  - Secure Boot Loader

19-8478; Rev 0; 3/16

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.)

V_{DD18} .....-0.3V to +1.89V
V_{DD12} .....-0.3V to +1.26V
V_{DDA} relative to V_{SSA} .....-0.3V to +1.89V
V_{RTC} .....-0.3V to +1.89V
V_{DDB} .....-0.3V to +3.6V
V_{REF} .....-0.3V to +3.6V
32KIN, 32KOUT.....-0.3V to +3.6V
RSTN, SRSTN, DP, DM, GPIO, JTAG .....-0.3V to +3.6V
AIN[1:0].....-0.3V to +5.5V
AIN[3:2].....-0.3V to +3.6V
V_{DDIO} .....-0.3V to +3.6V
V_{DDIOH} .....-0.3V to +3.6V
Total Current into All V_{DD18} Power Pins (sink) 100mA
Total Current into V_{SS} 100mA
Output Current (sink) by Any I/O Pin.....25mA
Output Current (source) by Any I/O Pin .....-25mA
Operating Temperature Range..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

100 WLP

Package Code	W1004D4+1
Outline Number	21-0452
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Single-Layer Board	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board	
Junction-to-Ambient (θ_{JA})	38.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD18}		1.71	1.8	1.89	V
	V_{DD12}		1.14	1.2	1.26	
	V_{DDA}		1.71	1.8	1.89	
	V_{RTC}		1.75	1.8	1.89	
	V_{DDIO}		1.71	1.8	3.6	
	V_{DDIOH}	V_{DDIOH} must be ≥ V_{DDIO}	1.71	1.8	3.6	
Power Fail Reset Voltage	V_{RST}	Monitors V_{DD18}	1.62		1.7	V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD18}		1.5		V
RAM Data Retention Voltage	V_{DRV}			0.93		V
V_{DD12} Dynamic Current, LP3 Mode	I_{DD12_DLP3}	Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, PMU disabled		106		µA/MHz
V_{DD12} Fixed Current, LP3 Mode	I_{DD12_FLP3}	Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, 96MHz oscillator selected as system clock		173		µA
		Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, 4MHz oscillator selected as system clock		72		
V_{DD18} Fixed Current, LP3 Mode	I_{DD18_FLP3}	Measured on the V_{DD18} + V_{DDA} device pins and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, 96MHz oscillator selected as system clock		366		µA
		Measured on the V_{DD18} + V_{DDA} device pins and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, 4MHz oscillator selected as system clock		33		
V_{DD12} Dynamic Current, LP2 Mode	I_{DD12_DLP2}	Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		27		µA/MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD12} Fixed Current, LP2 Mode	I_{DD12_FLP2}	Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active, 96MHz oscillator selected as system clock		173		µA
		Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active, 4MHz oscillator selected as system clock		72		
V_{DD18} Fixed Current, LP2 Mode	I_{DD18_FLP2}	Measured on the V_{DD18} + V_{DDA} device pins, ARM in sleep mode, PMU with two channels active, 96MHz oscillator selected as system clock		366		µA
		Measured on the V_{DD18} + V_{DDA} device pins. ARM in sleep mode, PMU with two channels active, 4MHz oscillator selected as system clock		33		
V_{DD12} Fixed Current, LP1 Mode	I_{DD12_FLP1}	Standby state with full data retention		1.86		µA
V_{DD18} Fixed Current, LP1 Mode	I_{DD18_FLP1}	Standby state with full data retention		120		nA
V_{RTC} Fixed Current, LP1 Mode	I_{DDRTC_FLP1}	RTC enabled, retention regulator powered by V_{DD12}		505		nA
V_{DD12} Fixed Current, LP0 Mode	I_{DD12_FLP0}			14		nA
V_{DD18} Fixed Current, LP0 Mode	I_{DD18_FLP0}			120		nA
V_{RTC} Fixed Current, LP0 Mode	I_{DDRTC_FLP0}	RTC enabled		505		nA
		RTC disabled		105		
LP2 Mode Resume Time	t_{LP2_ON}			0		µs
LP1 Mode Resume Time	t_{LP1_ON}			5		µs
LP0 Mode Resume Time	t_{LP0_ON}	Polling flash ready		11		µs
JTAG						
Input Low Voltage for TCK, TMS, TDI	V_{IL}				0.3 x V_{DDIO}	V
Input High Voltage for TCK, TMS, TDI	V_{IH}		0.7 x V_{DDIO}			V
Output Low Voltage for TDO	V_{OL}			0.2	0.4	V
Output High Voltage for TDO	V_{OH}		V_{DDIO} - 0.4			

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKS						
System Clock Frequency	f_{CK}		0.001		98	MHz
System Clock Period	t_{CK}			$1/f_{CK}$		ns
Internal Relaxation Oscillator Frequency	f_{INTCLK}	Factory default	94	96	98	MHz
		Firmware trimmed, required for USB compliance	95.76	96	96.24	
Internal RC Oscillator Frequency	f_{RCCLK}		3.9	4	4.1	MHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal		32.768		kHz
RTC Operating Current	I_{RTC_LP23}	LP2 or LP3 mode		0.7		µA
	I_{RTC_LP01}	LP0 or LP1 mode		0.35		
RTC Power-Up Time	t_{RTC_ON}			250		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO Pins	V_{IL}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
		V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	
Input Low Voltage for RSTN	V_{IL}				0.3 x V_{RTC}	V
Input Low Voltage for SRSTN	V_{IL}				0.3 x V_{DDIO}	
Input High Voltage for All GPIO Pins	V_{IH}	V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
		V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
Input High Voltage for RSTN	V_{IH}		0.7 x V_{RTC}			V
Input High Voltage for SRSTN	V_{IH}		0.7 x V_{DDIO}			V
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Output Low Voltage for All GPIO Pins	V_{OL}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, I_{OL} = 4mA, normal drive configuration		0.2	0.4	V
		V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, I_{OL} = 24mA, fast drive configuration		0.2	0.4	
		V_{DDIO} = 1.71V V_{DDIOH} = 2.97V, V_{DDIOH} selected as I/O supply, I_{OL} = 300µA		0.2	0.45	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined I_{OL}, All GPIO Pins	I_{OL_TOTAL}				48	mA
Output High Voltage for All GPIO Pins	V_{OH}	I_{OH} = -2mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, normal drive configuration	V_{DDIO} - 0.4			V
		I_{OH} = -8mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, fast drive configuration	V_{DDIO} - 0.4			
		I_{OH} = -300µA, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply	V_{DDIOH} - 0.45			
Ouput High Voltage for All GPIO Pins	V_{OH}	V_{DDIO} = 1.71V, V_{DDIOH} = 3.6V. V_{DDIO} selected as I/O supply, I_{OH} = -2mA	V_{DDIO} - 0.45			V
Combined I_{OH}, All GPIO Pins	I_{OH_TOTAL}				-48	mA
Input/Output Pin Capacitance for All Pins	C_{IO}			3		pF
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-100		+100	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor RSTN, SRSTN, TMS, TCK, TDI	R_{PU}			25		kΩ
Input Pullup/Pulldown Resistor for All GPIO Pins	R_{PU1}	Normal resistance		25		kΩ
	R_{PU2}	Highest resistance		1		MΩ
FLASH MEMORY						
Page Size		2MB flash		8		kB
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time per Word	t_{PROG}			60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years

ADC Electrical Characteristics

(Internal bandgap reference selected, ADC_SCALE = ADC_REFSCL = 1, unless otherwise specified. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution				10		Bits
ADC Clock Rate	f_{ACLK}		0.1		8	MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 0	0.05		V_{DDA} - 0.05	V
		AIN[1:0], ADC_CHSEL = 4–5, BUF_BYPASS = 0	0.05		5.5	
		AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 1	V_{SSA}		V_{DDA}	
		AIN[1:0], ADC_CHSEL = 4–5, BUF_BYPASS = 1	V_{SSA}		5.5	
Input Impedance	R_{AIN}	AIN[1:0], ADC_CHSEL = 4-5, ADC active		45		kΩ
Input Dynamic Current	I_{AIN}	Switched capactiance input current, ADC active, ADC buffer bypassed		4.5		µA
		Switched capacitance input current, ADC active, ADC buffer enabled		50		nA
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		1		pF
		Dynamically switched capacitance		250		fF
Integral Nonlinearity	INL				±2	LSb
Differential Nonlinearity	DNL				±1	LSb
Offset Error	V_{OS}			±1		LSb
Gain Error	GE			±2		LSb
Signal to Noise Ratio	SNR			58.5		dB
Signal to Noise and Distortion	SINAD			58.5		dB
Total Harmonic Distortion	THD			68.5		dB
Spurious Free Dynamic Range	SFDR			74		dB
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		240		µA
Input Buffer Active Current	I_{INBUF}			53		µA

ADC Electrical Characteristics (continued)

(Internal bandgap reference selected, ADC_SCALE = ADC_REFSCL = 1, unless otherwise specified. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Setup Time	t_{ADC_SU}	Any powerup of: ADC clock, ADC bias, reference buffer or input buffer to CpuAdcStart			10	µs
		Any power-up of: ADC clock or ADC bias to CpuAdcStart			48	t_{ACLK}
ADC Output Latency	t_{ADC}			1025		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.12	4	nA
		AIN2 or AIN3, ADC inactive or channel not selected.		0.02	1	
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
External Reference Voltage	V_{REF_EXT}	ADC_XREF = 1	1.17	1.23	1.29	V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm
Reference Dynamic Current	I_{REF_EXT}	ADC_XREF = 1, ADC active		4.1		µA
Reference Input Capacitance	C_{REFIN}	Dynamically switched capacitance, ADC_XREF = 1, ADC active		250		fF

SPI MASTER/SPIX MASTER Electrical Characteristics

(Guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{MCK}				48	MHz
SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MISO Input Valid to SCLK Sample Edge Setup	t_{MIS}		3			ns
MISO Input to SCLK Sample Edge	t_{MIH}			0		ns

SPI Timing:

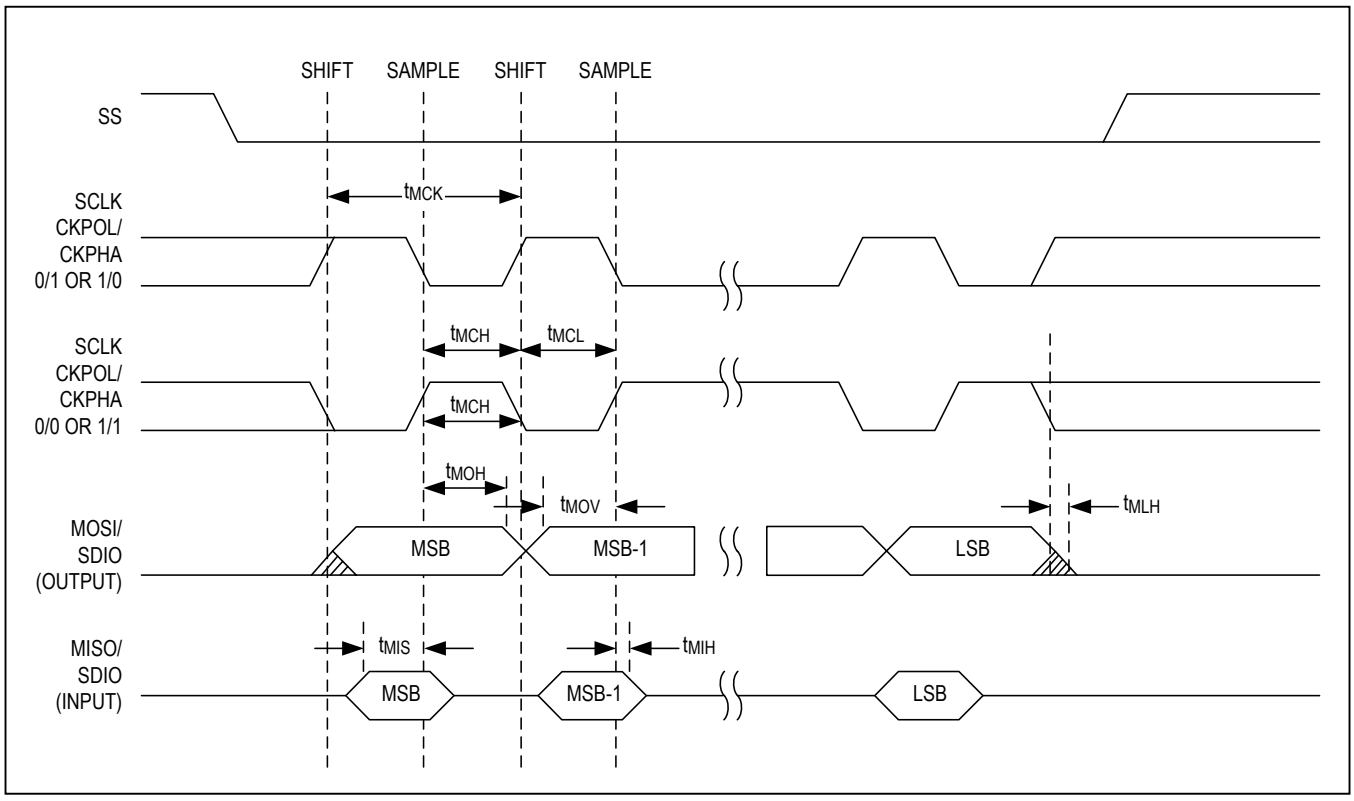


Figure 1. SPI Master/SPIX Master Communications Timing Diagram

USB Electrical Characteristics

(Guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB PHY Supply Voltage	V_{DDB}		2.97	3.3	3.63	V
Single-Ended Input High Voltage DP, DM	V_{IHD}		2			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to V_{SS}	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pull-up Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.09	

USB Timing Electrical Characteristics

(AC Electrical Specifications are guaranteed by design and are not production tested, V_{DD18}= V_{RST} to 1.89V, V_{DDB} = 3.63V, T_A=-20°C to +85°C, Guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R,t_F	C_L = 50pF	90		110	%

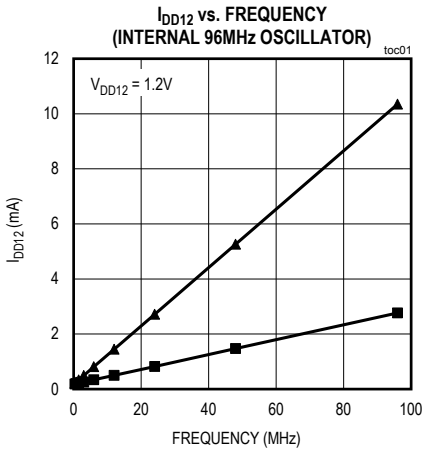
Electrical Characteristics - I²C BUS

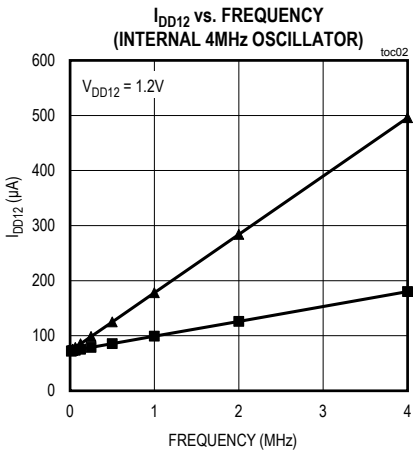
(Guaranteed by design and not production tested.)

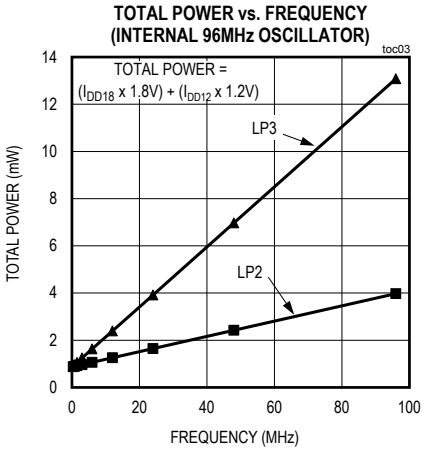
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode		100		kHz
		Fast mode		400		
Input High Voltage	V_{IH_I2C}	Fast mode, V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
		Fast mode, V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
		Standard mode, V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			
		Standard mode, V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
Input Low Voltage	V_{IL_I2C}	Fast mode, V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
		Fast mode, V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	
		Standard mode, V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	
		Standard mode, V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	Fast-mode		300		mV
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, I_{OL} = 4mA, normal drive configuration		0.2	0.4	V
		V_{DDIO} = 1.71V V_{DDIOH} = 2.97V, V_{DDIOH} selected as I/O supply, I_{OL} = 300µA		0.2	0.45	

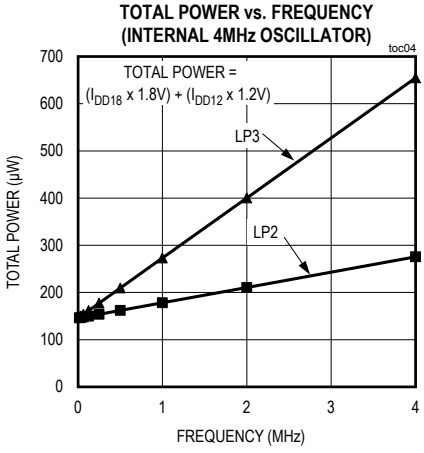
Typical Operating Characteristics

(V_{DD12} = 1.2V, V_{DD18} = 1.8V)









Pin Configuration

100-WLP

TOP VIEW (BUMPS ON BOTTOM)

	1	2	3	4	5	6	7	8	9	10
A	N.C.	V_{DDIOH}	V_{SSA}	V_{REF}	AIN0	AIN1	AIN2	AIN3	V_{DD18}	N.C.
B	P8.1	SRSTN	RSTN	V_{DDA}	TCK	TMS	TDO	TDI	V_{SS}	32KIN
C	P8.0	P0.1	P0.0	P6.0	P5.7	P5.5	P5.4	P5.2	V_{RTC}	32KOUT
D	P7.7	P0.4	P0.5	P0.3	P0.2	P5.6	P5.3	P5.0	V_{DDB}	V_{SS}
E	P7.6	P1.0	P0.7	P0.6	P1.1	P1.5	P3.1	P5.1	DP	V_{DDIO}
F	P7.5	V_{DD12}	P1.3	P1.2	P1.4	P3.0	P3.5	P3.7	DM	P4.7
G	P7.4	V_{SS}	P1.6	P1.7	P2.4	P2.6	P3.4	P4.4	P4.6	P4.5
H	P7.3	V_{DDIO}	P2.1	P2.2	P2.5	P2.7	P3.2	P4.1	P4.3	P4.2
J	P7.2	V_{SS}	P2.0	P2.3	V_{DD18}	V_{SS}	P3.3	P3.6	P4.0	P6.1
K	N.C.	P7.1	P7.0	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	N.C.

Bump Description

BUMP	NAME	FUNCTION
POWER PINS		
D9	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
F2	V_{DD12}	1.2V Nominal Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
C9	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
B4	V_{DDA}	Analog Supply Voltage. This pin must be bypassed to V_{SSA} with a 1.0µF capacitor as close as possible to this pin.
J5, A9	V_{DD18}	1.8V Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
H2, E10	V_{DDIO}	I/O Supply Voltage. 1.8V ≤ V_{DDIO} ≤ 3.6V. See EC table for V_{DDIO} specification. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A2	V_{DDIOH}	I/O Supply Voltage, High. 1.8V ≤ V_{DDIOH} ≤ 3.6V, always with V_{DDIOH} ≥ V_{DDIO}. See EC table for V_{DDIOH} specification. This pin must be bypassed to VSS with a 1.0µF capacitor as close as possible to the package.
A4	V_{REF}	ADC Reference. This pin must be left unconnected if an external reference is not used.
B9, D10, G2, J6, J2	V_{SS}	Digital Ground
A3	V_{SSA}	Analog Ground
CLOCK PINS		
C10	32KOUT	32KHz Crystal Oscillator Output
B10	32KIN	32kHz Crystal Oscillator Input. Connect a 6pF 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected. A 32kHz crystal or external clock source is required for proper USB operation.
USB PINS		
E9	DP	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
F9	DM	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
JTAG PINS		
B5	TCK/SWCLK	JTAG Clock or Serial Wire Debug Clock. This pin has an internal 25KΩ pullup to V_{DDIO}.
B6	TMS/SWDIO	JTAG Test Mode Select or Serial Wire Debug I/O. This pin has an internal 25KΩ pullup to V_{DDIO}.
B7	TDO	JTAG Test Data Output
B8	TDI	JTAG Test Data Input. This pin has an internal 25kΩ pullup to V_{DDIO}.

Bump Description (continued)

BUMP	NAME	FUNCTION
RESET PINS		
B3	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin is internally connected with an internal 25kΩ pullup to the V_{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
B2	SRSTN	Software Reset, Active-Low Input/Output. The device remains in software reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a reset to the ARM core, digital registers and peripherals (resetting most of the core logic on the V_{DD12} supply). This reset does not affect the POR only registers, RTC logic, ARM debug engine or JTAG debugger allowing for a soft reset without having to reconfigure all registers. After the device senses SRSTN as a logic 0, the pin automatically reconfigures as an output sourcing a logic 0. The device continues to output for 6 system clock cycles and then repeats the input sensing/output driving until SRSTN is sensed inactive. This pin is internally connected with an internal 25kΩ pullup to the V_{DDIO} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS (See the *Applications Information* section for GPIO Matrix)		
C3	P0.0	GPIO Port 0.0
C2	P0.1	GPIO Port 0.1
D5	P0.2	GPIO Port 0.2
D4	P0.3	GPIO Port 0.3
D2	P0.4	GPIO Port 0.4
D3	P0.5	GPIO Port 0.5
E4	P0.6	GPIO Port 0.6
E3	P0.7	GPIO Port 0.7
E2	P1.0	GPIO Port 1.0
E5	P1.1	GPIO Port 1.1
F4	P1.2	GPIO Port 1.2
F3	P1.3	GPIO Port 1.3
F5	P1.4	GPIO Port 1.4
E6	P1.5	GPIO Port 1.5
G3	P1.6	GPIO Port 1.6
G4	P1.7	GPIO Port 1.7
J3	P2.0	GPIO Port 2.0
H3	P2.1	GPIO Port 2.1
H4	P2.2	GPIO Port 2.2
J4	P2.3	GPIO Port 2.3
G5	P2.4	GPIO Port 2.4
H5	P2.5	GPIO Port 2.5
G6	P2.6	GPIO Port 2.6

Bump Description (continued)

BUMP	NAME	FUNCTION
H6	P2.7	GPIO Port 2.7
F6	P3.0	GPIO Port 3.0
E7	P3.1	GPIO Port 3.1
H7	P3.2	GPIO Port 3.2
J7	P3.3	GPIO Port 3.3
G7	P3.4	GPIO Port 3.4
F7	P3.5	GPIO Port 3.5
J8	P3.6	GPIO Port 3.6
F8	P3.7	GPIO Port 3.7
J9	P4.0	GPIO Port 4.0
H8	P4.1	GPIO Port 4.1
H10	P4.2	GPIO Port 4.2
H9	P4.3	GPIO Port 4.3
G8	P4.4	GPIO Port 4.4
G10	P4.5	GPIO Port 4.5
G9	P4.6	GPIO Port 4.6
F10	P4.7	GPIO Port 4.7
D8	P5.0	GPIO Port 5.0
E8	P5.1	GPIO Port 5.1
C8	P5.2	GPIO Port 5.2
D7	P5.3	GPIO Port 5.3
C7	P5.4	GPIO Port 5.4
C6	P5.5	GPIO Port 5.5
D6	P5.6	GPIO Port 5.6
C5	P5.7	GPIO Port 5.7
C4	P6.0	GPIO Port 6.0
J10	P6.1	GPIO Port 6.1
K9	P6.2	GPIO Port 6.2
K8	P6.3	GPIO Port 6.3
K7	P6.4	GPIO Port 6.4
K6	P6.5	GPIO Port 6.5
K5	P6.6	GPIO Port 6.6
K4	P6.7	GPIO Port 6.7
K3	P7.0	GPIO Port 7.0
K2	P7.1	GPIO Port 7.1
J1	P7.2	GPIO Port 7.2
H1	P7.3	GPIO Port 7.3
G1	P7.4	GPIO Port 7.4
F1	P7.5	GPIO Port 7.5

Bump Description (continued)

BUMP	NAME	FUNCTION
E1	P7.6	GPIO Port 7.6
D1	P7.7	GPIO Port 7.7
C1	P8.0	GPIO Port 8.0
B1	P8.1	GPIO Port 8.1
A1	N.C.	Not Connected.
A10	N.C.	Not Connected.
K1	N.C.	Not Connected.
K10	N.C.	Not Connected.
ANALOG INPUT PINS		
A5	AIN0	ADC Input 0. 5V tolerant input.
A6	AIN1	ADC Input 1. 5V tolerant input.
A7	AIN2	ADC Input 2
A8	AIN3	ADC Input 3

Detailed Description

The MAX32630/MAX32631 is a low-power, mixed signal microcontroller based on the ARM Cortex-M4 32-bit core with a maximum operating frequency of 96MHz. The MAX32631 is a secure version of the MAX32630, incorporating a trust protection unit (TPU) with encryption and advanced security features.

Application code executes from an onboard 2MB program flash memory, with up to 512KB SRAM available for general application use. An 8KB instruction cache improves execution throughput, and a transparent code scrambling scheme is used to protect customer intellectual property residing in the program flash memory. Additionally, a SPI execute in place (XIP) external memory interface allows application code and data (up to 16MB) to be accessed from an external SPI memory device.

A 10-bit delta-sigma ADC is provided with a multiplexer front end for four external input channels (two of which are 5V tolerant) and six internal channels. An onboard temperature sensor block allows direct die temperature measurement without requiring any external system components. Dedicated divided supply input channels allow direct monitoring of onboard power supplies such as V_{DD12}, V_{DD18}, V_{DDB}, and V_{RTC} by the ADC. Built-in limit monitors allow converted input samples to be compared against user-configurable high and low limits, with an option to trigger an interrupt and wake the CPU from a low power mode if attention is required.

A wide variety of communications and interface peripherals are provided, including a USB 2.0 slave interface, three master SPI interfaces, one slave SPI interface, four UART interfaces with multidrop support, three master I^2C interfaces, and a slave I^2C interface.

ARM Cortex-M4F Processor

The ARM Cortex-M4F processor is ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Cortex-M4F DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Analog-to-Digital Converter

The 10-bit delta-sigma ADC provides 4 external inputs and can also be configured to measure all internal power supplies. It operates at a maximum of 7.8ksps. AIN0 and AIN1 are 5V tolerant, making them suitable for monitoring batteries.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low-power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low power mode.

The ADC reference is selectable:

- Internal bandgap
- External reference
- V_{DD18}. This option disables the reference buffer to minimize power consumption.

Pulse Train Engine

Sixteen independent pulse train generators provide either a square wave or a repeating pattern from 2 bits to 32 bits in length. The frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, etc.) of the input pulse train module clock.

Any single pulse train generator or any desired group of pulse train generators can be restarted at the beginning of their patterns and synchronized with one another ensuring simultaneous startup. Additionally, each pulse train can operate in a single shot mode.

Clocking Scheme

The high-frequency internal relaxation oscillator operates at a nominal frequency of 96MHz. It is the primary clock source for the digital logic and peripherals. Select a 4MHz internal oscillator to optimize active power consumption. Wakeup is possible from either the 4MHz internal oscillator or the 96MHz internal oscillator. An external 32.768kHz timebase is required when using the RTC or USB features of the device. The time base can be generated by attaching a 32kHz crystal connected between 32KIN and 32KOUT, or an external clock source can also be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table. The 32kHz output can be directed out to pin P1.7 and remains active in all low power modes including LP0.

Interrupt Sources

The ARM nested vector interrupt controller (NVIC) provides a high-speed, deterministic interrupt response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags to indicate the specific source of the interrupt within the peripheral. 55 distinct interrupts can be grouped by firmware into 8 levels of priority (including internal and external interrupts). There are 9 interrupts for the GPIO ports, one for each port.

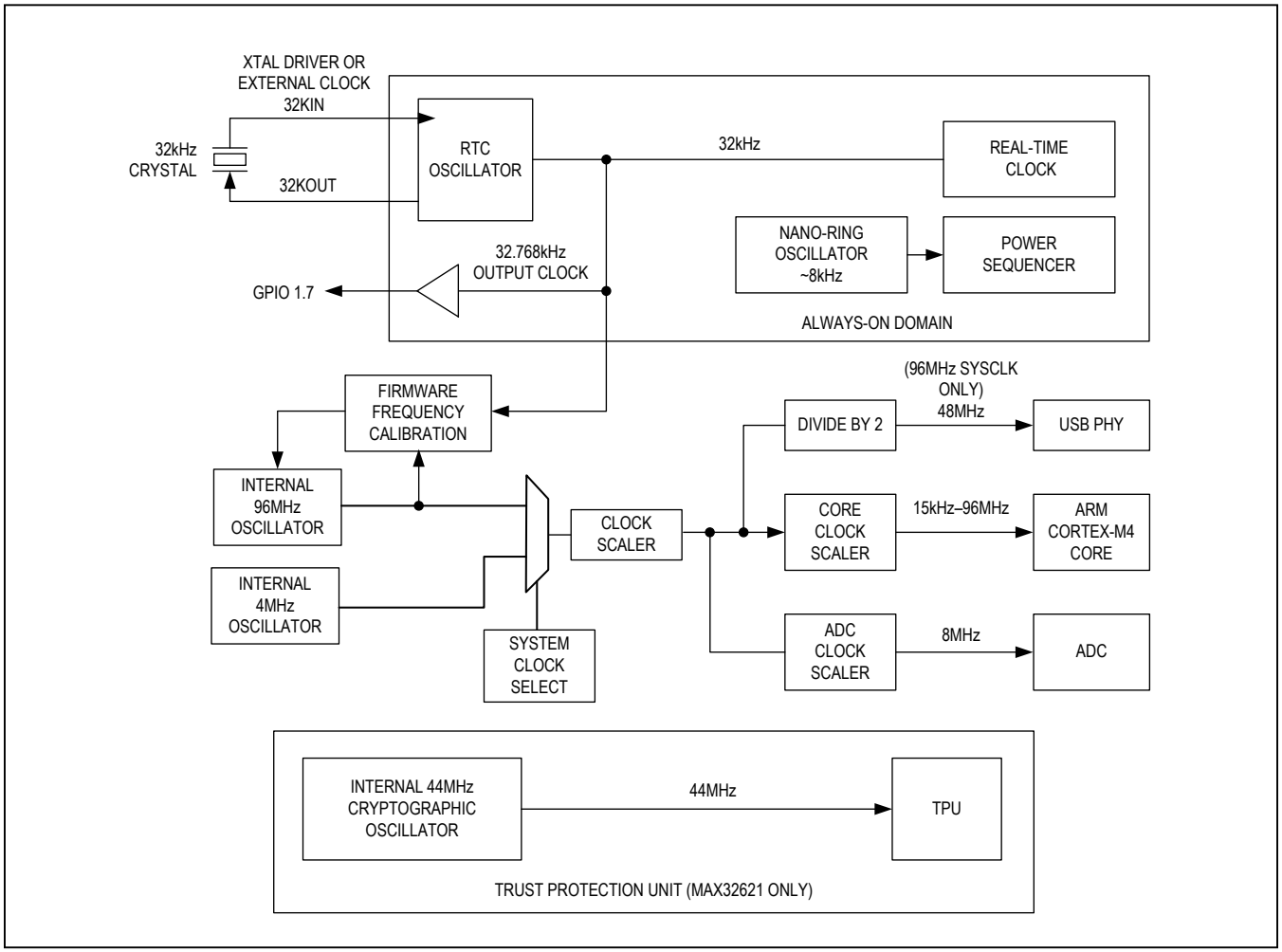


Figure 2. MAX32630/MAX32631 Clock Scheme

Real-Time Clock and Wake-Up Timer

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode. The minimum wake-up interval is 244µs. The V_{RTC} supports SRAM retention in power mode LP0.

CRC Module

A CRC hardware module is included to provide fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) polynomials.

Watchdog Timers

Two independent watchdog timers (WDT1 and WDT2) with window support are provided. The watchdog timers are independent and have multiple clock source options to ensure system security. The watchdog uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the watchdog timers must be written prior to timeout or within a window of time if window mode is enabled. Failure to write the watchdog timer during the programmed timing window results in a watchdog timeout. The WDT1 or WDT2 flags are set on reset if a watchdog expiration caused the system reset. The clock source options for the watchdog timers WDT1 and WDT2 include:

- Scaled system clock
- Real-time clock
- Power management clock

A third watchdog timer (WDT3) is provided for recovery from runaway code or system unresponsiveness. This recovery watchdog uses a 16-bit timer to generate the watchdog reset. When enabled, this watchdog must be written prior to timeout, resulting in a watchdog timeout. The WDT3 flag is set on reset if a watchdog expiration caused the system reset. The clock source for the recovery watchdog is the 8kHz nano ring, and the granularity of the timeout period is intended only for system recovery.

Programmable Timers

Six 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each of the 32-bit timers can also be split into two 16-bit timers, enabling 12 standard 16-bit timers.

32-bit timer features:

- 32-bit up/down autoreload
- Programmable 16-bit prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- GPIOs can be assigned as external timer inputs, clock gating or capture, limited to an input frequency of 1/4 of the peripheral clock frequency
- Timer output pin
- Configurable as 2x 16-bit general purpose timers
- Timer interrupt

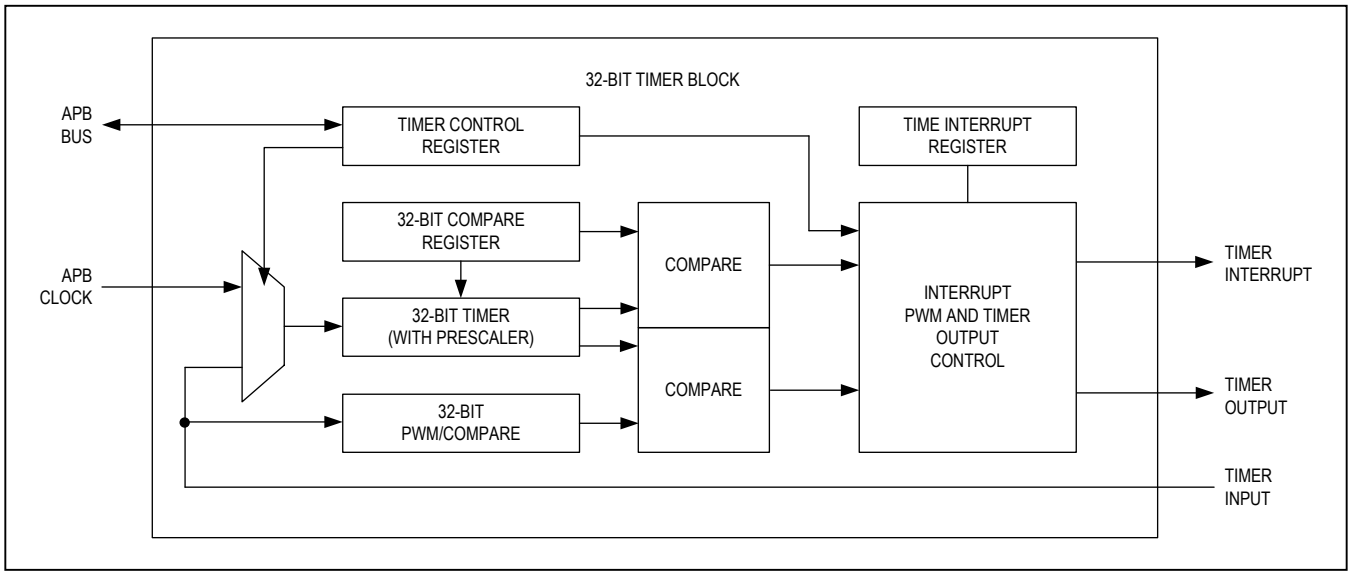


Figure 4. Timer Block Diagram, 32-Bit Mode

Serial Peripherals

USB Controller

The integrated USB slave controller is compliant with the full-speed (12Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator enables smart switching between the main supply and V_{DDB} when connected to a USB host controller.

The USB controller supports DMA for the endpoint buffers. A total of 7 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

An external 32kHz crystal or clock source is required for USB operation, even if the RTC function is not used. Although the USB timing is derived from the internal 96MHz oscillator, the default accuracy is not sufficient for USB operation. Periodic firmware adjustments of the 96MHz oscillator, using the 32kHz timebase as a reference, are necessary to comply with the USB timing requirements.

I2C Master and Slave Ports

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. Three I2C master engines and one I2C-selectable slave engine interface to a wide variety of I2C-compatible peripherals. These engines support both Standard-mode and Fast-mode I2C standards. The slave engine shares the same I/O port as the master engines and is selectable through the I/O configuration settings. It provides the following features:

- Master or slave mode operation
- Supports standard (7-bit) addressing or 10-bit addressing
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast-mode: 400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 16 bytes
- Transmitter FIFO depth of 16 bytes

Serial Peripheral Interface—Master

The SPI master-mode-only (SPIM) interface operates independently in a single or multiple slave system and is fully accessible to the user application.

The SPI ports provide a highly configurable, flexible, and efficient interface to communicate with a wide variety of SPI slave devices. The three SPI master ports (SPI0, SPI1, SPI2) support the following features:

- SPI modes (0, 3) for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and Quad I/O supported
- Up to 5 slave select lines per port
- Up to 2 slave ready lines
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- High-speed AHB access to transmit and receive using 32-byte FIFOs
- SS assertion and deassertion timing with respect to leading/trailing SCK edge

Serial Peripheral Interface—Slave

The SPI slave (SPIS) port provide a highly configurable, flexible, and efficient interface to communicate with a wide variety of SPI master devices. The SPI slave interface supports the following features:

- Supports SPI modes 0 and 3
- Full-duplex operation in single-bit, 4-wire mode
- Slave select polarity fixed (active low)
- Dual and Quad I/O supported
- High-speed AHB access to transmit and receive using 32-byte FIFOs
- Four interrupts to monitor FIFO levels

Serial Peripheral Interface Execute in Place (SPIX) Master

The SPI execute in place (SPIX) master allows the CPU to transparently execute instructions stored in an external SPI flash. Instructions fetched through the SPIX master are cached just like instructions fetched from internal program memory. The SPIX master can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

UART

All four universal asynchronous receiver-transmitter (UART) interfaces support full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) methodology. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate 1843.2kB

Trust Protection Unit (TPU) (MAX32631 Only)

The TPU enhances cryptographic data security for valuable intellectual property (IP) and data. A high-speed, dedicated, hardware-based math accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms including:

- AES-128
- AES-192
- AES-256
- 1024-bit DSA
- 2048-bit (CRT)

The device provides a pseudo-random number generator that can be used to create cryptographic keys for any application. A user-selectable entropy source further increases the randomness and key strength.

The secure bootloader protects against unauthorized access to program memory.

Peripheral Management Unit (PMU)

The PMU is a DMA-based link list processing engine that performs operations and data transfers involving memory and/or peripherals in the advanced peripheral bus (APB) and advanced high-performance bus (AHB) peripheral memory space while the main CPU is in a sleep state. This allows low-overhead peripheral operations to be performed without the CPU, significantly reducing overall power consumption. Using the PMU with the CPU in a sleep state provides a lower noise environment critical for obtaining optimum ADC performance.

Key features of the PMU engine include:

- Six independent channels with round-robin scheduling allows for multiple parallel operations
- Programmed using SRAM-based PMU op codes
- PMU action can be initiated from interrupt conditions from peripherals without CPU
- Integrated AHB bus master
- Coprocessor-like state machine

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals
- Errata sheets for specific revisions noting deviations from published specifications

For information regarding these documents, visit Technical Support at support.maximintegrated.com/micro.

Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

- Evaluation kits
- Software development kit
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

For technical support, go to **support.maximintegrated.com/micro**

Applications Information

Table 1. General-Purpose I/O Matrix

	PRIMARY FUNCTION	SECONDARY FUNCTION	TERTIARY FUNCTION	QUATERNARY FUNCTION	PULSE TRAIN	TIMER INPUT	GPIO INTERRUPT
P0.0	UART0A_RX	UART0B_TX			PT_PT0	TIMER_TMR0	GPIO_INT(P0)
P0.1	UART0A_TX	UART0B_RX			PT_PT1	TIMER_TMR1	GPIO_INT(P0)
P0.2	UART0A_CTS	UART0B_RTS			PT_PT2	TIMER_TMR2	GPIO_INT(P0)
P0.3	UART0A_RTS	UART0B_CTS			PT_PT3	TIMER_TMR3	GPIO_INT(P0)
P0.4	SPIM0A_SCK				PT_PT4	TIMER_TMR4	GPIO_INT(P0)
P0.5	SPIM0A_MOSI/ SDIO0				PT_PT5	TIMER_TMR5	GPIO_INT(P0)
P0.6	SPIM0A_MISO/ SDIO1				PT_PT6	TIMER_TMR0	GPIO_INT(P0)
P0.7	SPIM0A_SS0				PT_PT7	TIMER_TMR1	GPIO_INT(P0)
P1.0	SPIM1A_SCK	SPIX0A_SCK			PT_PT8	TIMER_TMR2	GPIO_INT(P1)
P1.1	SPIM1A_MOSI/ SDIO0	SPIX0A_ SDIO0			PT_PT9	TIMER_TMR3	GPIO_INT(P1)
P1.2	SPIM1A_MISO/ SDIO1	SPIX0A_ SDIO1			PT_PT10	TIMER_TMR4	GPIO_INT(P1)
P1.3	SPIM1A_SS0	SPIX0A_SS0			PT_PT11	TIMER_TMR5	GPIO_INT(P1)
P1.4	SPIM1A_SDIO2	SPIX0A_ SDIO2			PT_PT12	TIMER_TMR0	GPIO_INT(P1)
P1.5	SPIM1A_SDIO3	SPIX0A_ SDIO3			PT_PT13	TIMER_TMR1	GPIO_INT(P1)
P1.6	I2CM0A/S0A_SDA				PT_PT14	TIMER_TMR2	GPIO_INT(P1)
P1.7	I2CM0A/S0A_SCL				PT_PT15	TIMER_TMR3	GPIO_INT(P1)
P2.0	UART1A_RX	UART1B_TX			PT_PT0	TIMER_TMR4	GPIO_INT(P2)
P2.1	UART1A_TX	UART1B_RX			PT_PT1	TIMER_TMR5	GPIO_INT(P2)
P2.2	UART1A_CTS	UART1B_RTS			PT_PT2	TIMER_TMR0	GPIO_INT(P2)
P2.3	UART1A_RTS	UART1B_CTS			PT_PT3	TIMER_TMR1	GPIO_INT(P2)
P2.4	SPIM2A_SCK				PT_PT4	TIMER_TMR2	GPIO_INT(P2)
P2.5	SPIM2A_MOSI/ SDIO0				PT_PT5	TIMER_TMR3	GPIO_INT(P2)
P2.6	SPIM2A_MISO/ SDIO1				PT_PT6	TIMER_TMR4	GPIO_INT(P2)
P2.7	SPIM2A_SS0				PT_PT7	TIMER_TMR5	GPIO_INT(P2)
P3.0	UART2A_RX	UART2B_TX			PT_PT8	TIMER_TMR0	GPIO_INT(P3)
P3.1	UART2A_TX	UART2B_RX			PT_PT9	TIMER_TMR1	GPIO_INT(P3)
P3.2	UART2A_CTS	UART2B_RTS			PT_PT10	TIMER_TMR2	GPIO_INT(P3)
P3.3	UART2A_RTS	UART2B_CTS			PT_PT11	TIMER_TMR3	GPIO_INT(P3)
P3.4	I2CM1A/S0B_SDA	SPIM2A_SS1			PT_PT12	TIMER_TMR4	GPIO_INT(P3)

Table 1. General-Purpose I/O Matrix (continued)

	PRIMARY FUNCTION	SECONDARY FUNCTION	TERTIARY FUNCTION	QUATERNARY FUNCTION	PULSE TRAIN	TIMER INPUT	GPIO INTERRUPT
P3.5	I2CM1A/S0B_SCL	SPIM2A_SS2			PT_PT13	TIMER_TMR5	GPIO_INT(P3)
P3.6	SPIM1A_SS1	SPIX_SS1			PT_PT14	TIMER_TMR0	GPIO_INT(P3)
P3.7	SPIM1A_SS2	SPIX_SS2			PT_PT15	TIMER_TMR1	GPIO_INT(P3)
P4.0	OWM_I/O	SPIM2A_SR0			PT_PT0	TIMER_TMR2	GPIO_INT(P4)
P4.1	OWM_PUPEN	SPIM2A_SR1			PT_PT1	TIMER_TMR3	GPIO_INT(P4)
P4.2	SPIM0A_SDIO2	SPIS0A_SDIO2			PT_PT2	TIMER_TMR4	GPIO_INT(P4)
P4.3	SPIM0A_SDIO3	SPIS0A_SDIO3			PT_PT3	TIMER_TMR5	GPIO_INT(P4)
P4.4	SPIM0A_SS1	SPIS0A_SCLK			PT_PT4	TIMER_TMR0	GPIO_INT(P4)
P4.5	SPIM0A_SS2	SPIS0A_MOSI/SDIO0			PT_PT5	TIMER_TMR1	GPIO_INT(P4)
P4.6	SPIM0A_SS3	SPIS0A_MISO/SDIO1			PT_PT6	TIMER_TMR2	GPIO_INT(P4)
P4.7	SPIM0A_SS4	SPIS0A_SSEL			PT_PT7	TIMER_TMR3	GPIO_INT(P4)
P5.0		SPIM2B_SCK			PT_PT8	TIMER_TMR4	GPIO_INT(P5)
P5.1		SPIM2B_MOSI/SDIO0			PT_PT9	TIMER_TMR5	GPIO_INT(P5)
P5.2		SPIM2B_MISO/SDIO1			PT_PT10	TIMER_TMR0	GPIO_INT(P5)
P5.3		SPIM2B_SS0	UART3A_RX	UART3B_TX	PT_PT11	TIMER_TMR1	GPIO_INT(P5)
P5.4		SPIM2B_SDIO2	UART3A_TX	UART3B_RX	PT_PT12	TIMER_TMR2	GPIO_INT(P5)
P5.5		SPIM2B_SDIO3	UART3A_CTS	UART3B_RTS	PT_PT13	TIMER_TMR3	GPIO_INT(P5)
P5.6		SPIM2B_SR	UART3A_RTS	UART3B_CTS	PT_PT14	TIMER_TMR4	GPIO_INT(P5)
P5.7	I2CM2A/S0C_SDA	SPIM2B_SS1			PT_PT15	TIMER_TMR5	GPIO_INT(P5)
P6.0	I2CM2A/S0C_SCL	SPIM2B_SS2			PT_PT0	TIMER_TMR0	GPIO_INT(P6)
P6.1	SPIM2C_SCK	SPIS0B_SCK			PT_PT1	TIMER_TMR1	GPIO_INT(P6)
P6.2	SPIM2C_MOSI/SDIO0	SPIS0B_MOSI/SDIO0			PT_PT2	TIMER_TMR2	GPIO_INT(P6)
P6.3	SPIM2C_MISO/SDIO1	SPIS0B_MISO/SDIO1			PT_PT3	TIMER_TMR3	GPIO_INT(P6)
P6.4	SPIM2C_SS0	SPIS0B_SSEL			PT_PT4	TIMER_TMR4	GPIO_INT(P6)
P6.5	SPIM2C_SDIO2	SPIS0B_SDIO2			PT_PT5	TIMER_TMR5	GPIO_INT(P6)
P6.6	SPIM2C_SDIO3	SPIS0B_SDIO3			PT_PT6	TIMER_TMR0	GPIO_INT(P6)
P6.7	SPIM2C_SR0	I2CM2B/SE_SDA			PT_PT7	TIMER_TMR1	GPIO_INT(P6)

Table 1. General-Purpose I/O Matrix (continued)

	PRIMARY FUNCTION	SECONDARY FUNCTION	TERTIARY FUNCTION	QUATERNARY FUNCTION	PULSE TRAIN	TIMER INPUT	GPIO INTERRUPT
P7.0	SPIM2C_SS1	I2CM2B/ SE_SCL			PT_PT8	TIMER_TMR2	GPIO_INT(P7)
P7.1	SPIM2C_SS2	I2CM1B/ SD_SDA			PT_PT9	TIMER_TMR3	GPIO_INT(P7)
P7.2	SPIM2C_SR1	I2CM1B/ SD_SCL			PT_PT10	TIMER_TMR4	GPIO_INT(P7)
P7.3	SPIS0C_SCK	I2CM2C/ SG_SDA			PT_PT11	TIMER_TMR5	GPIO_INT(P7)
P7.4	SPIS0C_MOSI/ SDIO0	I2CM2C/ SG_SCL			PT_PT12	TIMER_TMR0	GPIO_INT(P7)
P7.5	SPIS0C_MISO/ SDIO1				PT_PT13	TIMER_TMR1	GPIO_INT(P7)
P7.6	SPIS0C_SS0				PT_PT14	TIMER_TMR2	GPIO_INT(P7)
P7.7	SPIS0C_SDIO2	I2CM1C/ SF_SDA			PT_PT15	TIMER_TMR3	GPIO_INT(P7)
P8.0	SPIS0C_SDIO3	I2CM1C/ SF_SCL			PT_PT0	TIMER_TMR4	GPIO_INT(P8)
P8.1					PT_PT1	TIMER_TMR5	GPIO_INT(P8)

Ordering Information

PART	FLASH	SRAM	TRUST PROTECTION UNIT (TPU)	PIN-PACKAGE
MAX32630IWG+	2MB	512KB	No	100 WLP
MAX32631IWG+	2MB	512KB	Yes	100 WLP
MAX32630IWG+T	2MB	512KB	No	100 WLP
MAX32631IWG+T	2MB	512KB	Yes	100 WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/16	Initial release	—

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