THE DATASHEET OF

LT1162CSW#TRPBF

Half-/Full-Bridge N-Channel Power MOSFET Drivers

FEATURES

- **Floating Top Driver Switches Up to 60V**
- Drives Gate of Top N-Channel MOSFET above Load HV Supply
- **180ns Transition Times Driving 10,000pF**
- **Adaptive Nonoverlapping Gate Drives Prevent Shoot-Through**
- Top Drive Protection at High Duty Cycles
- TTL/CMOS Input Levels
- Undervoltage Lockout with Hysteresis
- Operates at Supply Voltages from 10V to 15V
- Separate Top and Bottom Drive Pins

APPLICATIONS

- PWM of High Current Inductive Loads
- Half-Bridge and Full-Bridge Motor Control
- Synchronous Step-Down Switching Regulators
- 3-Phase Brushless Motor Drive
- High Current Transducer Drivers
- Class D Power Amplifiers

DESCRIPTION

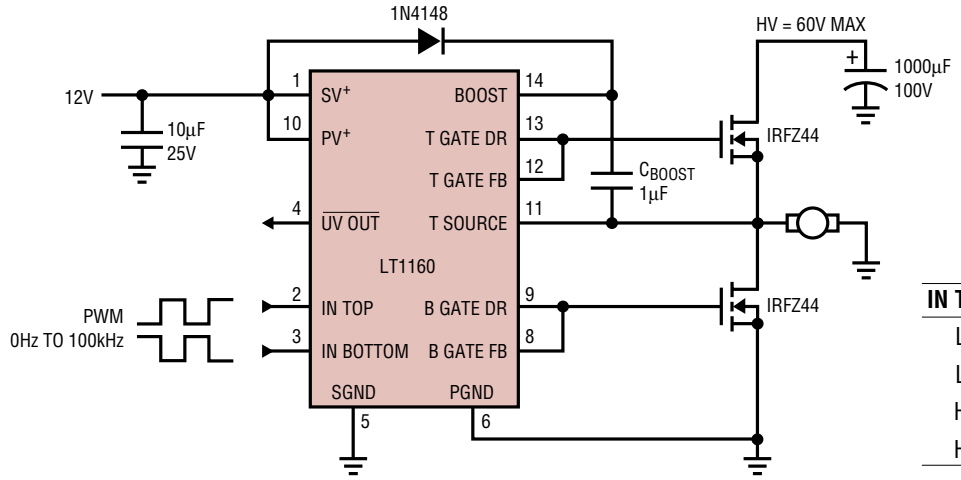
The LT®1160/LT1162 are cost effective half-/full-bridge N-channel power MOSFET drivers. The floating driver can drive the topside N-channel power MOSFETs operating off a high voltage (HV) rail of up to 60V.

The internal logic prevents the inputs from turning on the power MOSFETs in a half-bridge at the same time. Its unique adaptive protection against shoot-through currents eliminates all matching requirements for the two MOSFETs. This greatly eases the design of high efficiency motor control and switching regulator systems.

During low supply or start-up conditions, the undervoltage lockout actively pulls the driver outputs low to prevent the power MOSFETs from being partially turned on. The 0.5V hysteresis allows reliable operation even with slowly varying supplies.

The LT1162 is a dual version of the LT1160 and is available in a 24-pin PDIP or in a 24-pin SO Wide package.

TYPICAL APPLICATION



IN TOP	IN BOTTOM	T GATE DR	B GATE DR
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

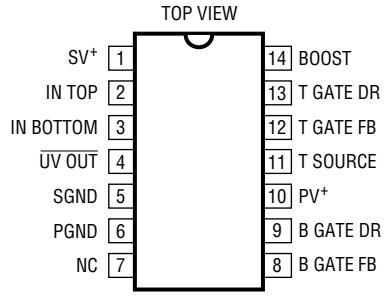
1160 TA01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) 20V
Boost Voltage 75V
Peak Output Currents (< 10µs) 1.5A
Input Pin Voltages ..... –0.3V to V^+ + 0.3V
Top Source Voltage ..... –5V to 60V
Boost to Source Voltage ..... –0.3V to 20V

Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



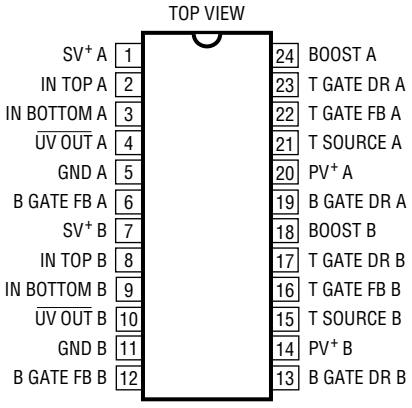
N PACKAGE
14-LEAD PDIP

S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LT1160CN
LT1160CS
LT1160IN
LT1160IS



N PACKAGE
24-LEAD PDIP

SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 80°C/W (SW)

ORDER PART NUMBER

LT1162CSW
LT1162ISW

OBSOLETE PART NUMBERS

LT1162CN
LT1162IN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test Circuit, T_A = 25°C, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V, C_{GATE} = 3000pF. Gate Feedback pins connected to Gate Drive pins, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	DC Supply Current (Note 4)	V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V V^+ = 15V, V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 0.8V		7 7 7	11 10 11	15 15 15	mA mA mA
I_{BOOST}	Boost Current (Note 4)	V^+ = 15V, $V_{TSOURCE}$ = 60V, V_{BOOST} = 75V, V_{INTOP} = $V_{INBOTTOM}$ = 0.8V		3	4.5	6	mA
V_{IL}	Input Logic Low		●		1.4	0.8	V
V_{IH}	Input Logic High		●	2	1.7		V
I_{IN}	Input Current	V_{INTOP} = $V_{INBOTTOM}$ = 4V	●		7	25	µA
V^+_{UVH}	V^+ Undervoltage Start-Up Threshold			8.4	8.9	9.7	V
V^+_{UVL}	V^+ Undervoltage Shutdown Threshold			7.8	8.3	8.8	V
V_{BUVH}	V_{BOOST} Undervoltage Start-Up Threshold	$V_{TSOURCE}$ = 60V (V_{BOOST} – $V_{TSOURCE}$)		8.8	9.3	9.8	V
V_{BUVL}	V_{BOOST} Undervoltage Shutdown Threshold	$V_{TSOURCE}$ = 60V (V_{BOOST} – $V_{TSOURCE}$)		8.2	8.7	9.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.Test Circuit, T_A = 25°C, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V, C_{GATE} = 3000pF. Gate Feedback pins connected to Gate Drive pins, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{UVOUT}	Undervoltage Output Leakage	V^+ = 15V	●		0.1	5	µA
V_{UVOUT}	Undervoltage Output Saturation	V^+ = 7.5V, I_{UVOUT} = 2.5mA	●		0.2	0.4	V
V_{OH}	Top Gate ON Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V	●	11	11.3	12	V
	Bottom Gate ON Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V	●	11	11.3	12	V
V_{OL}	Top Gate OFF Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V	●		0.4	0.7	V
	Bottom Gate OFF Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V	●		0.4	0.7	V
t_r	Top Gate Rise Time	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		130	200	ns
	Bottom Gate Rise Time	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		90	200	ns
t_f	Top Gate Fall Time	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		60	140	ns
	Bottom Gate Fall Time	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		60	140	ns
t_{D1}	Top Gate Turn-On Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		250	500	ns
	Bottom Gate Turn-On Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns
t_{D2}	Top Gate Turn-Off Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		300	600	ns
	Bottom Gate Turn-Off Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns
t_{D3}	Top Gate Lockout Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		300	600	ns
	Bottom Gate Lockout Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		250	500	ns
t_{D4}	Top Gate Release Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR}$ (Note 5)	●		250	500	ns
	Bottom Gate Release Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 5)	●		200	400	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: For the LT1160, Pins 1, 10 should be connected together. For the LT1162, Pins 1, 7, 14, 20 should be connected together.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

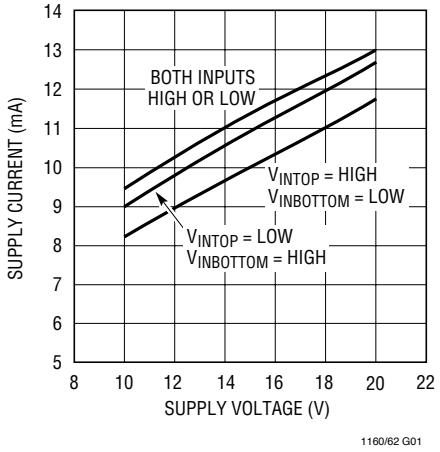
LT1160CN/LT1160IN: $T_J = T_A + (P_D)(70°C/W)$
LT1160CS/LT1160IS: $T_J = T_A + (P_D)(110°C/W)$
LT1162CN/LT1162IN: $T_J = T_A + (P_D)(58°C/W)$
LT1162CS/LT1162IS: $T_J = T_A + (P_D)(80°C/W)$

Note 4: I_S is the sum of currents through SV^+, PV^+ and Boost pins. I_{BOOST} is the current through the Boost pin. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Typical Performance Characteristics and Applications Information sections. The LT1160 = 1/2 LT1162.

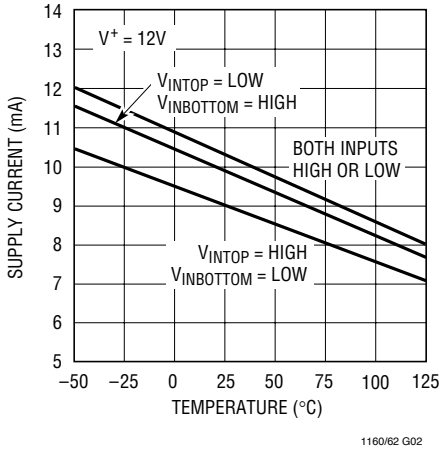
Note 5: See Timing Diagram. Gate rise times are measured from 2V to 10V and fall times are measured from 10V to 2V. Delay times are measured from the input transition to when the gate voltage has risen to 2V or decreased to 10V.

TYPICAL PERFORMANCE CHARACTERISTICS (LT1160 or 1/2 LT1162)

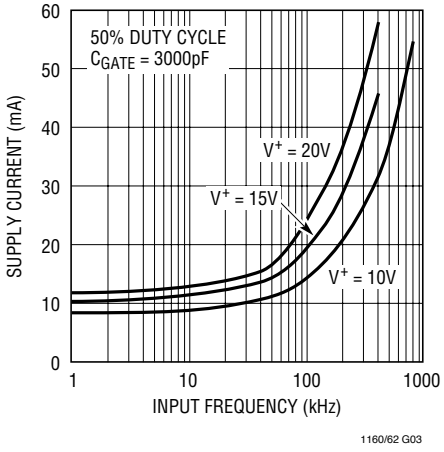
DC Supply Current vs Supply Voltage



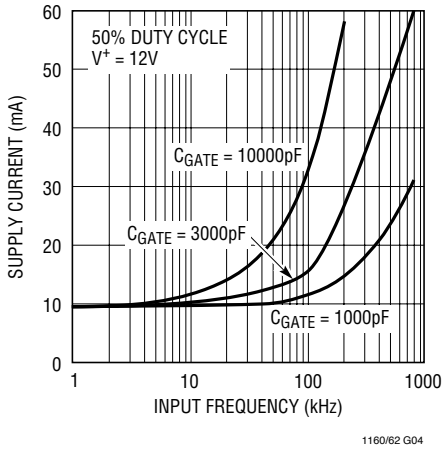
DC Supply Current vs Temperature



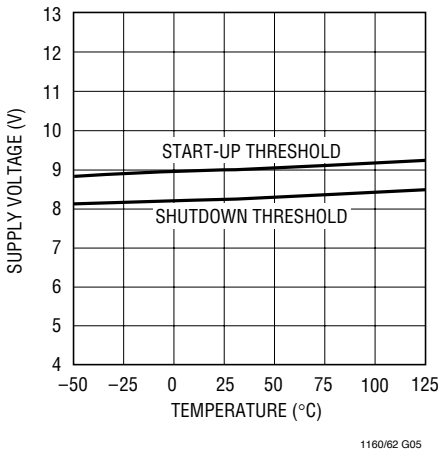
DC + Dynamic Supply Current vs Input Frequency



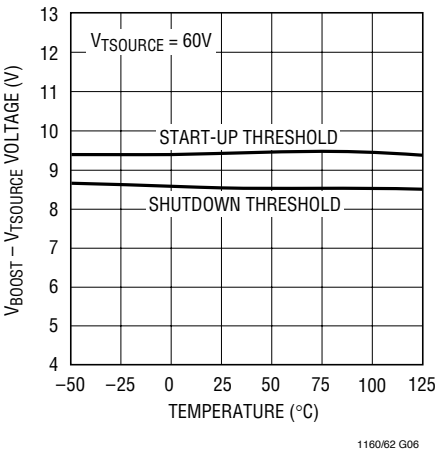
DC + Dynamic Supply Current vs Input Frequency



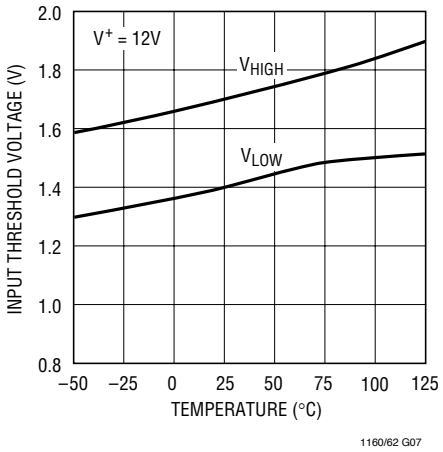
Undervoltage Lockout (V+)



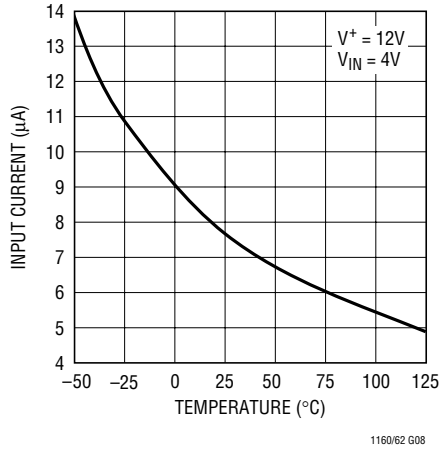
Undervoltage Lockout (VBOOST)



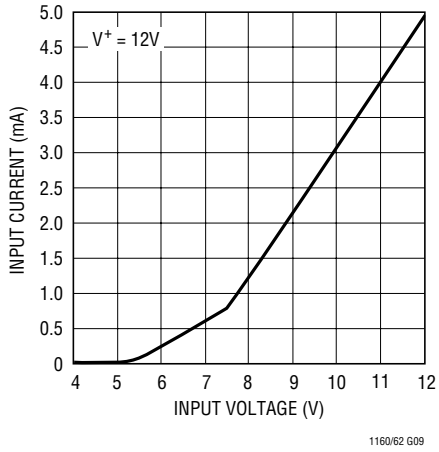
Input Threshold Voltage vs Temperature



Top or Bottom Input Pin Current vs Temperature

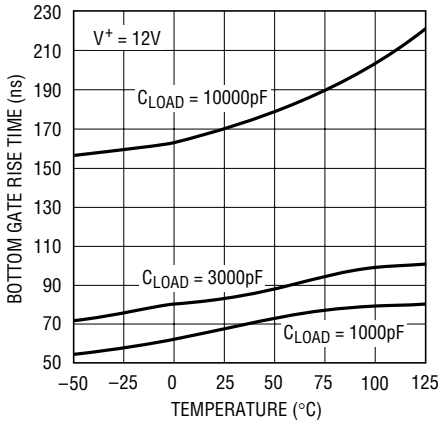


Top or Bottom Input Pin Current vs Input Voltage



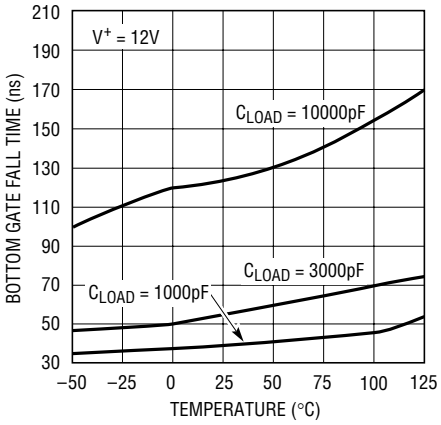
TYPICAL PERFORMANCE CHARACTERISTICS (LT1160 or 1/2 LT1162)

Bottom Gate Rise Time vs Temperature



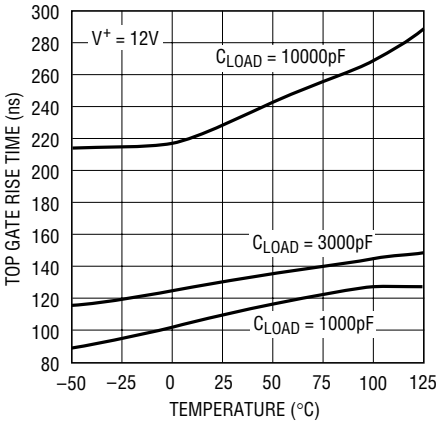
1160/62 G10

Bottom Gate Fall Time vs Temperature



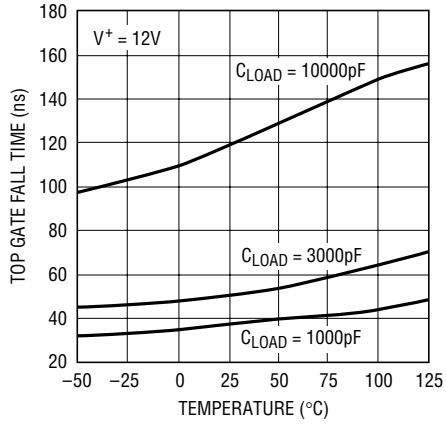
1160/62 G11

Top Gate Rise Time vs Temperature



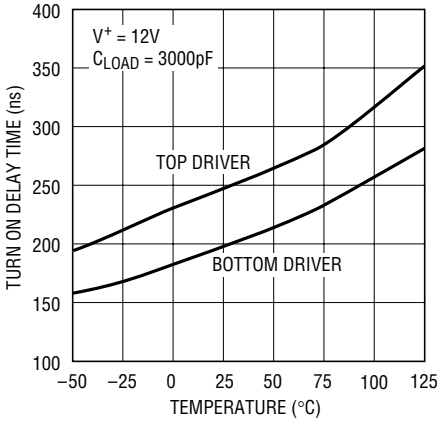
1160/62 G12

Top Gate Fall Time vs Temperature



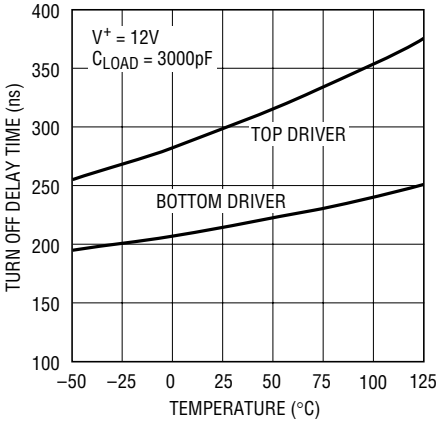
11160/62 G13

Turn-On Delay Time vs Temperature



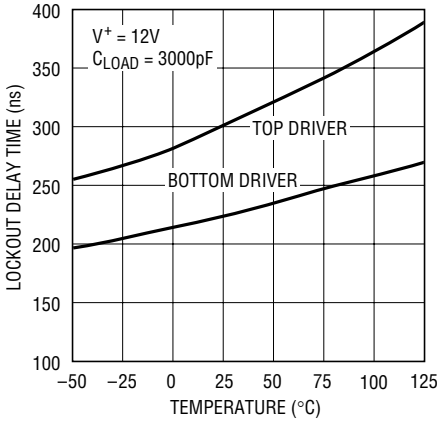
1160/62 G14

Turn-Off Delay Time vs Temperature



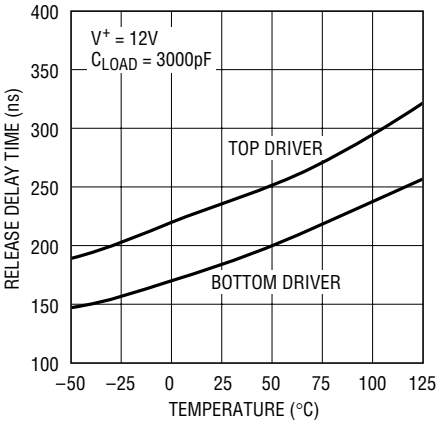
1160/62 G15

Lockout Delay Time vs Temperature



1160/62 G16

Release Delay Time vs Temperature



1160/62 G17

PIN FUNCTIONS

LT1160

SV+ (Pin 1): Main Signal Supply. Must be closely decoupled to the signal ground Pin 5.

IN TOP (Pin 2): Top Driver Input. Pin 2 is disabled when Pin 3 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

IN BOTTOM (Pin 3): Bottom Driver Input. Pin 3 is disabled when Pin 2 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

$\overline{\text{UV OUT}}$ (Pin 4): Undervoltage Output. Open collector NPN output which turns on when V^+ drops below the undervoltage threshold.

SGND (Pin 5): Small Signal Ground. Must be routed separately from other grounds to the system ground.

PGND (Pin 6): Bottom Driver Power Ground. Connects to source of bottom N-channel MOSFET.

B GATE FB (Pin 8): Bottom Gate Feedback. Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until Pin 8 has discharged to below 2.5V.

B GATE DR (Pin 9): Bottom Gate Drive. The high current drive point for the bottom MOSFET. When a gate resistor is used it is inserted between Pin 9 and the gate of the MOSFET.

PV+ (Pin 10): Bottom Driver Supply. Must be connected to the same supply as Pin 1.

T SOURCE (Pin 11): Top Driver Return. Connects to the top MOSFET source and the low side of the bootstrap capacitor.

T GATE FB (Pin 12): Top Gate Feedback. Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until $V_{12} - V_{11}$ has discharged to below 2.9V.

T GATE DR (Pin 13): Top Gate Drive. The high current drive point for the top MOSFET. When a gate resistor is used it is inserted between Pin 13 and the gate of the MOSFET.

BOOST (Pin 14): Top Driver Supply. Connects to the high side of the bootstrap capacitor.

LT1162

SV+ (Pins 1, 7): Main Signal Supply. Must be closely decoupled to ground Pins 5 and 11.

IN TOP (Pins 2, 8): Top Driver Input. The Input Top is disabled when the Input Bottom is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

IN BOTTOM (Pins 3, 9): Bottom Driver Input. The Input Bottom is disabled when the Input Top is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

$\overline{\text{UV OUT}}$ (Pins 4, 10): Undervoltage Output. Open collector NPN output which turns on when V^+ drops below the undervoltage threshold.

GND (Pins 5, 11): Ground Connection.

B GATE FB (Pins 6, 12): Bottom Gate Feedback. Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until Bottom Gate Feedback pins have discharged to below 2.5V.

B GATE DR (Pins 13, 19): Bottom Gate Drive. The high current drive point for the bottom MOSFET. When a gate resistor is used it is inserted between the Bottom Gate Drive pin and the gate of the MOSFET.

PV+ (Pins 14, 20): Bottom Driver Supply. Must be connected to the same supply as Pins 1 and 7.

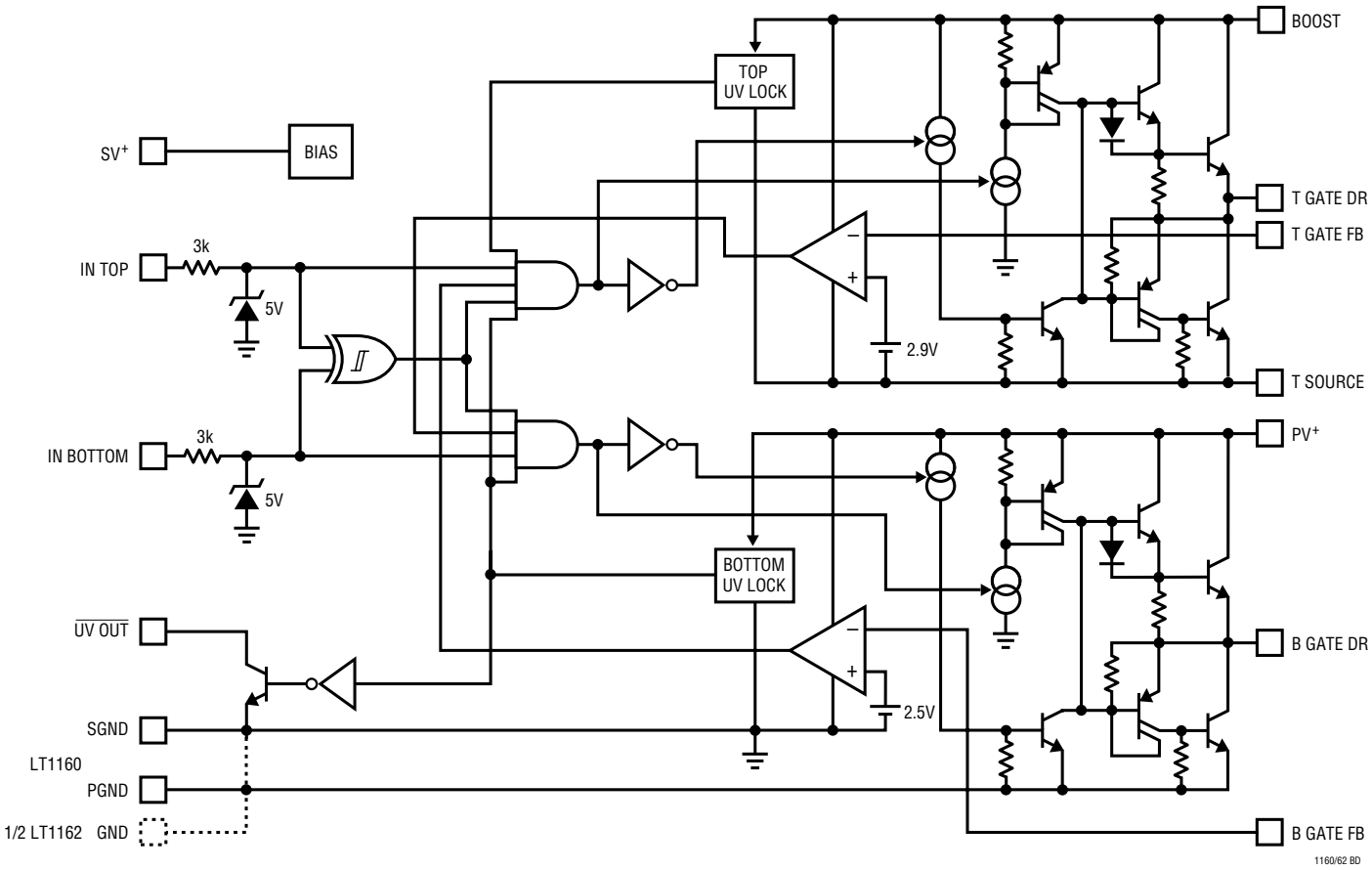
T SOURCE (Pins 15, 21): Top Driver Return. Connects to the top MOSFET source and the low side of the bootstrap capacitor.

T GATE FB (Pins 16, 22): Top Gate Feedback. Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until $V_{TGF} - V_{TSOURCE}$ has discharged to below 2.9V.

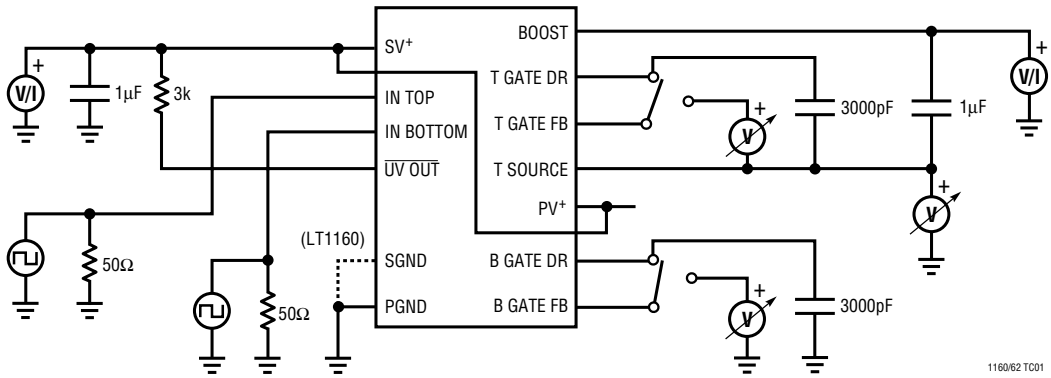
T GATE DR (Pins 17, 23): Top Gate Drive. The high current drive point for the top MOSFET. When a gate resistor is used it is inserted between the Top Gate Drive pin and the gate of the MOSFET.

BOOST (Pins 18, 24): Top Driver Supply. Connects to the high side of the bootstrap capacitor.

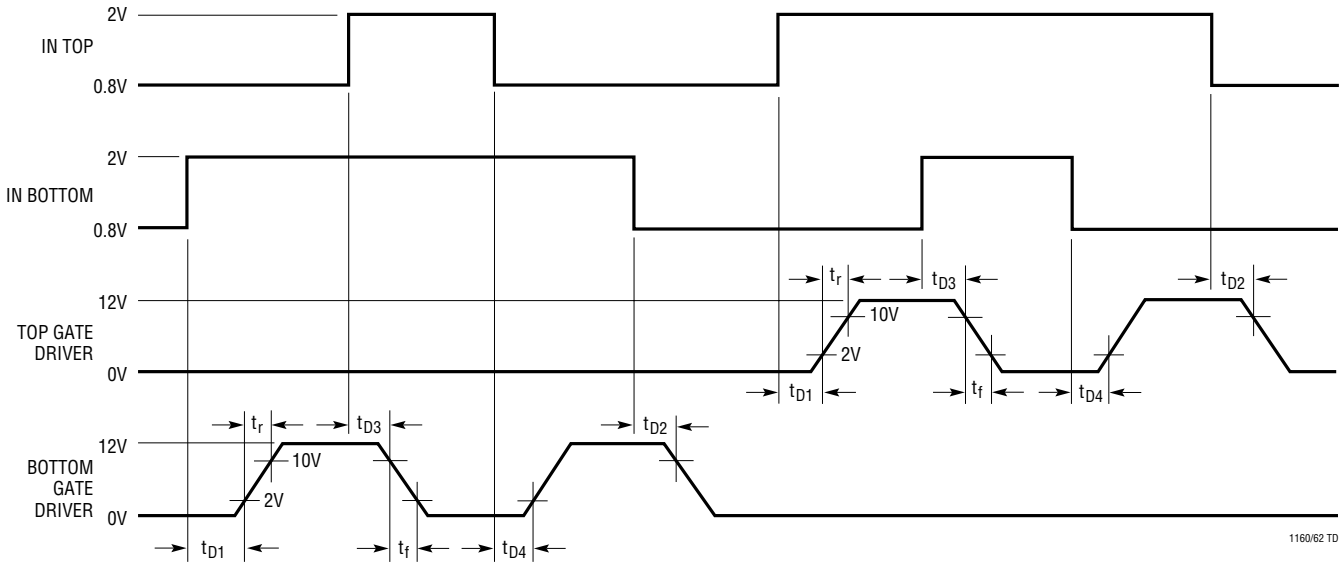
FUNCTIONAL DIAGRAM (LT1160 or 1/2 LT1162)



TEST CIRCUIT (LT1160 or 1/2 LT1162)



TIMING DIAGRAM



OPERATION (Refer to Functional Diagram)

The LT1160 (or 1/2 LT1162) incorporates two independent driver channels with separate inputs and outputs. The inputs are TTL/CMOS compatible; they can withstand input voltages as high as V^+. The 1.4V input threshold is regulated and has 300mV of hysteresis. Both channels are noninverting drivers. The internal logic prevents both outputs from simultaneously turning on under any input conditions. When both inputs are high both outputs are actively held low.

The floating supply for the top driver is provided by a bootstrap capacitor between the Boost pin and the Top Source pin. This capacitor is recharged each time the negative plate goes low in PWM operation.

The undervoltage detection circuit disables both channels when V^+ is below the undervoltage trip point. A separate UV detect block disables the high side channel when $V_{BOOST} - V_{TSOURCE}$ is below its own undervoltage trip point.

The top and bottom gate drivers in the LT1160 each utilize two gate connections: 1) a gate drive pin, which provides the turn on and turn off currents through an optional series gate resistor, and 2) a gate feedback pin which connects directly to the gate to monitor the gate-to-source voltage.

Whenever there is an input transition to command the outputs to change states, the LT1160 follows a logical sequence to turn off one MOSFET and turn on the other. First, turn-off is initiated, then V_{GS} is monitored until it has decreased below the turn-off threshold, and finally the other gate is turned on.

APPLICATIONS INFORMATION

Power MOSFET Selection

Since the LT1160 (or 1/2 LT1162) inherently protects the top and bottom MOSFETs from simultaneous conduction, there are no size or matching constraints. Therefore selection can be made based on the operating voltage and $R_{DS(ON)}$ requirements. The MOSFET BV_{DSS} should be greater than the HV and should be increased to approximately (2)(HV) in harsh environments with frequent fault conditions. For the LT1160 maximum operating HV supply of 60V, the MOSFET BV_{DSS} should be from 60V to 100V.

The MOSFET $R_{DS(ON)}$ is specified at T_J = 25°C and is generally chosen based on the operating efficiency required as long as the maximum MOSFET junction temperature is not exceeded. The dissipation while each MOSFET is on is given by:

$$P = D(I_{DS})^2(1+\partial)R_{DS(ON)}$$

Where D is the duty cycle and ∂ is the increase in $R_{DS(ON)}$ at the anticipated MOSFET junction temperature. From this equation the required $R_{DS(ON)}$ can be derived:

$$R_{DS(ON)} = \frac{P}{D\left(I_{DS}\right)^2\left(1+\partial\right)}$$

For example, if the MOSFET loss is to be limited to 2W when operating at 5A and a 90% duty cycle, the required $R_{DS(ON)}$ would be 0.089Ω/(1 + ∂). (1 + ∂) is given for each MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but ∂ = 0.007/°C can be used as an approximation for low voltage MOSFETs. Thus, if T_A = 85°C and the available heat sinking has a thermal resistance of 20°C/W, the MOSFET junction temperature will be 125°C and ∂ = 0.007(125 – 25) = 0.7. This means that the required $R_{DS(ON)}$ of the MOSFET will be 0.089Ω/1.7 = 0.0523Ω, which can be satisfied by an IRFZ34 manufactured by International Rectifier.

Transition losses result from the power dissipated in each MOSFET during the time it is transitioning from off to on, or from on to off. These losses are proportional to (f)(HV)^2 and vary from insignificant to being a limiting factor on operating frequency in some high voltage applications.

Paralleling MOSFETs

When the above calculations result in a lower $R_{DS(ON)}$ than is economically feasible with a single MOSFET, two or more MOSFETs can be paralleled. The MOSFETs will inherently share the currents according to their $R_{DS(ON)}$ ratio as long as they are thermally connected (e.g., on a common heat sink). The LT1160 top and bottom drivers can each drive five power MOSFETs in parallel with only a small loss in switching speeds (see Typical Performance Characteristics). A low value resistor (10Ω to 47Ω) in series with each individual MOSFET gate may be required to "decouple" each MOSFET from its neighbors to prevent high frequency oscillations (consult manufacturer's recommendations). If gate decoupling resistors are used the corresponding gate feedback pin can be connected to any one of the gates as shown in Figure 1.

Driving multiple MOSFETs in parallel may restrict the operating frequency to prevent overdissipation in the LT1160 (see the following Gate Charge and Driver Dissipation).

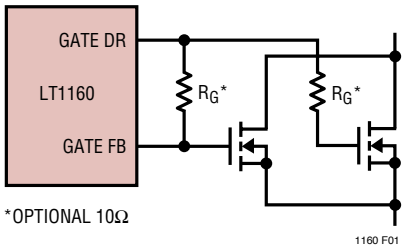


Figure 1. Paralleling MOSFETs

Gate Charge and Driver Dissipation

A useful indicator of the load presented to the driver by a power MOSFET is the total gate charge Q_G, which includes the additional charge required by the gate-to-drain swing. Q_G is usually specified for V_{GS} = 10V and $V_{DS} = 0.8V_{DS(MAX)}$. When the supply current is measured in a switching application, it will be larger than given by the DC electrical characteristics because of the additional supply current associated with sourcing the MOSFET gate charge:

$$I_{SUPPLY} = I_{DC} + \left(\frac{dQ_G}{dt}\right)_{TOP} + \left(\frac{dQ_G}{dt}\right)_{BOTTOM}$$

APPLICATIONS INFORMATION

The actual increase in supply current is slightly higher due to LT1160 switching losses and the fact that the gates are being charged to more than 10V. Supply Current vs Input Frequency is given in the Typical Performance Characteristics.

The LT1160 junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LT1160IS is limited to less than 31mA from a 12V supply:

$T_J = 85°C + (31mA)(12V)(110°C/W)$

$= 126°C$ exceeds absolute maximum

In order to prevent the maximum junction temperature from being exceeded, the LT1160 supply current must be verified while driving the full complement of the chosen MOSFET type at the maximum switching frequency.

Ugly Transient Issues

In PWM applications the drain current of the top MOSFET is a square wave at the input frequency and duty cycle. To prevent large voltage transients at the top drain, a low ESR electrolytic capacitor must be used and returned to the power ground. The capacitor is generally in the range of 25µF to 5000µF and must be physically sized for the RMS current flowing in the drain to prevent heating and premature failure. In addition, the LT1160 requires a separate 10µF capacitor connected closely between Pins 1 and 5 (the LT1162 requires two 10µF capacitors connected between Pins 1 and 5, and Pins 7 and 11).

The LT1160 top source is internally protected against transients below ground and above supply. However, the gate drive pins cannot be forced below ground. In most applications, negative transients coupled from the source to the gate of the top MOSFET do not cause any problems.

Switching Regulator Applications

The LT1160 (or 1/2 LT1162) is ideal as a synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. Most step-down regulators use a high current Schottky diode to conduct the inductor current when the switch is off. The fractions of the oscillator period that the switch is on (switch conducting) and off (diode conducting) are given by:

$$\text{Switch ON} = \left(\frac{V_{OUT}}{HV}\right)(\text{Total Period})$$

$$\text{Switch OFF} = \left(\frac{HV - V_{OUT}}{HV}\right)(\text{Total Period})$$

Note that for $HV > 2V_{OUT}$ the switch is off longer than it is on, making the diode losses more significant than the switch. The worst case for the diode is during a short circuit, when V_{OUT} approaches zero and the diode conducts the short-circuit current almost continuously.

Figure 2 shows the LT1160 used to synchronously drive a pair of power MOSFETs in a step-down regulator application, where the top MOSFET is the switch and the bottom MOSFET replaces the Schottky diode. Since both conduction paths have low losses, this approach can result in very high efficiency (90% to 95%) in most applications. For regulators under 10A, using low $R_{DS(ON)}$ N-channel MOSFETs eliminates the need for heat sinks. R_{GS} holds the top MOSFET off when HV is applied before the 12V supply.

One fundamental difference in the operation of a step-down regulator with synchronous switching is that it never becomes discontinuous at light loads. The inductor current doesn't stop ramping down when it reaches zero but actually reverses polarity resulting in a constant ripple current independent of load. This does not cause a significant efficiency loss (as might be expected) since the negative inductor current is returned to HV when the switch turns back on. However, I^2R losses will occur under these conditions due to the recirculating currents.

The LT1160 performs the synchronous MOSFET drive in a step-down switching regulator. A reference and PWM are required to complete the regulator. Any voltage mode or current mode PWM controller may be used but the LT3526 is particularly well-suited to high power, high efficiency applications such as the 10A circuit shown in Figure 4. In higher current regulators a small Schottky diode across the bottom MOSFET helps to reduce reverse-recovery switching losses.

APPLICATIONS INFORMATION

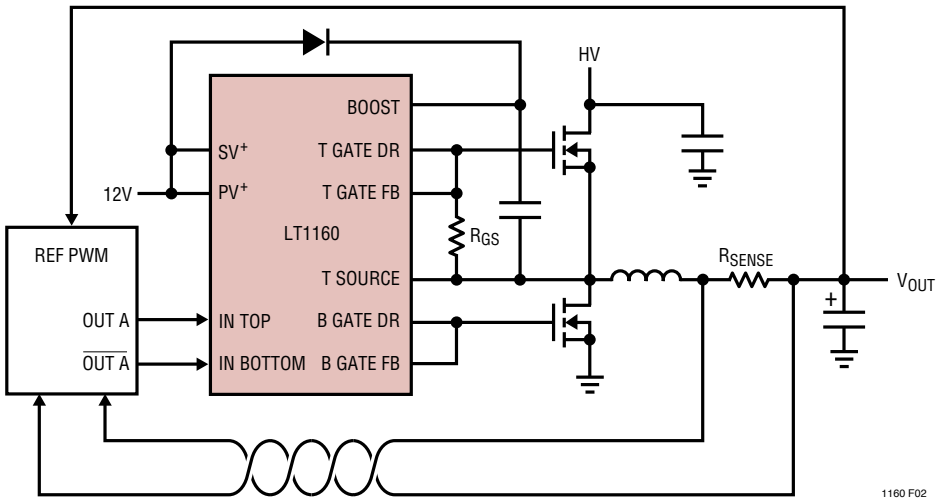


Figure 2. Adding Synchronous Switching to a Step-Down Switching Regulator

Motor Drive Applications

In applications where rotation is always in the same direction, a single LT1160 controlling a half-bridge can be used to drive a DC motor. One end of the motor may be connected either to supply or to ground as seen on Figure 3. A motor in this configuration is controlled by its inputs which give three alternatives: run, free running stop (coasting) and fast stop ("plugging" braking, with the motor shorted by one of the MOSFETs).

To drive a DC motor in both directions the LT1162 can be used to drive an H-bridge output stage. In this configuration the motor can be made to run clockwise, counterclockwise, stop rapidly ("plugging" braking) or free run (coast) to a stop. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a closed-loop control system with tachometric feedback is usually necessary.

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated square waves. This approach is particularly suitable for microcomputers/DSP control loops.

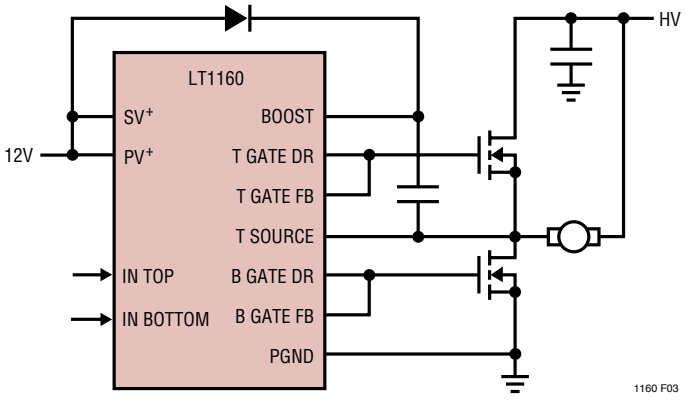


Figure 3. Driving a Supply Referenced Motor

TYPICAL APPLICATIONS

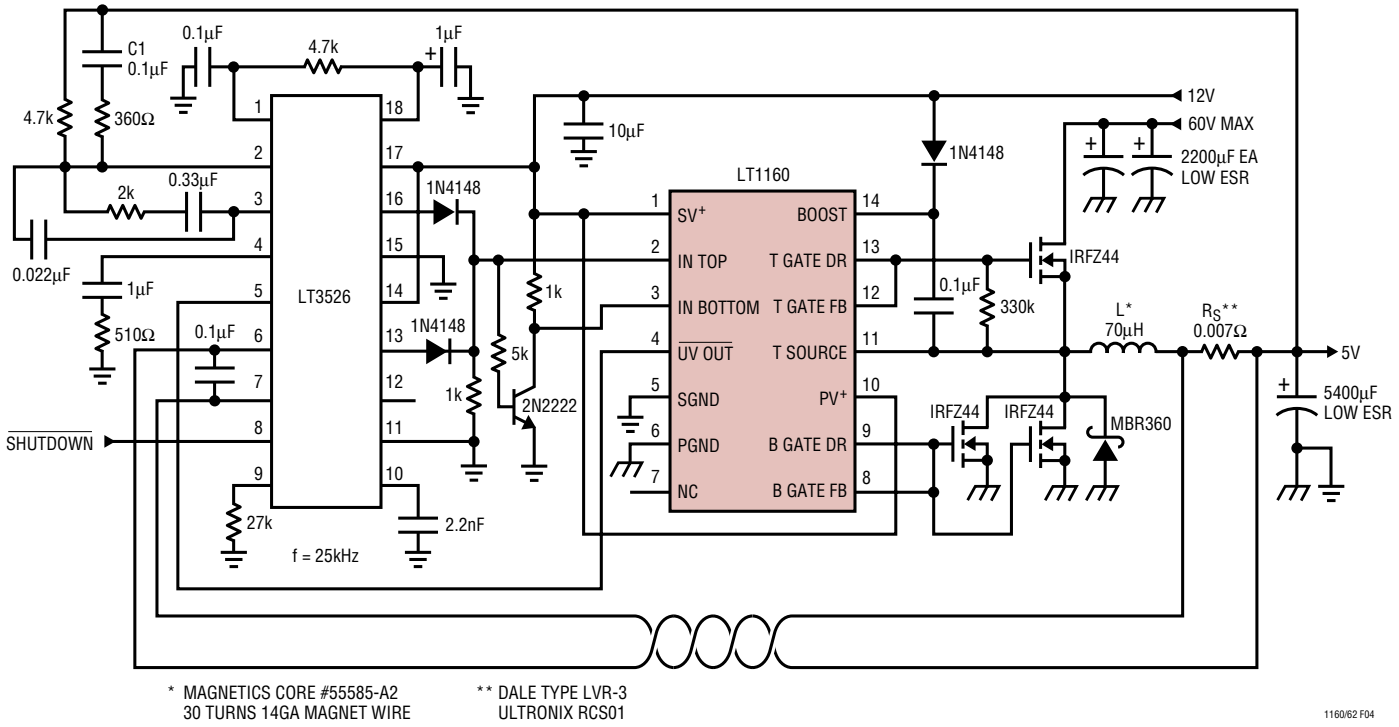


Figure 4. 90% Efficiency, 40V to 5V 10A Low Dropout Voltage Mode Switching Regulator

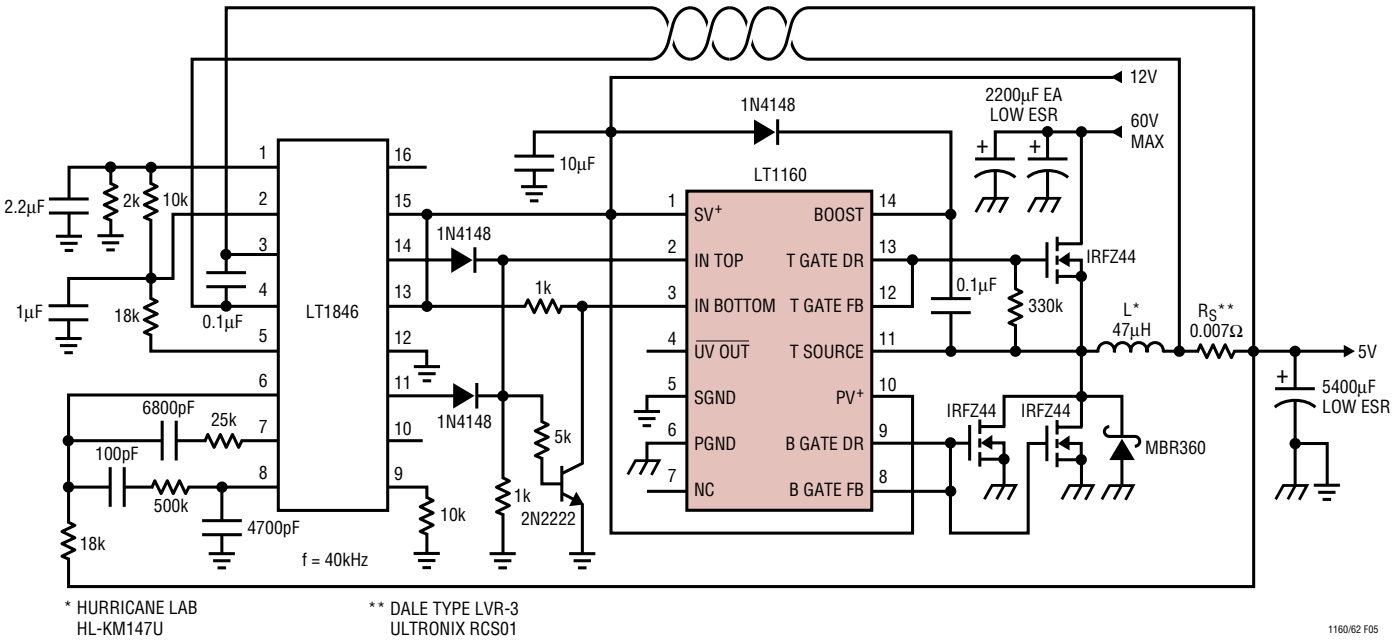


Figure 5. 90% Efficiency, 40V to 5V 10A Low Dropout Current Mode Switching Regulator

TYPICAL APPLICATIONS

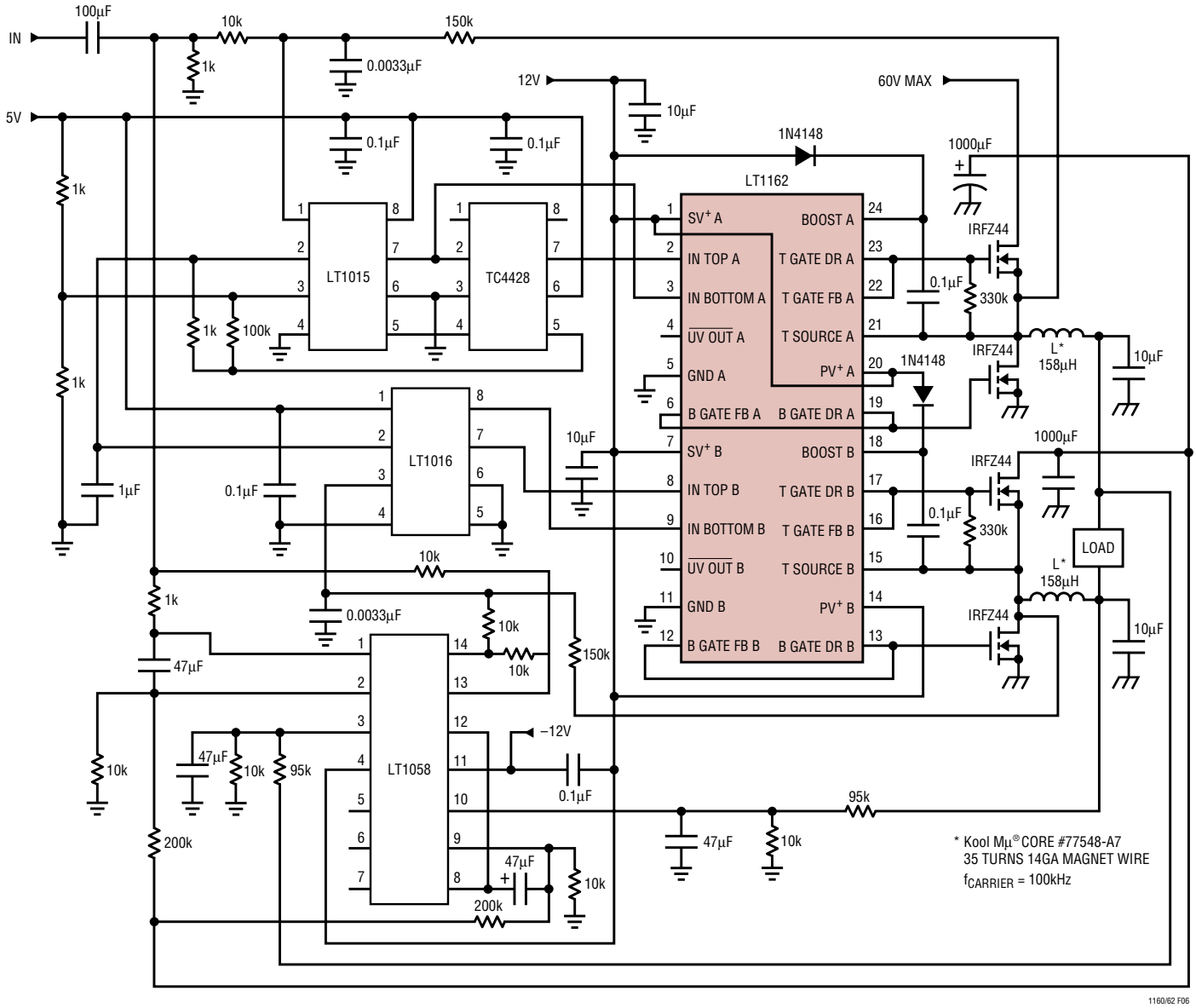


Figure 6. 200W Class D, 10Hz to 1kHz Amplifier

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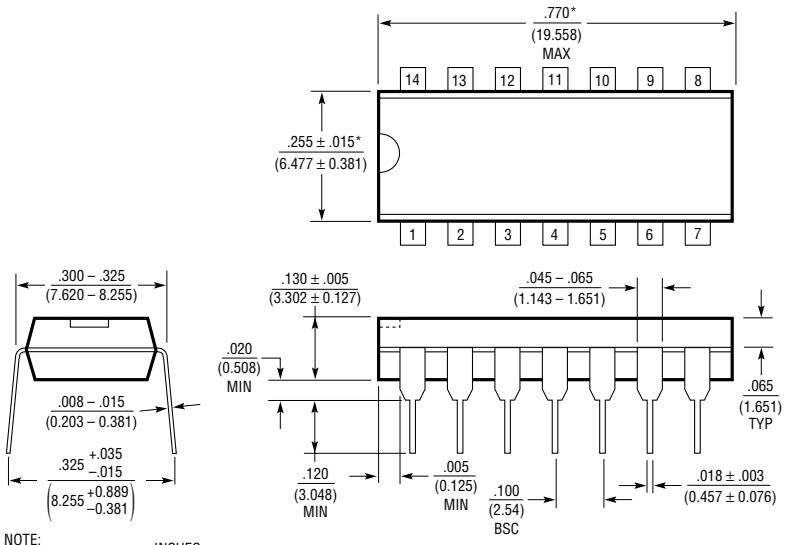
PACKAGE DESCRIPTION

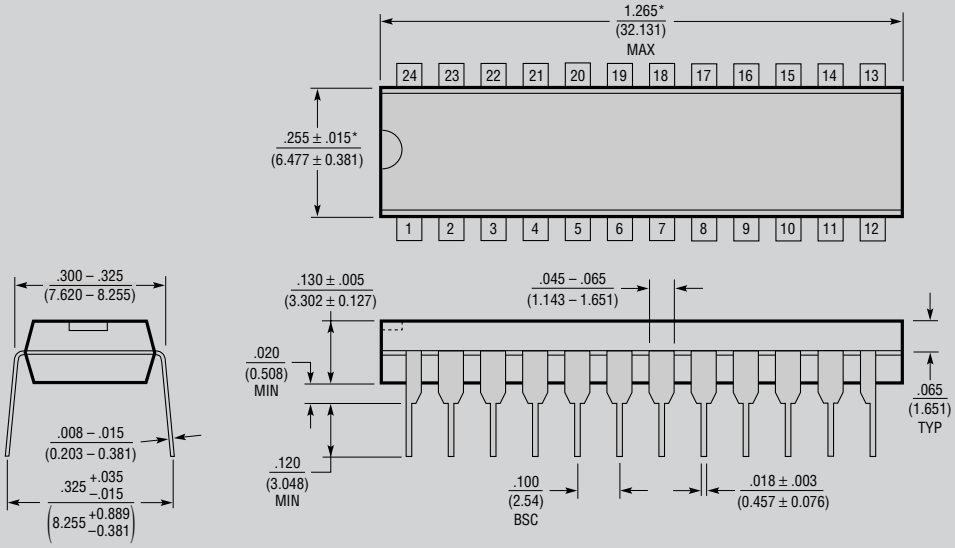
N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package
24-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



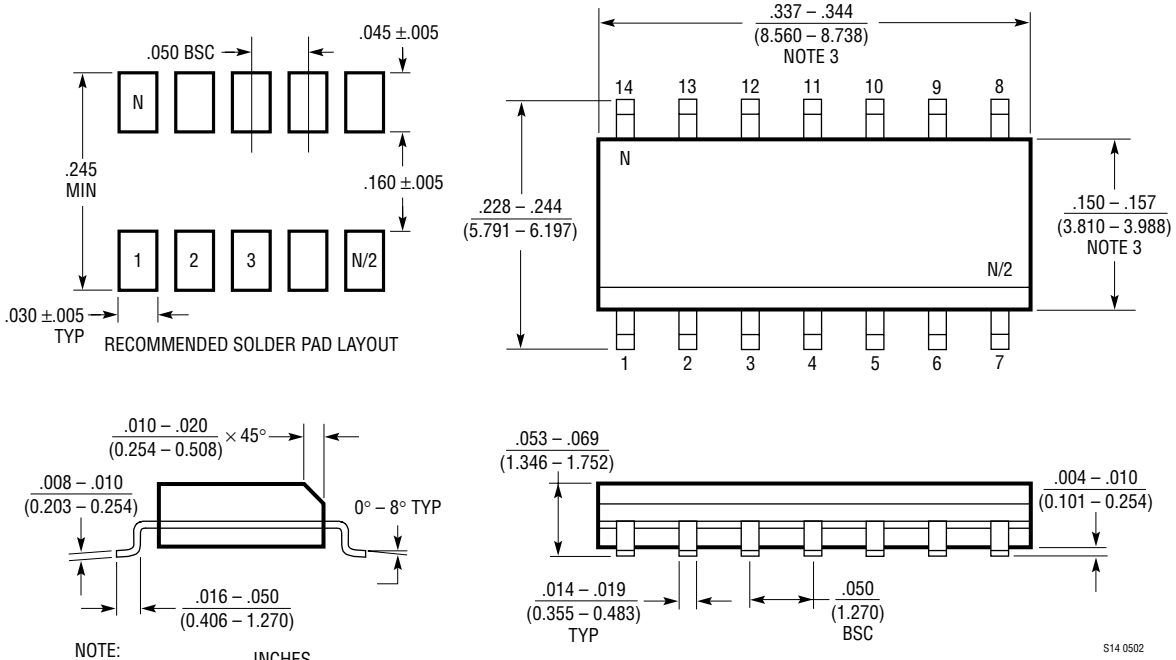
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

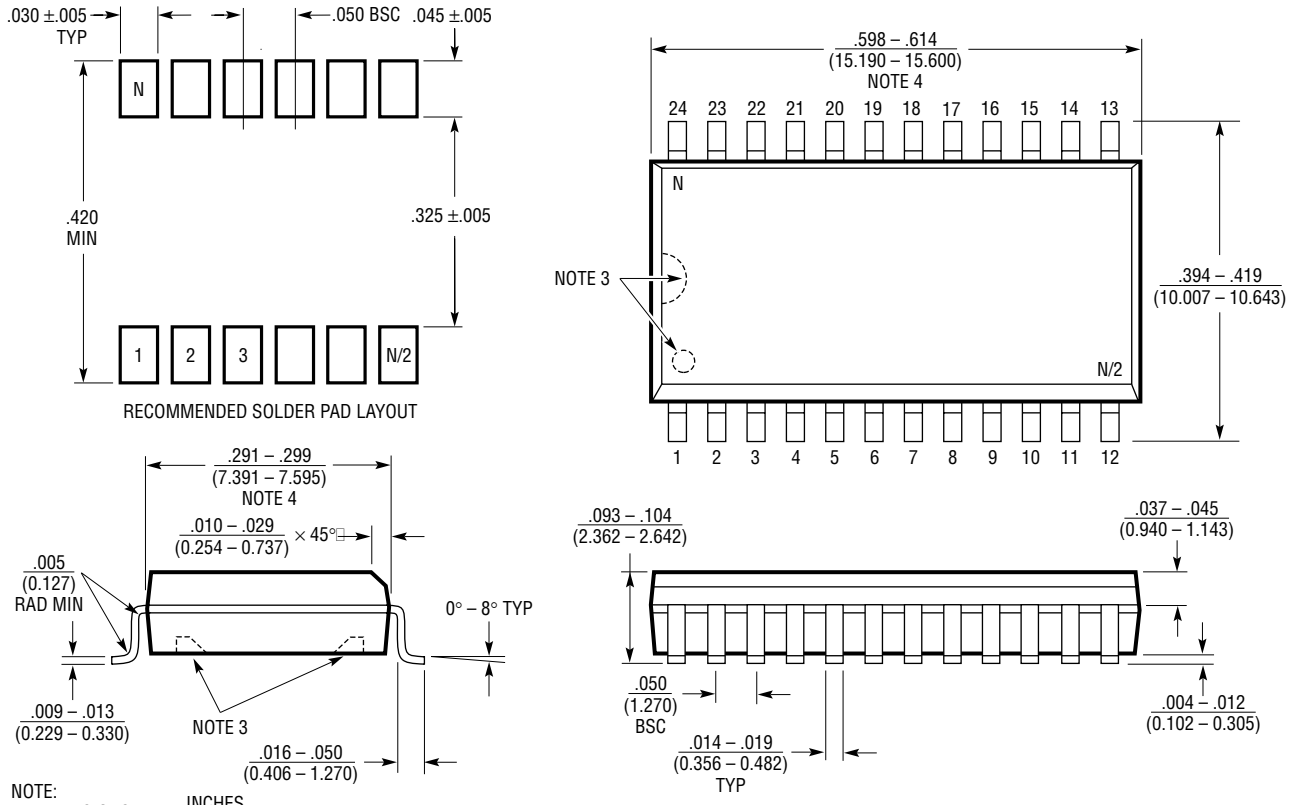
S Package
14-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

PACKAGE DESCRIPTION

SW Package
24-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1158	Half-Bridge N-Channel Power MOSFET Driver	Single Input, Continuous Current Protection and Internal Charge Pump for DC Operation
LT1336	Half-Bridge N-Channel Power MOSFET Driver with Boost Regulator	Onboard Boost Regulator to Supply the High Side Driver
LT1910	Protected High Side MOSFET Driver	V_{IN} = 8V to 48V, Protected from –15V to 60V Transients, Auto Restart, Fault Indication
LTC1922-1	Synchronous Phase Modulated Full-Bridge Controller	Output Power from 50W to Kilowatts, Adaptive Direct Sense Zero Voltage Switching Compensates for External Component Tolerances
LTC1923	Full-Bridge Controller for Thermoelectric Coolers	High Efficiency, Adjustable Slew Rate Reduces EMI 5mm × 5mm QFN and 28-Pin SSOP

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