



THE DATASHEET OF CD4020BCN



CD4020BC • CD4040BC • CD4060BC
14-Stage Ripple Carry Binary Counters •
12-Stage Ripple Carry Binary Counters •
14-Stage Ripple Carry Binary Counters

General Description

The CD4020BC, CD4060BC are 14-stage ripple carry binary counters, and the CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

Features

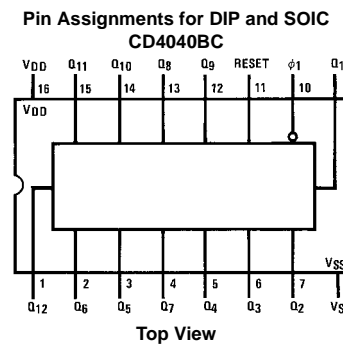
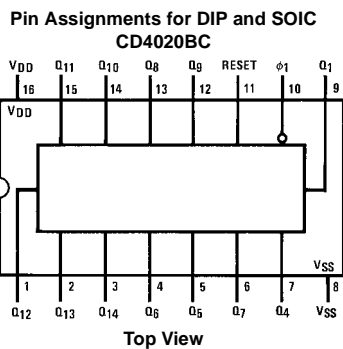
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation: 8 MHz typ. at V_{DD} = 10V
- Schmitt trigger clock input

Ordering Code:

Order Number	Package Number	Package Description
CD4020BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4020BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4040BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4040BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4060BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4060BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

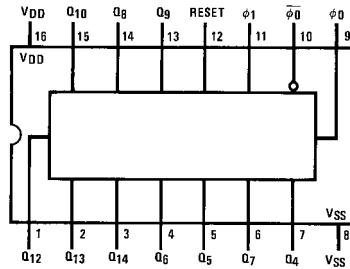
Connection Diagrams



CD4020BC • CD4040BC • CD4060BC 14-Stage Ripple Carry Binary Counters • 12-Stage Ripple Carry Binary Counters • 14-Stage Ripple Carry Binary Counters

Connection Diagrams (Continued)

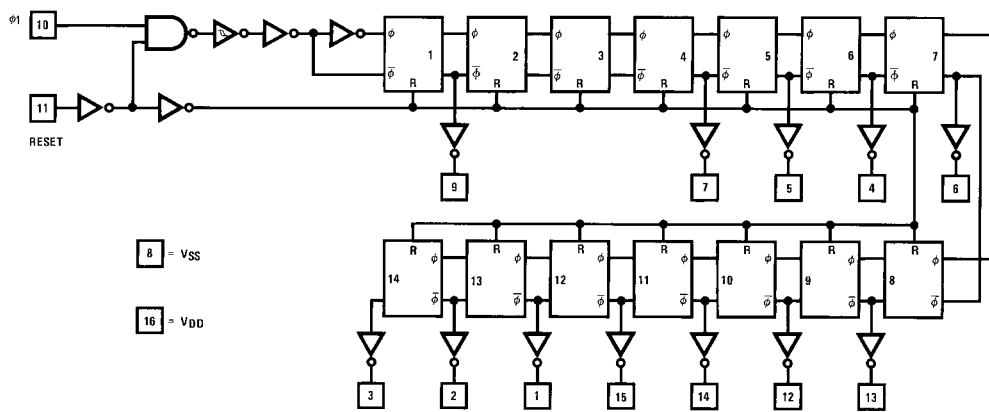
Pin Assignments for DIP and SOIC
CD4060BC



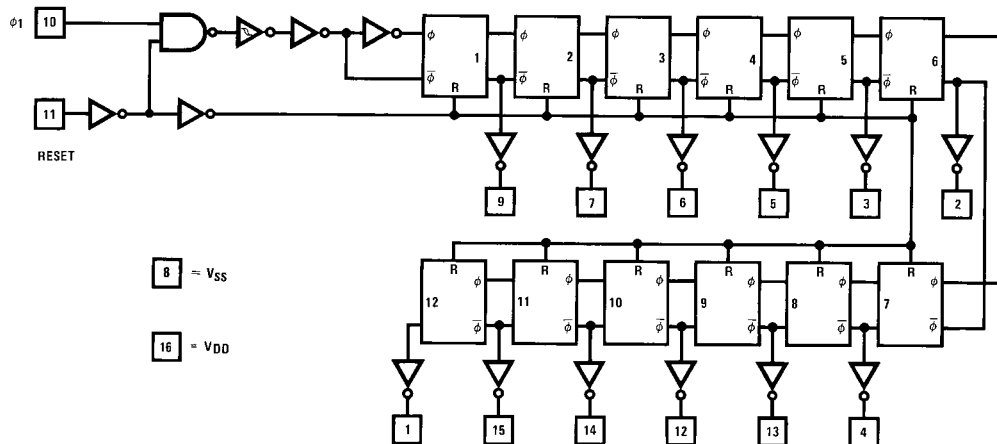
Top View

Schematic Diagrams

CD4020BC



CD4040BC



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{DD})	-0.5V to +18V
Input Voltage (V_{IN})	-0.5V to $V_{DD} + 0.5V$
Storage Temperature Range (T_S)	-65°C to +150°C
Package Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3V to +15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	-55°C to +125°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		5 10 20			5 10 20		150 300 600	μA
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V		1.5 3.0 4.0		2 4 6	1.5 3.0 4.0		1.5 3.0 4.0	V
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	3 6 9		3.5 7.0 11.0		V
I_{OL}	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1		-10^{-5} 10^{-5}	-0.1 0.1		-1.0 1.0	μA

Note 3: Data does not apply to oscillator points ϕ_0 and $\phi_{\bar{0}}$ of CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)						
CD4020BC, CD4040BC $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		250 100 75	550 210 150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		150 60 45	330 125 90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		125 50 40	335 125 100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$			No Limit No Limit No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	1.5 4 5	4 10 12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 100 80	450 210 170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 100 80	450 210 170	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Note 5)CD4060BC $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, $t_r = t_f = 20\text{ ns}$, unless otherwise noted

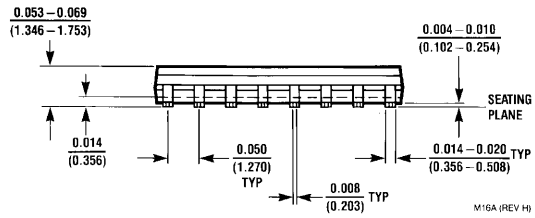
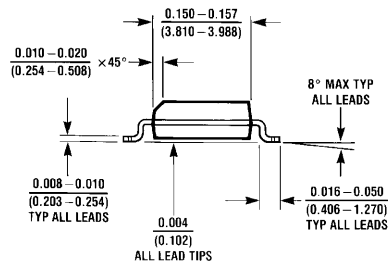
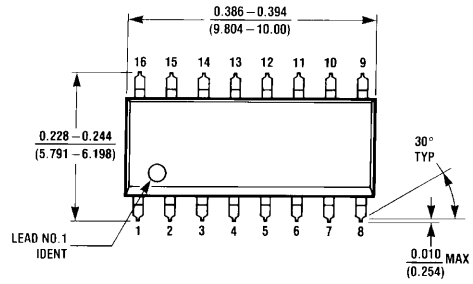
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL4} , t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		550 250 200	1300 525 400	ns
t_{PHL} , t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		150 60 45	330 125 90	ns
t_{THL} , t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns
t_{WL} , t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		170 65 50	500 170 125	ns
t_{rCL} , t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$			No Limit No Limit No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	1 3 4	3 8 10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 100 80	450 210 170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 100 80	450 210 170	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

RC Oscillator Notes:

- $R_2 = 2 R_1$ to $10 R_1$
- RC Oscillator applications are not recommended at supply voltages below 7.0V for $R_1 < 50\text{ k}\Omega$
- $f \approx \frac{1}{2.2 R_1 C_X}$ at $V_{CC} = 10\text{V}$

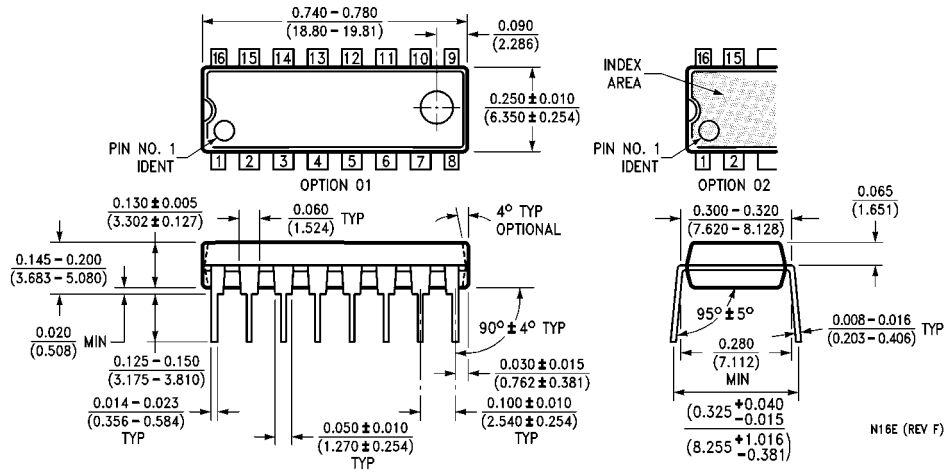
Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

M16A (REV H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View CD4020BCN on WIN SOURCE](#)
- ⊖ [Fairchild/ON Semiconductor Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management