



THE DATASHEET OF CD4019BE



CD4019B Types

CMOS Quad AND/OR Select Gate

High-Voltage Types (20-Volt Rating)

■ CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical $A + B$ function.

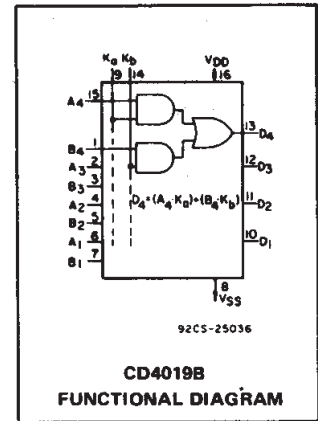
The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|--|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | -0.5V to +20V |
| Voltages referenced to V_{SS} Terminal | |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to $V_{DD} + 0.5V$ |
| DC INPUT CURRENT, ANY ONE INPUT | $\pm 10mA$ |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55^\circ C$ to $+100^\circ C$ | 500mW |
| For $T_A = +100^\circ C$ to $+125^\circ C$ | Derate Linearly at 12mW/ $^\circ C$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T_A) | $-55^\circ C$ to $+125^\circ C$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | $-65^\circ C$ to $+150^\circ C$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79mm$) from case for 10s max | $+265^\circ C$ |

Features:

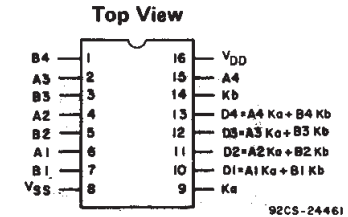
- Medium-speed operation
... $t_{PHL} = t_{PLH} = 60$ ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25 $^\circ C$
- Noise margin (full package-temperature range) =
 1 V at $V_{DD} = 5$ V
 2 V at $V_{DD} = 10$ V
 2.5 V at $V_{DD} = 15$ V



Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

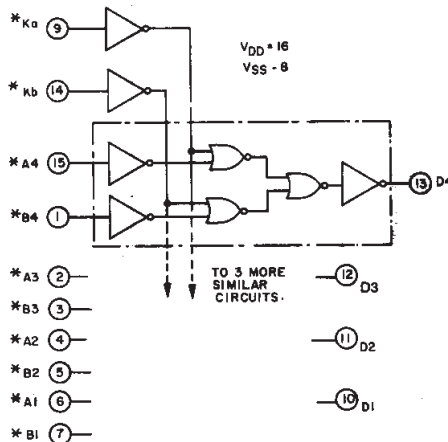
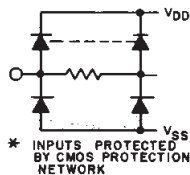
TERMINAL DIAGRAM



TRUTH TABLE

| K_A | K_B | A_n | B_n | D_n |
|-------|-------|-------|-------|-------|
| 1 | 0 | 1 | X | 1 |
| 1 | 0 | 0 | X | 0 |
| 0 | 1 | X | 1 | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 0 | X | X | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

X = Don't Care



92CS-39272

Fig. 1—Logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | Min. | Max. | Units |
|---|--------------|------|------|-------|
| Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) | - | 3 | 18 | V |

CD4019B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 1 | 1 | 30 | 30 | - | 0,02 | 1 | μA |
| | - | 0,10 | 10 | 2 | 2 | 60 | 60 | - | 0,02 | 2 | |
| | - | 0,15 | 15 | 4 | 4 | 120 | 120 | - | 0,02 | 4 | |
| | - | 0,20 | 20 | 20 | 20 | 600 | 600 | - | 0,04 | 20 | |
| Output Low (Sink) Current I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | - | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | - | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | - | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | - | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | - | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0,5 | 5 | | | 0,05 | | | 0 | 0,05 | V |
| | - | 0,10 | 10 | | | 0,05 | | | | 0,05 | |
| | - | 0,15 | 15 | | | 0,05 | | | 0 | 0,05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0,5 | 5 | | | 4,95 | | | 4,95 | 5 | V |
| | - | 0,10 | 10 | | | 9,95 | | | 9,95 | 10 | |
| | - | 0,15 | 15 | | | 14,95 | | | 14,95 | 15 | |
| Input Low Voltage, V _{IL} Max. | 0,5, 4,5 | - | 5 | | | 1,5 | | | - | 1,5 | V |
| | 1,9 | - | 10 | | | 3 | | | - | 3 | |
| | 1,5, 13,5 | - | 15 | | | 4 | | | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0,5, 4,5 | - | 5 | | | 3,5 | | | 3,5 | - | V |
| | 1,9 | - | 10 | | | 7 | | | 7 | - | |
| | 1,5, 13,5 | - | 15 | | | 11 | | | 11 | - | |
| Input Current I _{IN} Max. | - | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0,1 | μA |

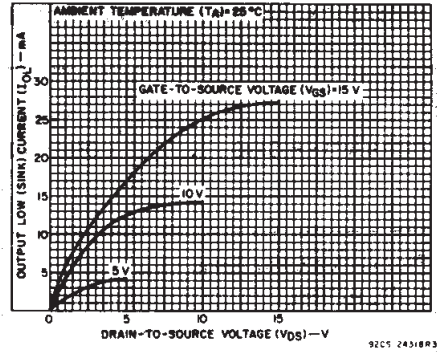


Fig. 2 - Typical output low (sink) current characteristics.

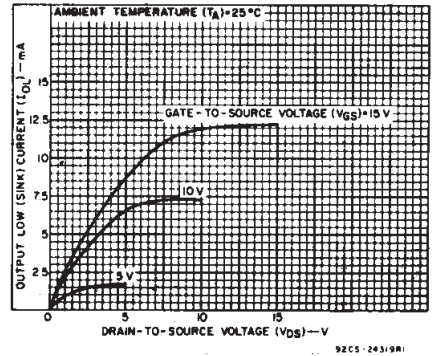


Fig. 3 - Minimum output low (sink) current characteristics.

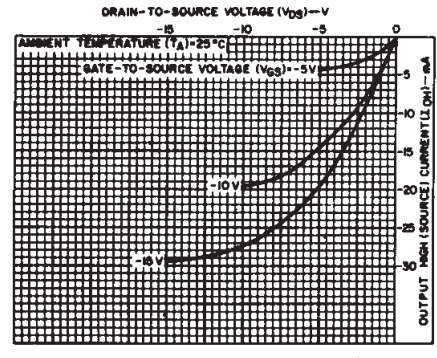


Fig. 4 - Typical output high (source) current characteristics.

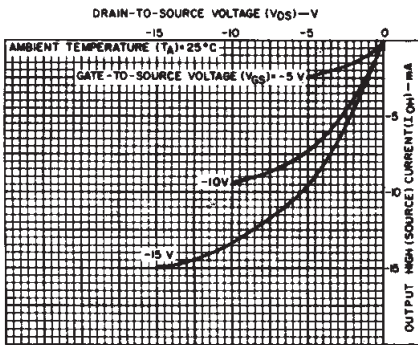


Fig. 5 - Minimum output high (source) current characteristics.

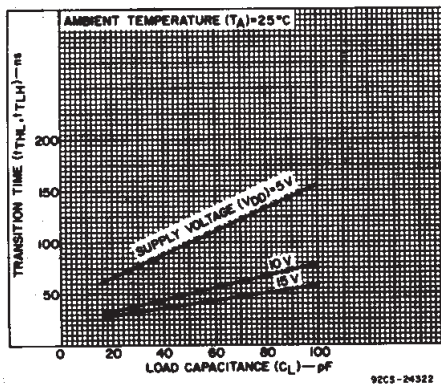


Fig. 6 - Typical transition time as a function of load capacitance.

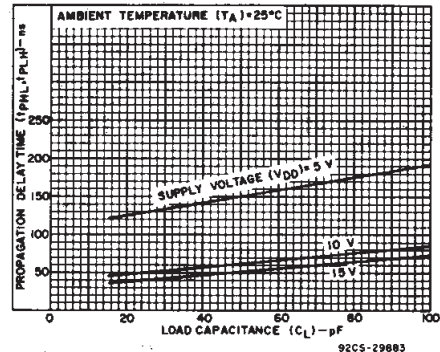


Fig. 7 - Propagation delay time as a function of load capacitance.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4019B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|--|------------------------|---------|------|------|-------|------|
| | | VDD (V) | Min. | Typ. | | Max. |
| Propagation Delay Time; t_{PLH}, t_{PHL} | | 5 | — | 150 | 300 | ns |
| | | 10 | — | 60 | 120 | |
| | | 15 | — | 50 | 100 | |
| Transition Time; t_{THL}, t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Input Capacitance, C_{IN} | All A and B Inputs | — | 5 | 7.5 | pF | |
| | K_a and K_b Inputs | — | 10 | 15 | pF | |

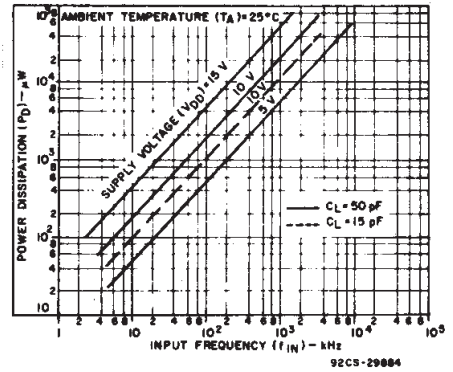


Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

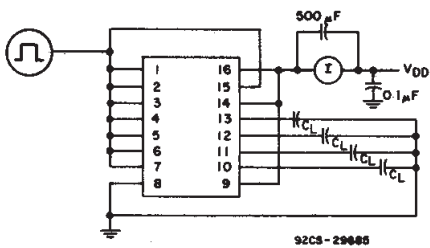


Fig. 9 — Dynamic power dissipation test circuit.

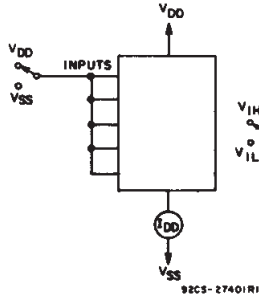


Fig. 10 — Quiescent device current test circuit.

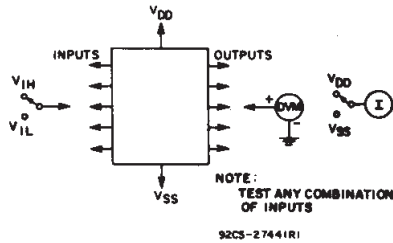


Fig. 11 — Input voltage test circuit.

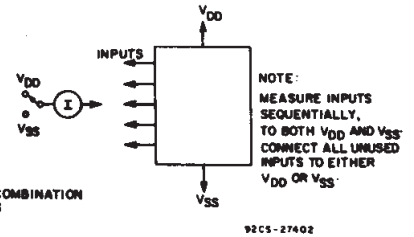


Fig. 12 — Input current test circuit.

TYPICAL APPLICATIONS

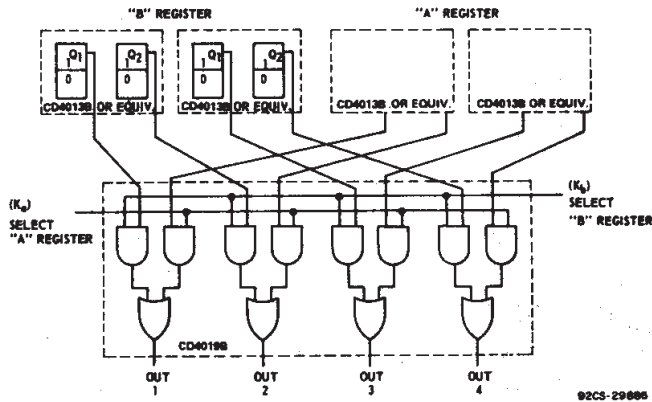


Fig. 13 — AND/OR select gating.

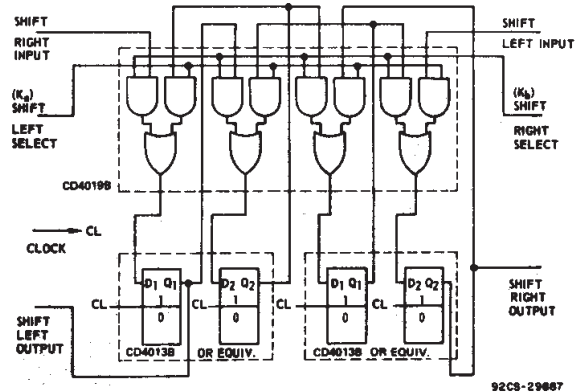


Fig. 14 — "Shift left/shift right" register.

CD4019B Types

TYPICAL APPLICATIONS (CONT'D)

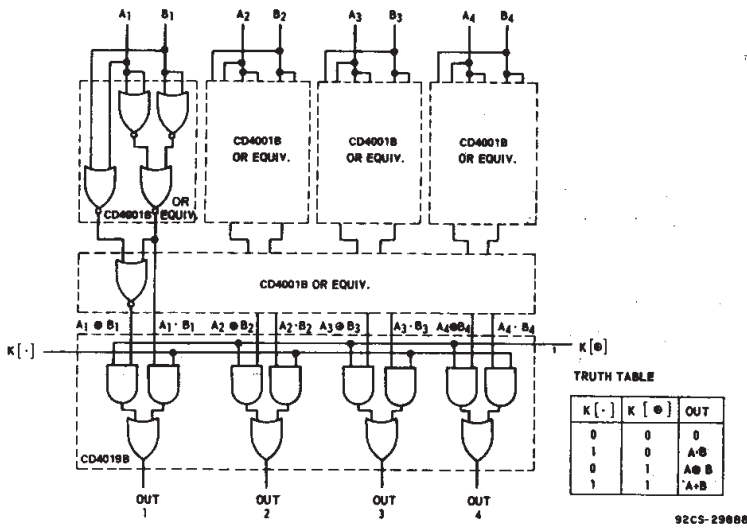


Fig. 15 - AND/OR Exclusive-OR selector.

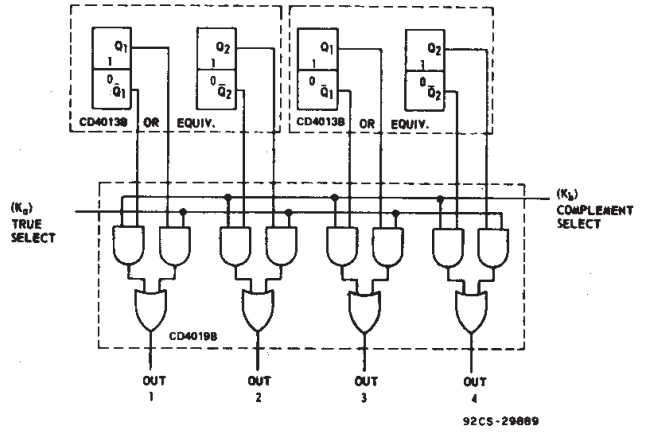
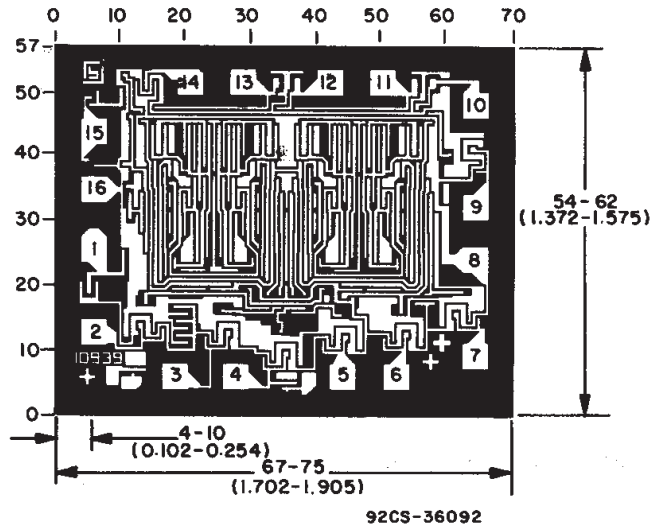


Fig. 16 - "True complement" selector.



Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4019BE | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4019BE | Samples |
| CD4019BEE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4019BE | Samples |
| CD4019BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4019BF | Samples |
| CD4019BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4019BF3A | Samples |
| CD4019BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4019BM | Samples |
| CD4019BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4019BM | Samples |
| CD4019BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4019BM | Samples |
| CD4019BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4019B | Samples |
| CD4019BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM019B | Samples |
| JM38510/05352BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 05352BEA | Samples |
| M38510/05352BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 05352BEA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4019B, CD4019B-MIL :

- Catalog: [CD4019B](#)
- Military: [CD4019B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4019BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4019BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4019BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4019BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4019BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4019BPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CD4019BE](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management