



THE DATASHEET OF CD4018BE



CD4018B Types

CMOS Presettable Divide-By-'N' Counter

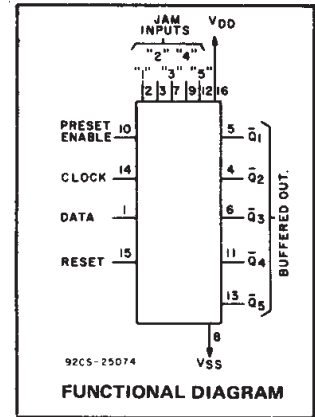
High-Voltage Types (20-Volt Rating)

■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\bar{Q}5$, $\bar{Q}4$, $\bar{Q}3$, $\bar{Q}2$, $\bar{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

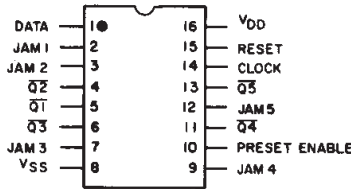
The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Medium speed operation 10 MHz (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5\text{ V}$
 - 2 V at $V_{DD} = 10\text{ V}$
 - 2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL DIAGRAM
Top View



92CS-24460

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|--|--|
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | |
| Voltages referenced to V_{SS} Terminal) | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to $V_{DD} + 0.5\text{V}$ |
| DC INPUT CURRENT, ANY ONE INPUT | $\pm 10\text{mA}$ |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ | 500mW |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ | 100mW |
| OPERATING-TEMPERATURE RANGE (T_A) | -55°C to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE (T_{stg}) | -65°C to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max | $+265^\circ\text{C}$ |

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4018B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Unless Otherwise Specified
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC | V_{DD} | Min. | Max. | UNITS |
|--|----------|-----------|------|---------------|
| Supply Voltage Range (at $T_A =$ Full Package-Temperature Range) | | 3 | 18 | V |
| Clock Input Frequency, f_{CL} | 5 | — | 3 | MHz |
| | 10 | — | 7 | |
| | 15 | — | 8.5 | |
| Clock Pulse Width, t_W | 5 | 160 | — | ns |
| | 10 | 70 | — | |
| | 15 | 50 | — | |
| Clock Rise & Fall Time, t_{rCL}, t_{fCL} | 5 | Unlimited | | μs |
| | 10 | | | |
| | 15 | | | |
| Data Input Set-Up Time, t_S | 5 | 40 | — | ns |
| | 10 | 12 | — | |
| | 15 | 16 | — | |
| Data Input Hold Time, t_H | 5 | 140 | — | ns |
| | 10 | 80 | — | |
| | 15 | 60 | — | |
| Preset or Reset Pulse Width, t_W | 5 | 160 | — | ns |
| | 10 | 70 | — | |
| | 15 | 50 | — | |
| Preset or Reset Removal Time | 5 | 160 | — | ns |
| | 10 | 60 | — | |
| | 15 | 40 | — | |

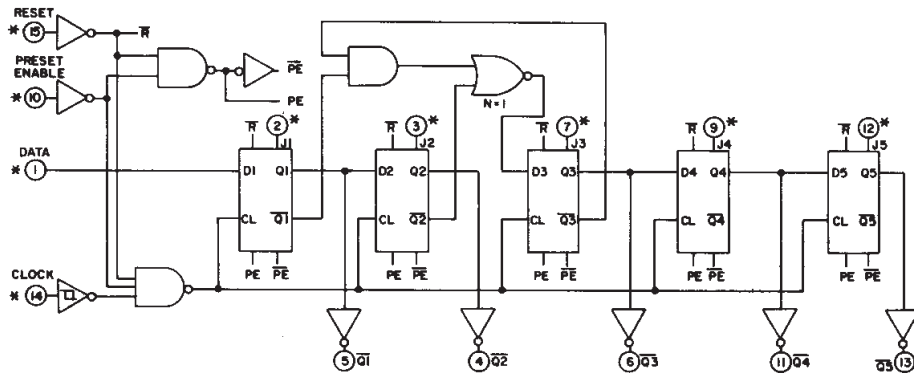
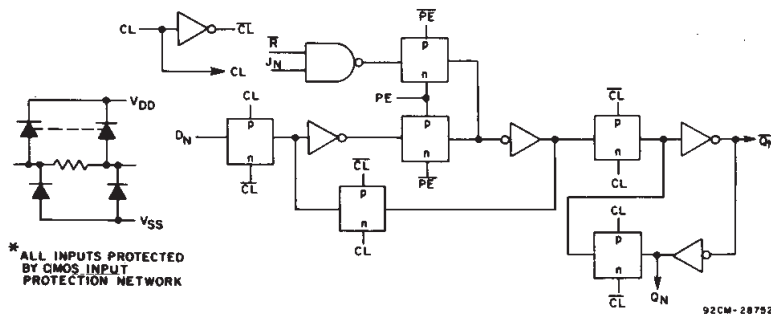


Fig. 1 - Logic diagram.



* ALL INPUTS PROTECTED BY CMOS INPUT PROTECTION NETWORK

92CM-28752

Fig. 2 - Detail of a typical stage.

CD4018B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | -55 | -40 | +85 | +125 | +25 | | | |
| | | | | | | | | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | - | 0,5 | 5 | 5 | 5 | 150 | 150 | - | 0,04 | 5 | μA |
| | - | 0,10 | 10 | 10 | 10 | 300 | 300 | - | 0,04 | 10 | |
| | - | 0,15 | 15 | 20 | 20 | 600 | 600 | - | 0,04 | 20 | |
| | - | 0,20 | 20 | 100 | 100 | 3000 | 3000 | - | 0,08 | 100 | |
| Output Low (Sink) Current, I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | - | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | - | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | - | |
| Output High (Source) Current, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | - | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | - | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | - | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | - | |
| Output Voltage: Low-Level, V _{OL} Max. | - | 0,5 | 5 | 0,05 | | | | - | 0 | 0,05 | V |
| | - | 0,10 | 10 | 0,05 | | | | - | 0 | 0,05 | |
| | - | 0,15 | 15 | 0,05 | | | | - | 0 | 0,05 | |
| Output Voltage: High-Level, V _{OH} Min. | - | 0,5 | 5 | 4,95 | | | | 4,95 | 5 | - | V |
| | - | 0,10 | 10 | 9,95 | | | | 9,95 | 10 | - | |
| | - | 0,15 | 15 | 14,95 | | | | 14,95 | 15 | - | |
| Input Low Voltage, V _{IL} Max. | 0,5,4,5 | - | 5 | 1,5 | | | | - | - | 1,5 | V |
| | 1,9 | - | 10 | 3 | | | | - | - | 3 | |
| | 1,5,13,5 | - | 15 | 4 | | | | - | - | 4 | |
| Input High Voltage, V _{IH} Min. | 0,5,4,5 | - | 5 | 3,5 | | | | 3,5 | - | - | V |
| | 1,9 | - | 10 | 7 | | | | 7 | - | - | |
| | 1,5,13,5 | - | 15 | 11 | | | | 11 | - | - | |
| Input Current, I _{IN} Max. | - | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | - | ±10 ⁻⁵ | ±0,1 | μA |

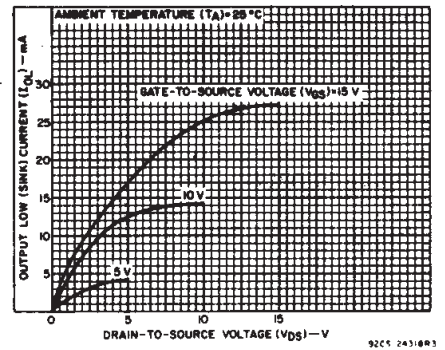


Fig. 3 - Typical output low (sink) current characteristics.

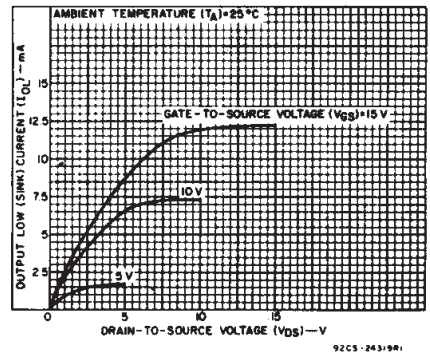


Fig. 4 - Minimum output low (sink) current characteristics.

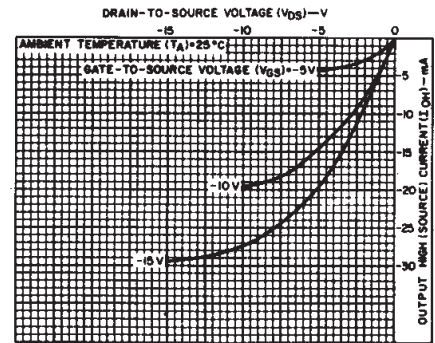


Fig. 5 - Typical output high (source) current characteristics.

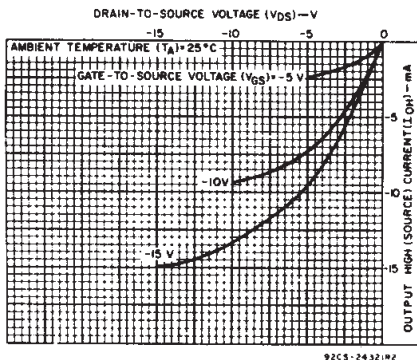


Fig. 6 - Minimum output high (source) current characteristics.

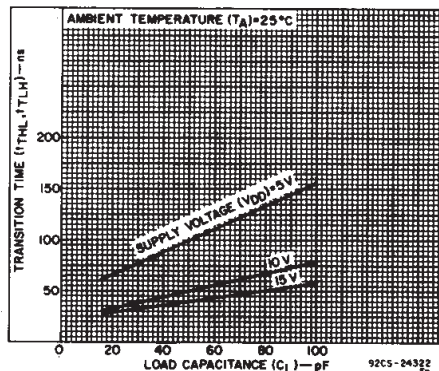


Fig. 7 - Typical transition time as a function of load capacitance.

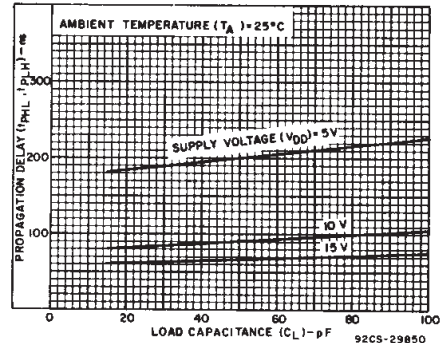


Fig. 8 - Typical propagation delay time as a function of load capacitance (CLOCK to Q).

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CD4018B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$,
 $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|---|-----------------|--------------|-----------|------|-------|---------------|
| | | V_{DD} (V) | Min. | Typ. | | Max. |
| CLOCKED OPERATION | | | | | | |
| Propagation Delay Time; t_{PLH}, t_{PHL} | | 5 | — | 200 | 400 | ns |
| | | 10 | — | 90 | 180 | |
| | | 15 | — | 65 | 130 | |
| Transition Time; t_{THL}, t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Maximum Clock Input Frequency, f_{CL} | | 5 | 3 | 6 | — | MHz |
| | | 10 | 7 | 14 | — | |
| | | 15 | 8.5 | 17 | — | |
| Minimum Clock Pulse Width, t_W | | 5 | — | 80 | 160 | ns |
| | | 10 | — | 35 | 70 | |
| | | 15 | — | 25 | 50 | |
| Clock Rise & Fall Time; t_{rCL}, t_{fCL} | | 5 | Unlimited | | | μs |
| | | 10 | | | | |
| | | 15 | | | | |
| Minimum Data Input Set-Up Time, t_S | | 5 | — | 20 | 40 | ns |
| | | 10 | — | 6 | 12 | |
| | | 15 | — | 3 | 6 | |
| Minimum Data Input Hold Time, t_H | | 5 | — | 70 | 140 | ns |
| | | 10 | — | 40 | 80 | |
| | | 15 | — | 30 | 60 | |
| Average Input Capacitance, C_I | Any Input | — | 5 | 7.5 | pF | |
| PRESET* OR RESET OPERATION | | | | | | |
| Propagation Delay Time; Preset or Reset to \bar{Q} t_{PLH}, t_{PHL} | | 5 | — | 275 | 550 | ns |
| | | 10 | — | 125 | 250 | |
| | | 15 | — | 90 | 180 | |
| Minimum Preset or Reset Pulse Width, t_W | | 5 | — | 80 | 160 | ns |
| | | 10 | — | 35 | 70 | |
| | | 15 | — | 25 | 50 | |
| Minimum Preset or Reset Removal Time | | 5 | — | 80 | 160 | ns |
| | | 10 | — | 30 | 60 | |
| | | 15 | — | 20 | 40 | |

* At PRESET ENABLE or JAM Inputs.

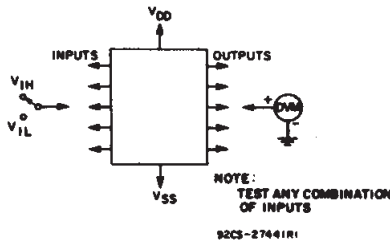


Fig. 12 — Input voltage test circuit.

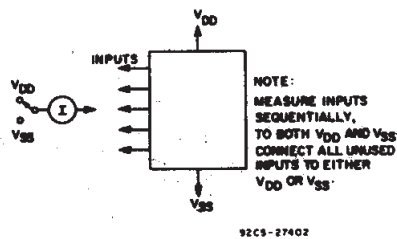


Fig. 13 — Input current test circuit.

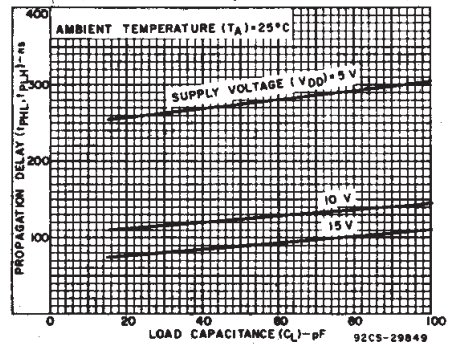


Fig. 9 — Typical propagation delay time as a function of load capacitance (RESET to Q).

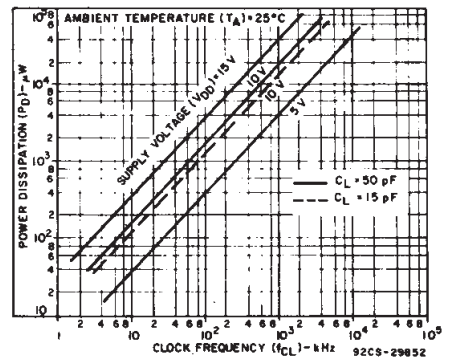


Fig. 10 — Typical dynamic power dissipation as a function of clock input frequency.

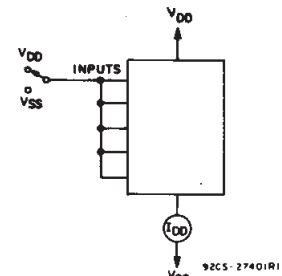


Fig. 11 — Quiescent device current test circuit.

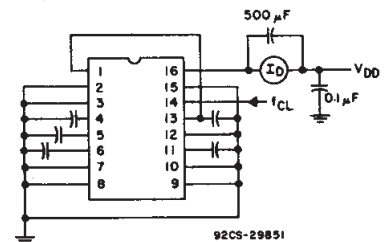
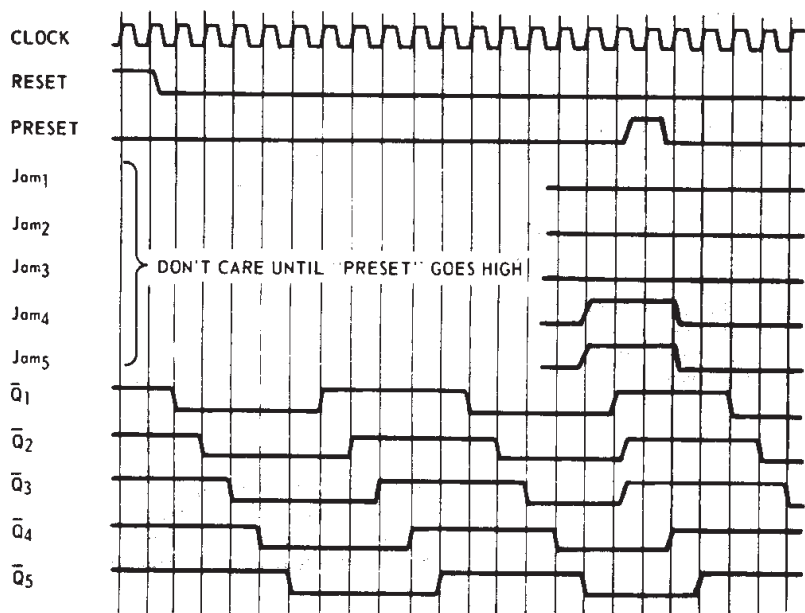


Fig. 14 — Dynamic power dissipation test circuit.

CD4018B Types

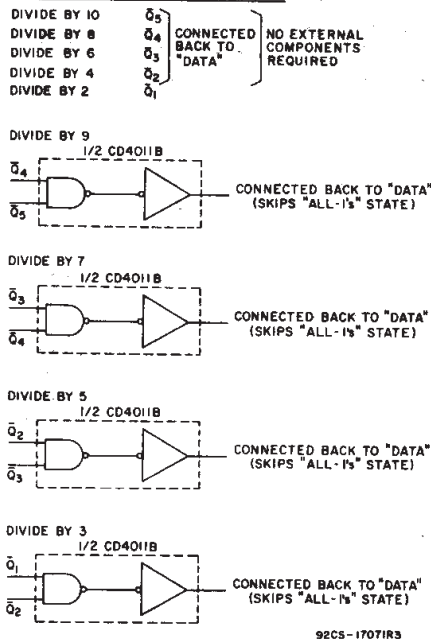
("DATA" INPUT TIED TO \bar{Q}_5 FOR DECADE COUNTER CONFIGURATION)



92SS-4148R2

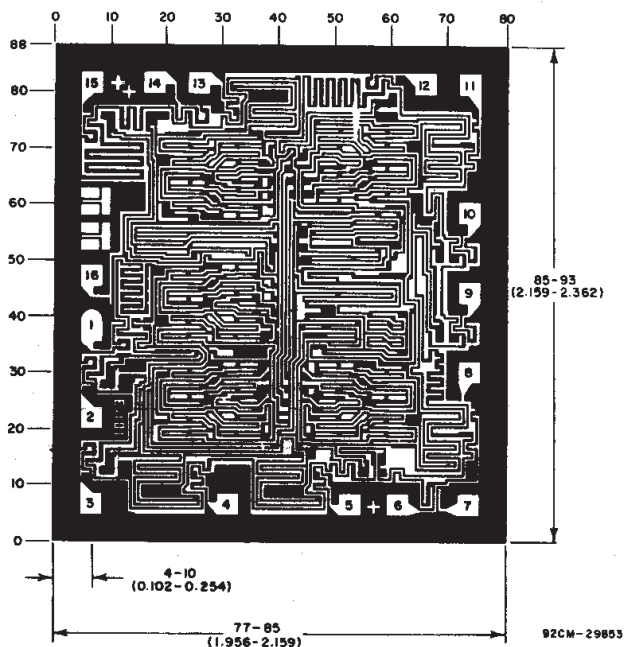
Fig. 15 — Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION



92CS-1707IR3

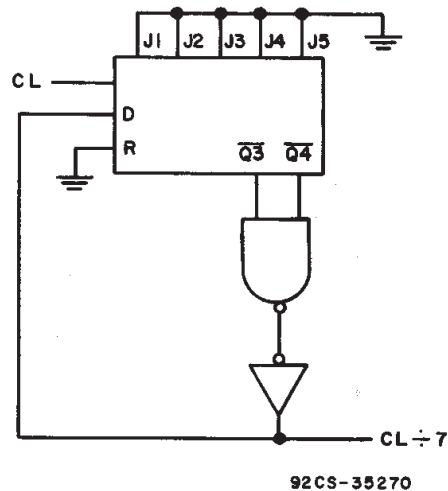
Fig. 16 — External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.



92CM-29853

Chip dimensions and pad layout for CD4018B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



92CS-35270

Fig. 17 — Example of divide by 7.

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4018BE | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4018BE | Samples |
| CD4018BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4018BF | Samples |
| CD4018BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4018BF3A | Samples |
| CD4018BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4018BM | Samples |
| CD4018BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4018BM | Samples |
| CD4018BMT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4018BM | Samples |
| CD4018BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4018B | Samples |
| CD4018BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM018B | Samples |
| CD4018BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM018B | Samples |
| JM38510/05652BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 05652BEA | Samples |
| M38510/05652BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 05652BEA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4018B, CD4018B-MIL :

- Catalog: [CD4018B](#)
- Military: [CD4018B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4018BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4018BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4018BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4018BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

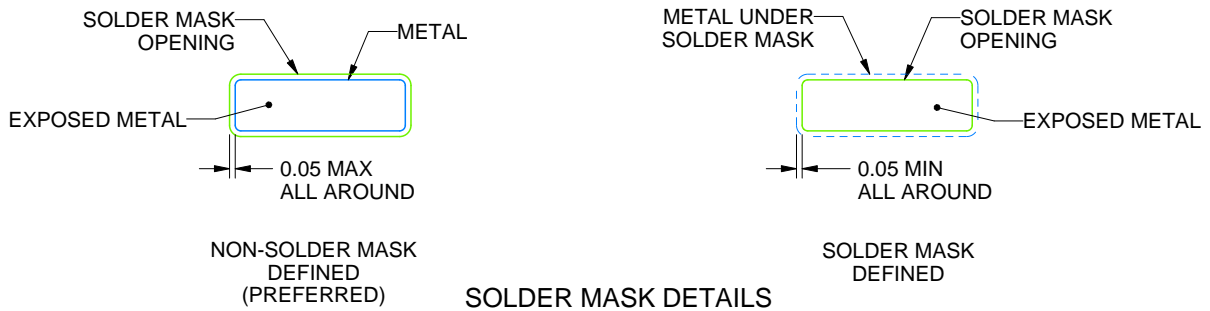
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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