



**THE DATASHEET OF
CC3200R1M2RGCR**



CC3200 SimpleLink™ Wi-Fi® and Internet-of-Things Solution, a Single-Chip Wireless MCU

1 Device Overview

1.1 Features

- CC3200 SimpleLink Wi-Fi—Consists of Applications Microcontroller, Wi-Fi Network Processor, and Power-Management Subsystems
- Wi-Fi CERTIFIED™ Chip
- Applications Microcontroller Subsystem
 - ARM® Cortex®-M4 Core at 80 MHz
 - Embedded Memory
 - RAM (Up to 256KB)
 - External Serial Flash Bootloader, and Peripheral Drivers in ROM
 - 32-Channel Direct Memory Access (μDMA)
 - Hardware Crypto Engine for Advanced Fast Security, Including
 - AES, DES, and 3DES
 - SHA2 and MD5
 - CRC and Checksum
 - 8-Bit Parallel Camera Interface
 - 1 Multichannel Audio Serial Port (McASP) Interface with Support for Two I2S Channels
 - 1 SD/MMC Interface
 - 2 Universal Asynchronous Receivers and Transmitters (UARTs)
 - 1 Serial Peripheral Interface (SPI)
 - 1 Inter-Integrated Circuit (I²C)
 - 4 General-Purpose Timers with 16-Bit Pulse-Width Modulation (PWM) Mode
 - 1 Watchdog Timer
 - 4-Channel 12-Bit Analog-to-Digital Converters (ADCs)
 - Up to 27 Individually Programmable, Multiplexed GPIO Pins
- Dedicated External SPI Interface for Serial Flash
- Wi-Fi Network Processor Subsystem
 - Featuring Wi-Fi Internet-On-a-Chip™
 - Dedicated ARM MCU
 - Completely Offloads Wi-Fi and Internet Protocols from the Application Microcontroller
 - Wi-Fi and Internet Protocols in ROM
 - 802.11 b/g/n Radio, Baseband, Medium Access Control (MAC), Wi-Fi Driver, and Supplicant
 - TCP/IP Stack
 - Industry-Standard BSD Socket Application
- Programming Interfaces (APIs)
 - 8 Simultaneous TCP or UDP Sockets
 - 2 Simultaneous TLS and SSL Sockets
- Powerful Crypto Engine for Fast, Secure Wi-Fi and Internet Connections with 256-Bit AES Encryption for TLS and SSL Connections
- Station, AP, and Wi-Fi Direct® Modes
- WPA2 Personal and Enterprise Security
- SimpleLink Connection Manager for Autonomous and Fast Wi-Fi Connections
- SmartConfig™ Technology, AP Mode, and WPS2 for Easy and Flexible Wi-Fi Provisioning
- TX Power
 - 18.0 dBm @ 1 DSSS
 - 14.5 dBm @ 54 OFDM
- RX Sensitivity
 - –95.7 dBm @ 1 DSSS
 - –74.0 dBm @ 54 OFDM
- Application Throughput
 - UDP: 16 Mbps
 - TCP: 13 Mbps
- Power-Management Subsystem
 - Integrated DC-DC Supports a Wide Range of Supply Voltage:
 - V_{BAT} Wide-Voltage Mode: 2.1 to 3.6 V
 - VIO is Always Tied with VBAT
 - Preregulated 1.85-V Mode
 - Advanced Low-Power Modes
 - Hibernate: 4 μA
 - Low-Power Deep Sleep (LPDS): 250 μA
 - RX Traffic (MCU Active): 59 mA @ 54 OFDM
 - TX Traffic (MCU Active): 229 mA @ 54 OFDM, Maximum Power
 - Idle Connected (MCU in LPDS): 825 μA @ DTIM = 1
- Clock Source
 - 40.0-MHz Crystal with Internal Oscillator
 - 32.768-kHz Crystal or External RTC Clock
- Package and Operating Temperature
 - 0.5-mm Pitch, 64-Pin, 9-mm x 9-mm QFN
 - Ambient Temperature Range: –40°C to 85°C



1.2 Applications

- For Internet-of-Things applications, such as:
 - Cloud Connectivity
 - Home Automation
 - Home Appliances
 - Access Control
 - Security Systems
 - Smart Energy
 - Internet Gateway
 - Industrial Control
 - Smart Plug and Metering
 - Wireless Audio
 - IP Network Sensor Nodes

1.3 Description

Start your design with the industry's first Wi-Fi CERTIFIED single-chip microcontroller unit (MCU) with built-in Wi-Fi connectivity. Created for the Internet of Things (IoT), the SimpleLink CC3200 device is a wireless MCU that integrates a high-performance ARM Cortex-M4 MCU, allowing customers to develop an entire application with a single IC. With on-chip Wi-Fi, Internet, and robust security protocols, no prior Wi-Fi experience is required for faster development. The CC3200 device is a complete platform solution including software, sample applications, tools, user and programming guides, reference designs, and the TI E2E™ support community. The device is available in a QFN package that is easy to layout.

The applications MCU subsystem contains an industry-standard ARM Cortex-M4 core running at 80 MHz. The device includes a wide variety of peripherals, including a fast parallel camera interface, I2S, SD/MMC, UART, SPI, I²C, and four-channel ADC. The CC3200 family includes flexible embedded RAM for code and data and ROM with external serial flash bootloader and peripheral drivers.

The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a-Chip and contains an additional dedicated ARM MCU that completely offloads the applications MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3200 device supports Station, Access Point, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi Internet-on-a-chip includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols.

The power-management subsystem includes integrated DC-DC converters supporting a wide range of supply voltages. This subsystem enables low-power consumption modes, such as the hibernate with RTC mode requiring less than 4 μ A of current.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|---------------------------------|----------|-----------------|
| CC3200R1MXRGCR/T ⁽²⁾ | QFN (64) | 9.0 mm x 9.0 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) X = 1 (128KB RAM) or 2 (256KB RAM)

1.4 Functional Block Diagram

Figure 1-1 shows the CC3200 hardware overview.

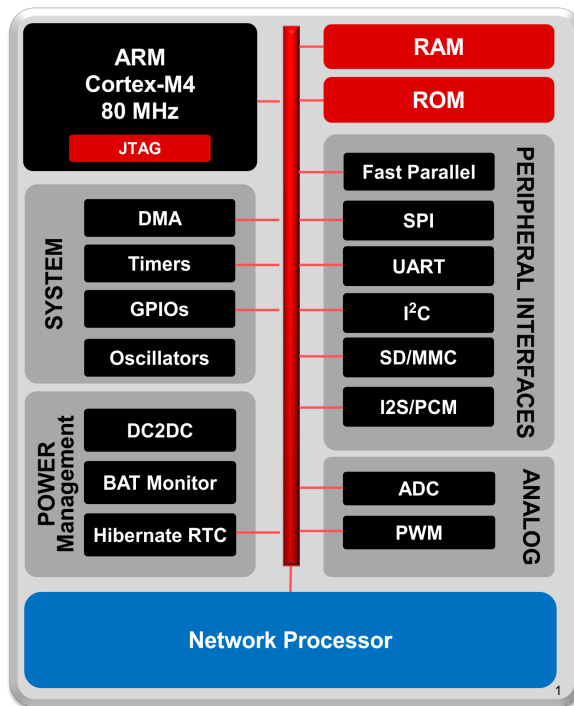


Figure 1-1. CC3200 Hardware Overview

Figure 1-2 shows an overview of the CC3200 embedded software.

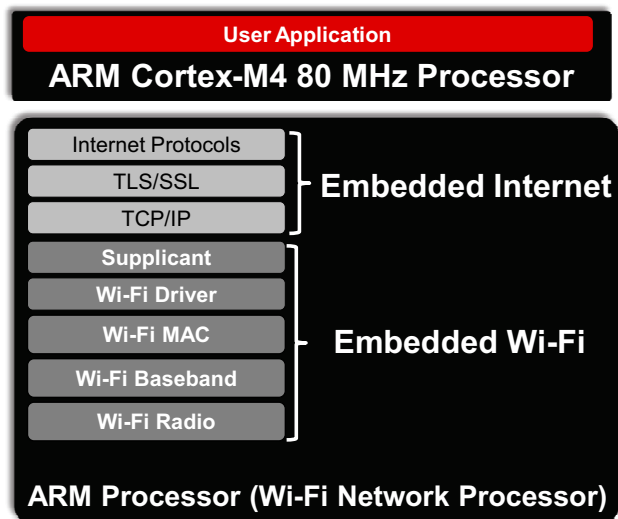


Figure 1-2. CC3200 Embedded Software Overview

Figure 1-3 shows a block diagram of the CC3200 device.

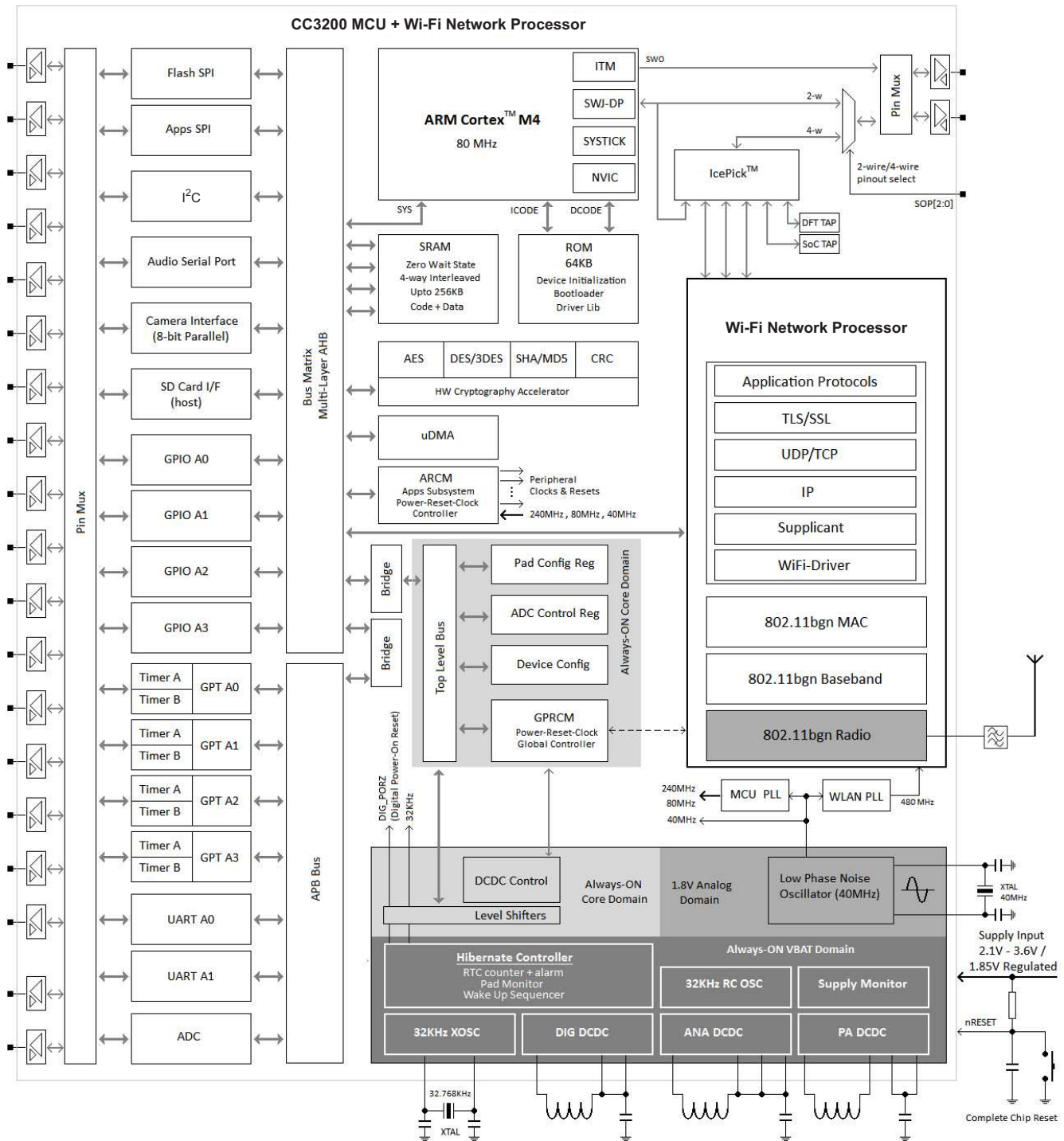


Figure 1-3. CC3200 Functional Block Diagram

Table of Contents

| | | | |
|---|-----------|---|-----------|
| 1 Device Overview | 1 | 4.11 Timing and Switching Characteristics | 34 |
| 1.1 Features | 1 | 5 Detailed Description | 48 |
| 1.2 Applications | 2 | 5.1 Overview | 48 |
| 1.3 Description | 2 | 5.2 Functional Block Diagram | 48 |
| 1.4 Functional Block Diagram | 3 | 5.3 ARM Cortex-M4 Processor Core Subsystem | 48 |
| 2 Revision History | 5 | 5.4 CC3200 Device Encryption | 49 |
| 3 Terminal Configuration and Functions | 6 | 5.5 Wi-Fi Network Processor Subsystem | 50 |
| 3.1 Pin Attributes and Pin Multiplexing | 6 | 5.6 Power-Management Subsystem | 51 |
| 3.2 Drive Strength and Reset States for Analog-Digital Multiplexed Pins | 26 | 5.7 Low-Power Operating Mode | 51 |
| 3.3 Pad State After Application of Power To Chip But Prior To Reset Release | 26 | 5.8 Memory | 53 |
| 4 Specifications | 27 | 5.9 Boot Modes | 55 |
| 4.1 Absolute Maximum Ratings | 27 | 6 Applications and Implementation | 58 |
| 4.2 Handling Ratings | 27 | 6.1 Application Information | 58 |
| 4.3 Power-On Hours | 27 | 7 Device and Documentation Support | 62 |
| 4.4 Recommended Operating Conditions | 27 | 7.1 Device Support | 62 |
| 4.5 Brown-Out and Black-Out | 28 | 7.2 Documentation Support | 63 |
| 4.6 Electrical Characteristics (3.3 V, 25°C) | 29 | 7.3 Community Resources | 63 |
| 4.7 WLAN Receiver Characteristics | 31 | 7.4 Trademarks | 63 |
| 4.8 WLAN Transmitter Characteristics | 31 | 7.5 Electrostatic Discharge Caution | 63 |
| 4.9 Current Consumption | 31 | 7.6 Glossary | 63 |
| 4.10 Thermal Characteristics for RGC Package | 34 | 8 Mechanical Packaging and Orderable Information | 64 |

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (August 2014) to Revision F | Page |
|---|------|
| • Added Wi-Fi CERTIFIED | 1 |
| • Added application throughput in Section 1.1, Features | 1 |
| • Changed LPDS drain value from 120 μ A in Section 1.1, Features | 1 |
| • Changed idle connected from 695 μ A in Section 1.1, Features | 1 |
| • Added note defining X in part number in Device Information table | 2 |
| • Changed part number in Device Information table from CC3200 | 2 |
| • Changed SDCARD signal names for pins 6, 7, 8, and 64 in Table 3-1 | 8 |
| • Changed use of pin 61 from no in Table 3-1 | 19 |
| • Added note in Section 4.4, Recommended Operating Conditions , on avoiding the PA auto-protect feature | 27 |
| • Added Table 4-1 | 28 |
| • Added note in Section 4.6, Electrical Characteristics (3.3 V, 25°C) , on proper device reset | 29 |
| • Changed Figure 4-8 to reflect T2, T3, and T4 measurements | 36 |
| • Changed Table 4-4 to reflect T2, T3, and T4 timing items | 36 |
| • Changed frequency accuracy from ± 20 ppm in Table 4-5 | 38 |
| • Added 4.11.3.6, WLAN Filter Requirements | 39 |
| • Deleted I3 (t_{LP}) and I4 (t_{HP}) from Table 4-10 | 41 |
| • Deleted I3 (t_{LP}) and I4 (t_{HP}) from Table 4-11 | 41 |
| • Changed TCP of throughput in Table 5-1 item 17 from 12 Mbps | 50 |
| • Changed part number of item 17 from CC3200R1-M2RTDR in Table 6-1 | 59 |
| • Added note following Table 6-1 | 59 |
| • Changed part number of item 16 from CC3200R1-M2RTDR in Table 6-2 | 61 |
| • Added note following Table 6-2 | 61 |

3 Terminal Configuration and Functions

Figure 3-1 shows pin assignments for the 64-pin QFN package.

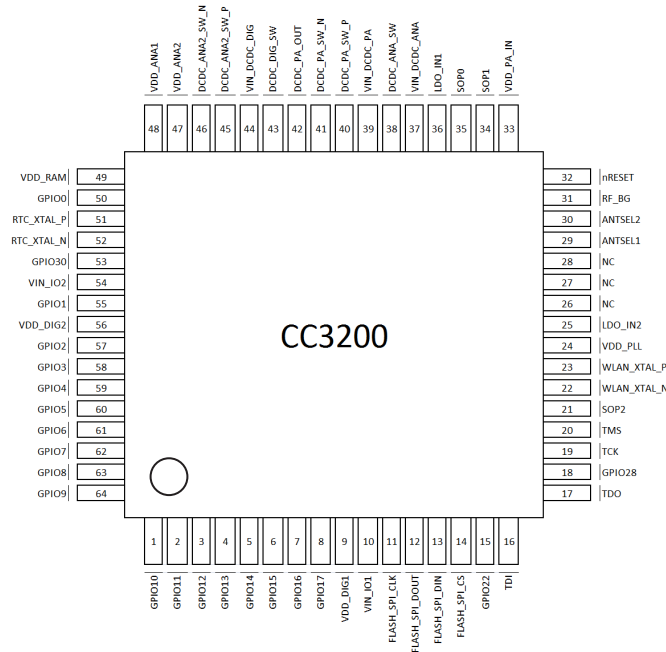


Figure 3-1. QFN 64-Pin Assignments (Top View)

3.1 Pin Attributes and Pin Multiplexing

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

NOTE

TI highly recommends using the CC3200 pin multiplexing utility to obtain the desired pinout.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used.

Table 3-1 describes the general pin attributes and presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers.

The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. Drive strength is configurable individually for each pin.
- All I/Os support 10-µA pullups and pulldowns.
- These pulls are not active and all of the I/Os remain floating while the device is in Hibernate state.
- The VIO and V_{BAT} supply must be tied together at all times.
- All digital I/Os are nonfail-safe.

NOTE

If an external device drives a positive voltage to the signal pads and the CC3200 device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3200 device can occur. To prevent current draw, TI recommends any one of the following:

- All devices interfaced to the CC3200 device must be powered from the same power rail as the chip.
 - Use level-shifters between the device and any external devices fed from other independent rails.
 - The nRESET pin of the CC3200 device must be held low until the VBAT supply to the device is driven and stable.
-

Table 3-1. Pin Multiplexing

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|-----|-------------------------|------------------------|-----------------|-------------------------------------|--------------------------------|---------------|-------------------------------|---------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 1 | GPIO10 | I/O | No | No | No | GPIO_PAD_CONFIG_10 (0x4402 E0C8) | 0 | GPIO10 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 1 | I2C_SCL | I2C Clock | O (Open Drain) | Hi-Z | | |
| | | | | | | | 3 | GT_PWM06 | Pulse-Width Modulated O/P | O | Hi-Z | | |
| | | | | | | | 7 | UART1_TX | UART TX Data | O | 1 | | |
| | | | | | | | 6 | SDCARD_CLK | SD Card Clock | O | 0 | | |
| | | | | | | | 12 | GT_CCP01 | Timer Capture Port | I | Hi-Z | | |
| 2 | GPIO11 | I/O | Yes | No | No | GPIO_PAD_CONFIG_11 (0x4402 E0CC) | 0 | GPIO11 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 1 | I2C_SDA | I2C Data | I/O (Open Drain) | Hi-Z | | |
| | | | | | | | 3 | GT_PWM07 | Pulse-Width Modulated O/P | O | Hi-Z | | |
| | | | | | | | 4 | pXCLK (XVCLK) | Free Clock To Parallel Camera | O | 0 | | |
| | | | | | | | 6 | SDCARD_CMD | SD Card Command Line | I/O | Hi-Z | | |
| | | | | | | | 7 | UART1_RX | UART RX Data | I | Hi-Z | | |
| | | | | | | | 12 | GT_CCP02 | Timer Capture Port | I | Hi-Z | | |
| | | | | | | | 13 | McAFSX | I2S Audio Port Frame Sync | O | Hi-Z | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|-----|-------------------------|------------------------|-----------------|-------------------------------------|--------------------------------|-----------------|---------------------------------|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 3 | GPIO12 | I/O | No | No | No | GPIO_PAD_CONFIG_12 (0x4402 E0D0) | 0 | GPIO12 | General Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 3 | McACLK | I2S Audio Port Clock O | O | Hi-Z | | |
| | | | | | | | 4 | pVS (VSYNC) | Parallel Camera Vertical Sync | I | Hi-Z | | |
| | | | | | | | 5 | I2C_SCL | I2C Clock | I/O (Open Drain) | Hi-Z | | |
| | | | | | | | 7 | UART0_TX | UART0 TX Data | O | 1 | | |
| | | | | | | | 12 | GT_CCP03 | Timer Capture Port | I | Hi-Z | | |
| 4 | GPIO13 | I/O | Yes | No | No | GPIO_PAD_CONFIG_13 (0x4402 E0D4) | 0 | GPIO13 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 5 | I2C_SDA | I2C Data | I/O (Open Drain) | | | |
| | | | | | | | 4 | pHS (HSYNC) | Parallel Camera Horizontal Sync | I | | | |
| | | | | | | | 7 | UART0_RX | UART0 RX Data | I | | | |
| | | | | | | | 12 | GT_CCP04 | Timer Capture Port | I | | | |
| 5 | GPIO14 | I/O | | No | No | GPIO_PAD_CONFIG_14 (0x4402 E0D8) | 0 | GPIO14 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 5 | I2C_SCL | I2C Clock | I/O (Open Drain) | | | |
| | | | | | | | 7 | GSPI_CLK | General SPI Clock | I/O | | | |
| | | | | | | | 4 | pDATA8 (CAM_D4) | Parallel Camera Data Bit 4 | I | | | |
| | | | | | | | 12 | GT_CCP05 | Timer Capture Port | I | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|------------|---------------|-------------------------|------------------------|-----------------|-------------------------------------|--------------------------------|------------------|----------------------------|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 6 | GPIO15 | I/O | | No | No | GPIO_PAD_CONFIG_15 (0x4402 E0DC) | 0 | GPIO15 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 5 | I2C_SDA | I2C Data | I/O (Open Drain) | | | |
| | | | | | | | 7 | GSPI_MISO | General SPI MISO | I/O | | | |
| | | | | | | | 4 | pDATA9 (CAM_D5) | Parallel Camera Data Bit 5 | I | | | |
| | | | | | | | 13 | GT_CCP06 | Timer Capture Port | I | | | |
| | | | | | | | 8 | SDCARD_DATA0 | SD Card Data | I/O | | | |
| 7 | GPIO16 | I/O | | No | No | GPIO_PAD_CONFIG_16 (0x4402 E0E0) | 0 | GPIO16 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | | | | | Hi-Z | | |
| | | | | | | | | | | | Hi-Z | | |
| | | | | | | | 7 | GSPI_MOSI | General SPI MOSI | I/O | Hi-Z | | |
| | | | | | | | 4 | pDATA10 (CAM_D6) | Parallel Camera Data Bit 6 | I | Hi-Z | | |
| | | | | | | | 5 | UART1_TX | UART1 TX Data | O | 1 | | |
| | | | | | | | 13 | GT_CCP07 | Timer Capture Port | I | Hi-Z | | |
| 8 | SDCARD_CLK | SD Card Clock | O | O | | | | | | | | | |
| 8 | GPIO17 | I/O | Wake-Up Source | No | No | GPIO_PAD_CONFIG_17 (0x4402 E0E4) | 0 | GPIO17 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 5 | UART1_RX | UART1 RX Data | I | | | |
| | | | | | | | 7 | GSPI_CS | General SPI Chip Select | I/O | | | |
| | | | | | | | 4 | pDATA11 (CAM_D7) | Parallel Camera Data Bit 7 | I | | | |
| | | | | | | | 8 | SDCARD_CMD | SD Card Command Line | I/O | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|----------------|------------|-------------------------|------------------------|---------------------|-------------------------------------|--------------------------------|----------------|---|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 9 | VDD_DIG1 | Int pwr | N/A | N/A | N/A | N/A | N/A | VDD_DIG1 | Internal Digital Core Voltage | | | | |
| 10 | VIN_IO1 | Sup. input | N/A | N/A | N/A | N/A | N/A | VIN_IO1 | Chip Supply Voltage (VBAT) | | | | |
| 11 | FLASH_SPI_CLK | O | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_CLK | Clock To SPI Serial Flash (Fixed Default) | O | Hi-Z ⁽³⁾ | Hi-Z | Hi-Z |
| 12 | FLASH_SPI_DOUT | O | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_DOUT | Data To SPI Serial Flash (Fixed Default) | O | Hi-Z ⁽³⁾ | Hi-Z | Hi-Z |
| 13 | FLASH_SPI_DIN | I | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_DIN | Data From SPI Serial Flash (Fixed Default) | I | | | |
| 14 | FLASH_SPI_CS | O | N/A | N/A | N/A | N/A | N/A | FLASH_SPI_CS | Chip Select To SPI Serial Flash (Fixed Default) | O | 1 | Hi-Z | Hi-Z |
| 15 | GPIO22 | I/O | No | No | No | GPIO_PAD_CONFIG_22 (0x4402 E0F8) | 0 | GPIO22 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 7 | McAFSX | I2S Audio Port Frame Sync | O | Hi-Z | | |
| | | | | | | | 5 | GT_CCP04 | Timer Capture Port | I | | | |
| 16 | TDI | I/O | No | No | MUXed with JTAG TDI | GPIO_PAD_CONFIG_23 (0x4402 E0FC) | 1 | TDI | JTAG TDI. Reset Default Pinout. | I | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO23 | General-Purpose I/O | I/O | | | |
| | | | | | | | 2 | UART1_TX | UART1 TX Data | O | 1 | | |
| | | | | | | | 9 | I2C_SCL | I2C Clock | I/O (Open Drain) | Hi-Z | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|-----|-------------------------|------------------------|--------------------------|-------------------------------------|--------------------------------|-------------|-----------------------------------|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 17 | TDO | I/O | Wake-Up Source | No | MUXed with JTAG TDO | GPIO_PAD_CONFIG_24 (0x4402 E100) | 1 | TDO | JTAG TDO. Reset Default Pinout. | O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO24 | General-Purpose I/O | I/O | | | |
| | | | | | | | 5 | PWM0 | Pulse Width Modulated O/P | O | | | |
| | | | | | | | 2 | UART1_RX | UART1 RX Data | I | | | |
| | | | | | | | 9 | I2C_SDA | I2C Data | I/O (Open Drain) | | | |
| | | | | | | | 4 | GT_CCP06 | Timer Capture Port | I | | | |
| | | | | | | | 6 | McAFSX | I2S Audio Port Frame Sync | O | | | |
| 18 | GPIO28 | I/O | | No | | GPIO_PAD_CONFIG_28 (0x4402 E110) | 0 | GPIO28 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| 19 | TCK | I/O | No | No | MUXed with JTAG/SWD-TCK | | 1 | TCK | JTAG/SWD TCK Reset Default Pinout | I | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 8 | GT_PWM03 | Pulse Width Modulated O/P | O | | | |
| 20 | TMS | I/O | No | No | MUXed with JTAG/SWD-TMSC | GPIO_PAD_CONFIG_29 (0x4402 E114) | 1 | TMS | JTAG/SWD TMS Reset Default Pinout | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO29 | General-Purpose I/O | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-------------|-----------|-------------------------|---|-----------------|-------------------------------------|--------------------------------|------------------------|---|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 21 ⁽⁴⁾⁽⁵⁾ | SOP2 | O Only | No | No | No | GPIO_PAD_CONFIG_25 (0x4402 E104) | 0 | GPIO25 | General-Purpose I/O | O | Hi-Z | Driven Low | Hi-Z |
| | | | | | | | 9 | GT_PWM02 | Pulse Width Modulated O/P | O | Hi-Z | | |
| | | | | | | | 2 | McAFSX | I2S Audio Port Frame Sync | O | Hi-Z | | |
| | | | | | | | See ⁽⁶⁾ | TCXO_EN | Enable to Optional External 40-MHz TCXO | O | O | | |
| | | | | | | | See ⁽⁷⁾ | SOP2 | Sense-On-Power 2 | I | | | |
| 22 | WLAN_XTAL_N | WLAN Ana. | N/A | N/A | N/A | N/A | See ⁽⁶⁾ | WLAN_XTAL_N | 40-MHz XTAL Pulldown if ext TCXO is used. | | | | |
| 23 | WLAN_XTAL_P | WLAN Ana. | N/A | N/A | N/A | N/A | | WLAN_XTAL_P | 40-MHz XTAL or TCXO clock input | | | | |
| 24 | VDD_PLL | Int. Pwr | N/A | N/A | N/A | N/A | | VDD_PLL | Internal analog voltage | | | | |
| 25 | LDO_IN2 | Int. Pwr | N/A | N/A | N/A | N/A | | LDO_IN2 | Analog RF supply from ANA DC-DC output | | | | |
| 26 | NC | WLAN Ana. | N/A | N/A | N/A | N/A | | NC | Reserved | | | | |
| 27 | NC | WLAN Ana. | N/A | N/A | N/A | N/A | | NC | Reserved | | | | |
| 28 | NC | WLAN Ana. | N/A | N/A | N/A | N/A | | NC | Reserved | | | | |
| 29 ⁽⁸⁾ | ANTSEL1 | O Only | No | User config not required ⁽⁹⁾ | No | GPIO_PAD_CONFIG_26 (0x4402 E108) | 0 | ANTSEL1 ⁽³⁾ | Antenna Selection Control | O | Hi-Z | Hi-Z | Hi-Z |
| 30 ⁽⁸⁾ | ANTSEL2 | O Only | No | User config not required ⁽⁹⁾ | No | GPIO_PAD_CONFIG_27 (0x4402 E10C) | 0 | ANTSEL2 ⁽³⁾ | Antenna Selection Control | O | Hi-Z | Hi-Z | Hi-Z |
| 31 | RF_BG | WLAN Ana. | N/A | N/A | N/A | N/A | | RF_BG | RF BG band | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|--------------|----------------|-------------------------|------------------------|-----------------|-------------------------|--------------------------------|--------------|--|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 32 | nRESET | Glob. Rst | N/A | N/A | N/A | N/A | | nRESET | Master chip reset. Active low. | | | | |
| 33 | VDD_PA_IN | Int. Pwr | N/A | N/A | N/A | N/A | | VDD_PA_IN | PA supply voltage from PA DC-DC output. | | | | |
| 34 ⁽⁵⁾ | SOP1 | Config Sense | N/A | N/A | N/A | N/A | | SOP1 | Sense On Power 1 | | | | |
| 35 ⁽⁵⁾ | SOP0 | Config Sense | N/A | N/A | N/A | N/A | | SOP0 | Sense On Power 0 | | | | |
| 36 | LDO_IN1 | Internal Power | N/A | N/A | N/A | N/A | | LDO_IN1 | Analog RF supply from ana DC-DC output | | | | |
| 37 | VIN_DCDC_ANA | Supply Input | N/A | N/A | N/A | N/A | | VIN_DCDC_ANA | Analog DC-DC input (connected to chip input supply [VBAT]) | | | | |
| 38 | DCDC_ANA_SW | Internal Power | N/A | N/A | N/A | N/A | | DCDC_ANA_SW | Analog DC-DC switching node. | | | | |
| 39 | VIN_DCDC_PA | Supply Input | N/A | N/A | N/A | N/A | | VIN_DCDC_PA | PA DC-DC input (connected to chip input supply [VBAT]) | | | | |
| 40 | DCDC_PA_SW_P | Internal Power | N/A | N/A | N/A | N/A | | DCDC_PA_SW_P | PA DCDC switching node | | | | |
| 41 | DCDC_PA_SW_N | Internal Power | N/A | N/A | N/A | N/A | | DCDC_PA_SW_N | PA DCDC switching node | | | | |
| 42 | DCDC_PA_OUT | Internal Power | N/A | N/A | N/A | N/A | | DCDC_PA_OUT | PA buck converter output | | | | |
| 43 | DCDC_DIG_SW | Internal Power | N/A | N/A | N/A | N/A | | DCDC_DIG_SW | DIG DC-DC switching node | | | | |
| 44 | VIN_DCDC_DIG | Supply Input | N/A | N/A | N/A | N/A | | VIN_DCDC_DIG | DIG DC-DC input (connected to chip input supply [VBAT]) | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|----------------|----------------|-------------------------|---|-----------------|-------------------------------------|--------------------------------|----------------|---|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 45 ⁽¹⁰⁾ | DCDC_ANA2_SW_P | I/O | No | User config not required ⁽⁹⁾⁽¹¹⁾ | No | GPIO_PAD_CONFIG_31 (0x4402 E11C) | 0 | GPIO31 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 9 | UART0_RX | UART0 RX Data | I | | | |
| | | | | | | | 12 | McAFSX | I2S Audio Port Frame Sync | O | | | |
| | | | | | | | 2 | UART1_RX | UART1 RX Data | I | | | |
| | | | | | | | 6 | McAXR0 | I2S Audio Port Data 0 (RX/TX) | I/O | | | |
| | | | | | | | 7 | GSPI_CLK | General SPI Clock | I/O | | | |
| | | | | | | | See ⁽⁶⁾ | DCDC_ANA2_SW_P | ANA2 DCDC Converter +ve Switching Node. | | | | |
| 46 | DCDC_ANA2_SW_N | Internal Power | N/A | N/A | N/A | N/A | N/A | DCDC_ANA2_SW_N | ANA2 DCDC Converter -ve Switching Node. | | | | |
| 47 | VDD_ANA2 | Internal Power | N/A | N/A | N/A | N/A | N/A | VDD_ANA2 | ANA2 DCDC O | | | | |
| 48 | VDD_ANA1 | Internal Power | N/A | N/A | N/A | N/A | N/A | VDD_ANA1 | Analog supply fed by ANA2 DCDC output | | | | |
| 49 | VDD_RAM | Internal Power | N/A | N/A | N/A | N/A | N/A | VDD_RAM | SRAM LDO output | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|------------|-----------|-------------------------|---|-----------------|------------------------------------|--------------------------------|-------------|--|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 50 | GPIO0 | I/O | No | User config not required ⁽⁹⁾ | No | GPIO_PAD_CONFIG_0 (0x4402 E0A0) | 0 | GPIO0 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 12 | UART0_CTS | UART0 Clear To Send Input (Active Low) | I | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 6 | McAXR1 | I2S Audio Port Data 1 (RX/TX) | I/O | Hi-Z | | |
| | | | | | | | 7 | GT_CCP00 | Timer Capture Port | I | Hi-Z | | |
| | | | | | | | 9 | GSPI_CS | General SPI Chip Select | I/O | Hi-Z | | |
| | | | | | | | 10 | UART1_RTS | UART1 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 3 | UART0_RTS | UART0 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 4 | McAXR0 | I2S Audio Port Data 0 (RX/TX) | I/O | Hi-Z | | |
| 51 | RTC_XTAL_P | RTC Clock | N/A | N/A | N/A | N/A | | RTC_XTAL_P | Connect 32.768-kHz XTAL or Froce external CMOS level clock | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|------------|--------------|-------------------------|---|-----------------|-------------------------------------|--------------------------------|-------------|--|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 52 ⁽¹⁰⁾ | RTC_XTAL_N | O Only | | User config not required ⁽⁹⁾⁽¹²⁾ | No | GPIO_PAD_CONFIG_32 (0x4402 E120) | | RTC_XTAL_N | Connect 32.768-kHz XTAL or connect a 100 kΩ to V _{supply} . | | | | |
| | | | | | | | 0 | GPIO32 | General-Purpose I/O | I/O | Hi-Z | | |
| | | | | | | | 2 | McACLK | I2S Audio Port Clock O | O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 4 | McAXR0 | I2S Audio Port Data (Only O Mode Supported On Pin 52) | O | Hi-Z | | |
| | | | | | | | 6 | UART0_RTS | UART0 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 8 | GSPI_MOSI | General SPI MOSI | I/O | Hi-Z | | |
| 53 | GPIO30 | I/O | No | User config not required ⁽⁹⁾ | No | GPIO_PAD_CONFIG_30 (0x4402 E118) | 0 | GPIO30 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 9 | UART0_TX | UART0 TX Data | O | 1 | | |
| | | | | | | | 2 | McACLK | I2S Audio Port Clock O | O | Hi-Z | | |
| | | | | | | | 3 | McAFSX | I2S Audio Port Frame Sync | O | Hi-Z | | |
| | | | | | | | 4 | GT_CCP05 | Timer Capture Port | I | Hi-Z | | |
| | | | | | | | 7 | GSPI_MISO | General SPI MISO | I/O | Hi-Z | | |
| 54 | VIN_IO2 | Supply Input | N/A | N/A | N/A | N/A | | VIN_IO2 | Chip Supply Voltage (VBAT) | | | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|---|-------------------------|---------------------------------------|-----------------|------------------------------------|--------------------------------|-----------------|---|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 55 | GPIO1 | I/O | No | No | No | GPIO_PAD_CONFIG_1 (0x4402 E0A4) | 0 | GPIO1 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 3 | UART0_TX | UART0 TX Data | O | 1 | | |
| | | | | | | | 4 | pCLK (PIXCLK) | Pixel Clock From Parallel Camera Sensor | I | Hi-Z | | |
| | | | | | | | 6 | UART1_TX | UART1 TX Data | O | 1 | | |
| | | | | | | | 7 | GT_CCP01 | Timer Capture Port | I | Hi-Z | | |
| 56 | VDD_DIG2 | Internal Power | N/A | N/A | N/A | N/A | | VDD_DIG2 | Internal Digital Core Voltage | | | | |
| 57 ⁽¹³⁾ | GPIO2 | Analog Input (up to 1.8 V)/ Digital I/O | Wake-Up Source | See ⁽¹⁰⁾ (¹⁴) | No | GPIO_PAD_CONFIG_2 (0x4402 E0A8) | See ⁽⁶⁾ | ADC_CH0 | ADC Channel 0 Input (1.5V max) | I | | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO2 | General-Purpose I/O | I/O | Hi-Z | | |
| | | | | | | | 3 | UART0_RX | UART0 RX Data | I | Hi-Z | | |
| | | | | | | | 6 | UART1_RX | UART1 RXt Data | I | Hi-Z | | |
| | | | | | | | 7 | GT_CCP02 | Timer Capture Port | I | Hi-Z | | |
| 58 ⁽¹³⁾ | GPIO3 | Analog Input (up to 1.8 V)/ Digital I/O | No | See ⁽¹⁰⁾ (¹⁴) | No | GPIO_PAD_CONFIG_3 (0x4402 E0AC) | See ⁽⁶⁾ | ADC_CH1 | ADC Channel 1 Input (1.5V max) | I | | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO3 | General-Purpose I/O | I/O | Hi-Z | | |
| | | | | | | | 6 | UART1_TX | UART1 TX Data | O | 1 | | |
| | | | | | | | 4 | pDATA7 (CAM_D3) | Parallel Camera Data Bit 3 | I | Hi-Z | | |
| 59 ⁽¹³⁾ | GPIO4 | Analog Input (up to 1.8 V)/ Digital I/O | Wake-up Source | See ⁽¹⁰⁾ (¹⁴) | No | GPIO_PAD_CONFIG_4 (0x4402 E0B0) | See ⁽⁶⁾ | ADC_CH2 | ADC Channel 2 Input (1.5V max) | I | | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO4 | General-Purpose I/O | I/O | Hi-Z | | |
| | | | | | | | 6 | UART1_RX | UART1 RX Data | I | Hi-Z | | |
| | | | | | | | 4 | pDATA6 (CAM_D2) | Parallel Camera Data Bit 2 | I | Hi-Z | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|---|-------------------------|---|-----------------|------------------------------------|--------------------------------|-----------------|--|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 60 ⁽¹³⁾ | GPIO5 | Analog Input (up to 1.8 V)/ Digital I/O | No | See (10) (14) | No | GPIO_PAD_CONFIG_5 (0x4402 E0B4) | See (6) | ADC_CH3 | ADC Channel 3 Input (1.5V max) | I | | Hi-Z | Hi-Z |
| | | | | | | | 0 | GPIO5 | General-Purpose I/O | I/O | Hi-Z | | |
| | | | | | | | 4 | pDATA5 (CAM_D1) | Parallel Camera Data Bit 1 | I | Hi-Z | | |
| | | | | | | | 6 | McAXR1 | I2S Audio Port Data 1 (RX/TX) | I/O | Hi-Z | | |
| | | | | | | | 7 | GT_CCP05 | Timer Capture Port | I | Hi-Z | | |
| 61 | GPIO6 | I/O | No | No | No | GPIO_PAD_CONFIG_6 (0x4402 E0B8) | 0 | GPIO6 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 5 | UART0_RTS | UART0 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 4 | pDATA4 (CAM_D0) | Parallel Camera Data Bit 0 | I | Hi-Z | | |
| | | | | | | | 3 | UART1_CTS | UART1 Clear To Send Input (Active Low) | I | Hi-Z | | |
| | | | | | | | 6 | UART0_CTS | UART0 Clear To Send Input (Active Low) | I | Hi-Z | | |
| | | | | | | | 7 | GT_CCP06 | Timer Capture Port | I | Hi-Z | | |
| 62 | GPIO7 | I/O | No | No | No | GPIO_PAD_CONFIG_7 (0x4402 E0BC) | 0 | GPIO7 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 13 | McACLKX | I2S Audio Port Clock O | O | Hi-Z | | |
| | | | | | | | 3 | UART1_RTS | UART1 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 10 | UART0_RTS | UART0 Request To Send O (Active Low) | O | 1 | | |
| | | | | | | | 11 | UART0_TX | UART0 TX Data | O | 1 | | |

Table 3-1. Pin Multiplexing (continued)

| General Pin Attributes | | | | | | Function | | | | | Pad States | | |
|------------------------|-----------|-----|-------------------------|------------------------|-----------------|------------------------------------|--------------------------------|--------------|---|------------------|---------------------|--------------------|------------|
| Pkg Pin | Pin Alias | Use | Select as Wakeup Source | Config Addl Analog Mux | Muxed with JTAG | Dig. Pin Mux Config Reg | Dig. Pin Mux Config Mode Value | Signal Name | Signal Description | Signal Direction | LPDS ⁽¹⁾ | Hib ⁽²⁾ | nRESET = 0 |
| 63 | GPIO8 | I/O | No | No | No | GPIO_PAD_CONFIG_8 (0x4402 E0C0) | 0 | GPIO8 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 6 | SDCARD_IRQ | Interrupt from SD Card (Future support) | I | | | |
| | | | | | | | 7 | McAFSX | I2S Audio Port Frame Sync | O | | | |
| | | | | | | | 12 | GT_CCP06 | Timer Capture Port | I | | | |
| 64 | GPIO9 | I/O | No | No | No | GPIO_PAD_CONFIG_9 (0x4402 E0C4) | 0 | GPIO9 | General-Purpose I/O | I/O | Hi-Z | Hi-Z | Hi-Z |
| | | | | | | | 3 | GT_PWM05 | Pulse Width Modulated O/P | O | | | |
| | | | | | | | 6 | SDCARD_DATA0 | SD Cad Data | I/O | | | |
| | | | | | | | 7 | McAXR0 | I2S Audio Port Data (Rx/Tx) | I/O | | | |
| | | | | | | | 12 | GT_CCP00 | Timer Capture Port | I | | | |
| 65 | GND_TAB | | | | | | | | Thermal pad and electrical ground | | | | |

- (1) LPDS mode: The state of unused GPIOs in LPDS is input with 500 kΩ pull-down. For all used GPIOs, the user can enable internal pulls, which would hold them in a valid state.
- (2) Hibernate mode: The CC3200 device leaves the digital pins in a Hi-Z state without any internal pulls when the device enters hibernate state. This can cause glitches on output lines unless held at valid levels by external resistors.
- (3) To minimize leakage in some serial flash vendors during LPDS, TI recommends the user application always enable internal weak pull-downs on FLASH_SPI_DATA and FLASH_SPI_CLK pins.
- (4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a high impedance state but pulled down for SOP mode to disable TCXO. Because of SOP functionality, the pin must be used as output only.
- (5) Higher leakage current from the onboard serial flash can occur due to floating inputs when the device enters Hibernate mode. See reference schematics for recommended pull-up and pull-down resistors.
- (6) For details on proper use, see [Section 3.2, Drive Strength and Reset States for Analog-Digital Multiplexed Pins](#).
- (7) This pin is one of three that must have a passive pullup or pulldown resistor on board to configure the chip hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
- (8) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3200 device between two antennas. These pins should not be used for other functionalities in general.

- (9) Device firmware automatically enables the digital path during ROM boot.
- (10) Pin 45 is used by an internal DC-DC (ANA2_DCDC) and pin 52 is used by the RTC XTAL oscillator. These modules use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 45 and pin 52 as digital pads (see Figure 3-2). Because the CC3200R device does not require ANA2_DCDC, the pin can always be used for digital functions. However, pin 47 must be shorted to the supply input. Typically, pin 52 is used for RTC XTAL in most applications. However, in some applications a 32.768-kHz square-wave clock might always be available onboard. In such cases, the XTAL can be removed to free up pin 52 for digital functions. The external clock must then be applied at pin 51. For the chip to automatically detect this configuration, a 100K pull-up resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
- (11) VDD_FLASH must be shorted to V_{supply}.
- (12) To use the digital functions, RTC_XTAL_N must be pulled high to V_{supply} using 100-KΩ resistor.
- (13) This pin is shared by the ADC inputs and digital I/O pad cells. Important: The ADC inputs are tolerant up to 1.8 V. On the other hand, the digital pads can tolerate up to 3.6 V. Hence, care must be taken to prevent accidental damage to the ADC inputs. TI recommends that the output buffer(s) of the digital I/Os corresponding to the desired ADC channel be disabled first (that is, converted to high-impedance state), and thereafter the respective pass switches (S7, S8, S9, S10) should be enabled (see Section 3.2, Drive Strength and Reset States for Analog-Digital Multiplexed Pins).
- (14) Requires user configuration to enable the ADC channel analog switch. (The switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

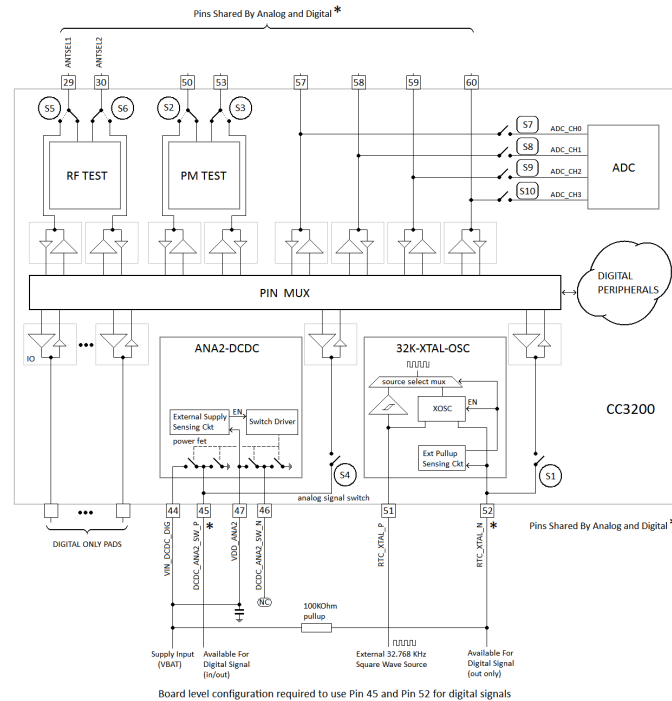


Figure 3-2. Board Configuration to Use Pins 45 and 52 as Digital Signals

3.1.1 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. For a list of NC pins, see [Table 3-2](#).

Table 3-2. Connections for Unused Pins

| FUNCTION | SIGNAL NAME | PIN NUMBER |
|-------------|-------------|------------|
| WLAN Analog | NC | 26 |
| WLAN Analog | NC | 27 |
| WLAN Analog | NC | 28 |

3.1.2 Recommended Pin Multiplexing Configurations

Table 3-3 lists the recommended pin multiplexing configurations.

Table 3-3. Recommended Pin Multiplexing Configurations

| CC3200 Recommended Pinout Grouping Use – Examples ⁽¹⁾ | | | | | | | | | | | |
|--|---|--|--|---|--|---|--|--|--|---|---------------------|
| | Home Security High-end Toys | Wifi Audio ++ Industrial | Sensor-Tag | Home Security Toys | Wifi Audio ++ Industrial | WiFi Remote w/ 7x7 keypad and audio | Sensor Door-Lock Fire-Alarm Toys w/o Cam | Industrial Home Appliances | Industrial Home Appliances Smart-Plug | Industrial Home Appliances" | GPIOs |
| | External 32 kHz ⁽²⁾ | External 32 kHz ⁽²⁾ | | | | | | | | External TCXO 40 MHz (-40 to +85°C) | |
| | Cam + I2S (Tx or Rx) + I2C + SPI + SWD + UART-Tx + (App Logger) 2 GPIO + 1PWM + *4 overlaid wakeup from Hib | I2S (Tx & Rx) + 1 Ch ADC + 1x 4wire UART + 1x 2wire UART + 1bit SD Card + SPI + I2C + SWD + 3 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib | I2S (Tx & Rx) + 2 Ch ADC + 2wire UART + SPI + I2C + SWD + 2 PWM + 6 GPIO + 3 GPIO with Wake-From-Hib | Cam + I2S (Tx or Rx) + I2C + SWD + UART-Tx + (App Logger) 4 GPIO + 1PWM + *4 overlaid wakeup from HIB | I2S (Tx & Rx) + 1 Ch ADC + 2x 2wire UART + 1bit SD Card + SPI + I2C + SWD + 4 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib | I2S (Tx & Rx) + 1 Ch ADC + UART (Tx Only) I2C + SWD + 15 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib | I2S (Tx or Rx) + 2 Ch ADC + 2 wire UART + SPI + I2C + 3 PWM + 3 GPIO with Wake-From-Hib + 5 GPIO SWD + | 4 Ch ADC + 1x 4wire UART + 1x 2wire UART + SPI + I2C + SWD + 1 PWM + 6 GPIO + 1 GPIO with Wake-From-Hib Enable for Ext 40 MHz TCXO | 3 Ch ADC + 2wire UART + SPI + I2C + SWD + 3 PWM + 9 GPIO + 2 GPIO with Wake-From-Hib | 2 Ch ADC + 2wire UART + I2C + SWD + 3 PWM + 11 GPIO + 5 GPIO with Wake-From-Hib | |
| Pin Number | Pinout #11 | Pinout #10 | Pinout #9 | Pinout #8 | Pinout #7 | Pinout #6 | Pinout #5 | Pinout #4 | Pinout #3 | Pinout #2 | Pinout #1 |
| 52 | GSPI-MOSI | McASP-D0 (Tx) | | | | | | | | | GPIO_32 output only |
| 53 | GSPI-MISO | MCASP-ACLKX | MCASP-ACLKX | GPIO_30 | GPIO_30 | GPIO_30 | GPIO_30 | UART0-TX | GPIO_30 | UART0-TX | GPIO_30 |
| 45 | GSPI-CLK | McASP-AFSX | McASP-D0 | GPIO_31 | McASP-AFSX | McASP-AFSX | McASP-AFSX | UART0-RX | GPIO_31 | UART0-RX | GPIO_31 |
| 50 | GSPI-CS | McASP-D1 (Rx) | McASP-D1 | McASP-D1 | McASP-D1 | McASP-D1 | McASP-D1 | UART0-CTS | GPIO_0 | GPIO_0 | GPIO_0 |
| 55 | pCLK (PIXCLK) | UART0-TX | UART0-TX | PIXCLK | UART0-TX | UART0-TX | UART0-TX | GPIO-1 | UART0-TX | GPIO_1 | GPIO_1 |
| 57 | (wake) GPIO2 | UART0-RX | UART0-RX | (wake) GPIO2 | UART0-RX | GPIO_2 | UART0-RX | ADC-0 | UART0-RX | (wake) GPIO_2 | (wake) GPIO_2 |
| 58 | pDATA7 (D3) | UART1-TX | ADC-CH1 | pDATA7 (D3) | UART1-TX | GPIO_3 | ADC-1 | ADC-1 | ADC-1 | ADC-1 | GPIO_3 |

(1) Pins marked "wake" can be configured to wake up the chip from HIBERNATE or LPDS state. In the current silicon revision, any wake pin can trigger wake up from HIBERNATE. The wakeup monitor in the hibernate control module logically ORs these pins applying a selection mask. However, wakeup from LPDS state can be triggered only by one of the wakeup pins that can be configured before entering LPDS. The core digital wakeup monitor use a mux to select one of these pins to monitor.

(2) The device supports the feeding of an external 32.768-kHz clock. This configuration frees one pin (32K_XTAL_N) to use in output-only mode with a 100k pullup.

Table 3-3. Recommended Pin Multiplexing Configurations (continued)

| CC3200 Recommended Pinout Grouping Use – Examples ⁽¹⁾ | | | | | | | | | | | |
|--|----------------------------|-------------------|-------------------|----------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 59 | pDATA6 (D2) | UART1-RX | (wake) GPIO_4 | pDATA6 (D2) | UART1-RX | GPIO_4 | (wake) GPIO_4 | ADC-2 | ADC-2 | (wake) GPIO_4 | (wake) GPIO_4 |
| 60 | pDATA5 (D1) | ADC-3 | ADC-3 | pDATA5 (D1) | ADC-3 | ADC-3 | ADC-3 | ADC-3 | ADC-3 | ADC-3 | GPIO_5 |
| 61 | pDATA4 (D0) | UART1-CTS | GPIO_6 | pDATA4 (D0) | GPIO_6 | GPIO_6 | GPIO_6 | UART0-RTS | GPIO_6 | GPIO_6 | GPIO_6 |
| 62 | McASP-ACLKX | UART1-RTS | GPIO_7 | McASP-ACLKX | McASP-ACLKX | McASP-ACLKX | McASP-ACLKX | GPIO_7 | GPIO_7 | GPIO_7 | GPIO_7 |
| 63 | McASP-AFSX | SDCARD-IRQ | McASP-AFSX | McASP-AFSX | SDCARD-IRQ | GPIO_8 | GPIO_8 | GPIO_8 | GPIO_8 | GPIO_8 | GPIO_8 |
| 64 | McASP-D0 | SDCARD-DATA | GT_PWM5 | McASP-D0 | SDCARD-DATA | GPIO_9 | GT_PWM5 | GT_PWM5 | GT_PWM5 | GT_PWM5 | GPIO_9 |
| 1 | UART1-TX | SDCARD-CLK | GPIO_10 | UART1-TX | SDCARD-CLK | GPIO_10 | GT_PWM6 | UART1-TX | GT_PWM6 | GPIO_10 | GPIO_10 |
| 2 | (wake) pXCLK (XVCLK) | SDCARD-CMD | (wake) GPIO_11 | (wake) pXCLK (XVCLK) | SDCARD-CMD | GPIO_11 | (wake) GPIO_11 | UART1-RX | (wake) GPIO_11 | (wake) GPIO_11 | (wake) GPIO_11 |
| 3 | pVS (VSYNC) | I2C-SCL | I2C-SCL | pVS (VSYNC) | I2C-SCL | GPIO_12 | I2C-SCL | I2C-SCL | I2C-SCL | GPIO_12 | GPIO_12 |
| 4 | (wake) pHS (HSYNC) | I2C-SDA | I2C-SDA | (wake) pHS (HSYNC) | I2C-SDA | GPIO_13 | I2C-SDA | I2C-SDA | I2C-SDA | (wake) GPIO_13 | (wake) GPIO_13 |
| 5 | pDATA8 (D4) | GSPI-CLK | GSPI-CLK | pDATA8 (D4) | GSPI-CLK | I2C-SCL | GSPI-CLK | GSPI-CLK | GSPI-CLK | I2C-SCL | GPIO_14 |
| 6 | pDATA9 (D5) | GSPI-MISO | GSPI-MISO | pDATA9 (D5) | GSPI-MISO | I2C-SDA | GSPI-MISO | GSPI-MISO | GSPI-MISO | I2C-SDA | GPIO_15 |
| 7 | pDATA10 (D6) | GSPI-MOSI | GSPI-MOSI | pDATA10 (D6) | GSPI-MOSI | GPIO_16 | GSPI-MOSI | GSPI-MOSI | GSPI-MOSI | GPIO_16 | GPIO_16 |
| 8 | (wake) pDATA11 (D7) | GSPI-CS | GSPI-CS | (wake) pDATA11 (D7) | GSPI-CS | GPIO_17 | GSPI-CS | GSPI-CS | GSPI-CS | (wake) GPIO_17 | (wake) GPIO_17 |
| 11 | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK | SPI-FLASH_CLK |
| 12 | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT | SPI-FLASH-DOUT |
| 13 | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN | SPI-FLASH-DIN |
| 14 | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS | SPI-FLASH-CS |
| 15 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 | GPIO_22 |
| 16 | I2C-SCL | GPIO_23 | GPIO_23 | I2C-SCL | GPIO_23 | GPIO_23 | GPIO_23 | GPIO_23 | GPIO_23 | GPIO_23 | GPIO_23 |
| 17 | I2C-SDA | (wake) GPIO_24 | (wake) GPIO_24 | I2C-SDA | (wake) GPIO_24 | (wake) GPIO_24 | (wake) GPIO_24 | (wake) GPIO_24 | (wake) GPIO_24 | GT-PWM0 | (wake) GPIO_24 |
| 19 | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK | SWD-TCK |
| 20 | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS | SWD-TMS |

Table 3-3. Recommended Pin Multiplexing Configurations (continued)

| CC3200 Recommended Pinout Grouping Use – Examples ⁽¹⁾ | | | | | | | | | | | |
|--|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|------------------|
| 18 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 | GPIO_28 |
| 21 | GT_PWM2 | GT_PWM2 | GT_PWM2 | GT_PWM2 | GT_PWM2 | GT_PWM2 | GT_PWM2 | TCXO_EN | GT_PWM2 | GT_PWM2 | GPIO_25 out only |

3.2 Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Table 3-4 describes the use, drive strength, and default state of these pins at first-time power up and reset (nRESET pulled low).

Table 3-4. Drive Strength and Reset States for Analog-Digital Multiplexed Pins

| Pin | Board Level Configuration and Use | Default State at First Power Up or Forced Reset | State after Configuration of Analog Switches (ACTIVE, LPDS, and HIB Power Modes) | Maximum Effective Drive Strength (mA) |
|-----|---|--|--|---------------------------------------|
| 29 | Connected to the enable pin of the RF switch (ANTSEL1). Other use not recommended. | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 30 | Connected to the enable pin of the RF switch (ANTSEL2). Other use not recommended. | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 45 | VDD_ANA2 (pin 47) must be shorted to the input supply rail. Otherwise, the pin is driven by the ANA2 DC-DC. | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 50 | Generic I/O | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 52 | The pin must have an external pullup of 100 K to the supply rail and must be used in output signals only. | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 53 | Generic I/O | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 57 | Analog signal (1.8 V absolute, 1.46 V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 58 | Analog signal (1.8 V absolute, 1.46 V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 59 | Analog signal (1.8 V absolute, 1.46 V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |
| 60 | Analog signal (1.8 V absolute, 1.46 V full scale) | ADC is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os. | 4 |

3.3 Pad State After Application of Power To Chip But Prior To Reset Release

When a stable power is applied to the CC3200 chip for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5 V, the level of the digital pads are undefined in the period starting from the release of nRESET and until DIG_DCDC powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of this external pull is 2.7 K Ω .

4 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | PINS | MIN | MAX | UNIT |
|---------------------------------------|------------|------|----------------|------|
| V_{BAT} and V_{IO} | 37, 39, 44 | -0.5 | 3.8 | V |
| $V_{IO}-V_{BAT}$ (differential) | 10, 54 | | 0.0 | V |
| Digital inputs | | -0.5 | $V_{IO} + 0.5$ | V |
| RF pins | | -0.5 | 2.1 | V |
| Analog pins (XTAL) | | -0.5 | 2.1 | V |
| Operating temperature range (T_A) | | -40 | +85 | °C |

4.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|-----------|---------------------------|--|-------|-------|---|
| T_{stg} | Storage temperature range | -55 | +125 | °C | |
| V_{ESD} | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | -2000 | +2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | -500 | +500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours

| CONDITIONS | POH |
|---|-----------------------|
| $T_{Ambient}$ up to 85°C, assuming 20% active mode and 80% sleep mode | 17,500 ⁽¹⁾ |

(1) The CC3200 device can be operated reliably for 10 years.

4.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

| PARAMETERS | PINS | CONDITIONS ⁽³⁾ ⁽⁴⁾ | MIN | TYP | MAX | UNIT |
|--|--------------------|--|------|------|-----|-----------|
| V_{BAT} , V_{IO} (shorted to V_{BAT}) | 10, 37, 39, 44, 54 | Direct battery connection | 2.1 | 3.3 | 3.6 | V |
| V_{BAT} , V_{IO} (shorted to V_{BAT}) | 10, 37, 39, 44, 54 | Preregulated 1.85 V | 1.76 | 1.85 | 1.9 | V |
| Ambient thermal slew | | | -20 | | 20 | °C/minute |

(1) Operating temperature is limited by crystal frequency variation.

(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.

(3) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300 mV.

(4) To ensure WLAN performance, ripple on the 1.85-V supply must be less than 2% (±40 mV).

4.5 Brown-Out and Black-Out

The device enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations (such as a TX packet) cause a dip in the supply voltage, potentially triggering a brown-out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (4 contacts for a 2 x AA battery) and the wiring and PCB routing resistance.

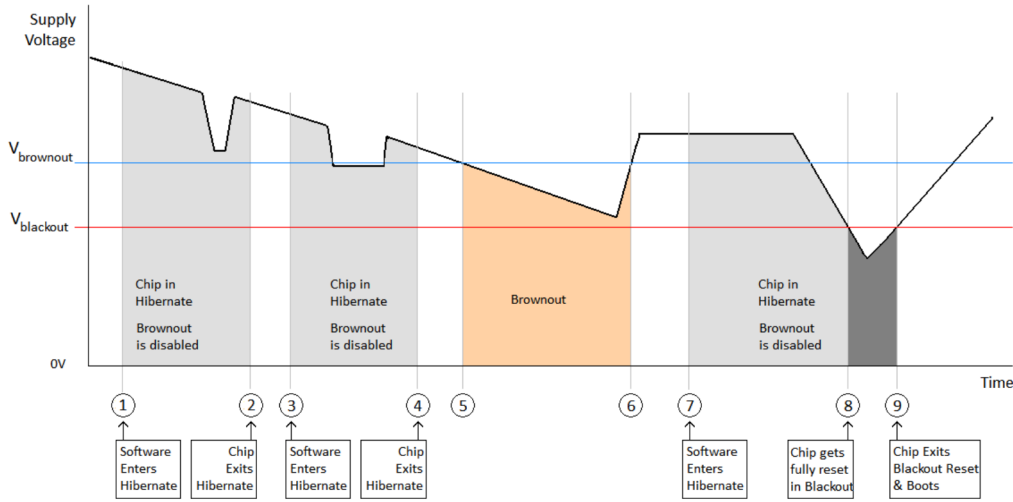


Figure 4-1. Brown-Out and Black-Out Levels (1 of 2)

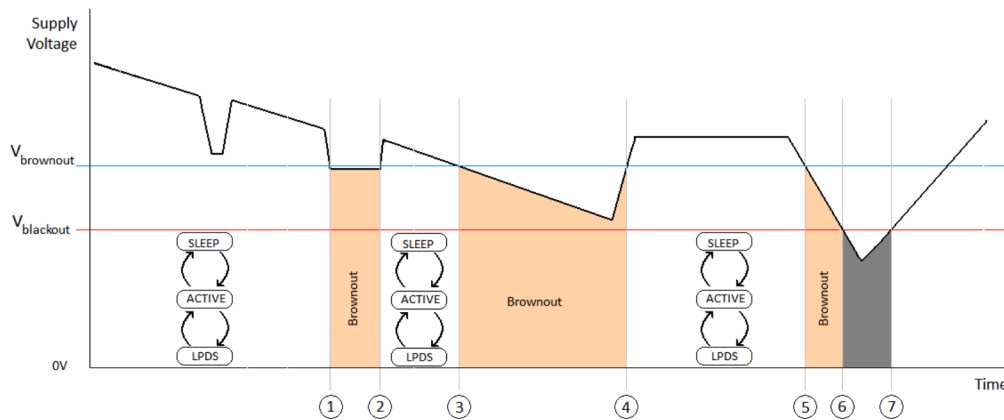


Figure 4-2. Brown-Out and Black-Out Levels (2 of 2)

In the brown-out condition, all sections of the device shut down except for the Hibernate module (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 μ A.

The black-out condition is equivalent to a hardware reset event in which all states within the device are lost. Table 4-1 lists the brown-out and black-out voltage levels.

Table 4-1. Brown-Out and Black-out Voltage Levels

| CONDITION | VOLTAGE LEVEL | UNIT |
|----------------|---------------|------|
| $V_{brownout}$ | 2.1 | V |
| $V_{blackout}$ | 1.67 | V |

4.6 Electrical Characteristics (3.3 V, 25°C)

| GPIO Pins Except 29, 30, 45, 50, 52, and 53 (25°C) ⁽¹⁾ | | | | | | |
|---|--|-----------------|------------|-----|-------------|------|
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
| C _{IN} | Pin capacitance | | | 4 | | pF |
| V _{IH} | High-level input voltage | | 0.65 × VDD | | VDD + 0.5 V | V |
| V _{IL} | Low-level input voltage | | −0.5 | | 0.35 × VDD | V |
| I _{IH} | High-level input current | | | 5 | | nA |
| I _{IL} | Low-level input current | | | 5 | | nA |
| V _{OH} | High-level output voltage (VDD = 3.0 V) | | 2.4 | | | V |
| V _{OL} | Low-level output voltage (VDD = 3.0 V) | | | | 0.4 | V |
| I _{OH} | High-level source current, V _{OH} = 2.4 | 2-mA Drive | 2 | | | mA |
| | | 4-mA Drive | 4 | | | mA |
| | | 6-mA Drive | 6 | | | mA |
| I _{OL} | Low-level sink current, V _{OL} = 0.4 | 2-mA Drive | 2 | | | mA |
| | | 4-mA Drive | 4 | | | mA |
| | | 6-mA Drive | 6 | | | mA |

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

| GPIO Pins 29, 30, 45, 50, 52, and 53 (25°C) ⁽¹⁾ | | | | | | |
|--|--|-----------------|------------|-----|------------|------|
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
| C _{IN} | Pin capacitance | | | 7 | | pF |
| V _{IH} | High-level input voltage | | 0.65 × VDD | | VDD + 0.5V | V |
| V _{IL} | Low-level input voltage | | −0.5 | | 0.35 × VDD | V |
| I _{IH} | High-level input current | | | 50 | | nA |
| I _{IL} | Low-level input current | | | 50 | | nA |
| V _{OH} | High-level output voltage (VDD= 3.0 V) | | 2.4 | | | V |
| V _{OL} | Low-level output voltage (VDD= 3.0 V) | | | | 0.4 | V |
| I _{OH} | High-level source current, V _{OH} = 2.4 | 2-mA Drive | 1.5 | | | mA |
| | | 4-mA Drive | 2.5 | | | mA |
| | | 6-mA Drive | 3.5 | | | mA |
| I _{OL} | Low-level sink current, V _{OL} = 0.4 | 2-mA Drive | 1.5 | | | mA |
| | | 4-mA Drive | 2.5 | | | mA |
| | | 6-mA Drive | 3.5 | | | mA |
| V _{IL} | nRESET ⁽²⁾ | | | 0.6 | | V |

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

(2) The nRESET pin must be held below 0.6 V to ensure the device is reset properly.

| Pin Internal Pullup and Pulldown (25°C) ⁽¹⁾ | | | | | |
|--|--|-----|-----|-----|------|
| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
| I _{OH} | Pull-Up current, V _{OH} = 2.4 (VDD = 3.0 V) | 5 | | 10 | μA |

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive-strength setting is 6 mA.

| Pin Internal Pullup and Pulldown (25°C) ⁽¹⁾ | | | | | | |
|--|--|-----------------|-----|-----|-----|---------|
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
| I_{OL} | Pull-Down current, $V_{OL} = 0.4$ ($V_{DD} = 3.0$ V) | | 5 | | | μ A |

4.7 WLAN Receiver Characteristics

$T_A = +25^\circ\text{C}$, $V_{\text{BAT}} = 2.1$ to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz)

| Parameter | Condition (Mbps) | Min | Typ | Max | Units |
|--|--------------------------|-----|-------|-----|-------|
| Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(10% PER) ⁽¹⁾ | 1 DSSS | | -95.7 | | dBm |
| | 2 DSSS | | -93.6 | | |
| | 11 CCK | | -88.0 | | |
| | 6 OFDM | | -90.0 | | |
| | 9 OFDM | | -89.0 | | |
| | 18 OFDM | | -86.0 | | |
| | 36 OFDM | | -80.5 | | |
| | 54 OFDM | | -74.0 | | |
| | MCS0 (GF) ⁽²⁾ | | -89.0 | | |
| | MCS7 (GF) ⁽²⁾ | | -71.0 | | |
| Maximum input level (10% PER) | 802.11b | | -4.0 | | |
| | 802.11g | | -10.0 | | |

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

(2) Sensitivity for mixed mode is 1-dB worse.

4.8 WLAN Transmitter Characteristics

$T_A = +25^\circ\text{C}$, $V_{\text{BAT}} = 2.1$ to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz).⁽¹⁾

| Parameter | Condition ⁽²⁾ | Min | Typ | Max | Units |
|--|--------------------------|-----|------|-----|-------|
| Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM | 1 DSSS | | 18.0 | | dBm |
| | 2 DSSS | | 18.0 | | |
| | 11 CCK | | 18.3 | | |
| | 6 OFDM | | 17.3 | | |
| | 9 OFDM | | 17.3 | | |
| | 18 OFDM | | 17.0 | | |
| | 36 OFDM | | 16.0 | | |
| | 54 OFDM | | 14.5 | | |
| | MCS7 (MM) | | 13.0 | | |
| Transmit center frequency accuracy | | -25 | | 25 | ppm |

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.

(2) In preregulated 1.85-V mode, maximum TX power is 0.25 to 0.75 dB lower for modulations higher than 18 OFDM.

4.9 Current Consumption

$T_A = +25^\circ\text{C}$, $V_{\text{BAT}} = 3.6$ V

| PARAMETER | | TEST CONDITIONS ^{(1) (2)} | | MIN | TYP | MAX | UNIT |
|------------|-----------------------------------|------------------------------------|---------|--------------------|-----|-----|------|
| MCU ACTIVE | NWP ACTIVE | TX | 1 DSSS | TX power level = 0 | 278 | | mA |
| | | | | TX power level = 4 | 194 | | |
| | | | 6 OFDM | TX power level = 0 | 254 | | |
| | | | | TX power level = 4 | 185 | | |
| | | | 54 OFDM | TX power level = 0 | 229 | | |
| | | | | TX power level = 4 | 166 | | |
| | | RX | 1 DSSS | | 59 | | |
| | | | 54 OFDM | | 59 | | |
| | NWP idle connected ⁽³⁾ | | | 15.3 | | | |

(1) TX power level = 0 implies maximum power (see [Figure 4-3](#) through [Figure 4-5](#)). TX power level = 4 implies output power backed off approximately 4 dB.

(2) The CC3200 system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.

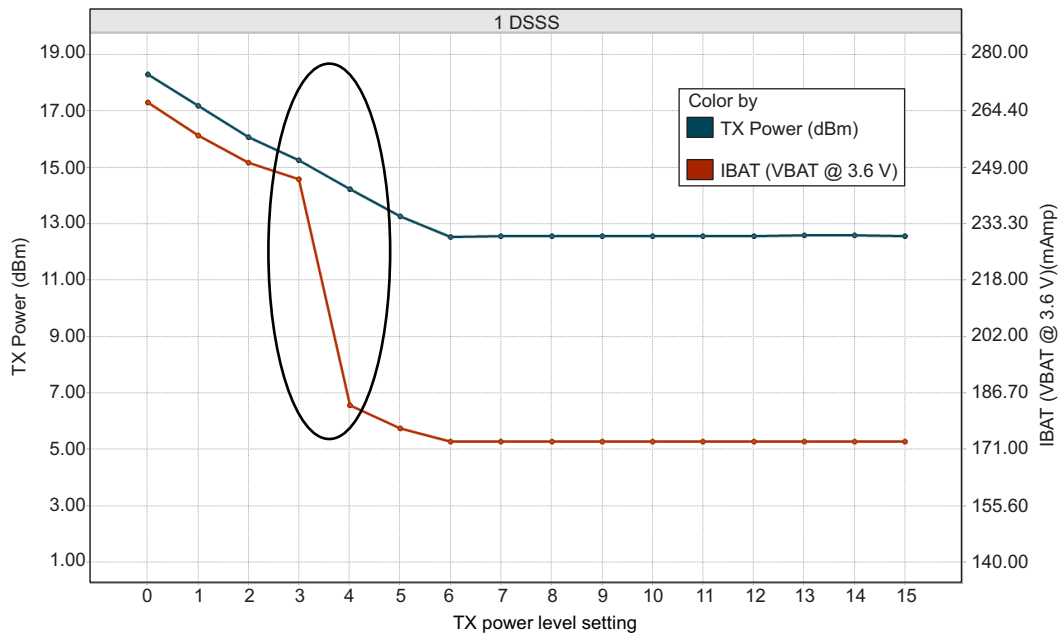
(3) DTIM = 1

Current Consumption (continued)

 $T_A = +25^\circ\text{C}$, $V_{BAT} = 3.6\text{ V}$

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ ⁽²⁾ | | MIN | TYP | MAX | UNIT |
|---|------------------------------|---|---------|--------------------|-----|---------------|------|
| MCU SLEEP | NWP ACTIVE | TX | 1 DSSS | TX power level = 0 | 275 | | mA |
| | | | | TX power level = 4 | 191 | | |
| | | | 6 OFDM | TX power level = 0 | 251 | | |
| | | | | TX power level = 4 | 182 | | |
| | | | 54 OFDM | TX power level = 0 | 226 | | |
| | | | | TX power level = 4 | 163 | | |
| | | RX | 1 DSSS | 56 | | | |
| 54 OFDM | 56 | | | | | | |
| NWP idle connected ⁽³⁾ | | | | 12.2 | | | |
| MCU LPDS | NWP active | TX | 1 DSSS | TX power level = 0 | 272 | | mA |
| | | | | TX power level = 4 | 188 | | |
| | | | 6 OFDM | TX power level = 0 | 248 | | |
| | | | | TX power level = 4 | 179 | | |
| | | | 54 OFDM | TX power level = 0 | 223 | | |
| | | | | TX power level = 4 | 160 | | |
| | | RX | 1 DSSS | 53 | | | |
| | | | 54 OFDM | 53 | | | |
| NWP LPDS ⁽⁴⁾ | | | | 0.25 | | | |
| NWP idle connected ⁽³⁾ | | | | 0.825 | | | |
| MCU hibernate ⁽⁵⁾ | NWP hibernate ⁽⁶⁾ | | | 4 | | μA | |
| Peak calibration current ⁽⁷⁾ | $V_{BAT} = 3.3\text{ V}$ | | | 450 | | mA | |
| | $V_{BAT} = 2.1\text{ V}$ | | | 670 | | | |
| | $V_{BAT} = 1.85\text{ V}$ | | | 700 | | | |

- (4) LPDS current does not include the external serial flash. The LPDS number reported is with retention of 64KB MCU SRAM. The CC3200 device can be configured to retain 0KB, 64KB, 128KB, 192KB or 256KB SRAM in LPDS. Each 64KB retained increases LPDS current by 4 μA .
- (5) For the 1.85-V mode, the Hibernate current is higher by 50 μA across all operating modes because of leakage into the PA and analog power inputs.
- (6) Serial flash current consumption in power-down mode during hibernate is not included.
- (7) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. Calibration is performed sparingly, typically when coming out of Hibernate and only if temperature has changed by more than 20°C or the time elapsed from prior calibration is greater than 24 hours.



Note: The area enclosed in the circle represents a significant reduction in current when transitioning from TX power level 3 to 4. In the case of lower range requirements (14 dbm output power), TI recommends using TX power level 4 to reduce the current.

Figure 4-3. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

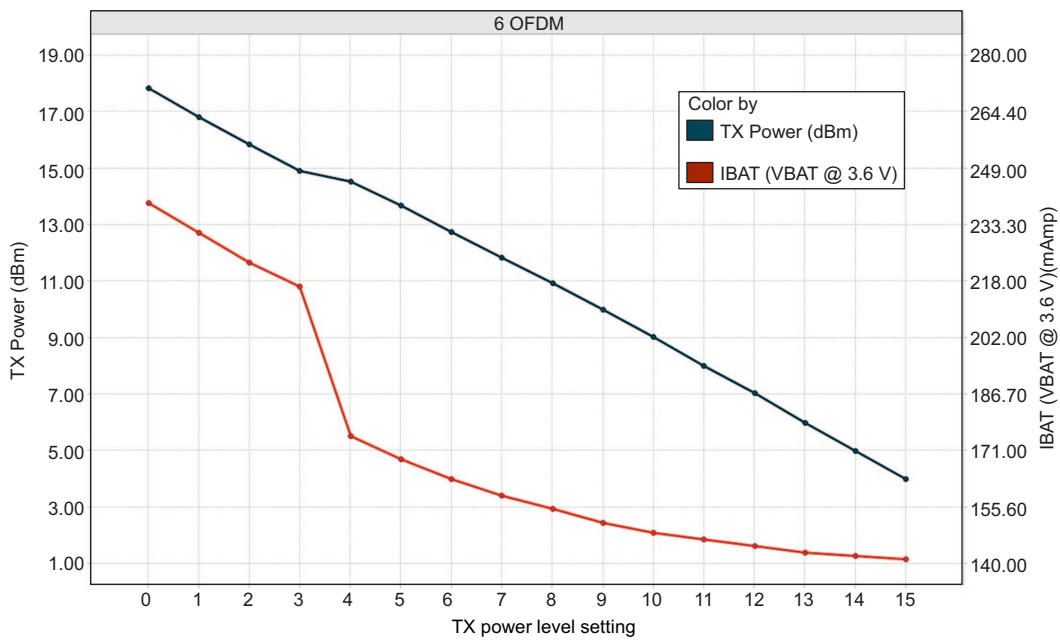


Figure 4-4. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

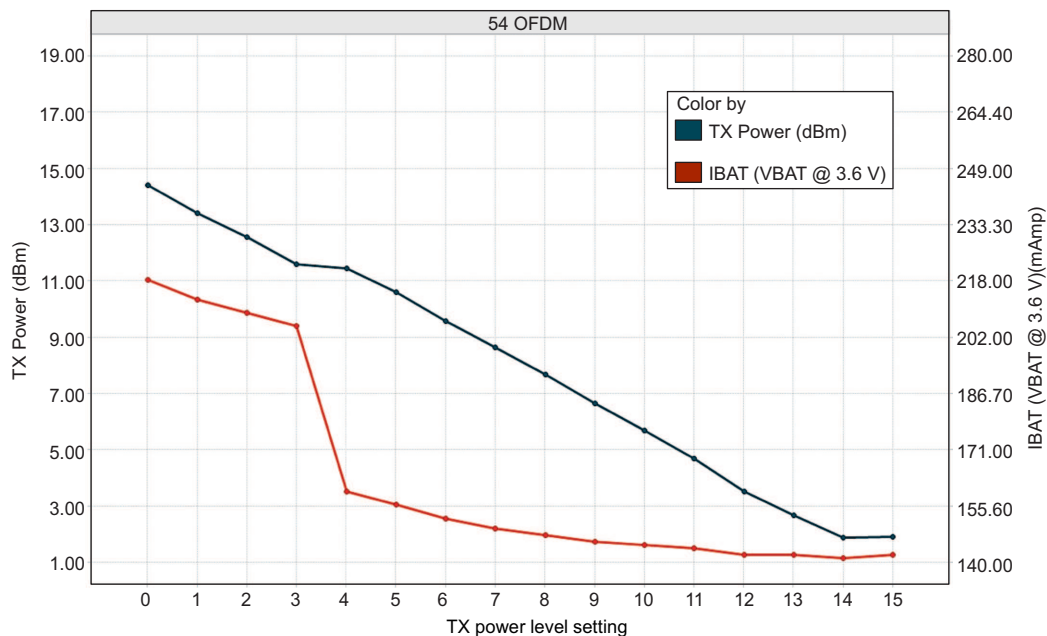


Figure 4-5. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

4.10 Thermal Characteristics for RGC Package

| PARAMETER | AIR FLOW | | | |
|---------------|-------------|---------------|---------------|---------------|
| | 0 lfm (C/W) | 150 lfm (C/W) | 250 lfm (C/W) | 500 lfm (C/W) |
| θ_{ja} | 23 | 14.6 | 12.4 | 10.8 |
| Ψ_{jt} | 0.2 | 0.2 | 0.3 | 0.1 |
| Ψ_{jb} | 2.3 | 2.3 | 2.2 | 2.4 |
| θ_{jc} | 6.3 | | | |
| θ_{jb} | 2.4 | | | |

4.11 Timing and Switching Characteristics

4.11.1 Power Supply Sequencing

For proper operation of the CC3200 device, perform the recommended power-up sequencing as follows:

1. Tie V_{BAT} (pins 37, 39, 44) and V_{IO} (pins 54 and 10) together on the board.
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100K || 0.1 μ F, RC = 10 ms).
3. For an external RTC clock, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see [Section 4.11.2, Reset Timing](#).

4.11.2 Reset Timing

4.11.2.1 nRESET (32K XTAL)

Figure 4-6 shows the reset timing diagram for the 32K XTAL first-time power-up and reset removal.

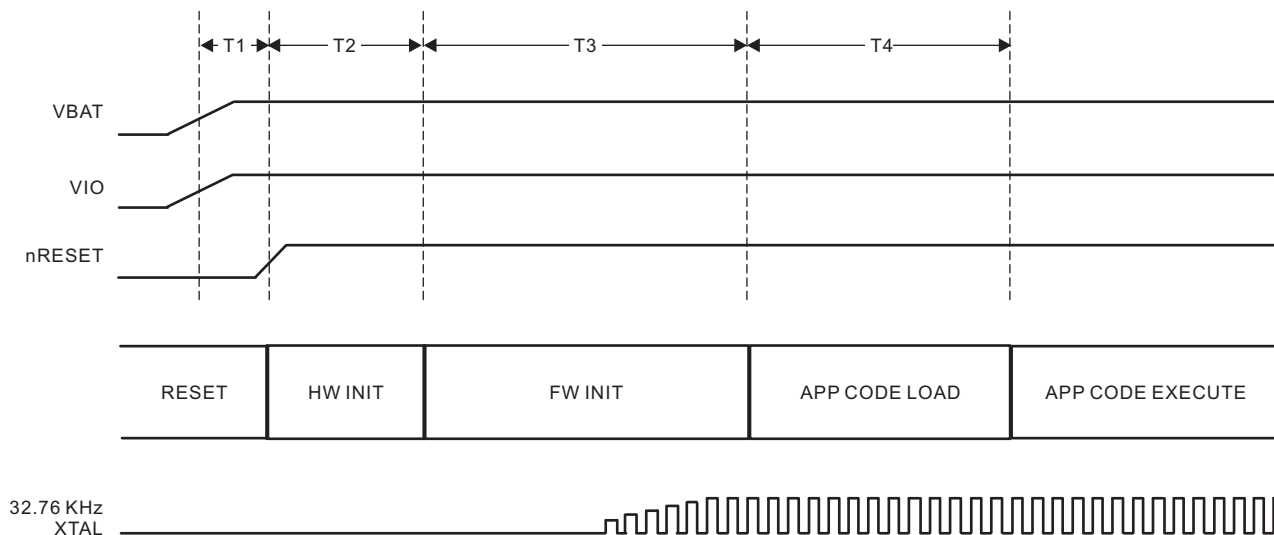


Figure 4-6. First-Time Power-Up and Reset Removal Timing Diagram (32K XTAL)

Table 4-2 describes the timing requirements for the 32K XTAL first-time power-up and reset removal.

Table 4-2. First-Time Power-Up and Reset Removal Timing Requirements (32K XTAL)

| Item | Name | Description | Min | Typ | Max |
|------|---|---|-----|-------|-----|
| T1 | Supply settling time | Depends on application board power supply, decap, and so on | | 3 ms | |
| T2 | Hardware wakeup time | | | 25 ms | |
| T3 | Time taken by ROM firmware to initialize hardware | Includes 32.768 -kHz XOSC settling time | | 1.1 s | |
| T4 | App code load time | Image size (KByte) x 0.75 ms | | | |

4.11.2.2 nRESET (External 32K)

Figure 4-7 shows the reset timing diagram for the external 32K first-time power-up and reset removal.

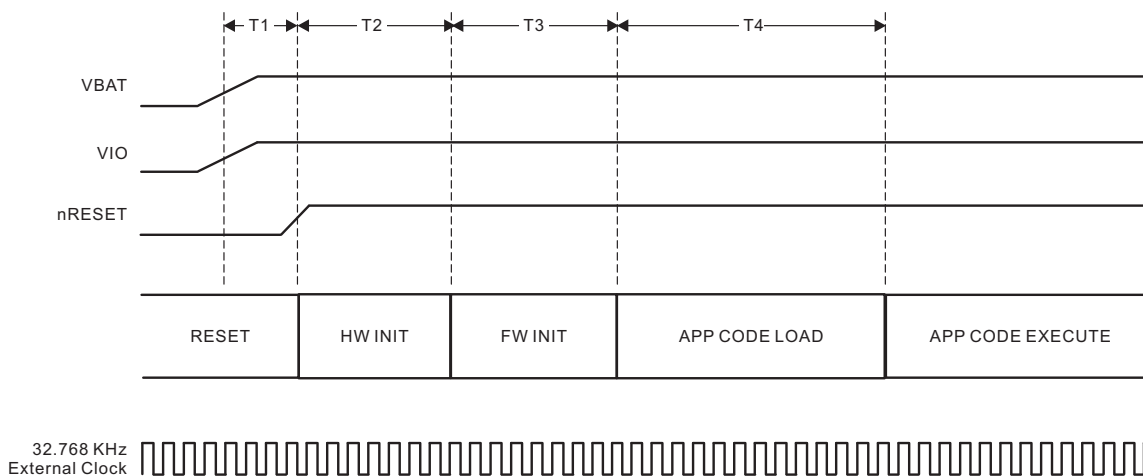


Figure 4-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32K)

Table 4-3 describes the timing requirements for the external 32K first-time power-up and reset removal.

Table 4-3. First-Time Power-Up and Reset Removal Timing Requirements (External 32K)

| Item | Name | Description | Min | Typ | Max |
|------|---|---|-----|-------|-----|
| T1 | Supply settling time | Depends on application board power supply, decap, and so on | | 3 ms | |
| T2 | Hardware wakeup time | | | 25 ms | |
| T3 | Time taken by ROM firmware to initialize hardware | Time taken by ROM firmware | | 3 ms | |
| T4 | App code load time | Image size (KByte) x 0.75 ms | | | |

4.11.2.3 Wakeup from Hibernate

Figure 4-8 shows the timing diagram for wakeup from the hibernate state.

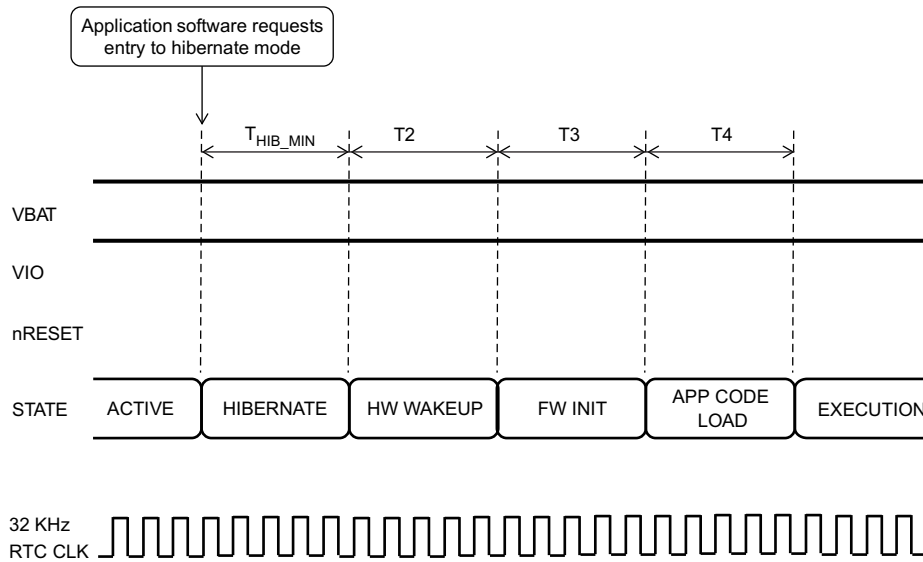


Figure 4-8. Wakeup From Hibernate Timing Diagram

NOTE

The 32.768-kHz XTAL is kept enabled by default when the chip goes to hibernate.

Table 4-4 describes the software hibernate timing requirements.

Table 4-4. Software Hibernate Timing Requirements

| Item | Name | Description | Min | Typ | Max |
|----------------|------------------------------|--|-----|------------------------------|-----|
| T_{hib_min} | Minimum hibernate time | The time for which the device has to be held in hibernate mode | | 10 ms | |
| T2 | Hardware wakeup time | Time taken by the hardware to initialize | | 25 ms | |
| T3 | Firmware initialization time | Time taken by the ROM firmware to initialize the hardware | | 3 ms | |
| T4 | Code download time | Time taken to download the code from the serial flash to on-chip RAM | | Image size (KByte) x 0.75 ms | |

4.11.3 Clock Specifications

The CC3200 device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of cheaper crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and reduce overall cost.

4.11.3.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz \pm 150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance.

Figure 4-9 shows the crystal connections for the slow clock.

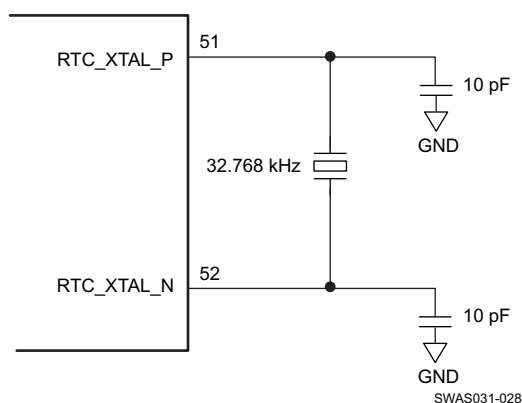


Figure 4-9. RTC Crystal Connections

4.11.3.2 Slow Clock Using an External Clock

When an RTC clock oscillator is present in the system, the CC3200 device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line and the RTC_XTAL_N line is held to VIO. The clock must be a CMOS-level clock compatible with VIO fed to the device.

Figure 4-10 shows the external RTC clock input connection.

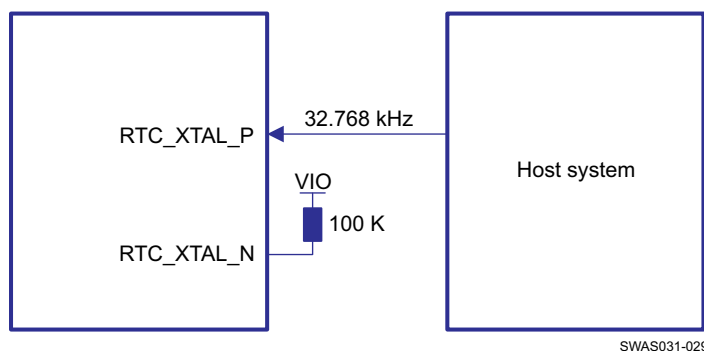


Figure 4-10. External RTC Clock Input

4.11.3.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3200 device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The XTAL is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 4-11 shows the crystal connections for the fast clock.

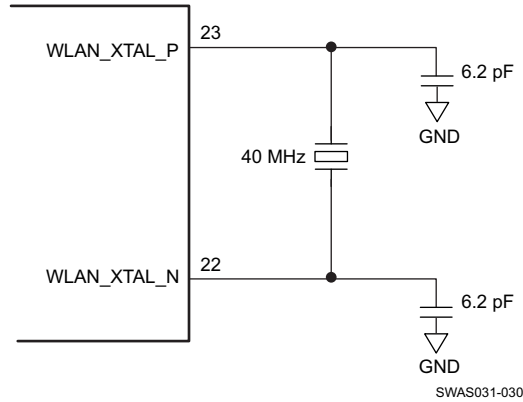


Figure 4-11. Fast Clock Crystal Connections

4.11.3.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3200 device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 4-12 shows the connection.

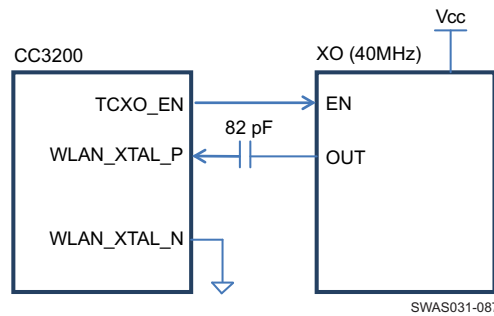


Figure 4-12. External TCXO Input

Table 4-5 lists the external F_{ref} clock requirements.

Table 4-5. External F_{ref} Clock Requirements (–40°C to +85°C)

| Characteristics | Condition | Sym | Min | Typ | Max | Unit |
|---|---------------------------------------|-----|-----|-------|-----|------|
| Frequency | | | | 40.00 | | MHz |
| Frequency accuracy (Initial + temp + aging) | | | | | ±25 | ppm |
| Frequency input duty cycle | | | 45 | 50 | 55 | % |
| Clock voltage limits | Sine or clipped sine wave, AC coupled | Vpp | 0.7 | | 1.2 | Vpp |

Table 4-5. External F_{ref} Clock Requirements (–40°C to +85°C) (continued)

| Characteristics | | Condition | Sym | Min | Typ | Max | Unit |
|----------------------|-------------|-----------|-----|-----|-----|--------|------------|
| Phase noise @ 40 MHz | | @ 1 kHz | | | | –125 | dBc/Hz |
| | | @ 10 kHz | | | | –138.5 | dBc/Hz |
| | | @ 100 kHz | | | | –143 | dBc/Hz |
| Input impedance | Resistance | | | 12 | | | K Ω |
| | Capacitance | | | | | 7 | pF |

4.11.3.5 Input Clocks/Oscillators

Table 4-6 lists the RTC crystal requirements.

Table 4-6. RTC Crystal Requirements

| CHARACTERISTICS | CONDITION | SYM | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|-----|-----|--------|-----------|------------|
| Frequency | | | | 32.768 | | kHz |
| Frequency accuracy | Initial + temp + aging | | | | ± 150 | ppm |
| Crystal ESR | 32.768 kHz, C1 = C2 = 10 pF | | | | 70 | k Ω |

Table 4-7 lists the external RTC digital clock requirements.

Table 4-7. External RTC Digital Clock Requirements

| CHARACTERISTICS | CONDITION | SYM | MIN | TYP | MAX | UNIT |
|--|-------------------------|-----------|----------------------|-------|----------------------|------------|
| Frequency | | | | 32768 | | Hz |
| Frequency accuracy (Initial + temp + aging) | | | | | ± 150 | ppm |
| Input transition time t_r/t_f (10% to 90%) | | t_r/t_f | | | 100 | ns |
| Frequency input duty cycle | | | 20 | 50 | 80 | % |
| Slow clock input voltage limits | Square wave, DC coupled | V_{ih} | $0.65 \times V_{IO}$ | | V_{IO} | V |
| | | V_{il} | 0 | | $0.35 \times V_{IO}$ | V peak |
| Input impedance | | | 1 | | | M Ω |
| | | | | | 5 | pF |

Table 4-8 lists the WLAN fast-clock crystal requirements.

Table 4-8. WLAN Fast-Clock Crystal Requirements

| CHARACTERISTICS | CONDITION | SYM | MIN | TYP | MAX | UNIT |
|--------------------|--------------------------|-----|-----|-----|----------|------|
| Frequency | | | | 40 | | MHz |
| Frequency accuracy | Initial + temp + aging | | | | ± 25 | ppm |
| Crystal ESR | 40 MHz, C1 = C2 = 6.2 pF | | 40 | 50 | 60 | Ohm |

4.11.3.6 WLAN Filter Requirements

The device requires an external bandpass filter to meet the various emission standards, including FCC. Table 4-9 presents the attenuation requirements for the bandpass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

Table 4-9. WLAN Filter Requirements

| Parameter | Frequency (MHz) | Requirements | | | |
|-------------|-----------------|--------------|-----|-----|-------|
| | | Min | Typ | Max | Units |
| Return loss | 2412 to 2484 | 10 | | | dB |

Table 4-9. WLAN Filter Requirements (continued)

| Parameter | Frequency (MHz) | Requirements | | | |
|-------------------------------|-----------------|--------------|-----|-----|----------|
| | | Min | Typ | Max | Units |
| Insertion loss ⁽¹⁾ | 2412 to 2484 | | 1 | 1.5 | dB |
| Attenuation | 800 to 830 | 30 | 45 | | dB |
| | 1600 to 1670 | 20 | 25 | | |
| | 3200 to 3300 | 30 | 48 | | |
| | 4000 to 4150 | 45 | 50 | | |
| | 4800 to 5000 | 20 | 25 | | |
| | 5600 to 5800 | 20 | 25 | | |
| | 6400 to 6600 | 20 | 35 | | |
| | 7200 to 7500 | 35 | 45 | | |
| | 7500 to 10000 | 20 | 25 | | |
| Reference Impedance | 2412 to 2484 | | 50 | | Ω |
| Filter type | Bandpass | | | | |

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

4.11.4 Peripherals

This section describes the peripherals that are supported by the CC3200 device:

- SPI
- McASP
- GPIO
- I²C
- IEEE 1149.1 JTAG
- ADC
- Camera parallel port
- UART

4.11.4.1 SPI

4.11.4.1.1 SPI Master

The CC3200 microcontroller includes one SPI module, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase, a programmable timing control between chip select and external clock generation, and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 4-13 shows the timing diagram for the SPI master.

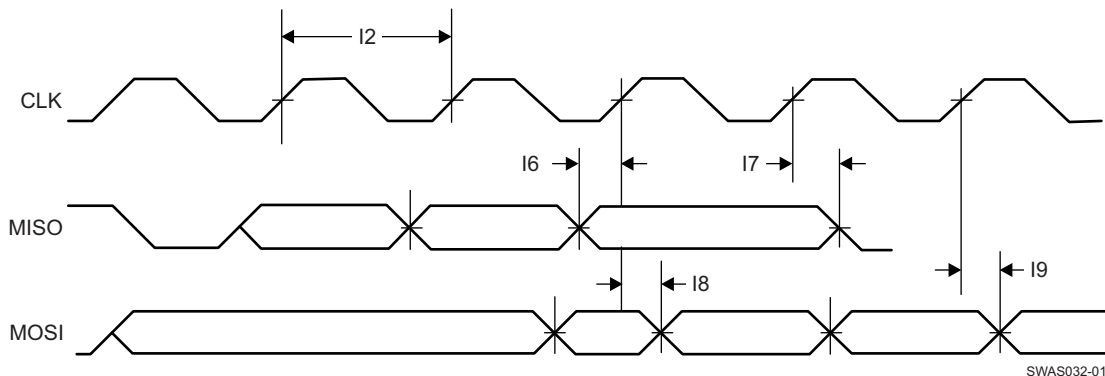


Figure 4-13. SPI Master Timing Diagram

Table 4-10 lists the timing parameters for the SPI master.

Table 4-10. SPI Master Timing Parameters

| Parameter Number | Parameter ⁽¹⁾ | Parameter Name | Min | Max | Unit |
|------------------|--------------------------|----------------------|-----|-----|------|
| I1 | F | Clock frequency | | 20 | MHz |
| I2 | T_{clk} | Clock period | 50 | | ns |
| I5 | D | Duty cycle | 45 | 55 | % |
| I6 | t_{IS} | RX data setup time | 1 | | ns |
| I7 | t_{IH} | RX data hold time | 2 | | ns |
| I8 | t_{OD} | TX data output delay | | 8.5 | ns |
| I9 | t_{OH} | TX data hold time | | 8 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.4.1.2 SPI Slave

Figure 4-14 shows the timing diagram for the SPI slave.

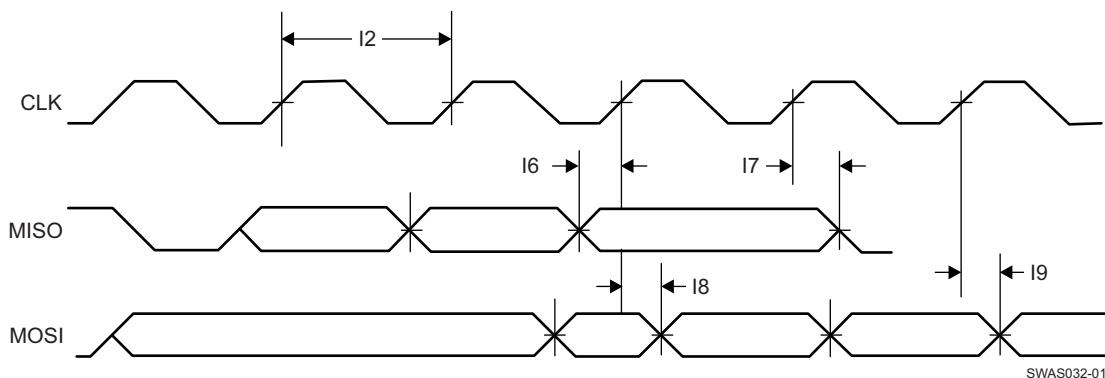


Figure 4-14. SPI Slave Timing Diagram

Table 4-11 lists the timing parameters for the SPI slave.

Table 4-11. SPI Slave Timing Parameters

| Parameter Number | Parameter ⁽¹⁾ | Parameter Name | Min | Max | Unit |
|------------------|--------------------------|--------------------------------|-----|-----|------|
| I1 | F | Clock frequency @ VBAT = 3.3 V | | 20 | MHz |
| | | Clock frequency @ VBAT ≤ 2.1 V | | 12 | |

(1) Timing parameter assumes a maximum load of 20 pF at 3.3 V.

Table 4-11. SPI Slave Timing Parameters (continued)

| Parameter Number | Parameter ⁽¹⁾ | Parameter Name | Min | Max | Unit |
|------------------|--------------------------|----------------------|-----|-----|------|
| I2 | Tclk | Clock period | 50 | | ns |
| I5 | D | Duty cycle | 45 | 55 | % |
| I6 | tIS | RX data setup time | 4 | | ns |
| I7 | tIH | RX data hold time | 4 | | ns |
| I8 | tOD | TX data output delay | | 20 | |
| I9 | tOH | TX data hold time | | 24 | ns |

4.11.4.2 McASP

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

4.11.4.2.1 I2S Transmit Mode

Figure 4-15 shows the timing diagram for the I2S transmit mode.

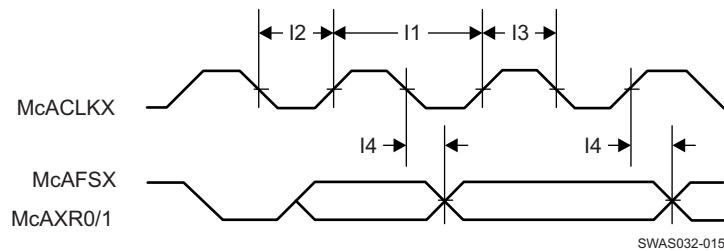
**Figure 4-15. I2S Transmit Mode Timing Diagram**

Table 4-12 lists the timing parameters for the I2S transmit mode.

Table 4-12. I2S Transmit Mode Timing Parameters

| Parameter Number | Parameter ⁽¹⁾ | Parameter Name | Min | Max | Unit |
|------------------|--------------------------|-------------------|-----|----------|------|
| I1 | fclk | Clock frequency | | 9.216 | MHz |
| I2 | tLP | Clock low period | | 1/2 fclk | ns |
| I3 | tHT | Clock high period | | 1/2 fclk | ns |
| I4 | tOH | TX data hold time | | 22 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.4.2.2 I2S Receive Mode

Figure 4-16 shows the timing diagram for the I2S receive mode.

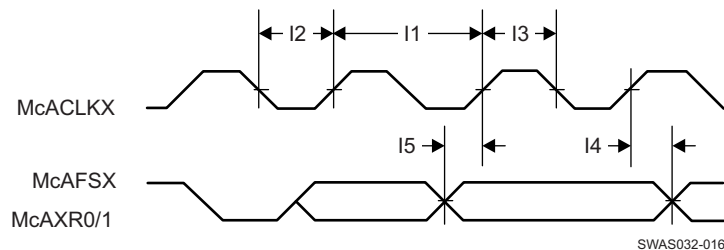
**Figure 4-16. I2S Receive Mode Timing Diagram**

Table 4-13 lists the timing parameters for the I2S receive mode.

Table 4-13. I2S Receive Mode Timing Parameters

| Parameter Number | Parameter ⁽¹⁾ | Parameter Name | Min | Max | Unit |
|------------------|--------------------------|--------------------|-----|----------|------|
| I1 | fclk | Clock frequency | | 9.216 | MHz |
| I2 | tLP | Clock low period | | 1/2 fclk | ns |
| I3 | tHT | Clock high period | | 1/2 fclk | ns |
| I4 | tOH | RX data hold time | | 0 | ns |
| I5 | tOS | RX data setup time | | 15 | ns |

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.4.3 GPIO

All digital pins of the device can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 μ A), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 4-17 shows the GPIO timing diagram.

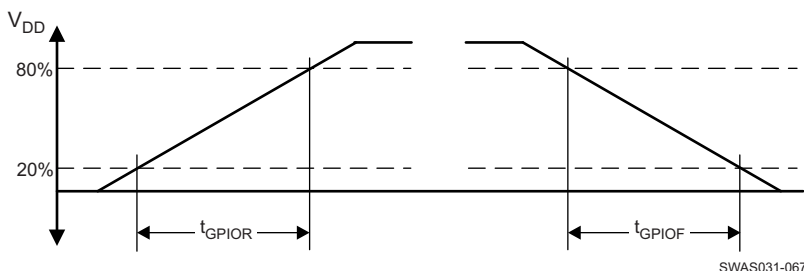


Figure 4-17. GPIO Timing

4.11.4.3.1 GPIO Output Transition Time Parameters ($V_{supply} = 3.3 V$)

Table 4-14 lists the GPIO output transition times for $V_{supply} = 3.3 V$.

Table 4-14. GPIO Output Transition Times ($V_{supply} = 3.3 V$)⁽¹⁾⁽²⁾

| Drive Strength (mA) | Drive Strength Control Bits | T_r (ns) | | | T_f (ns) | | |
|---------------------|----------------------------------|------------|-----|------|------------|-----|------|
| | | Min | Nom | Max | Min | Nom | Max |
| 2 | 2MA_EN=1 4MA_EN=0 8MA_EN=0 | 8.0 | 9.3 | 10.7 | 8.2 | 9.5 | 11.0 |
| 4 | 2MA_EN=0 4MA_EN=1 8MA_EN=0 | 6.6 | 7.1 | 7.6 | 4.7 | 5.2 | 5.8 |
| 8 | 2MA_EN=0 4MA_EN=0 8MA_EN=1 | 3.2 | 3.5 | 3.7 | 2.3 | 2.6 | 2.9 |
| 14 | 2MA_EN=1 4MA_EN=1 8MA_EN=1 | 1.7 | 1.9 | 2.0 | 1.3 | 1.5 | 1.6 |

(1) $V_{supply} = 3.3 V$, $T = 25^\circ C$, total pin load = 30 pF

(2) The transition data applies to the pins other than the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

4.11.4.3.2 GPIO Output Transition Time Parameters ($V_{\text{supply}} = 1.8 \text{ V}$)

Table 4-15 lists the GPIO output transition times for $V_{\text{supply}} = 1.8 \text{ V}$.

Table 4-15. GPIO Output Transition Times ($V_{\text{supply}} = 1.8 \text{ V}$)⁽¹⁾⁽²⁾

| Drive Strength (mA) | Drive Strength Control Bits | T_r (ns) | | | T_f (ns) | | |
|---------------------|----------------------------------|------------|------|------|------------|------|------|
| | | Min | Nom | Max | Min | Nom | Max |
| 2 | 2MA_EN=1 4MA_EN=0 8MA_EN=0 | 11.7 | 13.9 | 16.3 | 11.5 | 13.9 | 16.7 |
| 4 | 2MA_EN=0 4MA_EN=1 8MA_EN=0 | 13.7 | 15.6 | 18.0 | 9.9 | 11.6 | 13.6 |
| 8 | 2MA_EN=0 4MA_EN=0 8MA_EN=1 | 5.5 | 6.4 | 7.4 | 3.8 | 4.7 | 5.8 |
| 14 | 2MA_EN=1 4MA_EN=1 8MA_EN=1 | 2.9 | 3.4 | 4.0 | 2.2 | 2.7 | 3.3 |

(1) $V_{\text{supply}} = 1.8 \text{ V}$, $T = 25^\circ\text{C}$, total pin load = 30 pF

(2) The transition data applies to the pins other than the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

4.11.4.3.3 GPIO Input Transition Time Parameters

Table 4-16 lists the input transition time parameters.

Table 4-16. GPIO Input Transition Time Parameters

| Parameter | Condition | Symbol | Min | Max | Unit |
|--|-----------|--------|-----|-----|------|
| Input transition time (t_r, t_f), 10% to 90% | | t_r | 1 | 3 | ns |
| | | t_f | 1 | 3 | |

4.11.4.4 I²C

The CC3200 microcontroller includes one I²C module operating with standard (100 Kbps) or fast (400 Kbps) transmission speeds.

Figure 4-18 shows the I²C timing diagram.

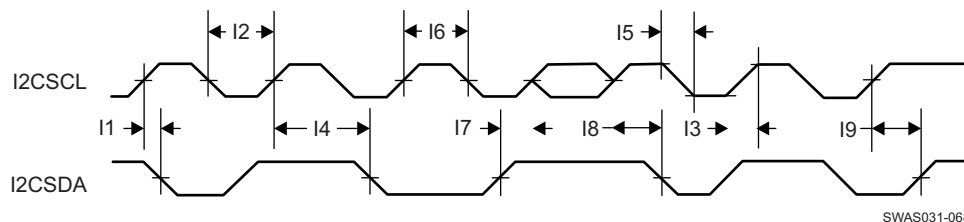


Figure 4-18. I²C Timing

Table 4-17 lists the I²C timing parameters.

Table 4-17. I²C Timing Parameters⁽¹⁾

| Parameter Number | Parameter | Parameter Name | Min | Max | Unit |
|------------------|-------------------|----------------------------|----------------------|----------------------|--------------|
| I2 | t _{LP} | Clock low period | See ⁽²⁾ . | - | System clock |
| I3 | t _{SRT} | SCL/SDA rise time | - | See ⁽³⁾ . | ns |
| I4 | t _{DH} | Data hold time | NA | - | |
| I5 | t _{SFT} | SCL/SDA fall time | - | 3 | ns |
| I6 | t _{HT} | Clock high time | See ⁽²⁾ . | - | System clock |
| I7 | t _{DS} | Data setup time | t _{LP} /2 | | System clock |
| I8 | t _{SCSR} | Start condition setup time | 36 | - | System clock |
| I9 | t _{SCS} | Stop condition setup time | 24 | - | System clock |

- (1) All timing is with 6-mA drive and 20-pF load.
- (2) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
- (3) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic 1 is the result of external pullup. Rise time depends on the external signal capacitance and external pullup register value.

4.11.4.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1, *Test Access Port and Boundary- Scan Architecture*.

Figure 4-19 shows the JTAG timing diagram.

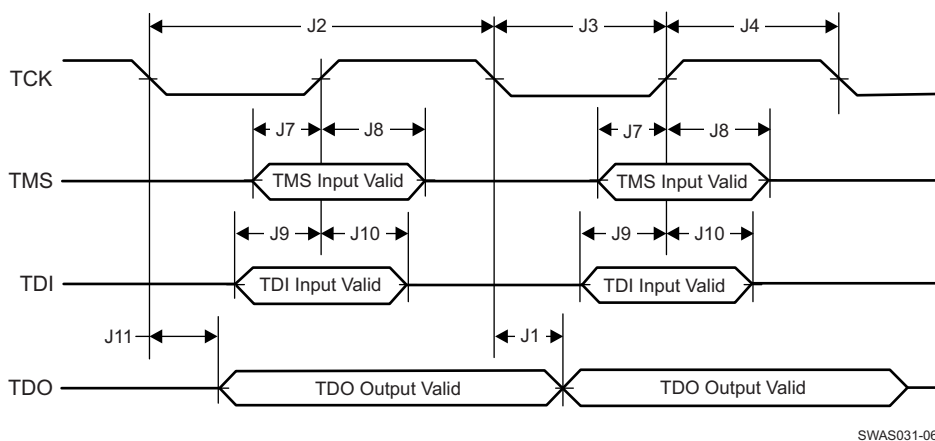


Figure 4-19. JTAG Timing

Table 4-18 lists the JTAG timing parameters.

Table 4-18. JTAG Timing Parameters

| Parameter Number | Parameter | Parameter Name | Min | Max | Unit |
|------------------|---------------------|-------------------|-----|---------------------|------|
| J1 | f _{TCK} | Clock frequency | | 15 | MHz |
| J2 | t _{TCK} | Clock period | | 1/f _{TCK} | ns |
| J3 | t _{CL} | Clock low period | | t _{TCK} /2 | ns |
| J4 | t _{CH} | Clock high period | | t _{TCK} /2 | ns |
| J7 | t _{TMS_SU} | TMS setup time | 1 | | |
| J8 | t _{TMS_HO} | TMS hold time | 16 | | |
| J9 | t _{TDI_SU} | TDI setup time | 1 | | |
| J10 | t _{TDI_HO} | TDI hold time | 16 | | |

Table 4-18. JTAG Timing Parameters (continued)

| Parameter Number | Parameter | Parameter Name | Min | Max | Unit |
|------------------|-----------|----------------|-----|-----|------|
| J11 | tTDO_HO | TDO hold time | | 15 | |

4.11.4.6 ADC

Table 4-19 lists the ADC electrical specifications.

Table 4-19. ADC Electrical Specifications

| Parameter | Description | Condition and Assumptions | Min | Typ | Max | Unit |
|--------------------------|---|--|------|---------|-----|----------|
| Nbits | Number of bits | | | 12 | | Bits |
| INL | Integral nonlinearity | Worst-case deviation from histogram method over full scale (not including first and last three LSB levels) | -2.5 | | 2.5 | LSB |
| DNL | Differential nonlinearity | Worst-case deviation of any step from ideal | -1 | | 4 | LSB |
| Input range | | | 0 | | 1.4 | V |
| Driving source impedance | | | | | 100 | Ω |
| FCLK | Clock rate | Successive approximation input clock rate | | 10 | | MHz |
| Input capacitance | | | | 3.2 | | pF |
| Number of channels | | | | 4 | | |
| F _{sample} | Sampling rate of each ADC | | | 62.5 | | KSPS |
| F _{input_max} | Maximum input signal frequency | | | | 31 | kHz |
| SINAD | Signal-to-noise and distortion | Input frequency dc to 300 Hz and 1.4 V _{pp} sine wave input | 55 | 60 | | dB |
| I _{active} | Active supply current | Average for analog-to-digital during conversion without reference current | | 1.5 | | mA |
| I _{PD} | Power-down supply current for core supply | Total for analog-to-digital when not active (this must be the SoC level test) | | 1 | | μ A |
| Absolute offset error | | FCLK = 10 MHz | | \pm 2 | | mV |
| Gain error | | | | \pm 2 | | % |

Figure 4-20 shows the ADC clock timing diagram.

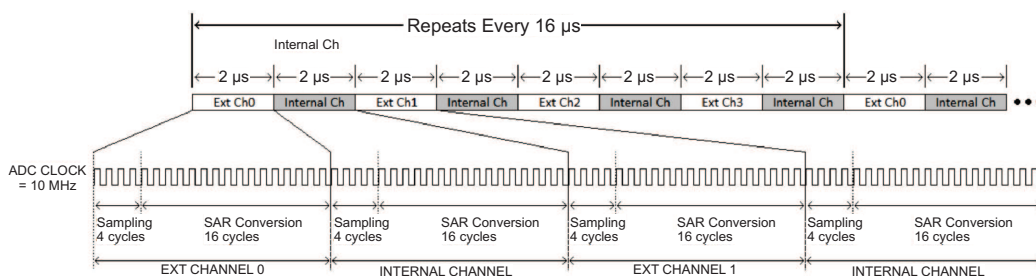


Figure 4-20. ADC Clock Timing

4.11.4.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 4-21 shows the timing diagram for the camera parallel port.

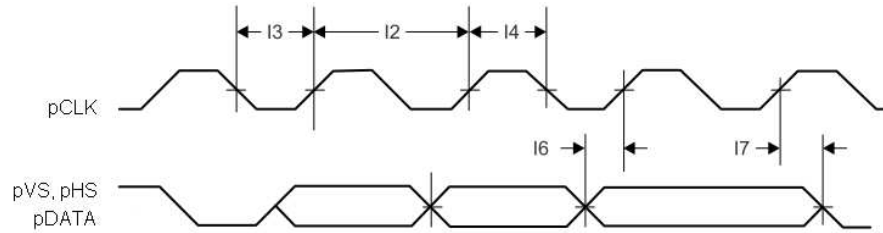


Figure 4-21. Camera Parallel Port Timing Diagram

Table 4-20 lists the timing parameters for the camera parallel port.

Table 4-20. Camera Parallel Port Timing Parameters

| Parameter Number | Parameter | Parameter Name | Min | Max | Unit |
|------------------|-----------|--------------------|-----|-------------|------|
| | pCLK | Clock frequency | | 2 | MHz |
| I2 | T_{clk} | Clock period | | $1/pCLK$ | ns |
| I3 | t_{LP} | Clock low period | | $T_{clk}/2$ | ns |
| I4 | t_{HT} | Clock high period | | $T_{clk}/2$ | ns |
| I7 | D | Duty cycle | | 45 to 55 | % |
| I8 | t_{IS} | RX data setup time | | 2 | ns |
| I9 | t_{IH} | RX data hold time | | 2 | ns |

4.11.4.8 UART

The CC3200 device includes two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16 x 8 TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
 - 5, 6, 7, or 8 data bits
 - Even, odd, stick, or no-parity bit generation and detection
 - 1 or 2 stop-bit generation
- RTS and CTS hardware flow support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using μ DMA
 - Separate channels for transmit and receive
 - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
 - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

5 Detailed Description

5.1 Overview

The CC3200 device has a rich set of peripherals for diverse application requirements. The device optimizes bus matrix and memory management to give the application developer the needed advantage. This section briefly highlights the internal details of the CC3200 device and offers suggestions for application configurations.

5.1.1 Device Features

5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the CC3200 SimpleLink Wi-Fi solution.

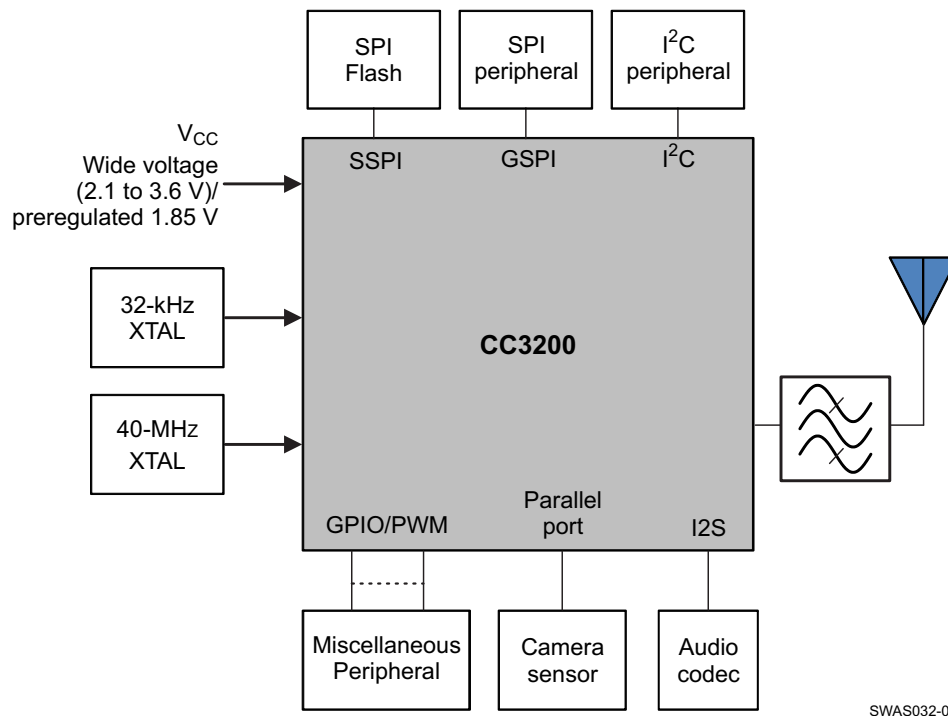


Figure 5-1. Functional Block Diagram

5.3 ARM Cortex-M4 Processor Core Subsystem

The high-performance ARM Cortex-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The ARM Cortex-M4 core has low-latency interrupt processing with the following features:
 - A 32-bit ARM Cortex Thumb® instruction set optimized for embedded applications
 - Handler and thread modes
 - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
 - Support for ARMv6 unaligned accesses

- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
 - Bits of priority configurable from 3 to 8
 - Dynamic reprioritization of interrupts
 - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
 - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
 - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
 - Wake-up interrupt controller (WIC) providing ultra-low power sleep mode support
- Bus interfaces:
 - Three advanced high-performance bus (AHB-Lite) interfaces: ICode, DCode, and system bus interfaces
 - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
 - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
 - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
 - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

5.4 CC3200 Device Encryption

Figure 5-2 shows a standard MCU for the CC3200 device. Application image and user data files are not encrypted. Network certificates are encrypted using a device-specific key.

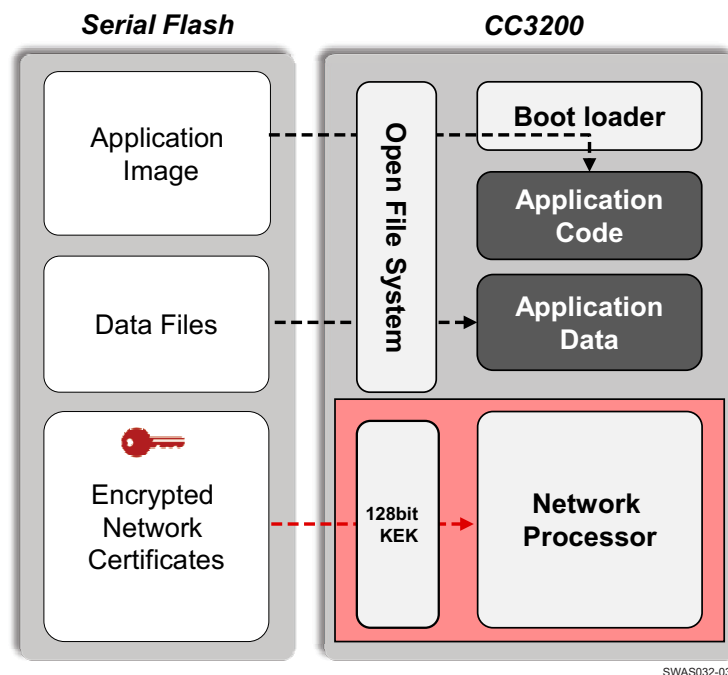


Figure 5-2. CC3200 Standard MCU

5.5 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated ARM MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3200 device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv4 TCP/IP stack.

Table 5-1 summarizes the NWP features.

Table 5-1. Summary of Features Supported by the NWP Subsystem

| Item | Domain | Category | Feature | Details |
|------|--------|---------------|-----------------------|--|
| 1 | TCP/IP | Network Stack | IPv4 | Baseline IPv4 stack |
| 2 | TCP/IP | Network Stack | TCP/UDP | Base protocols |
| 3 | TCP/IP | Protocols | DHCP | Client and server mode |
| 4 | TCP/IP | Protocols | ARP | Support ARP protocol |
| 5 | TCP/IP | Protocols | DNS/mDNS | DNS Address resolution and local server |
| 6 | TCP/IP | Protocols | IGMP | Up to IGMPv3 for multicast management |
| 7 | TCP/IP | Applications | mDNS | Support multicast DNS for service publishing over IP |
| 8 | TCP/IP | Applications | mDNS-SD | Service discovery protocol over IP in local network |
| 9 | TCP/IP | Applications | Web Sever/HTTP Server | URL static and dynamic response with template. |
| 10 | TCP/IP | Security | TLS/SSL | TLS v1.2 (client/server)/SSL v3.0 |
| 11 | TCP/IP | Security | TLS/SSL | For the supported Cipher Suite, go to SimpleLink Wi-Fi CC3200 SDK . |
| 12 | TCP/IP | Sockets | RAW Sockets | User-defined encapsulation at WLAN MAC/PHY or IP layers |
| 13 | WLAN | Connection | Policies | Allows management of connection and reconnection policy |
| 14 | WLAN | MAC | Promiscuous mode | Filter-based Promiscuous mode frame receiver |
| 15 | WLAN | Performance | Initialization time | From enable to first connection to open AP less than 50 ms |
| 16 | WLAN | Performance | Throughput | UDP = 16 Mbps |
| 17 | WLAN | Performance | Throughput | TCP = 13 Mbps |
| 18 | WLAN | Provisioning | WPS2 | Enrollee using push button or PIN method. |
| 19 | WLAN | Provisioning | AP Config | AP mode for initial product configuration (with configurable Web page and beacon Info element) |
| 20 | WLAN | Provisioning | SmartConfig | Alternate method for initial product configuration |
| 21 | WLAN | Role | Station | 802.11bgn Station with legacy 802.11 power save |
| 22 | WLAN | Role | Soft AP | 802.11 bg single station with legacy 802.11 power save |
| 23 | WLAN | Role | P2P | P2P operation as GO |
| 24 | WLAN | Role | P2P | P2P operation as CLIENT |
| 25 | WLAN | Security | STA-Personal | WPA2 personal security |
| 26 | WLAN | Security | STA-Enterprise | WPA2 enterprise security |
| 27 | WLAN | Security | STA-Enterprise | EAP-TLS |
| 28 | WLAN | Security | STA-Enterprise | EAP-PEAPv0/TLS |
| 29 | WLAN | Security | STA-Enterprise | EAP-PEAPv1/TLS |
| 30 | WLAN | Security | STA-Enterprise | EAP-PEAPv0/MSCHAPv2 |
| 31 | WLAN | Security | STA-Enterprise | EAP-PEAPv1/MSCHAPv2 |
| 32 | WLAN | Security | STA-Enterprise | EAP-TTLS/EAP-TLS |
| 33 | WLAN | Security | STA-Enterprise | EAP-TTLS/MSCHAPv2 |
| 34 | WLAN | Security | AP-Personal | WPA2 personal security |

5.6 Power-Management Subsystem

The CC3200 power-management subsystem contains DC-DC converters to accommodate the differing voltage or current requirements of the system.

- Digital DC-DC
 - Input: VBAT wide voltage (2.1 to 3.6 V) or preregulated 1.85 V
- ANA1 DC-DC
 - Input: VBAT wide voltage (2.1 to 3.6 V)
 - In preregulated 1.85-V mode, the ANA1 DC-DC converter is bypassed.
- PA DC-DC
 - Input: VBAT wide voltage (2.1 to 3.6 V)
 - In preregulated 1.85-V mode, the PA DC-DC converter is bypassed.

In preregulated 1.85-V mode, the ANA1 DC-DC and PA DC-DC converters are bypassed. The CC3200 device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in the following sections.

5.6.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC-DC converters. This scheme is the most common mode for the device as it supports wide-voltage operation from 2.1 to 3.6 V (for electrical connections, see [Section 6.1.1, Typical Application – CC3200 Wide-Voltage Mode](#)).

5.6.2 Preregulated 1.85 V

The preregulated 1.85-V mode of operation applies an external regulated 1.85 V directly at the pins 10, 25, 33, 36, 37, 39, 44, 48, and 54 of the device. The VBAT and the VIO are also connected to the 1.85-V supply. This mode provides the lowest BOM count version in which inductors used for PA DC-DC and ANA1 DC-DC (2.2 and 1 μ H) and a capacitor (22 μ F) can be avoided. For electrical connections, see [Section 6.1.2, Typical Application – CC3200 Preregulated 1.85-V Mode](#).

In the preregulated 1.85-V mode, the regulator providing the 1.85 V must have the following characteristics:

- Load current capacity ≥ 900 mA.
- Line and load regulation with $< 2\%$ ripple with 500 mA step current and settling time of < 4 μ s with the load step.
- The regulator must be placed very close to the CC3200 device so that the IR drop to the device is very low.

5.7 Low-Power Operating Mode

From a power-management perspective, the CC3200 device comprises the following two independent subsystems:

- Cortex-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Cortex-M4 application processor runs the user application loaded from an external serial flash. The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in [Table 5-2](#).

NOTE

[Table 5-2](#) lists the modes by power consumption, with highest power modes listed first.

Table 5-2. User Program Modes

| Application Processor (MCU) Mode | Description |
|----------------------------------|--|
| MCU active mode | MCU executing code at 80-MHz state rate |
| MCU sleep mode | The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral. |
| MCU LPDS mode | State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs defined in Table 3-1 as the wake-up source. |
| MCU hibernate mode | The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The real-time clock (RTC) clock keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO (GPIO0–GPIO6). |

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception.

Table 5-3. Networking Subsystem Modes

| Network Processor Mode | Description |
|--|--|
| Network active mode processing layer 3, 2, and 1 | Transmitting or receiving IP protocol packets |
| Network active mode (processing layer 2 and 1) | Transmitting or receiving MAC management frames; IP processing not required. |
| Network active listen mode | Special power optimized active mode for receiving beacon frames (no other frames supported) |
| Network connected Idle | A composite mode that implements 802.11 infrastructure power save operation. The CC3200R network processor automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the access point. If not, the network processor returns to LPDS mode and the cycle repeats. |
| Network LPDS mode | Low-power state between beacons in which the state is retained by the network processor, allowing for a rapid wake up. |
| Network disabled | |

The operation of the application and network processor ensures that the device remains in the lowest power mode most of the time to preserve battery life. [Table 5-4](#) summarizes the important CC3200 chip-level power modes.

Table 5-4. Important Chip-Level Power Modes

| Power States for Applications MCU and Network Processor | Network Processor Active Mode (Transmit, Receive, or Listen) | Network Processor LPDS Mode | Network Processor Disabled |
|---|---|---|----------------------------|
| MCU active mode | Chip = active (C) | Chip = active | Chip = active |
| MCU LPDS mode | Chip = active (A) | Chip = LPDS (B) | Chip = LPDS |
| MCU hibernate mode | Not supported because chip is hibernated by MCU; thus, network processor cannot be in active mode | Not supported because chip is hibernated by MCU; thus, network processor cannot be in LPDS mode | Chip = hibernate (D) |

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of modes A (receiving a beacon frame) and B (waiting for the next beacon).
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data spends most of the time in mode D (hibernate), jumping briefly to mode C (active) to transmit data.

5.8 Memory

5.8.1 External Memory Requirements

The CC3200 device maintains a proprietary file system on the SFLASH. The CC3200 file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always located at the beginning of the SFLASH. The applications microcontroller must access the SFLASH memory area allocated to the file system directly through the CC3200 file system. The applications microcontroller must not access the SFLASH memory area directly.

The file system manages the allocation of SFLASH blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on SFLASH using human-readable file names rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system (see [Figure 5-2](#)).

All file types can have a maximum of 128 supported files in the file system. All files are stored in blocks of 4KB and thus use a minimum of 4KB of flash space. Encrypted files with fail-safe support and optional security are twice the original size and use a minimum of 8KB. Encrypted files are counted as fail safe in terms of space. The maximum file size is 16MB.

[Table 5-5](#) lists the SFLASH size recommendations.

Table 5-5. CC3200 SFLASH Size Recommendations

| Item | Typical Fail-Safe | Typical NonFail-Safe |
|--------------------------------|-------------------|----------------------|
| File system | 20KB | 20KB |
| Service pack | 224KB | 112KB |
| System and configuration files | 216KB | 108KB |
| MCU code | 512KB | 256KB |
| Total | 8Mb | 4Mb |
| Recommended | 16Mb | 8Mb |

The CC3200 device supports JEDEC specification SFDP (serial flash device parameters). The following SFLASH devices are verified for functionality with the CC3200 device in addition to the ones in the reference design:

- Micron (N25Q128-A13BSE40): 128Mb
- Spansion (S25FL208K): 8Mb
- Winbond (W25Q16V): 16Mb
- Adesto (AT25DF081A): 8Mb
- Macronix (MX25L12835F-M2): 128Mb

For compatibility with the CC3200 device, the SFLASH device must support the following commands:

- Command 0x9F (read the device ID [JEDEC]). Procedure: SEND 0x9F, READ 3 bytes.
- Command 0x05 (read the status of the SFLASH). Procedure: SEND 0x05, READ 1 byte. Assume bit 0 is busy and bit 1 is write enable.

- Command 0x06 (set write enable). Procedure: SEND 0x06, read status until write-enable bit is set.
- Command 0xC7 (chip erase). Procedure: SEND 0xC7, read status until busy bit is cleared.
- Command 0x03 (read data). Procedure: SEND 0x03, SEND 24-bit address, read n bytes.
- Command 0x02 (write page). Procedure: SEND 0x02, SEND 24-bit address, write n bytes ($0 < n < 256$).
- Command 0x20 (sector erase). Procedure: SEND 0x20, SEND 24-bit address, read status until busy bit is cleared. Sector size is assumed to be always 4K.

5.8.2 Internal Memory

The CC3200 device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. To select the appropriate SRAM configuration, see the device variants listed in the orderable addendum at the end of this datasheet. The micro direct memory access (μ DMA) controller can transfer data to and from SRAM and various peripherals. The CC3200 ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3200 API list.

5.8.2.1 SRAM

The CC3200 family provides up to 256KB of zero-wait-state, on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is located at offset 0x2000 0000 of the device memory map.

Use the μ DMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

5.8.2.2 ROM

The internal zero-wait-state ROM of the CC3200 device is at address 0x0000 0000 of the device memory and programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The CC3200 DriverLib software library controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory to be used for other purposes.

5.8.2.3 Memory Map

Table 5-6 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 5-6. Memory Map

| Start Address | End Address | Description | Comment |
|---------------|-------------|---|---------|
| 0x0000 0000 | 0x0007 FFFF | On-chip ROM (Bootloader + DriverLib) | |
| 0x2000 0000 | 0x2003 FFFF | Bit-banded on-chip SRAM | |
| 0x2200 0000 | 0x23FF FFFF | Bit-band alias of 0x2000 0000 through 0x200F FFFF | |
| 0x4000 0000 | 0x4000 0FFF | Watchdog timer A0 | |
| 0x4000 4000 | 0x4000 4FFF | GPIO port A0 | |
| 0x4000 5000 | 0x4000 5FFF | GPIO port A1 | |
| 0x4000 6000 | 0x4000 6FFF | GPIO port A2 | |

Table 5-6. Memory Map (continued)

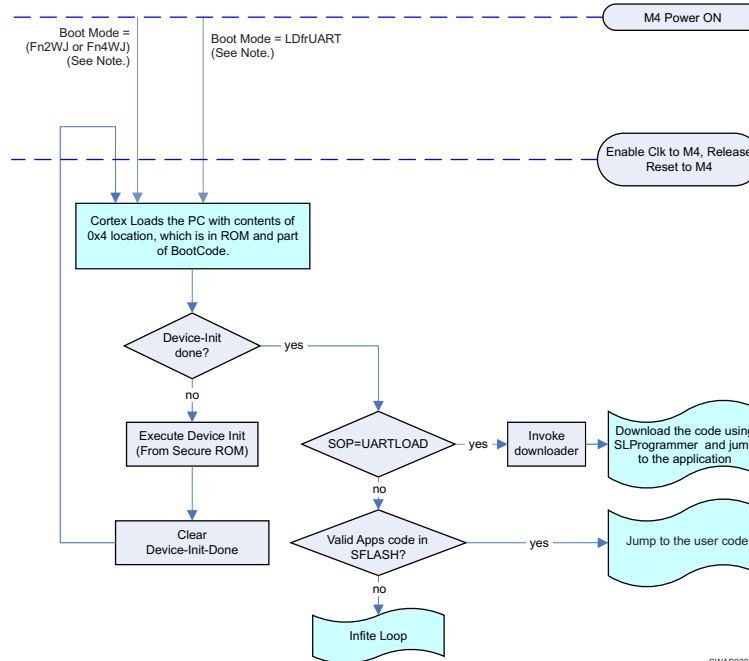
| Start Address | End Address | Description | Comment |
|---------------|-------------|--|--------------------------------|
| 0x4000 7000 | 0x4000 7FFF | GPIO port A3 | |
| 0x4000 C000 | 0x4000 CFFF | UART A0 | |
| 0x4000 D000 | 0x4000 DFFF | UART A1 | |
| 0x4002 0000 | 0x4002 07FF | I ² C A0 (Master) | |
| 0x4002 0800 | 0x4002 0FFF | I ² C A0 (Slave) | |
| 0x4003 0000 | 0x4003 0FFF | General-purpose timer A0 | |
| 0x4003 1000 | 0x4003 1FFF | General-purpose timer A1 | |
| 0x4003 2000 | 0x4003 2FFF | General-purpose timer A2 | |
| 0x4003 3000 | 0x4003 3FFF | General-purpose timer A3 | |
| 0x400F 7000 | 0x400F 7FFF | Configuration registers | |
| 0x400F E000 | 0x400F EFFF | System control | |
| 0x400F F000 | 0x400F FFFF | μDMA | |
| 0x4200 0000 | 0x43FF FFFF | Bit band alias of 0x4000.0000 through 0x400F.FFFF | |
| 0x4401 C000 | 0x4401 EFFF | McASP | |
| 0x4402 0000 | 0x4402 0FFF | SSPI | Used for external serial flash |
| 0x4402 1000 | 0x4402 2FFF | GSPI | Used by application processor |
| 0x4402 5000 | 0x4402 5FFF | MCU reset clock manager | |
| 0x4402 6000 | 0x4402 6FFF | MCU configuration space | |
| 0x4402 D000 | 0x4402 DFFF | Global power, reset, and clock manager (GPRCM) | |
| 0x4402 E000 | 0x4402 EFFF | MCU shared configuration | |
| 0x4402 F000 | 0x4402 FFFF | Hibernate configuration | |
| 0x4403 0000 | 0x4403 FFFF | Crypto range (includes apertures for all crypto-related blocks as follows) | |
| 0x4403 0000 | 0x4403 0FFF | DTHE registers and TCP checksum | |
| 0x4403 5000 | 0x4403 5FFF | MD5/SHA | |
| 0x4403 7000 | 0x4403 7FFF | AES | |
| 0x4403 9000 | 0x4403 9FFF | DES | |
| 0xE000 0000 | 0xE000 0FFF | Instrumentation trace Macrocell™ | |
| 0xE000 1000 | 0xE000 1FFF | Data watchpoint and trace (DWT) | |
| 0xE000 2000 | 0xE000 2FFF | Flash patch and breakpoint (FPB) | |
| 0xE000 E000 | 0xE000 EFFF | Nested vectored interrupt controller (NVIC) | |
| 0xE004 0000 | 0xE004 0FFF | Trace port interface unit (TPIU) | |
| 0xE004 1000 | 0xE004 1FFF | Reserved for embedded trace macrocell (ETM) | |
| 0xE004 2000 | 0xE00F FFFF | Reserved | |

5.9 Boot Modes

5.9.1 Overview

The boot process of the application processor includes two phases. The first phase consists of unrestricted access to all register space and configuration of the specific device setting. In the second phase, the application processor executes user-specific code.

Figure 5-3 shows the bootloader flow chart.



Note: For definitions of the SoP mode functional configurations, see [Table 5-7](#).

Figure 5-3. Bootloader Flow Chart

5.9.2 Invocation Sequence/Boot Mode Selection

The following sequence of events occur during the Cortex processor boot:

1. After power-on-reset (POR), the processor starts execution.
2. The processor jumps to the first few lines (FFL) of code in the ROM to determine if the current boot is the first device-init boot or the second MCU boot. The determination is based on the Device-Init flag in a secure register. The Device-Init flag is set out of POR. The registers in the secure region are accessible only in the device-init mode.
3. If the current boot is the first boot, the processor executes the device-init code from ROM.
4. At the end of the boot, the processor clears the Device-Init flag and changes the master ID of the processor and the DMA. These registers are part of the secure region.
5. The processor resets itself, initiating a second boot.
6. During the second boot, the processor rereads the Device-Init flag, the bit is cleared, and the processor obtains a different master ID.
7. After executing FFL and the unsecure boot code, the processor jumps to the developer code (application).
8. For the rest of the operation (until the next power cycle), the Cortex mode is designated the MCU. During this phase, access to the secure region is restricted.

5.9.3 Boot Mode List

The CC3200 device implements a sense-on-power (SoP) scheme to determine the device operation mode. The device can be configured to power up in one of the three following modes:

- Fn4WJ: Functional mode with a 4-wire JTAG mapped to fixed pins.
- Fn2WJ: Functional mode with a 2-wire SWD mapped to fixed pins.
- LDfrUART: UART load mode to flash the system during development and in OEM assembly line (for example, serial flash connected to the CC3200R device).

SoP values are sensed from the device pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and then determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0) [Table 5-7](#) show the pull configurations.

Table 5-7. CC32x0 Functional Configurations

| Name | SoP[2] | SoP[1] | SoP[0] | SoP Mode | Comment |
|----------------|----------|----------|----------|----------|---|
| UARTLOAD | Pullup | Pulldown | Pulldown | LDfrUART | Factory/Lab Flash/SRAM load through UART. Device waits indefinitely for UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode. |
| FUNCTIONAL_2WJ | Pulldown | Pulldown | Pullup | Fn2WJ | Functional development mode. In this mode, two-pin SWD is available to the developer. TMS and TCK are available for debugger connection. |
| FUNCTIONAL_4WJ | Pulldown | Pulldown | Pulldown | Fn4WJ | Functional development mode. In this mode, four-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection. |

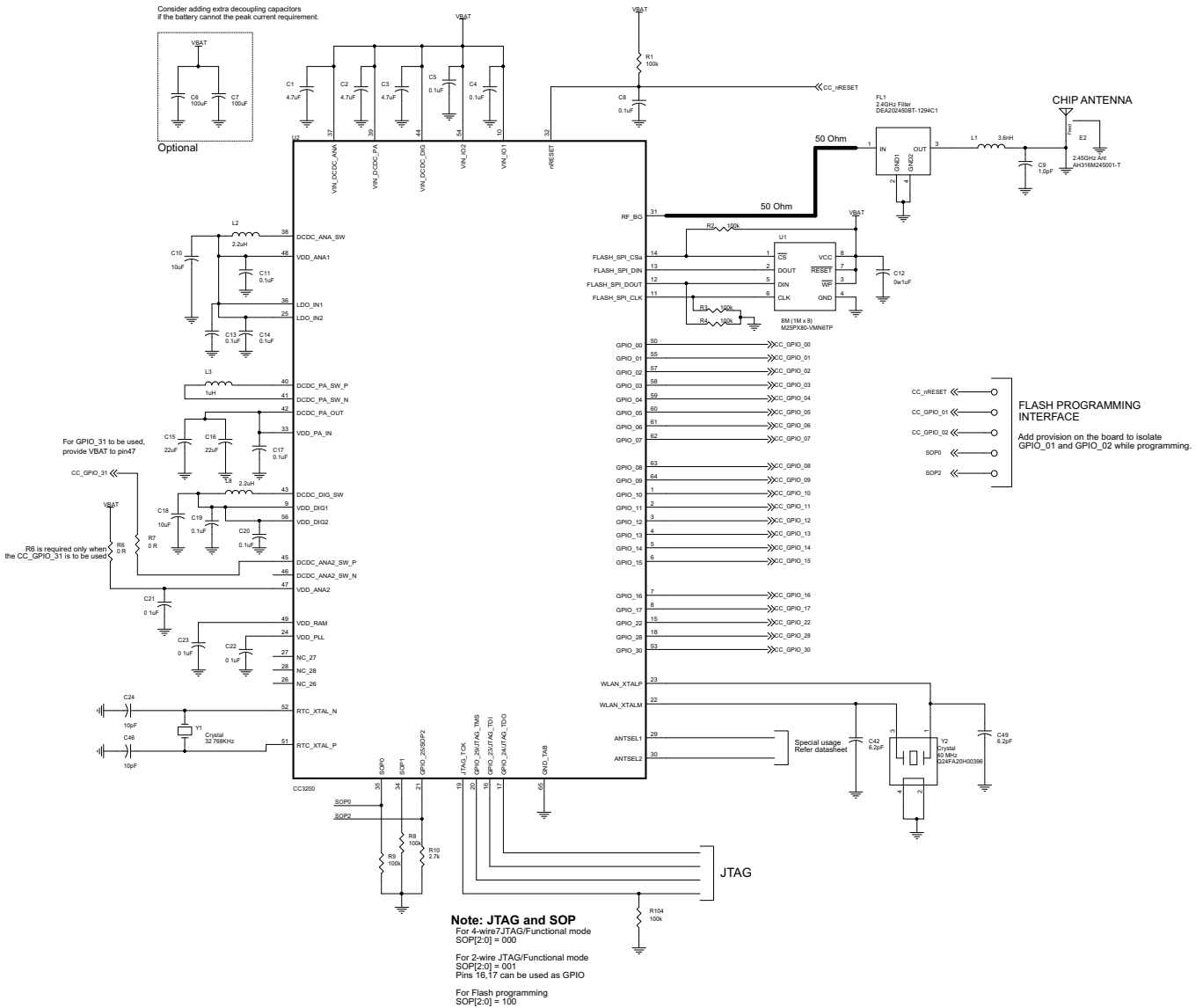
The recommended value of pull resistors for SOP0 and SOP1 is 100 k Ω and 2.7 k Ω for SOP2. SOP2 can be used by the application for other functions after chip power-up is complete. However, to avoid spurious SOP values from being sensed at power-up, TI strongly recommends that the SOP2 pin be used only for output signals. On the other hand, the SOP0 and SOP1 pins are multiplexed with WLAN analog test pins and are not available for other functions.

6 Applications and Implementation

6.1 Application Information

6.1.1 Typical Application – CC3200 Wide-Voltage Mode

Figure 6-1 shows the schematics for an application using the CC3200 wide-voltage mode.



NOTE: This schematic is rated from 2.3 to 3.6 V because of the limitation of the serial flash.

Figure 6-1. Schematics for CC3200 Wide-Voltage Mode Application

Table 6-1 lists the bill of materials for an application using the CC3200 wide-voltage mode.

Table 6-1. Bill of Materials for CC3200 Wide-Voltage Mode Application

| Item | Qty | Part Reference | Value | Manufacturer | Part Number | Description |
|------|-----|---|----------------|--|----------------------|--|
| 1 | 3 | C1 C2 C3 | 4.7 μ F | Samsung Electro-Mechanics America, Inc | CL05A475MQ5NRNC | Capacitor, Ceramic: 4.7 μ F 6.3 V 20% X5R 0402 |
| 2 | 13 | C4 C5 C8 C11 C12 C13 C14 C17 C19 C20 C21 C22 C23 | 0.1 μ F | Taiyo Yuden | LMK105BJ104KV-F | Capacitor, Ceramic: 0.1 μ F 10 V 10% X5R 0402 |
| 3 | 1 | C9 | 1.0 pF | Murata Electronics North America | GJM1555C1H1R0BB01D | Capacitor, Ceramic: 1 pF 50 V NP0 0402 |
| 4 | 2 | C10 C18 | 10 μ F | Murata Electronics North America | GRM188R60J106ME47D | Capacitor, Ceramic: 10 μ F 6.3 V 20% X5R 0603 |
| 5 | 2 | C15 C16 | 22 μ F | Taiyo Yuden | AMK107BBJ226MAHT | Capacitor, Ceramic: 22 μ F 4 V 20% X5R 0603 |
| 6 | 2 | C24 C46 | 10 pF | Murata Electronics North America | GRM1555C1H100FA01D | Capacitor, Ceramic: 10 pF 50 V 1% NP0 0402 |
| 7 | 2 | C42 C49 | 6.2 pF | Murata Electronics North America | GRM1555C1H6R2BA01D | Capacitor, Ceramic: 6.2 pF 50 V NP0 0402 |
| 8 | 1 | E2 | 2.4-GHz Ant | Taiyo Yuden | AH316M245001-T | Chip Antenna: 50 Ω Bluetooth WLAN ZigBee® WIMAX |
| 9 | 1 | FL1 | 2.4-GHz Filter | TDK-Epcos | DEA202450BT-1294C1-H | Filter, Bandpass: 2.4 GHz WLAN SMD |
| 10 | 1 | L1 | 3.6 nH | Murata Electronics North America | LQP15MN3N6B02D | Inductor: 3.6 nH 0.1 nH 0402 |
| 11 | 2 | L2 L8 | 2.2 μ H | Murata Electronics North America | LQM2HPN2R2MG0L | Inductor: 2.2 μ H 20% 1300 mA 1008 |
| 12 | 1 | L3 | 1 μ H | Murata | LQM2HPN1R0MJ0L | Inductor, Power: 1.0 μ H 1500 mA 1007 |
| 16 | 1 | U1 | 8M (1M x 8) | Micron Technology Inc | M25PX80-VMN6TP | IC Flash: 8Mb 75 MHz 8SO |
| 17 | 1 | U2 | CC3200 | Texas Instruments | CC3200R1 | ARM M4 MCU with 802.11bgn WI-FI |
| 18 | 1 | Y1 | Crystal | Abracon Corporation | ABS07-32.768KHZ-T | Crystal: 32.768 kHz 12.5 pF SMD |
| 19 | 1 | Y2 | Crystal | Epson | Q24FA20H00396 | Crystal: 40 MHz 8 pF SMD |

NOTE

Use any 5% tolerance resistor 0402 or higher package.

6.1.2 Typical Application – CC3200 Preregulated 1.85-V Mode

Figure 6-2 shows the schematics for an application using the CC3200 preregulated 1.85-V mode.

Table 6-1 lists the bill of materials for an application using the CC3200 preregulated 1.85-V mode.

Table 6-2. Bill of Materials for CC3200 Preregulated 1.85-V Mode Application

| Item | Qty | Part Reference | Value | Manufacturer | Part Number | Description |
|------|-----|---|----------------|--|----------------------|--|
| 1 | 3 | C1 C2 C3 | 4.7 μ F | Samsung Electro-Mechanics America, Inc | CL05A475MQ5NRNC | Capacitor, Ceramic: 4.7 μ F 6.3 V 20% X5R 0402 |
| 2 | 12 | C4 C5 C8 C11 C12 C14 C17 C19 C20 C21 C22 C23 | 0.1 μ F | Taiyo Yuden | LMK105BJ104KV-F | Capacitor, Ceramic: 0.1 μ F 10 V 10% X5R 0402 |
| 3 | 1 | C9 | 1.0 pF | Murata Electronics North America | GJM1555C1H1R0BB01D | Capacitor, Ceramic: 1 pF 50 V NP0 0402 |
| 4 | 1 | C16 | 22 μ F | Taiyo Yuden | AMK107BBJ226MAHT | Capacitor, Ceramic: μ F 4 V 20% X5R 0603 |
| 5 | 2 | C13 C18 | 10 μ F | Murata Electronics North America | GRM188R60J106ME47D | Capacitor, Ceramic: 10 μ F 6.3 V 20% X5R 0603 |
| 6 | 2 | C24 C46 | 10 pF | Murata Electronics North America | GRM1555C1H100FA01D | Capacitor, Ceramic: 10 pF 50 V 1% NP0 0402 |
| 7 | 2 | C42 C49 | 6.2 pF | Murata Electronics North America | GRM1555C1H6R2BA01D | Capacitor, Ceramic: 6.2 pF 50 V NP0 0402 |
| 8 | 1 | E2 | 2.4-GHz Ant | Taiyo Yuden | AH316M245001-T | Antenna, Chip: 50 Ω Bluetooth WLAN ZigBee WIMAX |
| 9 | 1 | FL1 | 2.4-GHz Filter | TDK-Epcos | DEA202450BT-1294C1-H | Filter, Bandpass: 2.4 GHz WLAN SMD |
| 10 | 1 | L1 | 3.6 nH | Murata Electronics North America | LQP15MN3N6B02D | Inductor: 3.6 nH 0.1 nH 0402 |
| 11 | 1 | L8 | 2.2 μ H | Murata Electronics North America | LQM2HPN2R2MG0L | Inductor: 2.2 μ H 20% 1300 mA 1008 |
| 15 | 1 | U1 | 8M (1M x 8) | Winbond | W25Q80BWZPIG | IC FLASH 8Mb 75 MHz 8WSON |
| 16 | 1 | U2 | CC3200 | Texas Instruments | CC3200R1 | ARM M4 MCU with 802.11bgn WIFI |
| 17 | 1 | Y1 | Crystal | Abracon Corporation | ABS07-32.768KHZ-T | Crystal: 32.768 kHz 12.5 pF SMD |
| 18 | 1 | Y2 | Crystal | Epson | Q24FA20H00396 | Crystal: 40 MHz 8 pF SMD |

NOTE

Use any 5% tolerance resistor 0402 or higher package.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

The CC3200 evaluation board includes a set of tools and documentation to help the user during the development phase.

7.1.1.1 PinMux Tool

The CC3200 device uses pin multiplexing extensively to accommodate the large number of peripheral functions in the smallest possible package. The PinMux tool is a utility used to select the appropriate pin multiplexing configuration that meets the end application requirements. The PinMux tool makes it easy to understand the various pin multiplexing options and enables the best configuration to be chosen without error.

7.1.1.2 Radio Tool

The SimpleLink radio tool is a utility for operating and testing the CC3200 chipset designs during development of the application board. The CC3200 device has an auto-calibrated radio that enables easy connection to the antenna without requiring expertise in radio circuit design.

7.1.1.3 Uniflash Flash Programmer

The Uniflash flash programmer utility allows end users to communicate with the SimpleLink device to update the serial flash. The easy GUI interface enables flashing of files (including read-back verification option), storage format (secured and nonsecured formatting), version reading for boot loader and chip ID, and so on.

7.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3200 device and support tools (see [Figure 7-1](#)).

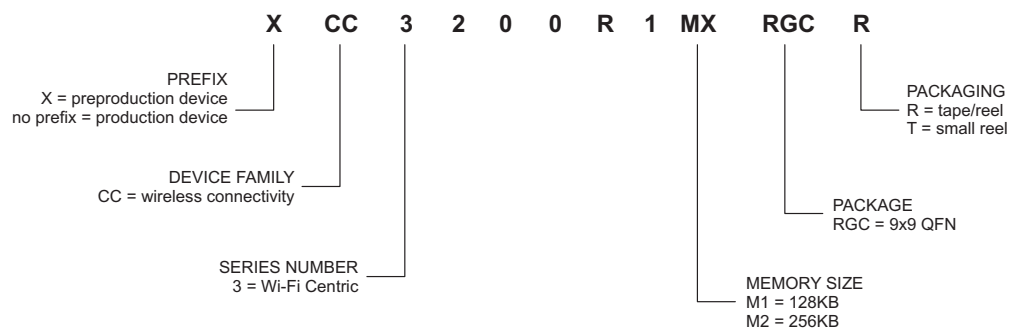


Figure 7-1. CC3200 Device Nomenclature

7.2 Documentation Support

The following documents provide support for the CC3200 device.

| | |
|-------------------------|--|
| SWRU372 | <i>CC3200 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad Getting Started Guide</i> |
| SWRU367 | <i>CC3200 SimpleLink Wi-Fi and IoT Solution With MCU Technical Reference Manual</i> |
| SWRU369 | <i>CC3200 SimpleLink Wi-Fi and IoT Solution With MCU Programmer's Guide</i> |
| SWRU370 | <i>CC3100 and CC3200 SimpleLink Wi-Fi and IoT Solution Layout Guidelines</i> |
| SWRC289 | <i>CC3200 SimpleLink Wi-Fi and IoT Solution With MCU LaunchPad Board Design Files</i> |

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.4 Trademarks

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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary




[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| CC3200R1M1RGCR | ACTIVE | VQFN | RGC | 64 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC3200R1 M1 |  |
| CC3200R1M2RGC | ACTIVE | VQFN | RGC | 64 | 260 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC3200R1 M2 |  |
| CC3200R1M2RGCR | ACTIVE | VQFN | RGC | 64 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC3200R1 M2 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

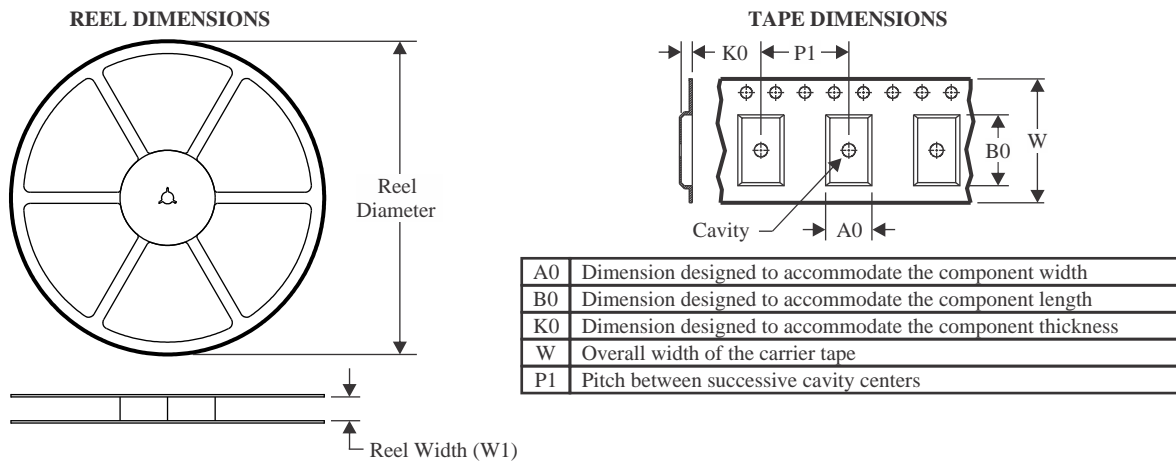
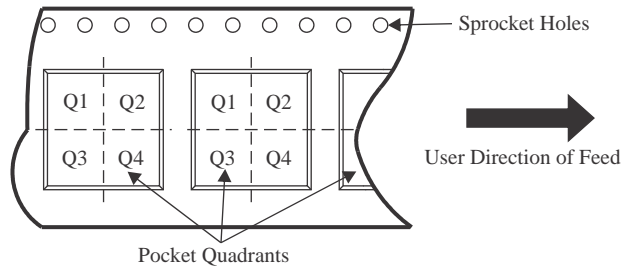
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

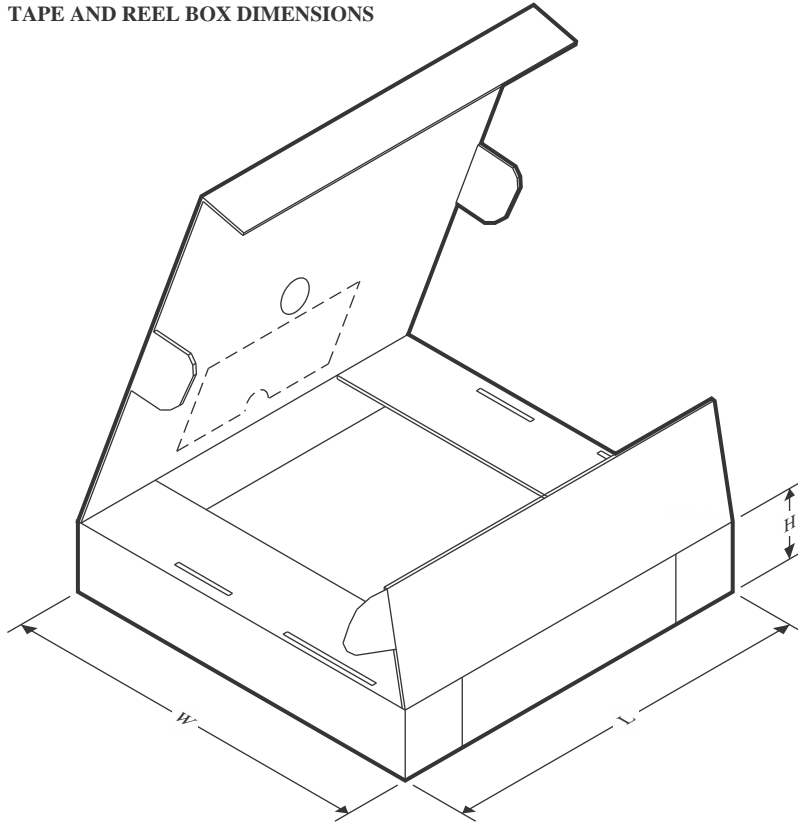
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

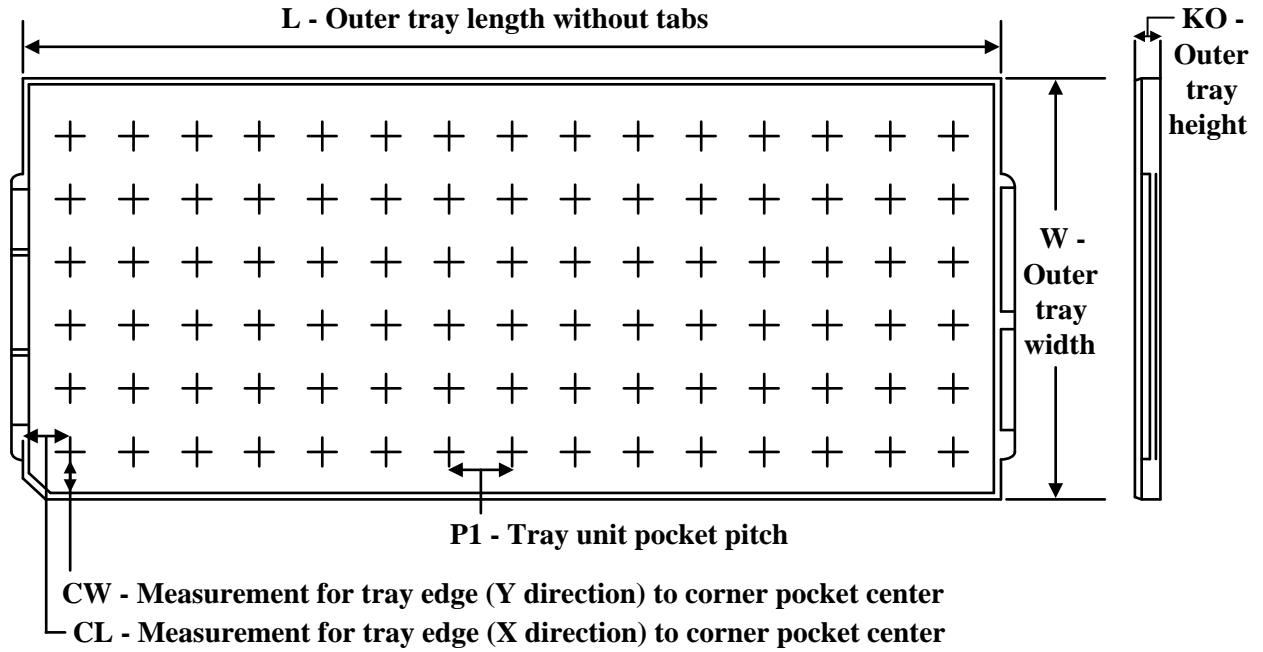
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC3200R1M1RGCR | VQFN | RGC | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC3200R1M2RGCR | VQFN | RGC | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC3200R1M1RGCR | VQFN | RGC | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| CC3200R1M2RGCR | VQFN | RGC | 64 | 2500 | 367.0 | 367.0 | 38.0 |

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| CC3200R1M2RGC | RGC | VQFN | 64 | 260 | 26 x 10 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |

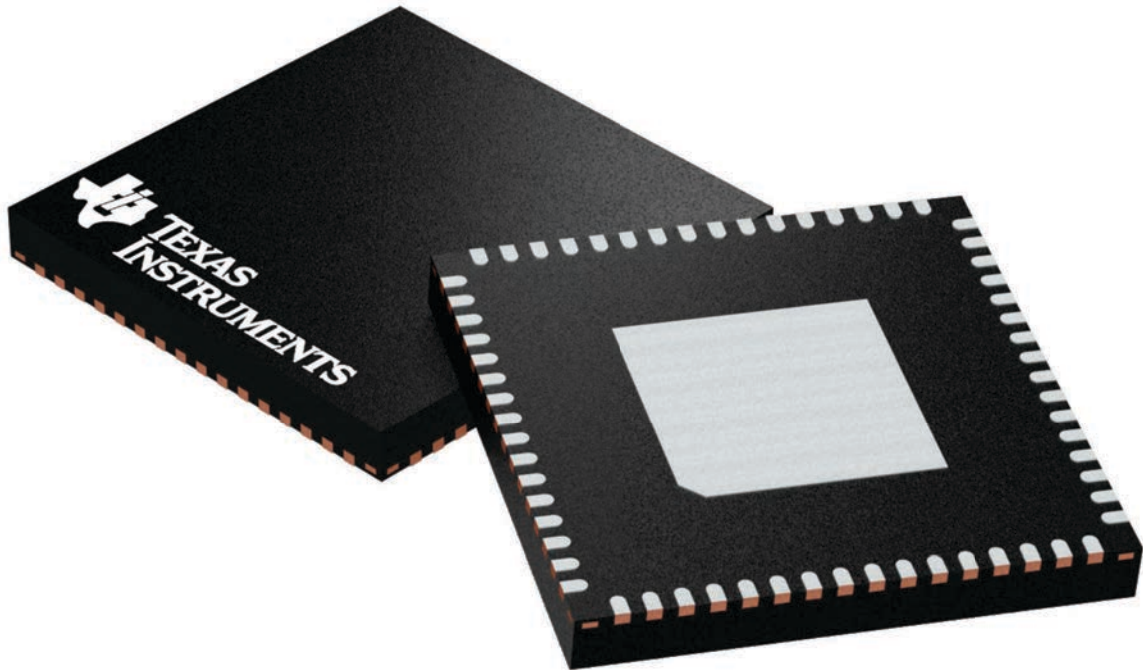
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

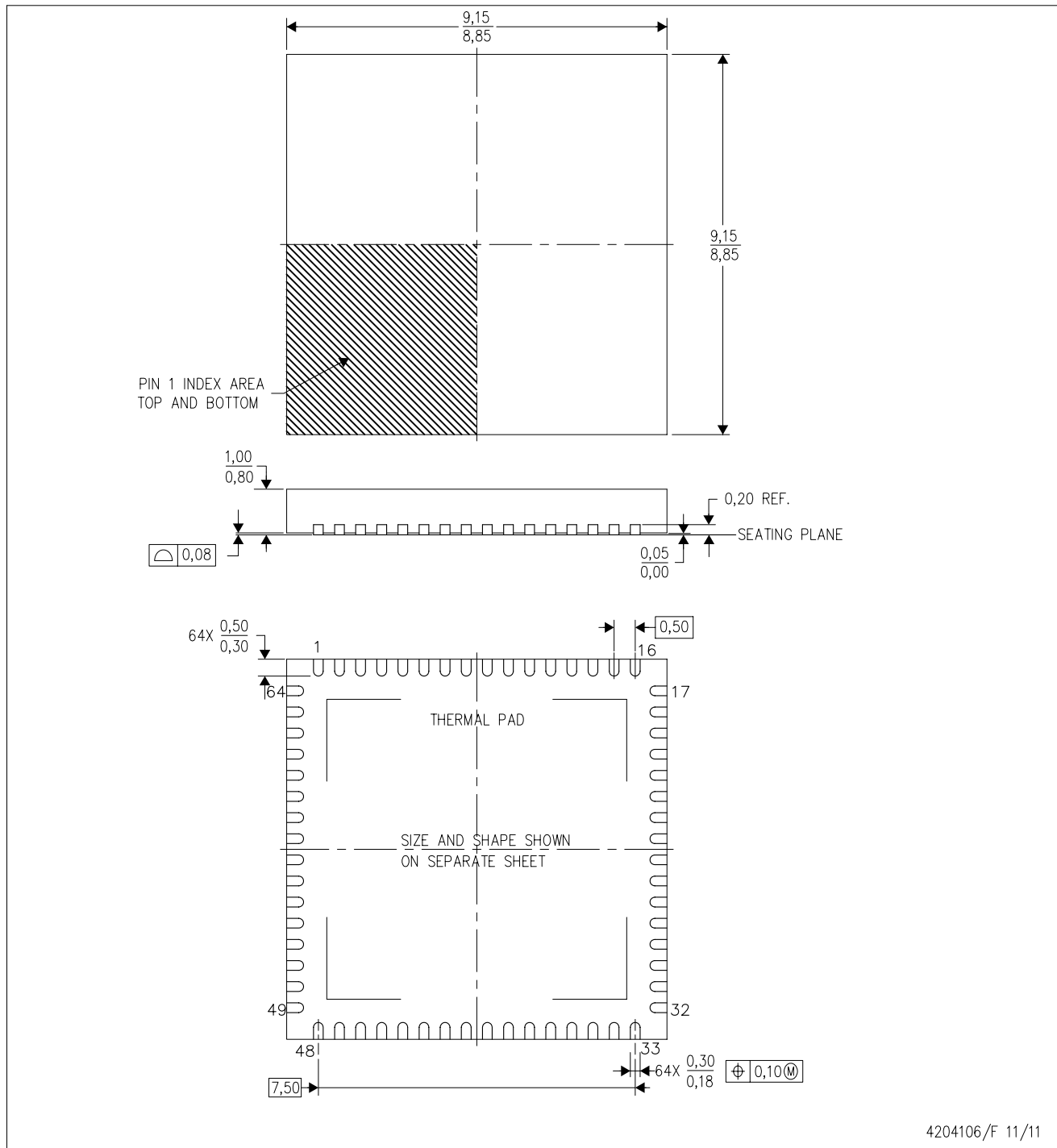


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

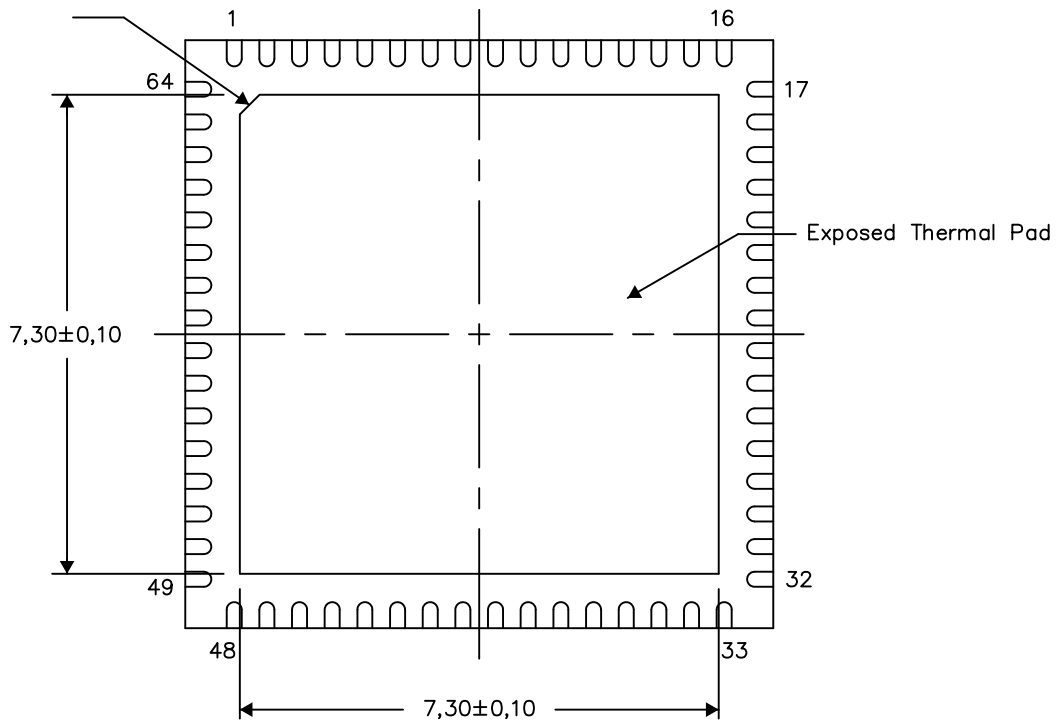
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
CO,30



Bottom View

Exposed Thermal Pad Dimensions

4206192-14/AE 03/15

NOTE: A. All linear dimensions are in millimeters

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