

A True System-on-Chip Solution for 2.4-GHz IEEE 802.15.4 and ZigBee Applications

Check for Samples: [CC2530F32](#), [CC2530F64](#), [CC2530F128](#), [CC2530F256](#)

FEATURES

- **RF/Layout**
 - 2.4-GHz IEEE 802.15.4 Compliant RF Transceiver
 - Excellent Receiver Sensitivity and Robustness to Interference
 - Programmable Output Power Up to 4.5 dBm
 - Very Few External Components
 - Only a Single Crystal Needed for Asynchronous Networks
 - 6-mm × 6-mm QFN40 Package
 - Suitable for Systems Targeting Compliance With Worldwide Radio-Frequency Regulations: ETSI EN 300 328 and EN 300 440 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T-66 (Japan)
- **Low Power**
 - Active-Mode RX (CPU Idle): 24 mA
 - Active Mode TX at 1 dBm (CPU Idle): 29 mA
 - Power Mode 1 (4 μs Wake-Up): 0.2 mA
 - Power Mode 2 (Sleep Timer Running): 1 μA
 - Power Mode 3 (External Interrupts): 0.4 μA
 - Wide Supply-Voltage Range (2 V–3.6 V)
- **Microcontroller**
 - High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch
 - 32-, 64-, 128-, or 256-KB In-System-Programmable Flash
 - 8-KB RAM With Retention in All Power Modes
 - Hardware Debug Support
- **Peripherals**
 - Powerful Five-Channel DMA
 - Integrated High-Performance Op-Amp and Ultralow-Power Comparator
- IEEE 802.15.4 MAC Timer, General-Purpose Timers (One 16-Bit, Two 8-Bit)
- IR Generation Circuitry
- 32-kHz Sleep Timer With Capture
- CSMA/CA Hardware Support
- Accurate Digital RSSI/LQI Support
- Battery Monitor and Temperature Sensor
- 12-Bit ADC With Eight Channels and Configurable Resolution
- AES Security Coprocessor
- Two Powerful USARTs With Support for Several Serial Protocols
- 21 General-Purpose I/O Pins (19 × 4 mA, 2 × 20 mA)
- Watchdog Timer
- **Development Tools**
 - CC2530 Development Kit
 - CC2530 ZigBee® Development Kit
 - CC2530 RemoTI™ Development Kit for RF4CE
 - SmartRF™ Software
 - Packet Sniffer
 - IAR Embedded Workbench™ Available

APPLICATIONS

- 2.4-GHz IEEE 802.15.4 Systems
- RF4CE Remote Control Systems (64-KB Flash and Higher)
- ZigBee Systems (256-KB Flash)
- Home/Building Automation
- Lighting Systems
- Industrial Control and Monitoring
- Low-Power Wireless Sensor Networks
- Consumer Electronics
- Health Care



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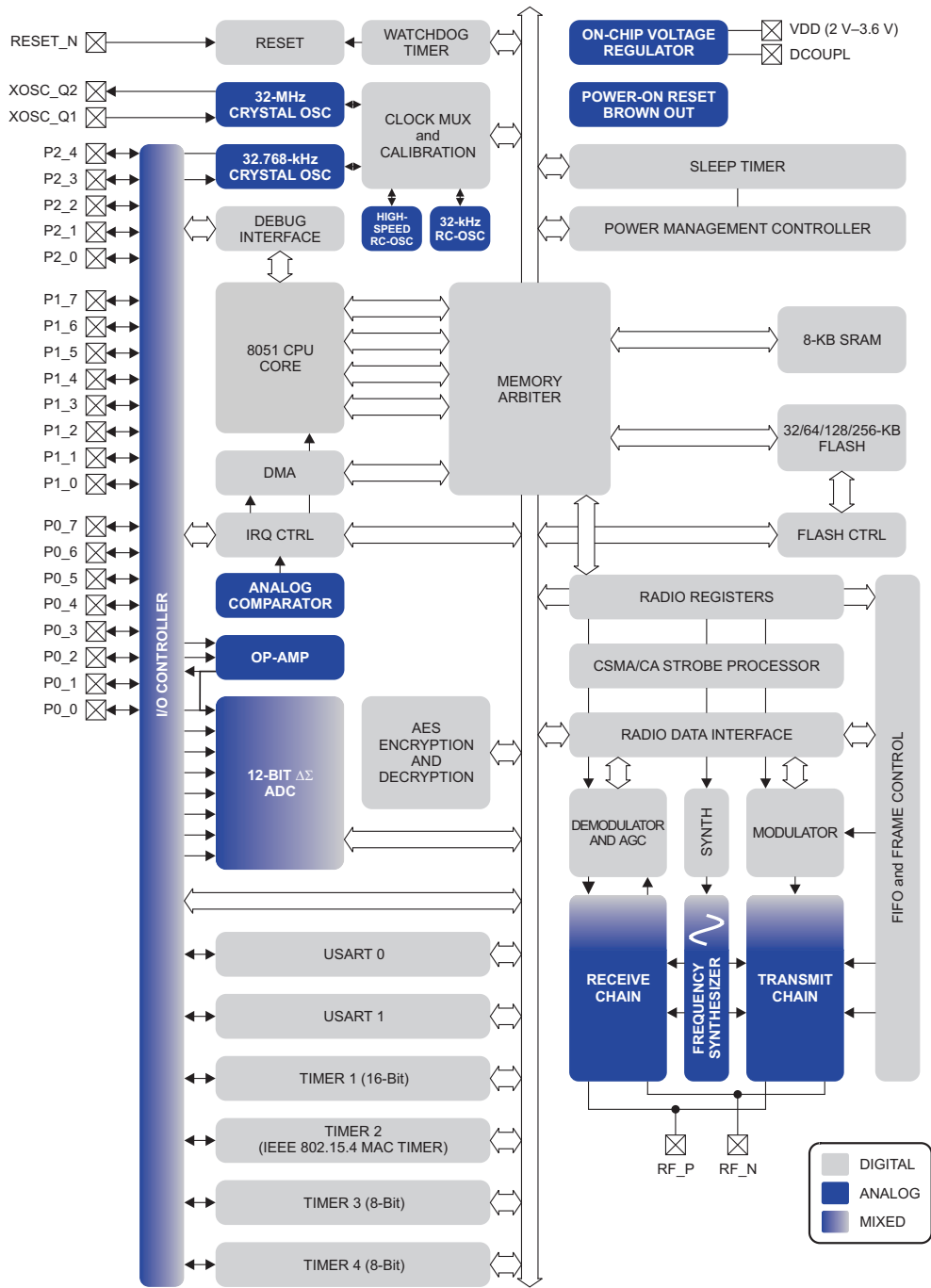
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DESCRIPTION

The CC2530 is a true system-on-chip (SoC) solution for IEEE 802.15.4, Zigbee and RF4CE applications. It enables robust network nodes to be built with very low total bill-of-material costs. The CC2530 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful features. The CC2530 comes in four different flash versions: CC2530F32/64/128/256, with 32/64/128/256 KB of flash memory, respectively. The CC2530 has various operating modes, making it highly suited for systems where ultralow power consumption is required. Short transition times between operating modes further ensure low energy consumption.

Combined with the industry-leading and golden-unit-status ZigBee protocol stack (Z-Stack™) from Texas Instruments, the CC2530F256 provides a robust and complete ZigBee solution.

Combined with the golden-unit-status RemoTI stack from Texas Instruments, the CC2530F64 and higher provide a robust and complete ZigBee RF4CE remote-control solution.



B0301-02



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|--|------|---------------------|------|
| Supply voltage | All supply pins must have the same voltage | -0.3 | 3.9 | V |
| Voltage on any digital pin | | -0.3 | VDD + 0.3, ≤ 3.9 | V |
| Input RF level | | | 10 | dBm |
| Storage temperature range | | -40 | 125 | °C |
| ESD ⁽²⁾ | All pads, according to human-body model, JEDEC STD 22, method A114 | | 2 | kV |
| | According to charged-device model, JEDEC STD 22, method C101 | | 500 | V |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) CAUTION: ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|--|-----|-----|------|
| Operating ambient temperature range, T _A | | -40 | 125 | °C |
| Operating supply voltage | | 2 | 3.6 | V |

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2530 EM reference design with T_A = 25°C and VDD = 3 V, unless otherwise noted. **Boldface** limits apply over the entire operating range, T_A = -40°C to 125°C, VDD = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---------------------------------|------|-------------|------|
| I _{core} Core current consumption | Digital regulator on. 16-MHz RCOSC running. No radio, crystals, or peripherals active. Medium CPU activity: normal flash access ⁽¹⁾ , no RAM access | | 3.4 | | mA |
| | 32-MHz XOSC running. No radio or peripherals active. Medium CPU activity: normal flash access ⁽¹⁾ , no RAM access | | 6.5 | 8.9 | mA |
| | 32-MHz XOSC running, radio in RX mode, -50-dBm input power, no peripherals active, CPU idle | | 20.5 | | mA |
| | 32-MHz XOSC running, radio in RX mode at -100-dBm input power (waiting for signal), no peripherals active, CPU idle | | 24.3 | 29.6 | mA |
| | 32-MHz XOSC running, radio in TX mode, 1-dBm output power, no peripherals active, CPU idle | | 28.7 | | mA |
| | 32-MHz XOSC running, radio in TX mode, 4.5-dBm output power, no peripherals active, CPU idle | | 33.5 | 39.6 | mA |
| | Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention | | 0.2 | 0.3 | mA |
| | Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention | | | 1 | 2 |
| Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention | | 0.4 | 1 | μA | |
| I _{peri} Peripheral Current Consumption (Adds to core current I _{core} for each peripheral unit activated) | Timer 1 | Timer running, 32-MHz XOSC used | | 90 | μA |
| | Timer 2 | Timer running, 32-MHz XOSC used | | 90 | μA |
| | Timer 3 | Timer running, 32-MHz XOSC used | | 60 | μA |
| | Timer 4 | Timer running, 32-MHz XOSC used | | 70 | μA |
| | Sleep timer | Including 32.753-kHz RCOSC | | 0.6 | μA |
| | ADC | When converting | | 1.2 | mA |
| | Flash | Erase | | 1 | mA |
| | | Burst write peak current | | 6 | mA |

- (1) Normal flash access means that the code used exceeds the cache storage, so cache misses happen frequently.

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2530 EM reference design with T_A = 25°C and VDD = 3 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-----------------|-----|-----|-----|------|
| WAKE-UP AND TIMING | | | | | |

GENERAL CHARACTERISTICS (continued)

 Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|------|-----|------|----------|
| Power mode 1 → active | Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC | | 4 | | μs |
| Power mode 2 or 3 → active | Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC | | 0.1 | | ms |
| Active → TX or RX | Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF | | 0.5 | | ms |
| | With 32-MHz XOSC initially on | | | 192 | μs |
| RX/TX and TX/RX turnaround | | | | 192 | μs |
| RADIO PART | | | | | |
| RF frequency range | Programmable in 1-MHz steps, 5 MHz between channels for compliance with [1] | 2394 | | 2507 | MHz |
| Radio baud rate | As defined by [1] | | 250 | | kbps |
| Radio chip rate | As defined by [1] | | 2 | | MChip/s |
| Flash erase cycles | | | | 20 | k cycles |
| Flash page size | | | 2 | | KB |

RF RECEIVE SECTION

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, and $f_c = 2440\text{ MHz}$, unless otherwise noted.

Boldface limits apply over the entire operating range, $T_A = -40^\circ\text{C}$ to 125°C , $V_{DD} = 2\text{ V}$ to 3.6 V , and $f_c = 2394\text{ MHz}$ to 2507 MHz .

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|--|-------------------|------|
| Receiver sensitivity | PER = 1%, as specified by [1] [1] requires -85 dBm | | -97 | -92 -88 | dBm |
| Saturation (maximum input level) | PER = 1%, as specified by [1] [1] requires -20 dBm | | 10 | | dBm |
| Adjacent-channel rejection, 5-MHz channel spacing | Wanted signal -82 dBm, adjacent modulated channel at 5 MHz, PER = 1 %, as specified by [1]. [1] requires 0 dB | | 49 | | dB |
| Adjacent-channel rejection, -5-MHz channel spacing | Wanted signal -82 dBm, adjacent modulated channel at -5 MHz, PER = 1 %, as specified by [1]. [1] requires 0 dB | | 49 | | dB |
| Alternate-channel rejection, 10-MHz channel spacing | Wanted signal -82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1] [1] requires 30 dB | | 57 | | dB |
| Alternate-channel rejection, -10-MHz channel spacing | Wanted signal -82 dBm, adjacent modulated channel at -10 MHz, PER = 1 %, as specified by [1] [1] requires 30 dB | | 57 | | dB |
| Channel rejection $\geq 20\text{ MHz}$ $\leq -20\text{ MHz}$ | Wanted signal at -82 dBm. Undesired signal is an IEEE 802.15.4 modulated channel, stepped through all channels from 2405 to 2480 MHz. Signal level for PER = 1%. | | 57 57 | | dB |
| Co-channel rejection | Wanted signal at -82 dBm. Undesired signal is 802.15.4 modulated at the same frequency as the desired signal. Signal level for PER = 1%. | | -3 | | dB |
| Blocking/desensitization 5 MHz from band edge 10 MHz from band edge 20 MHz from band edge 50 MHz from band edge -5 MHz from band edge -10 MHz from band edge -20 MHz from band edge -50 MHz from band edge | Wanted signal 3 dB above the sensitivity level, CW jammer, PER = 1%. Measured according to EN 300 440 class 2. | | -33 -33 -32 -31 -35 -35 -34 -34 | | dBm |
| Spurious emission. Only largest spurious emission stated within each band. 30 MHz–1000 MHz 1 GHz–12.75 GHz | Conducted measurement with a 50- Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T-66. | | < -80 -57 | | dBm |
| Frequency error tolerance ⁽¹⁾ | [1] requires minimum 80 ppm | | ± 150 | | ppm |
| Symbol rate error tolerance ⁽²⁾ | [1] requires minimum 80 ppm | | ± 1000 | | ppm |

(1) Difference between center frequency of the received RF signal and local oscillator frequency.

(2) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$, unless otherwise noted.

Boldface limits apply over the entire operating range, $T_A = -40^\circ\text{C}$ to 125°C , $V_{DD} = 2\text{ V}$ to 3.6 V and $f_c = 2394\text{ MHz}$ to 2507 MHz .

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|----------------|---|----------------|------|
| Nominal output power | Delivered to a single-ended 50-Ω load through a balun using maximum-recommended output-power setting [1] requires minimum -3 dBm | 0 -8 | 4.5 | 8 10 | dBm |
| Programmable output power range | | | 32 | | dB |
| Spurious emissions Measured conducted according to stated regulations. Only largest spurious emission stated within each band. | Max recommended output power setting ⁽¹⁾ 25 MHz–1000 MHz (outside restricted bands) 25 MHz–2400 MHz (within FCC restricted bands) 25 MHz–1000 MHz (within ETSI restricted bands) 1800–1900 MHz (ETSI restricted band) 5150–5300 MHz (ETSI restricted band) At $2 \times f_c$ and $3 \times f_c$ (FCC restricted band) At $2 \times f_c$ and $3 \times f_c$ (ETSI EN 300-440 and EN 300-328) ⁽²⁾ 1 GHz–12.75 GHz (outside restricted bands) At 2483.5 MHz and above (FCC restricted band) $f_c = 2480\text{ MHz}$ ⁽³⁾ | | -60 -60 -60 -57 -55 -42 -31 -53 -42 | | dBm |
| Error vector magnitude (EVM) | Measured as defined by [1] using maximum-recommended output-power setting [1] requires maximum 35%. | | 2% | | |
| Optimum load impedance | Differential impedance as seen from the RF port (RF_P and RF_N) towards the antenna | | 69 + j29 | | Ω |

- (1) Texas Instruments CC2530 EM reference design is suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T-66.
- (2) Margins for passing conducted requirements at the third harmonic can be improved by using a simple band-pass filter connected between matching network and RF connector (1.8 pF in parallel with 1.6 nH); this filter must be connected to a good RF ground.
- (3) Margins for passing FCC requirements at 2483.5 MHz and above when transmitting at 2480 MHz can be improved by using a lower output-power setting or having less than 100% duty cycle.

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|----------|
| Crystal frequency | | | 32 | | MHz |
| Crystal frequency accuracy requirement ⁽¹⁾ | | -40 | | 40 | ppm |
| ESR Equivalent series resistance | | 6 | | 60 | Ω |
| C_0 Crystal shunt capacitance | | 1 | | 7 | pF |
| C_L Crystal load capacitance | | 10 | | 16 | pF |
| Start-up time | | | 0.3 | | ms |
| Power-down guard time | The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load. | 3 | | | ms |

(1) Including aging and temperature dependency, as specified by [1]

32.768-kHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|--------|-----|------------|
| Crystal frequency | | | 32.768 | | kHz |
| Crystal frequency accuracy requirement ⁽¹⁾ | | -40 | | 40 | ppm |
| ESR Equivalent series resistance | | | 40 | 130 | k Ω |
| C_0 Crystal shunt capacitance | | | 0.9 | 2 | pF |
| C_L Crystal load capacitance | | | 12 | 16 | pF |
| Start-up time | | | 0.4 | | s |

(1) Including aging and temperature dependency, as specified by [1]

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-------------|-----|---------------------|
| Calibrated frequency ⁽¹⁾ | | | 32.753 | | kHz |
| Frequency accuracy after calibration | | | $\pm 0.2\%$ | | |
| Temperature coefficient ⁽²⁾ | | | 0.4 | | $\%/^\circ\text{C}$ |
| Supply-voltage coefficient ⁽³⁾ | | | 3 | | $\%/V$ |
| Calibration time ⁽⁴⁾ | | | 2 | | ms |

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.

(2) Frequency drift when temperature changes after calibration

(3) Frequency drift when supply voltage changes after calibration

(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEPCMD.OSC32K_CALDIS is 0.

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-------|-----|------|
| Frequency ⁽¹⁾ | | | 16 | | MHz |
| Uncalibrated frequency accuracy | | | ±18% | | |
| Calibrated frequency accuracy | | | ±0.6% | ±1% | |
| Start-up time | | | | 10 | µs |
| Initial calibration time ⁽²⁾ | | | 50 | | µs |

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.

(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEP_CMD.OSC_PD is set to 0.

RSSI/CCA CHARACTERISTICS

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| RSSI range | | | 100 | | dB |
| Absolute uncalibrated RSSI/CCA accuracy | | | ±4 | | dB |
| RSSI/CCA offset ⁽¹⁾ | | | 73 | | dB |
| Step size (LSB value) | | | 1 | | dB |

(1) Real RSSI = Register value – offset

FREQEST CHARACTERISTICS

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------|-----|------|-----|------|
| FREQEST range | | | ±250 | | kHz |
| FREQEST accuracy | | | ±40 | | kHz |
| FREQEST offset ⁽¹⁾ | | | 20 | | kHz |
| Step size (LSB value) | | | 7.8 | | kHz |

(1) Real FREQEST = Register value – offset

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-------------------------------|-----|------|-----|--------|
| Phase noise, unmodulated carrier | At ±1-MHz offset from carrier | | -110 | | dBc/Hz |
| | At ±2-MHz offset from carrier | | -117 | | |
| | At ±5-MHz offset from carrier | | -122 | | |

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|---|-----|------|-----|------------|----|
| Output at 25°C | Measured using integrated ADC using internal bandgap voltage reference and maximum resolution | | 1480 | | 12-bit ADC | |
| Temperature coefficient | | | 4.5 | | /1°C | |
| Voltage coefficient | | | 1 | | /0.1 V | |
| Initial accuracy without calibration | | | | ±10 | | °C |
| Accuracy using 1-point calibration (entire temperature range) | | | | ±5 | | °C |
| Current consumption when enabled (ADC current not included) | | | | 0.5 | | mA |

OP-AMP CHARACTERISTICS

T_A = 25°C, VDD = 3 V. All measurement results are obtained using the CC2530 reference designs post-calibration.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------|-----|------------|-----|----------|
| Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x03, OPAMPC = 0x01 | | | | | |
| Output maximum voltage | | | VDD – 0.07 | | V |
| Output minimum voltage | | | 0.07 | | V |
| Open-loop gain | | | 108 | | dB |
| Gain-bandwidth product | | | 2 | | MHz |
| Slew rate | | | 107 | | V/μs |
| Input maximum voltage | | | VDD + 0.13 | | V |
| Input minimum voltage | | | –55 | | mV |
| Input offset voltage | | | 40 | | μV |
| CMRR Common-mode rejection ratio | | | 90 | | dB |
| Supply current | | | 0.4 | | mA |
| Input noise voltage | f = 0.01 Hz to 1 Hz | | 1.1 | | nV/√(Hz) |
| | f = 0.1 Hz to 10 Hz | | 1.7 | | |
| Non-Chopping Configuration, Register APCFG = 0x07, OPAMPMC = 0x00, OPAMPC = 0x01 | | | | | |
| Output maximum voltage | | | VDD – 0.07 | | V |
| Output minimum voltage | | | 0.07 | | V |
| Open-loop gain | | | 108 | | dB |
| Gain-bandwidth product | | | 2 | | MHz |
| Slew rate | | | 107 | | V/μs |
| Input maximum voltage | | | VDD + 0.13 | | V |
| Input minimum voltage | | | –55 | | mV |
| Input offset voltage | | | 0.8 | | mV |
| CMRR Common-mode rejection ratio | | | 90 | | dB |
| Supply current | | | 0.4 | | mA |
| Input noise voltage | f = 0.01 Hz to 1 Hz | | 60 | | nV/√(Hz) |
| | f = 0.1 Hz to 10 Hz | | 65 | | |

COMPARATOR CHARACTERISTICS

T_A = 25°C, VDD = 3 V. All measurement results are obtained using the CC2530 reference designs, post-calibration.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------|-----|------|-----|-------|
| Common-mode maximum voltage | | | VDD | | V |
| Common-mode minimum voltage | | | –0.3 | | |
| Input offset voltage | | | 1 | | mV |
| Offset vs temperature | | | 16 | | μV/°C |
| Offset vs operating voltage | | | 4 | | mV/V |
| Supply current | | | 230 | | nA |
| Hysteresis | | | 0.15 | | mV |

ADC CHARACTERISTICS

T_A = 25°C and VDD = 3 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--|--|-----|-------|-----|---------|
| | Input voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | External reference voltage differential | VDD is voltage on AVDD5 pin | 0 | | VDD | V |
| | Input resistance, signal | Using 4-MHz clock speed | | 197 | | kΩ |
| | Full-scale signal ⁽¹⁾ | Peak-to-peak, defines 0 dBFS | | 2.97 | | V |
| ENOB ⁽¹⁾ | Effective number of bits | Single-ended input, 7-bit setting | | 5.7 | | bits |
| | | Single-ended input, 9-bit setting | | 7.5 | | |
| | | Single-ended input, 10-bit setting | | 9.3 | | |
| | | Single-ended input, 12-bit setting | | 10.8 | | |
| | | Differential input, 7-bit setting | | 6.5 | | |
| | | Differential input, 9-bit setting | | 8.3 | | |
| | | Differential input, 10-bit setting | | 10.0 | | |
| | | Differential input, 12-bit setting | | 11.5 | | |
| | Useful power bandwidth | 7-bit setting, both single and differential | | 0–20 | | kHz |
| THD ⁽¹⁾ | Total harmonic distortion | Single-ended input, 12-bit setting, –6 dBFS | | –75.2 | | dB |
| | | Differential input, 12-bit setting, –6 dBFS | | –86.6 | | |
| | Signal to nonharmonic ratio ⁽¹⁾ | Single-ended input, 12-bit setting | | 70.2 | | dB |
| | | Differential input, 12-bit setting | | 79.3 | | |
| | | Single-ended input, 12-bit setting, –6 dBFS | | 78.8 | | |
| | | Differential input, 12-bit setting, –6 dBFS | | 88.9 | | |
| CMRR | Common-mode rejection ratio | Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Crosstalk | Single-ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution | | >84 | | dB |
| | Offset | Midscale | | –3 | | mV |
| | Gain error | | | 0.68 | | % |
| DNL ⁽¹⁾ | Differential nonlinearity | 12-bit setting, mean | | 0.05 | | LSB |
| | | 12-bit setting, maximum | | 0.9 | | |
| INL ⁽¹⁾ | Integral nonlinearity | 12-bit setting, mean | | 4.6 | | LSB |
| | | 12-bit setting, maximum | | 13.3 | | |
| SINAD ⁽¹⁾ (–THD+N) | Signal-to-noise-and-distortion | Single-ended input, 7-bit setting | | 35.4 | | dB |
| | | Single-ended input, 9-bit setting | | 46.8 | | |
| | | Single-ended input, 10-bit setting | | 57.5 | | |
| | | Single-ended input, 12-bit setting | | 66.6 | | |
| | | Differential input, 7-bit setting | | 40.7 | | |
| | | Differential input, 9-bit setting | | 51.6 | | |
| | | Differential input, 10-bit setting | | 61.8 | | |
| | | Differential input, 12-bit setting | | 70.8 | | |
| | Conversion time | 7-bit setting | | 20 | | μs |
| | | 9-bit setting | | 36 | | |
| | | 10-bit setting | | 68 | | |
| | | 12-bit setting | | 132 | | |
| | Power consumption | | | 1.2 | | mA |
| | Internal reference voltage | | | 1.15 | | V |
| | Internal reference VDD coefficient | | | 4 | | mV/V |
| | Internal reference temperature coefficient | | | 0.4 | | mV/10°C |

(1) Measured with 300-Hz sine-wave input and VDD as reference.

CONTROL INPUT AC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 125°C , $V_{DD} = 2\text{ V}$ to 3.6 V , unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|---------------|
| System clock, f_{SYSCLK} $t_{\text{SYSCLK}} = 1/f_{\text{SYSCLK}}$ | The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used. | 16 | | 32 | MHz |
| RESET_N low duration | See item 1, Figure 1 . This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but might not lead to complete reset of all modules within the chip. | 1 | | | μs |
| Interrupt pulse duration | See item 2, Figure 1 . This is the shortest pulse that is recognized as an interrupt request. | 20 | | | ns |

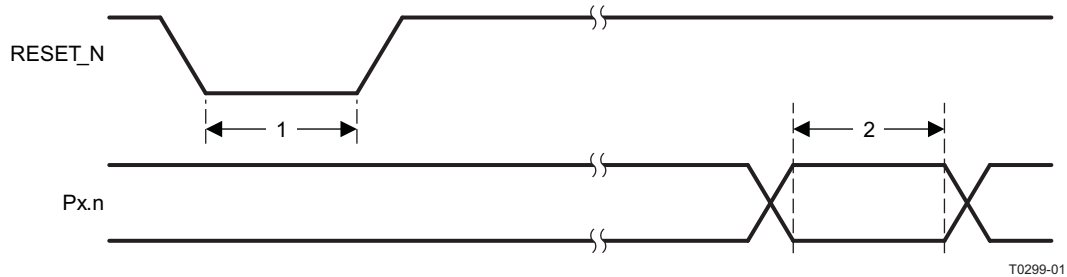
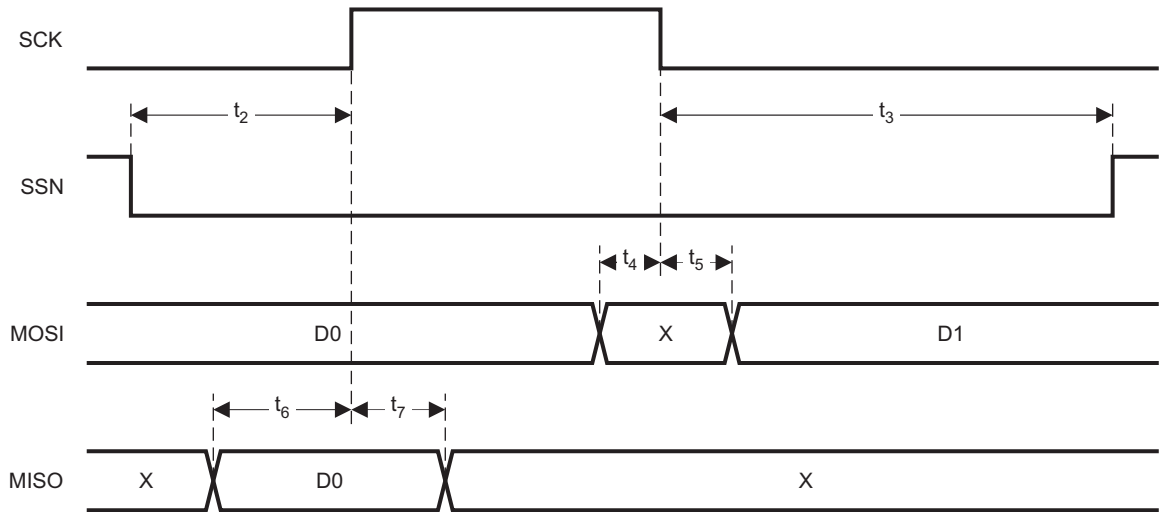


Figure 1. Control Input AC Characteristics

SPI AC CHARACTERISTICS

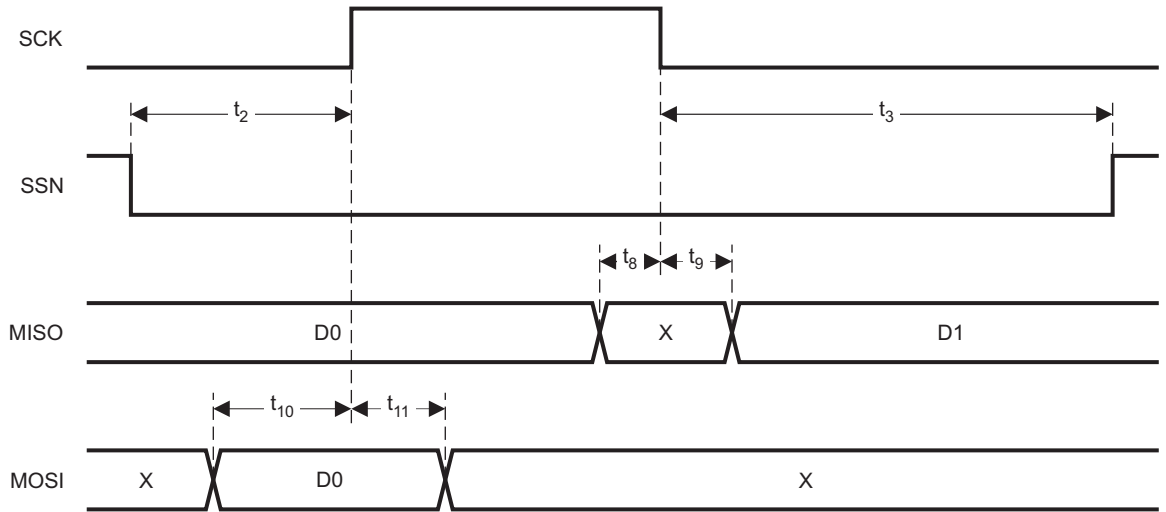
T_A = -40°C to 125°C, VDD = 2 V to 3.6 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------|-----|-----|-----|------|
| t ₁ SCK period | Master, RX and TX | 250 | | | ns |
| | Slave, RX and TX | 250 | | | |
| SCK duty cycle | Master | | 50% | | |
| t ₂ SSN low to SCK | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₃ SCK to SSN high | Master | 63 | | | ns |
| | Slave | 63 | | | |
| t ₄ MOSI early out | Master, load = 10 pF | | | 7 | ns |
| t ₅ MOSI late out | Master, load = 10 pF | | | 10 | ns |
| t ₆ MISO setup | Master | 90 | | | ns |
| t ₇ MISO hold | Master | 10 | | | ns |
| SCK duty cycle | Slave | | 50% | | ns |
| t ₁₀ MOSI setup | Slave | 35 | | | ns |
| t ₁₁ MOSI hold | Slave | 10 | | | ns |
| t ₉ MISO late out | Slave, load = 10 pF | | | 95 | ns |
| Operating frequency | Master, TX only | | | 8 | MHz |
| | Master, RX and TX | | | 4 | |
| | Slave, RX only | | | 8 | |
| | Slave, RX and TX | | | 4 | |



T0478-01

Figure 2. SPI Master AC Characteristics



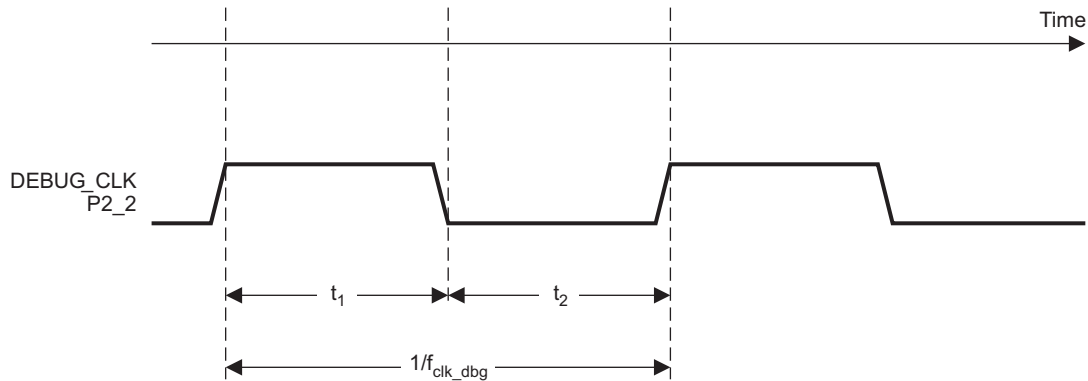
T0479-01

Figure 3. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

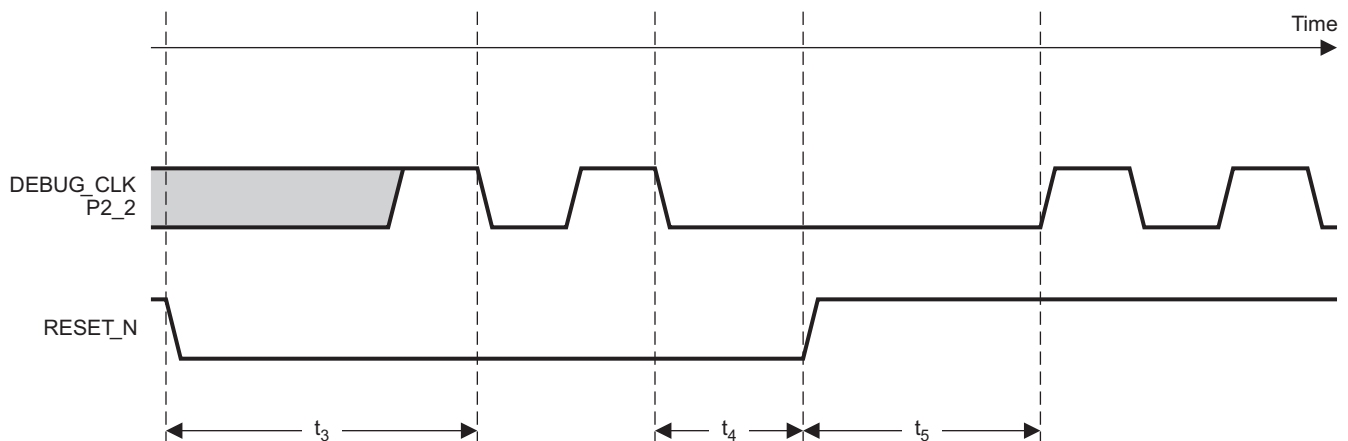
T_A = -40°C to 125°C, VDD = 2 V to 3.6 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|------|
| f _{clk_dbg} Debug clock frequency (see Figure 4) | | | | 12 | MHz |
| t ₁ Allowed high pulse on clock (see Figure 4) | | 35 | | | ns |
| t ₂ Allowed low pulse on clock (see Figure 4) | | 35 | | | ns |
| t ₃ EXT_RESET_N low to first falling edge on debug clock (see Figure 5) | | 167 | | | ns |
| t ₄ Falling edge on clock to EXT_RESET_N high (see Figure 5) | | 83 | | | ns |
| t ₅ EXT_RESET_N high to first debug command (see Figure 5) | | 83 | | | ns |
| t ₆ Debug data setup (see Figure 6) | | 2 | | | ns |
| t ₇ Debug data hold (see Figure 6) | | 4 | | | ns |
| t ₈ Clock-to-data delay (see Figure 6) | Load = 10 pF | | | 30 | ns |



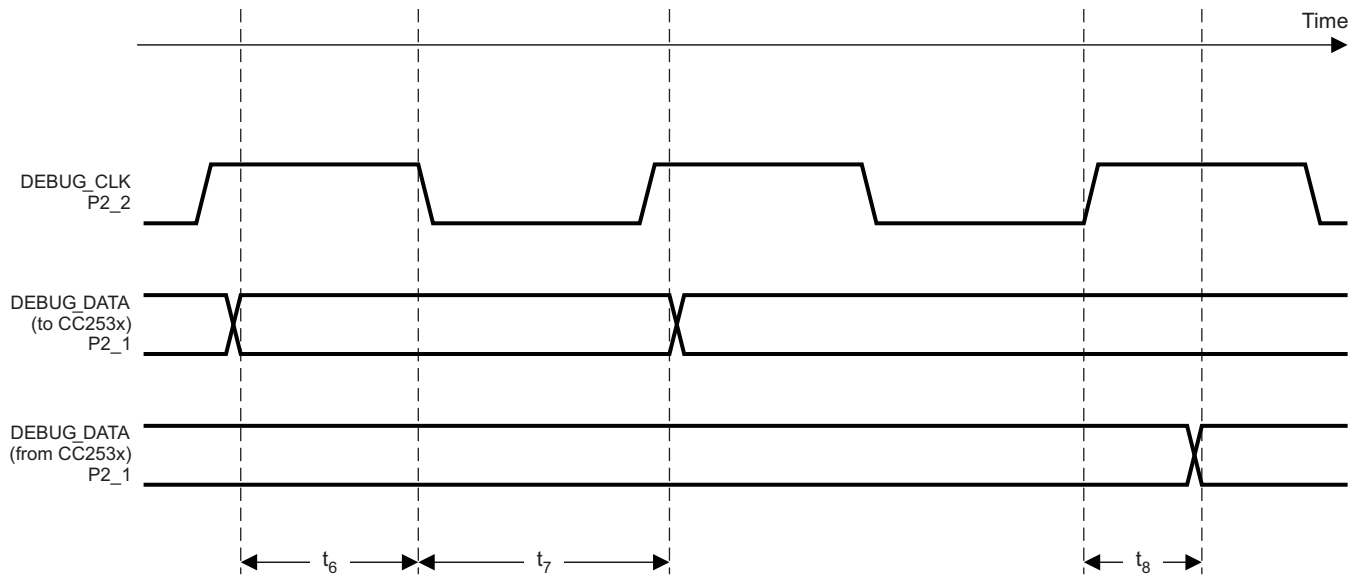
T0436-01

Figure 4. Debug Clock – Basic Timing



T0437-01

Figure 5. Data Setup and Hold Timing



T0438-01

Figure 6. Debug Enable Timing

TIMER INPUTS AC CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to 125°C , $V_{DD} = 2\text{ V}$ to 3.6 V , unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---|-----|-----|-----|---------------------|
| Input capture pulse duration | Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate (16 or 32 MHz). | 1.5 | | | t_{SYSCLK} |

DC CHARACTERISTICS

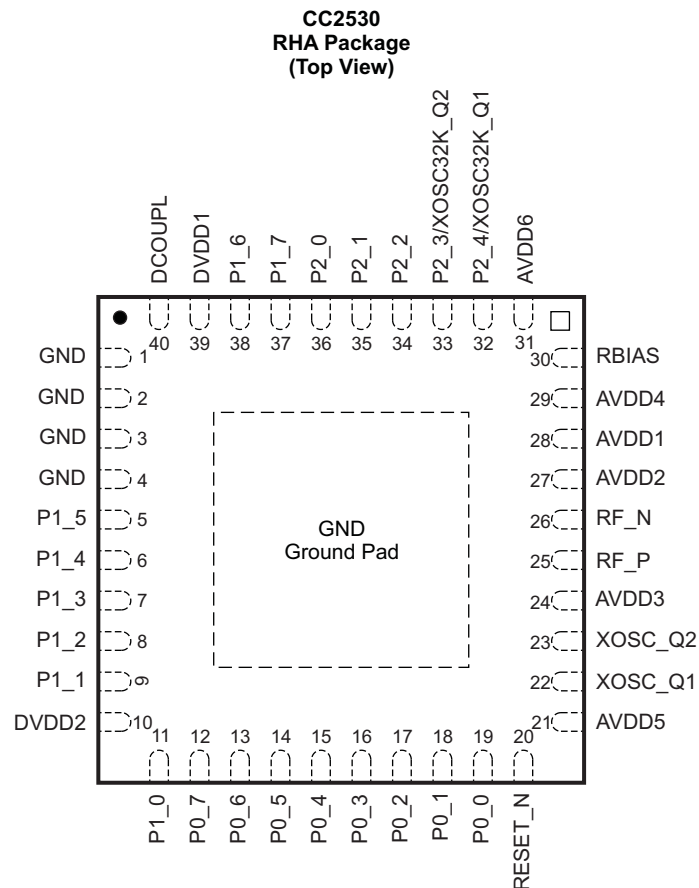
T_A = 25°C, VDD = 3 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|-------------------|-----|-----|-----|------|
| Logic-0 input voltage | | | | 0.5 | V |
| Logic-1 input voltage | | 2.5 | | | V |
| Logic-0 input current | Input equals 0 V | -50 | | 50 | nA |
| Logic-1 input current | Input equals VDD | -50 | | 50 | nA |
| I/O-pin pullup and pulldown resistors | | | 20 | | kΩ |
| Logic-0 output voltage, 4-mA pins | Output load 4 mA | | | 0.5 | V |
| Logic-1 output voltage, 4-mA pins | Output load 4 mA | 2.4 | | | V |
| Logic-0 output voltage, 20-mA pins | Output load 20 mA | | | 0.5 | V |
| Logic-1 output voltage, 20-mA pins | Output load 20 mA | 2.4 | | | V |

DEVICE INFORMATION

PIN DESCRIPTIONS

The CC2530 pinout is shown in Figure 7 and a short description of the pins follows.



P0076-02

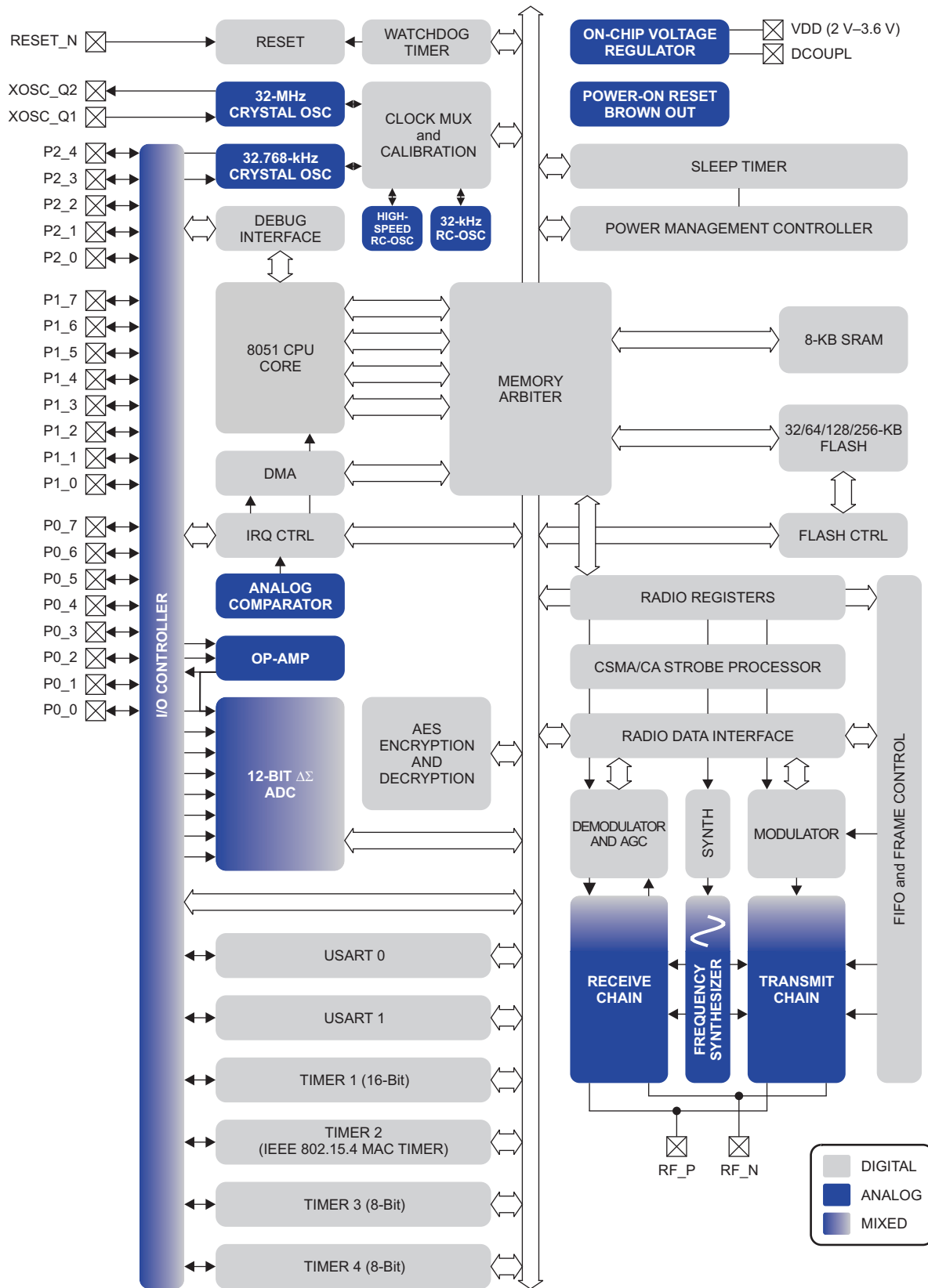
NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 7. Pinout Top View

Table 1. Pin Descriptions

| PIN NAME | PIN | PIN TYPE | DESCRIPTION |
|---------------------|------------|----------------------------|--|
| AVDD1 | 28 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD2 | 27 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD3 | 24 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD4 | 29 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD5 | 21 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| AVDD6 | 31 | Power (analog) | 2-V–3.6-V analog power-supply connection |
| DCOUPPL | 40 | Power (digital) | 1.8-V digital power-supply decoupling. Do not use for supplying external circuits. |
| DVDD1 | 39 | Power (digital) | 2-V–3.6-V digital power-supply connection |
| DVDD2 | 10 | Power (digital) | 2-V–3.6-V digital power-supply connection |
| GND | — | Ground | The ground pad must be connected to a solid ground plane. |
| GND | 1, 2, 3, 4 | Unused pins | Connect to GND |
| P0_0 | 19 | Digital I/O | Port 0.0 |
| P0_1 | 18 | Digital I/O | Port 0.1 |
| P0_2 | 17 | Digital I/O | Port 0.2 |
| P0_3 | 16 | Digital I/O | Port 0.3 |
| P0_4 | 15 | Digital I/O | Port 0.4 |
| P0_5 | 14 | Digital I/O | Port 0.5 |
| P0_6 | 13 | Digital I/O | Port 0.6 |
| P0_7 | 12 | Digital I/O | Port 0.7 |
| P1_0 | 11 | Digital I/O | Port 1.0 – 20-mA drive capability |
| P1_1 | 9 | Digital I/O | Port 1.1 – 20-mA drive capability |
| P1_2 | 8 | Digital I/O | Port 1.2 |
| P1_3 | 7 | Digital I/O | Port 1.3 |
| P1_4 | 6 | Digital I/O | Port 1.4 |
| P1_5 | 5 | Digital I/O | Port 1.5 |
| P1_6 | 38 | Digital I/O | Port 1.6 |
| P1_7 | 37 | Digital I/O | Port 1.7 |
| P2_0 | 36 | Digital I/O | Port 2.0 |
| P2_1 | 35 | Digital I/O | Port 2.1 |
| P2_2 | 34 | Digital I/O | Port 2.2 |
| P2_3/ XOSC32K_Q2 | 33 | Digital I/O, Analog I/O | Port 2.3/32.768 kHz XOSC |
| P2_4/ XOSC32K_Q1 | 32 | Digital I/O, Analog I/O | Port 2.4/32.768 kHz XOSC |
| RBIAS | 30 | Analog I/O | External precision bias resistor for reference current |
| RESET_N | 20 | Digital input | Reset, active-low |
| RF_N | 26 | RF I/O | Negative RF input signal to LNA during RX Negative RF output signal from PA during TX |
| RF_P | 25 | RF I/O | Positive RF input signal to LNA during RX Positive RF output signal from PA during TX |
| XOSC_Q1 | 22 | Analog I/O | 32-MHz crystal oscillator pin 1 or external-clock input |
| XOSC_Q2 | 23 | Analog I/O | 32-MHz crystal oscillator pin 2 |

CIRCUIT DESCRIPTION



B0301-02

Figure 8. CC2530 Block Diagram

A block diagram of the CC2530 is shown in [Figure 8](#). The modules can be roughly divided into one of three categories: CPU- and memory-related modules; modules related to peripherals, clocks, and power management; and radio-related modules. In the following subsections, a short description of each module that appears in [Figure 8](#) is given.

For more details about the modules and their usage, see the corresponding chapters in the CC253x User's Guide ([SWRU191](#)).

CPU and Memory

The **8051 CPU** core used in the CC253x device family is a single-cycle 8051-compatible core. It has three different memory-access buses (SFR, DATA and CODE/XDATA) with single-cycle access to SFR, DATA, and the main SRAM. It also includes a debug interface and an 18-input extended interrupt unit.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. Any interrupt service request is serviced also when the device is in idle mode by going back to active mode. Some interrupts can also wake up the device from sleep mode (power modes 1–3).

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory access points, access of which can map to one of three physical memories: an 8-KB SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The 8-KB SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3). This is an important feature for low-power applications.

The **32/64/128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces. In addition to holding program code and constants, the non-volatile memory allows the application to save data that must be preserved such that it is available after restarting the device. Using this feature one can, e.g., use saved network-specific data to avoid the need for a full start-up and network find-and-join process .

Clocks and Power Management

The digital core and peripherals are powered by a 1.8-V low-dropout **voltage regulator**. It provides **power management** functionality that enables low power operation for long battery life using different power modes. Five different **reset** sources exist to reset the device.

Peripherals

The CC2530 includes many different peripherals that allow the application designer to develop advanced applications.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute supplied instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The device contains flash memory for storage of program code. The flash memory is programmable from the user software and through the debug interface. The **flash controller** handles writing and erasing the embedded flash memory. The flash controller allows page-wise erasure and 4-bytewise programming.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. CPU interrupts can be enabled on each pin individually. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface) achieve highly efficient operation by using the DMA controller for data transfers between SFR or XREG addresses and flash/SRAM.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in **IR Generation Mode** where it counts Timer 3 periods and the output is ANDed with the output of Timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 (the MAC Timer) is specially designed for supporting an IEEE 802.15.4 MAC or other time-slotted protocol in software. The timer has a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends, as well as two 16-bit output compare registers and two 24-bit overflow compare registers that can send various command strobes (start RX, start TX, etc.) at specific times to the radio modules.

Timer 3 and Timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as a PWM output.

The **sleep timer** is an ultralow-power timer that counts 32-kHz crystal oscillator or 32-kHz RC oscillator periods. The sleep timer runs continuously in all operating modes except power mode 3 (PM3). Typical applications of this timer are as a real-time counter or as a wake-up timer to come out of power mode 1 (PM1) or 2 (PM2).

The **ADC** supports 7 to 12 bits of resolution in a 30 kHz to 4 kHz bandwidth, respectively. DC and audio conversions with up to eight input channels (Port 0) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **operational amplifier** is intended to provide front-end buffering and gain for the ADC. Both inputs as well as the output are available on pins, so the feedback network is fully customizable. A chopper-stabilized mode is available for applications that need good accuracy with high gain.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

The **random-number generator** uses a 16-bit LFSR to generate pseudorandom numbers, which can be read by the CPU or used directly by the command strobe processor. It can be seeded with random data from noise in the radio ADC.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The core is able to support the AES operations required by IEEE 802.15.4 MAC security, the ZigBee network layer, and the application layer.

A built-in **watchdog timer** allows the CC2530 to reset itself in case the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out. It can alternatively be configured for use as a general 32-kHz timer.

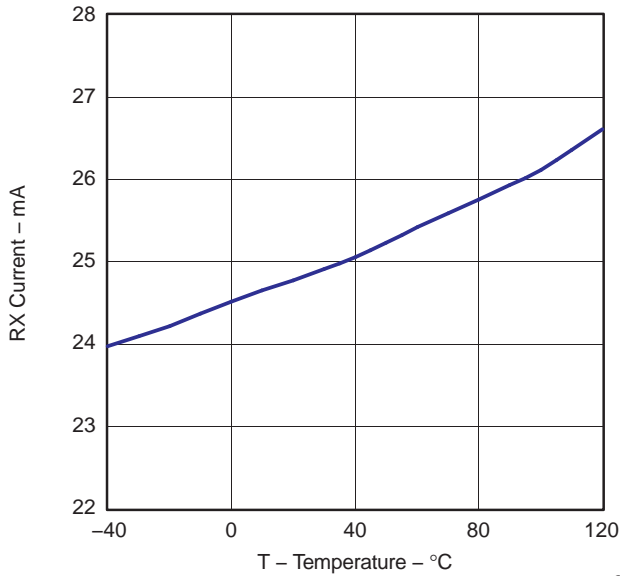
USART 0 and USART 1 are each configurable as either a SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses.

Radio

The CC2530 features an IEEE 802.15.4-compliant radio transceiver. The RF core controls the analog radio modules. In addition, it provides an interface between the MCU and the radio which makes it possible to issue commands, read status, and automate and sequence radio events. The radio also includes a packet-filtering and address-recognition module.

TYPICAL CHARACTERISTICS

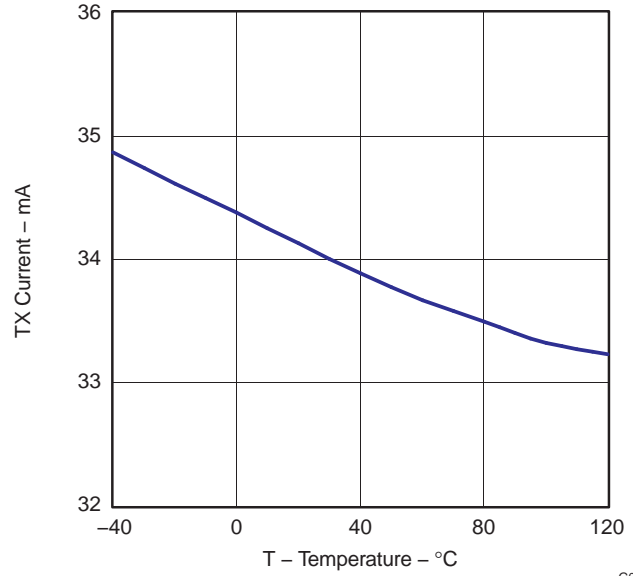
**RX CURRENT (-100 dBm INPUT)
 vs
 TEMPERATURE**



G001

Figure 9.

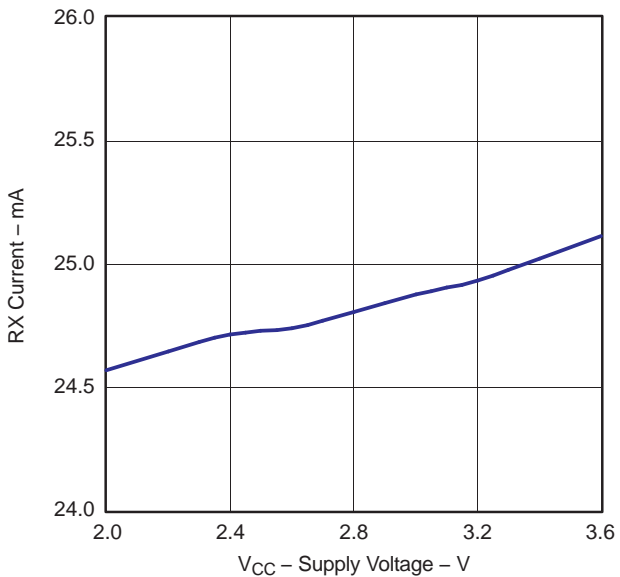
**TX CURRENT (TXPOWER = 0xF5)
 vs
 TEMPERATURE**



G002

Figure 10.

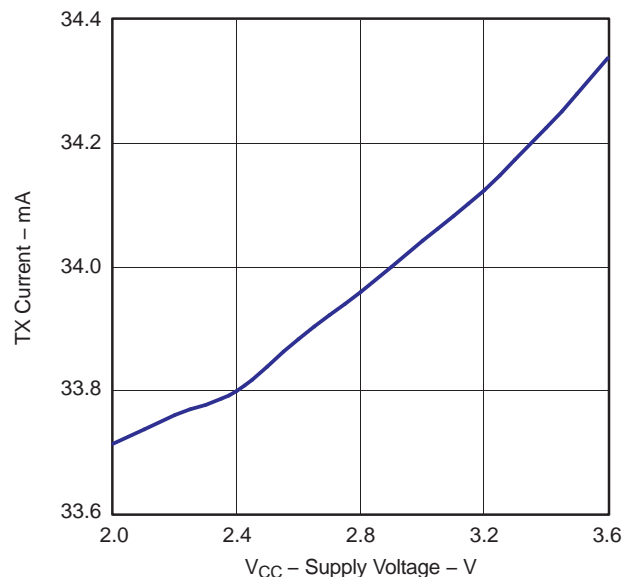
**RX CURRENT (-100 dBm INPUT)
 vs
 SUPPLY VOLTAGE**



G003

Figure 11.

**TX CURRENT (TXPOWER = 0xF5)
 vs
 SUPPLY VOLTAGE**

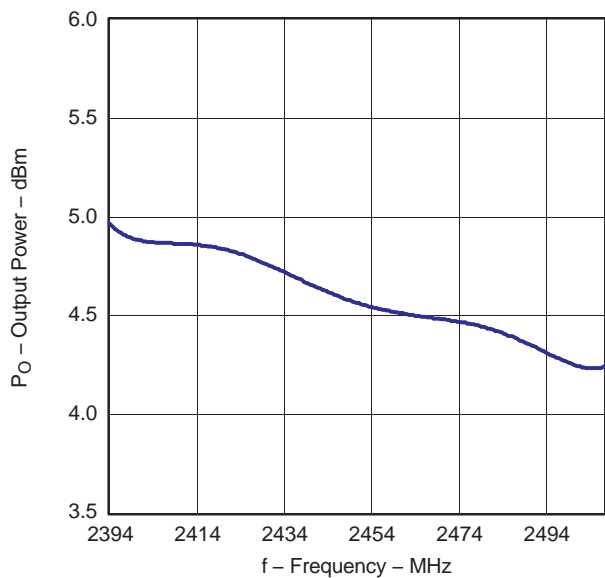


G004

Figure 12.

TYPICAL CHARACTERISTICS (continued)

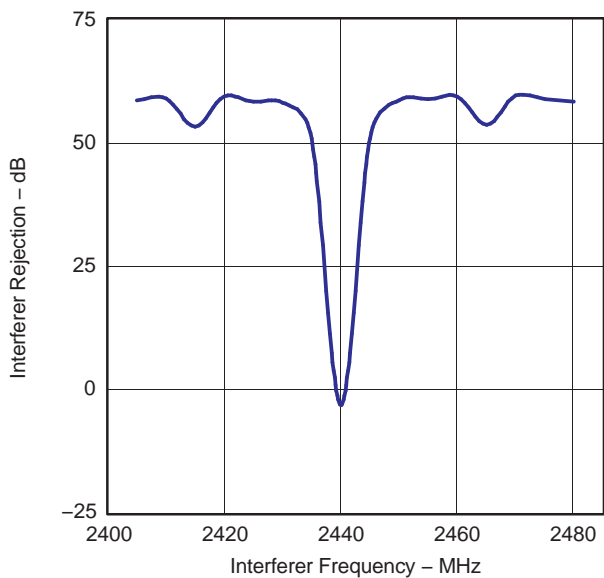
OUTPUT POWER (TXPOWER = 0xF5)
vs
FREQUENCY



G005

Figure 13.

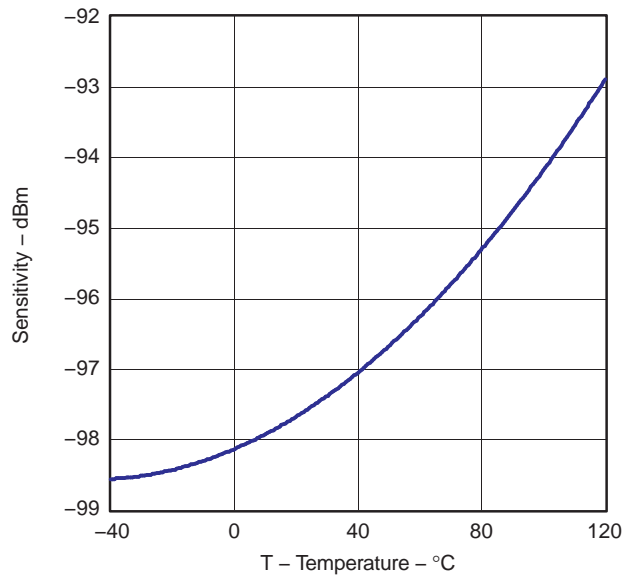
INTERFERER REJECTION (802.15.4 INTERFERER)
vs
INTERFERER FREQUENCY (CARRIER AT -82 dBm, 2440 MHz)



G006

Figure 14.

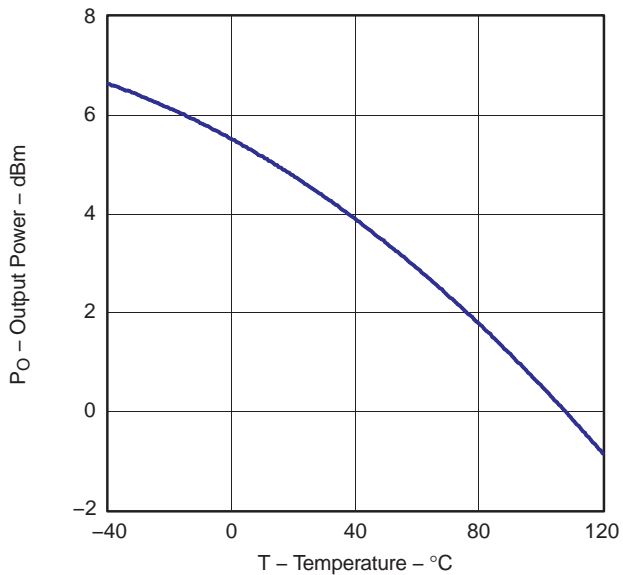
SENSITIVITY
vs
TEMPERATURE



G007

Figure 15.

OUTPUT POWER (TXPOWER = 0xF5)
vs
TEMPERATURE



G008

Figure 16.

TYPICAL CHARACTERISTICS (continued)

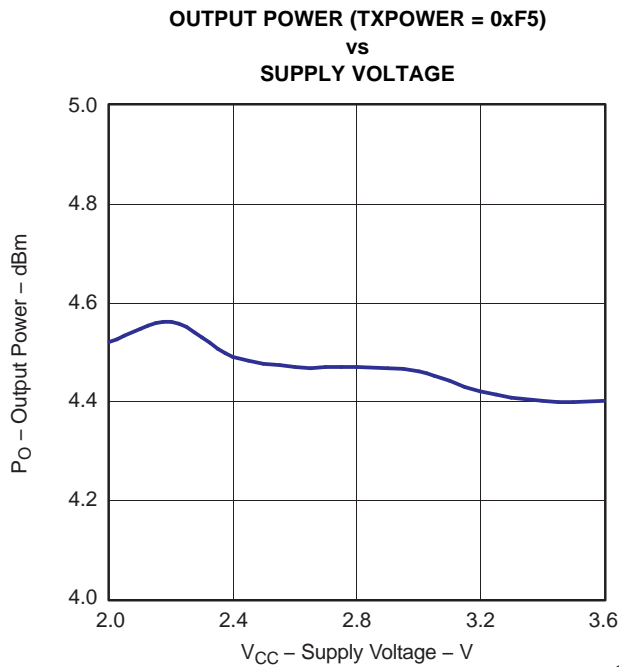


Figure 17.

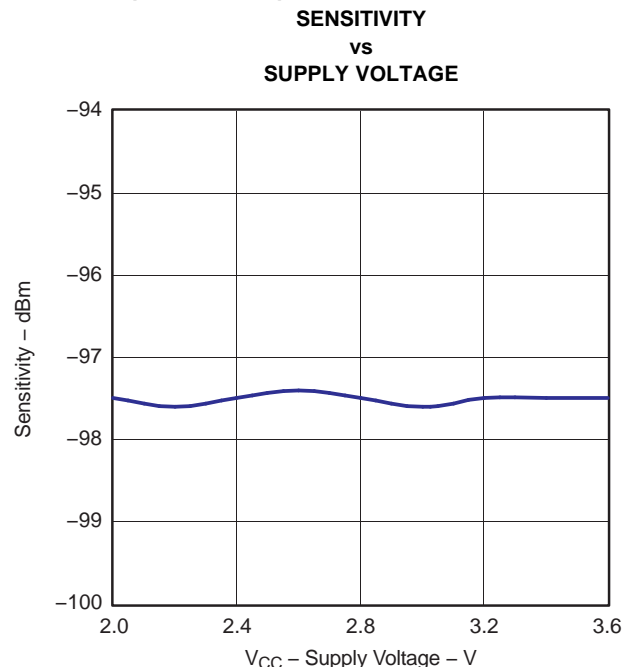


Figure 18.

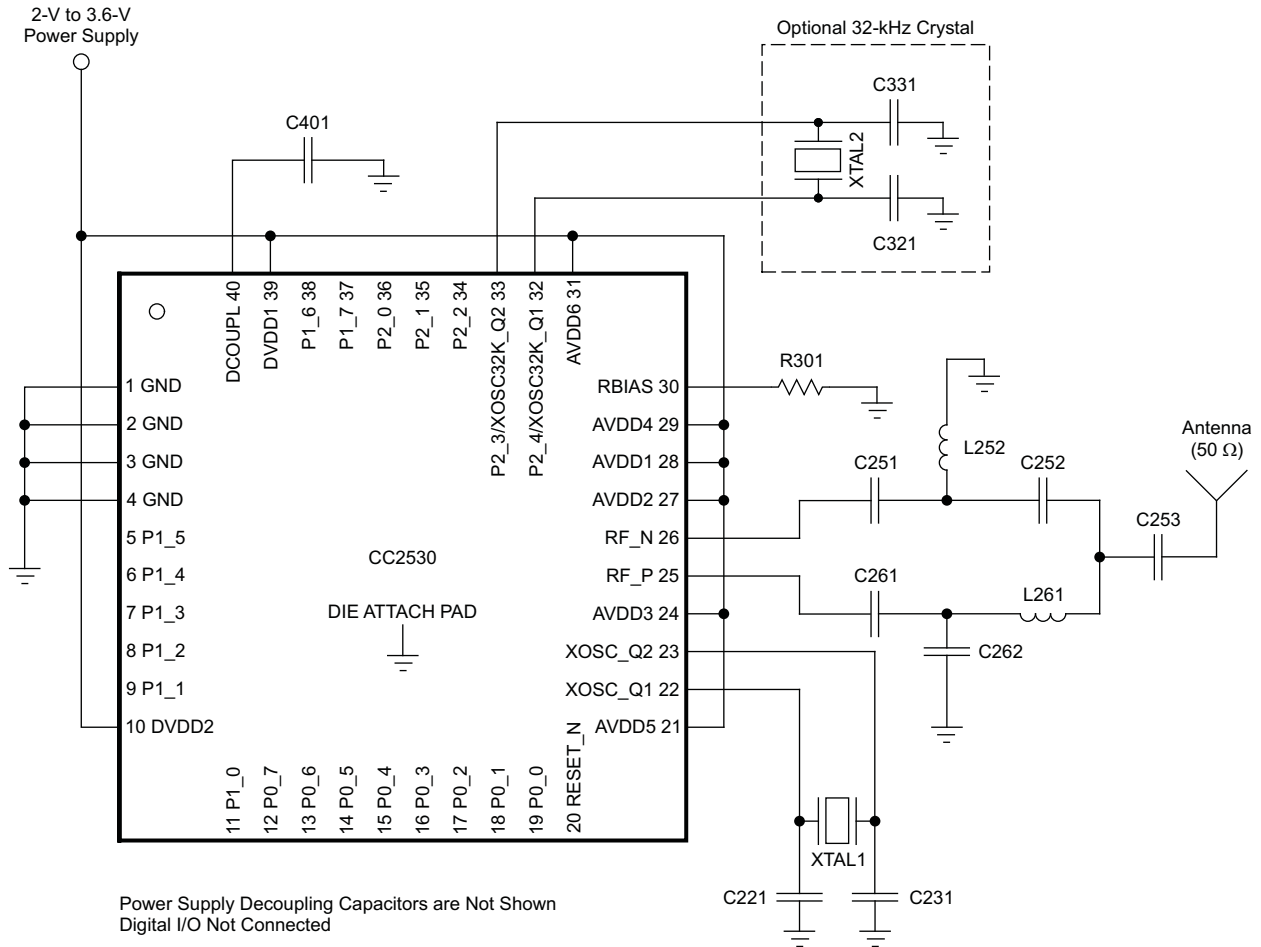
Table 2. Recommended Output Power Settings⁽¹⁾

| TXPOWER Register Setting | Typical Output Power (dBm) | Typical Current Consumption (mA) |
|--------------------------|----------------------------|----------------------------------|
| 0xF5 | 4.5 | 34 |
| 0xE5 | 2.5 | 31 |
| 0xD5 | 1 | 29 |
| 0xC5 | -0.5 | 28 |
| 0xB5 | -1.5 | 27 |
| 0xA5 | -3 | 27 |
| 0x95 | -4 | 26 |
| 0x85 | -6 | 26 |
| 0x75 | -8 | 25 |
| 0x65 | -10 | 25 |
| 0x55 | -12 | 25 |
| 0x45 | -14 | 25 |
| 0x35 | -16 | 25 |
| 0x25 | -18 | 24 |
| 0x15 | -20 | 24 |
| 0x05 | -22 | 23 |
| 0x05 and TXCTRL = 0x09 | -28 | 23 |

(1) Measured on Texas Instruments CC2530 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$, unless otherwise noted. See [References](#), Item 1, for recommended register settings.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2530. A typical application circuit is shown in Figure 19. Typical values and description of external components are shown in Table 3.



S0383-01

Figure 19. CC2530 Application Circuit

Table 3. Overview of External Components (Excluding Supply Decoupling Capacitors)

| Component | Description | Value |
|-----------|---|--------|
| C251 | Part of the RF matching network | 18 pF |
| C261 | Part of the RF matching network | 18 pF |
| L252 | Part of the RF matching network | 2 nH |
| L261 | Part of the RF matching network | 2 nH |
| C262 | Part of the RF matching network | 1 pF |
| C252 | Part of the RF matching network | 1 pF |
| C253 | Part of the RF matching network | 2.2 pF |
| C331 | 32kHz xtal loading capacitor | 15 pF |
| C321 | 32kHz xtal loading capacitor | 15 pF |
| C231 | 32MHz xtal loading capacitor | 27 pF |
| C221 | 32MHz xtal loading capacitor | 27 pF |
| C401 | Decoupling capacitor for the internal digital regulator | 1 μF |

Table 3. Overview of External Components (Excluding Supply Decoupling Capacitors) (continued)

| Component | Description | Value |
|-----------|------------------------------------|-------|
| R301 | Resistor used for internal biasing | 56 kΩ |

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. The recommended balun shown consists of C262, L261, C252, and L252.

If a balanced antenna such as a folded dipole is used, the balun can be omitted.

Crystal

An external 32-MHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-MHz crystal oscillator. See the [32-MHz Crystal Oscillator](#) section for details. The load capacitance seen by the 32-MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{\text{parasitic}} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{\text{parasitic}} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

On-Chip 1.8-V Voltage-Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

References

1. IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
<http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf>
2. CC253x User's Guide – CC253x System-on-Chip Solution for 2.4 GHz IEEE 802.15.4 and ZigBee Applications (SWRU191)

Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. Our selection includes RF transceivers, RF transmitters, RF front ends, and System-on-Chips as well as various software solutions for the sub-1- and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

The Low-Power RF E2E Online Community provides technical support forums, videos and blogs, and the chance to interact with fellow engineers from all over the world.

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Low-Power RF Online Community

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- RF design help
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- RF certification services and RF circuit manufacturing

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REVISION HISTORY

| Changes from Revision A (November 2010) to Revision B | Page |
|--|------|
| • Changed recommendation for single-crystal implementations to asynchronous networks | 1 |
| • Added op-amp and comparator to peripherals list | 1 |
| • Revised block diagram | 3 |
| • Added number of erase cycles and page size for flash | 5 |
| • Updated ESR for 32 kHz crystal | 8 |
| • Updated voltage coefficient for temperature sensor | 9 |
| • Added tables for op-amp and comparator to the <i>Electrical Characteristics</i> section | 10 |
| • Changed SPI AC characteristics SSN low from SCK negative edge to SCK positive edge and split into separate master and slave tables. | 13 |
| • Revised block diagram | 19 |
| • Corrected description of Timer 2 (MAC Timer) | 21 |
| • Improved readability of sleep timer description. | 21 |
| • Added the <i>operational amplifier</i> and the <i>ultralow-power analog comparator</i> paragraphs from the SWRS084 after <i>The ADC supports... channels</i> paragraph | 21 |
| • Removed sentence that pseudorandom data can be used for security | 21 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2530F128RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F128 | Samples |
| CC2530F128RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F128 | Samples |
| CC2530F256RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F256 | Samples |
| CC2530F256RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F256 | Samples |
| CC2530F32RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F32 | Samples |
| CC2530F32RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F32 | Samples |
| CC2530F64RHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F64 | Samples |
| CC2530F64RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | CC2530 F64 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

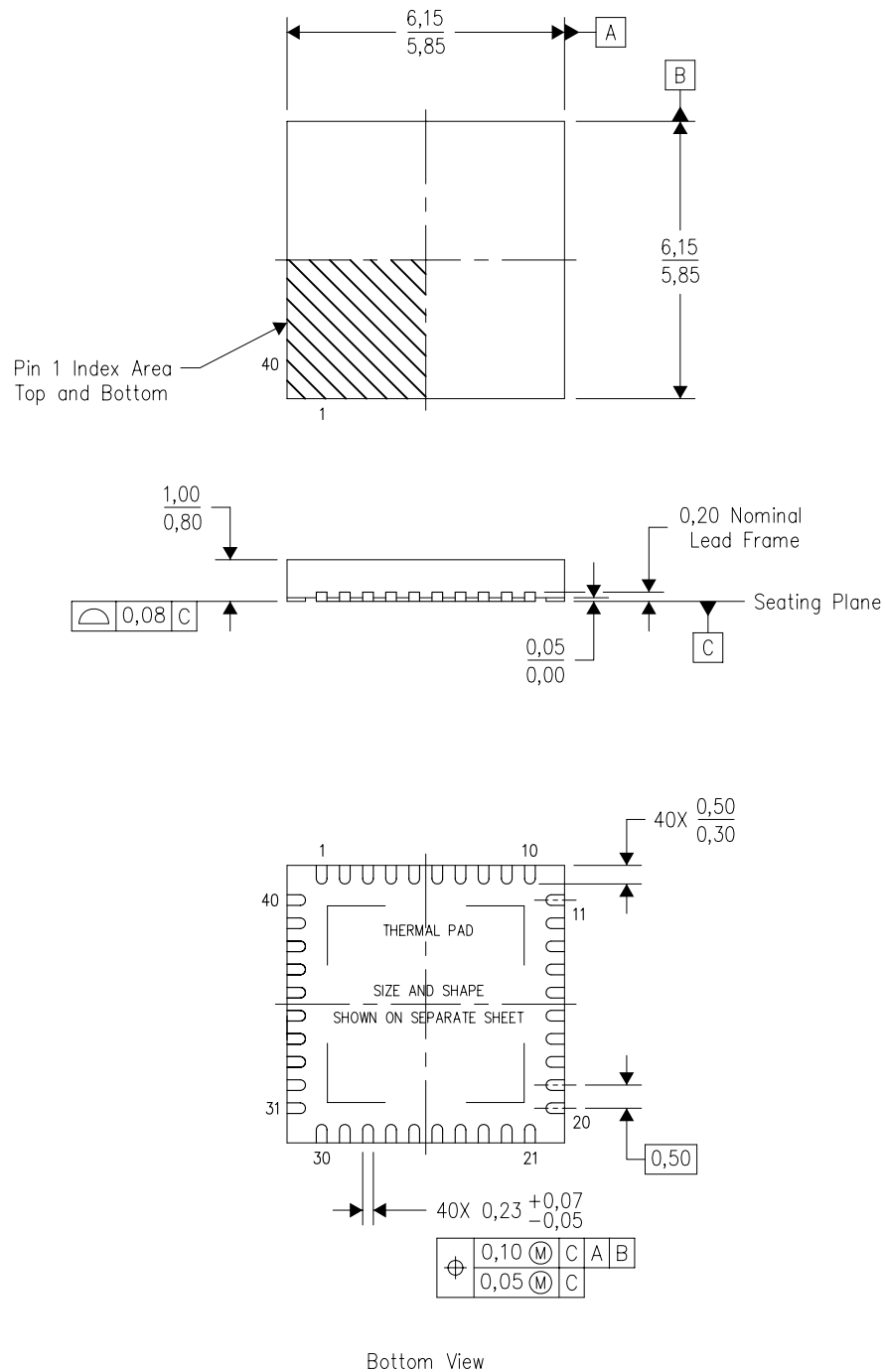
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

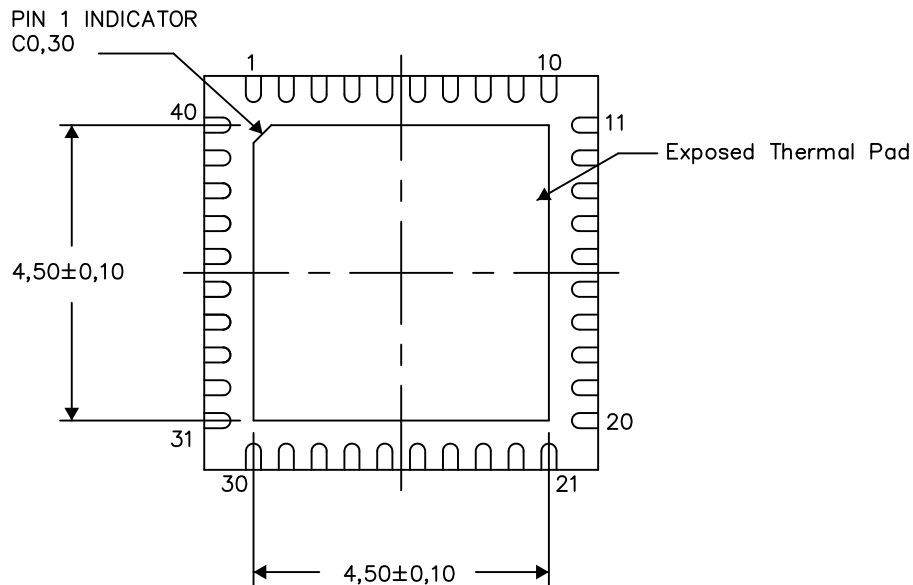
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

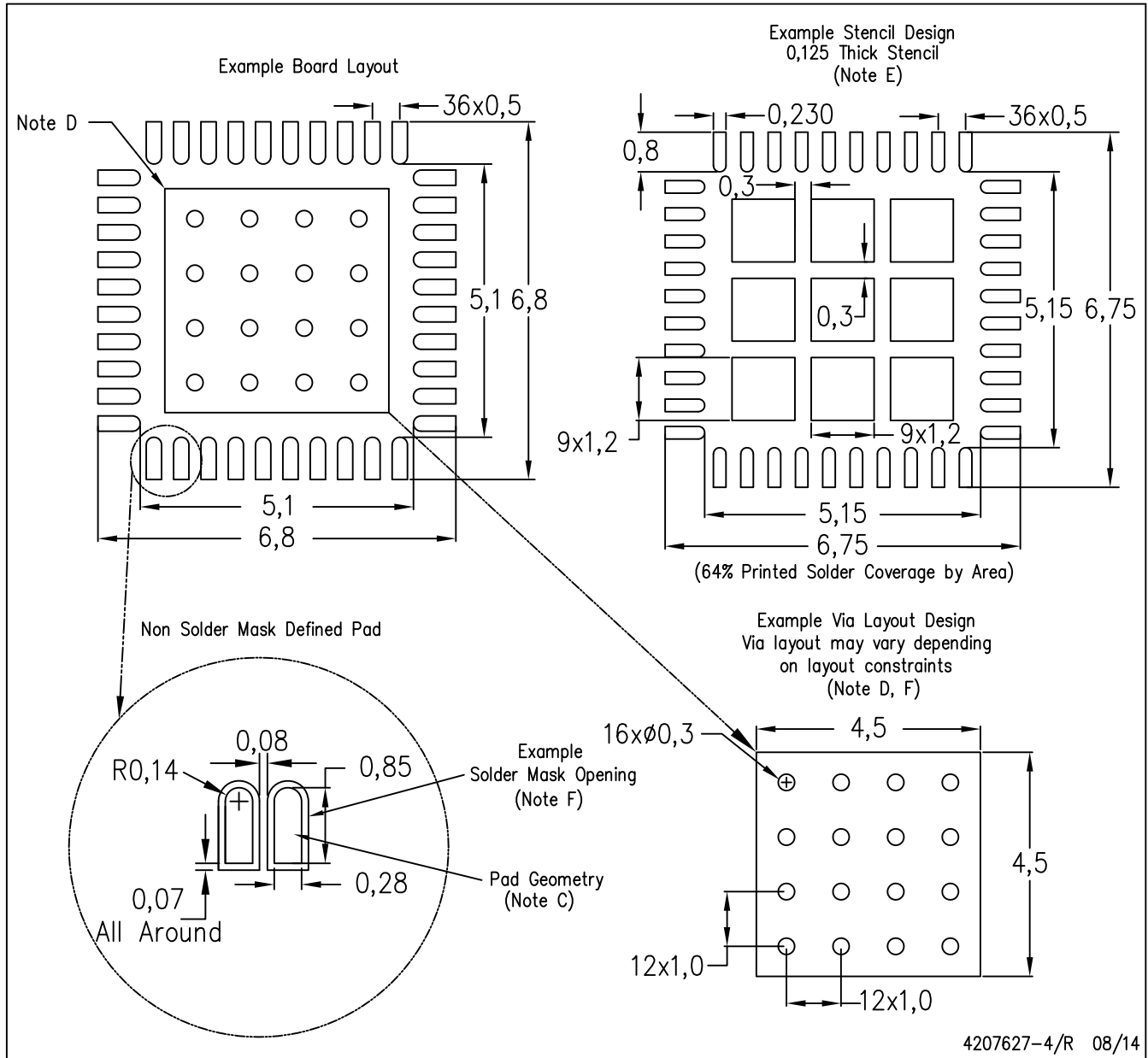
Exposed Thermal Pad Dimensions

4206355-4/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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