THE DATASHEET OF

IRS2334MPBF

International
IOR Rectifier

IRS2334SPbF
IRS2334MPbF

Three Phase Gate driver HVIC

Features

- Floating channel designed for bootstrap operation
- Fully operational to 600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Integrated dead time protection
- Shoot-through (cross-conduction) prevention logic
- Under-Voltage lockout for both channels
- Independent 3 half-bridge drivers
- 3.3 V input logic compatible
- Advanced input filter
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant

Typical Applications

- Motor Control
- Low Power Fans
- General Purpose Inverters
- Micro/Mini Inverter Drivers

Product Summary

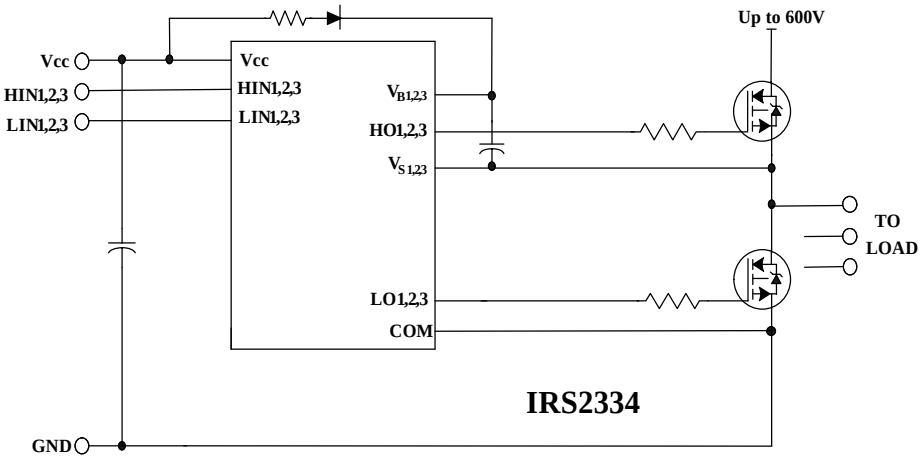
Topology	3 phase
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	200 mA & 350 mA
t_{ON} & t_{OFF} (typical)	530 ns

Package Options

20 leads wide body SOIC

28 leads MLPQ 5x5 (32 leads without 4)

Typical Connection Diagram



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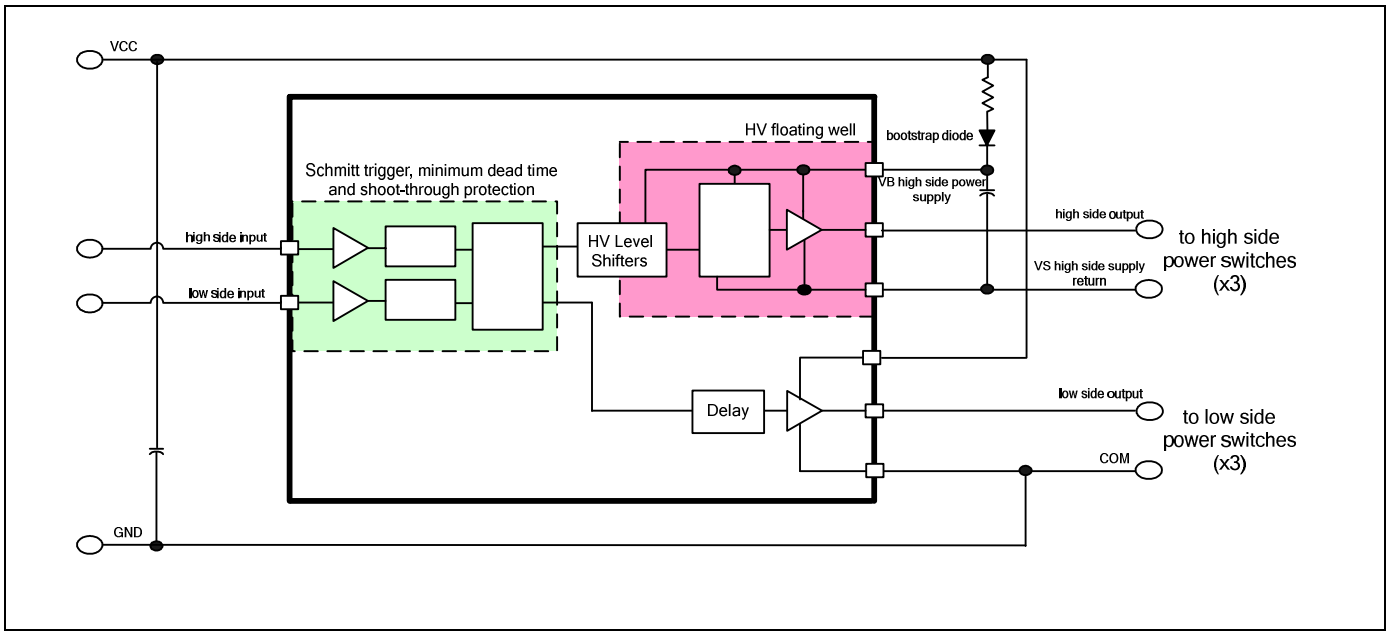
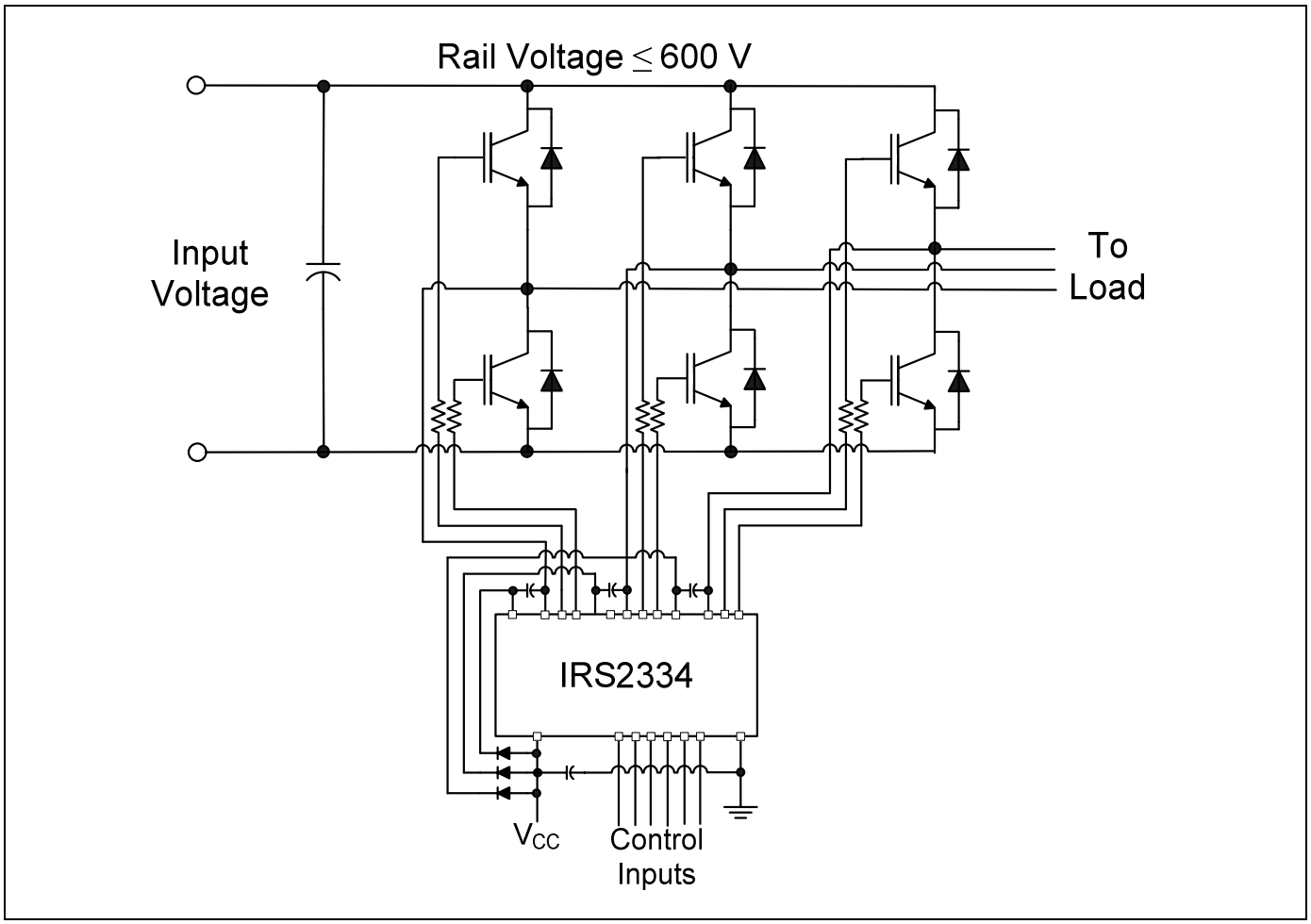
Description

The IRS2334 is a high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC and latch immune CMOS technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration up to 600 V.

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††
		Comments: This IC has passed JEDEC industrial qualification. IR consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2 , 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1C (per JEDEC standard JESD22-A114)
	Machine Model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise specified. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		$V_{B1,2,3}$ - 25†	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High side floating output voltage		$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25†	
$V_{LO1,2,3}$	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic and analog input voltages		-0.3	V_{CC} + 0.3	
PW_{HIN}	High-side input pulse width		500	—	ns
dV_S/dt	Allowable offset supply voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ TA ≤25°C	20 lead SOIC	—	1.14	W
		28 lead MLPQ	—	3.363	
Rth_{JA}	Thermal resistance, junction to ambient	20 lead SOIC	—	65.8	°C/W
		28 lead MLPQ	—	22.3	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

† All supplies are fully tested at 25 V. An internal 25 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise specified. The $V_{S1,2,3}$ offset ratings are tested with all supplies biased at 15 V.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ +10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	Static high side floating supply offset voltage†	-8	600	
$V_{S1,2,3}(t)$	Transient high side floating supply offset voltage††	-50	600	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low side and logic fixed supply voltage	10	20	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to $–V_{BS}$.
†† Operational for transient negative V_S of -50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Static Electrical Characteristics

(V_{CC}-COM) = ($V_{B1,2,3}$-$V_{S1,2,3}$) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the output leads LO1,2,3 and HO1,2,3 respectively. The V_{CCUV} and V_{BSUV} parameters are referenced to COM and V_S respectively.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
V_{OH}	High level output voltage	—	0.9	1.4		I_O = 20 mA
V_{OL}	Low level output voltage	—	0.4	0.6		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold	10.4	11.1	11.6		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold	10.2	10.9	11.4		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under-voltage hysteresis	0.1	0.2	—		
I_{LK}	Offset supply leakage current	—	1	50	µA	V_B =V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	40	120		V_{IN} = 0 V
I_{QCC}	Quiescent V_{CC} supply current	—	300	700	µA	
I_{IN+}	Logic "1" input bias current	—	150	250	µA	V_{IN} = 5 V
I_{IN-}	Logic "0" input bias current	—		1		V_{IN} = 0 V
I_{o+}	Output high short circuit pulsed current	120	200	—	mA	V_O = 0 V or 15 V PW ≤ 10 µs
I_{o-}	Output low short circuit pulsed current	250	350	—		

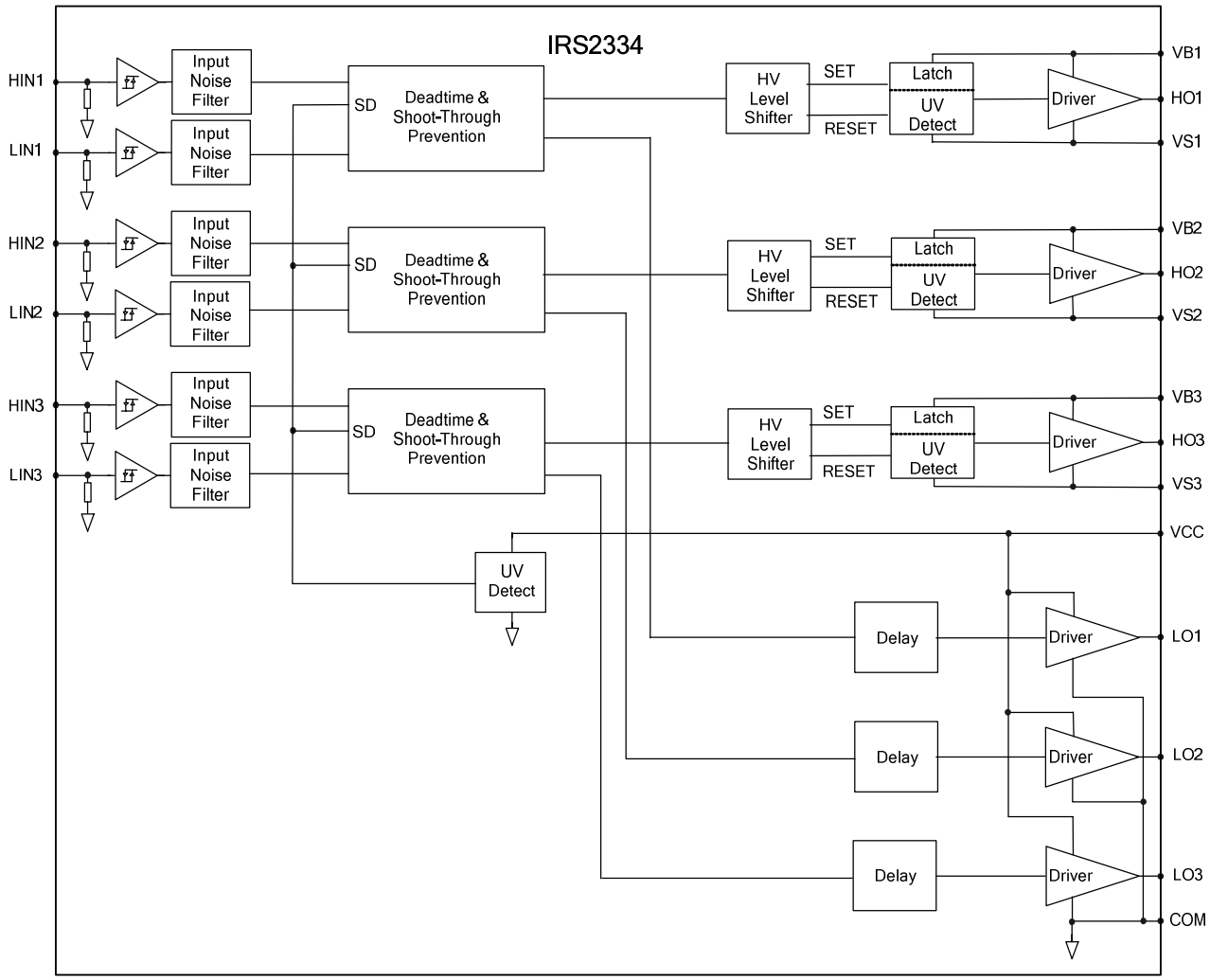
Dynamic Electrical Characteristics

V_{CC} = $V_{B1,2,3}$ = 15 V, $V_{S1,2,3}$ = COM, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

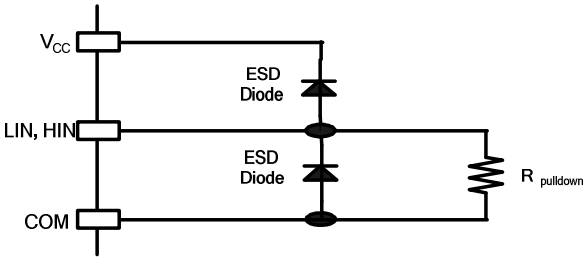
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0V and 5V
t_{off}	Turn-off propagation delay	400	530	750		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{FILIN}	Input filter time	200	350	510		
DT	Dead time	190	290	420		V_{IN} = 0V & 5V External dead time 0s
MDT	Dead time matching	—	—	60		
MT	t_{on}, t_{off} propagation delay matching time	—	—	50		
PM	PW pulse width distortion†	—	—	75		PW input =10µs

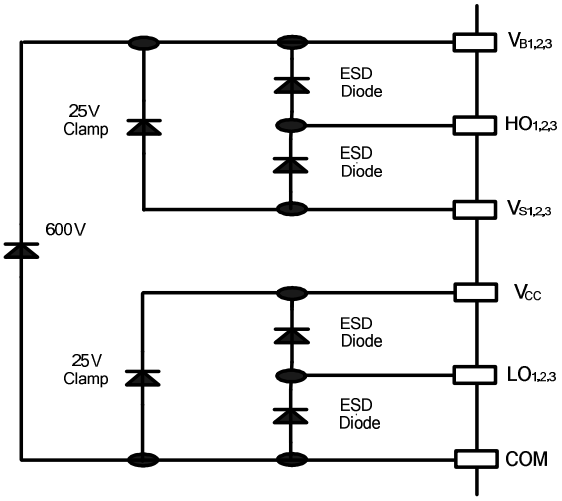
† PM is defined as PW_{IN} - PW_{OUT}.

Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams



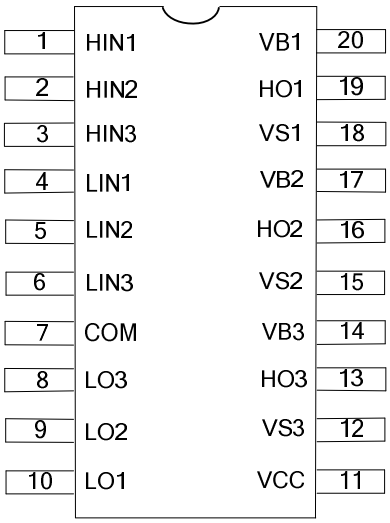


Lead Definitions

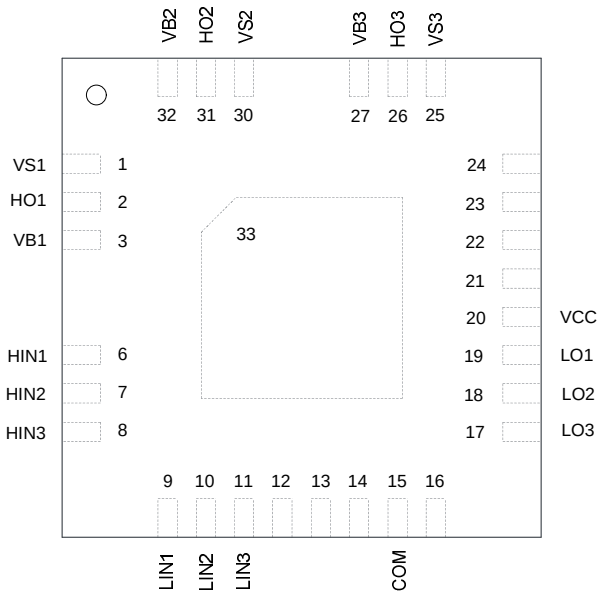
Symbol	Description
VCC	Low side and logic power supply
VB1	High side floating power supply (phase 1)
VB2	High side floating power supply (phase 2)
VB3	High side floating power supply (phase 3)
VS1	High side floating supply return (phase 1)
VS2	High side floating supply return (phase 2)
VS3	High side floating supply return (phase 3)
HIN1	Logic input for high side gate driver output HO1, input is in-phase with output
HIN2	Logic input for high side gate driver output HO2, input is in-phase with output
HIN3	Logic input for high side gate driver output HO3, input is in-phase with output
LIN1	Logic input for low side gate driver output LO1, input is in-phase with output
LIN2	Logic input for low side gate driver output LO2, input is in-phase with output
LIN3	Logic input for low side gate driver output LO3, input is in-phase with output
HO1	High side gate driver output (phase 1)
HO2	High side gate driver output (phase 2)
HO3	High side gate driver output (phase 3)
LO1	Low side gate driver output (phase 1)
LO2	Low side gate driver output (phase 2)
LO3	Low side gate driver output (phase 3)
COM	Low side supply return

Lead Assignments

20 leads wide body SOIC



32 leads MLPQ 5x5 without 4 leads



The central exposed pad (33) has to be connected to COM for better electrical performance.

Application Information and Additional Details

IGBT/MOSFET Gate Drive

The IRS2334 HVIC is designed to drive high side and low side MOSFET or IGBT power devices. Figures 1 and 2 show the definition of some of the relevant parameters associated with the gate driver output functionality. The output current that drives the gate of the external power switches is defined as I_O. The output voltage that drives the gate of the external power switches is defined as V_{HO} for the high side and V_{LO} for the low side; this parameter is sometimes generically called V_{OUT} and in this case the high side and low side output voltages are not differentiated.

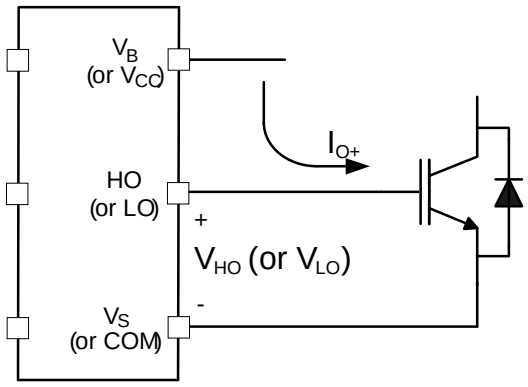


Figure 1: HVIC sourcing current

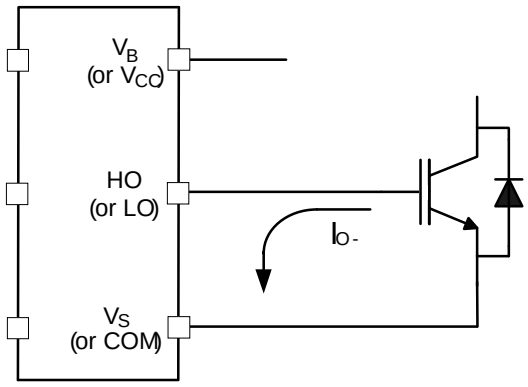


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS2334 HVIC is shown in Figure 3. The definitions of some of the relevant parameters associated with the gate driver input to output transmission are given.

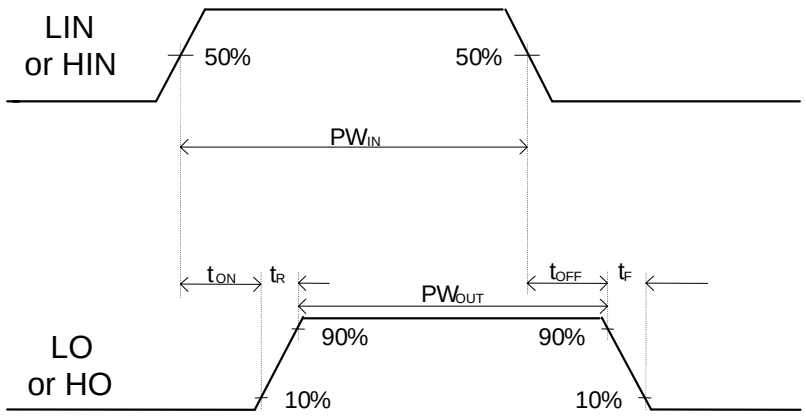


Figure 3: Switching time waveforms

During interval A of Figure 4 the HVIC receives the command to turn on both the high and low side switches at the same time; correspondingly, the shoot-through protection prevents the high and low side signals HO and LO turn on by keeping them low.

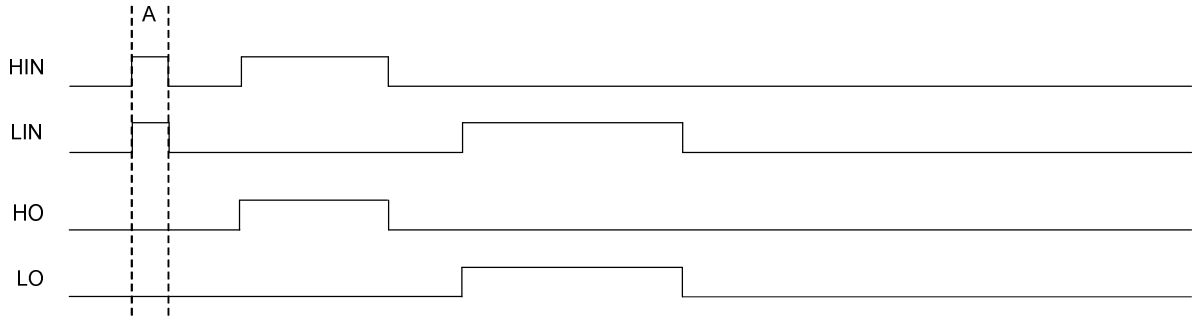


Figure 4: Input/output timing diagram

Deadtime

The IRS2334 HVIC provides an integrated deadtime protection circuitry. The deadtime interval for this HVIC is fixed; while other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time interval in which both the gate driver outputs LO and HO are held off; to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime commanded by the host microcontroller is shorter than DT, while external deadtimes larger than DT are not modified by the gate driver. Figure 7 illustrates the deadtime interval definition and the relationship between the output gate signals.

The deadtime interval introduced is matched with respect to the commutation from HIN turning off to LIN turning on, and viceversa. Figure 5 defines the two deadtime parameters DT1 and DT2. The deadtime matching parameter MDT is defined as the maximum difference between DT1 and DT2.

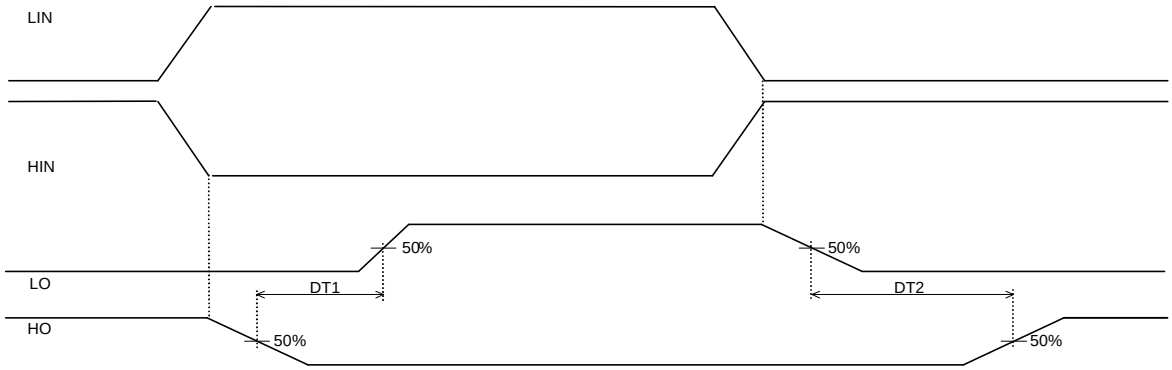


Figure 5: Deadtime definition

Matched Propagation Delays

The IRS2334 HVIC is designed for propagation delay matching. With this feature, the input to output propagation delays t_{ON}, t_{OFF} are the same for the low side and the high side channels; the maximum difference being specified by the delay matching parameter MT as defined in Figure 6.

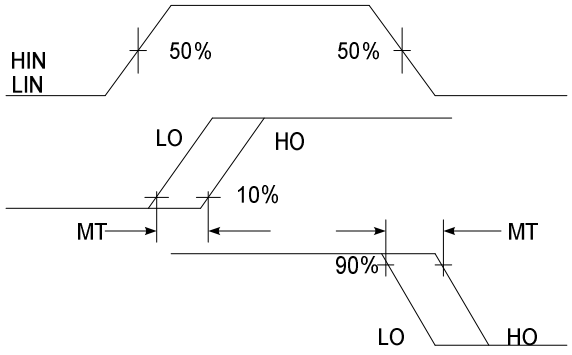


Figure 6: Delay Matching Waveform Definition

Input Logic Compatibility

The IRS2334 HVIC is designed with inputs compatible with standard CMOS and TTL outputs with 3.3 V and 5 V logic level signals. Figure 7 shows how an input signal is logically interpreted.

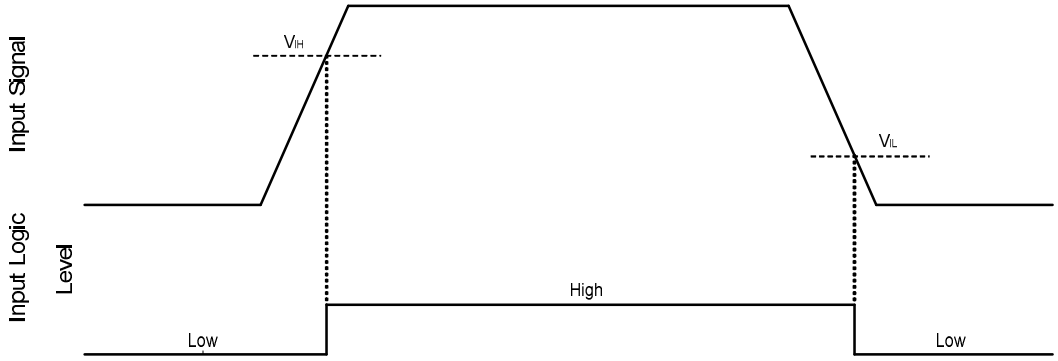


Figure 7: HIN & LIN input thresholds

Shoot-Through Protection

The IRS2334 is equipped with a shoot-through protection circuitry which prevents cross-conduction of the power switches. Table 1 shows the input to output relationship in the form of a truth table. Note that the HVIC has non-inverting inputs (the output is in-phase with the respective input).

HIN	LIN	HO	LO
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Table 1: Input/output truth table

Under-Voltage Lockout Protection

The IRS2334 HVIC provides under-voltage lockout protection on both the V_{CC} low side and logic fixed power supply and the VBS high side floating power supply. Figure 8 illustrates this concept by considering the V_{CC} (or V_{BS}) plotted over time: as the waveform crosses the UVLO threshold, the under-voltage protection is entered or exited.

Upon power up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the gate driver outputs LO and HO will remain disabled. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during normal operation, the under-voltage lockout circuitry will shutdown the gate driver outputs LO and HO.

Upon power up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the gate driver output HO will remain disabled. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during normal operation, the under-voltage lockout circuitry will shutdown the high side gate driver output HO.

The UVLO protection ensures that the HVIC drives external power devices only with a gate supply voltage sufficient to fully enhance them. Without this protection, the gates of the external power switches could be driven with a low voltage, which would result in power switches conducting current while with a high channel impedance, which would produce very high conduction losses possibly leading to power device failure.

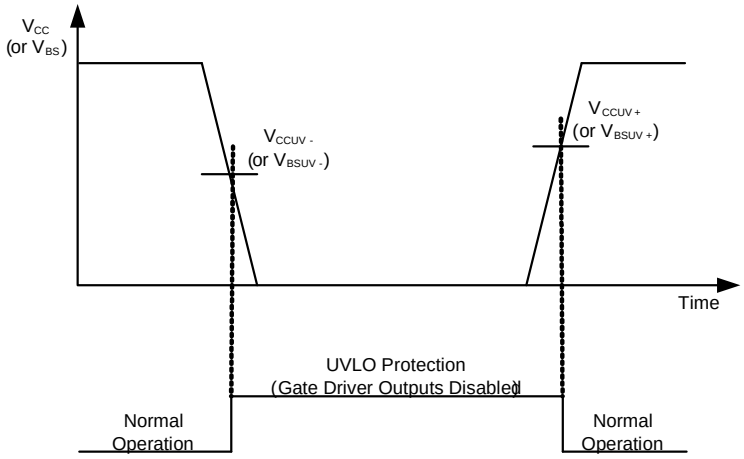


Figure 8: UVLO protection

Truth Table: Under-Voltage lockout

Table 2 provides the truth table for the IRS2334 HVIC.

The 1st line shows that for V_{CC} below the UVLO threshold both the gate driver outputs LO and HO are disabled. After V_{CC} returns above V_{CCUV}, the gate driver outputs return functional.

The 2nd line shows that for V_{BS} below the UVLO threshold, the gate driver output HO is disabled. After V_{BS} returns above V_{BSUV}, HO remains low until a new rising transition of HIN is received.

The last line shows the normal operation of the HVIC.

	VCC	VBS	outputs	
			LO	HO
UVLO V_{CC}	<V_{CCUV}		0	0
UVLO V_{BS}	15 V	<V_{BSUV}	LIN	0
Normal operation	15 V	15 V	LIN	HIN

Table 2: UVLO truth table

Advanced Input Filter

The IRS2334 HVIC provides an advanced input filter that improves the input/output pulse symmetry of the signals processed by the HVIC. This input filter is inserted at the HIN and LIN input pins. The working principle of the filter is shown in Figures 9 and 10.

Figure 9 shows a typical input filter and the asymmetry it produces on its output signal. The upper waveforms of Example 1 show an input signal with a pulse duration mush longer than the filtering time t_{FILIN}; the resulting output signal has a duration given approximately by the difference between the input signal and t_{FILIN}. The lower waveforms of Example 2 show an input signal with a pulse duration slightly longer than the filtering time t_{FILIN}; the resulting output signal has a duration given approximately by the difference between the input signal and $t_{FILIN,}$ much shorter than it should be.

Figure 10 shows the advanced input filter and the symmetry it produces on its output signal. The upper waveforms of Example 1 show an input signal with a pulse duration much longer than the filtering time t_{FILIN}; the resulting output signal has approximately the same duration as the input signal. The lower waveforms of Example 2 show an input signal with a pulse duration slightly longer than the filtering time t_{FILIN}; the resulting output signal has approximately the same duration as the input signal.

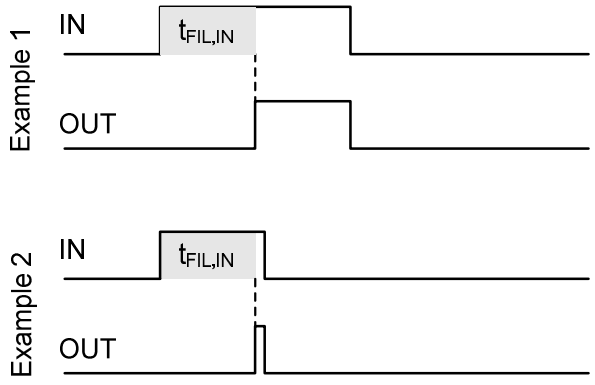


Figure 9: Typical input filter

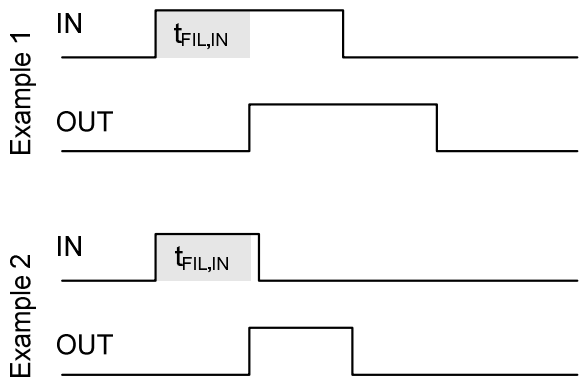


Figure 10: Advanced input filter

Short-Pulse and Noise Rejection

The advanced input filter that improves the input/output pulse symmetry of the signals processed by the HVIC also helps the rejection of noise spikes and of short pulses on the input signals.

Input signals with a pulse duration less than the filtering time t_{FILIN} will be filtered out. In Figure 11 Example 1 shows an input signal in the low state with superimposed positive noise spikes of duration less than t_{FILIN}; the advanced input filter filters out the noise spikes and the output signal remains in the low state. Example 2 shows an input signal in the high state with superimposed negative noise spikes of duration less than t_{FILIN}; the advanced input filter filters out the noise spikes and the output signal remains in the high state.

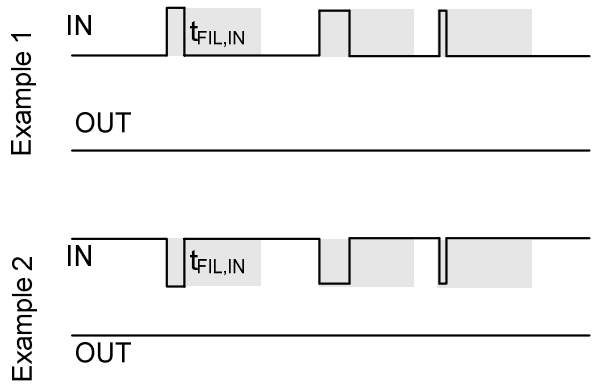


Figure 11: Noise rejection of the advanced input filter

The measured characteristic of the advanced input filter is shown in Figure 12. On the left side the characteristic for narrow ON pulses is shown (short positive pulse) while on the left side the characteristic for narrow OFF pulses is shown (short negative pulse). The x-axis represents the input pulse duration PW_{IN}, while the y-axis the resulting output pulse duration PW_{OUT}. For pulses with input pulse duration PW_{IN} less than the filtering time t_{FILIN} the resulting output pulse duration PW_{OUT} is zero because the filter rejects the input signal. For pulses with input pulse duration PW_{IN} greater than the filtering time t_{FILIN} the resulting output pulse duration PW_{OUT} tracks the input pulse durations well, the higher the duration the better the symmetry.

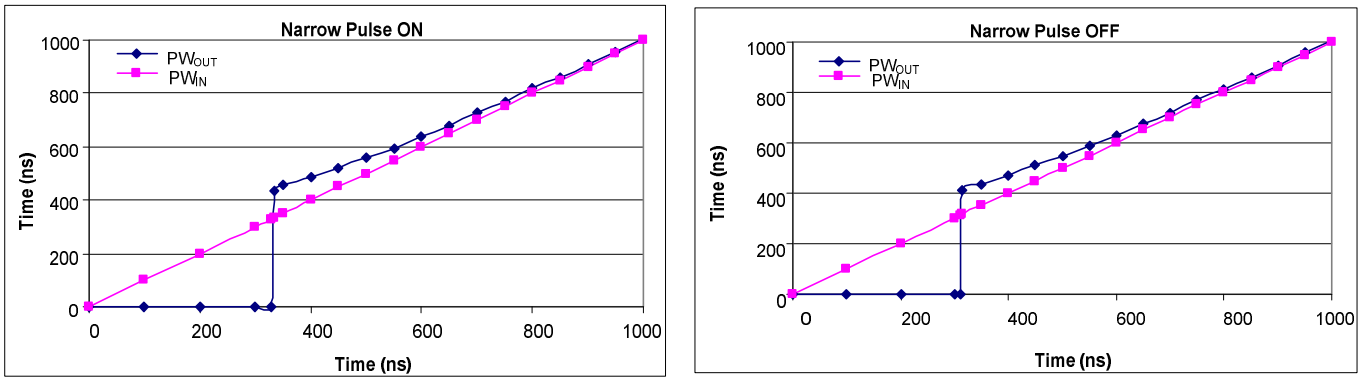


Figure 12: Measured advanced input filter characteristic

The difference between the output pulse duration PW_{OUT} and the input pulse duration PW_{IN} of both the narrow ON and narrow OFF cases is shown in Figure 13. The x-axis represents the input pulse duration PW_{IN}, while the y-axis the resulting difference $PW_{OUT}–PW_{IN}$.

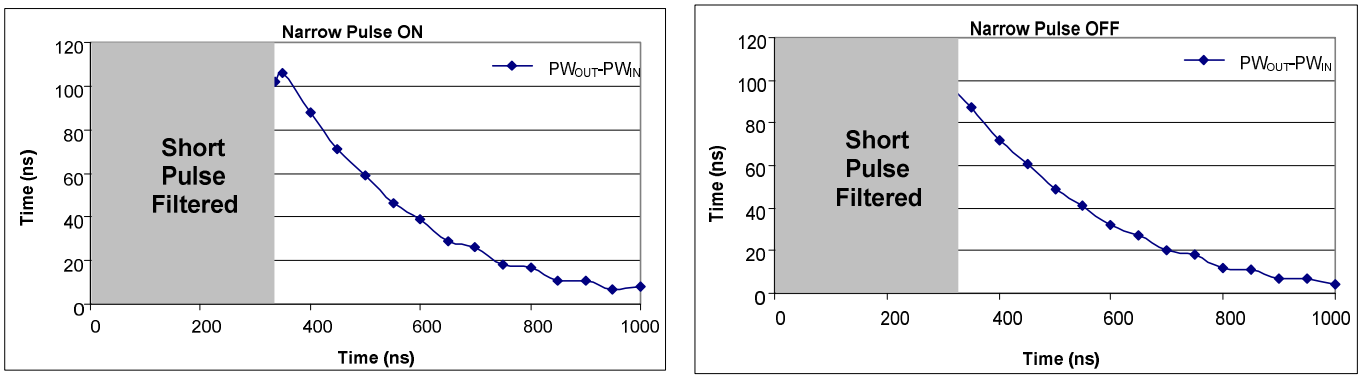


Figure 13: Difference between the input pulse duration and the output pulse duration

Tolerant to Negative VS Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power devices switch on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 14; where we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 15 and 16) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

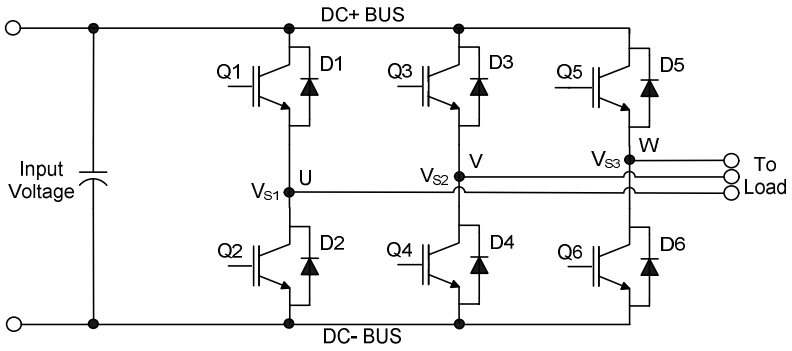


Figure 14: Three phase inverter

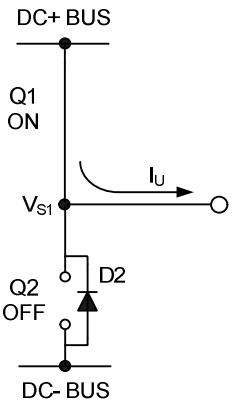


Figure 15: Q1 conducting

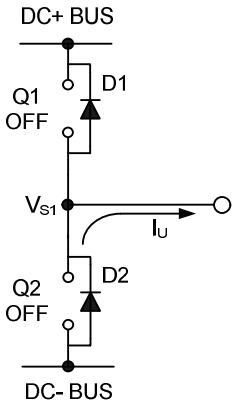


Figure 16: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 17 and 18), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

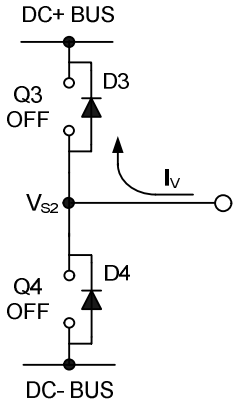


Figure 17: D3 conducting

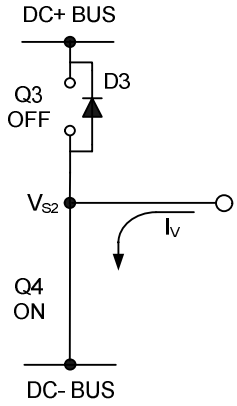


Figure 18: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 19 depicts one leg of the three phase inverter; Figures 20 and 21 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

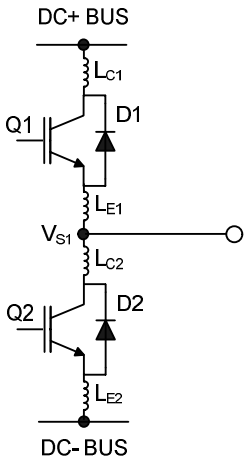


Figure 19: Parasitic Elements

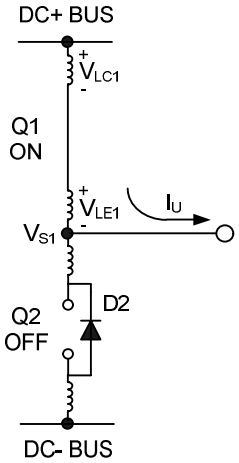


Figure 20: V_S positive

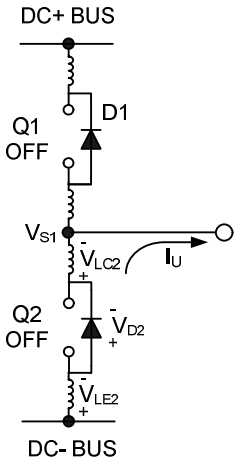


Figure 21: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS2334's robustness can be seen in Figure 22, where there is represented the IRS2334 Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

At V_{BS}=15V in case of -V_S transients greater than -16.5 V for a period of time greater than 50 ns; the HVIC will hold by design the high-side outputs in the off state for 4.5 µs.

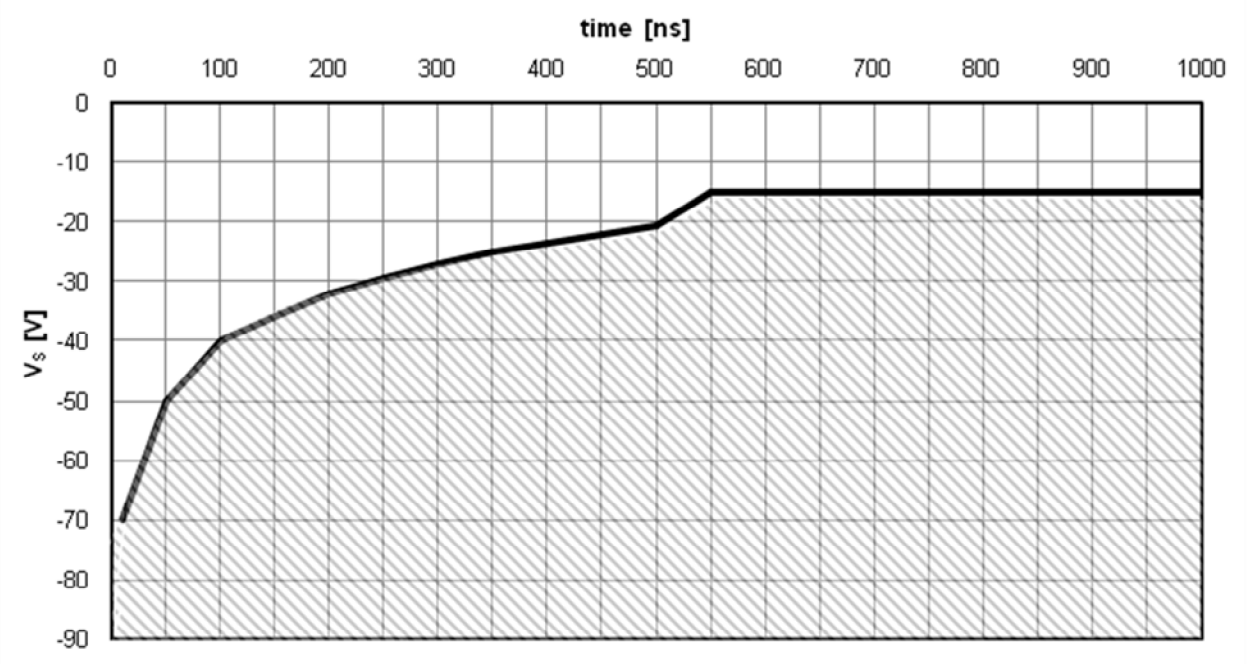


Figure 22: Negative V_S transient SOA @ VBS=15V

Even though the IRS2334 has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side. For IRS2334M the central exposed pad has to be connected to COM for better electrical performance.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 23). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

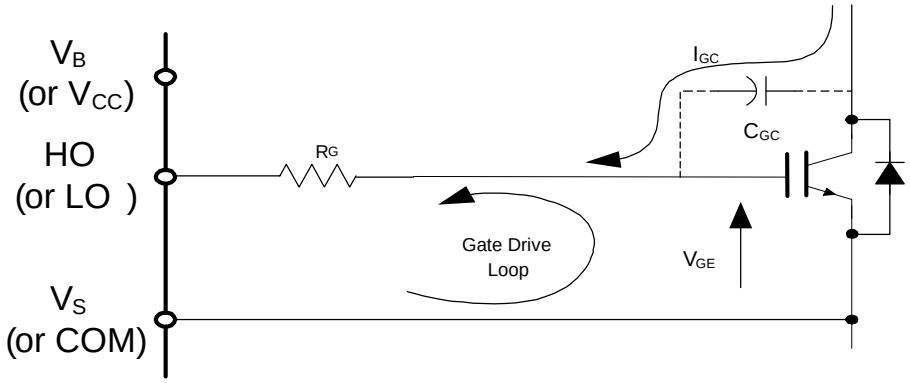


Figure 23: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor between the VCC and COM pins. This connection is shown in Figure 24. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

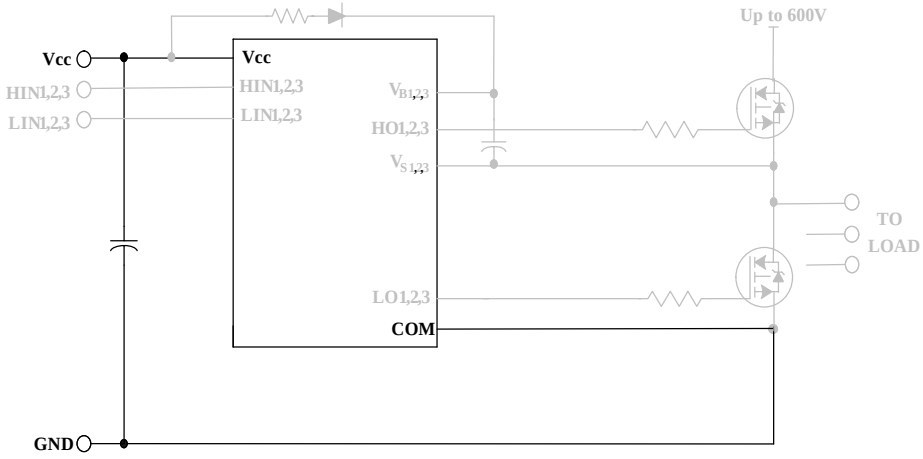


Figure 24: Supply capacitor

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side source to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes

placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 25), and in some cases using a clamping diode between COM and V_S (see Figure 26). See DT04-4 at www.irf.com for more detailed information.

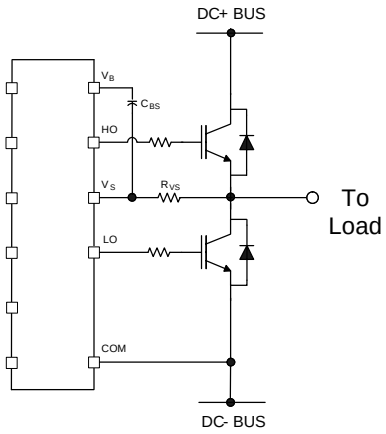


Figure 25: V_S resistor

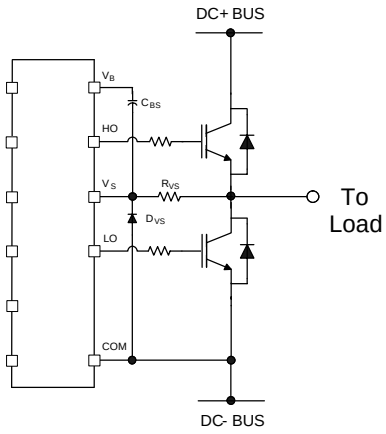


Figure 26: V_S clamping diode

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Parameter Temperature Trends

Figures 27-44 provide information on the experimental performance of the IRS2334 HVIC. The line plotted in each figure is generated from actual experimental data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

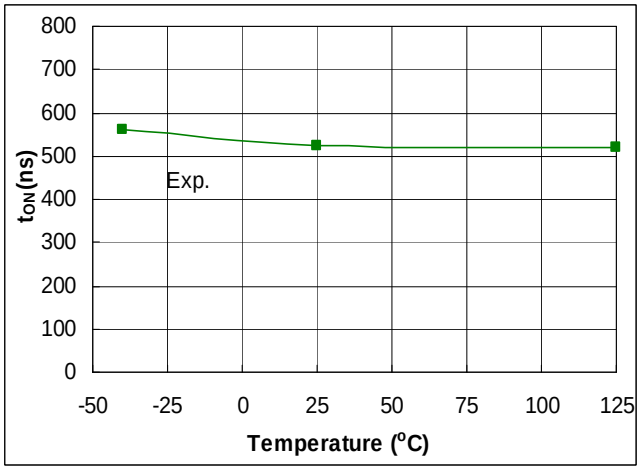


Fig. 27. Turn-on Propagation Delay vs. Temperature

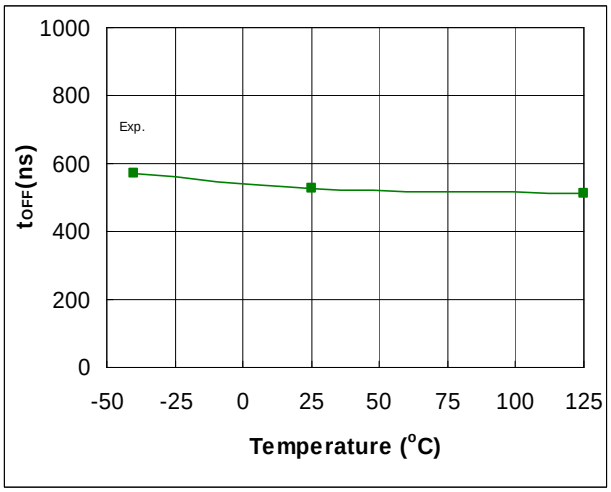


Fig. 28. Turn-off Propagation Delay vs. Temperature

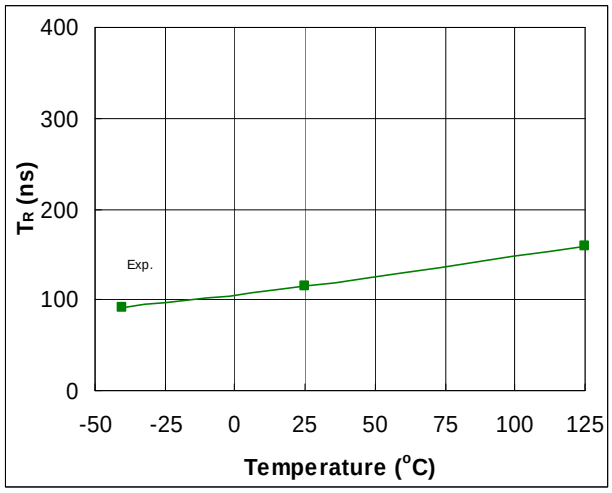


Fig. 29. Turn-on Rise Time vs. Temperature

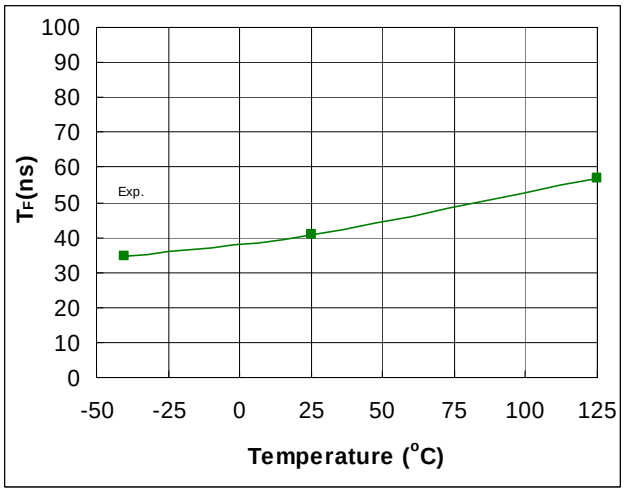


Fig.30. Turn-off Fall Time vs. Temperature

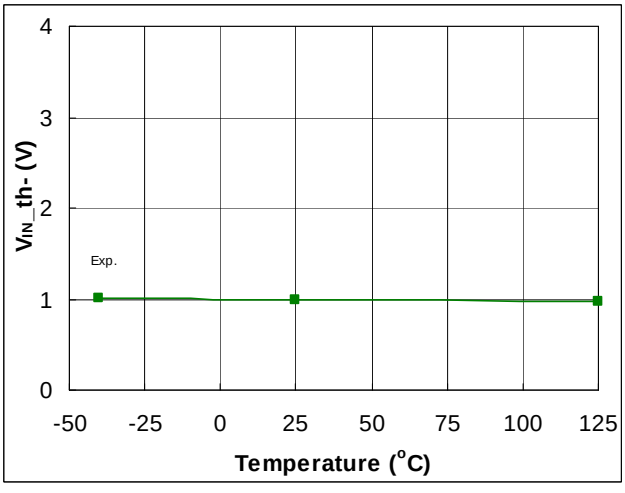


Fig. 31. Input Negative Going Threshold vs. Temperature

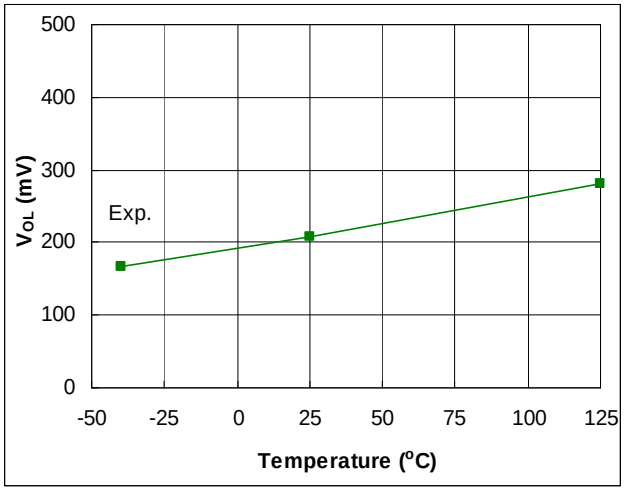


Fig. 32. Low Level Output Voltage vs. Temperature

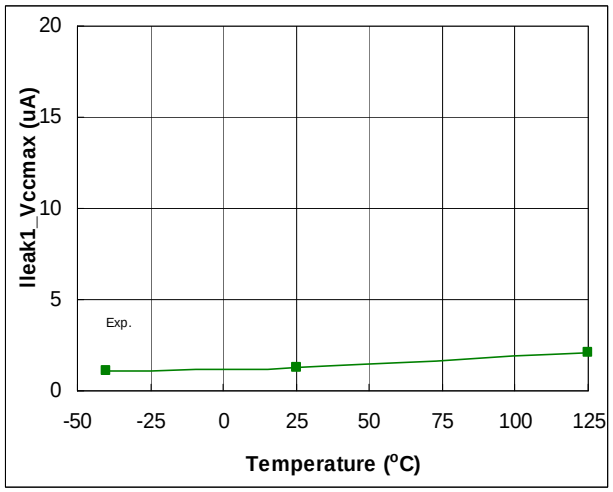


Fig. 33. Offset Supply Leakage Current vs. Temperature

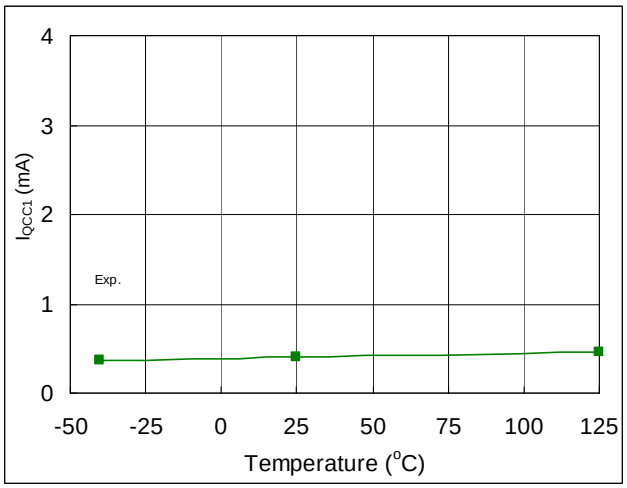


Fig. 34. Quiescent VCC Supply Current vs. Temperature

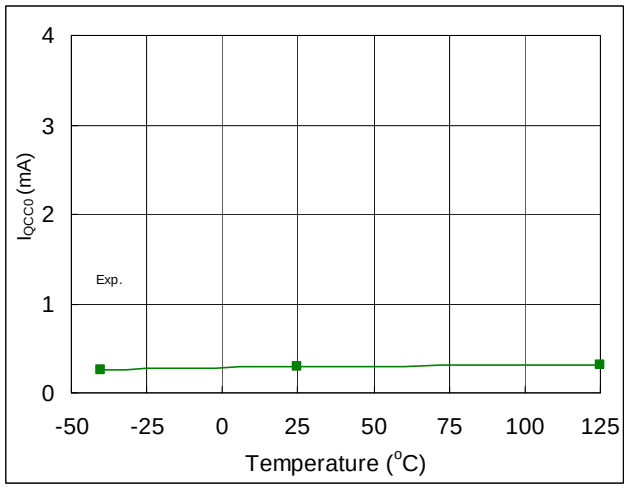


Fig. 35. Quiescent VCC Supply Current vs. Temperature

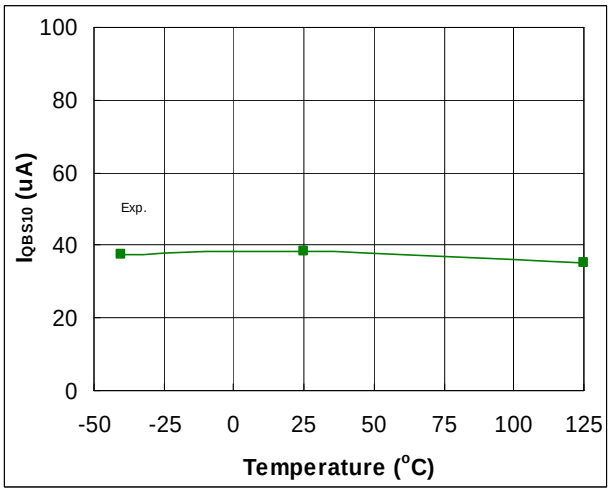


Fig. 36. Quiescent VBS Supply Current vs. Temperature

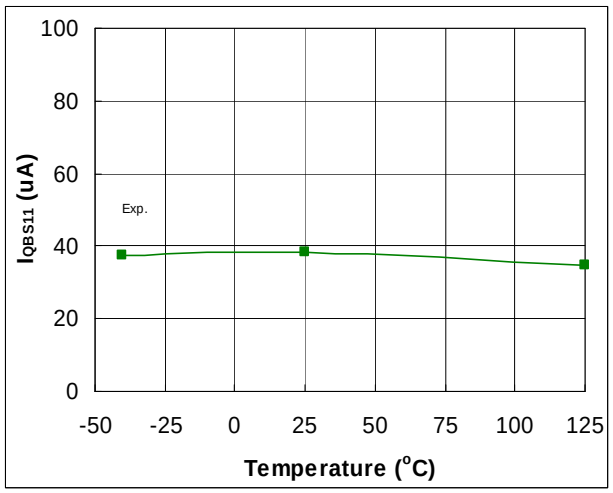


Fig. 37. Quiescent VBS Supply Current vs. Temperature

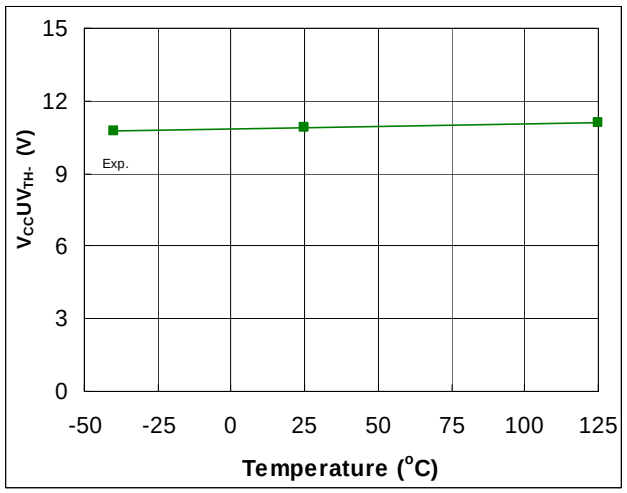


Fig. 38. VCC Supply Under-voltage Negative Going Threshold vs. Temperature

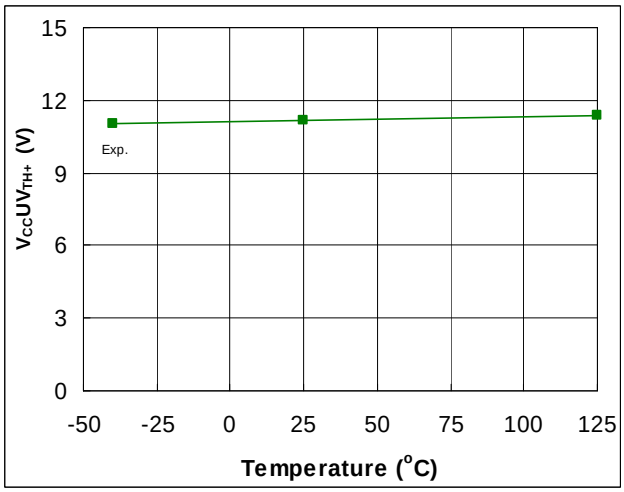


Fig. 39. VCC Supply Under-voltage Positive Going Threshold vs. Temperature

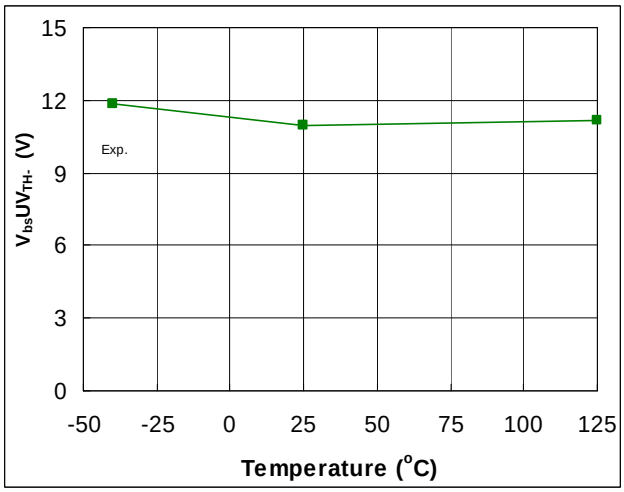


Fig. 40. VBS Supply Under-voltage Negative Going Threshold vs. Temperature

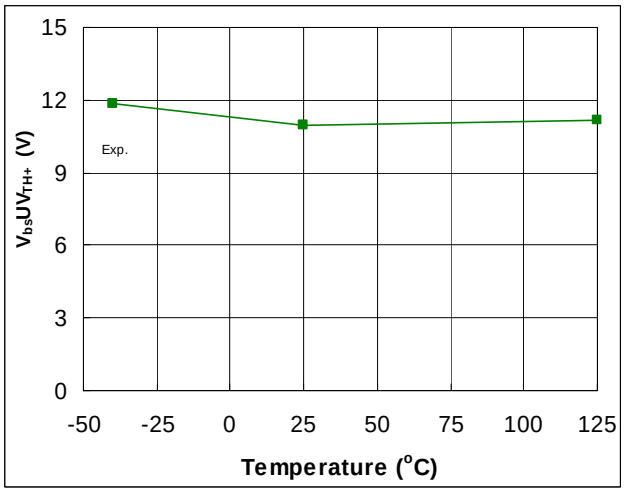


Fig. 41. VBS Supply Under-voltage Positive Going Threshold vs. Temperature

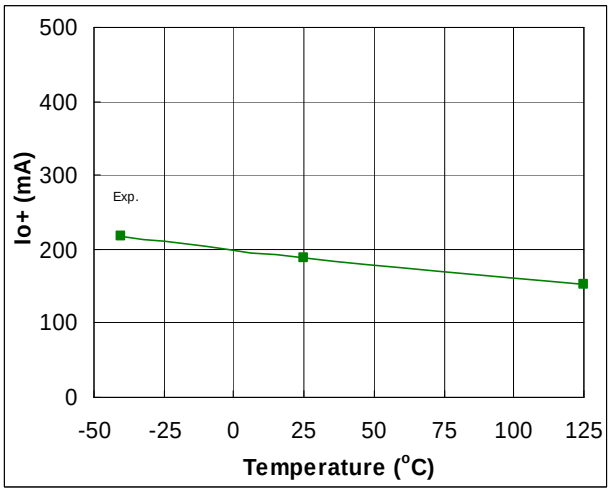


Fig. 42. Output High Short Circuit Pulsed Current vs. Temperature

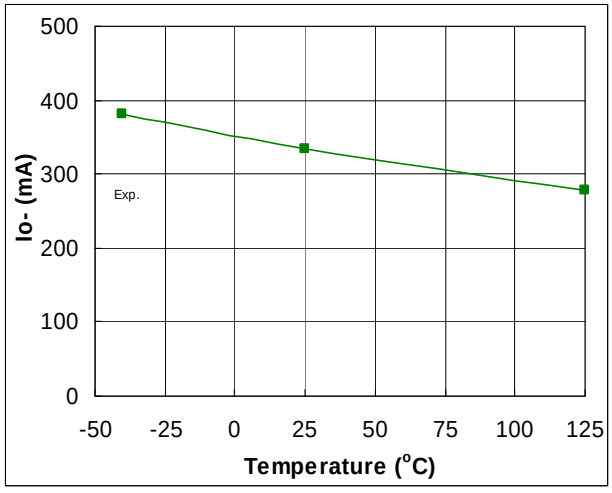


Fig. 43. Output Low Short Circuit Pulsed Current vs. Temperature

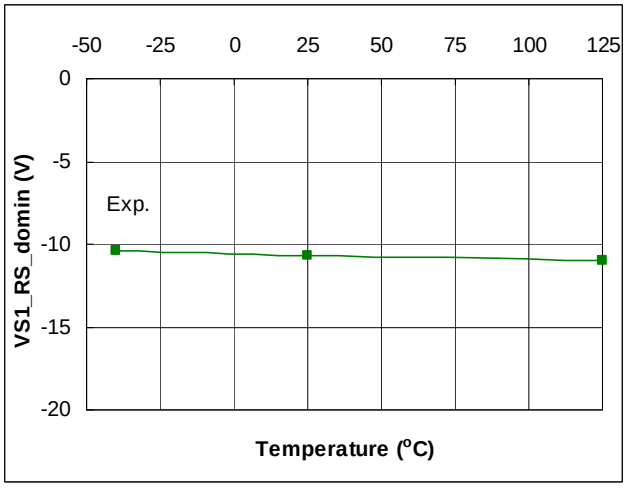
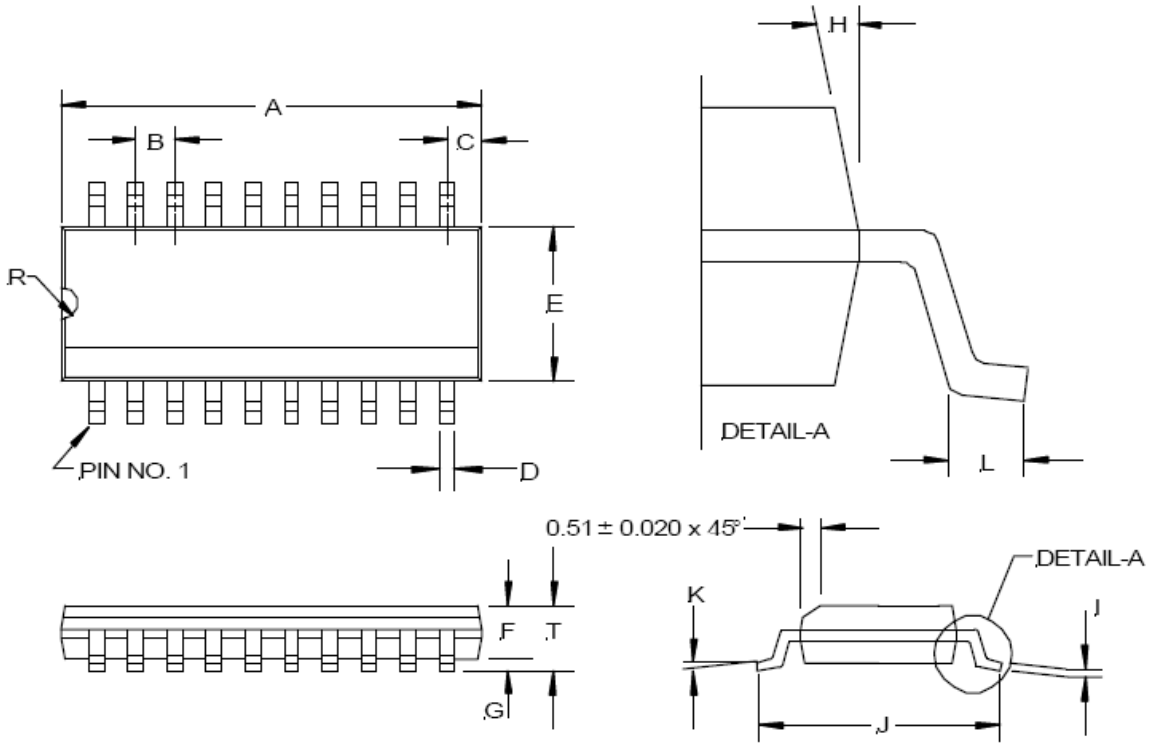


Fig. 44. Max –Vs vs. Temperature

Package Details

(W) SOIC Package
20-Pin Surface Mount, Wide Body

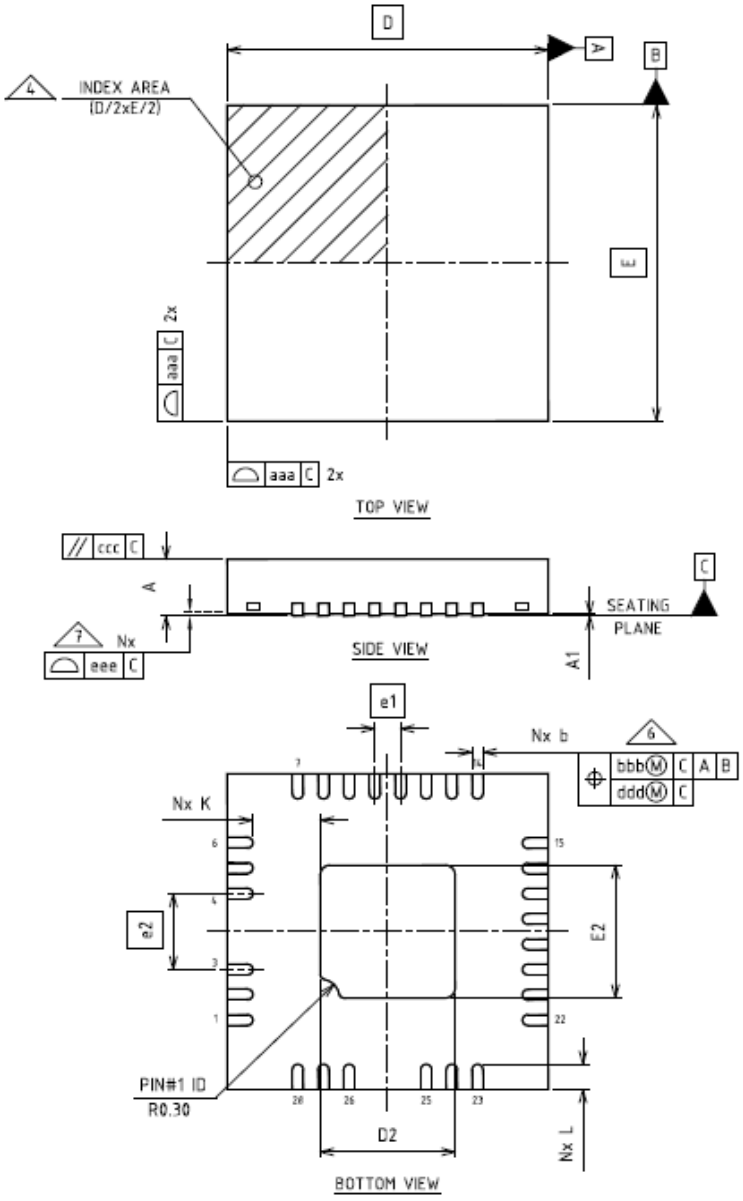


SYMBOL	20-PIN	
	MIN	MAX
A	12.598	12.979
B	1.018	1.524
C	0.66 REF	
D	0.33	0.508
E	7.40	7.60
F	2.032	2.64
G	0.10	0.30
I	0.229	0.32
J	10.008	10.654
K	0°	8°
L	0.406	1.270
R	0.63	0.89
T	2.337	2.642

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

Package Details

28 (32 – 4) lead MLPQ



Dimension Table				
Thickness / Symbol	V : Very Thin			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.15	0.20	0.25	6
D	5.00 BSC			
E	5.00 BSC			
e1	0.40 BSC			
e2	1.20 BSC			
D2	1.95	2.10	2.20	
E2	1.95	2.10	2.20	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa	0.05			
bbb	0.07			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	28			3
ND	8			5
NE	8			5
NOTES	1, 2			
LF PART NO	439034			
LF DWG. NO	CARSEM-S07004			
REV.	A			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

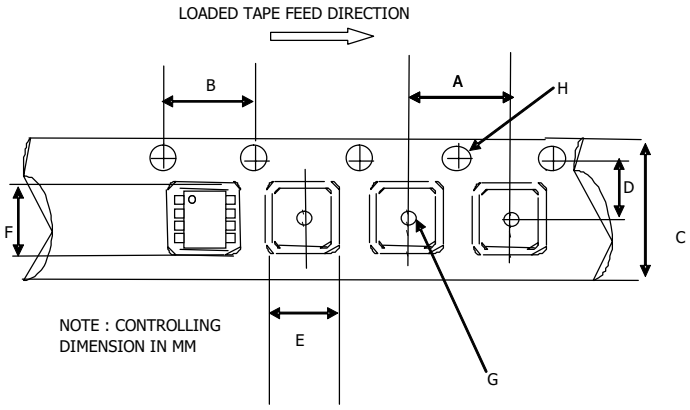
4. The location of the marked terminal #1 identifier is within the hatched.

5. ND and NE refer to the number of terminals on D and E side respectively.

6. Dimension b applies to the metallized terminal. If the terminal has a radius on its end, dimension b should not be measured in that radius area.

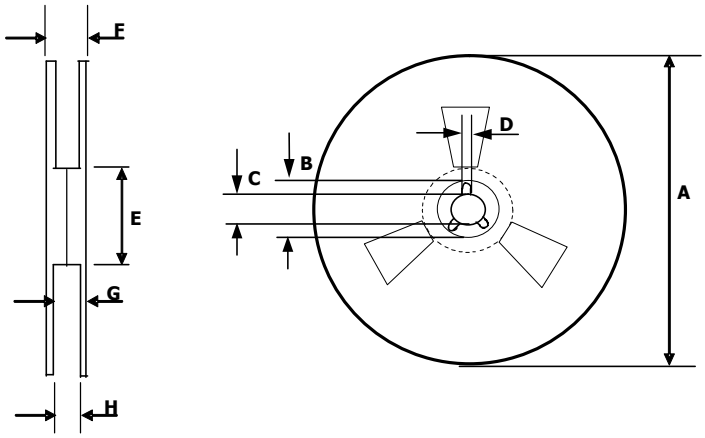
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Tape and Reel Details



CARRIER TAPE DIMENSION FOR 20SOICW

	Metric		Imperial	
Code	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	13.20	13.40	0.520	0.528
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

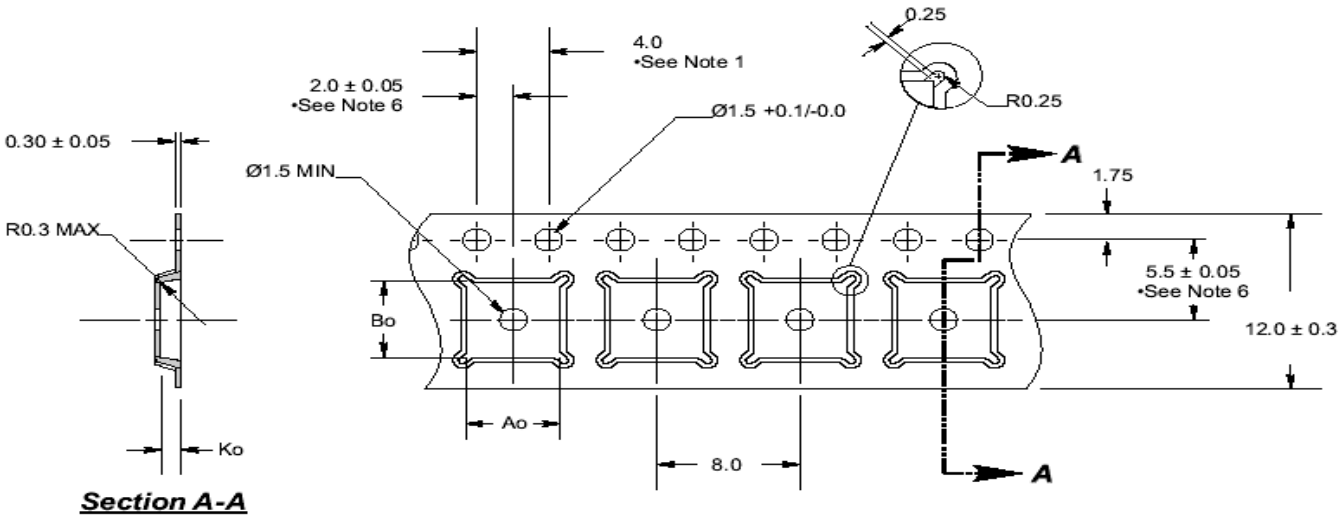


REEL DIMENSIONS FOR 20SOICW

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

Tape and Reel Details:

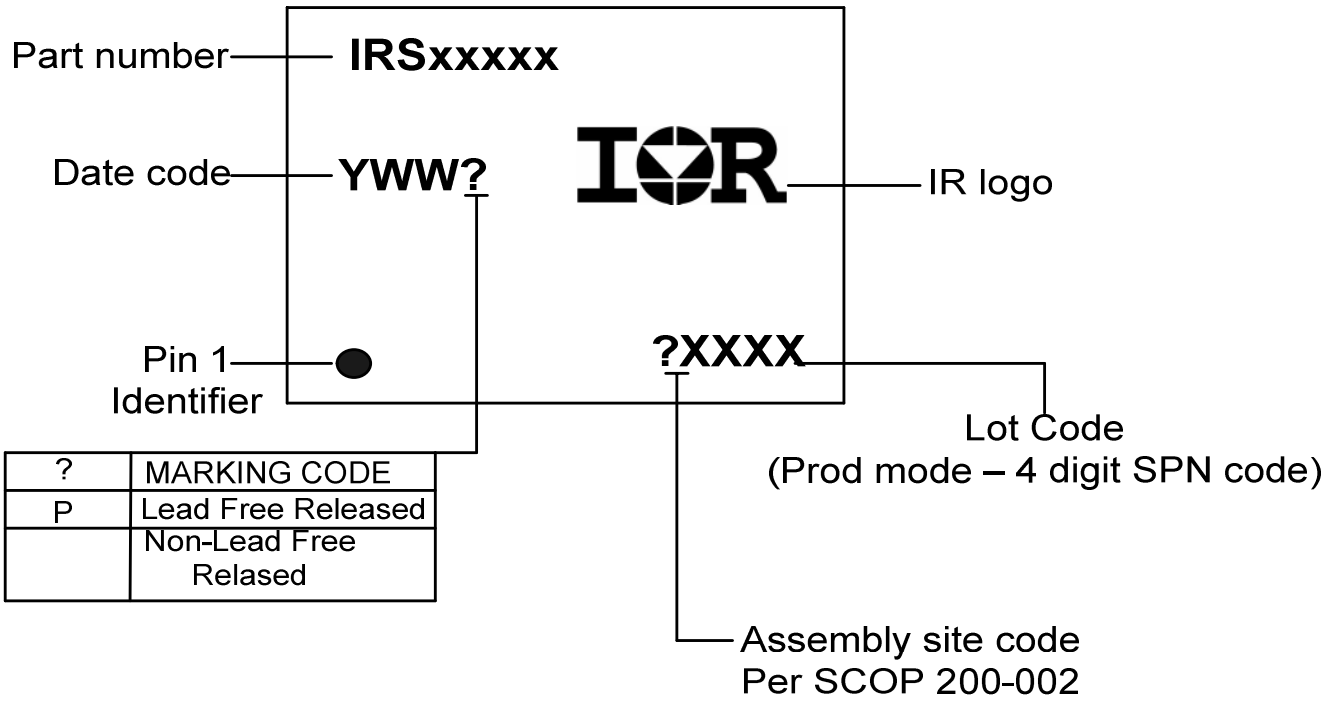
28 (32 – 4) lead MLPQ 5x5mm



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: PS + C.
4. Ao and Bo measured as indicated.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 5.25 mm
Bo = 5.25 mm
Ko = 1.1 mm

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2334	SOIC20W	Tube/Bulk	38	IRS2334 SPBF
		Tape and Reel	1000	IRS2334 STRPBF
	28L MLPQ 5x5mm (32 leads without 4)	Tray	624	IRS2334 MPBF
		Tape and Reel	3000	IRS2334 MTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

Revision	Date	Change comments
5.0	24 Jun 2009	Ramanan updated lead assignment, MLPQ 5x5 package information and Absolute Max Ratings to reflect 25V capability
5.1	30 Jun 2009	Updated: format, lead assignment, functional block diagram, Added: simplified block diagram, typical application diagram, qualification information, application details, parameters temperature trend, tape and reel detail, order information, revision history Removed: inputs internally clamped at 5.2V in static electrical characteristic
5.2	3 July 2009	Lead definition corrected, delay matching waveform definition figure added
5.3	Aug 2009	Package and tape & reel details for MLPQ 32-4 leads 5x5 added, package thermal parameters added
5.4	12 Nov 2009	Advanced input filter section added
5.5		TBD values in Static Electrical Characteristics updated
5.6	9 Dec 2009	Changed MM ESD rating from Class C to Class B
5.7	12 Mar 2010	Parameter limits updated: IQCC, IQBS, IIN+
5.8	02 Apr 2010	I_{o+}, I_{o-} values corrected
5.9	26 Jan 2011	Update temperature dependence tables, UVcc hyst corrected
5.10	31 Jan 2011	Include the IRS2334MPbF in the datasheet title
5.11	24 Apr 2012	Lead assignment drawing modified
5.13	22 Jan 2013	MLPQ package drawing updated

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