THE DATASHEET OF

IR21381QPBF

International
IOR Rectifier

Data Sheet PD60232 revC

IR22381QPBF/IR21381Q(PbF)

3-PHASE AC MOTOR CONTROLLER IC

Features

- Floating channel up to +600V or +1200V
- "soft" over-current shutdown turns off desaturated output
- Integrated desaturation circuit
- Active biasing on sensing desaturation input
- Two stage turn on output for di/dt control
- Integrated brake IGBT driver with protection
- Voltage feedback sensing function
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- Under voltage lockout with hysteresis band
- Programmable deadtime
- Hard shutdown function

Product Summary

V_{OFFSET} (max)	600V or 1200V
$I_{O+/-}$ (min.)	220mA / 460mA
V_{OUT}	12.5V-20V
Brake ($I_{O+/-}$ min.)	40mA/80mA
Deadtime Asymmetry Skew (max.)	125nsec
Deadtime (typ. with RDT=39KΩ)	1µsec
DESAT Blanking time (typ.)	4.5µsec
DESAT filter time (typ.)	3.0µsec
Active bias on Desat input pin	90Ω
DSH, DSL input voltage threshold (typ.)	8.0V
Soft shutdown duration time (typ.)	6.0µsec
Voltage feedback matching delay time (max.)	400nsec

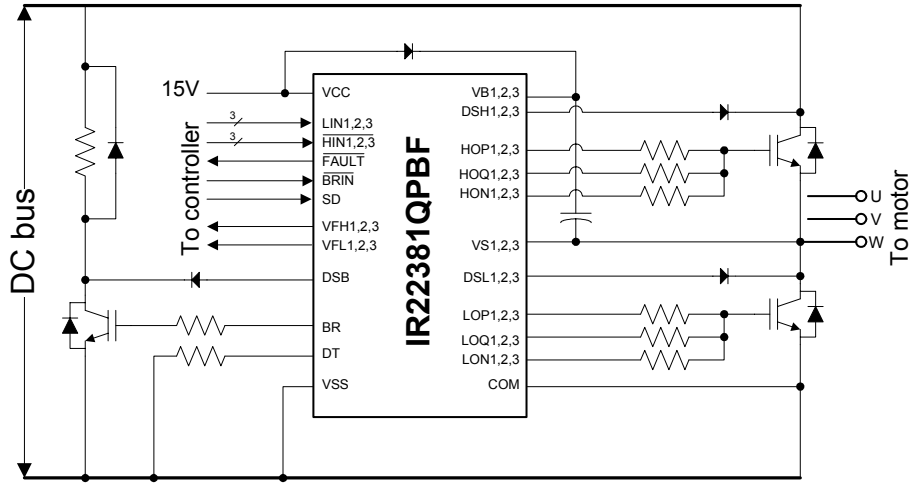
Package

64-Lead MQFP w/o 13 leads

Description

The IR22381Q and IR21381Q are high voltage, 3-phase IGBT driver best suited for AC motor drive applications. Integrated desaturation logic provides all mode of overcurrent protection, including ground fault protection. The sensing desaturation input is provided by active bias stage to reject noise. Soft shutdown is predominantly initiated in the event of overcurrent followed by turn-off of all six outputs. A shutdown input is provided for a customized shutdown function. The DT pin allows external resistor to program the deadtime. Output drivers have separate turn on/off pins with two stage turn-on output to achieve the desired di/dt switching level of IGBT. Voltage feedback provides accurate volt x second measurement.

Typical Connection



(Refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		$V_{B\,1,2,3}$ - 25	$V_{B\,1,2,3}$ + 0.3	V
V_B	High side floating supply voltage	(IR22381)	-0.3	1225	
		(IR21381)	-0.3	625	
V_{HO}	High side floating output voltage (HOP, HON, HOQ)		$V_{S1,2,3}$ - 0.3	$V_{B\,1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
COM	Power ground		V_{CC} - 25	V_{CC} + 0.3	
V_{LO}	Low side output voltage (LOP, LON, LOQ)		V_{COM} -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN/N, LIN, BRIN/N, SD)		-0.3	V_{CC} + 0.3 or V_{SS} +15 Which ever is lower	
V_{FLT}	FAULT/N output voltage		-0.3	V_{CC} + 0.3	
V_F	Feedback output voltage		-0.3	V_{CC} + 0.3	
V_{DSH}	High side desat/feedback input voltage		$V_{B\,1,2,3}$ - 25	$V_{B\,1,2,3}$ + 0.3	
V_{DSL}	Low side desat/feedback input voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{BR}	Brake output voltage		V_{COM} -0.3	V_{CC} + 0.3	
dVs/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C		—	2.0	W
R_{thJA}	Thermal resistance, junction to ambient		—	60	°C/W
T_J	Junction temperature		—	125	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS}. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition		Min.	Max.	Units
$V_{B\,1,2,3}$	High side floating supply voltage (Note 1)		$V_{S1,2,3}$+12.5	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage	(IR21381)	Note 2	600	
		(IR22381)	Note 2	1200	
$V_{HO\,1,2,3}$	High side (HOP/HOQ/HON) output voltage		$V_{S1,2,3}$	$V_{S1,2,3}$ + V_B	
$V_{LO1,2,3}$	Low side (LOP/LOQ/LON) output voltage		V_{COM}	V_{CC}	
V_{IN}	Logic input voltage (HIN/N, LIN, BRIN/N SD)		0	V_{SS} + 5	
V_{CC}	Low side supply voltage (Note 1)		12.5	20	
COM	Power ground		- 5	+ 5	
V_{FLT}	FAULT/N output voltage		0	V_{CC}	
V_F	Feedback output voltage		0	V_{CC}	
V_{DSH}	High side desat/feedback input voltage		$V_{B\,1,2,3}$ - 20	$V_{B\,1,2,3}$	
V_{DSL}	Low side desat/feedback input voltage		V_{CC} - 20	V_{CC}	
V_{BR}	BR output voltage		V_{COM}	V_{CC}	
T_A	Ambient temperature		-40	115	°C

Note 1: While internal circuitry is operational below the indicated supply voltages, the UV lockout disables the output drivers if the UV thresholds are not reached.

Note 2: Logic operational for V_S from V_{SS}-5V to V_{SS}+600V (IR21381) or 1200V (IR22381). Logic state held for V_S from V_{SS}-5V to V_{SS}-V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V and T_A = 25 °C unless otherwise specified.
I/O diagrams don't show ESD protection circuits.

Pin: V_{CC}, V_{SS}, V_B, V_S

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{cc1} supply undervoltage positive going threshold	10.3	11.2	12.5	V	
V_{CCUV-}	V_{cc1} supply undervoltage negative going threshold	9.5	10.2	11.3		
V_{CCUVH}	V_{cc1} supply undervoltage lockout hysteresis	-	1.0	-		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.3	11.2	11.9		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.2	10.9		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	-	1.0	-		
I_{LK}	Offset supply leakage current (IR21381Q)	-	-	50	µA	$V_{B1,2,3}$ =$V_{S1,2,3}$ = 600V
	Offset supply leakage current (IR22381Q)	-	-	50		$V_{B1,2,3}$ =$V_{S1,2,3}$ = 1200V
I_{QBS}	Quiescent V_{BS} supply current	-	150	300		V_{LIN}=0V,V_{HIN}=5V, $DSH_{1,2,3}$= $V_{S1,2,3}$
I_{QCC}	Quiescent Vcc supply current	-	3	6	mA	V_{LIN}=0V,V_{HIN}=5V DT=1µsec

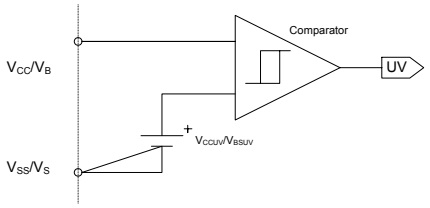


Figure 1: Undervoltage diagram

Pin: HIN/N, LIN, BRIN/N, SD

The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HOP/HOQ/ $HON_{1,2,3}$ and LOP/LOQ/$LON_{1,2,3}$).

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "0" input voltage (HIN/N, LIN, BRIN/N, SD)(OUT=LO)	2.0	-	-	V	V_{CC} = 12.5V to 20V
V_{IL}	Logic "1" input voltage (HIN/N, LIN, BRIN/N, SD)(OUT=HI)	-	-	0.8		
V_{t+}	Logic input positive going threshold (HIN/N, LIN, BRIN/N, SD)	1.2	1.6	2.0		
V_{t-}	Logic input negative going threshold (HIN/N, LIN, BRIN/N, SD)	0.8	1.2	1.6		
ΔV_T	Logic input hysteresis(HIN/N, LIN, BRIN/N, SD)	-	0.4	-		
I_{IN+}	Logic "1" input bias current (HIN/N, BRIN/N)	-2	-	0	µA	V_{IN} = 0V
	Logic "1" input bias current (LIN, SD)	-	85	140		V_{IN} = 5V
I_{IN-}	Logic "0" input bias current (HIN/N, BRIN/N)	-	85	140		V_{IN} = 5V
	Logic "0" input bias current (LIN, SD)	-2	-	0		V_{IN} = 0V

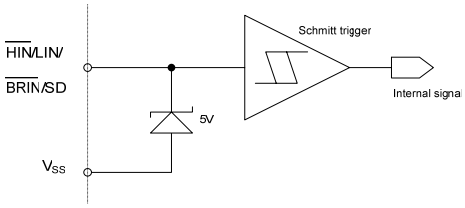


Figure 2: HIN/N, LIN and BRIN/N diagram

Pin: FAULT/N, VFH, VFL

V_{OLVF} is referenced to V_{ss}

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OLVF}	VFH or VFL low level output voltage	-	-	0.8	V	I_{VF} = 10mA
$R_{ON,VF}$	VFH or VFL output on resistance	-	60	-	Ω	
$R_{ON,FLT}$	FAULT/N low on resistance	-	60	-		

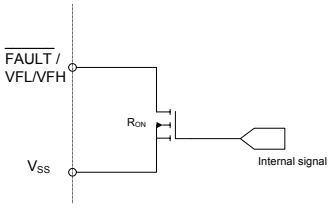


Figure 3: FAULT/N, VFH, VFL diagram

Pin: DSL, DSH, DSB

V_{DESAT} and I_{DESAT} parameters are referenced to COM and $V_{S1,2,3}$

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{DESAT+}	High $DSH_{1,2,3}$ and $DSL_{1,2,3}$ and DSB input threshold voltage	-	8.0	-	V	
VDESAT-	Low $DSH_{1,2,3}$ and $DSL_{1,2,3}$ or DSB input threshold voltage	-	7.0	-		
V_{DSTH}	DS input voltage hysteresis	-	1.0	-		
I_{DS+}	High DSH, DSL, DSB input bias current	-	15	-	µA	V_{DESAT} = 15V
I_{DS-}	Low DSH, DSL input bias current	-	-150	-		V_{DESAT} = 0V
I_{DSBR-}	Low DSB input bias current	-	-250	-		V_{DESAT} = 0V
I_{DSB}	DSH or DSL input bias current	-	-11.1	-	mA	V_{DESAT} = (V_{CC} or V_{BS}) – 1V

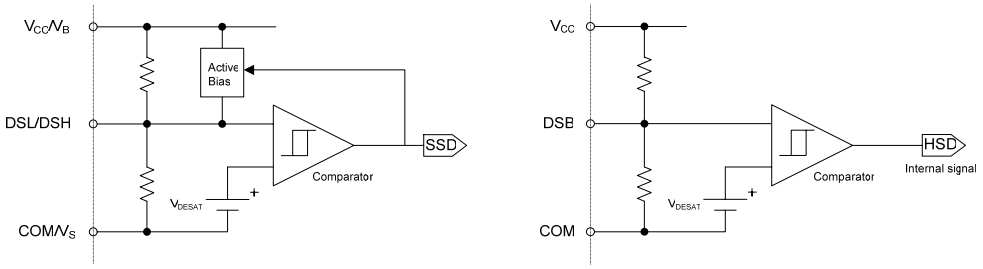


Figure 4: DSH, DSL and DSB diagram

Pin: HOP, LOP, HOQ, LOQ

The V_O and I_O parameters are referenced to COM and $VS_{1,2,3}$ and are applicable to the respective output leads: $HO_{1,2,3}$ and $LO_{1,2,3}$.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OH}	High level output voltage, V_{BIAS} – V_O (normal switching). HOP=HOQ, LOP=LOQ.	-	-	2	V	I_O = -20mA
I_{O1+}	Output high first stage short circuit pulsed current. HOP=HOQ, LOP=LOQ	200	350	-	mA	V_O=0V, V_{IN}=1 (Note 1) PW≤t_{on1} Figure 16
I_{O2+}	Output high second stage short circuit pulsed current. HOP=HOQ, LOP=LOQ	100	200	-		V_O=0V, V_{IN}=1 (Note 1) PW≤10µs

Note 1: for HOx → HINx/N = 0V, for LOx → LIN = 5V

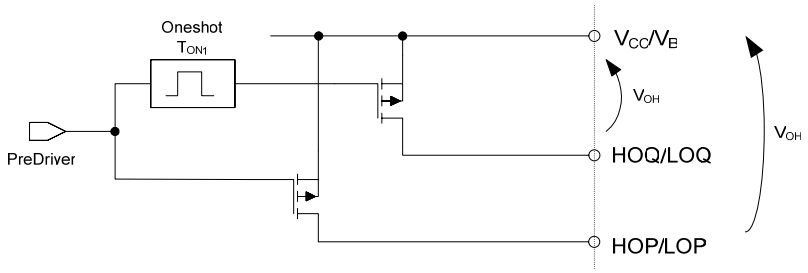


Figure 5: HOP/HOQ and LOP/LOQ diagram

Pin: HON, LON, SSDH, SSDL

The V_O and I_O parameters are referenced to COM and $VS_{1,2,3}$ and are applicable to the respective output leads: $HO_{1,2,3}$ and $LO_{1,2,3}$.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OL}	Low level output voltage, V_O (normal switching) HON, LON	-	-	2	V	I_O = 20mA
$R_{ON,SS}$	Soft shutdown on resistance (see Note 2)	-	500	-	Ω	PW ≤ t_{SS}
I_{O-}	Output low short circuit pulsed current	250	540	-	mA	V_O=15V, V_{IN}=0 (Note 3) PW≤10µs

Note 2: SSD operation only
Note 3: for HOx → HINx/N = 5V, for LOx → LIN = 0V

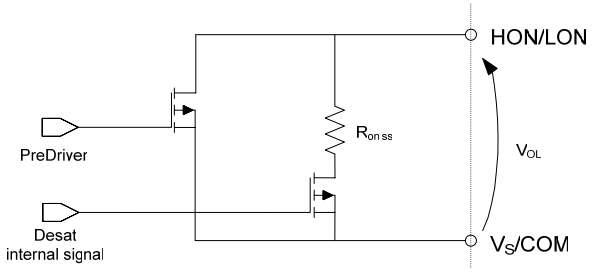


Figure 6: HON, LON diagram

Pin: BR

The V_O and I_O parameters are referenced to COM and are applicable to BR output .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{OHB}	BR high level output voltage, V_{CC}- V_{BR}	-	-	6	V	I_{BR} = -20mA
V_{OLB}	BR low level output voltage, V_{BR}	-	-	3		I_{BR} = 20mA
I_{OBR+}	BR output high short circuit pulsed current	40	70	-	mA	V_{BR}=15V, $V_{BRIN/N}$=0V PW≤10µs
I_{OBR-}	BR output low short circuit pulsed current	80	125	-		V_{BR}=0V, $V_{BRIN/N}$=5V PW≤10µs

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, $VS_{1,2,3}$ =V_{SS}, T_A = 25 °C and CL= 1000pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Characteristics						
t_{on1}	Turn-on first stage duration time	—	200	—	ns	VIN = 0 & 5V RL(HOQ/LOQ)=10Ω
t_{on}	Turn-on propagation delay	250	550	750		VIN = 0 & 5V $VS_{1,2,3}$ = 0 to 600 or 1200V HOP=HON,LOP=LON Figure 7
t_{off}	Turn-off propagation delay	250	550	750		
t_r	Turn-on rise time	—	80	—		
t_f	Turn-off fall time	—	25	—		
t_{DESAT1}	DSH to HO soft shutdown propagation delay at HO turn-on	—	4500	—		VHIN = 0V, VDESAT = 15V, Figure 11
t_{DESAT2}	DSH to HO soft shutdown propagation delay after blanking	—	3000	—		
t_{DESAT3}	DSL to LO soft shutdown propagation delay at LO turn-on	—	4500	—		VLIN = 5V VDESAT = 15V, Figure 11
t_{DESAT4}	DSL to LO soft shutdown propagation delay after blanking	—	3000	—		
t_{DESAT5}	DSB to HO hard shutdown propagation delay	—	3300	—		VHIN = 0V, VDESAT = 15V, Figure 11
t_{DESAT6}	DSB to LO hard shutdown propagation delay	—	3300	—		VLIN = 5V VDESAT = 15V, Figure 11
t_{DESAT7}	DSB to BR hard shutdown propagation delay	—	3000	—		VBRIN = 0V VDSB = 15V, Figure 11
$t_{VFHL1,2,3}$	VFH high to low propagation delay	—	550	—		VDESAT = 15V to 0V Figure 12
$t_{VFHHL1,2,3}$	VFH low to high propagation delay	—	550	—		VDESAT = 0V to 15V Figure 12
$t_{VFLH1,2,3}$	VFL low to high propagation delay	—	550	—		VDESAT = 0V to 15V Figure 12
$t_{VFLL1,2,3}$	VFL high to low propagation delay	—	550	—		VDESAT = 15V to 0V Figure 12
t_{PWVF}	Minimum pulse width of VFH and VFL	—	400	—		VDESAT = 15V to 0V or 0V to 15V Figure 12

AC Electrical Characteristics cont.

V_{BIAS} (V_{CC}, V_{BS}) = 15V, $V_{S1,2,3}$ = V_{SS}, T_A = 25 °C and C_L = 1000pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Characteristics cont.						
t_{DS}	Soft shutdown minimum pulse width of desat	—	3000	—	ns	CL=1000pF, V_{DS}=15V Figure 8-9
t_{SS}	Soft shutdown duration period	—	6000	—		V_{HIN} = 0V, V_{DS}=15V, Figure 11
$t_{FLT,DESAT1}$	DSH to FAULT propagation delay at HO turn-on	—	4800	—		
$t_{FLT,DESAT2}$	DSH to FAULT propagation delay after blanking	—	3300	—		V_{LIN} = 5V, V_{DS}=15V, Figure 11
$t_{FLT,DESAT3}$	DSL to FAULT propagation delay at LO turn-on	—	4500	—		
$t_{FLT,DESAT4}$	DSL to FAULT propagation delay after blanking	—	3000	—		
t_{FLTDSB}	DSB to FAULT propagation delay	—	3000	—		$V_{BRIN/N}$ = 0V V_{DESAT} = 15V, Figure 11
t_{FLTCLR}	LIN1=LIN2=LIN3=0 to FAULT	9.0	—	—	µs	V_{DESAT}=15V, Figure 11
t_{fault}	Minimum FAULT duration period	9.0	15.0	21.0		V_{DESAT}=15V, Figure 15 FLTCLR pending
t_{BL}	DS blanking time at turn on	—	4500	—	ns	V_{IN} = on V_{DESAT}=15V, Figure 11
t_{SD}	SD to output shutdown propagation delay	—	600	900		V_{IN} = on V_{DESAT}=0V, Figure 14
t_{EN}	SD disable propagation delay	—	600	900		V_{IN} = on V_{DESAT}=0V, Figure 14
t_{onBR}	BR output turn-on propagation	—	110	200		Figure 7
t_{offBR}	BR output turn-off propagation	—	125	200		
t_{rBR}	BR output turn-on rise time	—	235	400		
t_{fBR}	BR output turn-off fall time	—	130	250		
Dead-time/Delay Matching Characteristics						
DT	Deadtime	800	1000	1200	ns	Figure 12, External resistor=39kΩ
		76	100	124		Figure 12,External resistor=0kΩ
		4500	5000	5500		Figure 12, External resistor=220kΩ
MDT	Deadtime asymmetry skew, any of $DTL_{off1,2,3}$-$DTH_{off1,2,3}$	—	—	125		DT=1000ns Figure 12
PM	PWM propagation delay matching max {ton/toff} -min {ton/toff}, (ton/toff are applicable to all six channels)	—	—	125		DT=1000ns Figure 12
VM	Voltage feedback delay matching, I any of $t_{VFHL1,2,3}$, $t_{VFHHL1,2,3}$, $t_{VFLL1,2,3}$, $t_{VFLH1,2,3}$ - any of $t_{VFHL1,2,3}$, $t_{VFHHL1,2,3}$, $t_{VFLL1,2,3}$, $t_{VFLH1,2,3}$	—	—	400		Input pulse width >400nsec, Figure 13

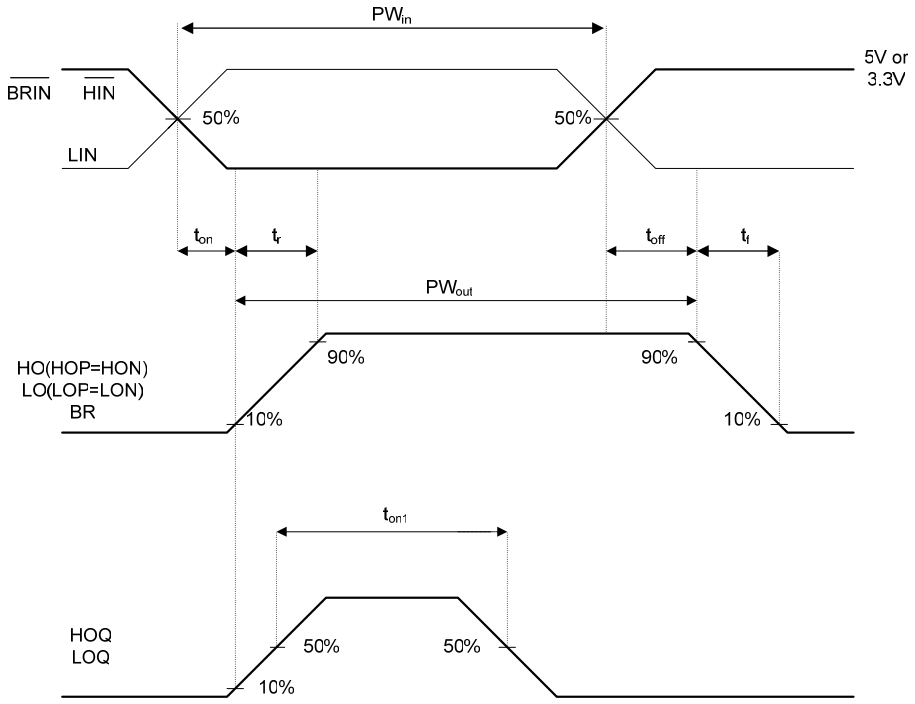


Figure 7: Switching Time Waveforms

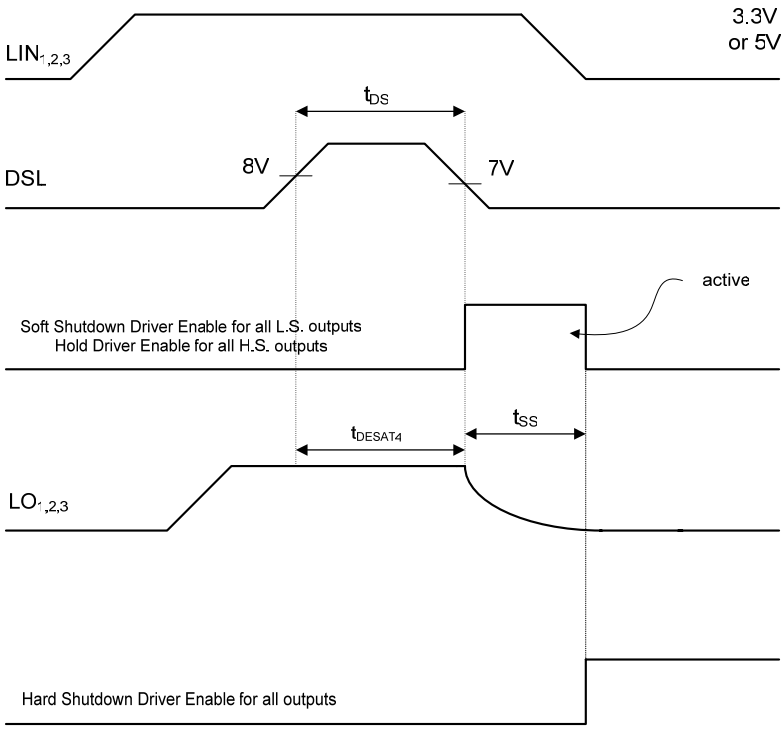


Figure 8: Low Side Desat Soft Shutdown Timing Waveform

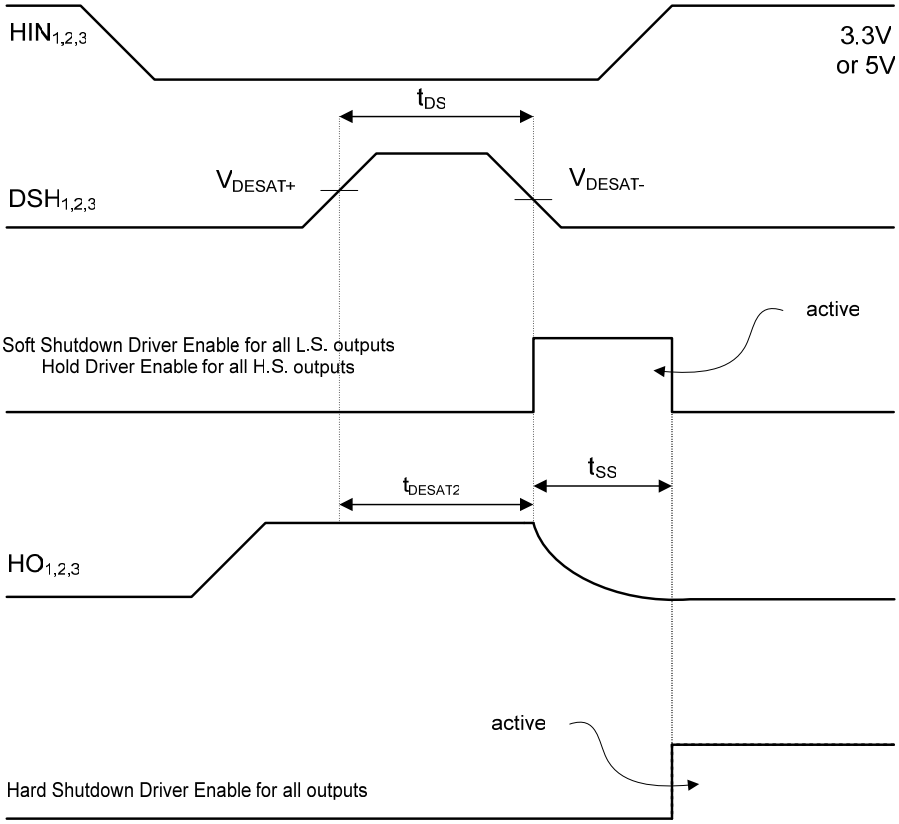


Figure 9: High Side Desat Soft Shutdown Timing Waveform

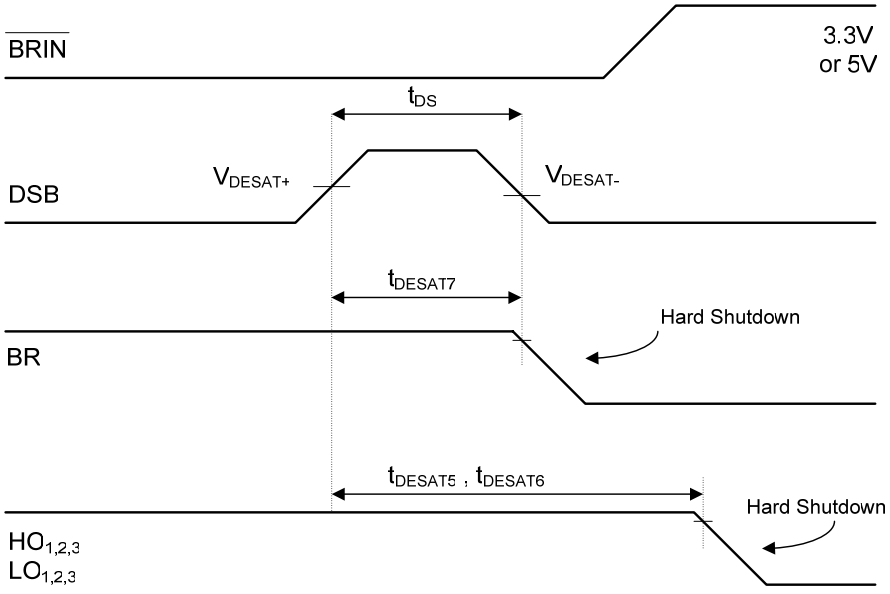


Figure 10: Brake Desat Timing Waveform

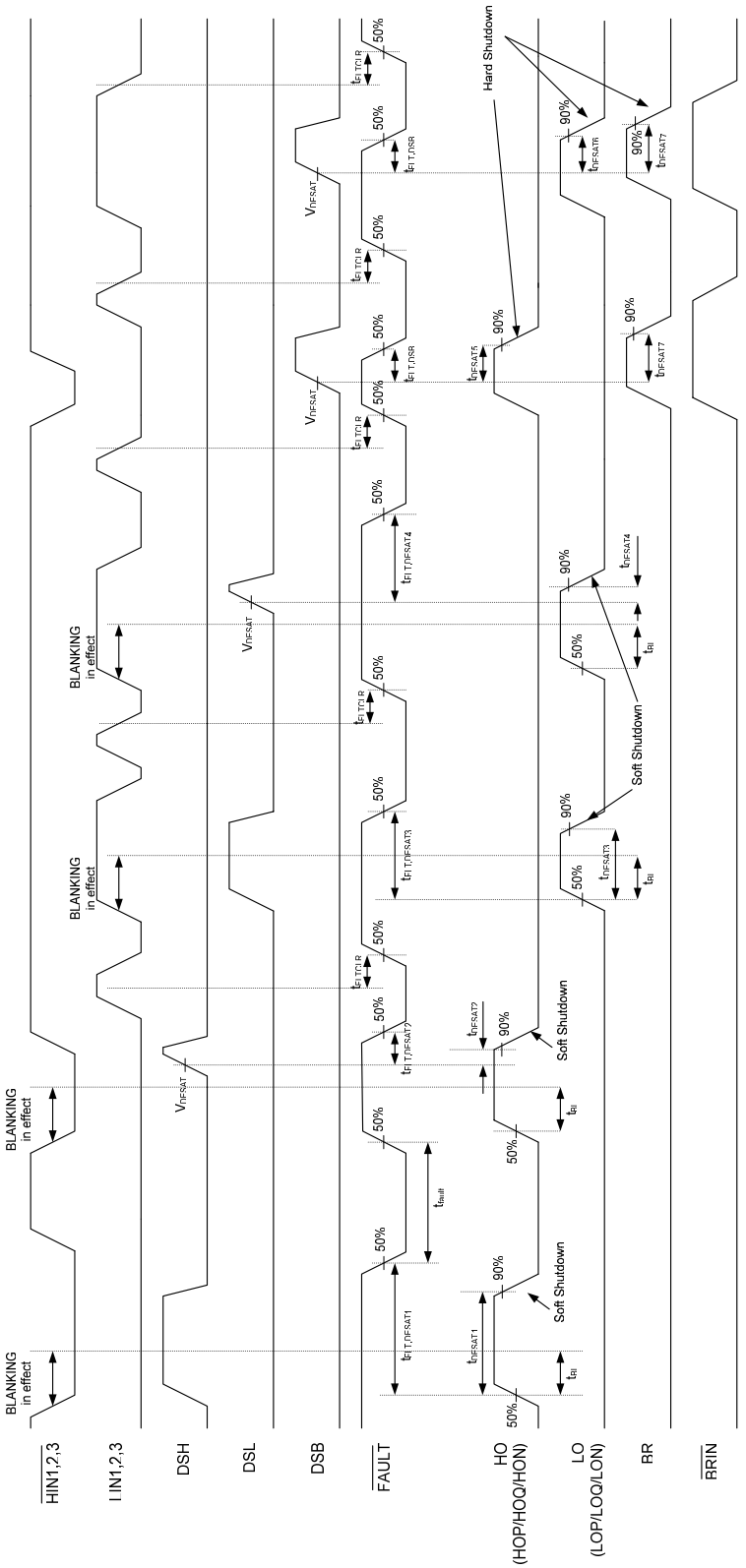


Figure 11: Desat Timing Diagram

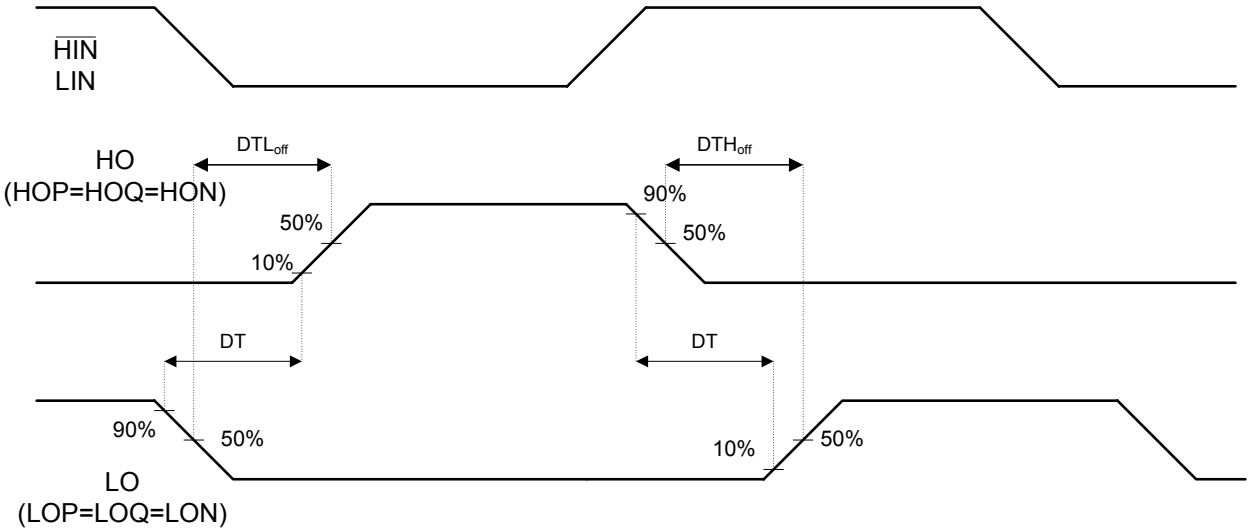


Figure 12: Internal Dead-Time Timing

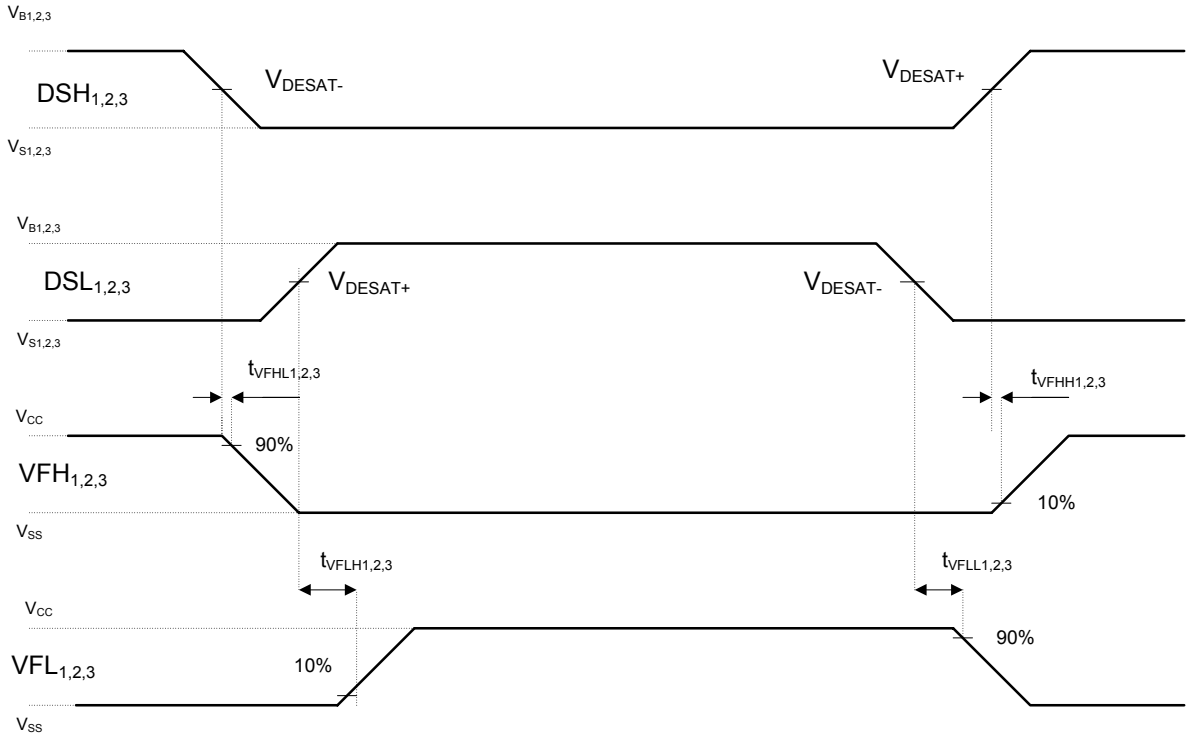


Figure 13: Voltage Feedback Timing

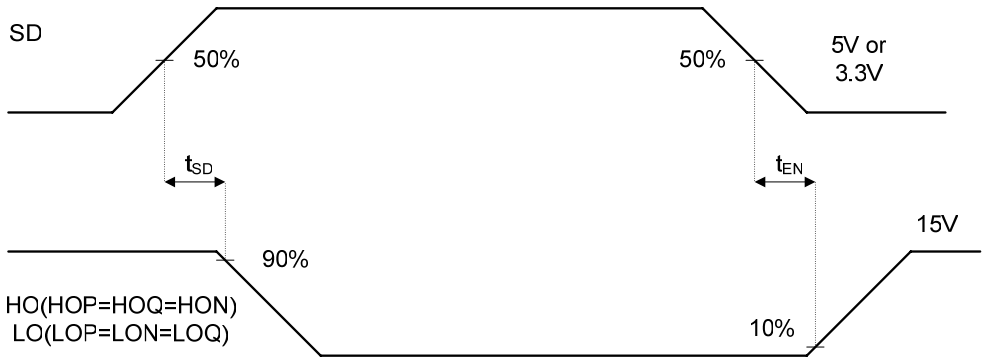


Figure 14: Shutdown Timing

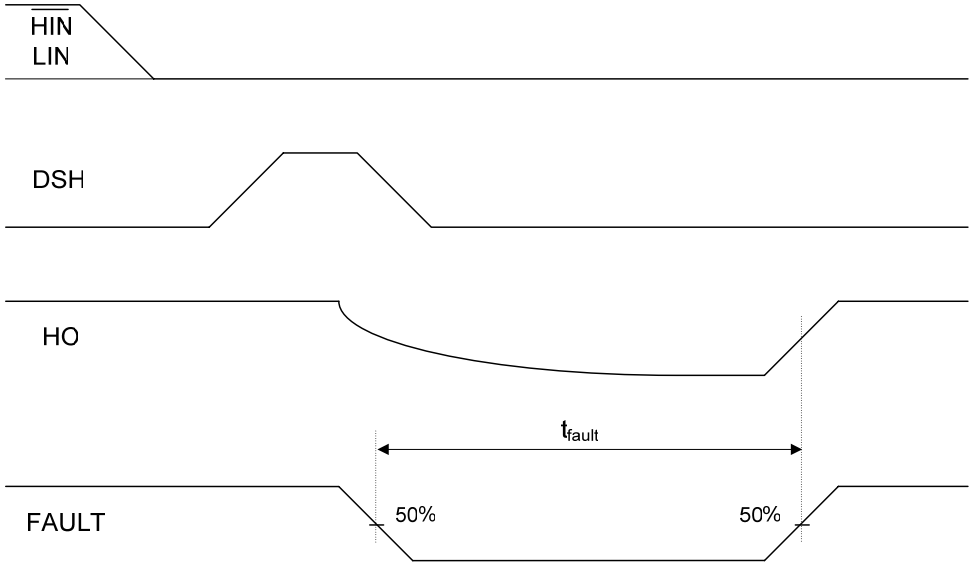


Figure 15: Fault Duration with Pending Faultclear Waveform
(See paragraph 1.4.5 on page 21)

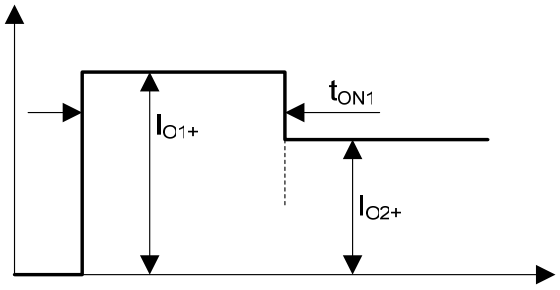


Figure 16: Output source current

Lead Assignments

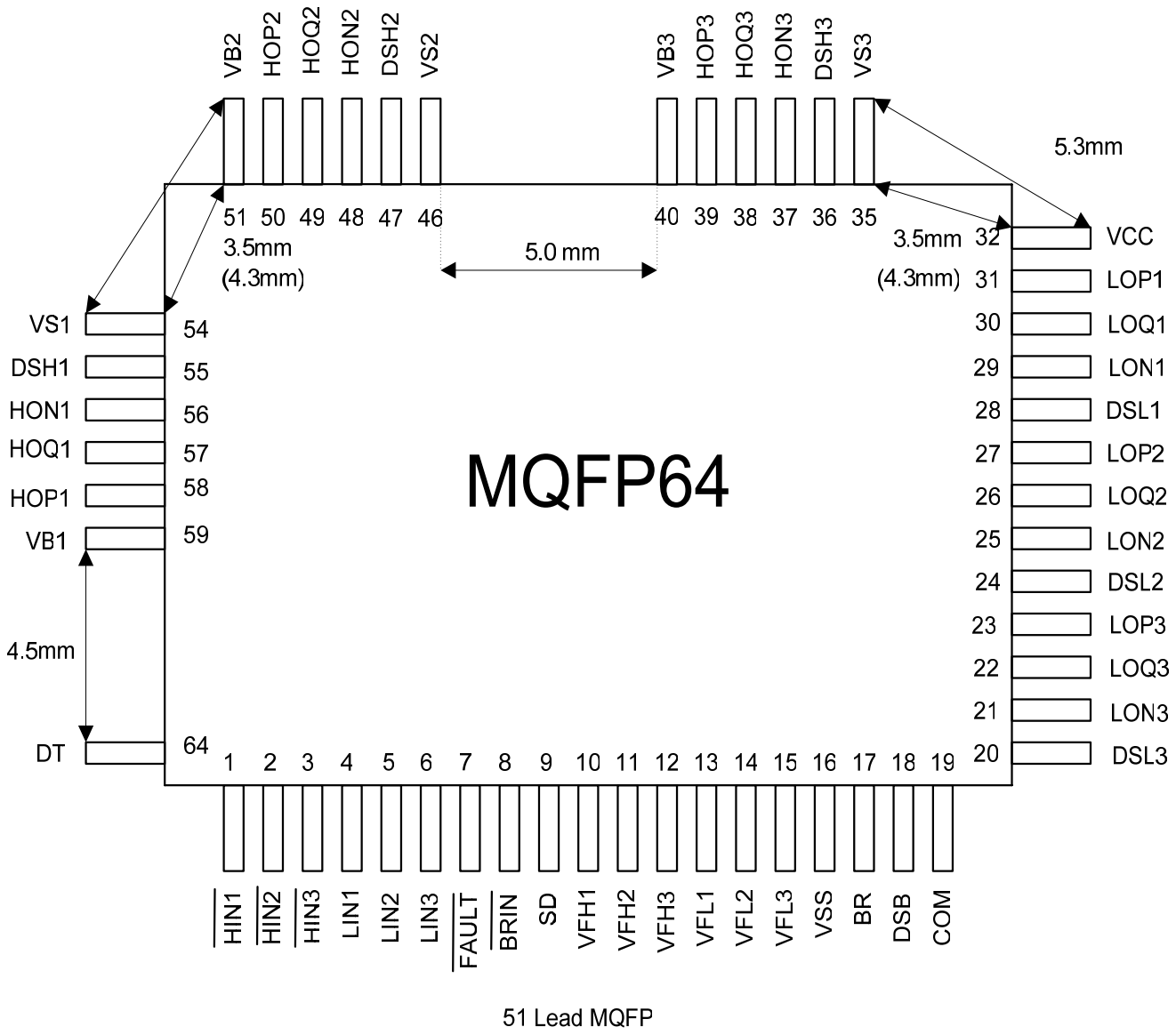


Figure 17: Package pin out

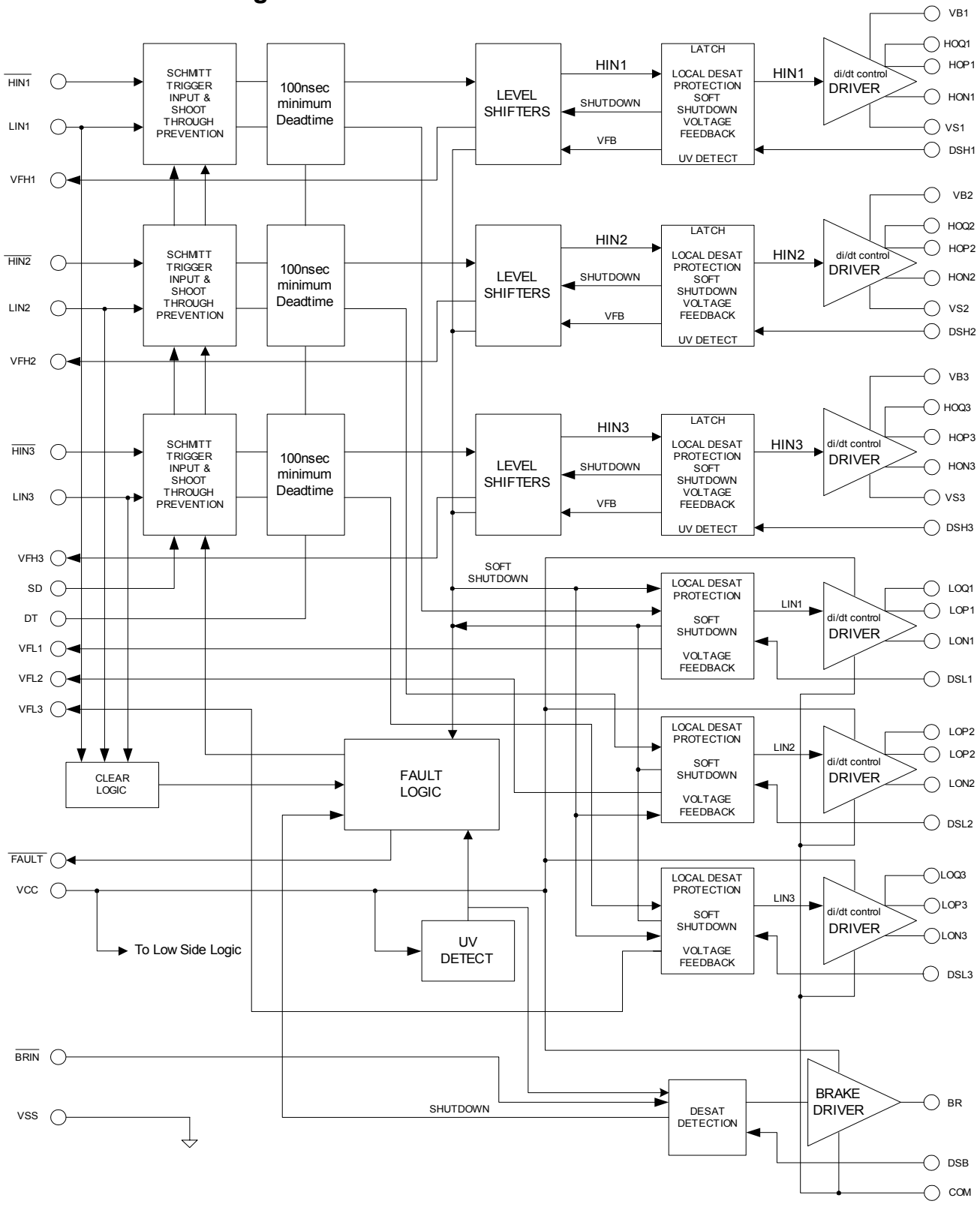
Lead Definitions

Symbol	Description
V_{CC}	Low side supply voltage
V_{SS}	Logic Ground
$HIN_{1,2,3}$ /N	Logic inputs for high side gate driver outputs ($HOP_{1,2,3}$/$HOQ_{1,2,3}$/$HON_{1,2,3}$)
$LIN_{1,2,3}$	Logic input for low side gate driver outputs ($LOP_{1,2,3}$/$LOQ_{1,2,3}$/$LON_{1,2,3}$)
FAULT/N	Fault output (latched and open drain)
SD	Shutdown input
DT	Programmable deadtime resistor pin
DSB	Brake IGBT desaturation protection input
BRIN/N	Logic input for brake driver

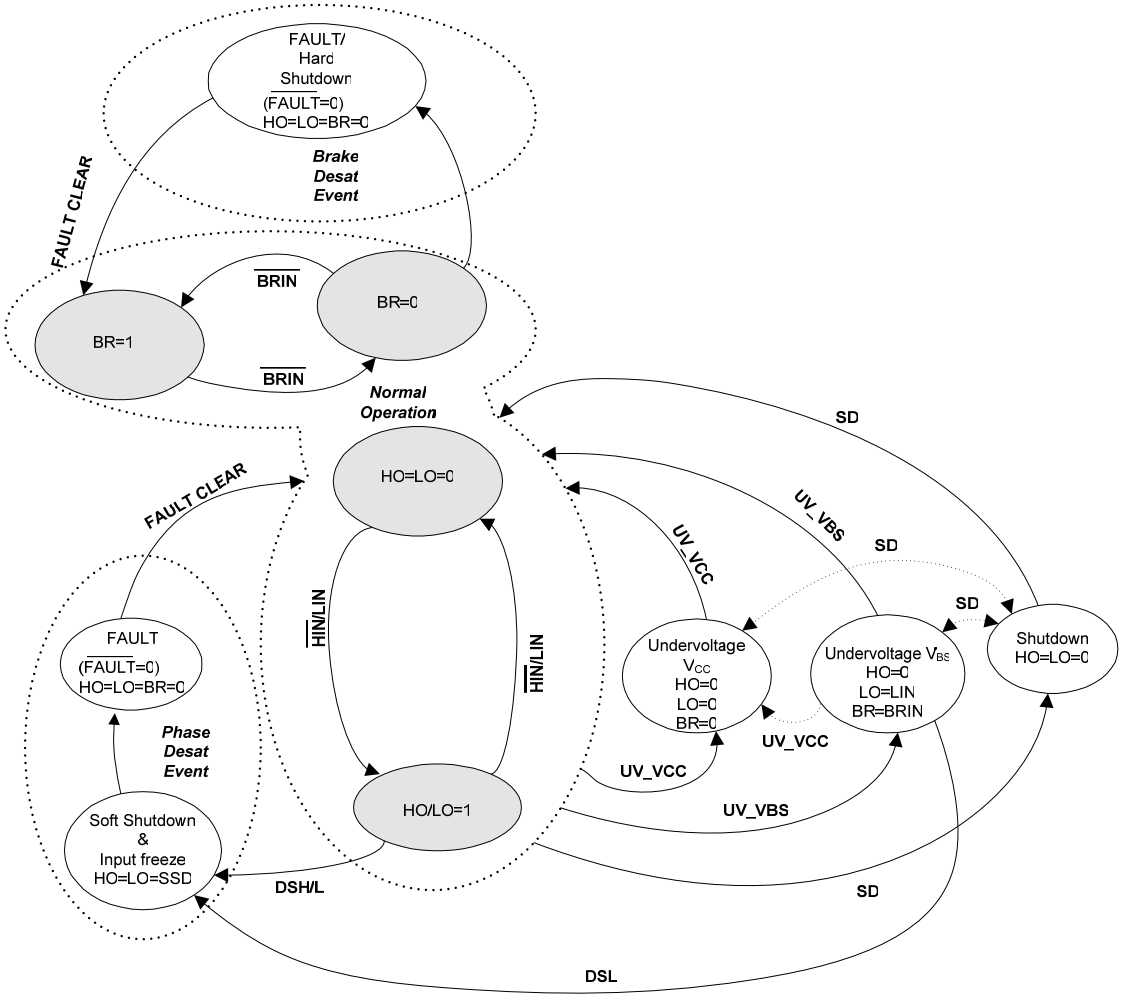
Lead Definitions continued

Symbol	Description
BR	Brake driver output
COM	Brake and Low side drivers return
$VB_{1,2,3}$	High side gate driver floating supply
$HOP_{1,2,3}$	High side driver sourcing output
$HOQ_{1,2,3}$	High side driver boost sourcing output
$HON_{1,2,3}$	High side driver sinking output
$DSH_{1,2,3}$	IGBT desaturation protection input and high side voltage feedback input (see par. 1.4.3 on page 19)
$VS_{1,2,3}$	High voltage floating supply return
$LOP_{1,2,3}$	Low side driver sourcing output
$LOQ_{1,2,3}$	Low side driver boost sourcing output
$LON_{1,2,3}$	Low side driver sinking output
$DSL_{1,2,3}$	IGBT desaturation protection input and low side voltage feedback input (see par. 1.4.3 on page 19)
$VFH_{1,2,3}$	High side voltage feedback logic output
$VFL_{1,2,3}$	Low side voltage feedback logic output

Functional block diagram



State diagram



Stable States

- FAULT
- Normal operation
- UNDERVOLTAGE V_{CC}
- SHUTDOWN (SD)
- UNDERVOLTAGE V_{BS}

Temporary States

- SOFT SHUTDOWN

System Variables

- FAULT CLEAR indicates: LIN1=LIN2=LIN3=0
- HIN/N /LIN/BRIN/N
- UV_VCC
- UV_VBS
- DSH/L, DSB
- SD

NOTE 1: a change of logic value of the signal labeled on lines (system variable) generates a state transition.
NOTE 2: Exiting from UNDERVOLTAGE V_{BS} state, the HO goes high only if a falling edge event happens in HIN/N.

Logic Table

Output drivers status description

HO/LO/BR status	HOP/LOP	HOQ/LOQ	HON/LON	BR
0	HiZ	HiZ	0	0
1	1	1 (after t_{on1})	HiZ	1
SSD	HiZ	HiZ	SSD pull-down	N/A
LO/HO/BR	Output follows inputs			

	INPUTS				OUTPUT	Under Voltage		Driver OUTPUTS		
Operation	**HIN/N**	**LIN**	**BRIN/N**	**SD**	**FAULT/N**	**VCC**	**VBS**	**HO**	**LO**	**BR**
Normal Operation	0	0	BRIN/N	0	1	No	No	1	0	BR
	1	1	BRIN/N	0	1	No	No	0	1	BR
	1	0	BRIN/N	0	1	No	No	0	0	BR
Anti Shoot Through	0	1	BRIN/N	0	1	No	No	0	0	BR
Shut Down	X	X	BRIN/N	1	1	X	X	0	0	BR
Under Voltage	X (**NOTE1**)	LIN	BRIN/N	0	1	No	Yes	0	LO	BR
	X	X	X	0	1	Yes	X	0	0	0
Soft SD (after DSL/H)	X	X	BRIN/N	X	1	No	No	SSD	SSD	BR
Hard SD (after DSB)	X	X	X	X	0	No	No	0	0	0
FAULT	X	X (**NOTE2**)	X	X	0	No	No	0	0	0
Fault Clear	X →HIN/N	LIN1= LIN2= LIN3= 0	BRIN/N	X	↓ (after t_{FLTCLR})	No	No	0 → HO	0	BR

NOTE1: Unless in Anti Shoot Through condition.
NOTE2: FAULT duration is at least t_{fault} when LIN1=LIN2=LIN3=0. Device stays in FAULT condition in all other cases.

Timing and logic state diagrams description

The following picture (Figure 18) shows the input/output logic diagram.

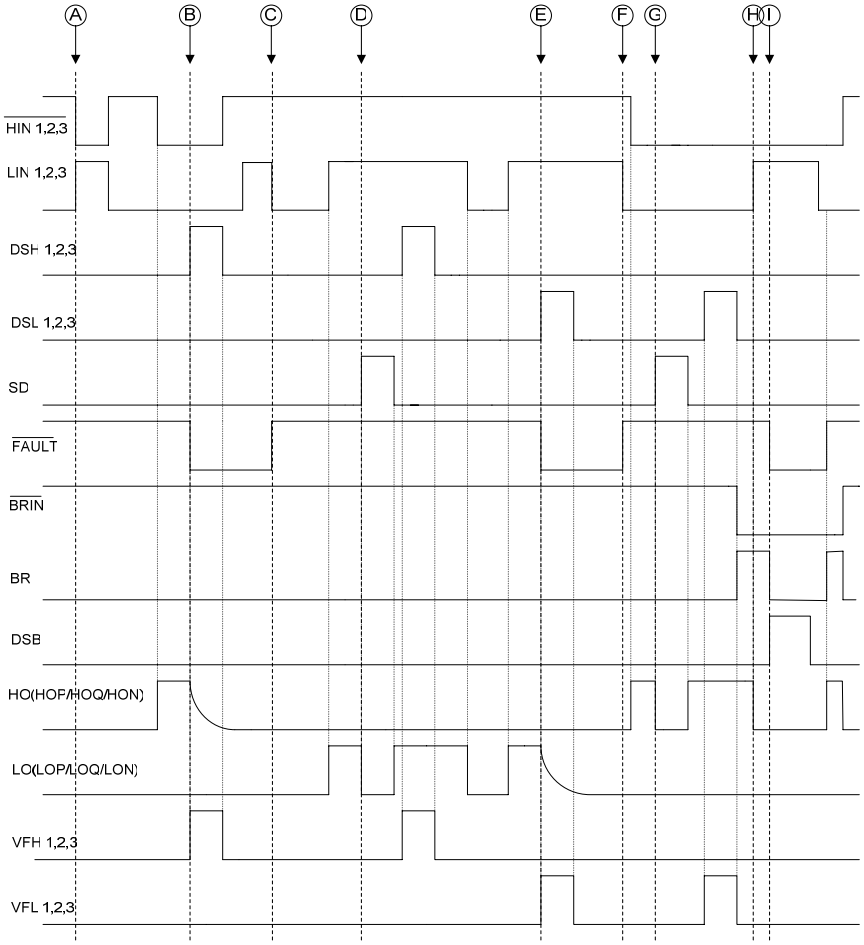


Figure 18: I/O timing diagram

Referred to timing diagram of Figure 18:

A. When the input signals are on together the outputs go off (anti-shoot through).
B. The HO signal is on and the high side IGBT desaturates, the HO turn off softly. FAULT goes low. While in SSD, if LIN goes up, LO does not change (freeze).
C. When FAULT is latched low (see FAULT section) it can be disabled by LIN1=LIN2=LIN3=0 condition.
D. SD disable HO and LO outputs.
E. The LO signal is on and the low side IGBT desaturates, the low side behaviour is the same as described in point B.
F. As C.
G. As D.
H. As A.
I. The BR signal is on and the brake IGBT desaturates. The driver goes in FAULT condition tuning off all the IGBTs (Hard shut down).

1 FEATURES DESCRIPTION

1.1 Start-up sequence

Device starts in FAULT condition at power-up unless FAULT clear condition is forced (i.e. LIN1=LIN2=LIN3=0 for at least t_{FLTCLR} – in this case FAULT is asserted for t_{fltclr}, then resets).
In FAULT condition driver outputs are insensitive to inputs: any noise on input pins is then rejected during system power-up.
As soon as the controller awakes, a FAULT clear action can be taken to enter the normal operating condition.

1.2 Normal operation mode

After clearing FAULT condition and supplies are stable the device becomes fully operative (see grey blocks in the State Diagram).
$HIN/N_{1,2,3}$, $LIN_{1,2,3}$ and BRIN/N produce driver outputs to switch accordingly, while the input logic checks the input signals preventing shoot-through events and including Dead-time (DT).

1.3 Shut down

The system controller can asynchronously command the Shutdown through the 3.3 V compatible CMOS I/O SD pin. This event is not latched.

1.4 Fault management

IR22381 is able to manage both the supply failure (undervoltage lockout on both low and high side circuits) and the desaturation of power transistors connected to its drivers outputs.

1.4.1 Undervoltage (UV)

The Undervoltage protection function disables the output stage of each driver preventing the power device being driven with too low voltages.
Both the low side (V_{CC} supplied) and the floating side (V_{BS} supplied) are controlled by a dedicate undervoltage function.
Undervoltage event on the V_{CC} (when $V_{CC} < UV_{VCC-}$) generates a diagnostic signal by forcing FAULT pin low (see FAULT section and Figure 20). This event disables both low side and floating drivers and the diagnostic signal holds until the under voltage condition is over. Fault condition is not latched and the FAULT pin is released once V_{CC} becomes higher than UV_{VCC+}.
The undervoltage on the V_{BS} works disabling only the floating driver. Undervoltage on V_{BS} does not prevent the low side driver to activate its output nor generate diagnostic signals. V_{BS} undervoltage condition ($V_{BS} < UV_{VBS-}$) latches the high side output stage in the low state. V_{BS} must be reestablished higher than UV_{VBS+} to return in normal operating mode. To turn on the floating driver H_{IN} must be re-asserted high (rising edge event on H_{IN} is required).

1.4.2 4.2 Power devices desaturation

Different causes can generate a power inverter failure: phase and/or rail supply short-circuit, overload conditions induced by the load, etc… In all these fault conditions a large current increase is produced in the IGBT.
The IR22381/IR21381 fault detection circuit monitors the IGBT emitter to collector voltage (V_{CE}) by means of an external high voltage diode. High current in the IGBT may cause the transistor to desaturate, i.e. V_{CE} to increase.
Once in desaturation, the current in power transistor can be as high as 10 times the nominal current. Whenever the transistor is switched off, this high current generates relevant voltage transients in the power stage that need to be smoothed out in order to avoid destruction (by over-voltages). The IR22381/IR21381 gate driver accomplish the transients control by smoothly turning off the desaturated transistor by means of the LON pin activating a so called *Soft ShutDown* sequence (SSD).

1.4.3 Desaturation detection: DSH/L and DSB pin function

Figure 19 shows the structure of the desaturation sensing and soft shutdown block. This configuration is the same for both high and low side output stages.

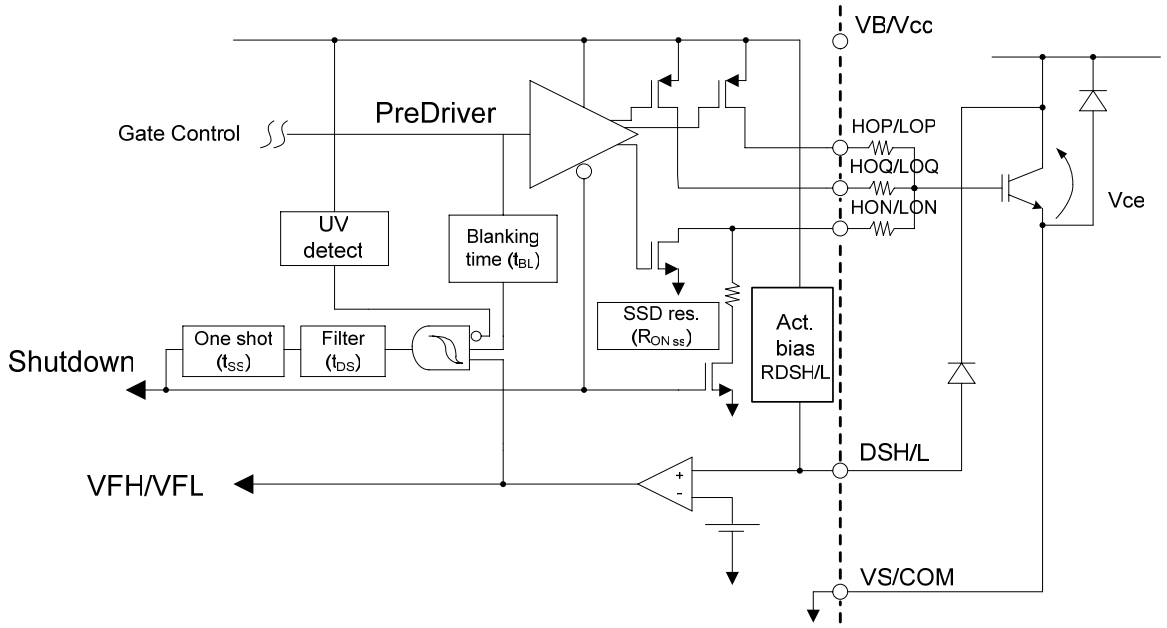


Figure 19: high and low side output stage for channels 1, 2, 3

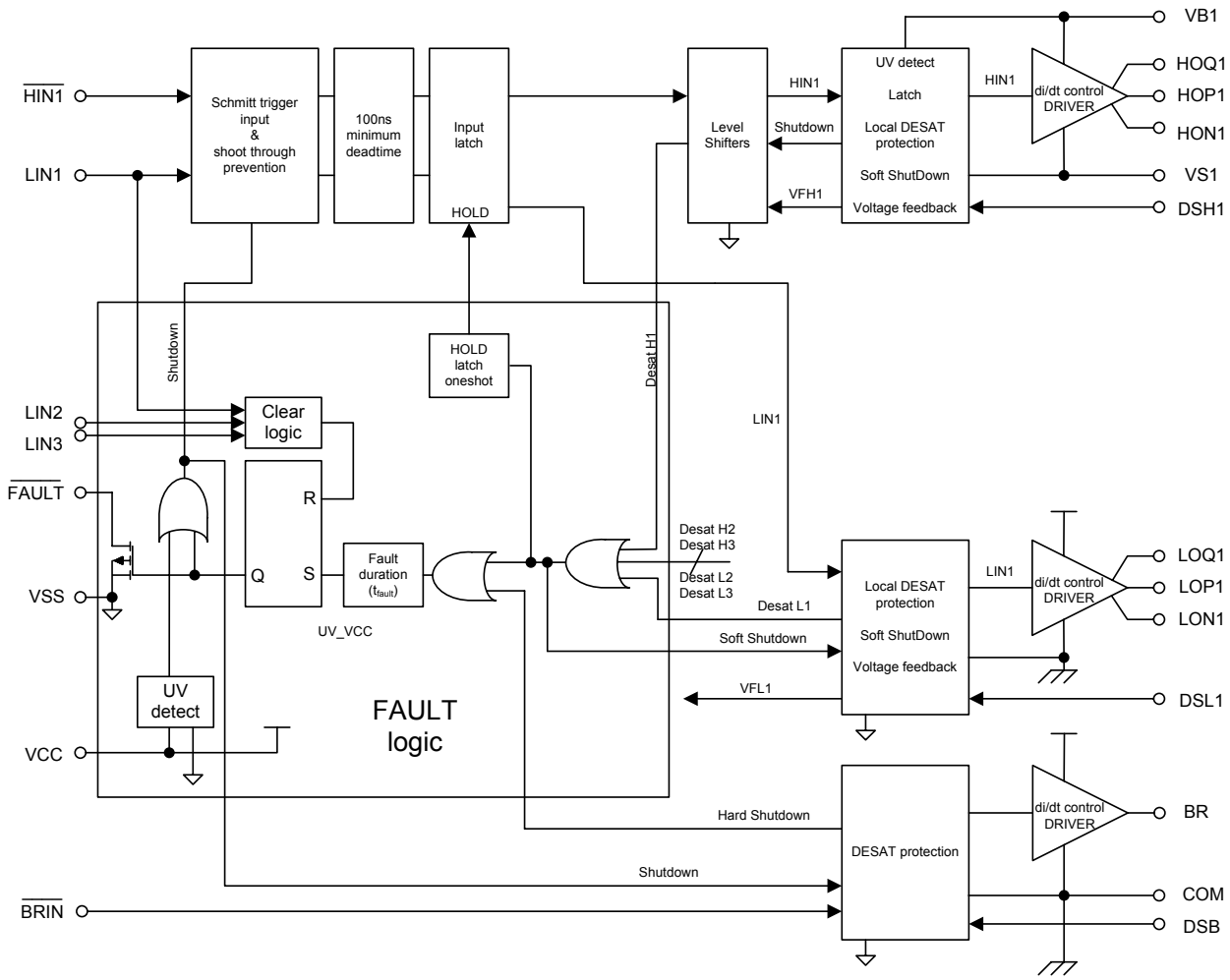


Figure 20: Fault management diagram

The external sensing diode should have BV>600V (or 1200V depending on application) and low stray capacitance (in order to minimize noise coupling and switching delays). The diode is biased by a dedicated circuit for IGBT driver outputs (see the active-bias section) and by a pull-up resistor for Brake output. When V_{CE} increases, the voltage at DSH/L pin increases too. Being internally biased to the local supply, DSH/L or DSB voltage is automatically clamped. When DSH/L or DSB exceed the V_{DESAT+} threshold the comparator triggers (see Figure 19). Comparator output is filtered in order to avoid false desaturation detection by externally induced noise; pulses shorter than t_{DS} are filtered out. To avoid detecting a false desaturation during IGBT turn on, the desaturation circuit is disabled by a Blanking signal (T_{BL}, see Blanking block in Figure 19). Blanking time is the estimated maximum IGBT turn on time and must be not exceeded by proper gate resistance sizing. When the IGBT is not completely saturated after T_{BL}, desaturation is detected and the driver will turn off.

1.4.4 SSD and Fault management

Output bridge
Desaturation event implies a large amount of current. For that reason, IR22381 turn off strategy is based on soft shutdown.
Eligible desaturation signals coming from DSH/L inputs initiate the Soft Shutdown sequence (SSD).
While in SSD, the SSD pull-down is activated ($R_{ON,SS}$ for t_{ss} – see Figure 19) to turn off the IGBT through HON/LON.
Figure 20 shows the fault management circuit. In this diagram Desat_H1,2,3 and Desat_L1,2,3 are the internal signals triggered by the desaturation event.

IR22381 accomplishes output bridge turn off in the following way:

- if the desaturated IGBT is a low side, all the low side IGBTs are softly turned off (SSD), while the high side IGBTs are kept in the state they were just before the desaturation event.
- If the desaturated IGBT is a high side, it is soflty turned off simultaneously with all the low side IGBTs. While the remaining HS IGBTs are kept in the state they were just before the desaturation event.

In any case, after the soft shutdown period (t_{SS}), all IGBTs are hardly shut down (brake IGBT included).
Desaturation event generates a FAULT signal (see Figure 11) that is latched until fault clear condition is verified.

It must be noted that while in Soft Shut Down, both Under Voltage fault and external Shut Down (SD) are masked until the end of SSD. Desaturation protection is working independently by the other control pins and it is disabled only when the output status is off.

Brake IGBT
Brake desaturation causes a hard shutdown for all the IGBTs.
Fault condition is asserted and hold until cleared by controller.

1.4.5 Fault Clear

Fault is cleared by forcing low simultaneously LIN1, LIN2 and LIN3 for at least t_{FLTCLR}.
When LIN inputs are simultaneously low and a desaturation event happens, FAULT is activated for a minimum amount of time of t_{fault}.

1.5 Active bias

For the purpose of sensing the power transistor desaturation the collector voltage is read by an external HV diode. The diode is normally biased by an internal pull up resistor connected to the local supply line (V_B or V_{CC}). When the transistor is “on” the diode is conducting and the amount of current flowing in the circuit is determined by the internal pull up resistor value.
In the high side circuit, the desaturation biasing current may become relevant for dimensioning the bootstrap capacitor (see Figure 23). In fact, too low pull up resistor value may result in high current discharging significantly the bootstrap capacitor. For that reason typical pull up resistor are in the range of 100 kΩ. This is the value of the internal pull up.
While the impedance of DSH/DSL pins is very low when the transistor is on (low impedance path through the external diode down to the power transistor), the impedance is only controlled by the pull up resistor when the transistor is off. In that case relevant dV/dt applied by the power transistor during the commutation at the output results in a considerable current injected through the stray capacitance of the diode into the desaturation detection pin (DSH/L). This coupled noise may be easily reduced using an active bias for the sensing diode.
An Active Bias structure is available DSH/L pin. The DSH/L pins present an active pull-up respectively to VB/VCC, and a pull-down respectively to VS/COM.
The dedicated biasing circuit reduces the impedance on the DSH/L pin when the voltage exceeds the V_{DESAT} threshold (see Figure 21). This low impedance helps in rejecting the noise providing the current inject by the parasitic capacitance. When the

power transistor is fully on, the sensing diode gets forward biased and the voltage at the DSH/L pin decreases. At this point the biasing circuit deactivates, in order to reduce the bias current of the diode as shown in Figure 21.

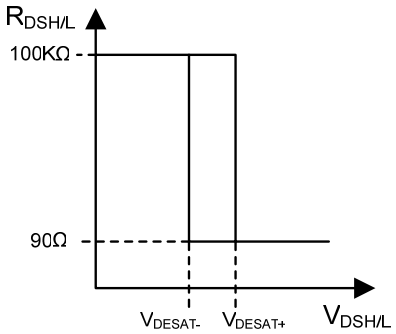


Figure 21: $R_{DSH/L}$ Active Biasing

1.6 Output stage

The structure is shown in Figure 19 and consists of two turn on stages (connected to HOP/LOP and HOQ/LOQ), one turn off stage for normal operation and one turn off stage for SSD operation (both connected to HON/LON).
When the driver turns on the IGBT (see Figure 16), a first stage is constantly activated (HOP/LOP) while an additional stage is maintained active only for a limited time (t_{ON1}, HOQ/LOQ). This feature boost the total driving capability in order to accommodate both fast gate charge to the plateau voltage and dV/dt control in switching.
At turn off, a single n-channel sinks up to 460mA (I_{O-}) and offers a low impedance path to prevent the self-turn on due to the parasitic Miller capacitance in the power switch.

1.7 Voltage FeedBack

Voltage feedback pins provide information about the state of the corresponding IGBT by means of sensing its collector.
The V_{DESAT} threshold discriminates whether the sensed IGBT can be considered on (DSH/L < V_{DESAT}) or off (DSH/L > V_{DESAT}).
IGBT state information is then sent to VFH/$L_{1,2,3}$ open collector outputs, which are tied to Vss ground.
See Figure 22 for functional details.

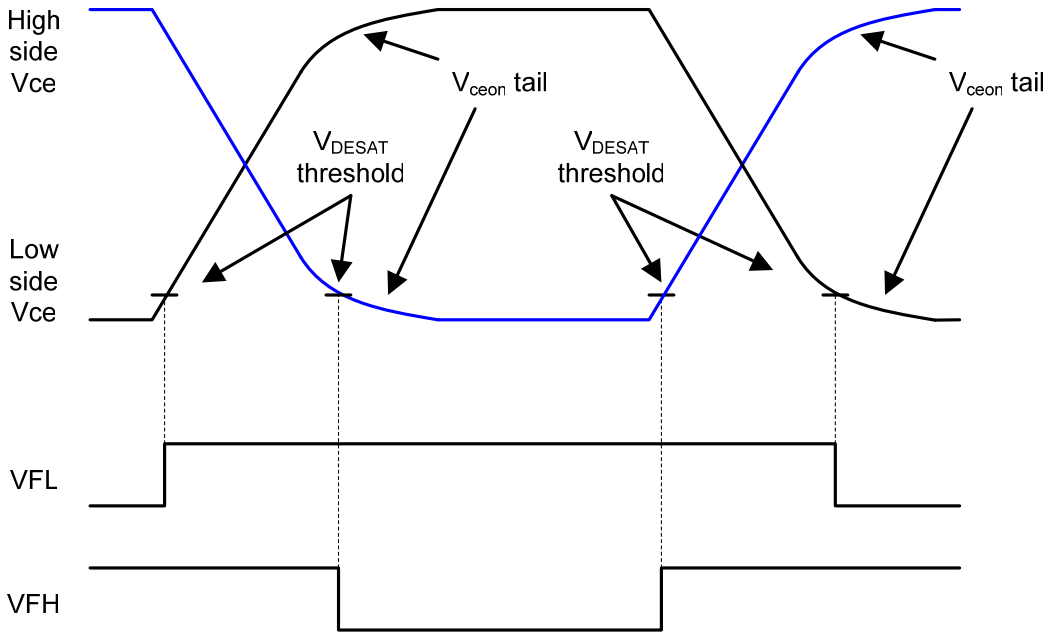


Figure 22: Voltage feedback functional diagram

2 Sizing tips

2.1 Bootstrap supply

The $V_{BS1,2,3}$ voltage provides the supply to the high side drivers circuitry of the IR22381/IR21381. V_{BS} supply sit on top of the V_S voltage and so it must be floating.
The bootstrap method to generate V_{BS} supply can be used with IR22381/IR21381 high side drivers. The bootstrap supply is formed by a diode and a capacitor connected as in Figure 23.

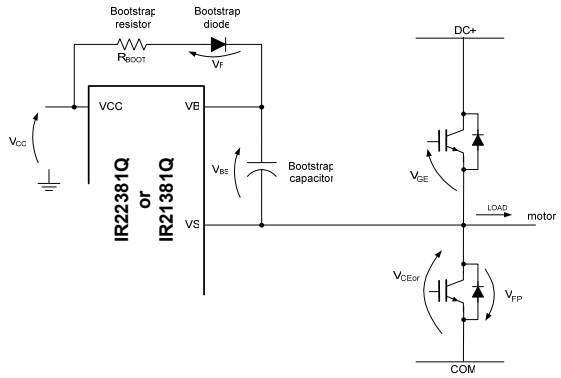


Figure 23: bootstrap supply schematic

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor.
Proper capacitor choice can reduce drastically these limitations.

Bootstrap capacitor sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (ΔV_{BS}) that we have to guarantee when the high side IGBT is on.
If V_{GEmin} is the minimum gate emitter voltage we want to maintain, the voltage drop must be:

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\min} - V_{CEon}$$

under the condition:

$$V_{GE\min} > V_{BSUV-}$$

where V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CEon} is emitter-collector voltage of low side IGBT and V_{BSUV-} is the high-side supply undervoltage negative going threshold.

Now we must consider the influencing factors contributing V_{BS} to decrease:

- IGBT turn on required Gate charge (Q_G);
- IGBT gate-source leakage current (I_{LK_GE});
- Floating section quiescent current (I_{QBS});
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE});
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS}); typical 20nC
- Bootstrap capacitor leakage current (I_{LK_CAP});
- High side on time (T_{HON}).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + \\ + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \cdot T_{HON}$$

The minimum size of bootstrap capacitor is:

$$C_{BOOT\min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

An example follows:

using a 15A @ 100°C IGBT (GB15XP120K):

- I_{QBS} = 250 µA (See Static Electrical Charact.);
- I_{LK} = 50 µA (See Static Electrical Charact.);
- Q_{LS} = 20 nC;
- Q_G = 58 nC (Q_{ge}+Q_{gc} Datasheet GB15XP120K);
- I_{LK_GE} = 250 nA (Datasheet GB15XP120K);
- I_{LK_DIODE} = 100 µA (with reverse recovery time <100 ns);
- I_{LK_CAP} = 0 (neglected for ceramic capacitor);
- I_{DS-} = *150* µA (see Static Electrical Charact.);
- T_{HON} = 100 µs.

And:

- V_{CC} = 18 V
- V_F = 1 V
- $V_{CEonmax}$ = 2.5 V
- V_{GEmin} = 11.9 V

the maximum voltage drop ΔV_{BS} becomes

$$\Delta V_{BS} \le V_{CC} - V_F - V_{GE\min} - V_{CEon} =$$

$$= 18V - 1V - 11.9V - 2.5V = 2.6V$$

And the bootstrap capacitor must be:

$$C_{BOOT} \geq \frac{133\,nC}{2.6\,V} = 51\,nF$$

NOTICE: Here above V_{CC} has been chosen to be 18V as an example. IGBTs can be supplied with higher/lower supply accordingly to design requirements. Vcc variations due to low voltage power supply must be accounted in the above formulas.

Some important considerations

a. Voltage ripple

There are three different cases making the bootstrap circuit get conductive (see Figure 23)

- I_{LOAD} < 0; the load current flows in the low side IGBT displaying relevant V_{CEon}

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

In this case we have the lowest value for V_{BS}. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off the Vs node is pushed up by the load current until the high side freewheeling diode get forwarded biased

- I_{LOAD} = 0; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

- I_{LOAD} > 0; the load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

In this case we have the highest value for V_{BS}. Turning on the high side IGBT, I_{LOAD} flows into it and V_S is pulled up.

To minimize the risk of undervoltage, bootstrap capacitor should be sized according to the I_{LOAD}<0 case.

b. Bootstrap Resistor

A resistor (R_{boot}) is placed in series with bootstrap diode (see Figure 23) so to limit the current when the bootstrap capacitor is initially charged. We suggest not exceeding some Ohms (typically 5, maximum 10 Ohm) to avoid increasing the V_{BS} time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

c. Bootstrap Capacitor

For high T_{HON} designs where is used an electrolytic tank capacitor, its ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot} generating a voltage step on V_{BS} at the first charge of bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint:

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \leq 3V$$

Parallel combination of small ceramic and large electrolytic capacitors is normally the best compromise, the first acting as fast charge thank for the gate charge only and limiting the dV_{BS}/dt by reducing the equivalent resistance while the second keeps the V_{BS} voltage drop inside the desired ΔV_{BS}.

d. Bootstrap Diode

The diode must have a BV> 600V (or 1200V depending on application) and a fast recovery time (trr < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply.

2.2 Gate resistances

The switching speed of the output transistor can be controlled by properly size the resistors controlling the turn-on and turn-off gate current. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver (R_{DRp} and R_{DRn}).

The examples always use IGBT power transistor. Figure 24 shows the nomenclature used in the following paragraphs. In addition, V_{ge}^* indicates the plateau voltage, Q_{gc} and Q_{ge} indicate the gate to collector and gate to emitter charge respectively.

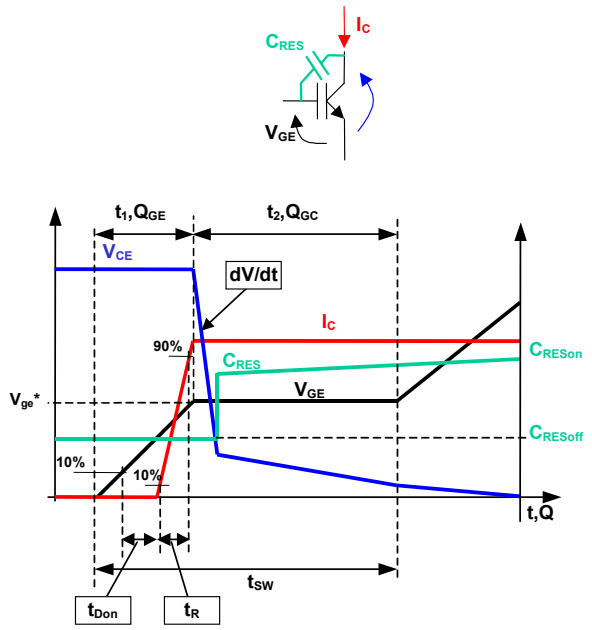


Figure 24: Nomenclature

2.2.1 Sizing the turn-on gate resistor

- Switching-time

For the matters of the calculation included hereafter, the switching time t_{sw} is defined as the time spent to reach the end of the plateau voltage (a total Q_{gc}+Q_{ge} has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from Q_{ge} and Q_{gc}, *Vcc*, V_{ge}^{*} (see Figure 25):

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

and

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{I_{avg}}$$

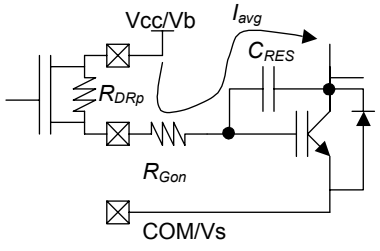


Figure 25: R_{Gon} sizing

where $R_{TOT} = R_{DRp} + R_{Gon}$

R_{Gon} = gate on-resistor
R_{DRp} = driver equivalent on-resistance

IR22381Q/IR21381Q HOP/LOP and HOQ/LOQ pins can be used to configure gate charge circuit.
Fast turn on can be configured using HOP and LOP pins (up to t_{ON1} switching time).
For slower turn on times HOQ and LOQ can be used.
Current partitioning can be changed acting on the output resistors.

In particular, shorting HOP to HOQ and LOP to LOQ, R_{DRp} is defined by

$$R_{DRp} = \begin{cases} \frac{t_{on1}}{t_{SW}}\left(\frac{Vcc}{I_{o1+}} + \frac{Vcc}{I_{o2+}}\left(\frac{t_{SW}}{t_{on1}} - 1\right)\right) & when \quad t_{SW} > t_{on1} \\ \frac{Vcc}{I_{o1+}} & when \quad t_{SW} \le t_{on1} \end{cases}$$

(I_{O1+} ,I_{O2+} and t_{on1} from "static Electrical Characteristics").

Table 1 reports the gate resistance size for two commonly used IGBTs (calculation made using typical datasheet values and assuming Vcc=15V).

- Output voltage slope

Turn-on gate resistor R_{Gon} can be sized to control output slope (dV_{OUT}/dt).
While the output voltage has a non-linear behaviour, the maximum output slope can be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}}$$

inserting the expression yielding I_{avg} and rearranging:

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{C_{RESoff} \cdot \frac{dV_{out}}{dt}}$$

As an example, Table 2 shows the sizing of gate resistance to get dV_{out}/dt=5V/ns when using two popular IGBTs, typical datasheet values and assuming *Vcc=15V*.

NOTICE: Turn on time must be lower than T_{BL} to avoid improper desaturation detection and SSD triggering.

Sizing the turn-off gate resistor

The worst case in sizing the turn-off resistor R_{Goff} is when the collector of the IGBT in off state is forced to commutate by external events (i.e. the turn-on of the companion IGBT).
In this case the dV/dt of the output node induces a parasitic current through C_{RESoff} flowing in R_{Goff} and R_{DRn} (see Figure 26).
If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on causing large oscillation and relevant cross conduction.

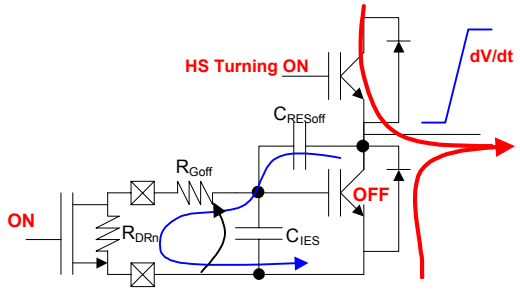


Figure 26: R_{Goff} sizing: current path when Low Side is off and High Side turns on

The transfer function between IGBT collector and IGBT gate then becomes:

$$\frac{V_{ge}}{V_{de}} = \frac{s \cdot (R_{Goff} + R_{DRn}) \cdot C_{RESoff}}{1 + s \cdot (R_{Goff} + R_{DRn}) \cdot (C_{RESoff} + C_{IES})}$$

Which yields to a high pass filter with a pole at:

$$1/\tau = \frac{1}{(R_{Goff} + R_{DRn}) \cdot (C_{RESoff} + C_{IES})}$$

As a result, when τ is faster than the collector rise time (to be verified after calculation) the transfer function can be approximated by:

$$\frac{V_{ge}}{V_{de}} = s \cdot (R_{Goff} + R_{DRn}) \cdot C_{RESoff}$$

So that $V_{ge} = (R_{Goff} + R_{DRn}) \cdot C_{RESoff} \cdot \frac{dV_{de}}{dt}$ in the time domain.
Then the condition:

$$V_{th} > V_{ge} = \left(R_{Goff} + R_{DRn}\right) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

must be verified to avoid spurious turn on.

Rearranging the equation yields:

$$(1) \quad R_{Goff} < \frac{V_{th}}{C_{RESoff} \cdot \frac{dV}{dt}} - R_{DRn}$$

In any case, the worst condition for a spurious turn on is with very fast steps on IGBT collector.
In that case collector to gate transfer function can be approximated with the capacitor divider:

$$V_{ge} = V_{de} \cdot \frac{C_{RESoff}}{(C_{RESoff} + C_{IES})}$$

which is driven only by IGBT characteristics.

As an example, table 3 reports R_{Goff} (calculated with the above mentioned equation (1)) for two popular IGBTs to withstand $dV_{out}/dt = 5V/ns$.

NOTICE: the above-described equations are intended being an approximated way for the gate resistances sizing. More accurate sizing may account more precise device modelling and parasitic component dependent on the PCB and power section layout and related connections.

Table 1: R_{Gon} sizing driven by t_{sw} constraint

IGBT	Qge	Qgc	Vge*	tsw	Iavg	Rtot	RGon → std commercial value	Tsw
GB15XP120K*	12nC	46nC	9V	500ns	116mA	77Ω	Rtot - RDRp = 15 Ω → 10 Ω	→465ns
GB05XP120K	3.7nC	14nC	9.5V	400ns	44mA	124Ω	Rtot - RDRp = 65 Ω → 68 Ω	→408ns
IRGB5B120KD	3.7nC	13nC	9.5V	500ns	33mA	164Ω	Rtot - RDRp = 102 Ω → 100 Ω	→502ns

Table 2: Table 2: RGon sizing driven by dVOUT/dt constraint

IGBT	Qge	Qgc	Vge*	CRESoff	Rtot	RGon → std commercial value	dVout/dt
GB15XP120K*	12nC	46nC	9V	38pF	47Ω	Rtot - RDRp = 4.5 Ω → 4.7Ω	→5V/ns
GB05XP120K	3.7nC	14nC	9.5V	12pF	91Ω	Rtot - RDRp = 48.8 Ω → 47Ω	→5.1V/ns
IRGB120KD	3.7nc	13nC	9.5V	11pF	100Ω	Rtot - RDRp = 57 Ω → 56 Ω	→5V/ns

Table 3: RGoff sizing

IGBT	Vth(min)	CRESoff	RGoff
GB15XP120K*	5	38pF	RGoff = 0 Ω
GB05XP120K	5	12pF	RGoff ≤ 55 Ω
IRG4PH20K(D)	5	11pF	RGoff ≤ 63 Ω

* sized with 18V supply

3 PCB LAYOUT TIPS

3.1 Distance from H to L voltage

The IR22381/IR21381Q pin out lacks some pins (see Figure 17) maximizing the distance between floating (from DC- to DC+) and low voltage pins . It's strongly recommended to place components tied to floating voltage in the respective high voltage portions of the device ($VB_{1,2,3}$, $VS_{1,2,3}$) side.

3.2 Ground plane

Ground plane must not be placed under or nearby the high voltage floating side to minimize noise coupling.

3.3 Gate drive loops

Current loops behave like an antenna able to receive and transmit EM noise. In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Figure 23 shows the high and low side gate loops.
Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect. For this reason is strongly recommended to place the three gate resistances close together and to minimize the loop area (see Figure 27).

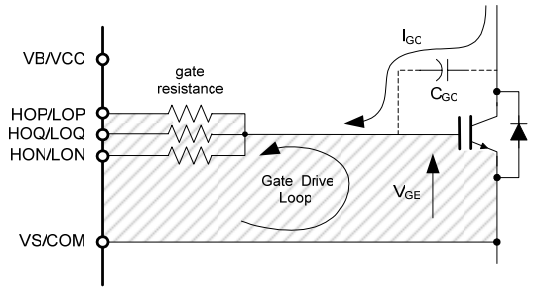


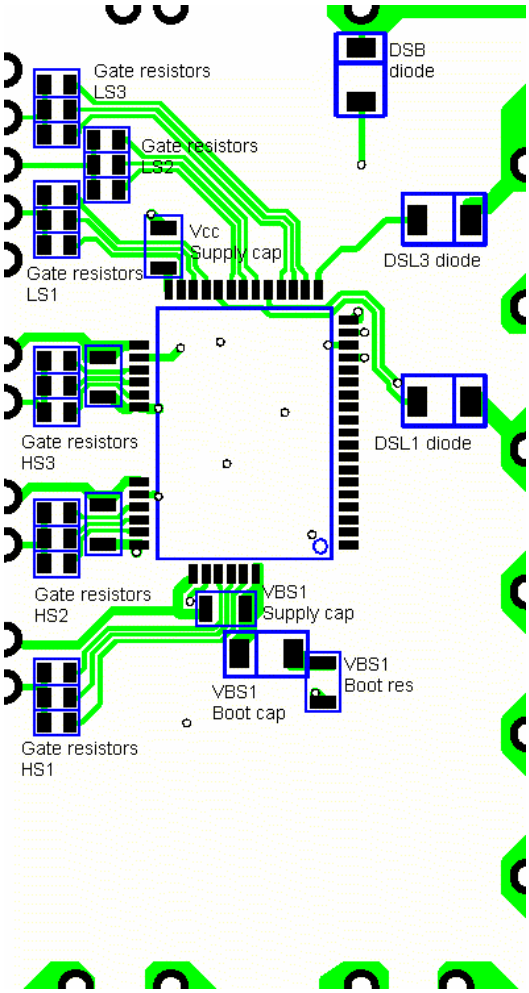
Figure 27: gate drive loop

3.4 Supply capacitors

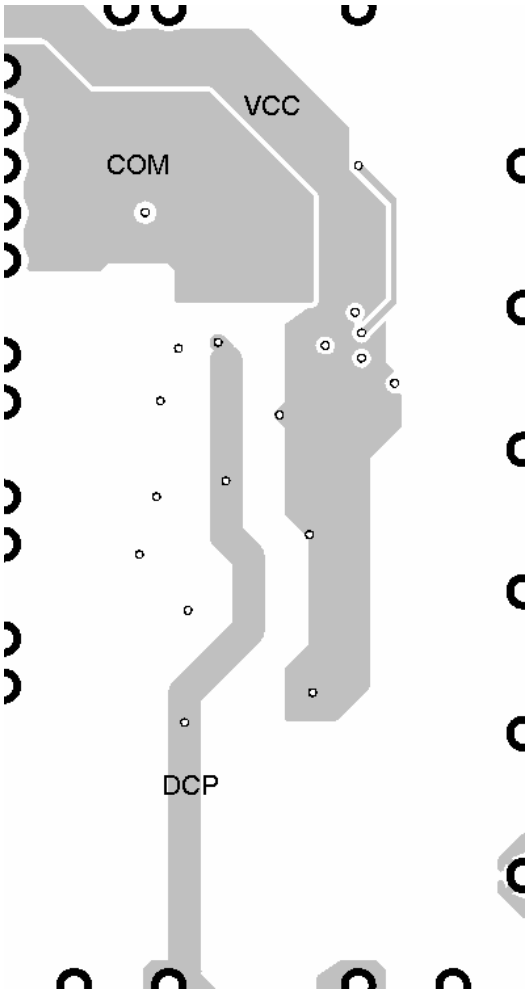
IR22381 output stages are able to quickly turn on IGBT with up to 460mA of output current. The supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/resistance.

3.5 Routing and placement example

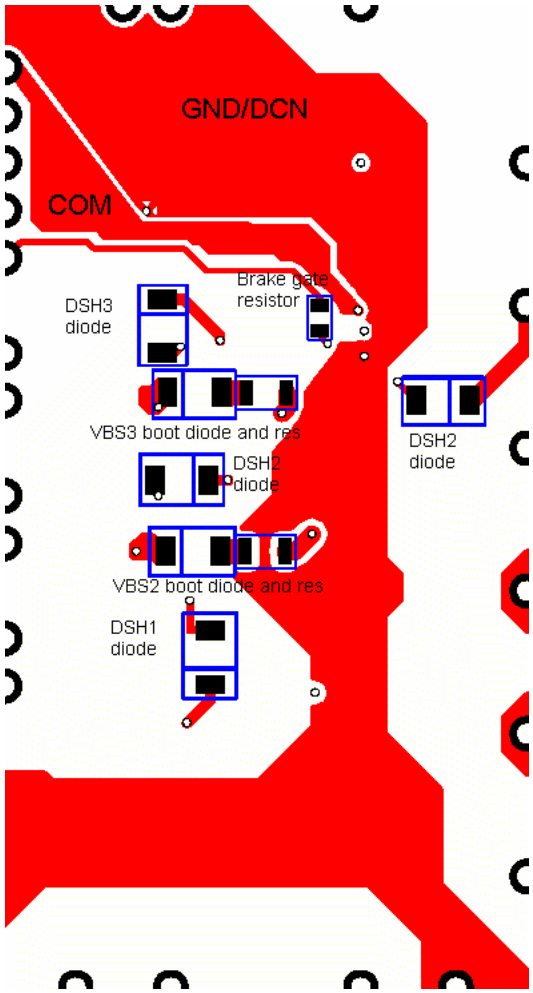
Figure 28 shows one of the possible layout solutions using a 3 layer PCB (low voltage signals not shown) on an ECONO PIM module. This example takes into account all the previous considerations. Placement and routing for supply capacitors and gate resistances in the high and low voltage side minimize respectively supply path and gate drive loop. The bootstrap diode is placed under the device to have the cathode as close as possible to bootstrap capacitor and the anode far from high voltage and close to V_{CC}.



a) TOP(Gate Drive)



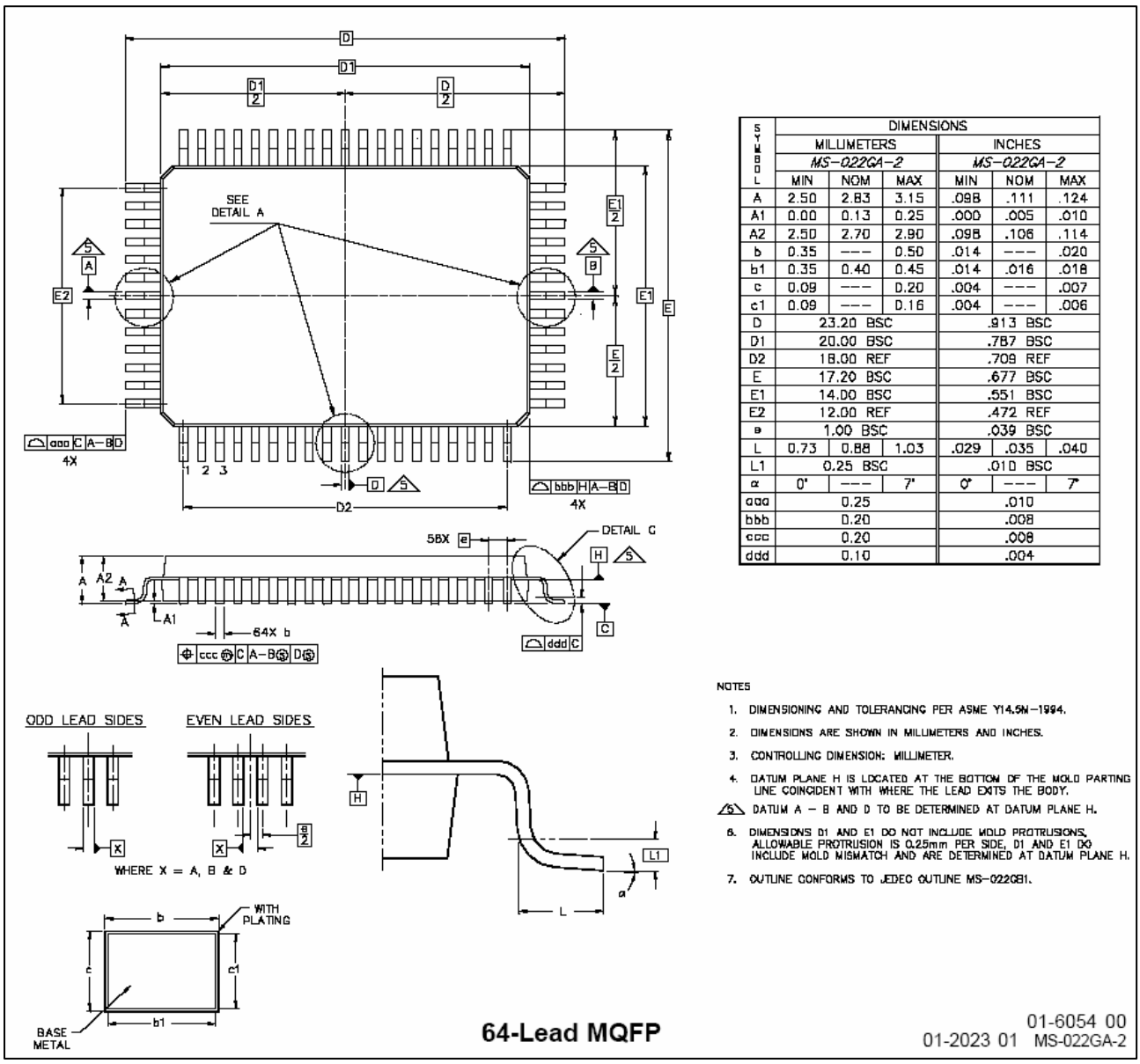
b) BOTTOM (GND)



c) MID (VCC/COM/DCP)

Figure 28: layout example: top (a), internal layer (b) and bottom (c) layer

Case Outline



SYMBOL	DIMENSIONS					
	MILLIMETERS			INCHES		
	MS-022GA-2			MS-022GA-2		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.50	2.83	3.15	.098	.111	.124
A1	0.00	0.13	0.25	.000	.005	.010
A2	2.50	2.70	2.90	.098	.106	.114
b	0.35	---	0.50	.014	---	.020
b1	0.35	0.40	0.45	.014	.016	.018
c	0.09	---	0.20	.004	---	.007
c1	0.09	---	0.16	.004	---	.006
D	23.20 BSC			.913 BSC		
D1	20.00 BSC			.787 BSC		
D2	18.00 REF			.709 REF		
E	17.20 BSC			.677 BSC		
E1	14.00 BSC			.551 BSC		
E2	12.00 REF			.472 REF		
e	1.00 BSC			.039 BSC		
L	0.73	0.88	1.03	.029	.035	.040
L1	0.25 BSC			.010 BSC		
α	0°	---	7°	0°	---	7°
aaa	0.25			.010		
bbb	0.20			.008		
ccc	0.20			.008		
ddd	0.10			.004		

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM A – B AND D TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. OUTLINE CONFORMS TO JEDEC OUTLINE MS-022GB1.

Qualification Level: Industrial level, MSL3, Lead-free.

ESD Classification:
Human Body Model (HBM): Class 2, per JESD22-A114-B
Machine Model (MM): Class B, per EIA/JESD22-A115-A

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