THE DATASHEET OF

ESP32-PICO-V3-02

ESP32-PICO Series

Datasheet

2.4 GHz Wi-Fi + Bluetooth® + Bluetooth LE SiP

Integrating all peripheral components in one single package

Including:

ESP32-PICO-D4

ESP32-PICO-V3

ESP32-PICO-V3-02

Version 1.0

Espressif Systems

Product Overview

The ESP32-PICO series is a System-in-Package (SiP) device that is based on the ESP32 SoC. The ESP32-PICO series include ESP32-PICO-D4, ESP32-PICO-V3, and ESP32-PICO-V3-02 variants. In this document, unless otherwise stated, "ESP32-PICO" refers to all the variants.

ESP32-PICO provides Wi-Fi 802.11b/g/n, Bluetooth® v4.2 BR/EDR, and Bluetooth LE functionalities. It integrates all peripheral components seamlessly in a single package, including a crystal oscillator, filter capacitors, SPI flash/PSRAM (optional), and RF matching circuit. ESP32-PICO is built in an ultra-small size, with robust performance and low energy consumption. It is well suited for any space-limited or battery-operated applications, such as wearable electronics, medical equipment, sensors, and other IoT products.

The ESP32-PICO series of variants are similar to each other, but still vary in some aspects, for example, the embedded chip revision, pin layout, dimensions, etc. Table 1 lists the differences between these variants. For detailed description please go to specific sections.

If you would like to migrate from the existing module design based on older ESP32-PICO variants to a new design based on newer ESP32-PICO variants, please refer to section 11 Migration Guide.

Table 1: Differences Between ESP32-PICO Series of Variants

Differences in	Section
Chip revision	Section 1 ESP32-PICO Series Comparison
In-package flash and PSRAM	Section 1 ESP32-PICO Series Comparison
Package and dimensions	Section 7 Package Information
Pin layout	Section 2.1 ESP32-PICO-D4, 2.2 ESP32-PICO-V3 and ESP32-PICO-V3-02
Pin compatibility	Section 2.4 Pin Compatibility Between ESP32-PICO Variants
Schematics	Section 5 Schematics
Peripheral schematics	Section 6 Peripheral Schematics

Block Diagram

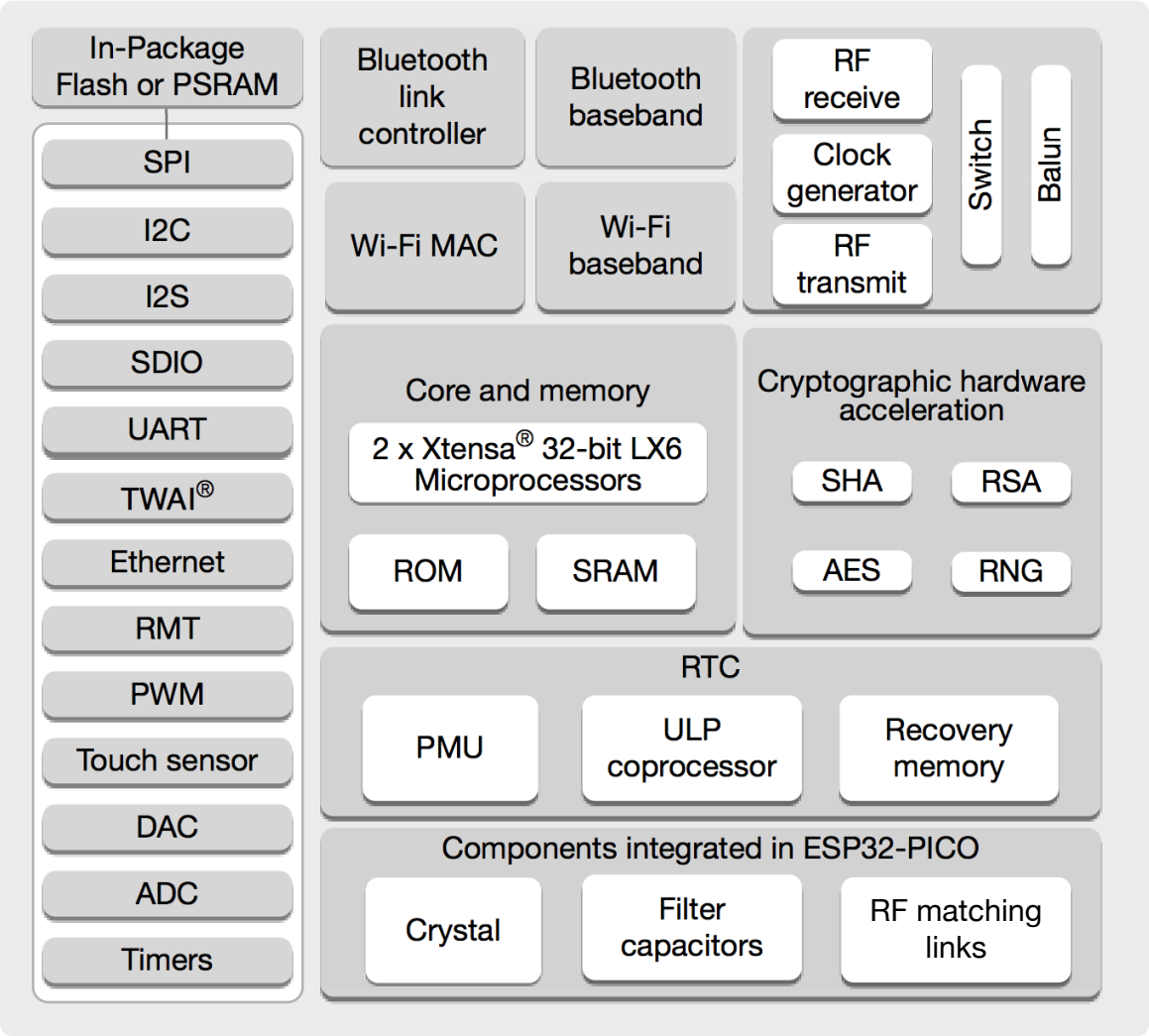


Figure 1: Block Diagram of ESP32-PICO

Features

CPU and On-Chip Memory

- Xtensa® dual-core 32-bit LX6 microprocessor, up to 240 MHz
- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC

In-Package Flash and PSRAM

- ESP32-PICO-D4: 4 MB flash
- ESP32-PICO-V3: 4 MB flash
- ESP32-PICO-V3-02: 8 MB flash, 2 MB PSRAM

Wi-Fi

- 802.11b/g/n
- 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth v4.2 BR/EDR and Bluetooth LE specification
- Class-1, class-2 and class-3 transmitter
- AFH
- CVSD and SBC

Peripherals

- Up to 34 GPIOs for ESP32-PICO-D4
  - 5 strapping GPIOs
  - 6 GPIOs used for in-package flash
  - 6 input-only GPIOs
- Up to 31 GPIOs for ESP32-PICO-V3
  - 5 strapping GPIOs
  - 2 GPIOs used for in-package flash
  - 6 input-only GPIOs
- Up to 31 GPIOs for ESP32-PICO-V3-02
  - 5 strapping GPIOs
  - 4 GPIOs used for in-package flash/PSRAM
  - 6 input-only GPIOs
- SD/SDIO/MMC Host Controller, UART, SPI, SDIO/SPI Slave Controller, I2C, LED PWM, Motor PWM, I2S, infrared remote controller, pulse counter, capacitive touch sensor, ADC, DAC, Ethernet MAC, TWAI® (compatible with ISO 11898-1, i.e. CAN 2.0 Specifications)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C

Note:
For a detailed description of the features listed above, please refer to *ESP32 Series Datasheet* > Section *Functional Description*.

Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS machines
- Service robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Speech Recognition
- Image Recognition
- SDIO Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

Contents

List of Tables

List of Figures

1 ESP32-PICO Series Comparison

1.1 ESP32-PICO Series Nomenclature

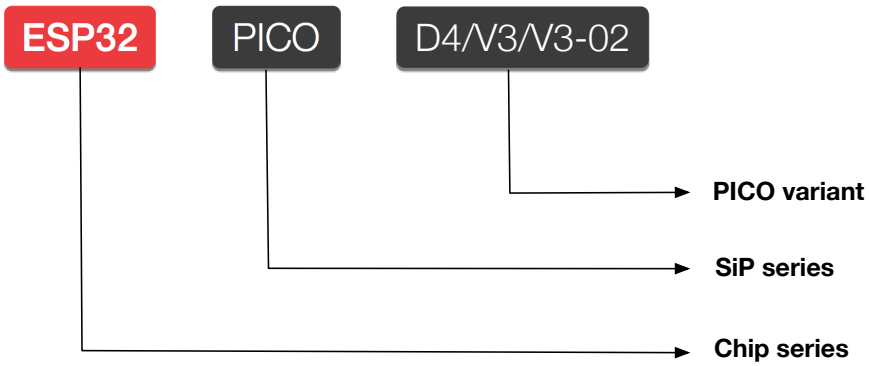


Figure 2: ESP32-PICO Series Nomenclature

1.2 Comparison

Table 2: ESP32-PICO Series Comparison

Ordering Code	Chip Revision[1]	In-Package Flash[5]	In-Package PSRAM	Dimensions (mm)
ESP32-PICO-D4	v1.0/v1.1[2]	4 MB (Quad SPI)	—	7.0 x 7.0 x 0.94
ESP32-PICO-V3	v3.0/v3.1[3, 4]	4 MB (Quad SPI)	—	7.0 x 7.0 x 0.94
ESP32-PICO-V3-02	v3.0/v3.1[3, 4]	8 MB (Quad SPI)	2 MB (Quad SPI)	7.0 x 7.0 x 1.11

[1] For chip revision identification and chip revision-specific errata, see *ESP32 Series SoC Errata*.

[2] The ESP32 chip revision on ESP32-PICO-D4 is upgraded from v1.0 to v1.1. See PCN20220901 for more details.

[3] The ESP32 chip revision on ESP32-PICO-V3 and ESP32-PICO-V3-02 is upgraded from v3.0 to v3.1. See PCN20220901 for more details.

[4] For differences between chip revision v3.0 and previous ESP32 chip revisions, please refer to *ESP32 Chip Revision v3.0 User Guide*.

[5] The in-package flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

2 Pin Definition

2.1 ESP32-PICO-D4

2.1.1 Pin Layout

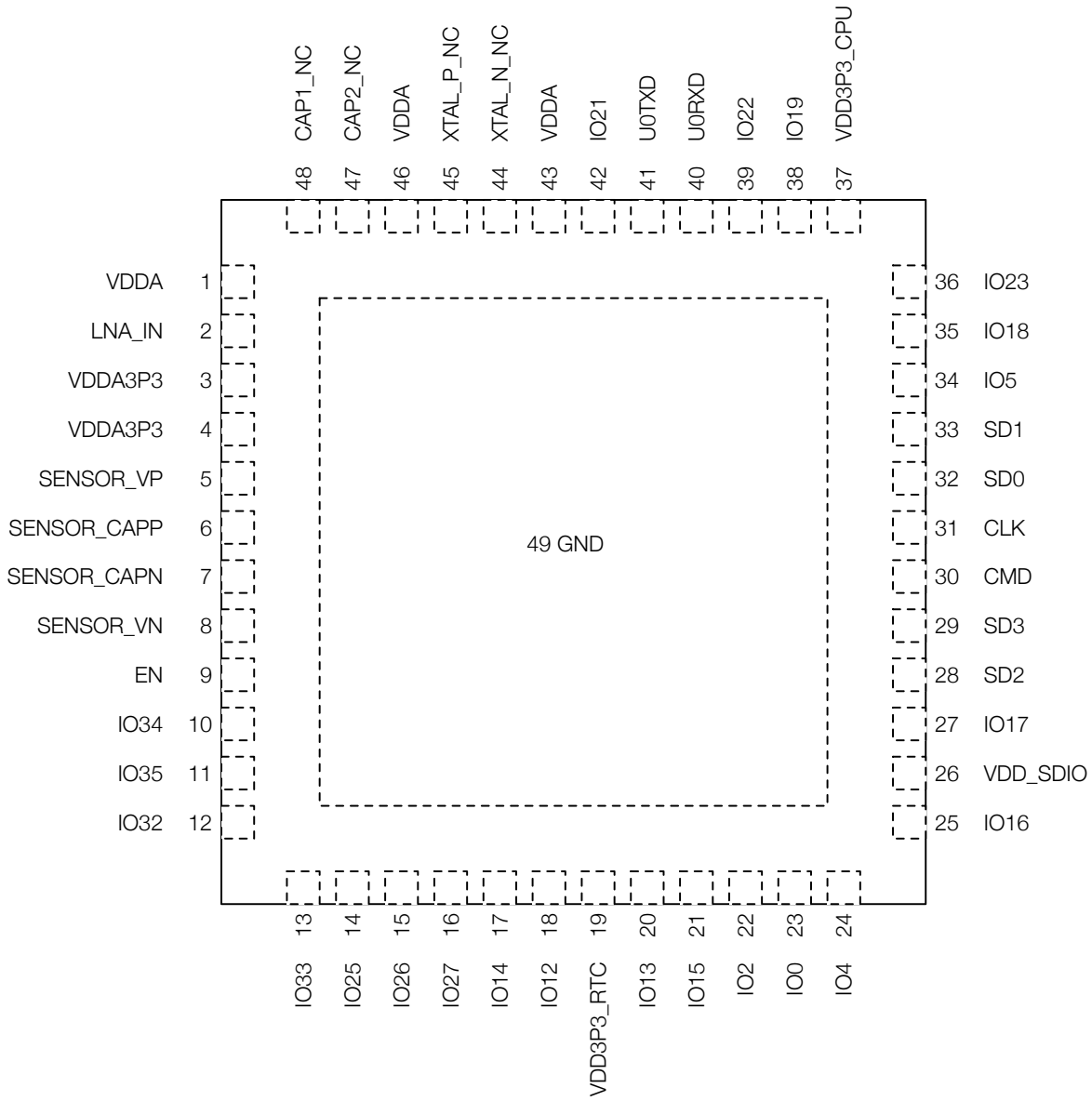


Figure 3: Pin Layout of ESP32-PICO-D4 (Top View)

2.1.2 Pin Description

Notes for Table 3 Pin Description:

1. The highlighted cells indicate pins that are connected to the in-package flash. For details see Section 2.1.3 Pin Mapping Between ESP32-PICO-D4 and Flash/PSRAM.
2. For definition of functions in column **Function**, see Section 2.3 Pin Function Description.
3. **Type**: I/O — Input/Output; I — Input.

Table 3: Pin Description of ESP32-PICO-D4

Name	No.	Type	Function
VDDA	1	Power	Analog power supply
LNA_IN	2	I/O	RF input and output
VDDA3P3	3	Power	Analog power supply
VDDA3P3	4	Power	Analog power supply
SENSOR_VP	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN	8	I	GPIO39, ADC1_CH3, RTC_GPIO3
EN	9	I	High: On; enables the SiP Low: Off; the SiP shuts down Note: Do not leave this pin floating.
IO34	10	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	11	I	GPIO35, ADC1_CH7, RTC_GPIO5
IO32	12	I/O	GPIO32, 32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	13	I/O	GPIO33, 32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	14	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	15	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	16	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	17	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	18	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
VDD3P3_RTC	19	Power	Input power supply for RTC IO
IO13	20	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
IO15	21	I/O	GPIO15, ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	22	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	23	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	24	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
IO16	25	I/O	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
VDD_SDIO	26	Power	Output power supply
IO17	27	I/O	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
SD2	28	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SD3	29	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
CMD	30	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS

Cont'd on next page

Table 3 – cont'd from previous page

Name	No.	Type	Function
CLK	31	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SD0	32	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SD1	33	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO5	34	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	35	I/O	GPIO18, VSPICLK, HS1_DATA7
IO23	36	I/O	GPIO23, VSPID, HS1_STROBE
VDD3P3_CPU	37	Power	Input power supply for CPU IO
IO19	38	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
IO22	39	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
U0RXD	40	I/O	GPIO3, U0RXD, CLK_OUT2
U0TXD	41	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO21	42	I/O	GPIO21, VSPIHD, EMAC_TX_EN
VDDA	43	Power	Analog power supply
XTAL_N_NC	44	—	NC
XTAL_P_NC	45	—	NC
VDDA	46	Power	Analog power supply
CAP2_NC	47	—	NC
CAP1_NC	48	—	NC

2.1.3 Pin Mapping Between ESP32-PICO-D4 and Flash/PSRAM

Table 4 lists ESP32 pins exposed on the package that are also used to connect the in-package flash and off-package PSRAM. **It is not recommended to use the pins connected to flash/PSRAM for any other purposes.**

Table 4: Pin Mapping Between ESP32-PICO-D4 and Flash/PSRAM

Pin No.	Pin Name	In-Package Flash	Off-Package PSRAM
31	CLK	FLASH_CLK	PSRAM_CLK
25	IO16	FLASH_CS	—
29	SD3[1]	—	PSRAM_CS
33	SD1	SI/SIO0	SI/SIO0
27	IO17	SO/SIO1	SI/SIO1
32	SD0	WP/SIO2	SIO2
30	CMD	HOLD/SIO3	SIO3

[1] SD3 is recommended for PSRAM_CS. You can also choose any available GPIO as PSRAM_CS.

2.2 ESP32-PICO-V3 and ESP32-PICO-V3-02

2.2.1 Pin Layout

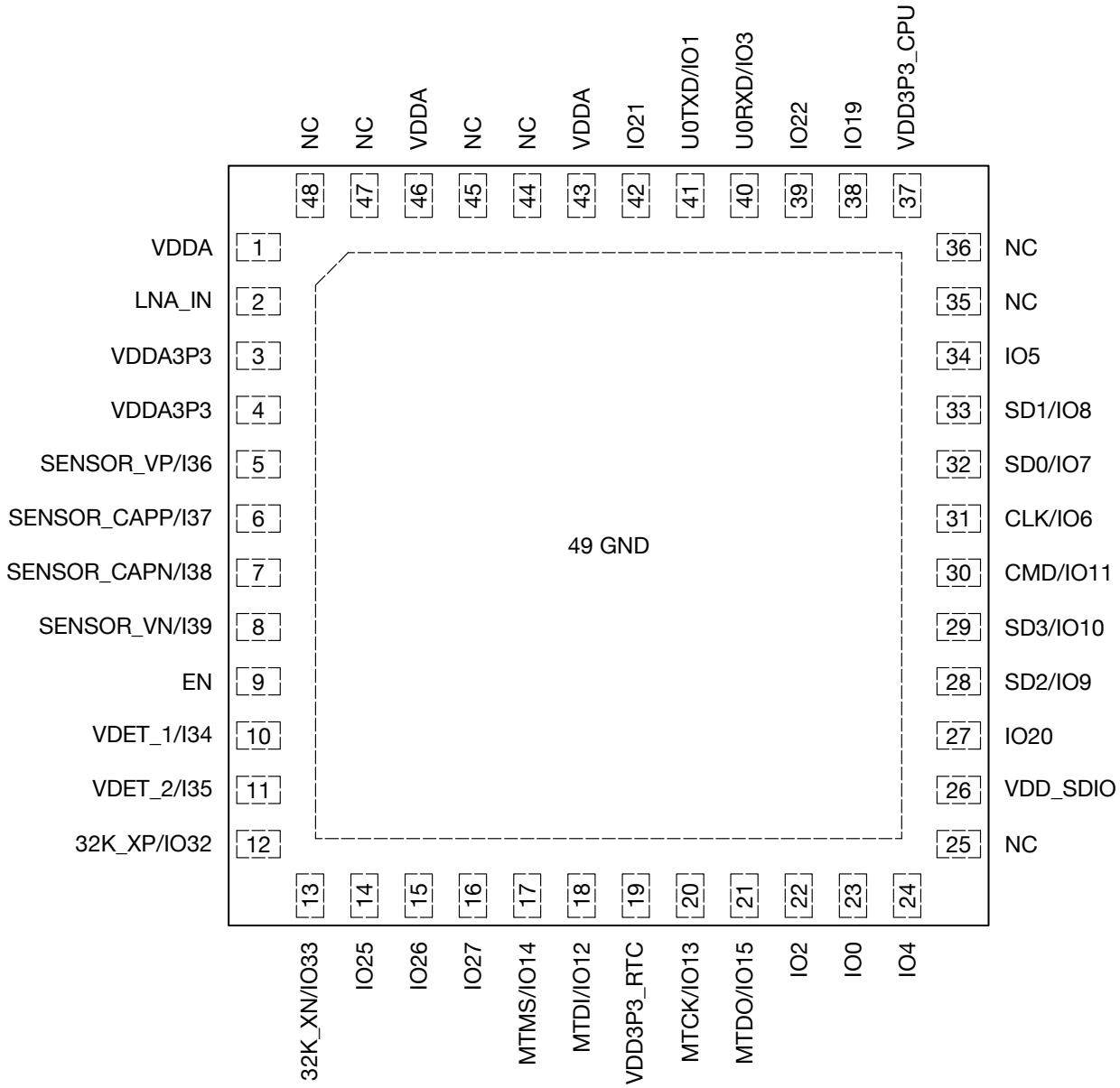


Figure 4: Pin Layout of ESP32-PICO-V3 and ESP32-PICO-V3-02 (Top View)

2.2.2 Pin Description

Notes for Table 5 Pin Description:

1. The highlighted cells indicate pins that are connected to in-package flash or PSRAM. See Section 2.2.3 Pin Mapping Between ESP32-PICO-V3/ESP32-PICO-V3-02 and Flash/PSRAM for details.
2. For ESP32-PICO-V3: IO6/IO7/IO8/IO9/IO10/IO11/IO20 belong to VDD_SDIO power domain and can not work when VDD_SDIO power shuts down.

3. For definition of functions in column **Function**, see Section 2.3 Pin Function Description.

Table 5: Pin Description of ESP32-PICO-V3 and ESP32-PICO-V3-02

Name	No.	Type	Function
VDDA	1	Power	Analog power supply
LNA_IN	2	I/O	RF input and output
VDDA3P3	3	Power	Analog power supply
VDDA3P3	4	Power	Analog power supply
SENSOR_VP/I36	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP/I37	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN/I38	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN/I39	8	I	GPIO39, ADC1_CH3, RTC_GPIO3
EN	9	I	High: On; enables the SiP Low: Off; the SiP powers off Note: Do not leave this pin floating.
VDET_1/I34	10	I	ADC1_CH6, RTC_GPIO4
VDET_2/I35	11	I	ADC1_CH7, RTC_GPIO5
32K_XP/IO32	12	I/O	32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
32K_XN/IO33	13	I/O	32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	14	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	15	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	16	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
MTMS/IO14	17	I/O	ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
MTDI/IO12	18	I/O	ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
VDD3P3_RTC	19	Power	Input power supply for RTC IO
MTCK/IO13	20	I/O	ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
MTDO/IO15	21	I/O	ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	22	I/O	ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	23	I/O	ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	24	I/O	ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
NC	25	—	NC
VDD_SDIO	26	Power	Output power supply
IO20	27	I/O	GPIO20
SD2/IO9	28	I/O	**ESP32-PICO-V3:** GPIO9, SD_DATA2, HS1_DATA2, U1RXD **ESP32-PICO-V3-02:** Used for connecting in-package PSRAM.

Cont'd on next page

Table 5 – cont'd from previous page

Name	No.	Type	Function
SD3/IO10	29	I/O	**ESP32-PICO-V3:** GPIO10, SD_DATA3, HS1_DATA3, U1TXD **ESP32-PICO-V3-02:** Used for connecting in-package PSRAM.
CMD/IO11	30	I/O	Used for connecting in-package flash
CLK/IO6	31	I/O	Used for connecting in-package flash
SD0/IO7	32	I/O	GPIO7, SD_DATA0, HS1_DATA0, U2RTS
SD1/IO8	33	I/O	GPIO8, SD_DATA1, HS1_DATA1, U2CTS
IO5	34	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
NC	35	—	NC
NC	36	—	NC
VDD3P3_CPU	37	Power	Input power supply for CPU IO
IO19	38	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
IO22	39	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
U0RXD/IO3	40	I/O	GPIO3, U0RXD, CLK_OUT2
U0TXD/IO1	41	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO21	42	I/O	GPIO21, VSPIHD, EMAC_TX_EN
VDDA	43	Power	Analog power supply
NC	44	—	NC
NC	45	—	NC
VDDA	46	Power	Analog power supply
NC	47	—	NC
NC	48	—	NC

2.2.3 Pin Mapping Between ESP32-PICO-V3/ESP32-PICO-V3-02 and Flash/PSRAM

Table 6 lists ESP32 pins exposed on the package that are also used to connect the in-package flash/PSRAM. **It is not recommended to use the pins connected to flash/PSRAM for any other purposes.**

Table 6: Pin Mapping Between ESP32-PICO-V3/ESP32-PICO-V3-02 and Flash/PSRAM

Pin No.	Pin Name	In-Package Flash	In-Package PSRAM
31	CLK/IO6	FLASH_CLK	—
30	CMD/IO11	FLASH_CS	—
28	SD2/IO9	—	PSRAM_CS
29	SD3/IO10	—	PSRAM_CLK

2.3 Pin Function Description

Table 7 provides description of pin functions.

Table 7: Pin Function Description

Function Name	Description
GPIO*x*	General-purpose input and output (*x* is GPIO number). GPIO pins can be assigned various functions, including digital and analog functions. For more information, please refer to *ESP32 Series Datasheet* > Appendix *IO_MUX*.
MTCK/MTDO/MTDI/MTMS	JTAG interface signals.
32K_XP/XN	32 KHz external clock input/output (connecting to ESP32-PICO's oscillator). P/N means differential clock positive/negative.
RTC_GPIO*x*	RTC domain GPIO function for low power management.
TOUCH*x*	Analog function for touch sensing.
ADC*x*_CH*y*	Analog to digital conversion channel. *x* is ADC number, *y* is channel number.
DAC_*x*	Digital to analog conversion module. *x* is DAC number.
CLK_OUT*x*	Clock output for debugging. *x* is clock number.
SPI*	Signals of SPI0/1 module. * is CLK, CS0, D, Q, WP, HD.
HSPI*	Signals of SPI2 module. * is CLK, CS0, D, Q, WP, HD.
VSPI*	Signals of SPI3 module. * is CLK, CS0, D, Q, WP, HD.
U0*	Signals of UART0 module. * is CTS, RTS, RXD, TXD.
U1*	Signals of UART1 module. * is CTS, RTS, RXD, TXD.
U2*	Signals of UART2 module. * is CTS, RTS, RXD, TXD.
SD_*	Signals of SDIO slave. * is CLK, CMD, DATA0 ~ DATA3.
HS1_*	Port 1 signals of the SDIO host, * is CLK, CMD, STROBE, DATA0 ~ DATA7.
HS2_*	Port 2 signals of the SDIO host, * is CLK, CMD, DATA0 ~ DATA3.
NC	Not connected.

2.4 Pin Compatibility Between ESP32-PICO Variants

While the ESP32-PICO variants are very similar from a pin-out perspective, there are several changes to the pins and their functions, as shown in Table 8. The differences in pins require attention when migrating from one variant to another.

Table 8: Pin Compatibility Between ESP32-PICO Variants

Pin No.	ESP32-PICO-D4	ESP32-PICO-V3	ESP32-PICO-V3-02
5, 6, 7, 8, 10, 11	Input-only and RTC GPIO	Input-only and RTC GPIO	Input-only and RTC GPIO
12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 23, 24	RTC GPIO	RTC GPIO	RTC GPIO
25	GPIO16, used for in-package flash	NC	NC

Cont'd on next page

Table 8 – cont'd from previous page

Pin No.	ESP32-PICO-D4	ESP32-PICO-V3	ESP32-PICO-V3-02
27	GPIO17, used for in-package flash	GPIO20, can be used freely	GPIO20, can be used freely
28	GPIO9, can be used freely	GPIO9, can be used freely	GPIO9, used for in-package PSRAM
29	GPIO10, can be used freely	GPIO10, can be used freely	GPIO10, used for in-package PSRAM
30	GPIO11, can be used freely	GPIO11, used for in-package flash	GPIO11, used for in-package flash
31	GPIO6, used for in-package flash	GPIO6, used for in-package flash	GPIO6, used for in-package flash
32	GPIO7, used for in-package flash	GPIO7, can be used freely	GPIO7, can be used freely
33	GPIO8, used for in-package flash	GPIO8, can be used freely	GPIO8, can be used freely
34, 38, 39, 42	GPIO, can be used freely	GPIO, can be used freely	GPIO, can be used freely
35	GPIO18, can be used freely	NC	NC
36	GPIO23, can be used freely	NC	NC
40	U0RXD	U0RXD	U0RXD
41	U0TXD	U0TXD	U0TXD

2.5 Strapping Pins

Note:
The content below is excerpted from *ESP32 Series Datasheet* > Section *Strapping Pins*. For the strapping pin mapping between the chip and ESP32-PICO, please refer to Chapter 5 *Schematics*.

There are five strapping pins:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak

pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on the chip.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 9 for a detailed boot-mode configuration by strapping pins.

Table 9: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V		1.8 V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don't-care		0	
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- FE: falling-edge, RE: rising-edge.
- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave", after booting.
- For ESP32 chips that contain an in-package flash or PSRAM, users need to note the logic level of MTDI. For example, ESP32-U4WDH contains an in-package flash that operates at 3.3 V, therefore, the MTDI should be low.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 10 and Figure 5.

Table 10: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	1

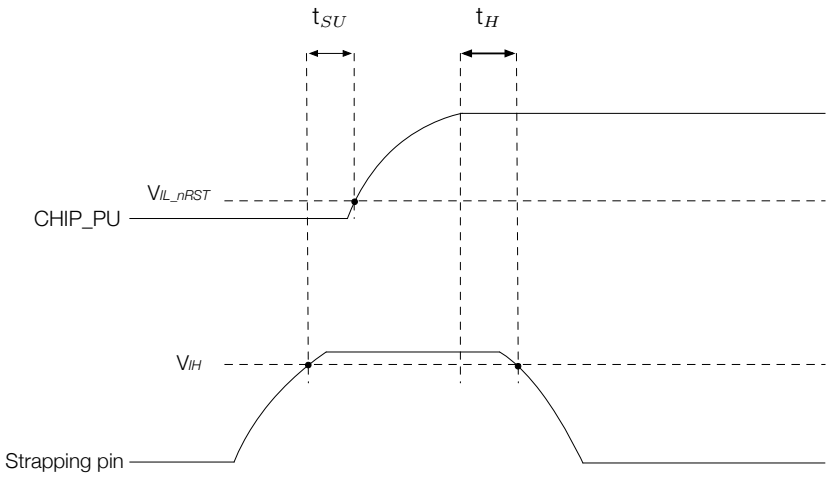


Figure 5: Visualization of Timing Parameters for the Strapping Pins

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Stresses above those listed in Table 11 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and normal operation of the device at these or any other conditions beyond those indicated in Section 3.2 Recommended Power Supply Characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11: Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO[1]	Allowed input voltage	–0.3	3.6	V
I_{output}[2]	Cumulative IO output current	—	1100	mA
T_{STORE}	Storage temperature	–40	85	°C

[1] For IO's power domain, please see *ESP32 Series Datasheet* > Appendix *IO MUX*.

[2] The product proved to be fully functional after all its IO pins were pulled high while being connected to ground for 24 consecutive hours at ambient temperature of 25 °C.

3.2 Recommended Power Supply Characteristics

Table 12: Recommended Power Supply Characteristics

Parameter	Description	Min	Typ	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC[1] VDD_SDIO[2]	Recommended input voltage	3.0	3.3	3.6	V
VDD3P3_CPU	Recommended input voltage	1.8	3.3	3.6	V
I_{VDD}	Cumulative input current	0.5	—	—	A
T	Operating temperature	–40	—	85	°C

[1] When writing eFuse, VDD3P3_RTC should be at least 3.3 V.

[2] VDD_SDIO:

- VDD_SDIO is powered by VDD3P3_RTC via 6 Ω resistor for 3.3 V flash/PSRAM, therefore, there will be some voltage drop from VDD3P3_RTC.
- VDD_SDIO can also be driven by an external power supply.

3.3 DC Characteristics (3.3 V, 25 °C)

Table 13: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		—	2	—	pF
V_{IH}	High-level input voltage		0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage		–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current		—	—	50	nA
I_{IL}	Low-level input current		—	—	50	nA
V_{OH}	High-level output voltage		0.8 × VDD[1]	—	—	V
V_{OL}	Low-level output voltage		—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	—	40	—	mA
		VDD3P3_RTC power domain [1, 2]	—	40	—	mA
		VDD_SDIO power domain [1, 3]	—	20	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)		—	28	—	mA
R_{PU}	Resistance of internal pull-up resistor		—	45	—	kΩ
R_{PD}	Resistance of internal pull-down resistor		—	45	—	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip		—	—	0.6	V

[1] VDD is the I/O voltage for a particular power domain of pins. For IO's power domain, please see *ESP32 Series Datasheet* > Appendix *IO MUX*.

[2] For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.

[3] Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

3.4 Current Consumption Characteristics

3.4.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 14: Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @ 19.5 dBm	370
		802.11g, 54 Mbps, OFDM @ 14 dBm	270
		802.11n, HT20, MCS7 @ 13 dBm	250
		802.11n, HT40, MCS7 @ 13 dBm	205
	RX	802.11b/g/n, HT20	113
		802.11n, HT40	120

3.4.2 Current Consumption in Other Modes

Table 15: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep[1, 2]	The CPU is powered on[3]	240 MHz	30 ~ 68 mA
		160 MHz	27 ~ 44 mA
		Normal speed: 80 MHz	20 ~ 31 mA
Light-sleep	—		0.8 mA
Deep-sleep	The ULP coprocessor is powered on[4]		150 μA
	ULP sensor-monitored pattern[5]		100 μA @1% duty
	RTC timer + RTC memory		10 μA
	RTC timer only		5 μA
Power off	CHIP_PU is set to low level, the chip is powered off		1 μA

[1] The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.

[2] When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.

[3] In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.

[4] During Deep-sleep, when the ULP coprocessor is powered on, peripherals such as GPIO and RTC I2C are able to operate.

[5] The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When ADC works with a duty cycle of 1%, the typical current consumption is 100 μA.

4 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The front-end circuit is a 0 Ω resistor.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

4.1 Wi-Fi Radio (2.4 GHz)

Table 16: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

4.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 17: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	19.5	—
802.11b, 11 Mbps, CCK	—	19.5	—
802.11g, 6 Mbps, OFDM	—	18.0	—
802.11g, 54 Mbps, OFDM	—	14.0	—
802.11n, HT20, MCS0	—	18.0	—
802.11n, HT20, MCS7	—	13.0	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	13.0	—

Table 18: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–26.5	–10.0
802.11b, 11 Mbps, CCK	—	–26.5	–10.0
802.11g, 6 Mbps, OFDM	—	–24.0	–5.0
802.11g, 54 Mbps, OFDM	—	–30.0	–25.0
802.11n, HT20, MCS0	—	–24.0	–5.0

Cont'd on next page

Table 18 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11n, HT20, MCS7	—	–30.5	–27.0
802.11n, HT40, MCS0	—	–24.0	–5.0
802.11n, HT40, MCS7	—	–30.5	–27.0

[1] EVM is measured at the corresponding typical TX power provided in Table 17 *Wi-Fi RF Transmitter (TX) Characteristics* above.

4.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n.

Table 19: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–97.0	—
802.11b, 2 Mbps, DSSS	—	–94.0	—
802.11b, 5.5 Mbps, CCK	—	–92.0	—
802.11b, 11 Mbps, CCK	—	–88.0	—
802.11g, 6 Mbps, OFDM	—	–93.0	—
802.11g, 9 Mbps, OFDM	—	–91.0	—
802.11g, 12 Mbps, OFDM	—	–89.0	—
802.11g, 18 Mbps, OFDM	—	–87.0	—
802.11g, 24 Mbps, OFDM	—	–84.0	—
802.11g, 36 Mbps, OFDM	—	–80.0	—
802.11g, 48 Mbps, OFDM	—	–77.0	—
802.11g, 54 Mbps, OFDM	—	–75.0	—
802.11n, HT20, MCS0	—	–92.0	—
802.11n, HT20, MCS1	—	–88.0	—
802.11n, HT20, MCS2	—	–86.0	—
802.11n, HT20, MCS3	—	–83.0	—
802.11n, HT20, MCS4	—	–80.0	—
802.11n, HT20, MCS5	—	–76.0	—
802.11n, HT20, MCS6	—	–74.0	—
802.11n, HT20, MCS7	—	–72.0	—
802.11n, HT40, MCS0	—	–89.0	—
802.11n, HT40, MCS1	—	–85.0	—
802.11n, HT40, MCS2	—	–83.0	—
802.11n, HT40, MCS3	—	–80.0	—
802.11n, HT40, MCS4	—	–76.0	—
802.11n, HT40, MCS5	—	–72.0	—
802.11n, HT40, MCS6	—	–71.0	—
802.11n, HT40, MCS7	—	–69.0	—

Table 20: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	0	—
802.11g, 54 Mbps, OFDM	—	–8	—
802.11n, HT20, MCS0	—	0	—
802.11n, HT20, MCS7	—	–8	—
802.11n, HT40, MCS0	—	0	—
802.11n, HT40, MCS7	—	–8	—

Table 21: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	35	—
802.11b, 11 Mbps, CCK	—	35	—
802.11g, 6 Mbps, OFDM	—	27	—
802.11g, 54 Mbps, OFDM	—	13	—
802.11n, HT20, MCS0	—	27	—
802.11n, HT20, MCS7	—	12	—
802.11n, HT40, MCS0	—	16	—
802.11n, HT40, MCS7	—	7	—

4.2 Bluetooth Radio

4.2.1 Receiver – Basic Data Rate

Table 22: Receiver Characteristics – Basic Data Rate

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @0.1% BER	—	—	–92	—	dBm
Maximum received signal @0.1% BER	—	0	—	—	dBm
Co-channel C/I	—	—	+7	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	—	–6	dB
	F = F0 – 1 MHz	—	—	–6	dB
	F = F0 + 2 MHz	—	—	–25	dB
	F = F0 – 2 MHz	—	—	–33	dB
	F = F0 + 3 MHz	—	—	–25	dB
	F = F0 – 3 MHz	—	—	–45	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm

Cont'd on next page

Table 22 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

4.2.2 Transmitter – Basic Data Rate

Table 23: Transmitter Characteristics – Basic Data Rate

Parameter	Description	Min	Typ	Max	Unit
RF transmit power*	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
+20 dB bandwidth	—	—	0.9	—	MHz
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–55	—	dBm
	F = F0 ± 3 MHz	—	–55	—	dBm
	F = F0 ± > 3 MHz	—	–59	—	dBm
$\Delta f1_{avg}$	—	—	—	155	kHz
$\Delta f2_{max}$	—	127	—	—	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	—	—	0.92	—	—
ICFT	—	—	–7	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift (DH1)	—	—	6	—	kHz
Drift (DH5)	—	—	6	—	kHz

* There are a total of eight power levels from 0 to 7, and the transmit power ranges from –12 dBm to 9 dBm. When the power level rises by 1, the transmit power increases by 3 dB. Power level 4 is used by default and the corresponding transmit power is 0 dBm.

4.2.3 Receiver – Enhanced Data Rate

Table 24: Receiver Characteristics – Enhanced Data Rate

Parameter	Description	Min	Typ	Max	Unit
π/4 DQPSK					
Sensitivity @0.01% BER	—	—	–92	—	dBm
Maximum received signal @0.01% BER	—	—	0	—	dBm
Co-channel C/I	—	—	11	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–7	—	dB
	F = F0 – 1 MHz	—	–7	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
8DPSK					

Cont'd on next page

Table 24 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @0.01% BER	—	—	–86	—	dBm
Maximum received signal @0.01% BER	—	—	–5	—	dBm
C/I c-channel	—	—	18	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	2	—	dB
	F = F0 – 1 MHz	—	2	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–25	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–38	—	dB

4.2.4 Transmitter – Enhanced Data Rate

Table 25: Transmitter Characteristics – Enhanced Data Rate

Parameter	Description	Min	Typ	Max	Unit
RF transmit power (see note under Table 23)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
$\pi/4$ DQPSK max w0	—	—	–0.72	—	kHz
$\pi/4$ DQPSK max wi	—	—	–6	—	kHz
$\pi/4$ DQPSK max |wi + w0|	—	—	–7.42	—	kHz
8DPSK max w0	—	—	0.7	—	kHz
8DPSK max wi	—	—	–9.6	—	kHz
8DPSK max |wi + w0|	—	—	–10	—	kHz
$\pi/4$ DQPSK modulation accuracy	RMS DEVM	—	4.28	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	13.3	—	%
8 DPSK modulation accuracy	RMS DEVM	—	5.8	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	14	—	%
In-band spurious emissions	F = F0 ± 1 MHz	—	–46	—	dBm
	F = F0 ± 2 MHz	—	–44	—	dBm
	F = F0 ± 3 MHz	—	–49	—	dBm
	F = F0 +/– > 3 MHz	—	—	–53	dBm
EDR differential phase coding	—	—	100	—	%

4.3 Bluetooth LE Radio

Table 26: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–12.0 ~ 9.0 dBm

4.3.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 27: Bluetooth LE - Transmitter Characteristics

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\ 1,\ 2,\ 3,\ \ldots k}$	—	2.2	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\ 3,\ 4,\ \ldots k}$	—	1.3	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\ 7,\ 8,\ \ldots k}$	—	1.5	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.6	—	kHz
Modulation characteristics	$\Delta\ F1_{\text{avg}}$	—	247.5	—	kHz
	Min. $\Delta\ F2_{\text{max}}$ (for at least 99.9% of all $\Delta\ F2_{\text{max}}$)	—	206.0	—	kHz
	$\Delta\ F2_{\text{avg}}/\Delta\ F1_{\text{avg}}$	—	0.86	—	—
In-band emissions	± 2 MHz offset	—	–55	—	dBm
	± 3 MHz offset	—	–57	—	dBm
	> ± 3 MHz offset	—	–59	—	dBm

4.3.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 28: Bluetooth LE - Receiver Characteristics

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–96.5	—	dBm
Maximum received signal @30.8% PER		—	—	5	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	10	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	2	—	dB
		F = F0 – 1 MHz	—	4	—	dB
		F = F0 + 2 MHz	—	–21	—	dB
		F = F0 – 2 MHz	—	–20	—	dB
		F = F0 + 3 MHz	—	–32	—	dB
		F = F0 – 3 MHz	—	–45	—	dB
		F ≥ F0 + 4 MHz	—	–29	—	dB
		F ≤ F0 – 4 MHz	—	–40	—	dB
	Image frequency	—	—	–29	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–29	—	dB
		F = F_{image} – 1 MHz	—	–32	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–10	—	dBm
		2003 MHz ~ 2399 MHz	—	–27	—	dBm
		2484 MHz ~ 2997 MHz	—	–27	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–36	—	dBm

5 Schematics

This section provides the reference designs for the ESP32-PICO series variants.

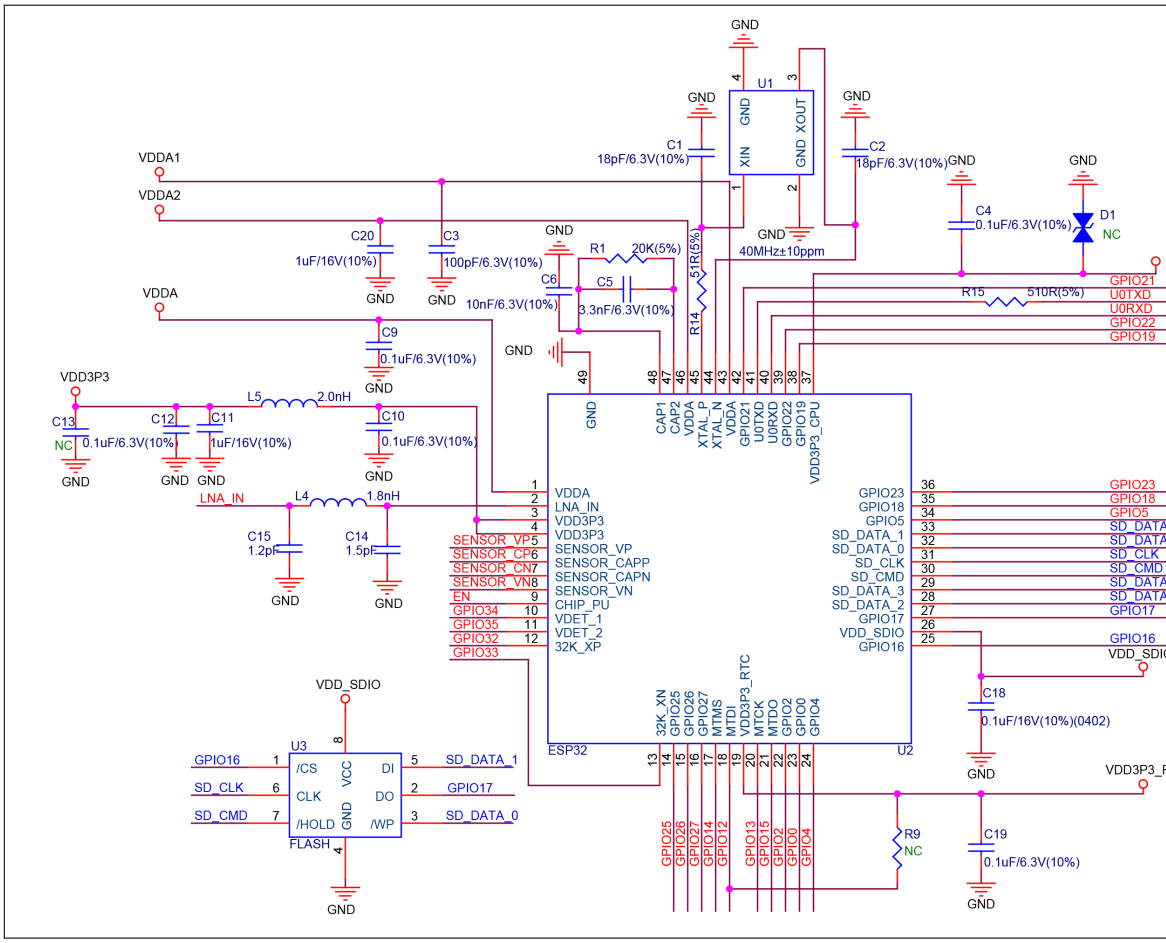


Figure 6: ESP32-PICO-D4 Schematics

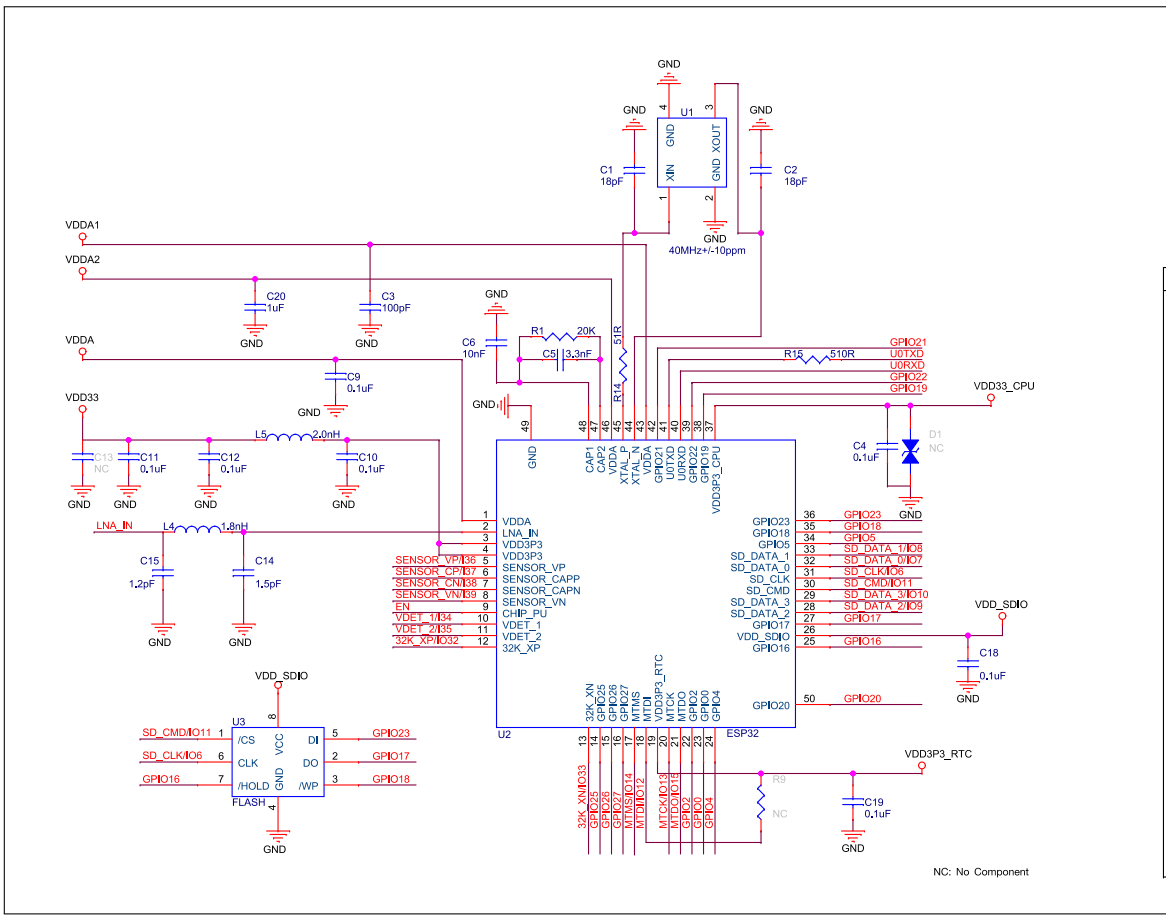


Figure 7: ESP32-PICO-V3 Schematics

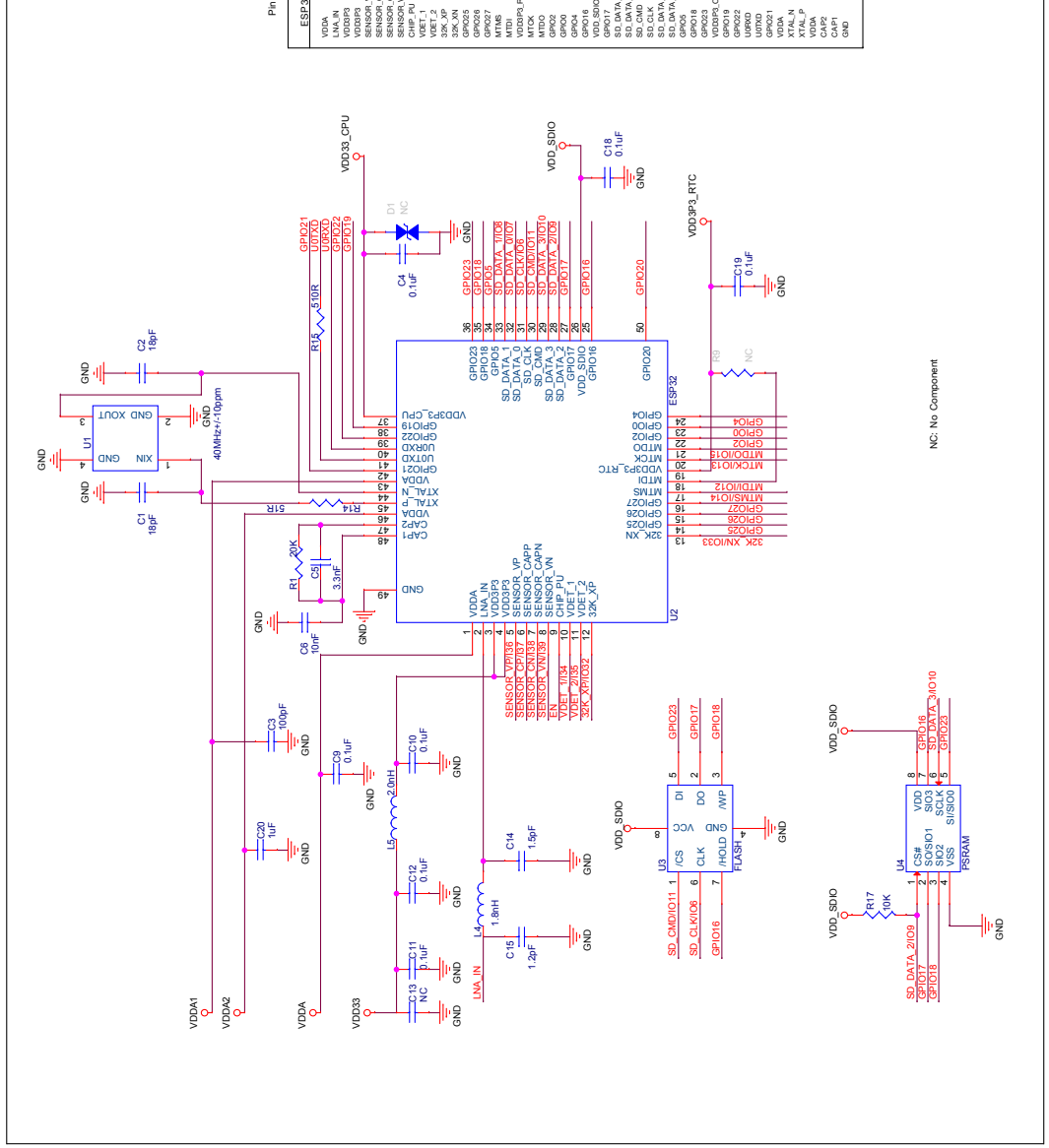
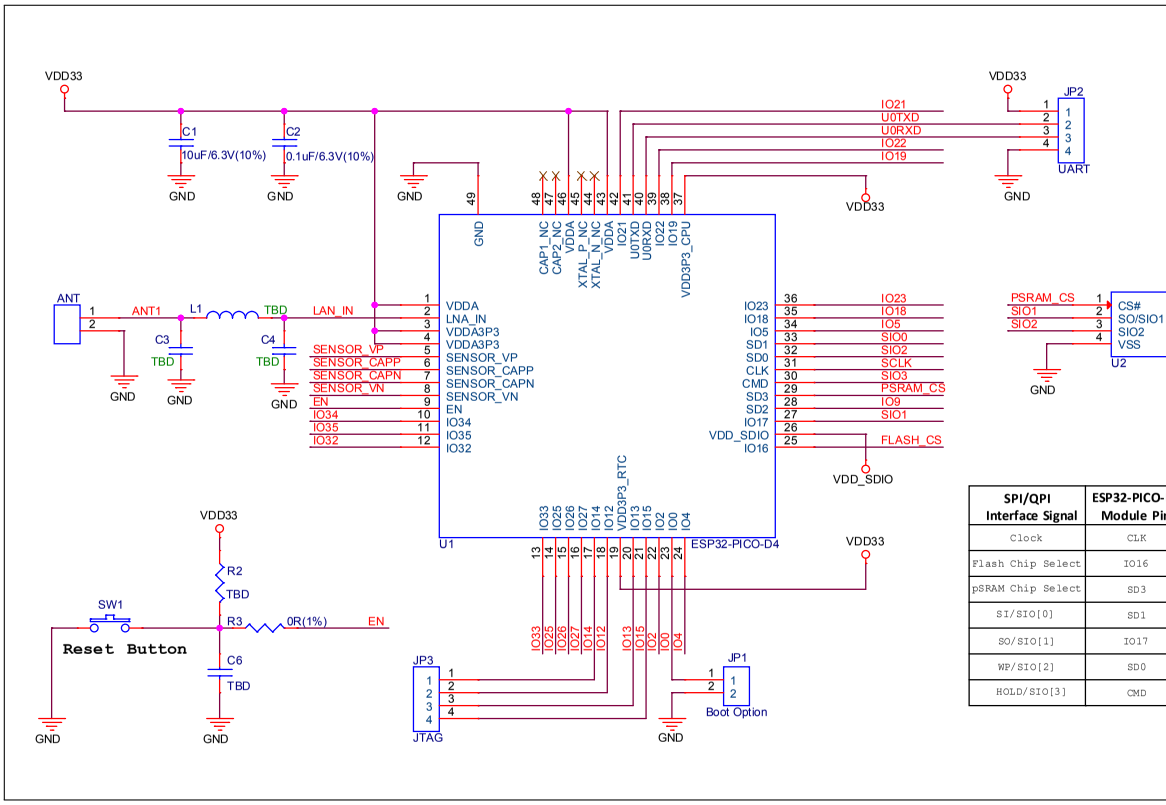


Figure 8: ESP32-PICO-V3-02 Schematics

6 Peripheral Schematics

This is the typical application circuit of the ESP32-PICO connected with peripheral components (for example, power supply
UART interface).



SPI/QPI Interface Signal	ESP32-PICO-D4 Module Pin
Clock	CLK
Flash Chip Select	IO16
pSRAM Chip Select	SD3
SI/SIO[0]	SD1
SO/SIO[1]	IO17
WP/SIO[2]	SD0
HOLD/SIO[3]	CMD

Figure 9: ESP32-PICO-D4 Peripheral Schematics

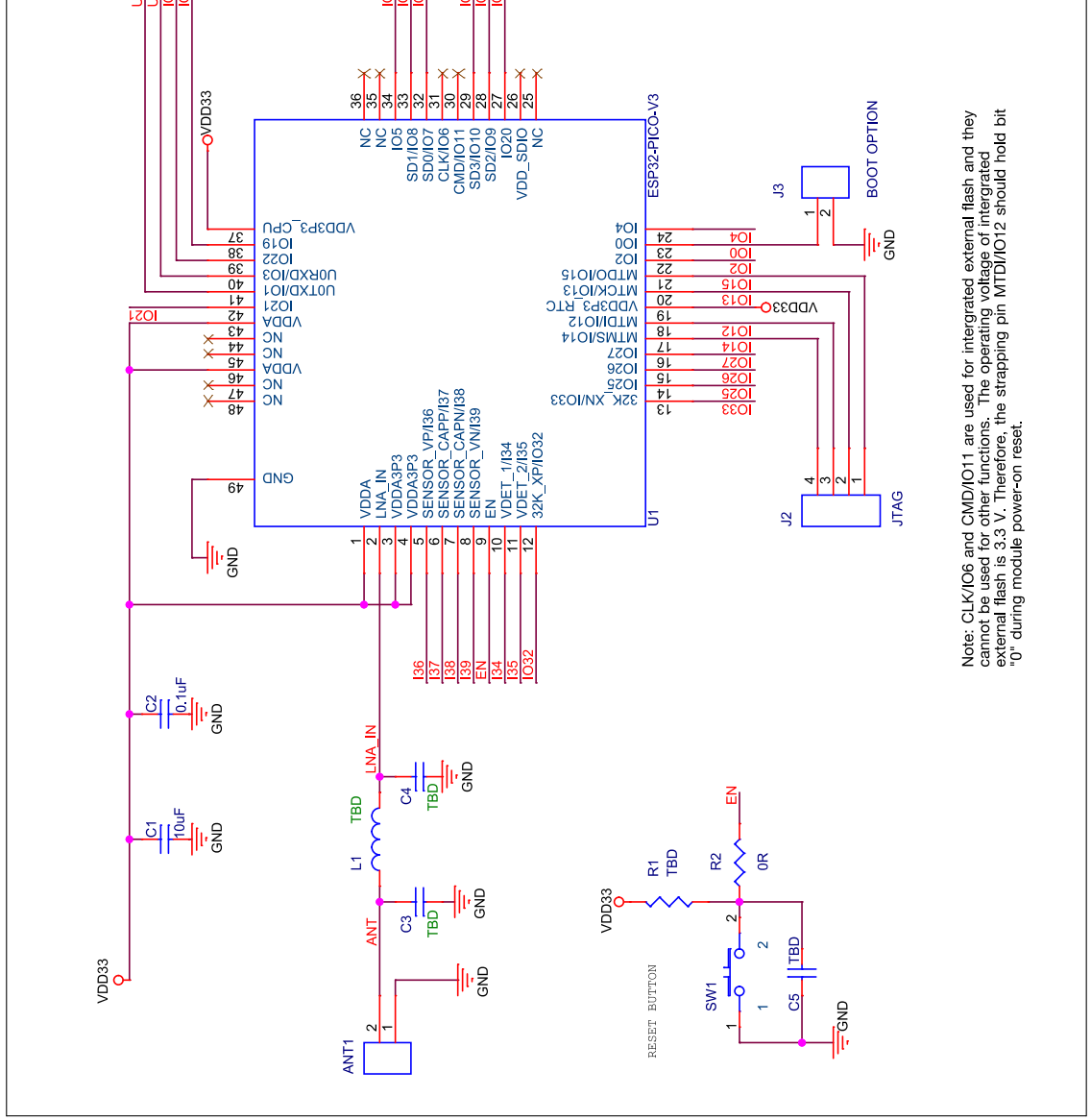


Figure 10: ESP32-PICO-V3 Peripheral Schematics

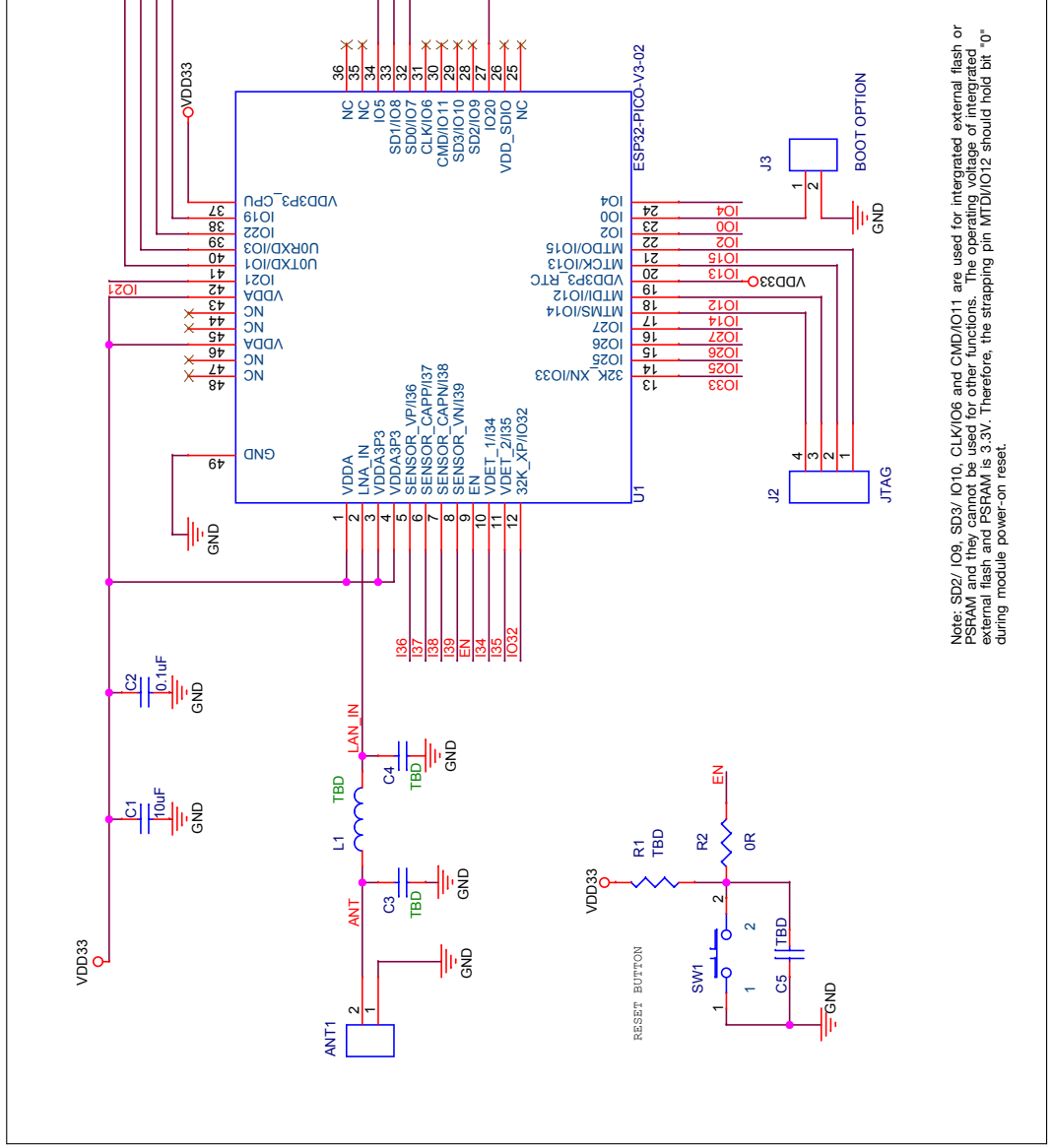
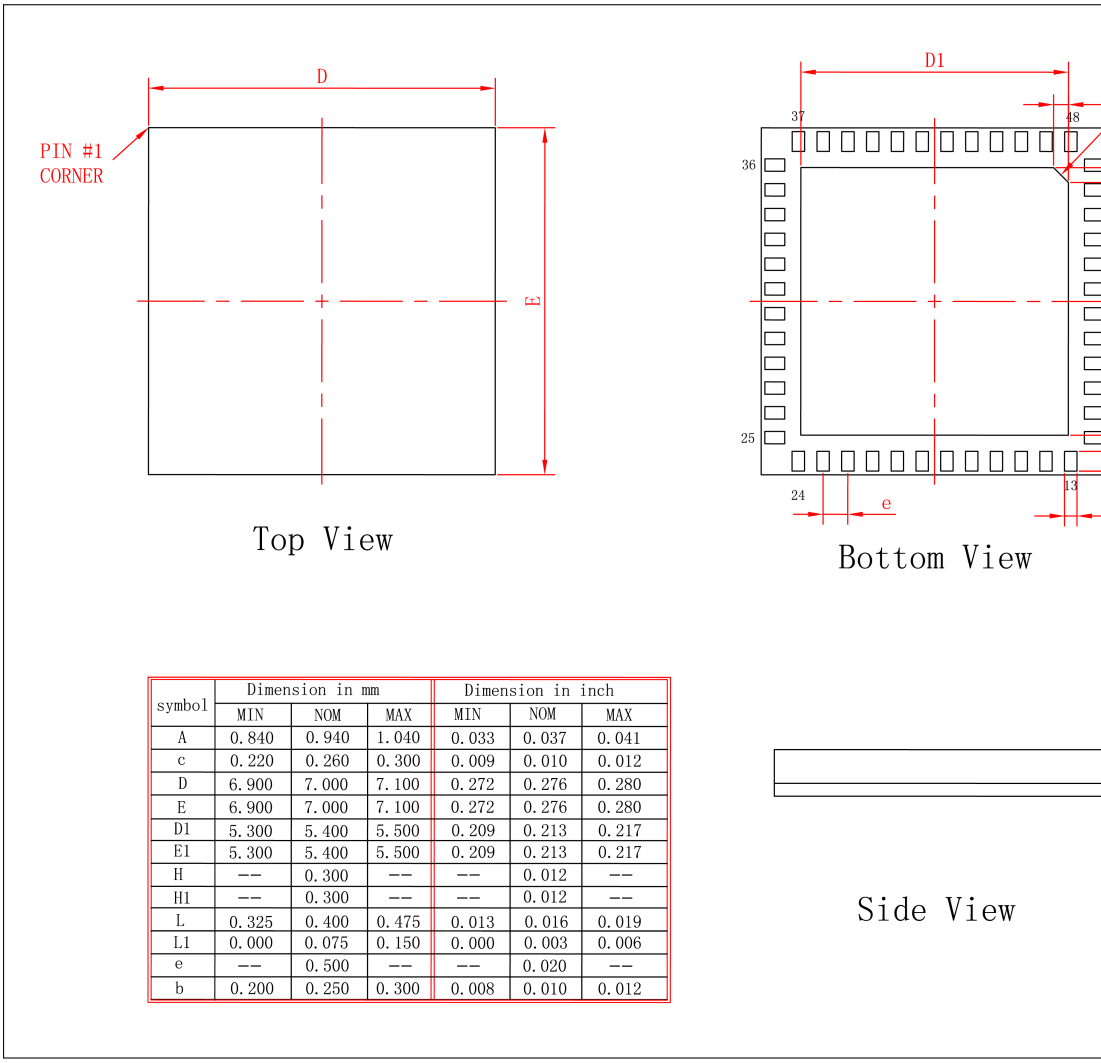


Figure 11: ESP32-PICO-V3-02 Peripheral Schematics

Note:

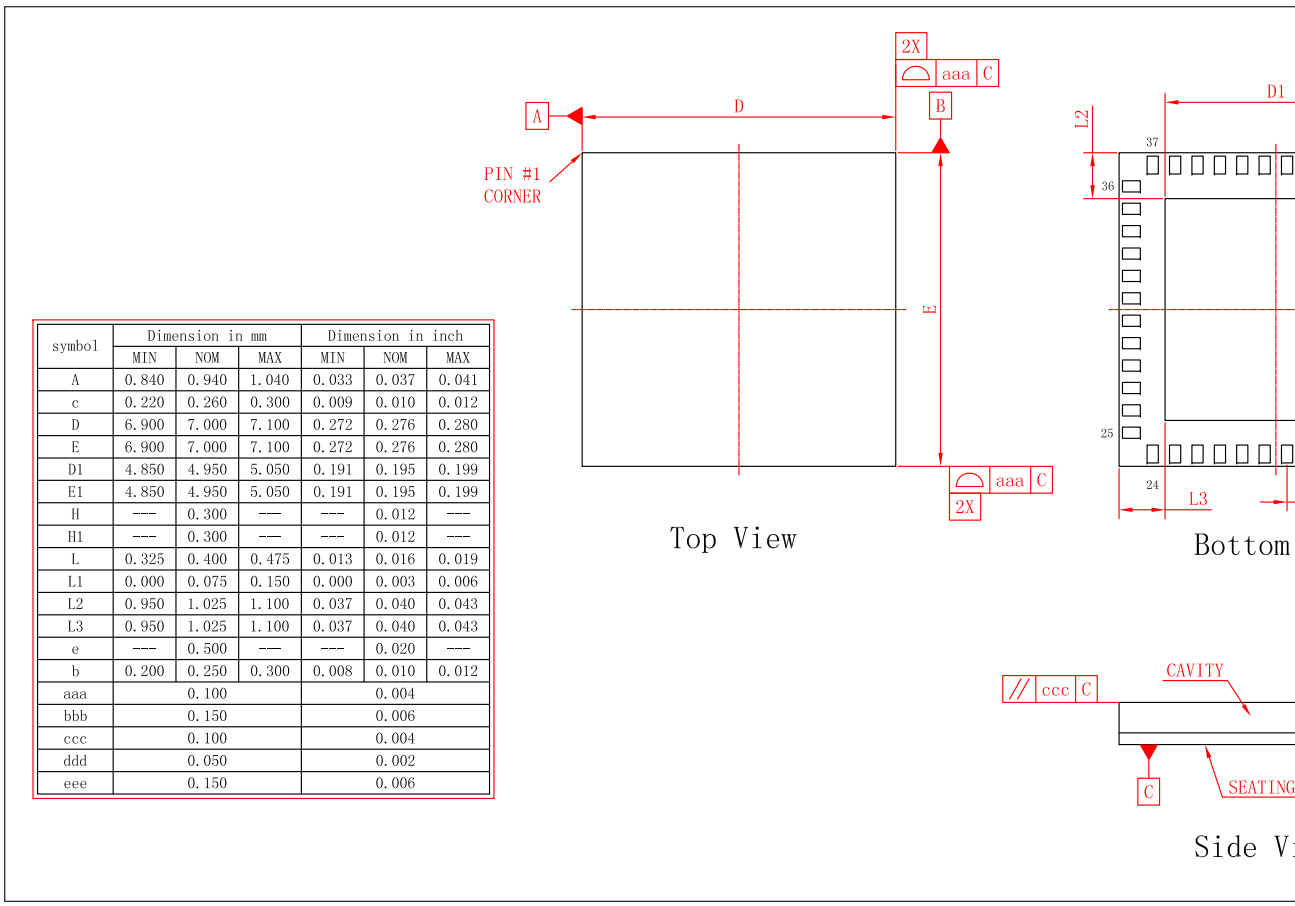
To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recomme
R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the SiP and the power-
ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Series Datasheet*.

7 Package Information



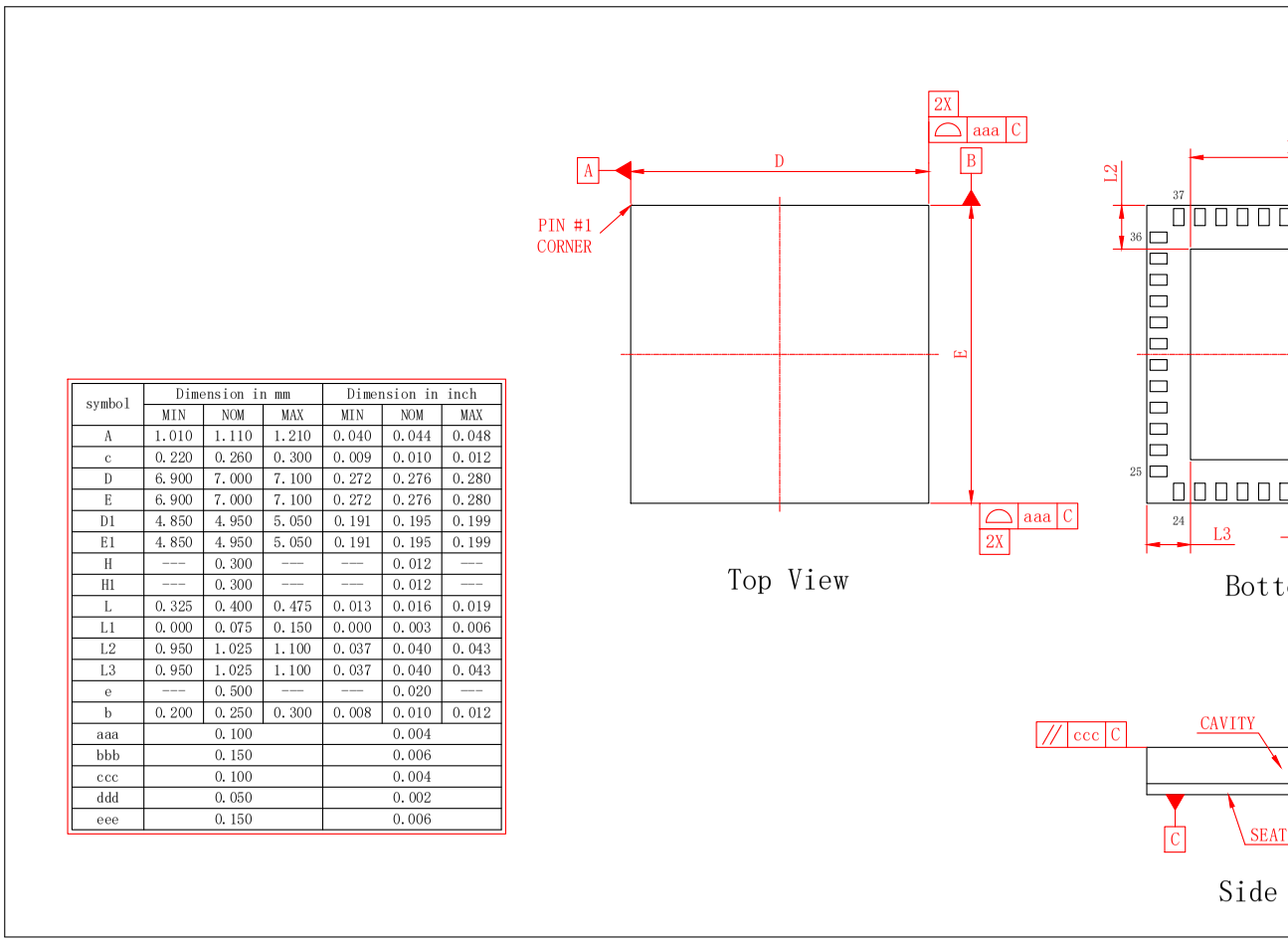
symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	5.300	5.400	5.500	0.209	0.213	0.217
E1	5.300	5.400	5.500	0.209	0.213	0.217
H	--	0.300	--	--	0.012	--
H1	--	0.300	--	--	0.012	--
L	0.325	0.400	0.475	0.013	0.016	0.019
L1	0.000	0.075	0.150	0.000	0.003	0.006
e	--	0.500	--	--	0.020	--
b	0.200	0.250	0.300	0.008	0.010	0.012

Figure 12: ESP32-PICO-D4 Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	4.850	4.950	5.050	0.191	0.195	0.199
E1	4.850	4.950	5.050	0.191	0.195	0.199
H	---	0.300	---	---	0.012	---
H1	---	0.300	---	---	0.012	---
L	0.325	0.400	0.475	0.013	0.016	0.019
L1	0.000	0.075	0.150	0.000	0.003	0.006
L2	0.950	1.025	1.100	0.037	0.040	0.043
L3	0.950	1.025	1.100	0.037	0.040	0.043
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.150			0.006		

Figure 13: ESP32-PICO-V3 Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.010	1.110	1.210	0.040	0.044	0.048
c	0.220	0.260	0.300	0.009	0.010	0.012
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	4.850	4.950	5.050	0.191	0.195	0.199
E1	4.850	4.950	5.050	0.191	0.195	0.199
H	---	0.300	---	---	0.012	---
H1	---	0.300	---	---	0.012	---
L	0.325	0.400	0.475	0.013	0.016	0.019
L1	0.000	0.075	0.150	0.000	0.003	0.006
L2	0.950	1.025	1.100	0.037	0.040	0.043
L3	0.950	1.025	1.100	0.037	0.040	0.043
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.150			0.006		

Figure 14: ESP32-PICO-V3-02 Package

8 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 15 *ESP32-PICO PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 15. You can view the source files for ESP32-PICO-D4, ESP32-PICO-V3, and ESP2-PICO-V3-02 with Autodesk Viewer.

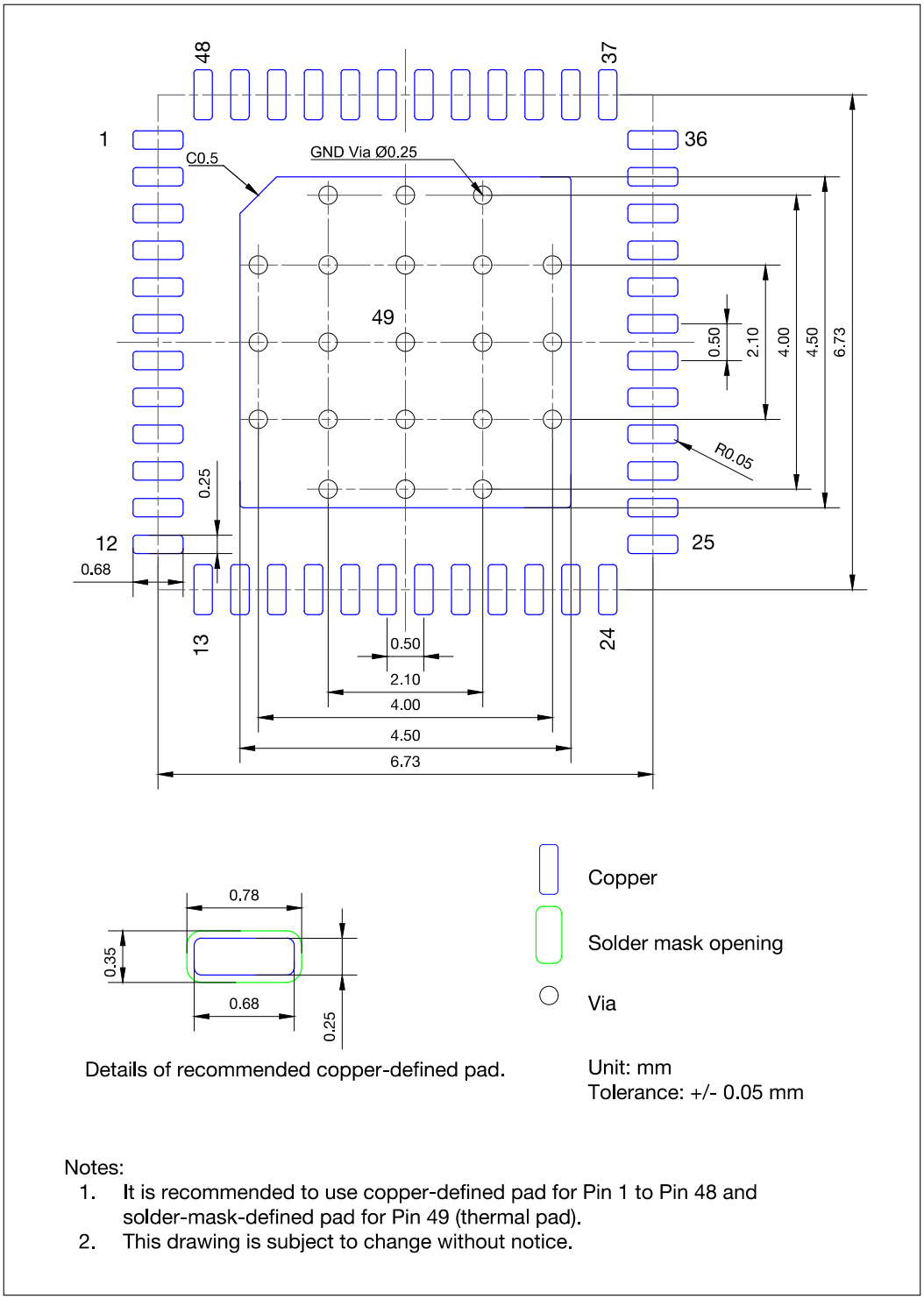


Figure 15: ESP32-PICO PCB Land Pattern

9 ESP32-PICO PCB Stencil

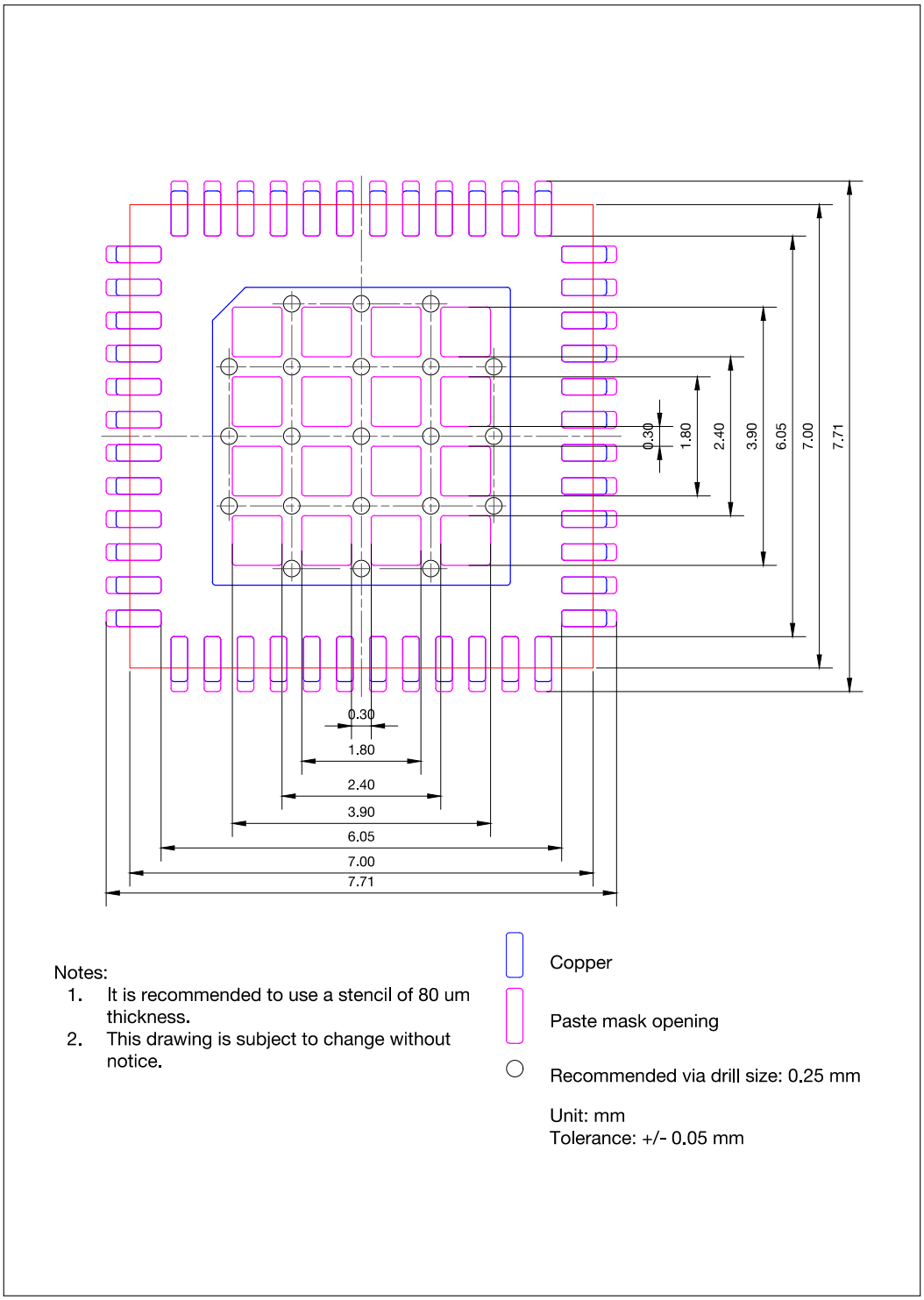


Figure 16: ESP32-PICO PCB STENCIL

10 Ultrasonic Vibration

Avoid exposing the device to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the crystal and lead to its malfunction or even failure. As a consequence, **the device may stop working or its performance may deteriorate**.

11 Migration Guide

This section provides an overview of the software and hardware changes when migrating from the existing module design based on an older ESP32-PICO variant to the new design based on a newer ESP32-PICO variant.

11.1 Migrating from ESP32-PICO-D4 to ESP32-PICO-V3

ESP32-PICO-D4 is the first introduced ESP32-PICO variant with ESP32 chip revision v1.0 or v1.1. ESP32-PICO-V3 contains a newer ESP32 chip inside (v3.0 or v3.1). For information about possible hardware and software changes in ESP32 chip revision v3.0, refer to *ESP32 Chip Revision v3.0 User Guide* .

ESP32-PICO-D4 and ESP32-PICO-V3 are not 1:1 pin-compatible. For changes in pin layout and functions, refer to Section 2.4 Pin Compatibility Between ESP32-PICO Variants.

Both ESP32-PICO-D4 and ESP32-PICO-V3 are produced with in-package flash. ESP32-PICO-D4 can connect to external PSRAM. However, ESP32-PICO-V3 cannot connect to external PSRAM.

EMC compliance and RF performance tests should be repeated after a design is updated to use ESP32-PICO-V3.

11.2 Migrating from ESP32-PICO-V3 to ESP32-PICO-V3-02

ESP32-PICO-V3-02 is a memory upgrade of ESP32-PICO-V3. ESP32-PICO-V3-02 has both in-package flash and PSRAM, while ESP32-PICO-V3 has only flash. It is not possible for both variants to connect to external PSRAM.

ESP32-PICO-V3-02 is designed to be largely pin-compatible with ESP32-PICO-V3, and thus requires only minor changes during migration. For changes in pin layout and functions, refer to Section 2.4 Pin Compatibility Between ESP32-PICO Variants.

EMC compliance and RF performance tests should be repeated after a design is updated to use ESP32-PICO-V3-02.

11.3 Summary

As summarized in this migration guide, there are minimal or no hardware and software changes required when migrating to newer ESP32-PICO variants. If you have any problems with migration, please contact Espressif Technical Support.

12 Related Documentation and Resources

Related Documentation

- ESP32 Series Datasheet – Specifications of the ESP32 hardware.
- ESP32 Technical Reference Manual – Detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Design Guidelines – Guidelines on how to integrate the ESP32 into your hardware product.
- ESP32 ECO and Workarounds for Bugs – Correction of ESP32 design errors.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32 Series SoCs* – Browse through all ESP32 SoCs.
  https://espressif.com/en/products/socs?id=ESP32
- *ESP32 Series Modules* – Browse through all ESP32-based modules.
  https://espressif.com/en/products/modules?id=ESP32
- *ESP32 Series DevKits* – Browse through all ESP32-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

Contact Us

- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2023-12-5	v1.0	Consolidated the three datasheets of ESP32-PICO variants into one. During the migration, some updates, improvements, and clarifications were made throughout the documentation. Major updates include: • Added Section 2.4 Pin Compatibility Between ESP32-PICO Variants • Added Section 10 Ultrasonic Vibration • Added Section 11 Migration Guide If you would like to check previous versions of the individual datasheets, please submit documentation feedback.

www.espressif.com

Disclaimer and Copyright Notice

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ESP32-PICO-V3-02 on WIN SOURCE
- Espressif Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management