



**THE DATASHEET OF  
DS26401DK**



# DS26401DK Octal T1/E1/J1 Framer Design Kit Daughter Card

[www.maxim-ic.com](http://www.maxim-ic.com)

## GENERAL DESCRIPTION

The DS26401DK is an easy-to-use evaluation board for the DS26401 octal T1/E1/J1 framer. It is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS26401DK comes complete with a DS26401 octal framer, two DS21448 quad LIUs, transformers, termination resistors, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and the Dallas' ChipView software give point-and-click access to configurations and status registers from a Windows®-based PC. On-board LEDs indicate loss-of-signal, loss-of-frame, and interrupt status.

Each DS26401DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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## DESIGN KIT CONTENTS

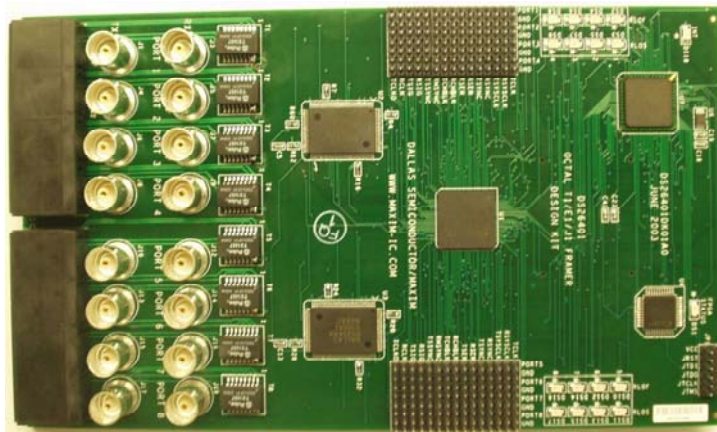
DS26401DK Board  
 DK101 Low-Cost Motherboard  
 CD-ROM  
     ChipView Software  
     DS26401DK Data Sheet  
     DK101 Data Sheet  
     DS26401 Data Sheet  
     DS21448 Data Sheet  
     DS26401 Errata Sheet  
     DS21448 Errata Sheet

## FEATURES

- Demonstrates Key Functions of the DS26401 Octal T1/E1/J1 Framer
- Includes Two DS21448 Quad LIUs, Transformers, BNC and RJ45 Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS26401 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal, Loss-of-Frame, and Interrupt
- Easy-to-Read Silk-Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

## ORDERING INFORMATION

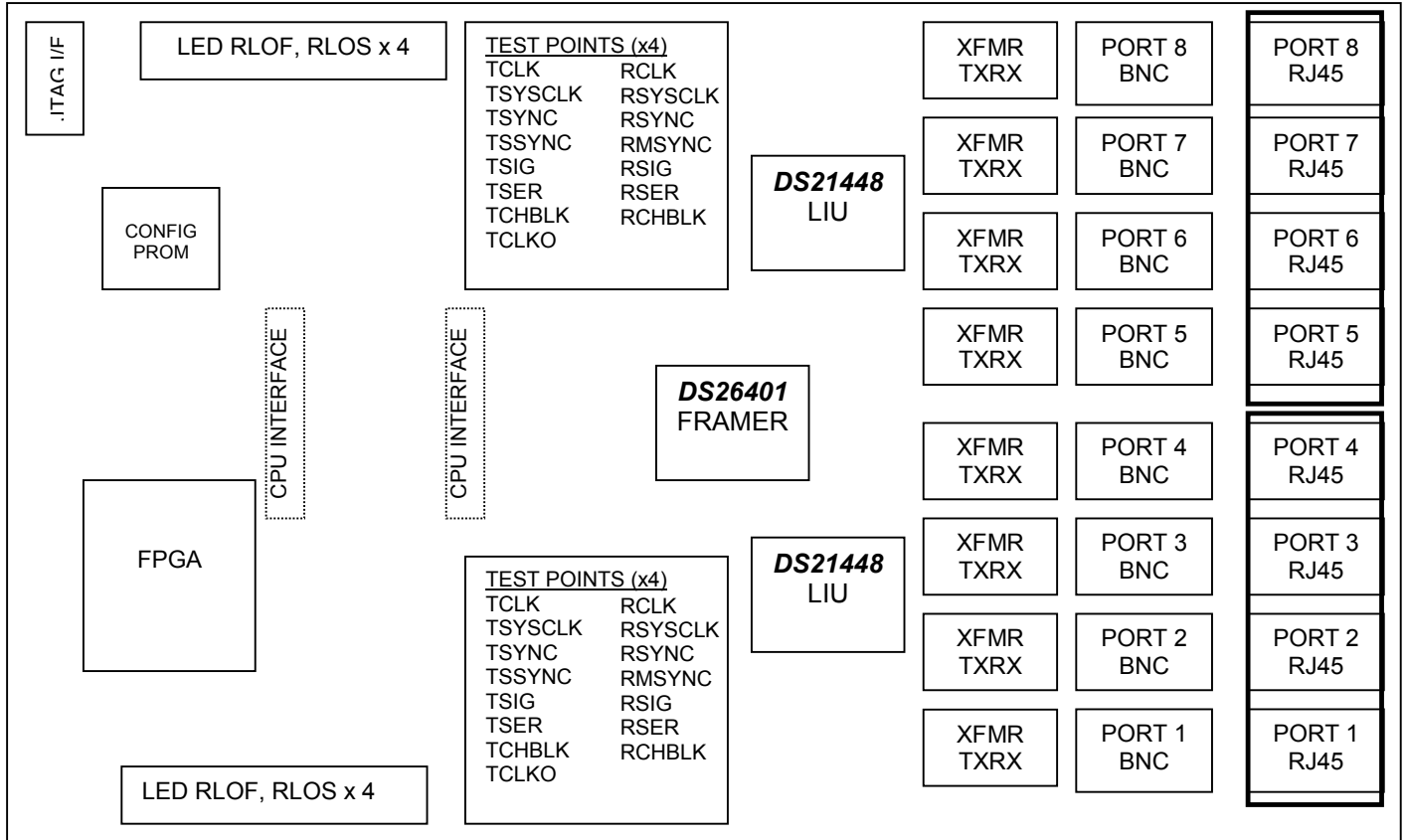
PART	DESCRIPTION
DS26401DK	DS26401 Demo Kit Daughter Card (with included DK101 motherboard)



**COMPONENT LIST**

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C3, C5, C7, C9, C11, C13, C15, C17–C24, C26, C28–C31, C35–C42	29	00.1 $\mu$ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C4, C6, C8, C10, C12, C14, C16	8	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
DS1, DS18	2	LED, green, SMD	Panasonic	LN1351C
DS2–DS17	16	LED, red, SMD	Panasonic	LN1251C
J1, J3–J10, J12–J18	16	5-pin connectors, 75 $\Omega$ BNC vertical	Bourns	CP-BNCPC-004
J2, J11	2	Right-angle, RJ45 8-pin 4-port jack	3M Electronics	43223-8140
J19, J20	2	50-pin headers, socket, SMD dual row, vertical	Samtec	TFM-125-02-S-D-LC
J21, J23, J25, J27, J29, J31, J33, J35	8	20-pin headers, dual row, vertical	Samtec	HDR-TSW-110-14-T-D
J22, J24, J26, J28, J30, J32, J34, J36	8	10-pin headers, dual row, vertical	Murrietta	N/A
JP1	1	12-pin connector, dual row, vertical	Murrietta	N/A
R1, R2, R5, R6, R9, R10, R13, R14, R17, R18, R21, R22, R25, R26, R29, R30, R67	17	0 $\Omega$ 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R3, R4, R7, R8, R11, R12, R15, R16, R19, R20, R23, R24, R27, R28, R31, R32	16	60.4 $\Omega$ 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF60R4V
R33–R35	3	10k $\Omega$ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R36, R37, R68	3	330 $\Omega$ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R38, R59–R66	9	30.1 $\Omega$ 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF30R1V
R39–R54	16	300 $\Omega$ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ301V
R55–R58	4	10.0k $\Omega$ 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1002V
T1–T8	8	XFMR, dual, 16-pin SMT	Pulse Engineering	TX1467
U1	1	Octal T1/E1/J1 framer	Dallas Semiconductor	DS26401
U2, U3	2	3.3V E1/T1/J1 quad LIU 128-pin LQFP, 0°C to +70°C	Dallas Semiconductor	DS21448L
U4	1	1M PROM for FPGA 44-pin TQFP	Xilinx	XC18V01VQ44C_U
U6	1	8-pin $\mu$ MAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	XILINX Spartan 2.5V FPGA, 256-pin BGA	Xilinx	XC2S50-5FG256C

# BOARD FLOORPLAN



## QUICK SETUP (REGISTER VIEW)

- Connect DS26401DK to DK101 motherboard.
- Connect serial cable to a PC and DK101.
- Power DK101 with 3.3V.
- Load ChipView software.
- Select COM port.
- Select Register View.
- For T1 applications, load the *401\_global\_t1\_DS26401DC.def* file. For E1 applications, load the *401\_global\_e1\_DS26401DC.def* file.
- Make sure that all the register settings are correct for the proper function desired for the DS26401DK.

Please refer to the DS26401 data sheet ([www.maxim-ic.com/DS26401](http://www.maxim-ic.com/DS26401)) and the DS21448 data sheet ([www.maxim-ic.com/DS21448](http://www.maxim-ic.com/DS21448)) for all questions pertaining to device functionality.

## ADDRESS MAP

DK101 daughter card address space begins at 0x81000000.

DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space.

**Table 1. Daughter Card Address Map**

SPAN NUMBER	OFFSET		
	DS26401	DS21448	FPGA
1	0x1000	0x2000	0x10
2	0x1200	0x3000	0x20
3	0x1400	0x4000	0x30
4	0x1600	0x5000	0x40
5	0x1800	0x6000	0x50
6	0x1A00	0x7000	0x60
7	0x1C00	0x8000	0x70
8	0x1E00	0x9000	0x80

Registers in the FPGA can be easily modified using ChipView.exe host-based user-interface software along with the definition file named *DS26401DC\_FPGA.def*.

## FPGA REGISTER MAP

**Table 2. FPGA Register map**

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0010 0x0020 0x0030 0x0040 0x0050 0x0060 0x0070 0x0080	TSIG_SR -1 TSIG_SR -2 TSIG_SR -3 TSIG_SR -4 TSIG_SR -5 TSIG_SR -6 TSIG_SR -7 TSIG_SR -8	Control	DS26401 TSIG Pin Setting Port 1 DS26401 TSIG Pin Setting Port 2 DS26401 TSIG Pin Setting Port 3 DS26401 TSIG Pin Setting Port 4 DS26401 TSIG Pin Setting Port 5 DS26401 TSIG Pin Setting Port 6 DS26401 TSIG Pin Setting Port 7 DS26401 TSIG Pin Setting Port 8
0X0011 0X0021 0X0031 0X0041 0x0051 0x0061 0x0071 0x0081	TSER_SR -1 TSER_SR -2 TSER_SR -3 TSER_SR -4 TSER_SR -5 TSER_SR -6 TSER_SR -7 TSER_SR -8	Control	DS26401 TSER Pin Setting Port 1 DS26401 TSER Pin Setting Port 2 DS26401 TSER Pin Setting Port 3 DS26401 TSER Pin Setting Port 4 DS26401 TSER Pin Setting Port 5 DS26401 TSER Pin Setting Port 6 DS26401 TSER Pin Setting Port 7 DS26401 TSER Pin Setting Port 8
0X0012 0X0022 0X0032 0X0042 0X0052 0X0062 0X0072 0X0082	TSSYNC_SR -1 TSSYNC_SR -2 TSSYNC_SR -3 TSSYNC_SR -4 TSSYNC_SR -5 TSSYNC_SR -6 TSSYNC_SR -7 TSSYNC_SR -8	Control	DS26401 TSSYNC Source Port 1 DS26401 TSSYNC Source Port 2 DS26401 TSSYNC Source Port 3 DS26401 TSSYNC Source Port 4 DS26401 TSSYNC Source Port 5 DS26401 TSSYNC Source Port 6 DS26401 TSSYNC Source Port 7 DS26401 TSSYNC Source Port 8
0X0013 0X0023 0X0033 0X0043 0X0053 0X0063 0X0073 0X0083	TSYSCLK -1 TSYSCLK -2 TSYSCLK -3 TSYSCLK -4 TSYSCLK -5 TSYSCLK -6 TSYSCLK -7 TSYSCLK -8	Control	DS26401 TSYSCLK Source Port 1 DS26401 TSYSCLK Source Port 2 DS26401 TSYSCLK Source Port 3 DS26401 TSYSCLK Source Port 4 DS26401 TSYSCLK Source Port 5 DS26401 TSYSCLK Source Port 6 DS26401 TSYSCLK Source Port 7 DS26401 TSYSCLK Source Port 8
0X0014 0X0024 0X0034 0X0044 0X0054 0X0064 0X0074 0X0084	RSYSCLK -1 RSYSCLK -2 RSYSCLK -3 RSYSCLK -4 RSYSCLK -5 RSYSCLK -6 RSYSCLK -7 RSYSCLK -8	Control	DS26401 RSYSCLK Source Port 1 DS26401 RSYSCLK Source Port 2 DS26401 RSYSCLK Source Port 3 DS26401 RSYSCLK Source Port 4 DS26401 RSYSCLK Source Port 5 DS26401 RSYSCLK Source Port 6 DS26401 RSYSCLK Source Port 7 DS26401 RSYSCLK Source Port 8

**Table 2. Register Map (continued)**

OFFSET	NAME	TYPE	DESCRIPTION
0X0015	TCLK –1	Control	DS26401TCLK Source Port 1
0X0025	TCLK –2		DS26401TCLK Source Port 2
0X0035	TCLK –3		DS26401TCLK Source Port 3
0X0045	TCLK –4		DS26401TCLK Source Port 4
0X0055	TCLK –5		DS26401TCLK Source Port 5
0X0065	TCLK –6		DS26401TCLK Source Port 6
0X0075	TCLK –7		DS26401TCLK Source Port 7
0X0085	TCLK –8		DS26401TCLK Source Port 8
0X0016	RSYNC –1	Control	DS26401RSYNC Source Port 1
0X0026	RSYNC –2		DS26401RSYNC Source Port 2
0X0036	RSYNC –3		DS26401RSYNC Source Port 3
0X0046	RSYNC –4		DS26401RSYNC Source Port 4
0X0056	RSYNC –5		DS26401RSYNC Source Port 5
0X0066	RSYNC –6		DS26401RSYNC Source Port 6
0X0076	RSYNC –7		DS26401RSYNC Source Port 7
0X0086	RSYNC –8		DS26401RSYNC Source Port 8
0X0017	TSYNC –1	Control	DS26401TSYNC Source Port 1
0X0027	TSYNC –2		DS26401TSYNC Source Port 2
0X0037	TSYNC –3		DS26401TSYNC Source Port 3
0X0047	TSYNC –4		DS26401TSYNC Source Port 4
0X0057	TSYNC –5		DS26401TSYNC Source Port 5
0X0067	TSYNC –6		DS26401TSYNC Source Port 6
0X0077	TSYNC –7		DS26401TSYNC Source Port 7
0X0087	TSYNC –8		DS26401TSYNC Source Port 8
0X0090	CLK	Control	LIU MCLK and REF CLK Source

**ID Registers****BID: BOARD ID (Offset = 0X0000)**

BID is read-only with a value of 0xD.

**XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)**

XBIDH is read-only with a value of 0x0.

**XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)**

XBIDM is read-only with a value of 0x1.

**XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)**

XBIDL is read-only with a value of 0x6.

**BREV: BOARD FAB REVISION (Offset = 0X0005)**

BREV is read-only and displays the current fab revision.

**AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)**

AREV is read-only and displays the current assembly revision.

**PREV: PLD REVISION (Offset = 0X0007)**

PREV is read-only and displays the current PLD firmware revision.

## Control Registers

Register Name: **TSIG\_SR**

Register Description: **DS26401 TSIG x Pin Setting**

Register Offset: **0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

**Bit 0 to 7: DS26401 Port x TSIG Source (D7, D6, D5, D4, D3, D2, D1, D0)**

The source for TSER is Defined as shown in Table 3.

**Table 3. TSERx Source Definition**

D3, D2, D1, D0	TSIG CONNECTION
0000	Tri-state TSIG
0001	Drive TSIG with RSIG1
0010	Drive TSIG with RSIG2
0011	Drive TSIG with RSIG3
0100	Drive TSIG with RSIG4
0101	Drive TSIG with RSIG5
0110	Drive TSIG with RSIG6
0111	Drive TSIG with RSIG7
1000	Drive TSIG with RSIG8
1010	Drive TSIG with T1 OSC
1011	Drive TSIG with E1 OSC
1100	Drive TSIG with 16.384MHz
1101	Drive TSIG with a logic 0
1110	Drive TSIG with a logic 1
1111	Tri-state TSIG

**Note:** Initial values are such that all values are tri-stated.

Register Name: **TSER\_SR**

Register Description: **DS26401 TSERx Pin Setting**

Register Offset: **0x0011, 0x0021, 0x0031, 0x0041, 0x0051, 0x0061, 0x0071, 0x0081**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

**Bit 0 to 3: DS26401 Port x TSER Source (D3, D2, D1, D0)**

The source for TSER is Defined as shown in Table 4.

**Table 4. TSERx Source Definition**

D3, D2, D1, D0	TSER CONNECTION
0000	Tri-state TSER
0001	Drive TSER with RSER1
0010	Drive TSER with RSER2
0011	Drive TSER with RSER3
0100	Drive TSER with RSER4
0101	Drive TSER with RSER5
0110	Drive TSER with RSER6
0111	Drive TSER with RSER7
1000	Drive TSER with RSER8
1010	Drive TSER with T1 OSC
1011	Drive TSER with E1 OSC
1100	Drive TSER with 16.384MHz
1101	Drive TSER with a logic 0
1110	Drive TSER with a logic 1
1111	Tri-state TSER

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **TSSYNC\_SR**

Register Description: **DS26401 TSSYNCx Pin Setting**

Register Offset: **0x0012, 0x0022, 0x0032, 0x0042, 0x0052, 0x0062, 0x0072, 0x0082**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0
Default	0	0	0	0	0	1	0	1

**Bit 0 to 2: DS26401 Port x TSSYNC Source (D3, D2, D1, D0)**

The source for TSSYNC is Defined as shown in Table 5.

**Table 5. TSSYNCx Source Definition**

D3, D2, D1, D0	TSSYNC CONNECTION
0000	Tri-state TSSYNC
0001	Drive TSSYNC with RMSYNC1
0010	Drive TSSYNC with RMSYNC2
0011	Drive TSSYNC with RMSYNC3
0100	Drive TSSYNC with RMSYNC4
0101	Drive TSSYNC with RMSYNC5
0110	Drive TSSYNC with RMSYNC6
0111	Drive TSSYNC with RMSYNC7
1000	Drive TSSYNC with RMSYNC8
1010	Drive TSSYNC with T1 OSC
1011	Drive TSSYNC with E1 OSC
1100	Drive TSSYNC with 16.385MHz
1101	Drive TSSYNC with a logic 0
1110	Drive TSSYNC with a logic 1
1111	Tri-state TSSYNC

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **TSYSCLK\_SR**

Register Description: **DS26401 TSYSCLKx Pin Setting**

Register Offset: **0x0013, 0x0023, 0x0033, 0x0043, 0x0053, 0x0063, 0x0073, 0x0083**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

**Bit 0 to 2: DS26401 Port x TSYSCLKC Source (D3, D2, D1, D0)**

The source for TSYSCLK is Defined as shown in Table 6.

**Table 6. TSYSCLKx Source Definition**

D3, D2, D1, D0	TSYSCLK CONNECTION
0000	Tri-state TSYSCLK
0001	Drive TSYSCLK with RCHBLK 1
0010	Drive TSYSCLK with RCHBLK 2
0011	Drive TSYSCLK with RCHBLK 3
0100	Drive TSYSCLK with RCHBLK 4
0101	Drive TSYSCLK with RCHBLK 5
0110	Drive TSYSCLK with RCHBLK 6
0111	Drive TSYSCLK with RCHBLK 7
1000	Drive TSYSCLK with RCHBLK 8
1001	BPCLK
1010	Drive TSYSCLK with T1 OSC
1011	Drive TSYSCLK with E1 OSC
1100	Drive TSYSCLK with 16.385MHz
1101	Drive TSYSCLK with a logic 0
1110	Drive TSYSCLK with a logic 1
1111	Tri-state TSYSCLK

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **RSYSCLK\_SR**

Register Description: **DS26401 RSYSCLKx Pin Setting**

Register Offset: **0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

**Bit 0 to 2: DS26401 Port x RSYSCLKC Source (D3, D2, D1, D0)**

The source for RSYSCLK is Defined as shown in Table 7.

**Table 7. RSYSCLKx Source Definition**

D3, D2, D1, D0	RSYSCLK CONNECTION
0000	Tri-state RSYSCLK
0001	Drive RSYSCLK with TCHBLK 1
0010	Drive RSYSCLK with TCHBLK 2
0011	Drive RSYSCLK with TCHBLK 3
0100	Drive RSYSCLK with TCHBLK 4
0101	Drive RSYSCLK with TCHBLK 5
0110	Drive RSYSCLK with TCHBLK 6
0111	Drive RSYSCLK with TCHBLK 7
1000	Drive RSYSCLK with TCHBLK 8
1001	BPCLK
1010	Drive RSYSCLK with T1 OSC
1011	Drive RSYSCLK with E1 OSC
1100	Drive RSYSCLK with 16.385MHz
1101	Drive RSYSCLK with a logic 0
1110	Drive RSYSCLK with a logic 1
1111	Tri-state RSYSCLK

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **TCLK\_SR**

Register Description: **DS26401 TCLKx Pin Setting**

Register Offset: **0x0015, 0x0025, 0x0035, 0x0045, 0x0055, 0x0065, 0x0075, 0x0085**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

**Bit 0 to 2: DS26401 Port x TCLK Source (D3, D2, D1, D0)**

The source for TCLK is Defined as shown in Table 8.

**Table 8. TCLKx Source Definition**

D3, D2, D1, D0	TCLK CONNECTION
0000	Tri-state TCLK
0001	Drive TCLK with TCLK 1
0010	Drive TCLK with TCLK 2
0011	Drive TCLK with TCLK 3
0100	Drive TCLK with TCLK 4
0101	Drive TCLK with TCLK 5
0110	Drive TCLK with TCLK 6
0111	Drive TCLK with TCLK 7
1000	Drive TCLK with TCLK 8
1010	Drive TCLK with T1 OSC
1011	Drive TCLK with E1 OSC
1100	Drive TCLK with 16.385MHz
1101	Drive TCLK with a logic 0
1110	Drive TCLK with a logic 1
1111	Tri-state TCLK

**Note:** Initial values are such that all ports are tri-stated.

Also note that RCLK from the LIU (DS21448) does not go directly to the FPGA. However, it is routed to the DS26401 and a test header. To get RCLK to fan out to all the ports on the DS26401, simply tri-state a port on the FPGA and manually jumper the RCLK X pin to the TCLK X pin. Then you can route that signal with register values 0001 to 1000 in the TCLK\_SR.

Register Name: **RSYNC\_SR**Register Description: **DS26401 RSYNCx Pin Setting**Register Offset: **0x0016, 0x0026, 0x0036, 0x0046, 0x0056, 0x0066, 0x0076, 0x0086**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

**Bit 0 to 2: DS26401 Port x RSYNC Source (D3, D2, D1, D0)**

The source for RSYNC is Defined as shown in Table 9.

**Table 9. RSYNCx Source Definition**

D3, D2, D1, D0	RSYNC CONNECTION
0000	Tri-state RSYNC
0001	Drive RSYNC with TSYNC 1
0010	Drive RSYNC with TSYNC 2
0011	Drive RSYNC with TSYNC 3
0100	Drive RSYNC with TSYNC 4
0101	Drive RSYNC with TSYNC 5
0110	Drive RSYNC with TSYNC 6
0111	Drive RSYNC with TSYNC 7
1000	Drive RSYNC with TSYNC 8
1010	Drive RSYNC with T1 OSC
1011	Drive RSYNC with E1 OSC
1100	Drive RSYNC with 16.385MHz
1101	Drive RSYNC with a logic 0
1110	Drive RSYNC with a logic 1
1111	Tri-state RSYNC

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **TSYNC\_SR**Register Description: **DS26401 TSYNCx Pin Setting**Register Offset: **0x0017, 0x0027, 0x0037, 0x0047, 0x0057, 0x0067, 0x0077, 0x0087**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0

**Bit 0 to 2: DS26401 Port x TSYNC Source (D4, D3, D2, D1, D0)**

The source for TSYNC is Defined as shown in Table 10.

**Table 10. TSYNCx Source Definition**

D4, D3, D2, D1, D0	TSYNC CONNECTION
00000	Tri-state TSYNC
00001	Drive TSYNC with RSYNC 1
00010	Drive TSYNC with RSYNC 2
00011	Drive TSYNC with RSYNC 3
00100	Drive TSYNC with RSYNC 4
00101	Drive TSYNC with RSYNC 5
00110	Drive TSYNC with RSYNC 6
00111	Drive TSYNC with RSYNC 7
01000	Drive TSYNC with RSYNC 8
01010	Drive TSYNC with T1 OSC
01011	Drive TSYNC with E1 OSC
01100	Drive TSYNC with 16.385MHz
01101	Drive TSYNC with a logic 0
01110	Drive TSYNC with a logic 1
10001	Drive TSYNC with RMSYNC 1
10010	Drive TSYNC with RMSYNC 2
10011	Drive TSYNC with RMSYNC 3
10100	Drive TSYNC with RMSYNC 4
10101	Drive TSYNC with RMSYNC 5
10110	Drive TSYNC with RMSYNC 6
10111	Drive TSYNC with RMSYNC 7
11000	Drive TSYNC with RMSYNC 8
11111	Tri-state TSYNC

**Note:** Initial values are such that all ports are tri-stated.

Register Name: **CLK\_SR**Register Description: **DS21448 MCLK A, DS21448 MCLK B, and REF CLK**Register Offset: **0x0090**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

**Table 11. MCLK A Source Definition**

D1, D0	MCLK A (DS21448 PORTS 1 TO 4)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

**Note:** Initial values are such that MCLK is 2.048MHz.**Table 12. MCLK B Source Definition**

D3, D2	MCLK B (DS21448 PORTS 5 TO 8)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

**Note:** Initial values are such that that MCLK is 2.048MHz.**Table 13. MCLK A Source Definition**

D5, D4	REF CLK
00	Tri-state REF CLK
01	Drive REF with 1.544MHz
10	Drive REF with 2.048MHz
11	Tri-state REF CLK

**Note:** Initial values are such that REF is 2.048MHz.

## DS26401 AND DS21448 INFORMATION

For more information about the DS26401 and DS21448, please consult the respective data sheets, available on our website at [www.maxim-ic.com/DS26401](http://www.maxim-ic.com/DS26401) and [www.maxim-ic.com/DS21448](http://www.maxim-ic.com/DS21448).

## TECHNICAL SUPPORT

For technical support, please email your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

## SCHEMATICS

The DS26401DK schematics are featured in the following pages.

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DS26401 DESIGN KIT

CREATED BY

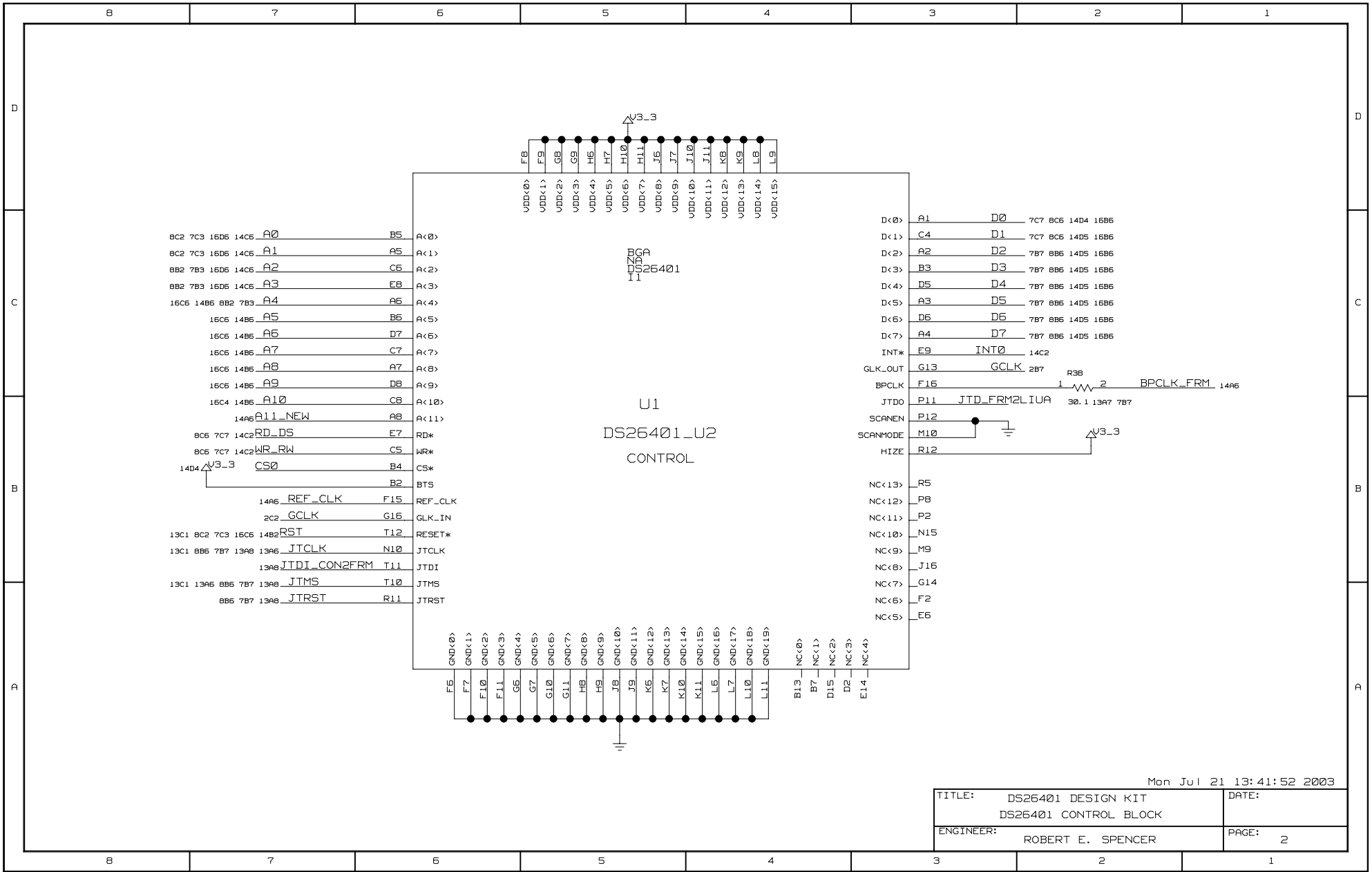
ROBERT E. SPENCER

JUNE 3, 2003

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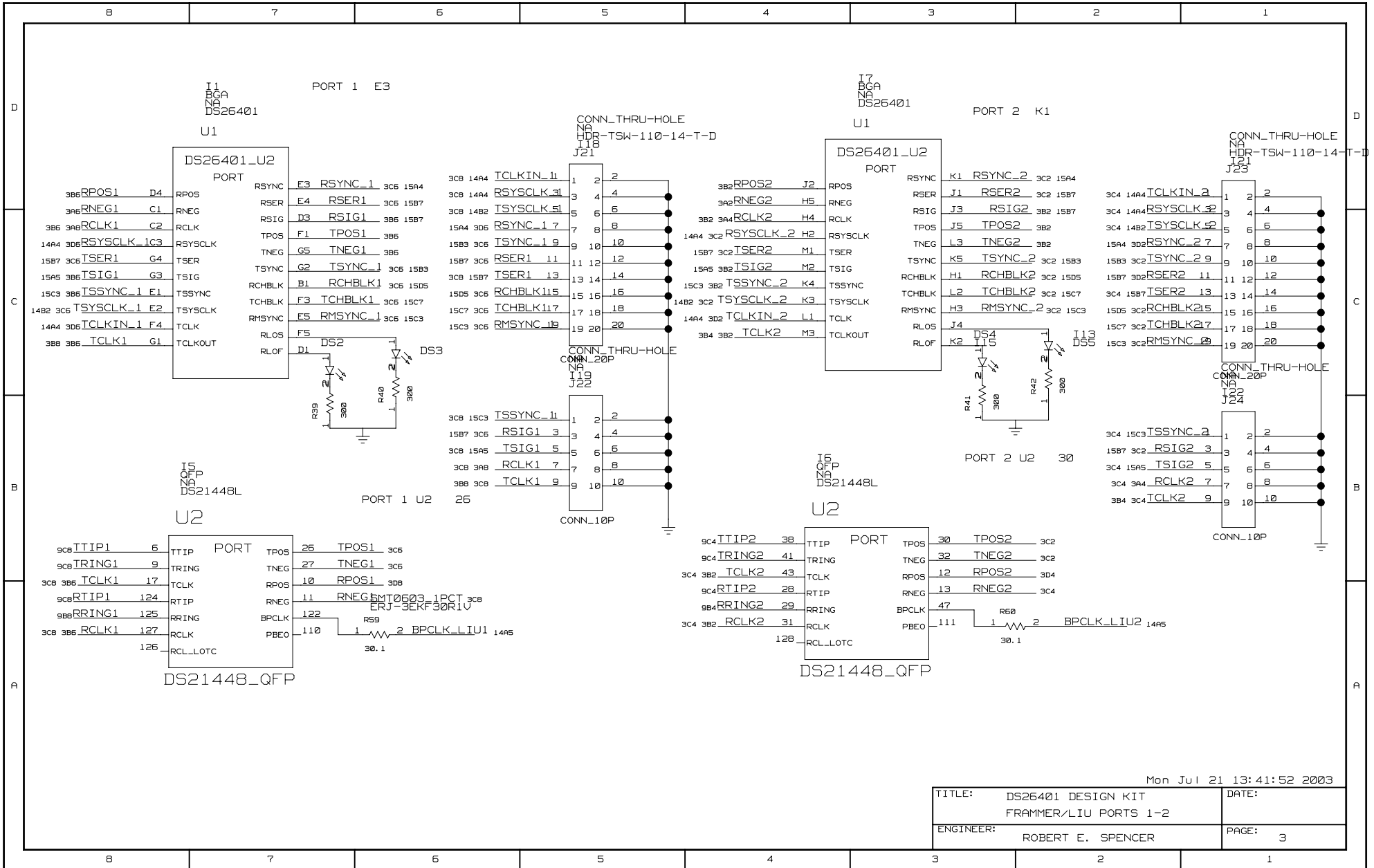
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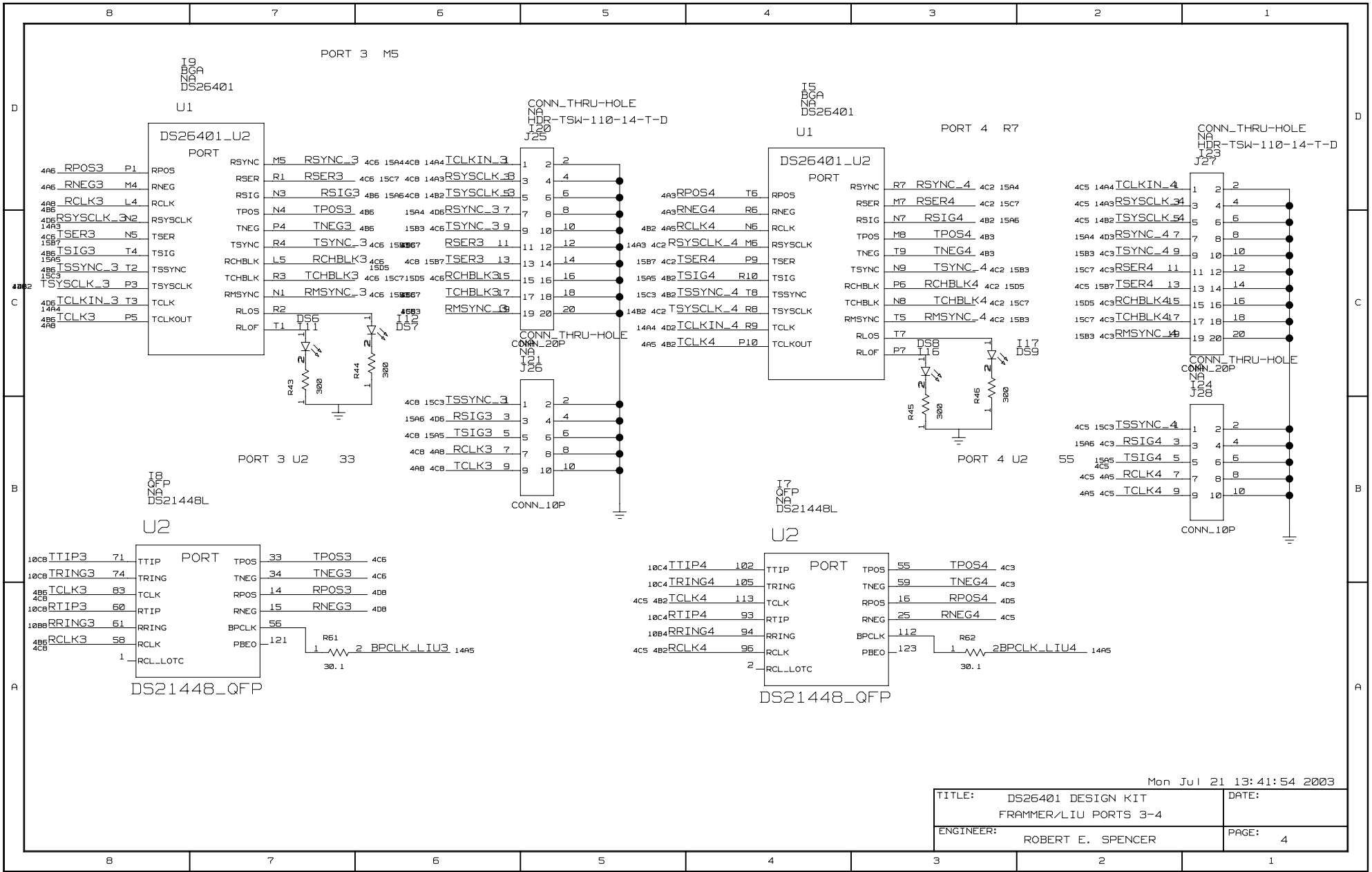
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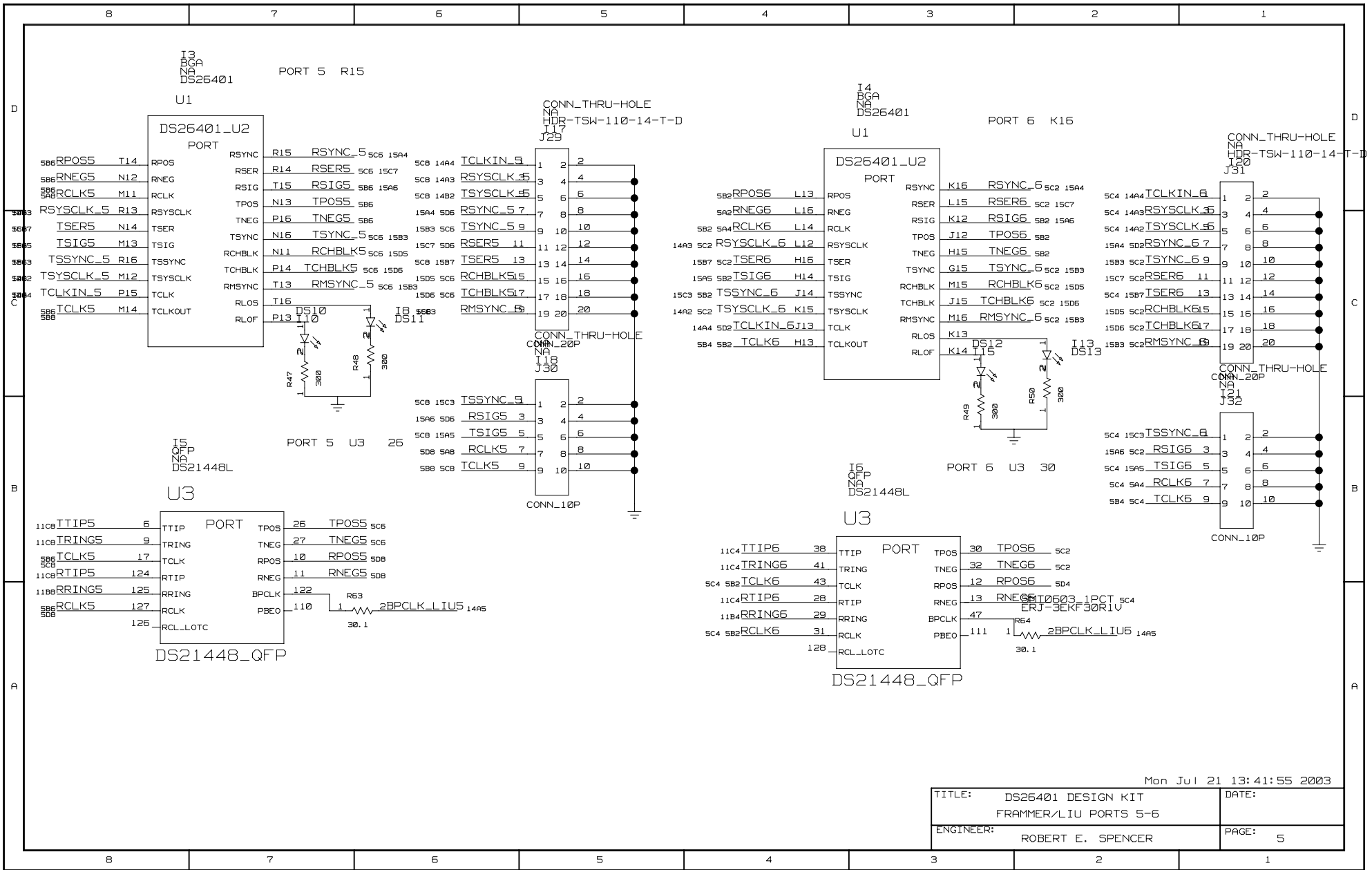
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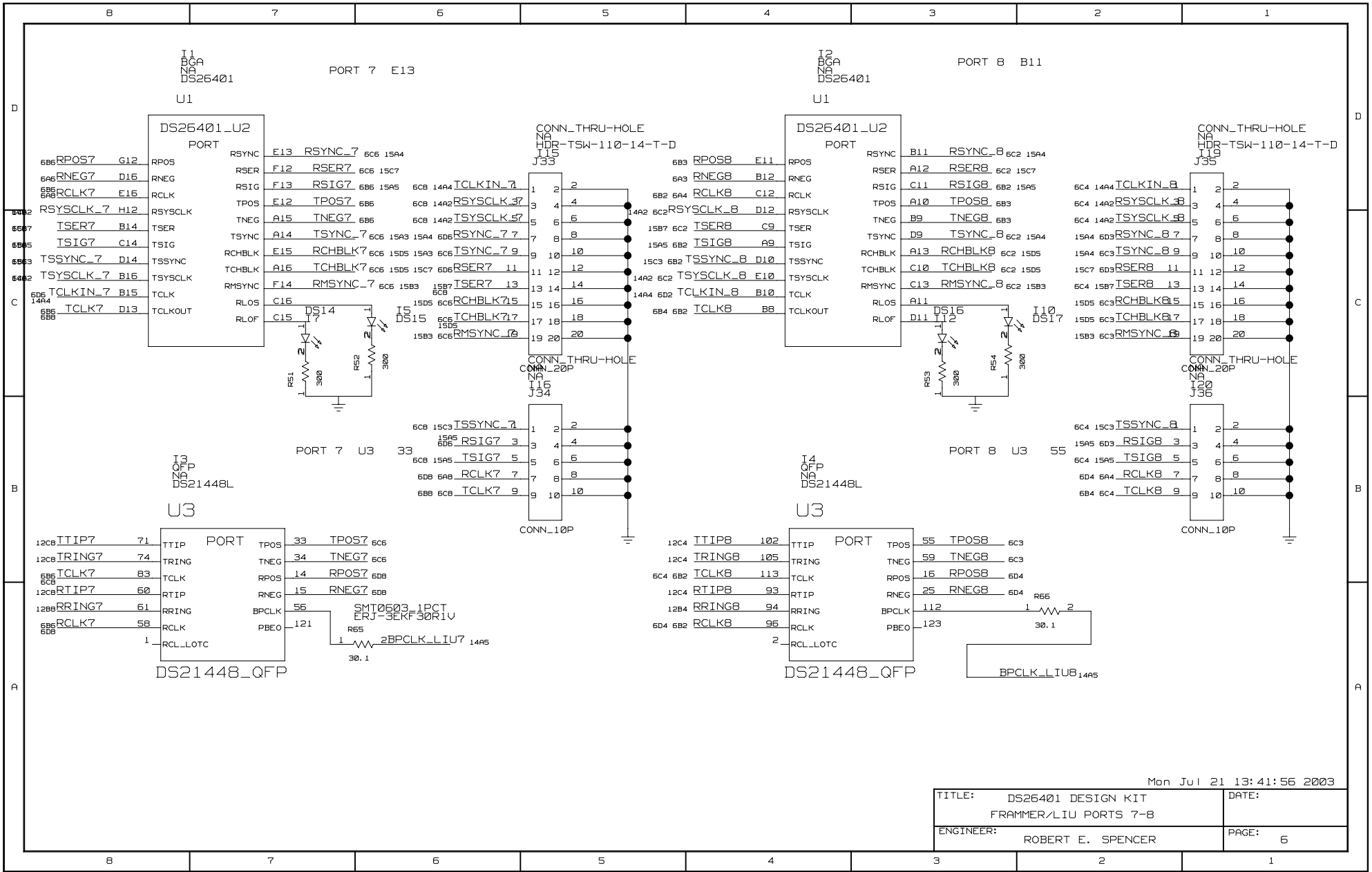
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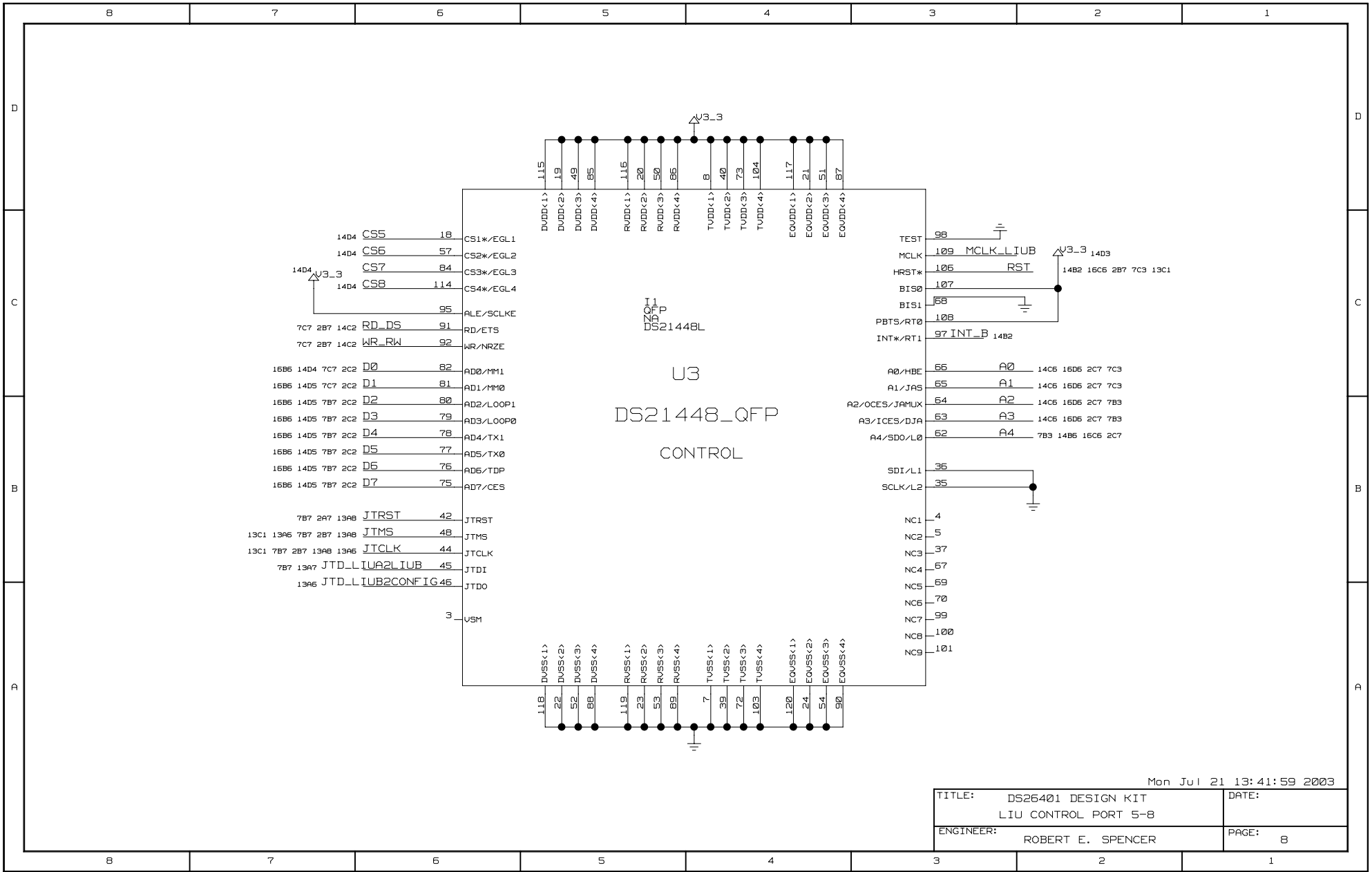
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ENGINEER: ROBERT E. SPENCER	PAGE: 5



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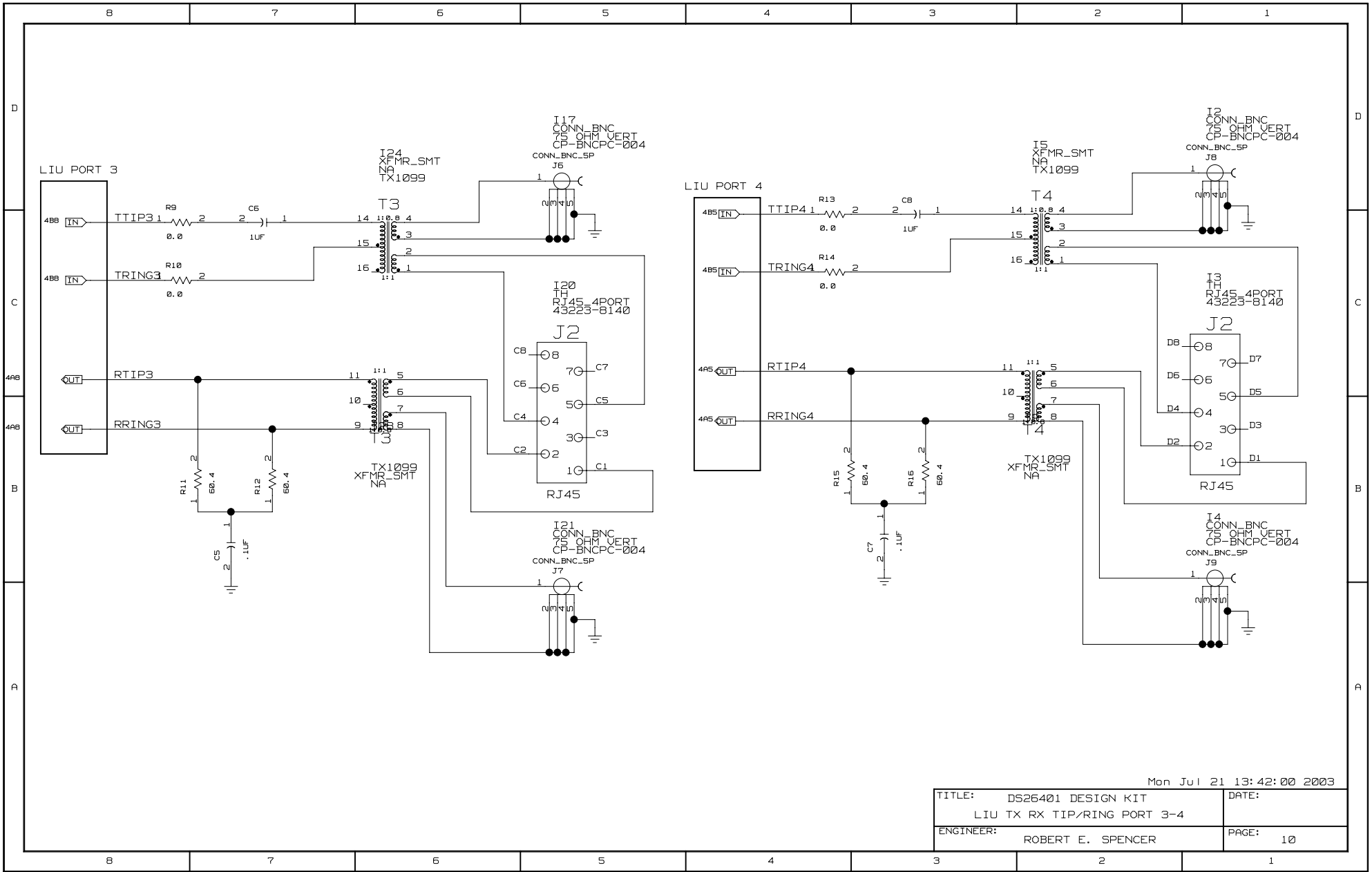




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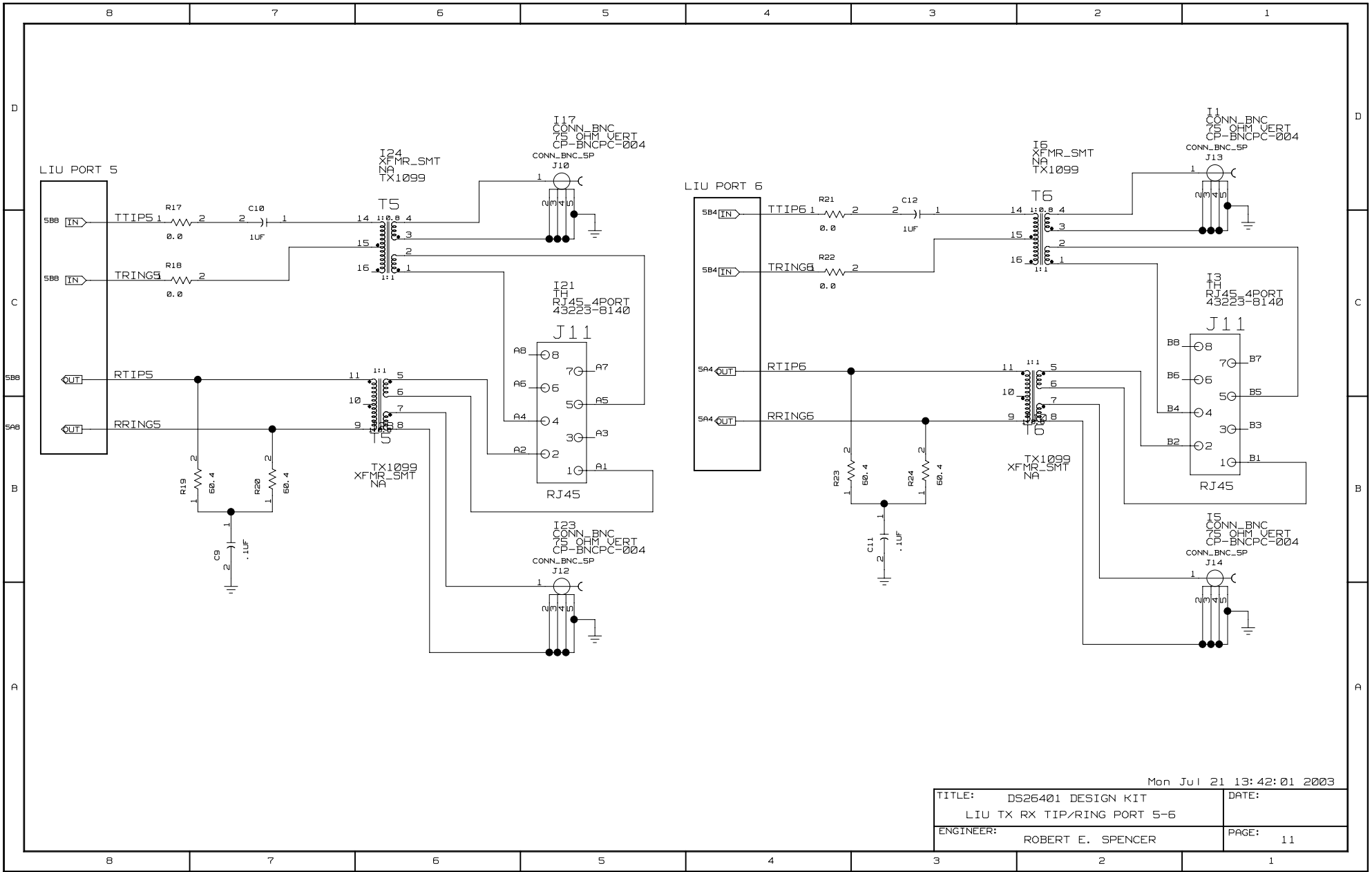
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ENGINEER: ROBERT E. SPENCER	PAGE: 8





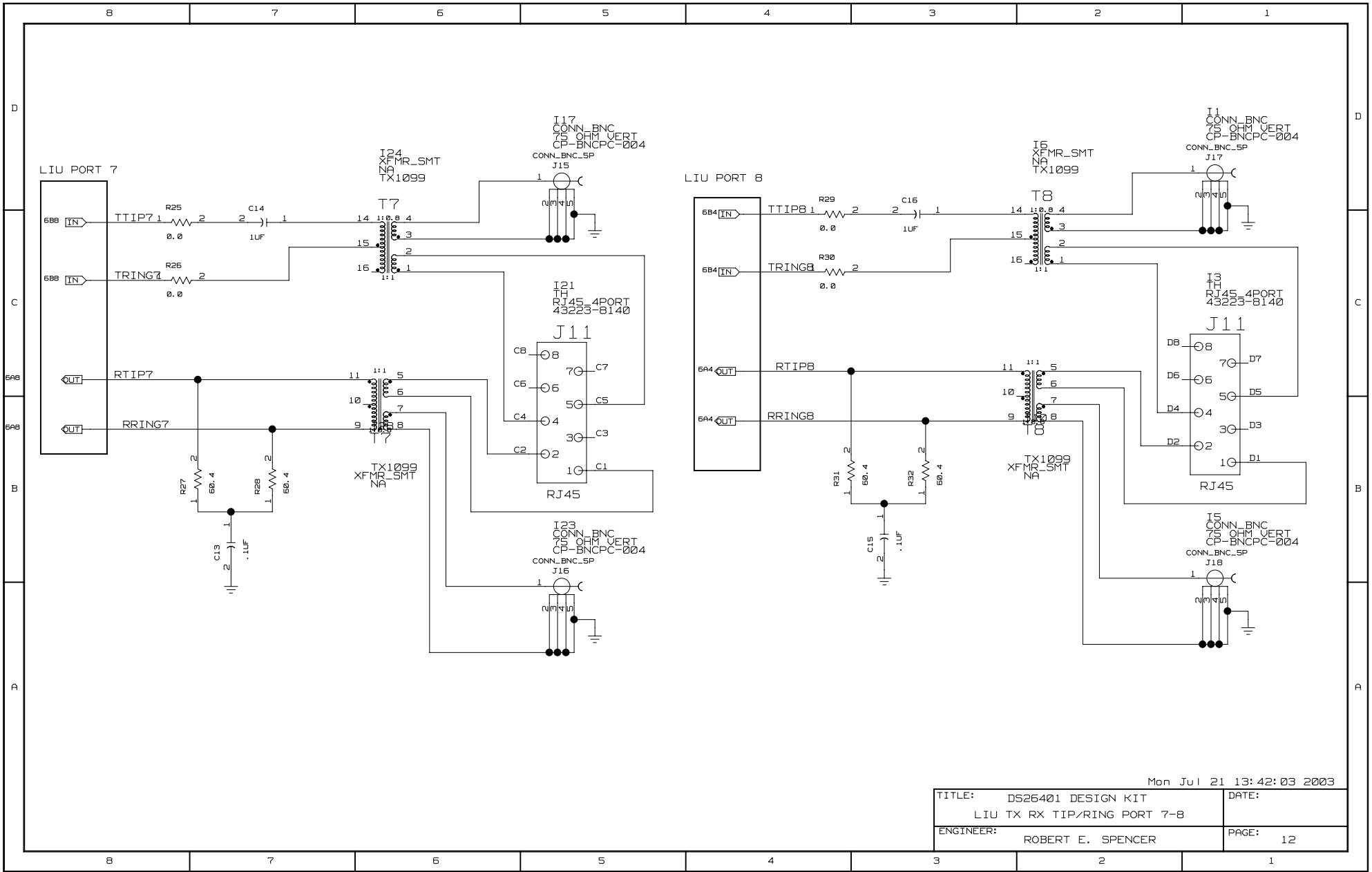
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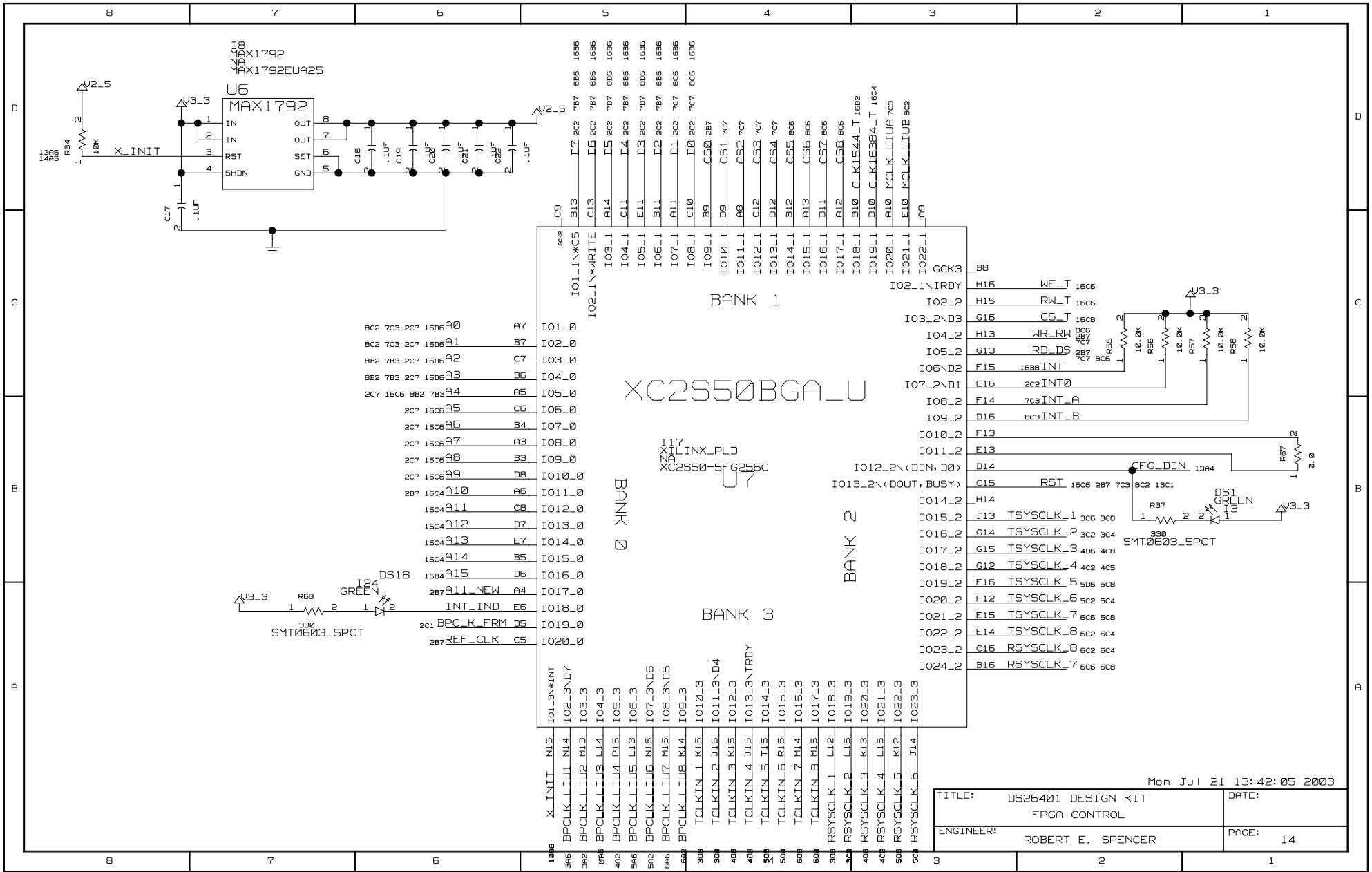
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ENGINEER: ROBERT E. SPENCER	PAGE: 11



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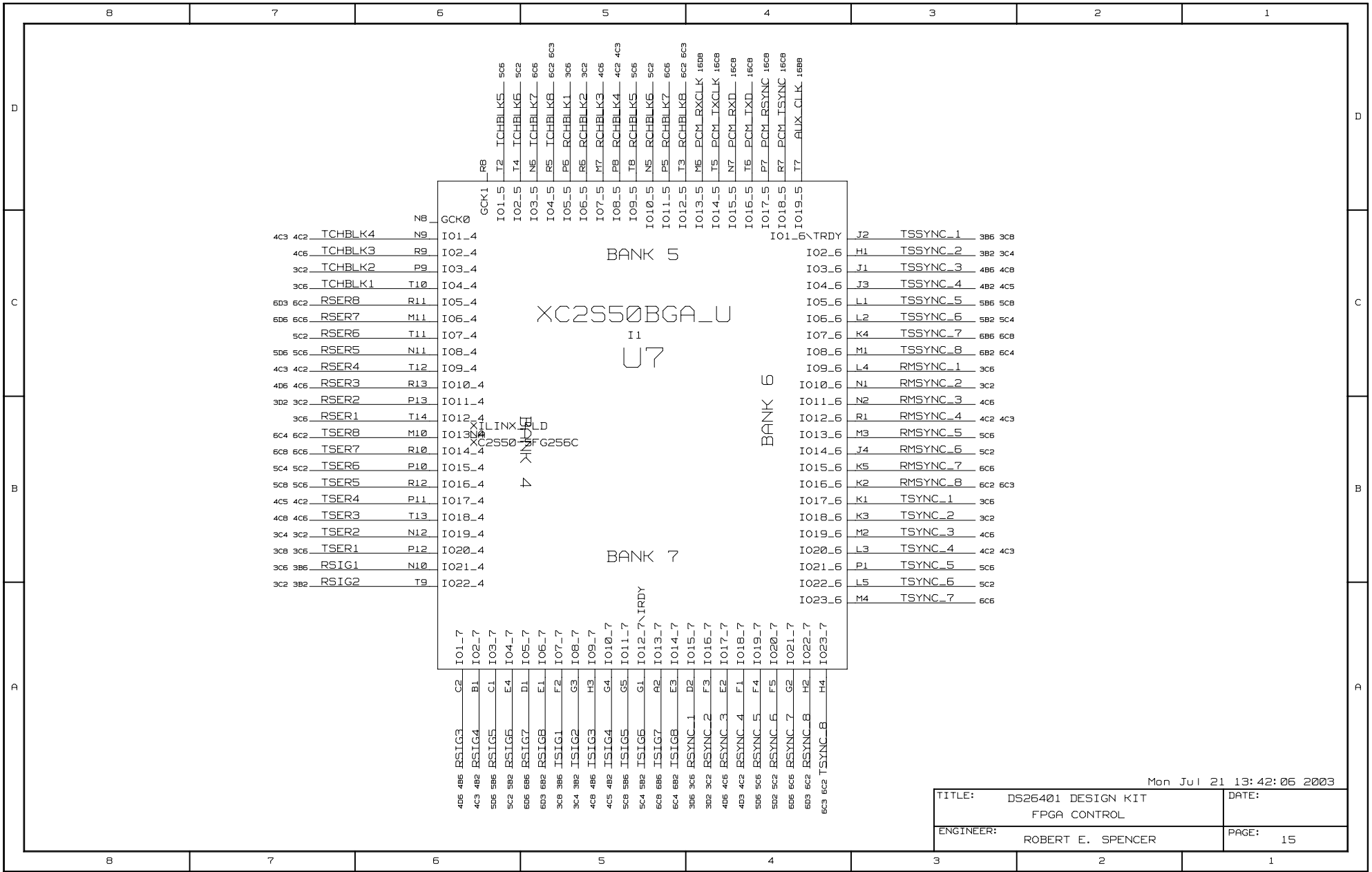
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ENGINEER:	ROBERT E. SPENCER	PAGE: 12

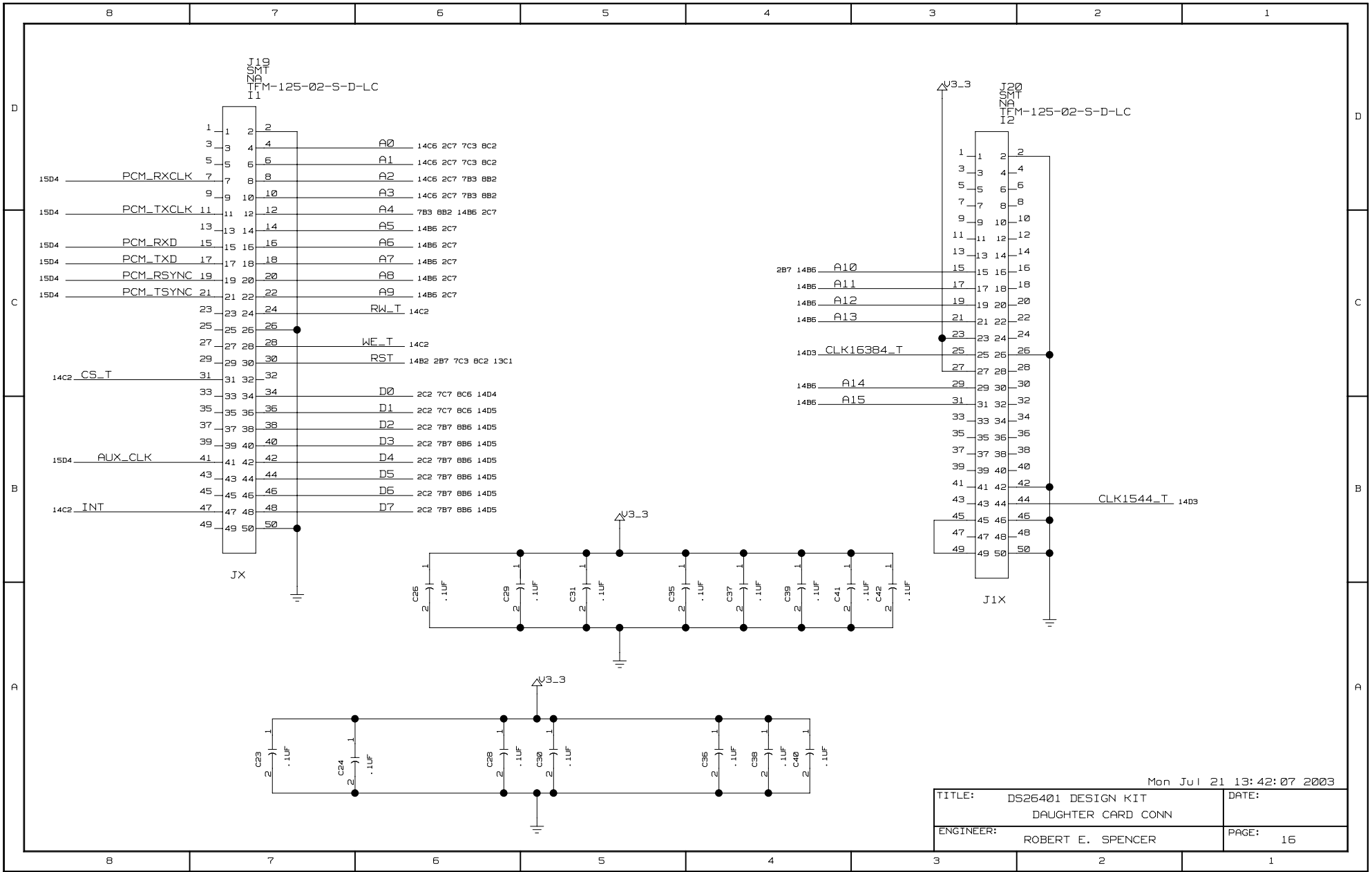


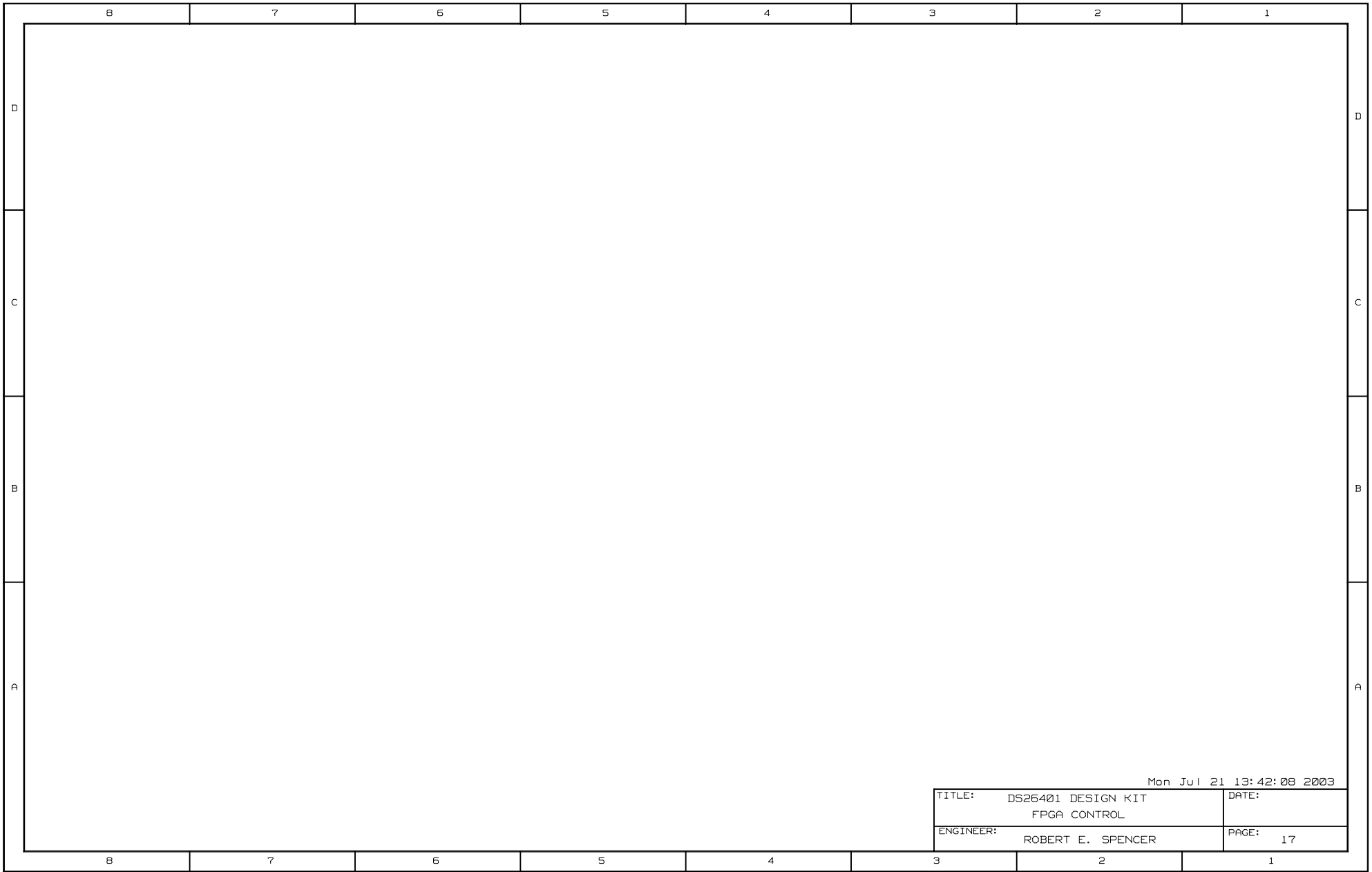


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ENGINEER: ROBERT E. SPENCER		PAGE: 14







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ENGINEER:	ROBERT E. SPENCER	PAGE:	17



	8	7	6	5	4	3	2	1
D	*** Signal Cross-Reference for the entire design ***		RCHBLK2	3C2< 3C2< 15D5<	RSYSCLK_3	4D6< 14A3< 4C9<	TSIG7	6B6< 15A5< 6C8<
	A0	14C6< 16D6< 2C7< 7C3< 8C2<	RCHBLK3	4C6< 4C6< 15D5<	RSYSCLK_4	4C2< 14A3< 4C5<	TSIG8	6B2< 15A5< 6C4<
	A1	14C6< 16D6< 2C7< 7C3< 8C2<	RCHBLK4	4C2< 4C3< 15D5<	RSYSCLK_5	5D6< 14A3< 5C8<	TSSYNC_1	3B6< 15C3< 3C8<
	A2	14C6< 16D6< 2C7< 7B3< 8B2<	RCHBLK5	5C6< 5C6< 15D5<	RSYSCLK_6	5C2< 14A3< 5C4<	TSSYNC_2	3B2< 15C3< 3C4<
	A3	14C6< 16D6< 2C7< 7B3< 8B2<	RCHBLK6	5C2< 5C2< 15D5<	RSYSCLK_7	6C6< 14A2< 6C8<	TSSYNC_3	4B6< 15C3< 4C8<
	A4	14C6< 16D6< 2C7< 7B3< 8B2<	RCHBLK7	6C6< 6C6< 15D5<	RSYSCLK_8	6C2< 14A2< 6C4<	TSSYNC_4	4B2< 15C3< 4C5<
	A5	7B3< 8B2< 14B6< 16C6< 2C7<	RCHBLK8	6C2< 6C3< 15D5<	RTIP1	9C8< 9A8<	TSSYNC_5	5B6< 15C3< 5C8<
	A6	14B6< 16C6< 2C7<	RCLK1	3A8< 3B6< 3C8<	RTIP2	9C4< 9A4<	TSSYNC_6	5B2< 15C3< 5C4<
	A7	14B6< 16C6< 2C7<	RCLK2	3A4< 3B2< 3C4<	RTIP3	10C8< 4B8<	TSSYNC_7	6B6< 15C3< 6C8<
	A8	14B6< 16C6< 2C7<	RCLK3	4A8< 4B6< 4C8<	RTIP4	10C4< 4B6<	TSSYNC_8	6B2< 15C3< 6C4<
C	A9	14B6< 16C6< 2C7<	RCLK4	4A6< 4B2< 4C5<	RTIP5	11C8< 5B8<	TSYNC_1	3C5< 3C5< 15B3<
	A10	14B6< 16C4< 2B7<	RCLK5	5A8< 5B6< 5D8<	RTIP6	11C4< 5A4<	TSYNC_2	3C2< 3C2< 15B3<
	A11	14B6< 16C4<	RCLK6	5A4< 5B2< 5C4<	RTIP7	12C8< 6A8<	TSYNC_3	4C6< 4C6< 15B3<
	A11_NEW	14A6< 2B7<	RCLK7	6A8< 6B6< 6D8<	RTIP8	12C4< 6A4<	TSYNC_4	4C2< 4C3< 15B3<
	A12	14B6< 16C4<	RCLK8	6A4< 6B2< 6D4<	RM_T	14C2< 16C6<	TSYNC_5	5C6< 5C6< 15B3<
	A13	14B6< 16C4<	RD_DS	14C2< 2B7< 7C7< 8C6<	TCHBLK1	3C6< 3C6< 15C7<	TSYNC_6	5C2< 5C2< 15B3<
	A14	14B6< 16C4<	REF_CLK	14A6< 2B7<	TCHBLK2	3C2< 3C2< 15C7<	TSYNC_7	6C6< 6C6< 15A3<
	A15	14B6< 16B4<	RMSYNC_1	3C6< 3C6< 15C3<	TCHBLK3	4C6< 4C6< 15C7<	TSYNC_8	6C2< 6C3< 15A4<
	AUX_CLK	15D4< 16B8<	RMSYNC_2	3C2< 3C2< 15C3<	TCHBLK4	4C2< 4C3< 15C7<	TSYSCLK_1	3C6< 14B2< 3C8<
	BPCLK_FRM	14A5< 2C1<	RMSYNC_3	4C6< 4C6< 15B3<	TCHBLK5	5C6< 5C6< 15D6<	TSYSCLK_2	3C2< 14B2< 3C4<
BPCLK_LIU1	14A5< 3A6<	RMSYNC_4	4C2< 4C3< 15B3<	TCHBLK6	5C2< 5C2< 15D6<	TSYSCLK_3	4D6< 14B2< 4C8<	
BPCLK_LIU2	14A5< 3A2<	RMSYNC_5	5C6< 5C6< 15B3<	TCHBLK7	6C6< 6C6< 15D5<	TSYSCLK_4	4C2< 14B2< 4C5<	
BPCLK_LIU3	14A5< 4A6<	RMSYNC_6	5C2< 5C2< 15B3<	TCHBLK8	6C2< 6C3< 15D5<	TSYSCLK_5	5D6< 14B2< 5C8<	
BPCLK_LIU4	14A5< 4A2<	RMSYNC_7	6C6< 6C6< 15B3<	TCLK1	3B6< 3C8< 3B8<	TSYSCLK_6	5C2< 14A2< 5C4<	
BPCLK_LIU5	14A5< 5A6<	RMSYNC_8	6C2< 6C3< 15B3<	TCLK2	3B2< 3C4< 3B4<	TSYSCLK_7	6C6< 14A2< 6C8<	
BPCLK_LIU6	14A5< 5A2<	RNEG1	3A6< 3C8<	TCLK3	4B6< 4C8< 4A8<	TSYSCLK_8	6C2< 14A2< 6C4<	
BPCLK_LIU7	14A5< 6A6<	RNEG2	3A2< 3C4<	TCLK4	4B2< 4C5< 4A5<	TTIP1	3B8< 9C8<	
BPCLK_LIU8	14A5< 6A2<	RNEG3	4A8< 4D8<	TCLK5	5B6< 5C8< 5B8<	TTIP2	3B4< 9C4<	
CCLK	13A6< 13C1<	RNEG4	4A8< 4C5<	TCLK6	5B2< 5C4< 5B4<	TTIP3	4B6< 10C8<	
CFG_DIN	13A4< 14B1<	RNEG5	5B6< 5D8<	TCLK7	6B6< 6C8< 6B8<	TTIP4	4B6< 10C4<	
CLKI544_T	14D3< 16B2<	RNEG6	5A2< 5C4<	TCLK8	6B2< 6C4< 6B4<	TTIP5	5B8< 11C8<	
CLKI63B4_T	14D3< 16C4<	RNEG7	6A6< 6D8<	TCLKIN_1	3D6< 14A4< 3C8<	TTIP6	5B4< 11C4<	
CS0	14D4< 2B7<	RNEG8	6A8< 6D4<	TCLKIN_2	3D2< 14A4< 3C4<	TTIP7	6B8< 12C8<	
CS1	14D4< 7C7<	RPOS1	3B6< 3D8<	TCLKIN_3	4D6< 14A4< 4C8<	TTIP8	6B4< 12C4<	
CS2	14D4< 7C7<	RPOS2	3B2< 3D4<	TCLKIN_4	4D2< 14A4< 4C5<	WE_T	14C2< 16C6<	
CS3	14D4< 7C7<	RPOS3	4A6< 4D8<	TCLKIN_5	5D6< 14A4< 5C8<	WR_RW	14C2< 2B7< 7C7< 8C6<	
CS4	14D4< 7C7<	RPOS4	4A3< 4D5<	TCLKIN_6	5D2< 14A4< 5C4<	XRST	13A6< 13C2<	
CS5	14D4< 8C6<	RPOS5	5B6< 5D8<	TCLKIN_7	6D6< 14A4< 6C8<	X_INIT	13A6< 14A5< 14D8<	
CS6	14D4< 8C6<	RPOS6	5B2< 5D4<	TCLKIN_8	6D2< 14A4< 6C4<			
CS7	14D4< 8C6<	RPOS7	6B6< 6D8<	TNEG1	3C6< 3B6<			
CS8	14D4< 8C6<	RPOS8	6B3< 6D4<	TNEG2	3C2< 3B2<			
CS_T	14C2< 16C8<	RRING1	9B8< 9A8<	TNEG3	4C6< 4B6<			
D0	2C2< 7C7< 8C5< 14D4< 16B6<	RRING2	9B4< 9A4<	TNEG4	4C3< 4B3<			
D1	2C2< 7C7< 8C5< 14D5< 16B6<	RRING3	10B8< 4A8<	TNEG5	5C6< 5B6<			
D2	2C2< 7B7< 8B6< 14D5< 16B6<	RRING4	10B4< 4A5<	TNEG6	5C2< 5B2<			
D3	2C2< 7B7< 8B6< 14D5< 16B6<	RRING5	11B8< 5A8<	TNEG7	6C6< 6B6<			
D4	2C2< 7B7< 8B6< 14D5< 16B6<	RRING6	11B4< 5A4<	TNEG8	6C3< 6B3<			
D5	2C2< 7B7< 8B6< 14D5< 16B6<	RRING7	12B8< 6A8<	TPOS1	3C6< 3B6<			
D6	2C2< 7B7< 8B6< 14D5< 16B6<	RRING8	12B4< 6A4<	TPOS2	3C2< 3B2<			
D7	2C2< 7B7< 8B6< 14D5< 16B6<	RSER1	3C6< 3C6< 15B7<	TPOS3	4C6< 4B6<			
DONE	13A6< 13C1<	RSER2	3C2< 3D2< 15B7<	TPOS4	4C3< 4B3<			
GCLK	2C2< 2B7<	RSER3	4C6< 4D6< 15C7<	TPOS5	5C6< 5B6<			
INT	14C2< 16B8<	RSER4	4C2< 4C3< 15C7<	TPOS6	5C2< 5B2<			
INT0	2C2< 14C2<	RSER5	5C6< 5D6< 15C7<	TPOS7	6C6< 6B6<			
INT_A	7C3< 14B2<	RSER6	5C2< 5C2< 15C7<	TPOS8	6C3< 6B3<			
INT_B	8C3< 14B2<	RSER7	6C6< 6D6< 15C7<	TRING1	3B8< 9C8<			
INT_IND	14A6<	RSER8	6C2< 6D3< 15C7<	TRING2	3B4< 9C4<			
JTCLK	13A6< 13A8< 2B7< 7B7< 8B6< 13C1<	RSIG1	3B6< 3C6< 15B7<	TRING3	4B8< 10C8<			
JTD1_CON2FRM	13A8< 2B7<	RSIG2	3B2< 3C2< 15B7<	TRING4	4B6< 10C4<			
JTD_CONF1G2FPGA	13A6< 13C1<	RSIG3	4B6< 4D6< 15A6<	TRING5	5B8< 11C8<			
JTD_FPGA2CON	13A8< 13C1<	RSIG4	4B2< 4C3< 15A6<	TRING6	5B4< 11C4<			
JTD_FRM2LIUA	2B3< 13A7< 7B7<	RSIG5	5B6< 5D6< 15A6<	TRING7	6B8< 12C8<			
JTD_LIU2LIUB	13A7< 7B7< 8B6<	RSIG6	5B2< 5C2< 15A6<	TRING8	6B4< 12C4<			
JTD_LIU2CONF1G	13A6< 8B6<	RSIG7	6B6< 6D6< 15A5<	TSER1	3C6< 15B7< 3C8<			
JTMS	13A8< 2B7< 7B7< 8B6< 13A6< 13C1<	RSIG8	6B2< 6D3< 15A5<	TSER2	3C2< 15B7< 3C4<			
JTRST	13A8< 2B7< 7B7< 8B6<	RST	14B2< 16C6< 2B7< 7C3< 8C2< 13C1<	TSER3	4C6< 15B7< 4C8<			
MCLK_LLIUA	14D3< 7C3<	RSYNC_1	3C6< 3D6< 15A4<	TSER4	4C2< 15B7< 4C5<			
MCLK_LLIUB	14D3< 8C2<	RSYNC_2	3C2< 3D2< 15A4<	TSER5	5C6< 15B7< 5C8<			
PCM_RSYNC	15D4< 16C8<	RSYNC_3	4C6< 4D6< 15A4<	TSER6	5C2< 15B7< 5C4<			
PCM_RXCLK	15D4< 16D8<	RSYNC_4	4C2< 4D3< 15A4<	TSER7	6C6< 15B7< 6C8<			
PCM_RXD	15D4< 16C8<	RSYNC_5	4C6< 5D6< 15A4<	TSER8	6C2< 15B7< 6C4<			
PCM_TSYNC	15D4< 16C8<	RSYNC_6	5C2< 5D2< 15A4<	TSIG1	3B6< 15A5< 3C8<			
PCM_TXCLK	15D4< 16C8<	RSYNC_7	6C6< 6D6< 15A4<	TSIG2	3B2< 15A5< 3C4<			
PCM_TXD	15D4< 16C8<	RSYNC_8	6C2< 6D3< 15A4<	TSIG3	4B6< 15A5< 4C8<			
RCHBLK1	3C6< 3C6< 15D5<	RSYSCLK_1	3D6< 14A4< 3C8<	TSIG4	4B2< 15A5< 4C5<			
		RSYSCLK_2	3C2< 14A4< 3C4<	TSIG5	5B6< 15A5< 5C8<			
				TSIG6	5B2< 15A5< 5C4<			
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