



**THE DATASHEET OF  
CYK001M16SCAU-70BAXI**





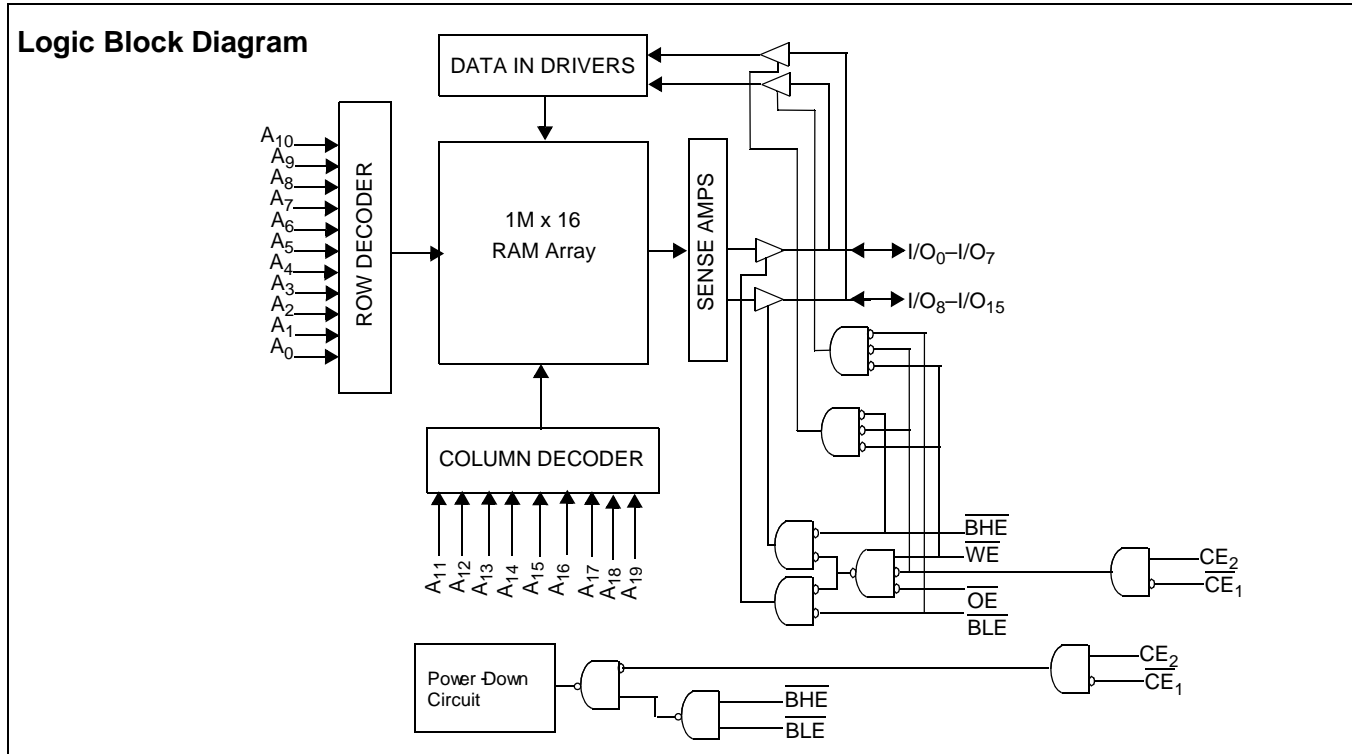
# 16-Mbit (1M x 16) Pseudo Static RAM

## Features

- Advanced low-power MoBL® architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.3V
- Typical active current: 3 mA @ f = 1 MHz
- Typical active current: 13 mA @ f = f<sub>MAX</sub>
- Low standby power
- Automatic power-down when deselected

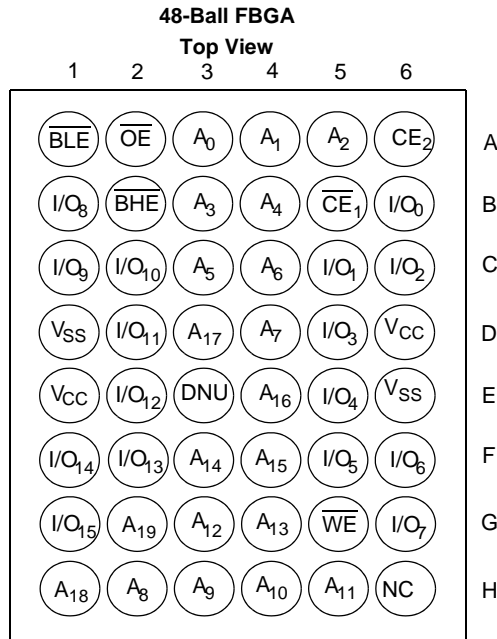
## Functional Description<sup>[1]</sup>

The CYK001M16SCCA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL) in portable applications such as cellular telephones. The device can be put into standby mode, reducing power consumption dramatically when deselected ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the chip is deselected ( $\overline{CE}_1$  HIGH,  $CE_2$  LOW) or  $\overline{OE}$  is deasserted HIGH, or during a write operation (Chip Enabled and Write Enable  $\overline{WE}$  LOW). Reading from the device is accomplished by asserting the Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table for a complete description of read and write modes.



**Note:**

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2, 3, 4]</sup>**

**Product Portfolio<sup>[5]</sup>**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating, I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
	Min.	Typ.	Max.		f = 1 MHz		f = f <sub>MAX</sub>			
					Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.		
CYK001M16SCCA	2.7	3.0	3.3	55	3	5	13	22	80	150
				70				17		

**Notes:**

2. DNU pins are to be left floating or tied to V<sub>SS</sub>.
3. Ball H6 is the address expansion pins for the 32-Mb density.
4. NC "no connect"—not connected internally to the die.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> (typ) and T<sub>A</sub> = 25°C.



**Maximum Ratings**<sup>[6, 7, 8]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -40°C to +85°C  
 Supply Voltage to Ground Potential ..... -0.4V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[6, 7, 8]</sup> ..... -0.4V to 3.3V

DC Input Voltage<sup>[6, 7, 8]</sup> ..... -0.4V to 3.3V  
 Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current ..... > 200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Industrial	-25°C to +85°C	2.7V to 3.3V

**DC Electrical Characteristics** (Over the Operating Range)

Parameter	Description	Test Conditions	CYK001M16SCCA-55			CYK001M16SCCA-70			Unit
			Min.	Typ. <sup>[5]</sup>	Max.	Min.	Typ. <sup>[5]</sup>	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.3	2.7		3.3	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.4			V <sub>CC</sub> - 0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		0.8 * V <sub>CC</sub>		V <sub>CC</sub> + 0.4	0.8 * V <sub>CC</sub>		V <sub>CC</sub> + 0.4	V
V <sub>IL</sub>	Input LOW Voltage	f = 0	-0.4		0.4	-0.4		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		13	22		13	17	mA
		f = 1 MHz		3	5		3	5	
I <sub>SB1</sub>	Automatic CE Power-down Current —CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V <sub>CC</sub> = 3.3V		100	525		100	525	μA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.3V		80	150		80	150	μA

**Capacitance**<sup>[9]</sup>

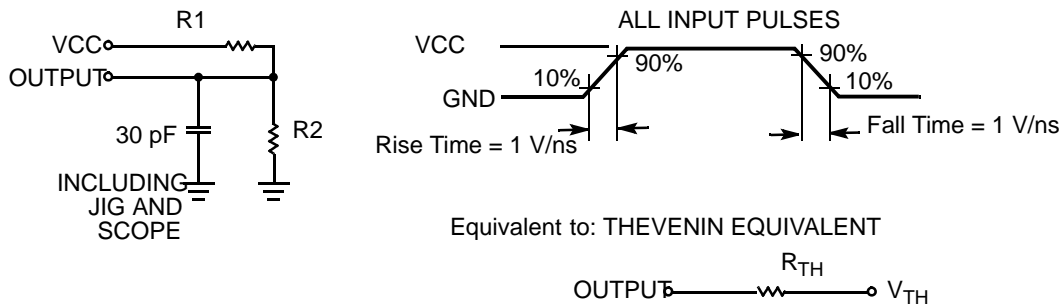
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

**Notes:**

6. V<sub>IH(MAX)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.
7. V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.
8. Overshoot and undershoot specifications are characterized and are not 100% tested.
9. Tested initially and after design or process changes that may affect these parameters.

**Thermal Resistance<sup>[9]</sup>**

Parameter	Description	Test Conditions	FBGA	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55	$^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction to Case)		17	$^{\circ}\text{C}/\text{W}$

**AC Test Loads and Waveforms**


Parameters	3.0V V <sub>CC</sub>	Unit
R1	22000	$\Omega$
R2	22000	$\Omega$
R <sub>TH</sub>	11000	$\Omega$
V <sub>TH</sub>	1.50	V

**Switching Characteristics (Over the Operating Range)<sup>[10, 11, 12, 13]</sup>**

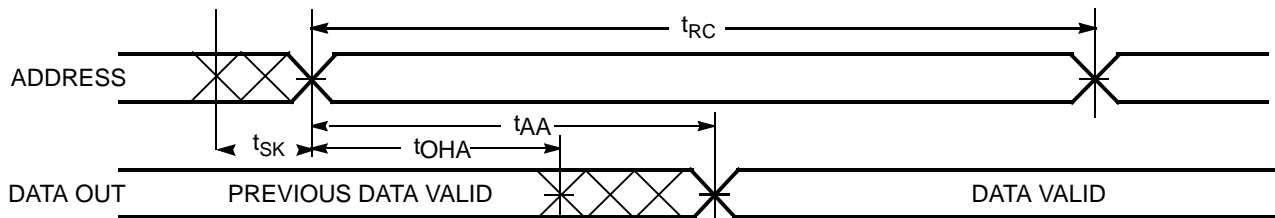
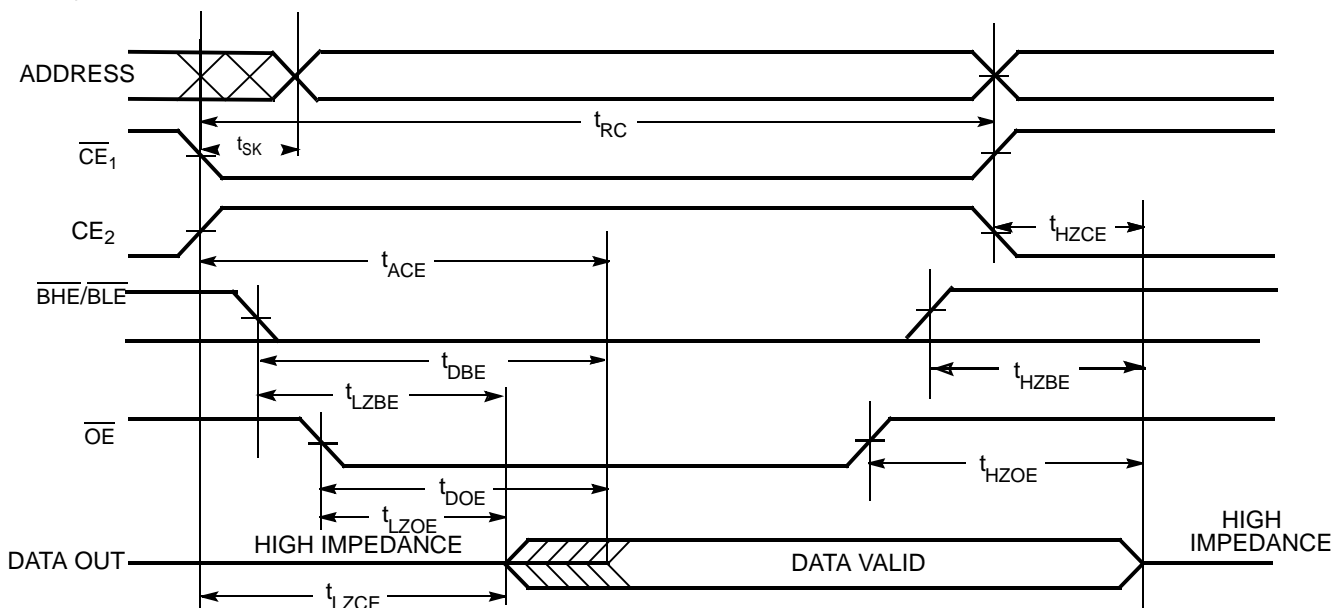
Parameter	Description	CYK001M16SCCA-55		CYK001M16SCCA-70		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55 <sup>[14]</sup>		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		5		ns
t <sub>ACE</sub>	$\overline{\text{CE}}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z <sup>[11, 12]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[11, 12]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[11, 12]</sup>	5		5		ns
t <sub>HZCE</sub>	$\overline{\text{CE}}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[11, 12]</sup>		25		25	ns
t <sub>DBE</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Low Z <sup>[11, 12]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{\text{BLE}}/\overline{\text{BHE}}$ HIGH to High-Z <sup>[11, 12]</sup>		10		25	ns
t <sub>SK</sub> <sup>[14]</sup>	Address Skew		0		10	ns

**Notes:**

- Test conditions assume signal transition time of 1 V/ns or higher, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0V to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ , CE<sub>1</sub> = V<sub>IL</sub>, CE<sub>2</sub> = V<sub>IH</sub>,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = \text{V}_{\text{IL}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be  $\overline{\text{CE}}$  controlled. In this case t<sub>ACE</sub> is the critical parameter and t<sub>SK</sub> is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

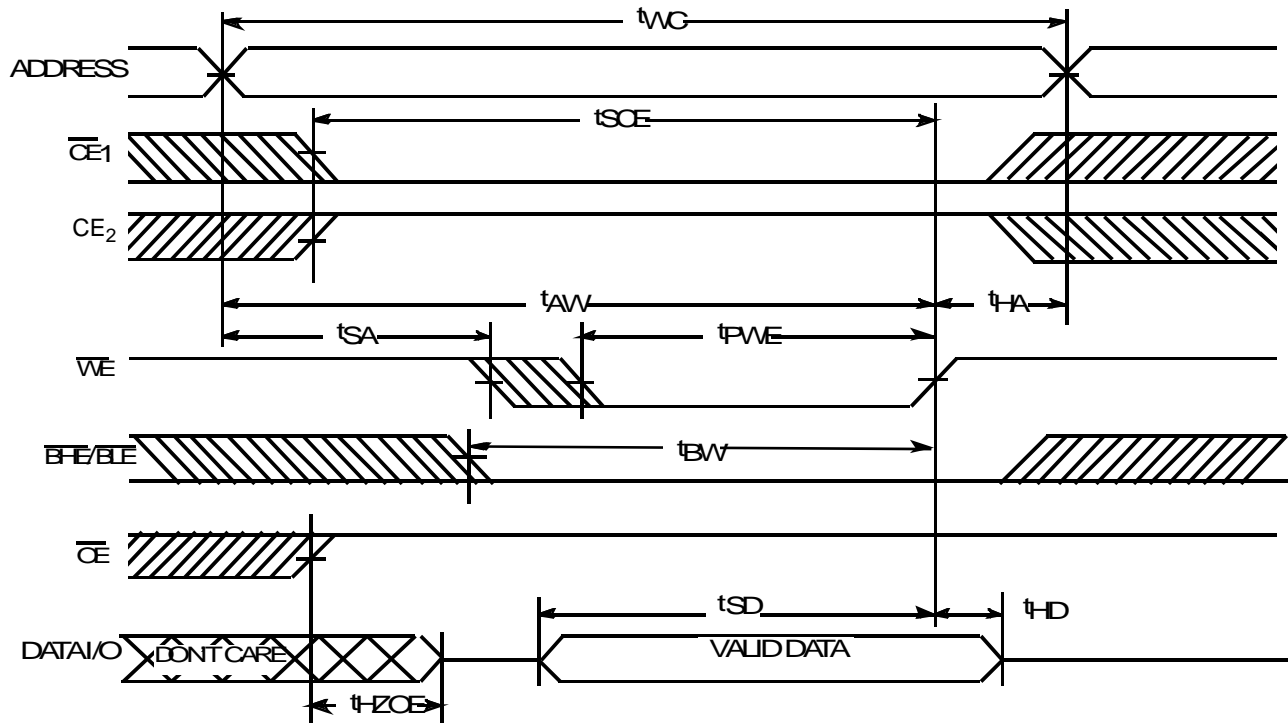
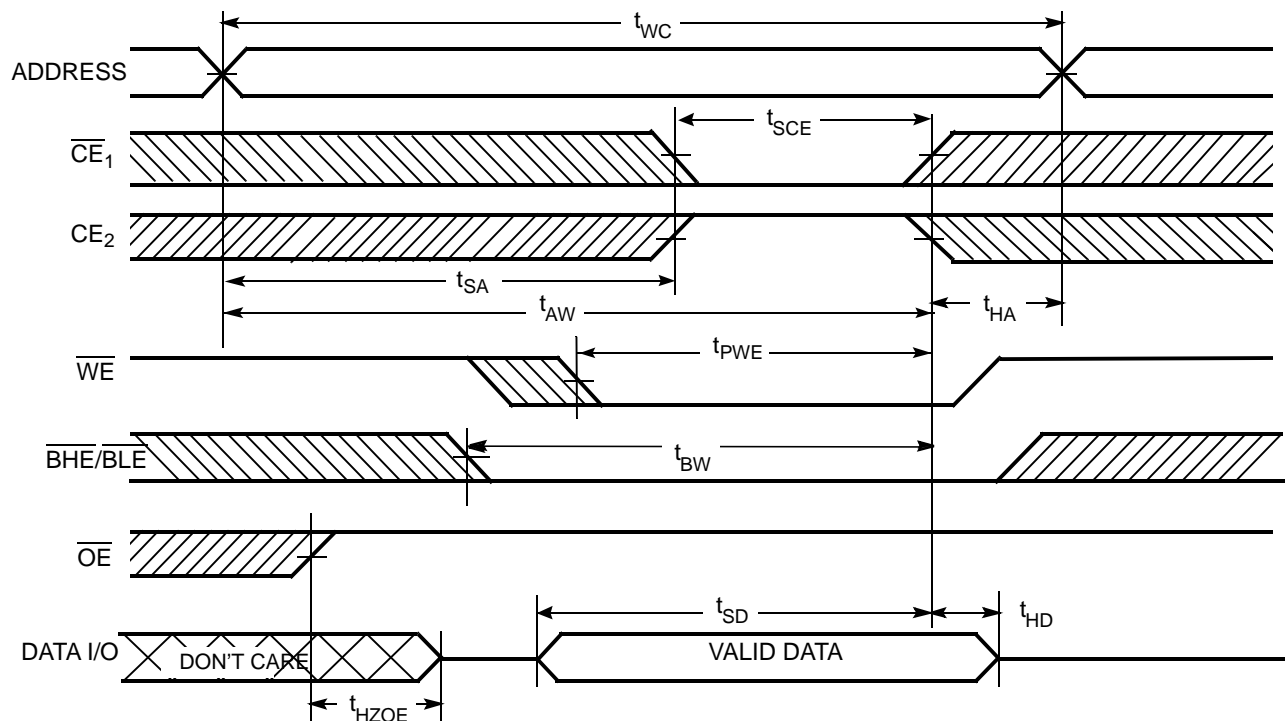
**Switching Characteristics** (Over the Operating Range)<sup>[10, 11, 12, 13]</sup> (continued)

Parameter	Description	CYK001M16SCCA-55		CYK001M16SCCA-70		Unit
		Min.	Max.	Min.	Max.	
<b>Write Cycle<sup>[13]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	45		55		ns
$t_{AW}$	Address Set-up to Write End	45		55		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		55		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		55		ns
$t_{SD}$	Data Set-up to Write End	25		25		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[11, 12]</sup>		25		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[11, 12]</sup>	5		5		ns

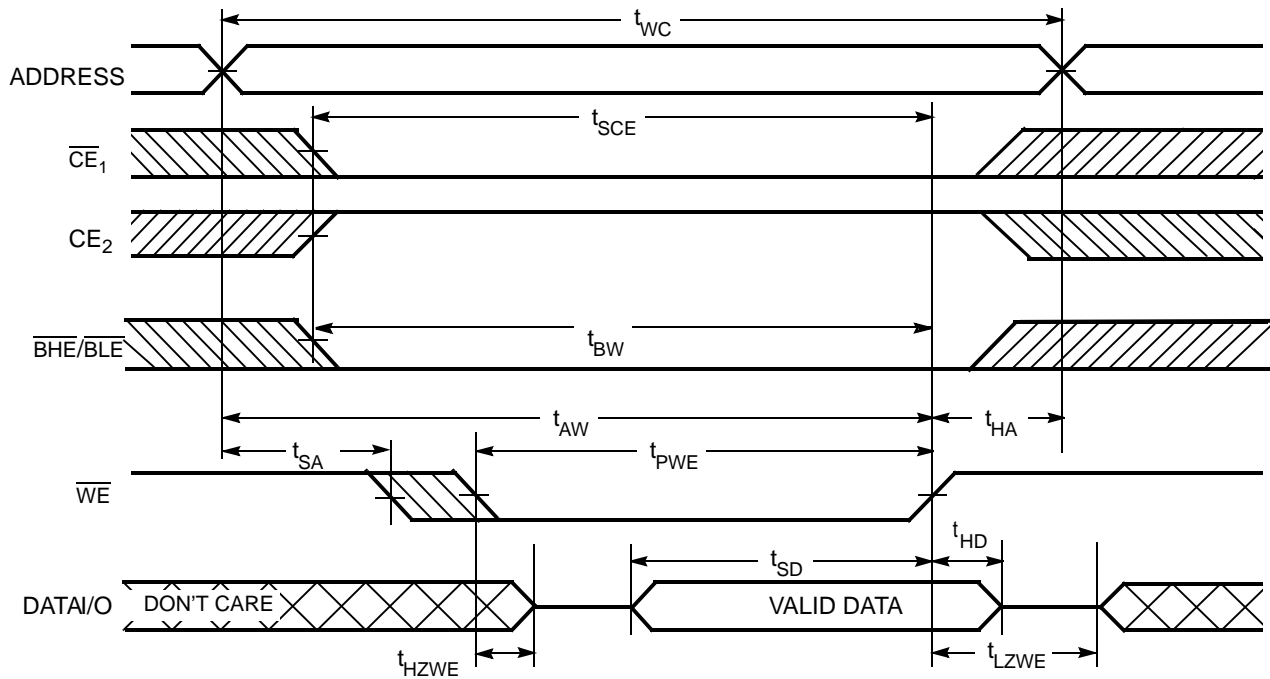
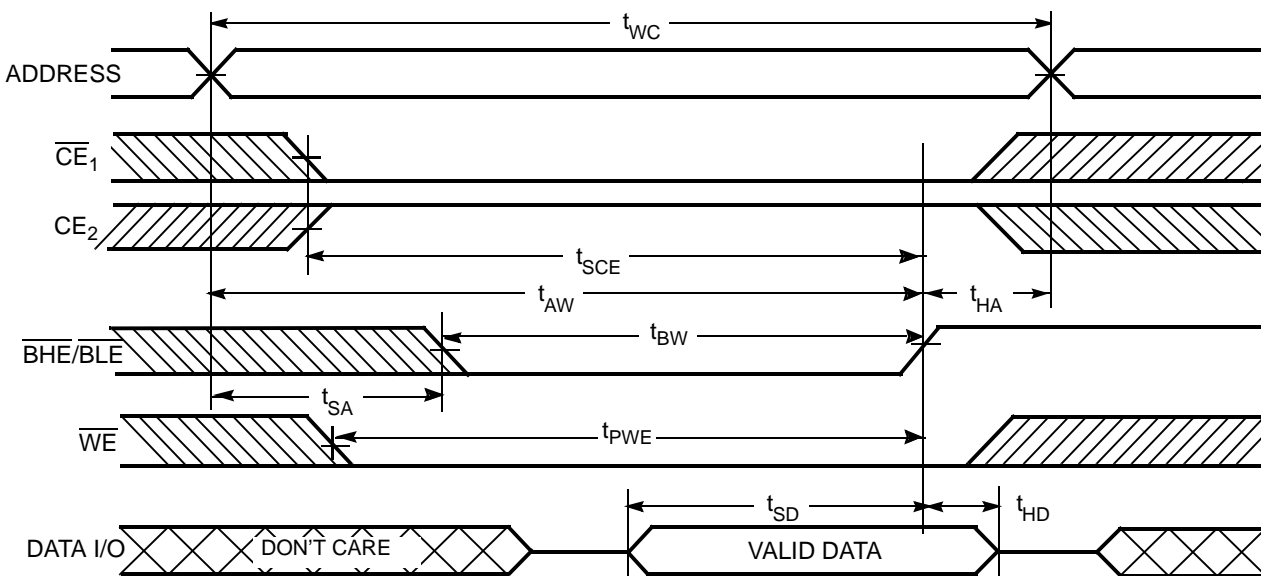
**Switching Waveforms**
**Read Cycle 1 (Address Transition Controlled)<sup>[14, 15, 16]</sup>**

**Read Cycle 2 ( $\overline{OE}$  Controlled)<sup>[14, 16]</sup>**

**Notes:**

15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$  and  $CE_2 = V_{IH}$ .

16.  $\overline{WE}$  is HIGH for Read Cycle.

**Switching Waveforms (continued)**
**Write Cycle No. 1 (WE Controlled)<sup>[12, 13, 17, 18, 19]</sup>**

**Write Cycle 2 (CE<sub>1</sub> or CE<sub>2</sub> Controlled)<sup>[12, 13, 17, 18, 19]</sup>**

**Notes:**

17. Data I/O is high impedance if  $\overline{OE} \geq V_{IH}$ .
18. If Chip Enable goes INACTIVE simultaneously with  $\overline{WE} = \text{HIGH}$ , the output remains in a high-impedance state.
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[18, 19]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[18, 19]</sup>**


**Truth Table<sup>[20]</sup>**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write (Upper Byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write (Lower Byte Only)	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write (Upper Byte Only)	Active ( $I_{CC}$ )

**Ordering Information**

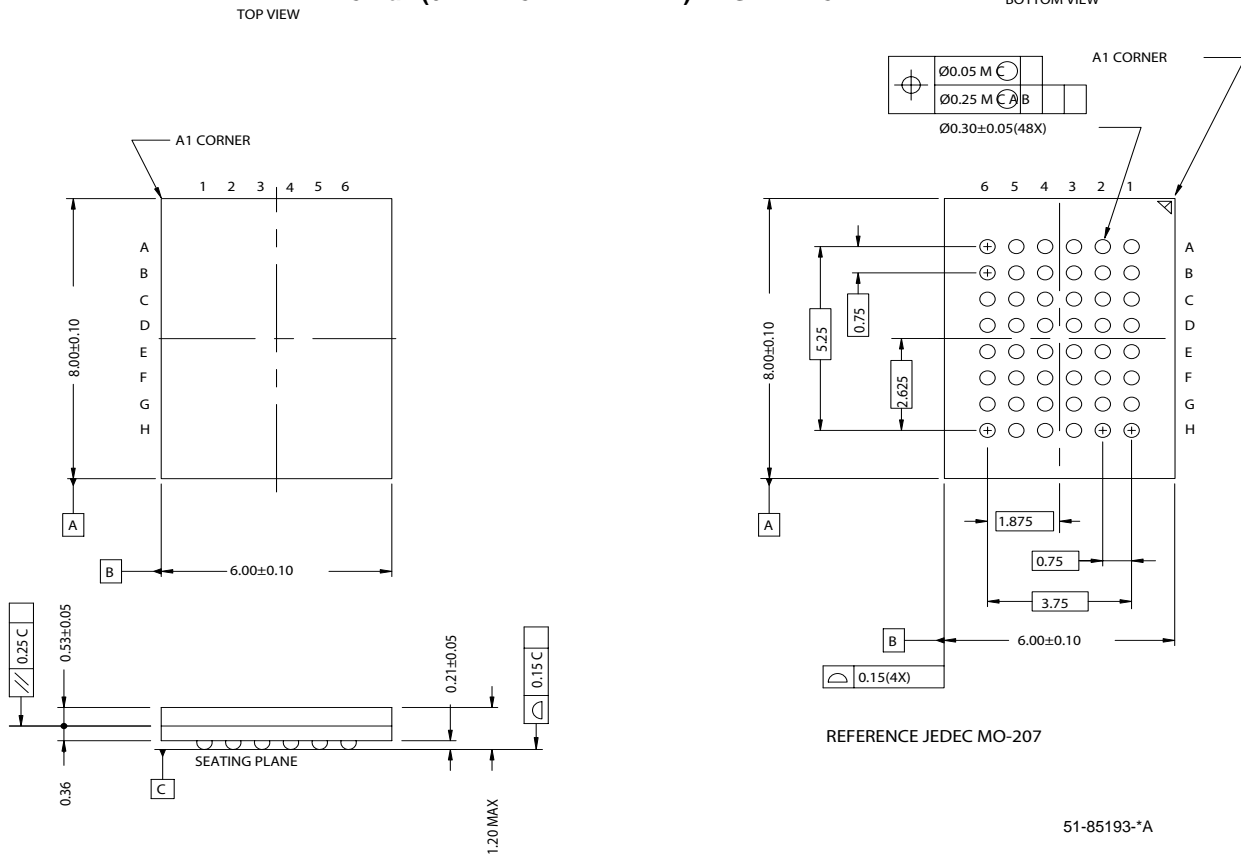
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CYK001M16SCCAU-55BAI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm)	Industrial
70	CYK001M16SCCAU-70BAI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm)	Industrial
55	CYK001M16SCCAU-55BAXI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial
70	CYK001M16SCCAU-70BAXI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial

**Note:**

20. H = Logic HIGH, L = Logic LOW, X = Don't Care

**Package Diagrams**

**48-Ball (6 mm x 8mm x 1.2 mm) FBGA BA48K**



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**Document History Page**

Document Title: CYK001M16SCCA 16-Mbit (1M x 16) Pseudo Static RAM				
Document Number: 38-05426				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	130539	01/27/04	AWK	New Data Sheet
*A	216680	03/26/04	REF	Added 55-ns Speed bin Updated from Advance Information to Final data sheet.
*B	220121	See ECN	REF	Changed the $t_{OHA}$ parameter for 70 ns speed grade from 10 ns to 5 ns
*C	225580	See ECN	AJU	Changed Ordering code from CYK001M16SCCA to CYK001M16SCCAU on page 8
*D	313999	See ECN	RKF	Added Pb-Free parts to the Ordering information

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