



**THE DATASHEET OF
CY8C4247AZA-M485**



Features

32-bit MCU subsystem

- 48 MHz Arm® Cortex®-M0 CPU with single-cycle multiply
- Up to 128 kB of flash with Read Accelerator
- Up to 16 kB of SRAM
- DMA engine

Programmable analog

- Four opamps that operate in Deep Sleep mode at very low current levels
- All opamps have reconfigurable high current pin-drive, high-bandwidth internal drive, ADC input buffering, and Comparator modes with flexible connectivity allowing input connections to any pin
- Four current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep mode
- 12-bit SAR ADC with 1-Msps conversion rate

Programmable digital

- Four programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Cypress-provided peripheral component library, user-defined state machines, and Verilog input

Low-power 1.71 to 5.5 V operation

- 20-nA Stop Mode with GPIO pin wakeup
- Hibernate and Deep Sleep modes allow wakeup-time vs power trade-offs

Capacitive sensing

- Infineon Capacitive Sigma-Delta (CSD) technique provides best-in-class SNR (>5:1) and water tolerance
- Infineon-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense)

Segment LCD drive

- LCD drive supported on all pins (common or segment)
- Operates in Deep Sleep mode with 4 bits per pin memory

Serial communication

- Four independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I2C, SPI, or UART functionality
- Two independent CAN blocks for industrial and automotive networking

Timing and pulse-width modulation

- Eight 16-bit timer/counter pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Package options

- 68-pin QFN, 64-pin TQFP wide and narrow pitch, and 48-pin and 44-pin TQFP packages
- Up to 55 programmable GPIOs
- GPIO pins can be CAPSENSE™, LCD, analog, or digital
- Drive modes, strengths, and slew rates are programmable

Extended industrial temperature operation

- -40°C to +105°C operation

Description

PSoC™ Creator design environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API component) for all fixed-function and programmable peripherals

Industry-standard tool compatibility

- After schematic entry, development can be done with Arm®-based industry-standard development tools

Description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex® -M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. Based on this platform architecture, PSoC™ 4200M is a combination of a microcontroller with digital programmable logic, programmable analog, programmable interconnect, high-performance analog-to-digital conversion, opamps with comparator mode, and standard communication and timing peripherals. The PSoC™ 4200M products will be fully compatible with members of the PSoC™ 4 platform for new applications and design needs. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

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1 Development ecosystem

1.1 PSoC™ 4 resources

Infineon provides a wealth of data at www.infineon.com to help you select the right PSoC™ device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC™ 4 MCU:

- Overview: [PSoC™ portfolio](#).
- Product selector: [PSoC™ 4 MCU](#)
- [Application Notes](#) cover a broad range of topics, from basic to advanced level, and include the following:
 - [AN79953](#): Getting Started with PSoC™ 4
 - [AN88619](#): PSoC™ Hardware Design Considerations.
 - [AN73854](#): PSoC™ - Introduction to Bootloaders
 - [AN89610](#): Arm® Cortex® Code Optimization
 - [AN86233](#): PSoC™ 4 MCU Power Reduction Techniques
 - [AN57821](#): Mixed Signal Circuit Board Layout.
 - [AN85951](#): PSoC™ 4 and PSoC™ 6 MCU CapSense Design Guide.
- [Code Examples](#) demonstrate product features and usage, and are also available on [GitHub repositories](#)
- [Technical reference manuals \(TRM\)](#) provide detailed descriptions of architecture and registers in each device family.
- [PSoC™ 4 MCU Programming Specification](#) provides the information necessary to program PSoC™ 4 MCU non-volatile memory.
- Development Tools
 - [PSoC™ Creator](#) is a free Windows-based IDE. It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, PSoC™ 5LP, and PSoC™ 6 MCU based systems. Applications are created using schematic capture and over 150 preverified, production-ready peripheral Components
 - [CY8CKIT-044](#) is a PSoC™ 4 Pioneer kits that is easy-to-use and an inexpensive development platforms. These include connectors for Arduino-compatible shields and Digilent Pmod daughter cards.
 - [CY8CKIT-043](#) is a very low-cost prototyping platform for sampling PSoC™ 4200M device.
 - [MiniProg4](#) and [MiniProg3](#) all-in-one development programmers and debuggers.
 - [PSoC™ 4 MCU CAD libraries](#) provide footprint and schematic support for common tools. [IBIS models](#) are also available.
- [Training videos](#) are available on a wide range of topics including the [PSoC™ MCUs](#).
- [Infineon Developer Community](#) enables connection with fellow PSoC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated [PSoC™ 4 MCU community](#).

1.2 PSoC™ Creator

[PSoC™ Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on PSoC™ 4 MCU. As [Figure 1](#) shows, with PSoC™ Creator you can:

1. Explore the library of 200+ components.
2. Drag and drop component icons to complete your hardware system design in the main design workspace.
3. Configure Components using the Component configuration tools and the Component datasheets.
4. Co-design your application firmware and hardware in the PSoC™ Creator IDE or build a project for a third-party IDE.
5. Prototype your solution with the PSoC™ 4 Pioneer kits. If a design change is needed, PSoC™ Creator and Components enable you to make changes on-the-fly without the need for hardware revisions.

1 Development ecosystem

For information on Infineon tools, refer to the documentation delivered with PSoC™ Creator software, and [AN79953: Getting started with PSoC™ 4](#).

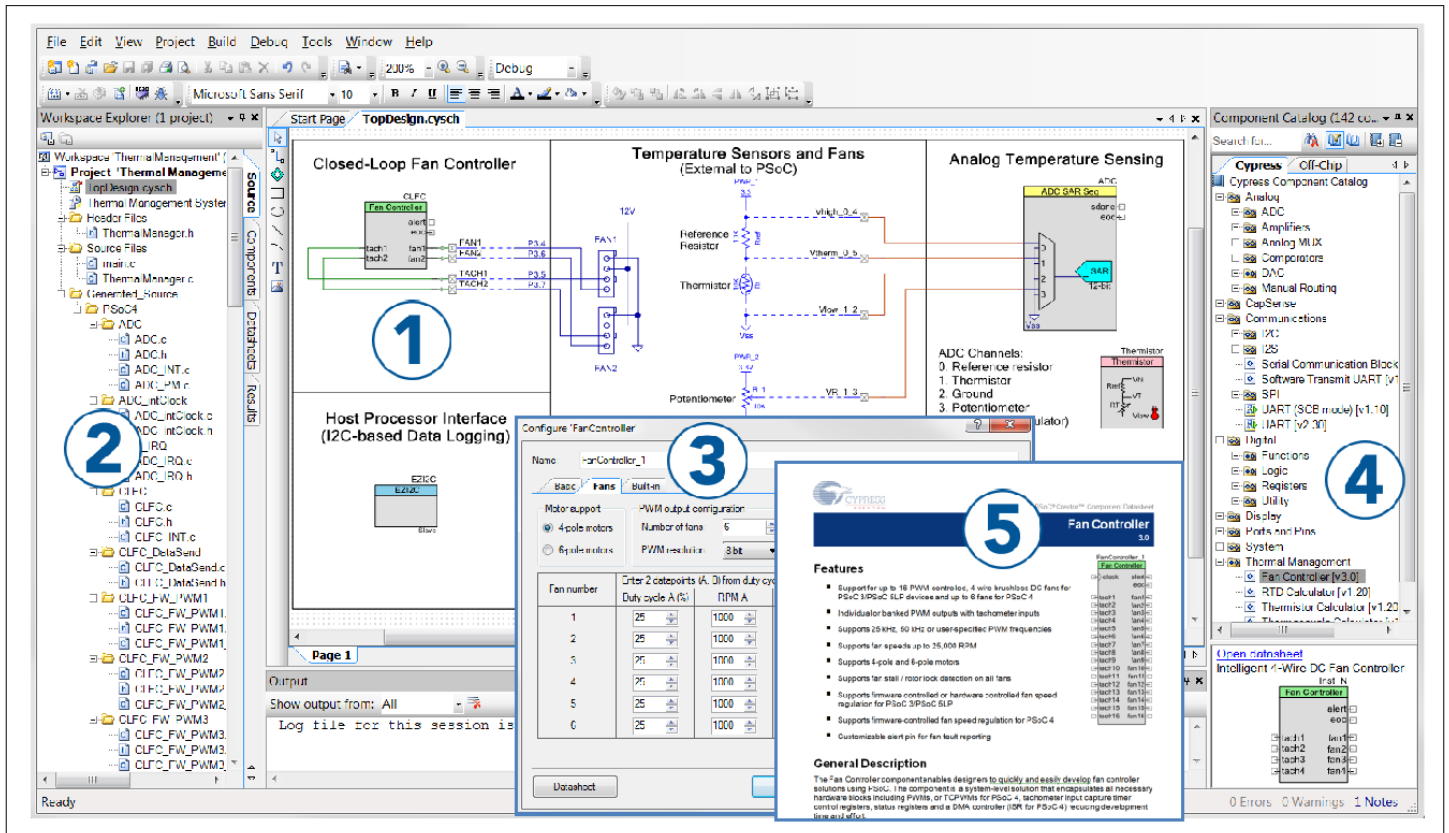


Figure 1 Multiple-sensor example project in PSoC™ Creator

2 Block diagram

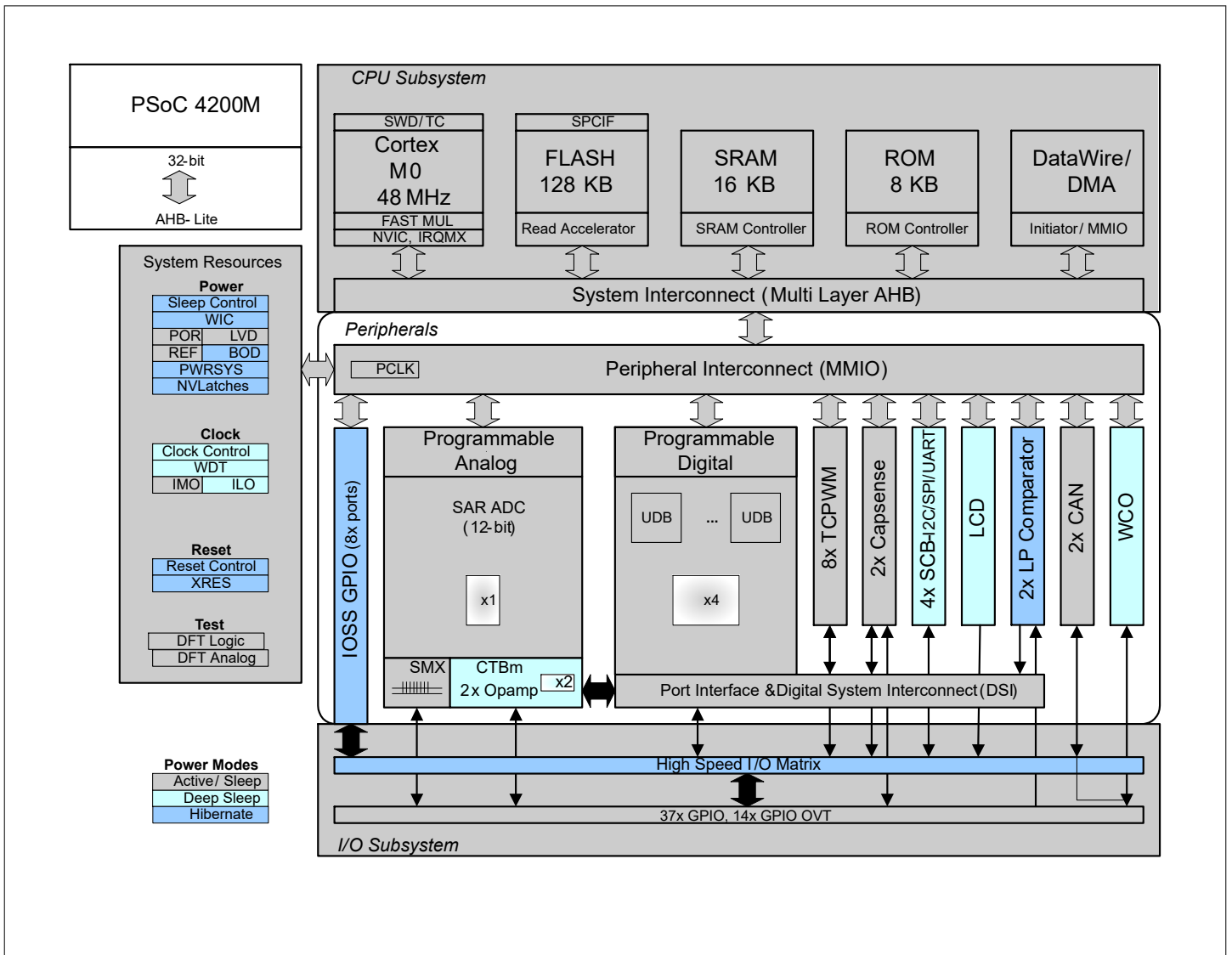


Figure 2 Block diagram

The PSoC™ 4200M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully-integrated programming and debug support for PSoC™ 4200M devices. The SWD interface is fully compatible with industry-standard third-party tools. PSoC™ 4200M provides a level of security not possible with multichip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in the firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and

interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC™ 4200M with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC™ 4200M allows the customer to make.

3 Functional definition

3.1 CPU and memory subsystem

3.1.1 CPU

The Cortex®-M0 CPU in the PSoC™ 4200M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with an extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC™ 4200M has four break-point (address) comparators and two watchpoint (data) comparators.

3.1.2 Flash

The PSoC™ 4200M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

3.1.3 SRAM

The SRAM memory is retained during Hibernate.

3.1.4 SROM

A supervisory ROM that contains boot and configuration routines is provided.

3.1.5 DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

3.2 System resources

3.2.1 Power system

The power system is described in detail in the section [Power](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper function or generate resets (brownout detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC™ 4200M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC™ 4200M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

3.2.2 Clock system

The PSoC™ 4200M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC™ 4200M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

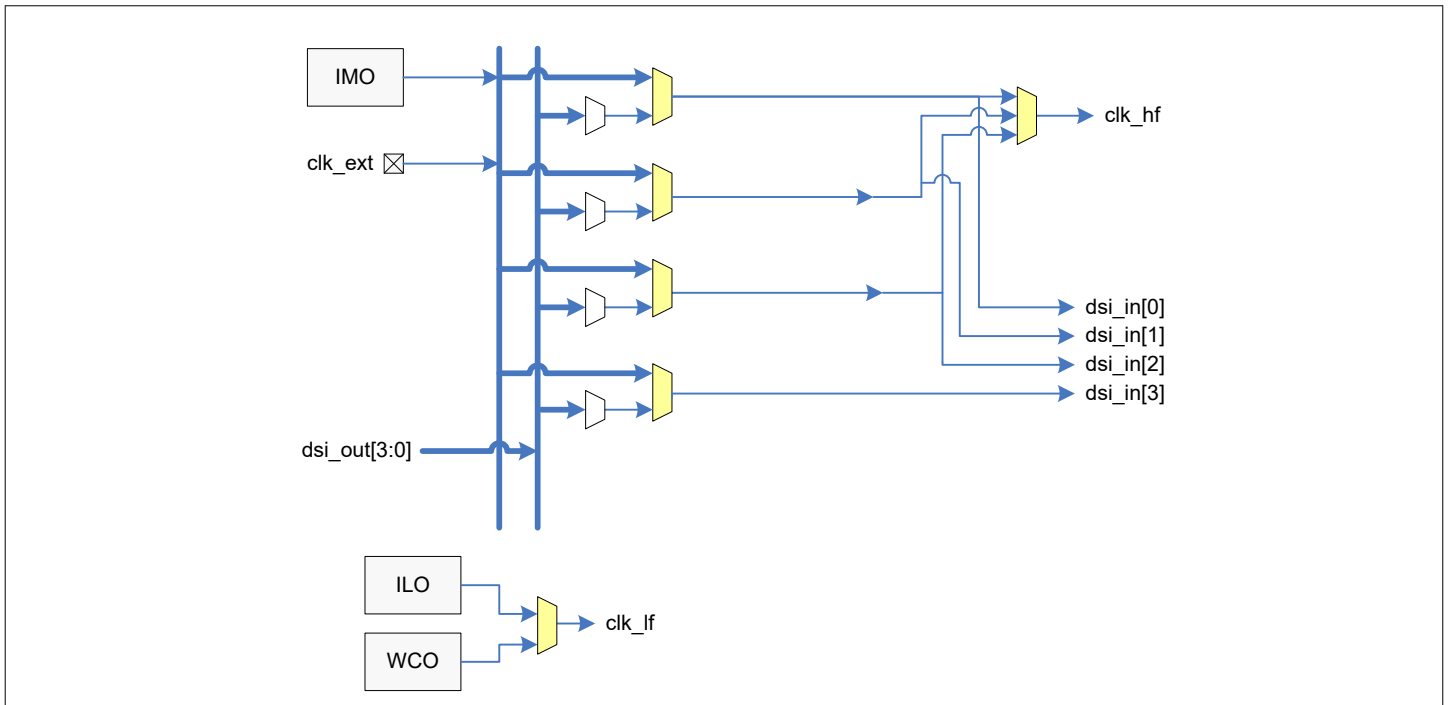


Figure 3 PSoC™ 4200M MCU clocking architecture

The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC™ 4200M, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC™ Creator.

3.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4200M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in non-volatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. The IMO tolerance with Infineon-provided calibration settings is $\pm 2\%$.

3.2.4 ILO clock source

The ILO is a very low-power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. The ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

3.2.5 Crystal oscillator

The PSoC™ 4200M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

3.2.6 Watchdog timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

3.2.7 Reset

The PSoC™ 4200M can be reset from a variety of sources including a software reset. The Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

3.2.8 Voltage reference

The PSoC™ 4200M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

3.3 Analog blocks

3.3.1 12-bit SAR ADC

The 12-bit 1 MSample/second SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to $\pm 1\%$) and by providing the choice of three internal voltage references: V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

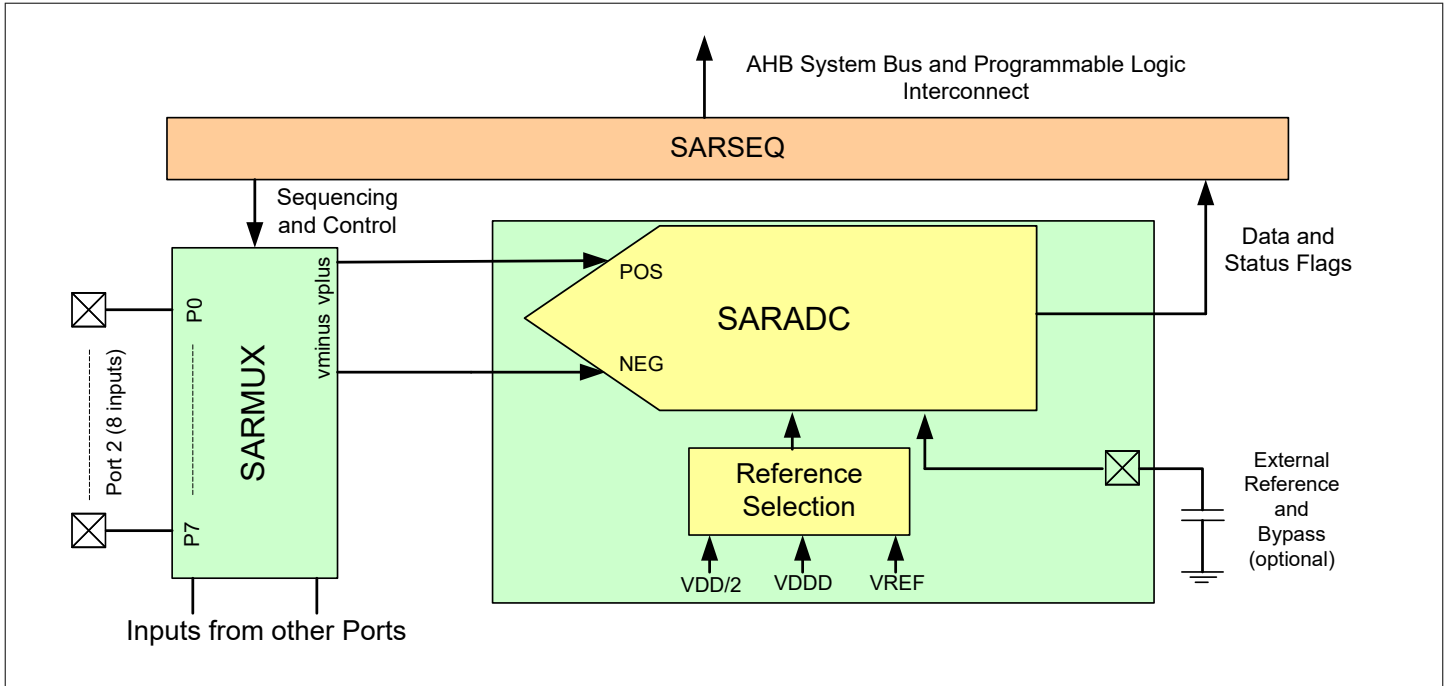


Figure 4 SAR ADC system diagram

3.3.2 Analog multiplex bus

The PSoC™ 4200M has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CAPSENSE™ blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CAPSENSE™ purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

3.3.3 Four opamps

The PSoC™ 4200M has four opamps with comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

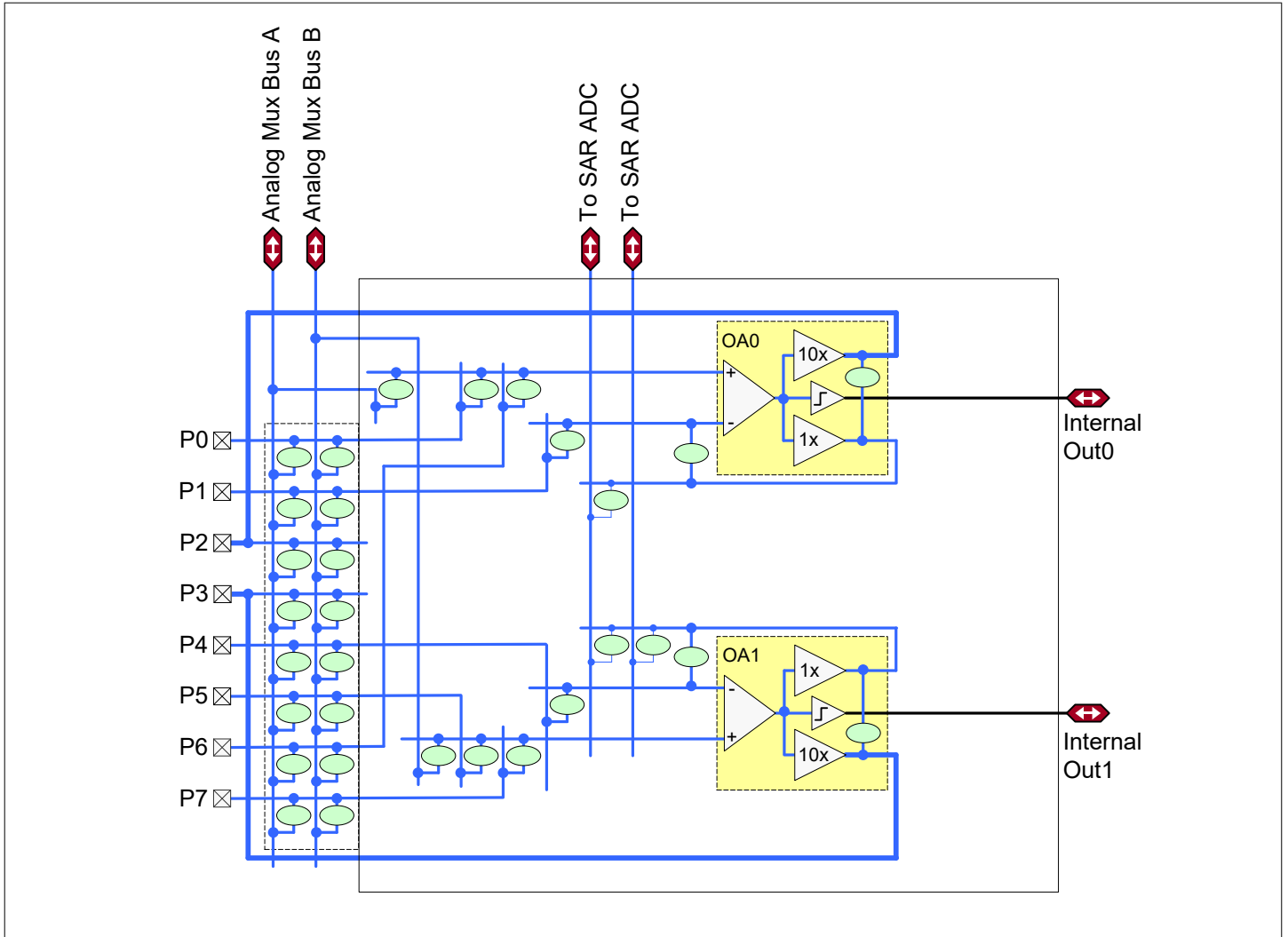


Figure 5 Identical opamp pairs in opamp subsystem

The ovals in Figure 5 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

3.3.4 Temperature sensor

The PSoC™ 4200M has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Infineon-supplied software that includes calibration and linearization.

3.3.5 Low-power comparators

The PSoC™ 4200M has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

3.4 Programmable digital

3.4.1 Universal digital blocks (UDBs) and port interfaces

The PSoC™ 4200M has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

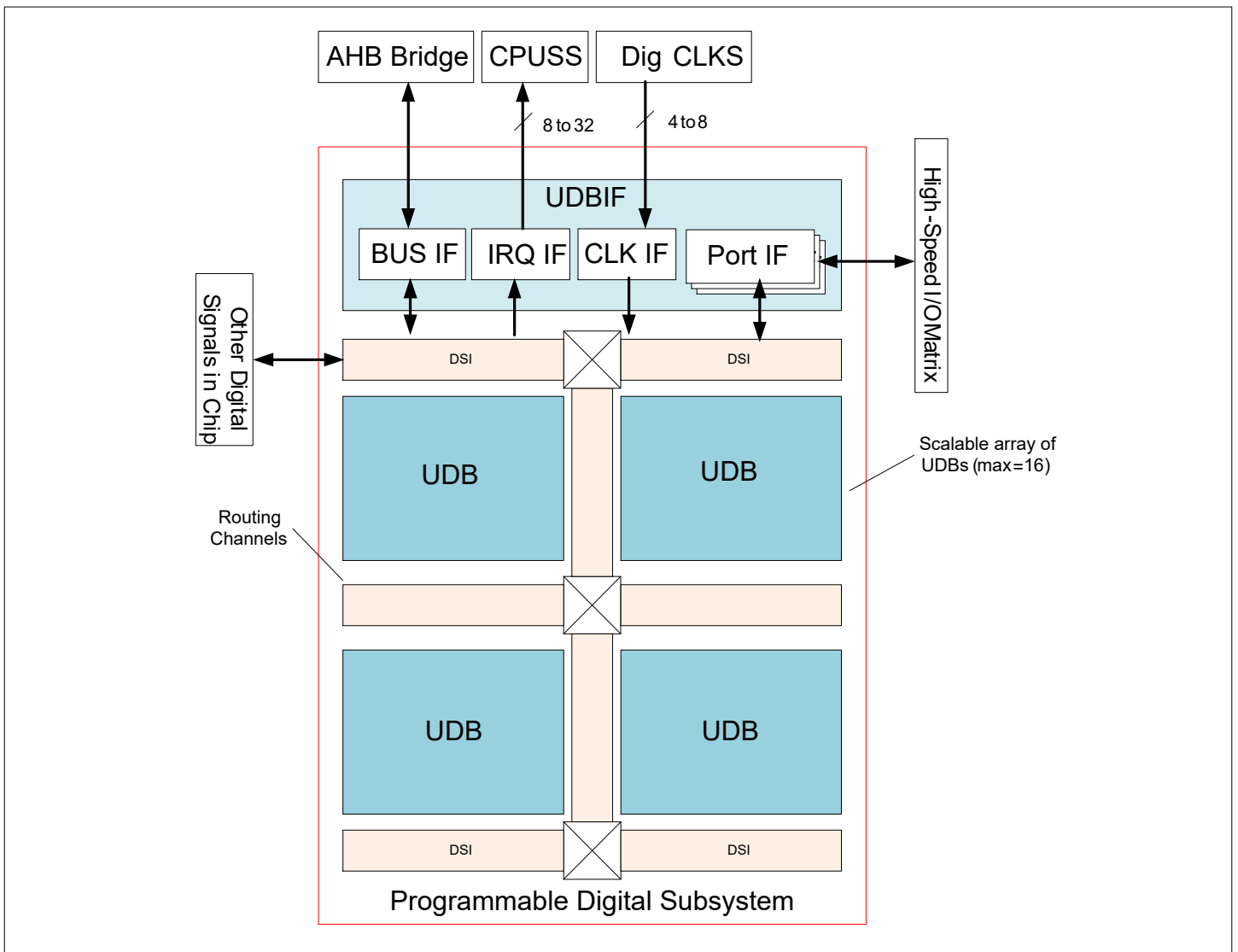


Figure 6 UDB array

The UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 7.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs can connect to any pin on Ports 0, 1, 2, and 3 (each port interconnect requires one UDB) through the DSI.

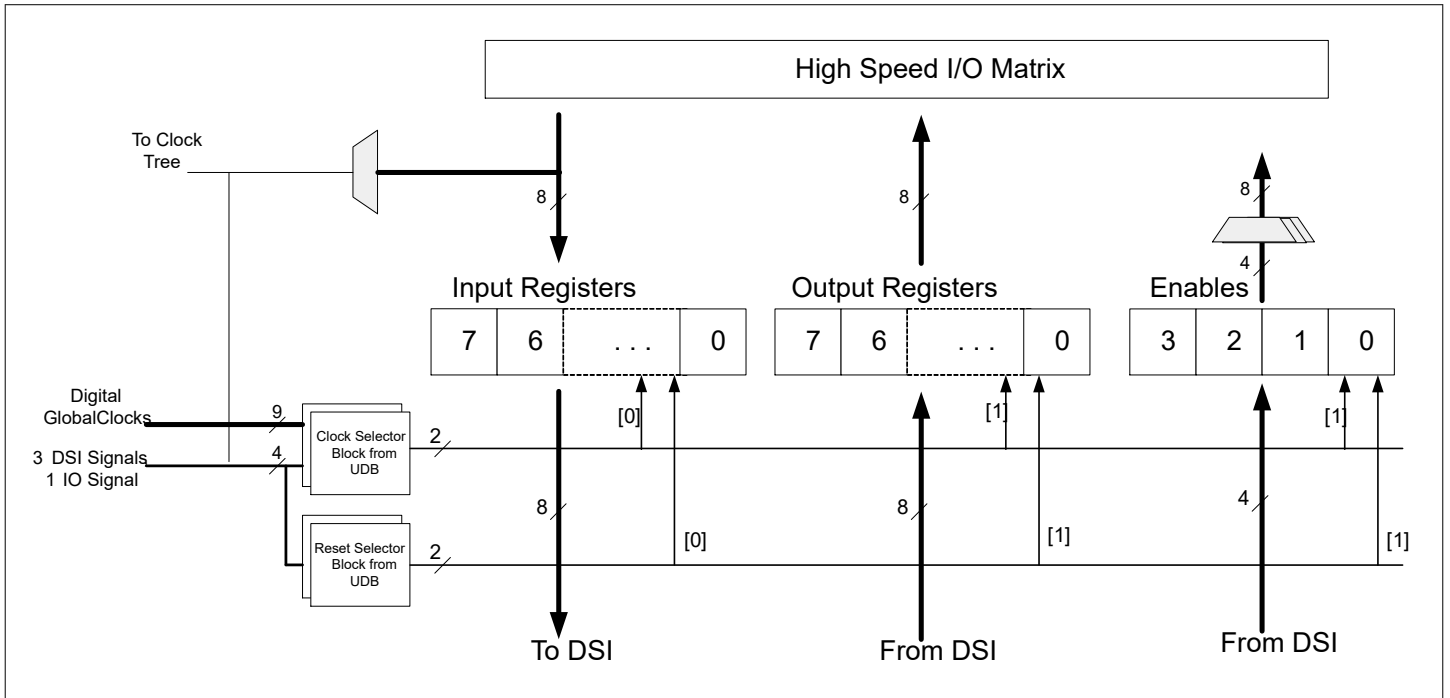


Figure 7 Port interface

3.5 Fixed function digital

3.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block uses a 16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC™ 4200M has eight TCPWM blocks.

3.5.2 Serial communication blocks (SCB)

The PSoC™ 4200M has four SCBs, which can each implement an I²C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI²C that creates a mailbox address range in the memory of the PSoC™ 4200M and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the

time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

3.5.3 CAN blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

3.6 GPIO

The PSoC™ 4200M has 55 GPIOs in the 68-pin QFN package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin on Ports 0, 1, 2, and 3 may be routed to any UDB through the DSI network. Only pins on Ports 0, 1, 2, and 3 may be routed through DSI signals.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (8 for PSoC™ 4200M).

The Pins of Port 6 (up to 6 depending on the package) are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 μ A when their inputs exceed V_{DDIO} in compliance with I²C specifications.

3.7 Special function peripherals

3.7.1 LCD segment drive

The PSoC™ 4200M has an LCD controller, which can drive up to eight commons and up to 49 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays.

3.7.2 CAPSENSE™

CAPSENSE™ is supported on all pins in the PSoC™ 4200M through a Capacitive Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CAPSENSE™ functionality can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CAPSENSE™ block, which provides automatic hardware tuning (Infineon SmartSense), to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CSD block has two IDACs which can be used for general purposes if CAPSENSE™ is not being used. (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available). The PSoC™ 4200M has two CSD blocks which can be used independently; one for CAPSENSE™ and one providing two IDACs.

The two CAPSENSE™ blocks are referred to as CSD0 and CSD1. Capacitance sensing inputs on Ports 0, 1, 2, 3, 4, 6, and 7 are sensed by CSD0. Capacitance sensing inputs on Port 5 are sensed by CSD1.

4 Pinouts

The following is the pin list for the PSoC™ 4200M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

| 68-QFN | | 64-TQFP | | 48-TQFP | | 44-TQFP | |
|--------|-----------|---------|-----------|---------|-----------|---------|-----------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 42 | P0.0 | 39 | P0.0 | 28 | P0.0 | 24 | P0.0 |
| 43 | P0.1 | 40 | P0.1 | 29 | P0.1 | 25 | P0.1 |
| 44 | P0.2 | 41 | P0.2 | 30 | P0.2 | 26 | P0.2 |
| 45 | P0.3 | 42 | P0.3 | 31 | P0.3 | 27 | P0.3 |
| 46 | P0.4 | 43 | P0.4 | 32 | P0.4 | 28 | P0.4 |
| 47 | P0.5 | 44 | P0.5 | 33 | P0.5 | 29 | P0.5 |
| 48 | P0.6 | 45 | P0.6 | 34 | P0.6 | 30 | P0.6 |
| 49 | P0.7 | 46 | P0.7 | 35 | P0.7 | 31 | P0.7 |
| 50 | XRES | 47 | XRES | 36 | XRES | 32 | XRES |
| 51 | VCCD | 48 | VCCD | 37 | VCCD | 33 | VCCD |
| 52 | VSSD | 49 | VSSD | 38 | VSSD | - | - |
| 53 | VDDD | 50 | VDDD | 39 | VDDD | 34 | VDDD |
| - | - | - | - | 40 | VDDA | 35 | VDDA |
| 62 | P1.0 | 58 | P1.0 | 42 | P1.0 | 37 | P1.0 |
| 63 | P1.1 | 59 | P1.1 | 43 | P1.1 | 38 | P1.1 |
| 64 | P1.2 | 60 | P1.2 | 44 | P1.2 | 39 | P1.2 |
| 65 | P1.3 | 61 | P1.3 | 45 | P1.3 | 40 | P1.3 |
| 66 | P1.4 | 62 | P1.4 | 46 | P1.4 | 41 | P1.4 |
| 67 | P1.5 | 63 | P1.5 | 47 | P1.5 | 42 | P1.5 |
| 68 | P1.6 | 64 | P1.6 | 48 | P1.6 | 43 | P1.6 |
| 1 | P1.7/VREF | 1 | P1.7/VREF | 1 | P1.7/VREF | 44 | P1.7/VREF |
| - | - | - | - | - | - | 1 | VSSD |
| 2 | P2.0 | 2 | P2.0 | 2 | P2.0 | 2 | P2.0 |
| 3 | P2.1 | 3 | P2.1 | 3 | P2.1 | 3 | P2.1 |
| 4 | P2.2 | 4 | P2.2 | 4 | P2.2 | 4 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | 5 | P2.3 | 5 | P2.3 |
| 6 | P2.4 | 6 | P2.4 | 6 | P2.4 | 6 | P2.4 |
| 7 | P2.5 | 7 | P2.5 | 7 | P2.5 | 7 | P2.5 |
| 8 | P2.6 | 8 | P2.6 | 8 | P2.6 | 8 | P2.6 |
| 9 | P2.7 | 9 | P2.7 | 9 | P2.7 | 9 | P2.7 |
| 10 | VSSA | 10 | VSSA | 10 | VSSD | 10 | VSSD |
| 11 | VDDA | 11 | VDDA | - | - | - | - |

4 Pinouts

| 68-QFN | | 64-TQFP | | 48-TQFP | | 44-TQFP | |
|--------|-------|---------|-------|---------|-------|---------|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 19 | P3.0 | 18 | P3.0 | 12 | P3.0 | 11 | P3.0 |
| 20 | P3.1 | 19 | P3.1 | 13 | P3.1 | 12 | P3.1 |
| 21 | P3.2 | 20 | P3.2 | 14 | P3.2 | 13 | P3.2 |
| 22 | P3.3 | 21 | P3.3 | 16 | P3.3 | 14 | P3.3 |
| 23 | P3.4 | 22 | P3.4 | 17 | P3.4 | 15 | P3.4 |
| 24 | P3.5 | 23 | P3.5 | 18 | P3.5 | 16 | P3.5 |
| 25 | P3.6 | 24 | P3.6 | 19 | P3.6 | 17 | P3.6 |
| 26 | P3.7 | 25 | P3.7 | 20 | P3.7 | 18 | P3.7 |
| 27 | VDDIO | 26 | VDDIO | 21 | VDDIO | 19 | VDDD |
| 28 | P4.0 | 27 | P4.0 | 22 | P4.0 | 20 | P4.0 |
| 29 | P4.1 | 28 | P4.1 | 23 | P4.1 | 21 | P4.1 |
| 30 | P4.2 | 29 | P4.2 | 24 | P4.2 | 22 | P4.2 |
| 31 | P4.3 | 30 | P4.3 | 25 | P4.3 | 23 | P4.3 |
| 32 | P4.4 | 31 | P4.4 | - | - | - | - |
| 33 | P4.5 | 32 | P4.5 | - | - | - | - |
| 34 | P4.6 | 33 | P4.6 | - | - | - | - |
| 35 | P4.7 | - | - | - | - | - | - |
| 54 | P5.0 | 51 | P5.0 | - | - | - | - |
| 55 | P5.1 | 52 | P5.1 | - | - | - | - |
| 56 | P5.2 | 53 | P5.2 | - | - | - | - |
| 57 | P5.3 | 54 | P5.3 | - | - | - | - |
| 58 | P5.4 | - | - | - | - | - | - |
| 59 | P5.5 | 55 | P5.5 | - | - | - | - |
| 60 | VDDA | 56 | VDDA | 40 | VDDA | 35 | VDDA |
| 61 | VSSA | 57 | VSSA | 41 | VSSA | 36 | VSSA |
| 12 | P6.0 | 12 | P6.0 | - | - | - | - |
| 13 | P6.1 | 13 | P6.1 | - | - | - | - |
| 14 | P6.2 | 14 | P6.2 | - | - | - | - |
| 15 | P6.3 | - | - | - | - | - | - |
| 16 | P6.4 | 15 | P6.4 | - | - | - | - |
| 17 | P6.5 | 16 | P6.5 | - | - | - | - |
| 18 | VSSIO | 17 | VSSIO | 10 | VSSD | 10 | VSSD |
| 39 | P7.0 | 37 | P7.0 | 26 | P7.0 | - | - |
| 40 | P7.1 | 38 | P7.1 | 27 | P7.1 | - | - |

4 Pinouts

| 68-QFN | | 64-TQFP | | 48-TQFP | | 44-TQFP | |
|--------|------|---------|------|---------|------|---------|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 41 | P7.2 | - | - | - | - | - | - |

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions.

| Port/ Pin | Analog | Alt. Function 1 | Alt. Function 2 | Alt. Function 3 | Alt. Function 4 | Alt. Function 5 |
|--------------|------------------|----------------------|-------------------|------------------------|------------------|-----------------------|
| P0.0 | lpcomp.in_p[0] | - | - | can[1].can_rx:0 | - | scb[0].spi_select 1:0 |
| P0.1 | lpcomp.in_n[0] | - | - | can[1].can_tx:0 | - | scb[0].spi_select 2:0 |
| P0.2 | lpcomp.in_p[1] | - | - | - | - | scb[0].spi_select 3:0 |
| P0.3 | lpcomp.in_n[1] | - | - | - | - | - |
| P0.4 | wco_in | - | scb[1].uart_rx:0 | - | scb[1].i2c_scl:0 | scb[1].spi_mosi: 1 |
| P0.5 | wco_out | - | scb[1].uart_tx:0 | - | scb[1].i2c_sda:0 | scb[1].spi_miso: 1 |
| P0.6 | - | ext_clk:0 | scb[1].uart_cts:0 | - | - | scb[1].spi_clk:1 |
| P0.7 | - | - | scb[1].uart_rts:0 | can[1].can_tx_en b_n:0 | wakeup | scb[1].spi_select 0:1 |
| P5.0 | ctb1.oa0.inp | tcpwm.line[4] | scb[2].uart_rx:0 | - | scb[2].i2c_scl:0 | scb[2].spi_mosi: 0 |
| P5.1 | ctb1.oa0.inm | tcpwm.line_com pl[4] | scb[2].uart_tx:0 | - | scb[2].i2c_sda:0 | scb[2].spi_miso: 0 |
| P5.2 | ctb1.oa0.out | tcpwm.line[5] | scb[2].uart_cts:0 | - | lpcomp.comp[0]:1 | scb[2].spi_clk:0 |
| P5.3 | ctb1.oa1.out | tcpwm.line_com pl[5] | scb[2].uart_rts:0 | - | lpcomp.comp[1]:1 | scb[2].spi_select 0:0 |
| P5.4 | ctb1.oa1.inm | tcpwm.line[6] | - | - | - | scb[2].spi_select 1:0 |
| P5.5 | ctb1.oa1.inp | tcpwm.line_com pl[6] | - | - | - | scb[2].spi_select 2:0 |
| P5.6 | ctb1.oa0.inp_alt | tcpwm.line[7] | - | - | - | scb[2].spi_select 3:0 |
| P5.7 | ctb1.oa1.inp_alt | tcpwm.line_com pl[7] | - | - | - | - |

4 Pinouts

| Port/ Pin | Analog | Alt. Function 1 | Alt. Function 2 | Alt. Function 3 | Alt. Function 4 | Alt. Function 5 |
|--------------|------------------|---------------------|-------------------|-----------------------|------------------|----------------------|
| P1.0 | ctb0.aa0.inp | tcpwm.line[2] | scb[0].uart_rx:1 | - | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | ctb0.aa0.inm | tcpwm.line_compl[2] | scb[0].uart_tx:1 | - | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | ctb0.aa0.out | tcpwm.line[3] | scb[0].uart_cts:1 | - | - | scb[0].spi_clk:1 |
| P1.3 | ctb0.aa1.out | tcpwm.line_compl[3] | scb[0].uart_rts:1 | - | - | scb[0].spi_select0:1 |
| P1.4 | ctb0.aa1.inm | tcpwm.line[6] | - | - | - | scb[0].spi_select1:1 |
| P1.5 | ctb0.aa1.inp | tcpwm.line_compl[6] | - | - | - | scb[0].spi_select2:1 |
| P1.6 | ctb0.aa0.inp_alt | tcpwm.line[7] | - | - | - | scb[0].spi_select3:1 |
| P1.7 | ctb0.aa1.inp_alt | tcpwm.line_compl[7] | - | - | - | - |
| P2.0 | sarmux.0 | tcpwm.line[4] | - | - | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | sarmux.1 | tcpwm.line_compl[4] | - | - | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | sarmux.2 | tcpwm.line[5] | - | - | - | scb[1].spi_clk:2 |
| P2.3 | sarmux.3 | tcpwm.line_compl[5] | - | - | - | scb[1].spi_select0:2 |
| P2.4 | sarmux.4 | tcpwm.line[0] | - | - | - | scb[1].spi_select1:1 |
| P2.5 | sarmux.5 | tcpwm.line_compl[0] | - | - | - | scb[1].spi_select2:1 |
| P2.6 | sarmux.6 | tcpwm.line[1] | - | - | - | scb[1].spi_select3:1 |
| P2.7 | sarmux.7 | tcpwm.line_compl[1] | - | - | - | scb[3].spi_select0:1 |
| P6.0 | - | tcpwm.line[4] | scb[3].uart_rx:0 | can[0].can_tx_enb_n:0 | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 |
| P6.1 | - | tcpwm.line_compl[4] | scb[3].uart_tx:0 | can[0].can_rx:0 | scb[3].i2c_sda:0 | scb[3].spi_miso:0 |
| P6.2 | - | tcpwm.line[5] | scb[3].uart_cts:0 | can[0].can_tx:0 | - | scb[3].spi_clk:0 |
| P6.3 | - | tcpwm.line_compl[5] | scb[3].uart_rts:0 | - | - | scb[3].spi_select0:0 |
| P6.4 | - | tcpwm.line[6] | - | - | - | scb[3].spi_select1:0 |

4 Pinouts

| Port/ Pin | Analog | Alt. Function 1 | Alt. Function 2 | Alt. Function 3 | Alt. Function 4 | Alt. Function 5 |
|--------------|------------------|---------------------|-------------------|-----------------------|------------------|----------------------|
| P6.5 | - | tcpwm.line_compl[6] | - | - | - | scb[3].spi_select2:0 |
| P3.0 | - | tcpwm.line[0] | scb[1].uart_rx:1 | - | scb[1].i2c_scl:2 | scb[1].spi_mosi:0 |
| P3.1 | - | tcpwm.line_compl[0] | scb[1].uart_tx:1 | - | scb[1].i2c_sda:2 | scb[1].spi_miso:0 |
| P3.2 | - | tcpwm.line[1] | scb[1].uart_cts:1 | - | swd_data | scb[1].spi_clk:0 |
| P3.3 | - | tcpwm.line_compl[1] | scb[1].uart_rts:1 | - | swd_clk | scb[1].spi_select0:0 |
| P3.4 | - | tcpwm.line[2] | - | - | - | scb[1].spi_select1:0 |
| P3.5 | - | tcpwm.line_compl[2] | - | - | - | scb[1].spi_select2:0 |
| P3.6 | - | tcpwm.line[3] | - | - | - | scb[1].spi_select3:0 |
| P3.7 | - | tcpwm.line_compl[3] | - | - | - | - |
| P4.0 | - | - | scb[0].uart_rx:0 | can[0].can_rx:1 | scb[0].i2c_scl:1 | scb[0].spi_mosi:0 |
| P4.1 | - | - | scb[0].uart_tx:0 | can[0].can_tx:1 | scb[0].i2c_sda:1 | scb[0].spi_miso:0 |
| P4.2 | csd[0].c_mod | - | scb[0].uart_cts:0 | can[0].can_tx_enb_n:1 | lpcomp.comp[0]:0 | scb[0].spi_clk:0 |
| P4.3 | csd[0].c_sh_tank | - | scb[0].uart_rts:0 | - | lpcomp.comp[1]:0 | scb[0].spi_select0:0 |
| P4.4 | - | - | - | can[1].can_tx_enb_n:1 | - | scb[0].spi_select1:2 |
| P4.5 | - | - | - | can[1].can_rx:1 | - | scb[0].spi_select2:2 |
| P4.6 | - | - | - | can[1].can_tx:1 | - | scb[0].spi_select3:2 |
| P4.7 | - | - | - | - | - | - |
| P7.0 | - | tcpwm.line[0] | scb[3].uart_rx:1 | - | scb[3].i2c_scl:1 | scb[3].spi_mosi:1 |
| P7.1 | - | tcpwm.line_compl[0] | scb[3].uart_tx:1 | - | scb[3].i2c_sda:1 | scb[3].spi_miso:1 |
| P7.2 | - | tcpwm.line[1] | scb[3].uart_cts:1 | - | - | scb[3].spi_clk:1 |

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VDDIO: I/O pin power domain.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply ($1.8\text{ V} \pm 5\%$).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

5 Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

PSoC™ 4200M allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

5.1 Unregulated external supply

In this mode, the PSoC™ 4200M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4200M supplies the internal logic and the VCCD output of the PSoC™ 4200M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 μ F; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 μ F range in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

| Power Supply | Bypass Capacitors |
|-------------------------|--|
| VDDD–VSS and VDDIO–VSS | 0.1 μ F ceramic at each pin plus bulk capacitor 1 to 10 μ F |
| VDDA–VSSA | 0.1 μ F ceramic at pin. Additional 1 μ F to 10 μ F bulk capacitor |
| VCCD–VSS | 1 μ F ceramic capacitor at the VCCD pin |
| VREF–VSSA (optional) | The internal bandgap may be bypassed with a 1 μ F to 10 μ F capacitor for better ADC performance |

5.2 Regulated external supply

In this mode, the PSoC™ 4200M is powered by an external power supply that must be within the range of 1.71 to 1.89 V ($1.8 \pm 5\%$); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

6 Electrical specifications

6.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------------------------|---|------|-----|----------------------|------|----------------------|
| SID1 | V _{DD_ABS} | Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA}) | -0.5 | - | 6 | V | Absolute maximum |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SSD} | -0.5 | - | 1.95 | V | Absolute maximum |
| SID3 | V _{GPIO_ABS} | GPIO voltage; V _{DDD} or V _{DDA} | -0.5 | - | V _{DD} +0.5 | V | Absolute maximum |
| SID4 | I _{GPIO_ABS} | Current per GPIO | -25 | - | 25 | mA | Absolute maximum |
| SID5 | I _{G-PIO_injection} | GPIO injection current per pin | -0.5 | - | 0.5 | mA | Absolute maximum |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | - | - | V | - |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | - | - | V | - |
| BID46 | LU | Pin current for latch-up | -140 | - | 140 | mA | - |

Note: Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device level specifications

All specifications are valid for -40°C ≤ TA ≤ 105°C and TJ ≤ 125°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2 DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------------|---|------|-----|------|------|-------------------------------|
| SID53 | V _{DD} | Power Supply Input Voltage (V _{DDA} = V _{DDD} = V _{DD}) | 1.8 | - | 5.5 | V | With regulator enabled |
| SID255 | V _{DDD} | Power Supply Input Voltage unregulated | 1.71 | 1.8 | 1.89 | V | Internally unregulated Supply |
| SID54 | V _{CCD} | Output voltage (for core logic) | - | 1.8 | - | V | - |

(table continues...)

Table 2 (continued) DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------------|-----------------------------------|-----|-----|-----|------|-----------------------|
| SID55 | C _{EFC} | External Regulator voltage bypass | 1 | 1.3 | 1.6 | μF | X5R ceramic or better |
| SID56 | C _{EXC} | Power supply decoupling capacitor | – | 1 | – | μF | X5R ceramic or better |

Active Mode, V_{DD} = 1.71 V to 5.5 V, –40°C to +105°C

| | | | | | | | |
|------|------------------|-----------------------------------|---|-----|------|----|---|
| SID6 | I _{DD1} | Execute from Flash; CPU at 6 MHz | – | 2.2 | 2.8 | mA | – |
| SID7 | I _{DD2} | Execute from Flash; CPU at 12 MHz | – | 3.7 | 4.2 | mA | – |
| SID8 | I _{DD3} | Execute from Flash; CPU at 24 MHz | – | 6.7 | 7.2 | mA | – |
| SID9 | I _{DD4} | Execute from Flash; CPU at 48 MHz | – | 13 | 13.8 | mA | – |

Sleep Mode, –40°C to +105°C

| | | | | | | | |
|-------|-------------------|---|---|------|-----|----|--|
| SID21 | I _{DD16} | I ² C wakeup, WDT, and Comparators on. Regulator Off | – | 1.75 | 2.1 | mA | V _{DD} = 1.71 to 1.89, 6 MHz |
| SID22 | I _{DD17} | I ² C wakeup, WDT, and Comparators on | – | 1.7 | 2.1 | mA | V _{DD} = 1.8 to 5.5, 6 MHz |
| SID23 | I _{DD18} | I ² C wakeup, WDT, and Comparators on. Regulator Off | – | 2.35 | 2.8 | mA | V _{DD} = 1.71 to 1.89, 12 MHz |
| SID24 | I _{DD19} | I ² C wakeup, WDT, and Comparators on | – | 2.25 | 2.8 | mA | V _{DD} = 1.8 to 5.5, 12 MHz |

Deep Sleep Mode, –40°C to + 60°C

| | | | | | | | |
|-------|-------------------|---|---|------|----|----|--------------------------------|
| SID30 | I _{DD25} | I ² C wakeup and WDT on. Regulator Off | – | 1.55 | 20 | μA | V _{DD} = 1.71 to 1.89 |
| SID31 | I _{DD26} | I ² C wakeup and WDT on | – | 1.35 | 15 | μA | V _{DD} = 1.8 to 3.6 |
| SID32 | I _{DD27} | I ² C wakeup and WDT on | – | 1.5 | 15 | μA | V _{DD} = 3.6 to 5.5 |

Deep Sleep Mode, +85°C

| | | | | | | | |
|-------|-------------------|---|---|---|----|----|--------------------------------|
| SID33 | I _{DD28} | I ² C wakeup and WDT on. Regulator Off | – | – | 60 | μA | V _{DD} = 1.71 to 1.89 |
| SID34 | I _{DD29} | I ² C wakeup and WDT on | – | – | 45 | μA | V _{DD} = 1.8 to 3.6 |
| SID35 | I _{DD30} | I ² C wakeup and WDT on | – | – | 30 | μA | V _{DD} = 3.6 to 5.5 |

Deep Sleep Mode, +105°C

| | | | | | | | |
|--------|--------------------|---|---|---|-----|----|--------------------------------|
| SID33Q | I _{DD28Q} | I ² C wakeup and WDT on. Regulator Off | – | – | 135 | μA | V _{DD} = 1.71 to 1.89 |
| SID34Q | I _{DD29Q} | I ² C wakeup and WDT on | – | – | 180 | μA | V _{DD} = 1.8 to 3.6 |
| SID35Q | I _{DD30Q} | I ² C wakeup and WDT on | – | – | 140 | μA | V _{DD} = 3.6 to 5.5 |

Hibernate Mode, –40°C to + 60°C

| | | | | | | | |
|-------|-------------------|---------------|---|-----|------|----|--------------------------------|
| SID39 | I _{DD34} | Regulator Off | – | 150 | 3000 | nA | V _{DD} = 1.71 to 1.89 |
|-------|-------------------|---------------|---|-----|------|----|--------------------------------|

(table continues...)

Table 2 (continued) DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------|-------------|-----|-----|------|------|------------------------------|
| SID40 | I _{DD35} | – | – | 150 | 1000 | nA | V _{DD} = 1.8 to 3.6 |
| SID41 | I _{DD36} | – | – | 150 | 1100 | nA | V _{DD} = 3.6 to 5.5 |

Hibernate Mode, +85°C

| | | | | | | | |
|-------|-------------------|---------------|---|---|------|----|--------------------------------|
| SID42 | I _{DD37} | Regulator Off | – | – | 4500 | nA | V _{DD} = 1.71 to 1.89 |
| SID43 | I _{DD38} | – | – | – | 3500 | nA | V _{DD} = 1.8 to 3.6 |
| SID44 | I _{DD39} | – | – | – | 3500 | nA | V _{DD} = 3.6 to 5.5 |

Hibernate Mode, +105°C

| | | | | | | | |
|--------|--------------------|---------------|---|---|------|----|--------------------------------|
| SID42Q | I _{DD37Q} | Regulator Off | – | – | 19.4 | µA | V _{DD} = 1.71 to 1.89 |
| SID43Q | I _{DD38Q} | – | – | – | 17 | µA | V _{DD} = 1.8 to 3.6 |
| SID44Q | I _{DD39Q} | – | – | – | 16 | µA | V _{DD} = 3.6 to 5.5 |

Stop Mode

| | | | | | | | |
|---------|--------------------|--|---|----|------|----|--------------------|
| SID304 | I _{DD43A} | Stop Mode current; V _{DD} = 3.6 V | – | 35 | 85 | nA | T = –40°C to +60°C |
| SID304A | I _{DD43B} | Stop Mode current; V _{DD} = 3.6 V | – | – | 1450 | nA | T = +85°C |

Stop Mode, +105°C

| | | | | | | | |
|---------|---------------------|--|---|---|------|----|---|
| SID304Q | I _{DD43AQ} | Stop Mode current; V _{DD} = 3.6 V | – | – | 5645 | nA | – |
|---------|---------------------|--|---|---|------|----|---|

XRES current

| | | | | | | | |
|--------|--------------------|------------------------------------|---|---|---|----|---|
| SID307 | I _{DD_XR} | Supply current while XRES asserted | – | 2 | 5 | mA | – |
|--------|--------------------|------------------------------------|---|---|---|----|---|

Table 3 AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|-------------------------|-----------------------------|-----|-----|-----|------|------------------------------|
| SID48 | F _{CPU} | CPU frequency | DC | – | 48 | MHz | 1.71 ≤ V _{DD} ≤ 5.5 |
| SID49 ¹⁾ | T _{SLEEP} | Wakeup from sleep mode | – | 0 | – | µs | – |
| SID50 ¹⁾ | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | – | 25 | µs | 24 MHz IMO |
| SID51 ¹⁾ | T _{HIBERNATE} | Wakeup from Hibernate mode | – | – | 0.7 | ms | – |
| SID51A ¹⁾ | T _{STOP} | Wakeup from Stop mode | – | – | 2 | ms | – |
| SID52 ¹⁾ | T _{RESETWIDTH} | External reset pulse width | 1 | – | – | µs | – |

1) Guaranteed by characterization.

6.2.1 GPIO

Table 4 GPIO DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|-----------------|--|-----------------------|-----|----------------------|------|--|
| SID57 | $V_{IH}^{1)}$ | Input voltage high threshold | $0.7 \times V_{DDD}$ | – | – | V | CMOS Input |
| SID57A | IIHS | Input current when Pad > V_{DDIO} for OVT inputs | – | – | 10 | μA | Per I ² C Spec |
| SID58 | V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DDD}$ | V | CMOS Input |
| SID241 | $V_{IH}^{1)}$ | LVTTL input, $V_{DDD} < 2.7$ V | $0.7 \times V_{DDD}$ | – | – | V | – |
| SID242 | V_{IL} | LVTTL input, $V_{DDD} < 2.7$ V | – | – | $0.3 \times V_{DDD}$ | V | – |
| SID243 | $V_{IH}^{1)}$ | LVTTL input, $V_{DDD} \geq 2.7$ V | 2.0 | – | – | V | – |
| SID244 | V_{IL} | LVTTL input, $V_{DDD} \geq 2.7$ V | – | – | 0.8 | V | – |
| SID59 | V_{OH} | Output voltage high level | $V_{DDD} - 0.6$ | – | – | V | $I_{OH} = 4$ mA, $V_{DDD} \geq 3$ V |
| SID60 | V_{OH} | Output voltage high level | $V_{DDD} - 0.5$ | – | – | V | $I_{OH} = 1$ mA at 1.8-V V_{DDD} |
| SID61 | V_{OL} | Output voltage low level | – | – | 0.6 | V | $I_{OL} = 4$ mA at 1.8-V V_{DDD} |
| SID62 | V_{OL} | Output voltage low level | – | – | 0.6 | V | $I_{OL} = 8$ mA, $V_{DDD} \geq 3$ V |
| SID62A | V_{OL} | Output voltage low level | – | – | 0.4 | V | $I_{OL} = 3$ mA, $V_{DDD} \geq 3$ V |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID65 ²⁾ | I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DDD} = 3.0$ V |
| SID65A ²⁾ | I_{IL_CTBM} | Input leakage current (absolute value) for CTBM pins | – | – | 4 | nA | – |
| SID66 | C_{IN} | Input capacitance | – | – | 7 | pF | – |
| SID67 | V_{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DDD} \geq 2.7$ V |
| SID68 | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DDD}$ | – | – | mV | – |
| SID69 ²⁾ | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μA | – |
| SID69A ²⁾ | I_{TOT_GPIO} | Maximum Total Source or Sink Chip Current | – | – | 200 | mA | – |

1) V_{IH} must not exceed $V_{DDD} + 0.2$ V.

2) Guaranteed by characterization.

Table 5 GPIO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|----------------------|--|-----|-----|------|------|--|
| SID70 | T _{RISEF} | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V V _{DDD} , Clod = 25 pF |
| SID71 | T _{FALLF} | Fall time in fast strong mode | 2 | – | 12 | ns | 3.3 V V _{DDD} , Clod = 25 pF |
| SID72 | T _{RISES} | Rise time in slow strong mode | 10 | – | 60 | ns | 3.3 V V _{DDD} , Clod = 25 pF |
| SID73 | T _{FALLS} | Fall time in slow strong mode | 10 | – | 60 | ns | 3.3 V V _{DDD} , Clod = 25 pF |
| SID74 | F _{GPIOUT1} | GPIO Fout; 3.3 V ≤ V _{DDD} ≤ 5.5 V. Fast strong mode. | – | – | 33 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID75 | F _{GPIOUT2} | GPIO Fout; 1.7 V ≤ V _{DDD} ≤ 3.3 V. Fast strong mode. | – | – | 16.7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID76 | F _{GPIOUT3} | GPIO Fout; 3.3 V ≤ V _{DDD} ≤ 5.5 V. Slow strong mode. | – | – | 7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID245 | F _{GPIOUT4} | GPIO Fout; 1.7 V ≤ V _{DDD} ≤ 3.3 V. Slow strong mode. | – | – | 3.5 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DDD} ≤ 5.5 V | – | – | 48 | MHz | 90/10% V _{IO} |

Note: Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

6.2.2 XRES

Table 6 XRES DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|---------------------|----------------------|---|------------------------|-----|------------------------|------|----------------------|
| SID77 | V _{IH} | Input voltage high threshold | 0.7 × V _{DDD} | – | – | V | CMOS Input |
| SID78 | V _{IL} | Input voltage low threshold | – | – | 0.3 × V _{DDD} | V | CMOS Input |
| SID79 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID80 | C _{IN} | Input capacitance | – | 3 | – | pF | – |
| SID81 ¹⁾ | V _{HYSXRES} | Input voltage hysteresis | – | 100 | – | mV | – |
| SID82 ¹⁾ | I _{DIODE} | Current through protection diode to V _{DDD} /V _{SS} | – | – | 100 | μA | – |

1) Guaranteed by characterization.

Table 7 XRES AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|---------------------|-------------------------|-------------------|-----|-----|-----|------|----------------------|
| SID83 ¹⁾ | T _{RESETWIDTH} | Reset pulse width | 1 | – | – | µs | – |

1) Guaranteed by characterization.

6.3 Analog peripherals

6.3.1 Opamp

Table 8 Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------|--------------------------|--|-----|------|------|------|---------------------|
| – | I _{DD} | Opamp block current. No load | – | – | – | – | – |
| SID269 | I _{DD_HI} | Power = high | – | 1100 | 1850 | µA | – |
| SID270 | I _{DD_MED} | Power = medium | – | 550 | 950 | µA | – |
| SID271 | I _{DD_LOW} | Power = low | – | 150 | 350 | µA | – |
| – | GBW | Load = 20 pF, 0.1 mA. V _{DDA} = 2.7 V | – | – | – | – | – |
| SID272 | GBW_HI | Power = high | 6 | – | – | MHz | – |
| SID273 | GBW_MED | Power = medium | 4 | – | – | MHz | – |
| SID274 | GBW_LO | Power = low | – | 1 | – | MHz | – |
| – | I _{OUT_MAX} | V _{DDA} ≥ 2.7 V, 500 mV from rail | – | – | – | – | – |
| SID275 | I _{OUT_MAX_HI} | Power = high | 10 | – | – | mA | – |
| SID276 | I _{OUT_MAX_MID} | Power = medium | 10 | – | – | mA | – |
| SID277 | I _{OUT_MAX_LO} | Power = low | – | 5 | – | mA | – |
| – | I _{OUT} | V _{DDA} = 1.71 V, 500 mV from rail | – | – | – | – | – |
| SID278 | I _{OUT_MAX_HI} | Power = high | 4 | – | – | mA | – |

(table continues...)

Table 8 (continued) Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------|--------------------------|--|-------|------|------------------------|-------|--|
| SID279 | I _{OUT_MAX_MID} | Power = medium | 4 | – | – | mA | – |
| SID280 | I _{OUT_MAX_LO} | Power = low | – | 2 | – | mA | – |
| SID281 | V _{IN} | Input voltage range | –0.05 | – | V _{DDA} – 0.2 | V | Charge-pump on, V _{DDA} ≥ 2.7 V |
| SID282 | V _{CM} | Input common mode voltage | –0.05 | – | V _{DDA} – 0.2 | V | Charge-pump on, V _{DDA} ≥ 2.7 V |
| – | V _{OUT} | V _{DDA} ≥ 2.7 V | – | – | – | | – |
| SID283 | V _{OUT_1} | Power = high, I _{load} = 10 mA | 0.5 | – | V _{DDA} – 0.5 | V | – |
| SID284 | V _{OUT_2} | Power = high, I _{load} = 1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID285 | V _{OUT_3} | Power = medium, I _{load} = 1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID286 | V _{OUT_4} | Power = low, I _{load} = 0.1 mA | 0.2 | – | V _{DDA} – 0.2 | V | – |
| SID288 | V _{OS_TR} | Offset voltage, trimmed | 1 | ±0.5 | 1 | mV | High mode |
| SID288A | V _{OS_TR} | Offset voltage, trimmed | – | ±1 | – | mV | Medium mode |
| SID288B | V _{OS_TR} | Offset voltage, trimmed | – | ±2 | – | mV | Low mode |
| SID290 | V _{OS_DR_TR} | Offset voltage drift, trimmed | –10 | ±3 | 10 | µV/°C | High mode. T _A ≤ 85°C. |
| SID290Q | V _{OS_DR_TR} | Offset voltage drift, trimmed | 15 | ±3 | 15 | µV/°C | High mode. T _A ≤ 105°C |

(table continues...)

Table 8 (continued) Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------|-----------------------|---|-----|-----|-----|---------|-------------------------|
| SID290A | V _{OS_DR_TR} | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Medium mode |
| SID290B | V _{OS_DR_TR} | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Low mode |
| SID291 | CMRR | DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to V _{DDA} - 0.5 V. | 60 | 70 | – | dB | V _{DD} = 3.6 V |
| SID292 | PSRR | At 1 kHz, 100-mV ripple | 70 | 85 | – | dB | V _{DD} = 3.6 V |
| – | Noise | | – | – | – | – | – |
| SID293 | V _{N1} | Input referred, 1 Hz - 1 GHz, power = high | – | 94 | – | µVrms | – |
| SID294 | V _{N2} | Input referred, 1 kHz, power = high | – | 72 | – | nV/rtHz | – |
| SID295 | V _{N3} | Input referred, 10 kHz, power = high | – | 28 | – | nV/rtHz | – |
| SID296 | V _{N4} | Input referred, 100 kHz, power = high | – | 15 | – | nV/rtHz | – |

(table continues...)

Table 8 (continued) Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|------------------|--|-----|------|-----|------------|--|
| SID297 | Cload | Stable up to maximum load. Performance specs at 50 pF | – | – | 125 | pF | – |
| SID298 | Slew_rate | Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7 V$ | 6 | – | – | V/ μ s | – |
| SID299 | T_op_wake | From disable to enable, no external RC dominating | – | 25 | – | μ s | – |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | – |
| – | Comp_mode | Comparator mode; 50 mV drive, Trise = Tfall (approx.) | – | – | – | | – |
| SID300 | T _{PD1} | Response time; power = high | – | 150 | – | ns | – |
| SID301 | T _{PD2} | Response time; power = medium | – | 400 | – | ns | – |
| SID302 | T _{PD3} | Response time; power = low | – | 2000 | – | ns | – |
| SID303 | Vhyst_op | Hysteresis | – | 10 | – | mV | – |
| Deep Sleep Mode | | Mode 2 is lowest current range. Mode 1 has higher GBW. | | | | | Deep Sleep mode. $V_{DDA} \geq 2.7 V$ |
| SID_DS_1 | IDD_HI_M1 | Mode 1, High current | – | 1400 | – | μ A | 25°C |

(table continues...)

Table 8 (continued) Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-----------|------------|------------------------|-----|-----|-----|------|---|
| SID_DS_2 | IDD_MED_M1 | Mode 1, Medium current | – | 700 | – | uA | 25°C |
| SID_DS_3 | IDD_LOW_M1 | Mode 1, Low current | – | 200 | – | uA | 25°C |
| SID_DS_4 | IDD_HI_M2 | Mode 2, High current | – | 120 | – | uA | 25°C |
| SID_DS_5 | IDD_MED_M2 | Mode 2, Medium current | – | 60 | – | uA | 25°C |
| SID_DS_6 | IDD_LOW_M2 | Mode 2, Low current | – | 15 | – | uA | 25°C |
| SID_DS_7 | GBW_HI_M1 | Mode 1, High current | – | 4 | – | MHz | 25°C |
| SID_DS_8 | GBW_MED_M1 | Mode 1, Medium current | – | 2 | – | MHz | 25°C |
| SID_DS_9 | GBW_LOW_M1 | Mode 1, Low current | – | 0.5 | – | MHz | 25°C |
| SID_DS_10 | GBW_HI_M2 | Mode 2, High current | – | 0.5 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| SID_DS_11 | GBW_MED_M2 | Mode 2, Medium current | – | 0.2 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| SID_DS_12 | GBW_LOW_M2 | Mode 2, Low current | – | 0.1 | – | MHz | 20-pF load, no DC load 0.2 V to $V_{DDA}-1.5$ V |
| SID_DS_13 | VOS_HI_M1 | Mode 1, High current | – | 5 | – | mV | With trim 25°C, 0.2 V to $V_{DDA}-1.5$ V |
| SID_DS_14 | VOS_MED_M1 | Mode 1, Medium current | – | 5 | – | mV | With trim 25°C, 0.2 V to $V_{DDA}-1.5$ V |
| SID_DS_15 | VOS_LOW_M1 | Mode 1, Low current | – | 5 | – | mV | With trim 25°C, 0.2 V to $V_{DDA}-1.5$ V |

(table continues...)

Table 8 (continued) Opamp specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-----------|-------------|------------------------|-----|-----|-----|------|--|
| SID_DS_16 | VOS_HI_M2 | Mode 2, High current | – | 5 | – | mV | With trim 25°C, 0.2 V to V _{DDA} -1.5 V |
| SID_DS_17 | VOS_MED_M2 | Mode 2, Medium current | – | 5 | – | mV | With trim 25°C, 0.2 V to V _{DDA} -1.5 V |
| SID_DS_18 | VOS_LOW_M2 | Mode 2, Low current | – | 5 | – | mV | With trim 25°C, 0.2 V to V _{DDA} -1.5 V |
| SID_DS_19 | IOUT_HI_M1 | Mode 1, High current | – | 10 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_20 | IOUT_MED_M1 | Mode 1, Medium current | – | 10 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_21 | IOUT_LOW_M1 | Mode 1, Low current | – | 4 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_22 | IOUT_HI_M2 | Mode 2, High current | – | 1 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_23 | IOUT_MED_M2 | Mode 2, Medium current | – | 1 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |
| SID_DS_24 | IOUT_LOW_M2 | Mode 2, Low current | – | 0.5 | – | mA | Output is 0.5 V to V _{DDA} -0.5 V |

6.3.2 Comparator

Table 9 Comparator DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|----------------------|---|-----|-----|-----|------|-------------------------|
| SID85 | V _{OFFSET2} | Input offset voltage, Common Mode voltage range from 0 to V _{DD} -1 | – | – | ±4 | mV | – |
| SID85A | V _{OFFSET3} | Input offset voltage. Ultra low-power mode (V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C) | – | ±12 | – | mV | – |

(table continues...)

Table 9 (continued) Comparator DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|-------------------|--|-----|-----|-------------------------|------|--------------------------|
| SID86 ¹⁾ | V _{HYST} | Hysteresis when enabled, Common Mode voltage range from 0 to V _{DD} -1 | – | 10 | 35 | mV | – |
| SID87 | V _{ICM1} | Input common mode voltage in normal mode | 0 | – | V _{DDD} – 0.1 | V | Modes 1 and 2 |
| SID247 | V _{ICM2} | Input common mode voltage in low power mode (V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C) | 0 | – | V _{DDD} | V | – |
| SID247A | V _{ICM3} | Input common mode voltage in ultra low power mode | 0 | – | V _{DDD} – 1.15 | V | – |
| SID88 ¹⁾ | CMRR | Common mode rejection ratio | 50 | – | – | dB | V _{DDD} ≥ 2.7 V |
| SID88A ¹⁾ | CMRR | Common mode rejection ratio | 42 | – | – | dB | V _{DDD} < 2.7 V |
| SID89 ¹⁾ | I _{CMP1} | Block current, normal mode | – | – | 400 | µA | – |
| SID248 ¹⁾ | I _{CMP2} | Block current, low power mode | – | – | 100 | µA | – |
| SID259 ¹⁾ | I _{CMP3} | Block current, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C) | – | 6 | 28 | µA | – |
| SID90 ¹⁾ | Z _{CMP} | DC input impedance of comparator | 35 | – | – | MΩ | – |

1) Guaranteed by characterization.

Table 10 Comparator AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|--------------------|--|-----|-----|-----|------|----------------------|
| SID91 | T _{RESP1} | Response time, normal mode | – | – | 110 | ns | 50-mV overdrive |
| SID258 | T _{RESP2} | Response time, low power mode | – | – | 200 | ns | 50-mV overdrive |
| SID92 | T _{RESP3} | Response time, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0°C, V _{DDD} ≥ 1.8 V for Temp > 0°C) | – | – | 15 | µs | 200-mV overdrive |

6.3.3 Temperature sensor

Table 11 Temperature sensor specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|----------------------|-----------------------------|-----|-----|-----|------|----------------------|
| SID93 | T _{SENSACC} | Temperature sensor accuracy | –5 | ±1 | +5 | °C | –40°C to +85°C |

6.3.4 SAR ADC

Table 12 SAR ADC DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|-----------|------------------------------------|-----------------|-----|------------------|------|------------------------------------|
| SID94 | A_RES | Resolution | - | - | 12 | bits | - |
| SID95 | A_CHNIS_S | Number of channels - single ended | - | - | 16 | | - |
| SID96 | A-CHNKS_D | Number of channels - differential | - | - | 8 | | Diff inputs use neighboring I/O |
| SID97 ¹⁾ | A-MONO | Monotonicity | Yes | | | | - |
| SID98 | A_GAINERR | Gain error | - | - | ±0.1 | % | With external reference |
| SID99 | A_OFFSET | Input offset voltage | - | - | 2 | mV | Measured with 1-V V _{REF} |
| SID100 | A_ISAR | Current consumption | - | - | 1 | mA | - |
| SID101 ¹⁾ | A_VINS | Input voltage range - single ended | V _{SS} | - | V _{DDA} | V | - |
| SID102 ¹⁾ | A_VIND | Input voltage range - differential | V _{SS} | - | V _{DDA} | V | - |
| SID103 ¹⁾ | A_INRES | Input resistance | - | - | 2.2 | KΩ | - |
| SID104 ¹⁾ | A_INCAP | Input capacitance | - | - | 10 | pF | - |

1) Guaranteed by characterization.

Table 13 SAR ADC AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-----------|---|------|-----|------|------|--|
| SID106 | A_PSRR | Power supply rejection ratio | 70 | - | - | dB | - |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | - | - | dB | Measured at 1 V |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap | - | - | 1 | MspS | - |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap. Reference = V _{DD} | - | - | 1 | MspS | - |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference | - | - | 100 | KspS | - |
| SID109 | A_SNDR | Signal-to-noise and distortion ratio (SINAD) | 66 | - | - | dB | F _{IN} = 10 kHz |
| SID111 | A_INL | Integral non linearity | -1.4 | - | +1.4 | LSB | V _{DD} = 1.71 to 5.5, 1 MspS, V _{ref} = 1 to 5.5 |

(table continues...)

Table 13 (continued) SAR ADC AC specifications

(Guaranteed by characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-----------|----------------------------|------|-----|-------|------|---|
| SID111A | A_INL | Integral non linearity | -1.4 | - | +1.4 | LSB | $V_{DD} = 1.71$ to 3.6 , 1 Msps, $V_{ref} = 1.71$ to V_{DD} |
| SID111B | A_INL | Integral non linearity | -1.4 | - | +1.4 | LSB | $V_{DD} = 1.71$ to 5.5 , 500 ksps, $V_{ref} = 1$ to 5.5 |
| SID112 | A_DNL | Differential non linearity | -0.9 | - | +1.35 | LSB | $V_{DD} = 1.71$ to 5.5 , 1 Msps, $V_{ref} = 1$ to 5.5 |
| SID112A | A_DNL | Differential non linearity | -0.9 | - | +1.35 | LSB | $V_{DD} = 1.71$ to 3.6 , 1 Msps, $V_{ref} = 1.71$ to V_{DD} |
| SID112B | A_DNL | Differential non linearity | -0.9 | - | +1.35 | LSB | $V_{DD} = 1.71$ to 5.5 , 500 ksps, $V_{ref} = 1$ to 5.5 |
| SID113 | A_THD | Total harmonic distortion | - | - | -65 | dB | $F_{IN} = 10$ kHz. |

6.3.5 CSD

Table 14 CSD block specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|--------------------------|------------|--|------|-------|-----|-------|--|
| CSD specification | | | | | | | |
| SID308 | VCSD | Voltage range of operation | 1.71 | - | 5.5 | V | - |
| SID309 | IDAC1 | DNL for 8-bit resolution | -1 | - | 1 | LSB | - |
| SID310 | IDAC1 | INL for 8-bit resolution | -3 | - | 3 | LSB | - |
| SID311 | IDAC2 | DNL for 7-bit resolution | -1 | - | 1 | LSB | - |
| SID312 | IDAC2 | INL for 7-bit resolution | -3 | - | 3 | LSB | - |
| SID313 ¹⁾ | SNR | Ratio of counts of finger to noise | 5 | - | - | Ratio | Capacitance range of 9 to 35 pF, 0.1- pF sensitivity |
| SID314 | IDAC1_CRT1 | Output current of Idac1 (8-bits) in High range | - | 612 | - | μA | - |
| SID314A | IDAC1_CRT2 | Output current of Idac1 (8-bits) in Low range | - | 306 | - | μA | - |
| SID315 | IDAC2_CRT1 | Output current of Idac2 (7-bits) in High range | - | 304.8 | - | μA | - |

(table continues...)

Table 14 (continued) CSD block specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------|---|-----|-------|-----|------|----------------------|
| SID315A | IDAC2_CRT2 | Output current of Idac2 (7-bits) in Low range | – | 152.4 | – | µA | – |

1) Guaranteed by characterization.

6.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

6.4.1 Timer/Counter/PWM

Table 15 TCPWM specifications

(Guaranteed by characterization.)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|--------------|-----------|--|------|-----|-----|------|--|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | – | – | 155 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | – | – | 650 | µA | All modes (Timer/Counter/PWM) |
| SID.TCPWM.3 | TCPWMFREQ | Operating frequency | – | – | Fc | MHz | Fc max = Fcpu. Maximum = 24 MHz |
| SID.TCPWM.4 | TPWMENEXT | Input Trigger Pulse Width for all Trigger Events | 2/Fc | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. |
| SID.TCPWM.5 | TPWMEXT | Output Trigger Pulse widths | 2/Fc | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | TCRES | Resolution of Counter | 1/Fc | – | – | ns | Minimum time between successive counts |

(table continues...)

Table 15 (continued) TCPWM specifications

(Guaranteed by characterization.)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|--------------|-----------|------------------------------|------|-----|-----|------|--|
| SID.TCPWM.5B | PWMRES | PWM Resolution | 1/Fc | – | – | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | QRES | Quadrature inputs resolution | 1/Fc | – | – | ns | Minimum pulse width between Quadrature phase inputs. |

6.4.2 I2C

Table 16 Fixed I²C DC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------|---|-----|-----|-----|------|----------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 50 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | μA | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | μA | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | μA | – |

Table 17 Fixed I²C AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------|-------------|-----|-----|-----|------|----------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | – |

6.4.3 LCD direct drive

Table 18 LCD direct drive DC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|----------------|--|-----|-----|------|---------|-------------------------------------|
| SID154 | I_{LCDLOW} | Operating current in low power mode | – | 5 | – | μA | 16 × 4 small segment disp. at 50 Hz |
| SID155 ¹⁾ | C_{LCDCAP} | LCD capacitance per segment/ common driver | – | 500 | 5000 | pF | – |
| SID156 | LCD_{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | I_{LCDOP1} | PWM Mode current. 5-V bias. 24-MHz IMO | – | 0.6 | – | mA | 32 × 4 segments. 50 Hz, 25 °C |
| SID158 | I_{LCDOP2} | PWM Mode current. 3.3-V bias. 24-MHz IMO. | – | 0.5 | – | mA | 32 × 4 segments. 50 Hz, 25 °C |

1) Guaranteed by design.

Table 19 LCD direct drive AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-----------|----------------|-----|-----|-----|------|----------------------|
| SID159 | F_{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Table 20 Fixed UART DC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------|--|-----|-----|-----|---------|----------------------|
| SID160 | I_{UART1} | Block current consumption at 100 Kbps | – | – | 55 | μA | – |
| SID161 | I_{UART2} | Block current consumption at 1000 Kbps | – | – | 312 | μA | – |

Table 21 Fixed UART AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------|-------------|-----|-----|-----|------|----------------------|
| SID162 | F_{UART} | Bit rate | – | – | 1 | Mbps | – |

6.4.4 SPI specifications

Table 22 Fixed SPI DC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------|-------------------------------------|-----|-----|-----|------|----------------------|
| SID163 | I _{SPI1} | Block current consumption at 1 Mbps | – | – | 360 | μA | – |
| SID164 | I _{SPI2} | Block current consumption at 4 Mbps | – | – | 560 | μA | – |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbps | – | – | 600 | μA | – |

Table 23 Fixed SPI AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------------|---|-----|-----|-----|------|----------------------|
| SID166 | F _{SPI} | SPI operating frequency (master; 6X oversampling) | – | – | 8 | MHz | – |

Table 24 Fixed SPI Master mode AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|------------------|--|-----|-----|-----|------|----------------------|
| SID167 | T _{DMO} | MOSI valid after Sclock driving edge | – | – | 15 | ns | – |
| SID168 | T _{DSI} | MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used | 20 | – | – | ns | – |
| SID169 | T _{HMO} | Previous MOSI data hold time with respect to capturing edge at Slave | 0 | – | – | ns | – |

Table 25 Fixed SPI Slave mode AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|----------------------|---|-----|-----|-------------------|------|----------------------|
| SID170 | T _{DMI} | MOSI valid before Sclock capturing edge | 40 | – | – | ns | – |
| SID171 | T _{DSO} | MISO valid after Sclock driving edge | – | – | 42 + 3 × (1/FCPU) | ns | – |
| SID171A | T _{DSO_ext} | MISO valid after Sclock driving edge in Ext. Clock mode | – | – | 48 | ns | – |
| SID172 | T _{HSO} | Previous MISO data hold time | 0 | – | – | ns | – |
| SID172A | T _{SSELSCK} | SSEL Valid to first SCK Valid edge | 100 | – | – | ns | – |

6.5 Memory

Table 26 Flash DC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-----------------|---------------------------|------|-----|-----|------|----------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | – |

Table 27 Flash AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|-----------------------|--------------------------|--|-------|-----|-----|---------|-------------------------|
| SID174 | T _{ROWWRITE} | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | T _{ROWERASE} | Row erase time | – | – | 13 | ms | – |
| SID176 | T _{ROWPROGRAM} | Row program time after erase | – | – | 7 | ms | – |
| SID178 | T _{BULKERASE} | Bulk erase time (128 KB) | – | – | 35 | ms | – |
| SID179 | T _{SECTORERASE} | Sector erase time (8 KB) | – | – | 15 | ms | – |
| SID180 ¹⁾ | T _{DEVPROG} | Total device program time | – | – | 15 | seconds | – |
| SID181 ¹⁾ | F _{END} | Flash endurance | 100 K | – | – | cycles | – |
| SID182 ¹⁾ | F _{RET} | Flash retention. T _A ≤ 55°C, 100 K P/E cycles | 20 | – | – | years | – |
| SID182A ¹⁾ | – | Flash retention. T _A ≤ 85°C, 10 K P/E cycles | 10 | – | – | years | – |
| SID182B ¹⁾ | F _{RETQ} | Flash retention. T _A ≤ 105°C, 10 K P/E cycles, ≤ three years at T _A ≥ 85°C | 10 | 20 | – | years | – |

1) Guaranteed by characterization.

6.6 System resources

6.6.1 Power-on reset (POR) with Brown Out

Table 28 Imprecise Power-on reset (PRES)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|-----------------------|----------------------|------|-----|------|------|----------------------|
| SID185 ¹⁾ | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.45 | V | – |
| SID186 ¹⁾ | V _{FALLIPOR} | Falling trip voltage | 0.75 | – | 1.4 | V | – |
| SID187 ¹⁾ | V _{IPORHYST} | Hysteresis | 15 | – | 200 | mV | – |

1) Guaranteed by characterization.

Table 29 Precise Power-on reset (POR)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|------------------------|--|------|-----|-----|------|----------------------|
| SID190 ¹⁾ | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.64 | – | – | V | – |
| SID192 ¹⁾ | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.4 | – | – | V | – |

1) Guaranteed by characterization.

6.6.2 Voltage monitors

Table 30 Voltage monitors DC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|--------------------|--------------------------|------|------|------|------|----------------------|
| SID195 | V _{LVI1} | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V | – |
| SID196 | V _{LVI2} | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | V | – |
| SID197 | V _{LVI3} | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | V | – |
| SID198 | V _{LVI4} | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | V | – |
| SID199 | V _{LVI5} | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | V | – |
| SID200 | V _{LVI6} | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | V | – |
| SID201 | V _{LVI7} | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | V | – |
| SID202 | V _{LVI8} | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | V | – |
| SID203 | V _{LVI9} | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | V | – |
| SID204 | V _{LVI10} | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | V | – |
| SID205 | V _{LVI11} | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | V | – |
| SID206 | V _{LVI12} | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | V | – |
| SID207 | V _{LVI13} | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | V | – |
| SID208 | V _{LVI14} | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | V | – |
| SID209 | V _{LVI15} | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | V | – |
| SID210 | V _{LVI16} | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | V | – |
| SID211 ¹⁾ | LVI_IDD | Block current | – | – | 100 | µA | – |

1) Guaranteed by characterization.

Table 31 Voltage monitors AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|----------------------|---------------------------|-----|-----|-----|------|----------------------|
| SID212 ¹⁾ | T _{MONTRIP} | Voltage monitor trip time | – | – | 1 | µs | – |

1) Guaranteed by characterization.

6.6.3 SWD interface

Table 32 SWD interface specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|-----------------------|--------------|---|----------------|-----|---------------|------|---------------------------------------|
| SID213 | F_SWCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID215 ¹⁾ | T_SWDI_SETUP | $T = 1/f\text{ SWDCLK}$ | $0.25 \cdot T$ | – | – | ns | – |
| SID216 ¹⁾ | T_SWDI_HOLD | $T = 1/f\text{ SWDCLK}$ | $0.25 \cdot T$ | – | – | ns | – |
| SID217 ¹⁾ | T_SWDO_VALID | $T = 1/f\text{ SWDCLK}$ | – | – | $0.5 \cdot T$ | ns | – |
| SID217A ¹⁾ | T_SWDO_HOLD | $T = 1/f\text{ SWDCLK}$ | 1 | – | – | ns | – |

1) Guaranteed by characterization.

6.6.4 Internal main oscillator

Table 33 IMO DC specifications

(Guaranteed by design.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------|---------------------------------|-----|-----|------|------|----------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | – | – | 1000 | μA | – |
| SID219 | I _{IMO2} | IMO operating current at 24 MHz | – | – | 325 | μA | – |
| SID220 | I _{IMO3} | IMO operating current at 12 MHz | – | – | 225 | μA | – |
| SID221 | I _{IMO4} | IMO operating current at 6 MHz | – | – | 180 | μA | – |
| SID222 | I _{IMO5} | IMO operating current at 3 MHz | – | – | 150 | μA | – |

Table 34 IMO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------------|--------------------------------------|-----|-----|-----|------|--|
| SID223 | F _{IMOTOL1} | Frequency variation from 3 to 48 MHz | – | – | ±2 | % | ±3% if T _A > 85 °C and IMO frequency < 24 MHz |
| SID226 | T _{STARTIMO} | IMO startup time | – | – | 12 | μs | – |
| SID227 | T _{JITRMSIMO1} | RMS Jitter at 3 MHz | – | 156 | – | ps | – |

(table continues...)

Table 34 (continued) IMO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------------|----------------------|-----|-----|-----|------|----------------------|
| SID228 | T _{JITRMSIM02} | RMS Jitter at 24 MHz | – | 145 | – | ps | – |
| SID229 | T _{JITRMSIM03} | RMS Jitter at 48 MHz | – | 139 | – | ps | – |

6.6.5 Internal low-speed oscillator

Table 35 ILO DC specifications

(Guaranteed by design.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|----------------------|---------------------------------|-----|-----|------|------|----------------------|
| SID231 ¹⁾ | I _{ILO1} | ILO operating current at 32 kHz | – | 0.3 | 1.05 | μA | – |
| SID233 ²⁾ | I _{ILOLEAK} | ILO leakage current | – | 2 | 15 | nA | – |

1) Guaranteed by characterization.

2) Guaranteed by design.

Table 36 ILO AC specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|------------------------|--------------------------|-----|-----|-----|------|---|
| SID234 ¹⁾ | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | – |
| SID236 ¹⁾ | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | F _{ILOTRIM1} | 32 kHz trimmed frequency | 15 | 32 | 50 | kHz | Max ILO frequency is 70 kHz if T _A > 85 °C |

1) Guaranteed by characterization.

Table 37 External clock specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|------------|---|-----|-----|-----|------|----------------------|
| SID305 ¹⁾ | ExtClkFreq | External Clock input Frequency | 0 | – | 48 | MHz | – |
| SID306 ¹⁾ | ExtClkDuty | Duty cycle; Measured at V _{DD/2} | 45 | – | 55 | % | – |

1) Guaranteed by characterization.

Table 38 Watch crystal oscillator (WCO) specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|------------------------------------|---------------------|--|------|-----|-----|------|--------------------------------|
| IMO WCO-PLL calibrated mode | | | | | | | |
| SID330 | IMO _{WCO1} | Frequency variation with IMO set to 3 MHz | -0.6 | - | 0.6 | % | Does not include WCO tolerance |
| SID331 | IMO _{WCO2} | Frequency variation with IMO set to 5 MHz | -0.4 | - | 0.4 | % | Does not include WCO tolerance |
| SID332 | IMO _{WCO3} | Frequency variation with IMO set to 7 MHz or 9 MHz | -0.3 | - | 0.3 | % | Does not include WCO tolerance |
| SID333 | IMO _{WCO4} | All other IMO frequency settings | -0.2 | - | 0.2 | % | Does not include WCO tolerance |

WCO specifications

| | | | | | | | |
|--------|--------------------|-------------------------------------|---|--------|------|-----|----------------------|
| SID398 | F _{WCO} | Crystal frequency | - | 32.768 | - | kHz | - |
| SID399 | F _{TOL} | Frequency tolerance | - | 50 | 250 | ppm | With 20-ppm crystal. |
| SID400 | ESR | Equivalent series resistance | - | 50 | - | kΩ | - |
| SID401 | PD | Drive level | - | - | 1 | μW | - |
| SID402 | T _{START} | Startup time | - | - | 500 | ms | - |
| SID403 | C _L | Crystal load capacitance | 6 | - | 12.5 | pF | - |
| SID404 | C ₀ | Crystal shunt capacitance | - | 1.35 | - | pF | - |
| SID405 | I _{WCO1} | Operating current (high power mode) | - | - | 8 | uA | - |

Table 39 UDB AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-----------|-------------|-----|-----|-----|------|----------------------|
|----------|-----------|-------------|-----|-----|-----|------|----------------------|

Datapath performance

| | | | | | | | |
|--------|------------------------|---|---|---|----|-----|---|
| SID249 | F _{MAX-TIMER} | Max frequency of 16-bit timer in a UDB pair | - | - | 48 | MHz | - |
| SID250 | F _{MAX-ADDER} | Max frequency of 16-bit adder in a UDB pair | - | - | 48 | MHz | - |
| SID251 | F _{MAX_CRC} | Max frequency of 16-bit CRC/PRS in a UDB pair | - | - | 48 | MHz | - |

PLD Performance in UDB

| | | | | | | | |
|--------|----------------------|--|---|---|----|-----|---|
| SID252 | F _{MAX_PLD} | Max frequency of 2-pass PLD function in a UDB pair | - | - | 48 | MHz | - |
|--------|----------------------|--|---|---|----|-----|---|

Clock to Output Performance

(table continues...)

Table 39 (continued) UDB AC specifications

(Guaranteed by characterization.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|---------------------------|---|-----|-----|-----|------|----------------------|
| SID253 | T _{CLK_OUT_UBD1} | Prop. delay for clock in to data out at 25 °C, Typ. | – | 15 | – | ns | – |
| SID254 | T _{CLK_OUT_UBD2} | Prop. delay for clock in to data out, Worst case. | – | 25 | – | ns | – |

Table 40 Block specs

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------------------|------------------------|---|-----|-----|-----|---------|--|
| SID256* | T _{WS48} * | Number of wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | T _{WS24} * | Number of wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |
| SID260 ¹⁾ | V _{REFSAR} | Trimmed internal reference to SAR | –1 | – | +1 | % | Percentage of V _{bg} (1.024 V). |
| SID261 ¹⁾ | F _{SARINTREF} | SAR operating speed without external reference bypass | – | – | 100 | ksps | 12-bit resolution. |
| SID262 ²⁾ | T _{CLKSWITCH} | Clock switching from clk1 to clk2 in clk1 periods | 3 | – | 4 | Periods | – |

* Tws48 and Tws24 are guaranteed by Design

1) Guaranteed by characterization.

2) Guaranteed by design.

Table 41 UDB port adaptor specifications

(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V_{DDIO} and V_{DD}.)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|----------|-------------------------|---------------------------------------|-----|-----|-----|------|----------------------|
| SID263 | T _{LCLKDO} | LCLK to output delay | – | – | 18 | ns | – |
| SID264 | T _{DINLCLK} | Input setup time to LCLK rising edge | – | – | 7 | ns | – |
| SID265 | T _{DINLCLKHLD} | Input hold time from LCLK rising edge | 0 | – | – | ns | – |
| SID266 | T _{LCLKHIZ} | LCLK to output tristated | – | – | 28 | ns | – |
| SID267 | T _{FLCLK} | LCLK frequency | – | – | 33 | MHz | – |
| SID268 | T _{LCLKDUTY} | LCLK duty cycle (percentage high) | 40 | – | 60 | % | – |

Table 42 **CAN specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / conditions |
|-----------------|------------------|--------------------------------|------------|------------|------------|-------------|-----------------------------|
| SID420 | IDD_CAN | Block current consumption | – | – | 200 | uA | – |
| SID421 | CAN_bits | CAN Bit rate (Min 8-MHZ clock) | – | – | 1 | Mbps | – |

7 Ordering information

The PSoC™ 4200M part numbers and features are listed in the [Table 43](#).

Table 43 PSoC™ 4200M ordering information

| Category | Product | Features | | | | | | | | | | | | | | Packages | | | | |
|----------|-------------------|---------------------|------------|-----------|-----|--------------|-----|-------------------------|------------------|----------------|----------------|--------------|------------|-----|------|----------|---------|------------------------|------------------------|--------|
| | | Max CPU speed (MHz) | Flash (KB) | SRAM (KB) | UDB | Opamp (CTBm) | CSD | IDAC (1X7-Bit, 1-8-Bit) | Direct LCD drive | 12-bit SAR ADC | LP comparators | TCPWM blocks | SCB blocks | CAN | GPIO | 44-TQFP | 48-TQFP | 64-TQFP (0.5-mm pitch) | 64-TQFP (0.8-mm pitch) | 68-QFN |
| 4245 | CY8C4245AZI-M433 | 48 | 32 | 4 | 4 | 2 | - | - | - | 1000 ksp/s | 2 | 8 | 3 | - | 38 | - | ✓ | - | - | - |
| | CY8C4245AZI-M443 | 48 | 32 | 4 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 3 | - | 38 | - | ✓ | - | - | - |
| | CY8C4245AZI-M445 | 48 | 32 | 4 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | ✓ | - | - |
| | CY8C4245LTI-M445 | 48 | 32 | 4 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4245LTI-DM405 | 48 | 32 | 4 | 4 | - | - | - | - | - | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4245AXI-M445 | 48 | 32 | 4 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | - | ✓ | - |
| 4246 | CY8C4246AXI-M443 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 2 | - | 36 | ✓ | - | - | - | - |
| | CY8C4246AZI-M443 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 3 | - | 38 | - | ✓ | - | - | - |
| | CY8C4246AZI-M445 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | ✓ | - | - |
| | CY8C4246AZI-M475 | 48 | 64 | 8 | 4 | 4 | - | 2 | - | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | ✓ | - | - |
| | CY8C4246LTI-M445 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4246LTI-M475 | 48 | 64 | 8 | 4 | 4 | - | 2 | - | 1000 ksp/s | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4246LTI-DM405 | 48 | 64 | 8 | 4 | - | - | - | - | - | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4246AXI-M445 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | - | ✓ | - |
| | CY8C4246AZQ-M443 | 48 | 64 | 8 | 4 | 2 | 1 | - | ✓ | 1000 ksp/s | 2 | 8 | 3 | - | 38 | - | ✓ | - | - | - |
| 4247 | CY8C4247LTI-M475 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | - | 1000 ksp/s | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4247AZI-M475 | 48 | 128 | 16 | 4 | 4 | - | 4 | - | 1000 ksp/s | 2 | 8 | 4 | - | 51 | - | - | ✓ | - | - |
| | CY8C4247AZI-M485 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | ✓ | 1000 ksp/s | 2 | 8 | 4 | ✓ | 51 | - | - | ✓ | - | - |
| | CY8C4247AXI-M485 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | ✓ | 1000 ksp/s | 2 | 8 | 4 | ✓ | 51 | - | - | - | ✓ | - |
| | CY8C4247LTQ-M475 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | ✓ | 1000 ksp/s | 2 | 8 | 4 | - | 55 | - | - | - | - | ✓ |
| | CY8C4247AZQ-M485 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | ✓ | 1000 ksp/s | 2 | 8 | 4 | ✓ | 51 | - | - | ✓ | - | - |
| | CY8C4247AXQ-M485 | 48 | 128 | 16 | 4 | 4 | 2 | 4 | ✓ | 1000 ksp/s | 2 | 8 | 4 | ✓ | 51 | - | - | - | ✓ | - |

The nomenclature used in the preceding table is based on the following part numbering convention:

Table 44 **MPN nomenclature**

| Field | Description | Values | Meaning |
|-------|-------------------|---------|--|
| CY8C | Infineon prefix | | |
| 4 | Architecture | 4 | PSoC™ 4 |
| A | Family | 2 | 4200 Family |
| B | CPU speed | 4 | 48 MHz |
| C | Flash capacity | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package code | AX, AZ | TQFP |
| | | LT | QFN |
| | | BU | BGA |
| | | FD | CSP |
| F | Temperature range | I | Industrial |
| | | Q | Extended Industrial |
| S | Series designator | N/A | PSoC™ 4 Base Series |
| | | L | PSoC™ 4 L-Series |
| | | BL | PSoC™ 4 BLE |
| | | M | PSoC™ 4 M-Series |
| XYZ | Attributes code | 000-999 | Code of feature set in the specific family |

7.1 Part numbering conventions

The part number fields are defined as follows.

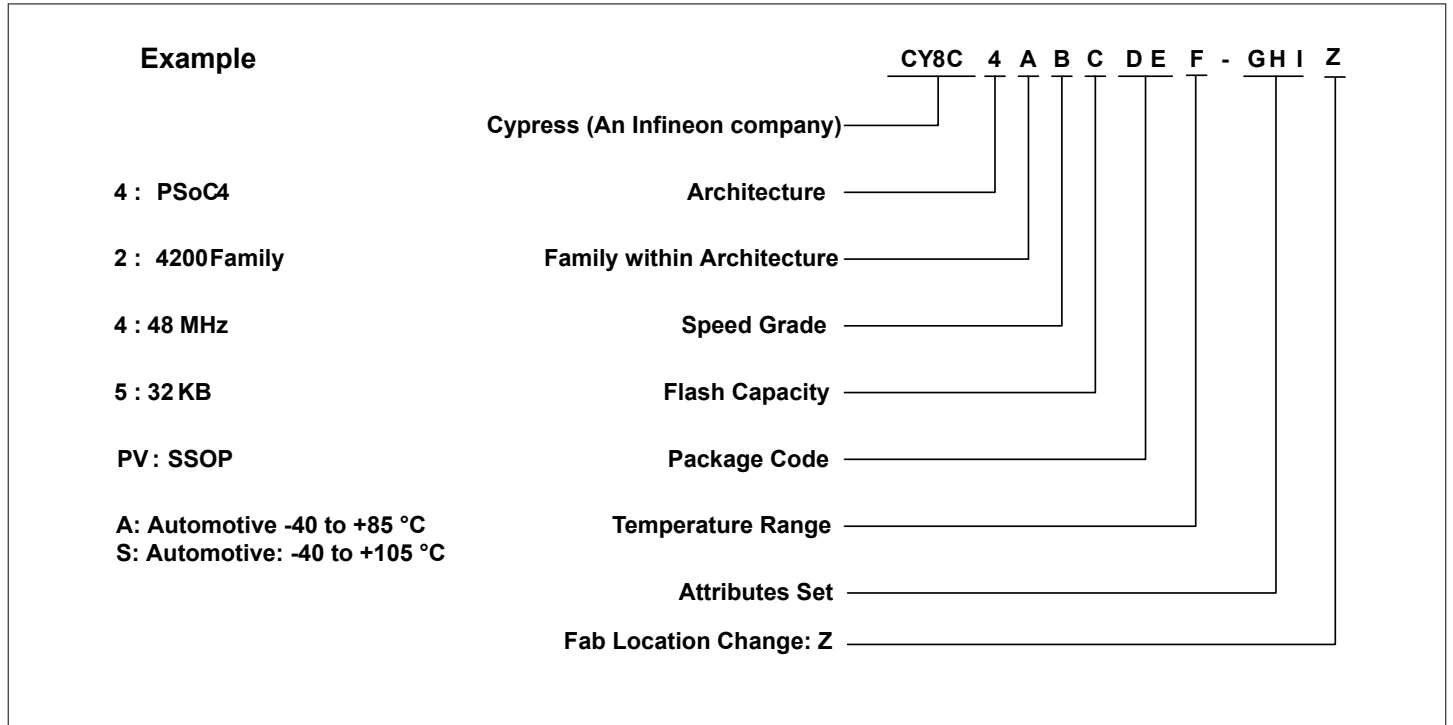


Figure 8 Part numbering conventions

8 Packaging

Table 45 Package dimensions

| Spec ID# | Package | Description | Package Dwg # |
|----------|-------------|--|---------------|
| PKG_1 | 68-pin QFN | 68-pin QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch | 001-09618 |
| PKG_2 | 64-pin TQFP | 64-pin TQFP, 10 mm x 10 mm x 1.4 mm height with 0.5 mm pitch | 51-85051 |
| PKG_4 | 64-pin TQFP | 64-pin TQFP, 14 mm x 14 mm x 1.4 mm height with 0.8 mm pitch | 51-85046 |
| PKG_5 | 48-pin TQFP | 48-pin TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch | 51-85135 |
| PKG_6 | 44-pin TQFP | 44-pin TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch | 51-85064 |

Table 46 Package characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|---|------------|-----|------|-----|---------|
| T _A | Operating ambient temperature | – | –40 | 25 | 85 | °C |
| T _J | Operating junction temperature | – | –40 | – | 100 | °C |
| T _{JA} | Package θ_{JA} (68-pin QFN) | – | – | 16.8 | – | °C/Watt |
| T _{JC} | Package θ_{JC} (68-pin QFN) | – | – | 2.9 | – | °C/Watt |
| T _{JA} | Package θ_{JA} (64-pin TQFP, 0.5 mm pitch) | – | – | 56 | – | °C/Watt |
| T _{JC} | Package θ_{JC} (64-pin TQFP, 0.5 mm pitch) | – | – | 19.5 | – | °C/Watt |
| T _{JA} | Package θ_{JA} (64-pin TQFP, 0.8 mm pitch) | – | – | 66.4 | – | °C/Watt |
| T _{JC} | Package θ_{JC} (64-pin TQFP, 0.8 mm pitch) | – | – | 18.2 | – | °C/Watt |
| T _{JA} | Package θ_{JA} (48-pin TQFP, 0.5 mm pitch) | – | – | 67.3 | – | °C/Watt |
| T _{JC} | Package θ_{JC} (48-pin TQFP, 0.5 mm pitch) | – | – | 30.4 | – | °C/Watt |
| T _{JA} | Package θ_{JA} (44-pin TQFP, 0.8 mm pitch) | – | – | 57 | – | °C/Watt |
| T _{JC} | Package θ_{JC} (44-pin TQFP, 0.8 mm pitch) | – | – | 25.9 | – | °C/Watt |

Note: All θ_{JA} and θ_{JC} values are simulated, not characterized.

Table 47 Solder reflow peak temperature

| Package | Maximum peak temperature | Maximum time at peak temperature |
|--------------|--------------------------|----------------------------------|
| All packages | 260°C | 30 seconds |

Table 48 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|--------------|-------|
| All packages | MSL 3 |

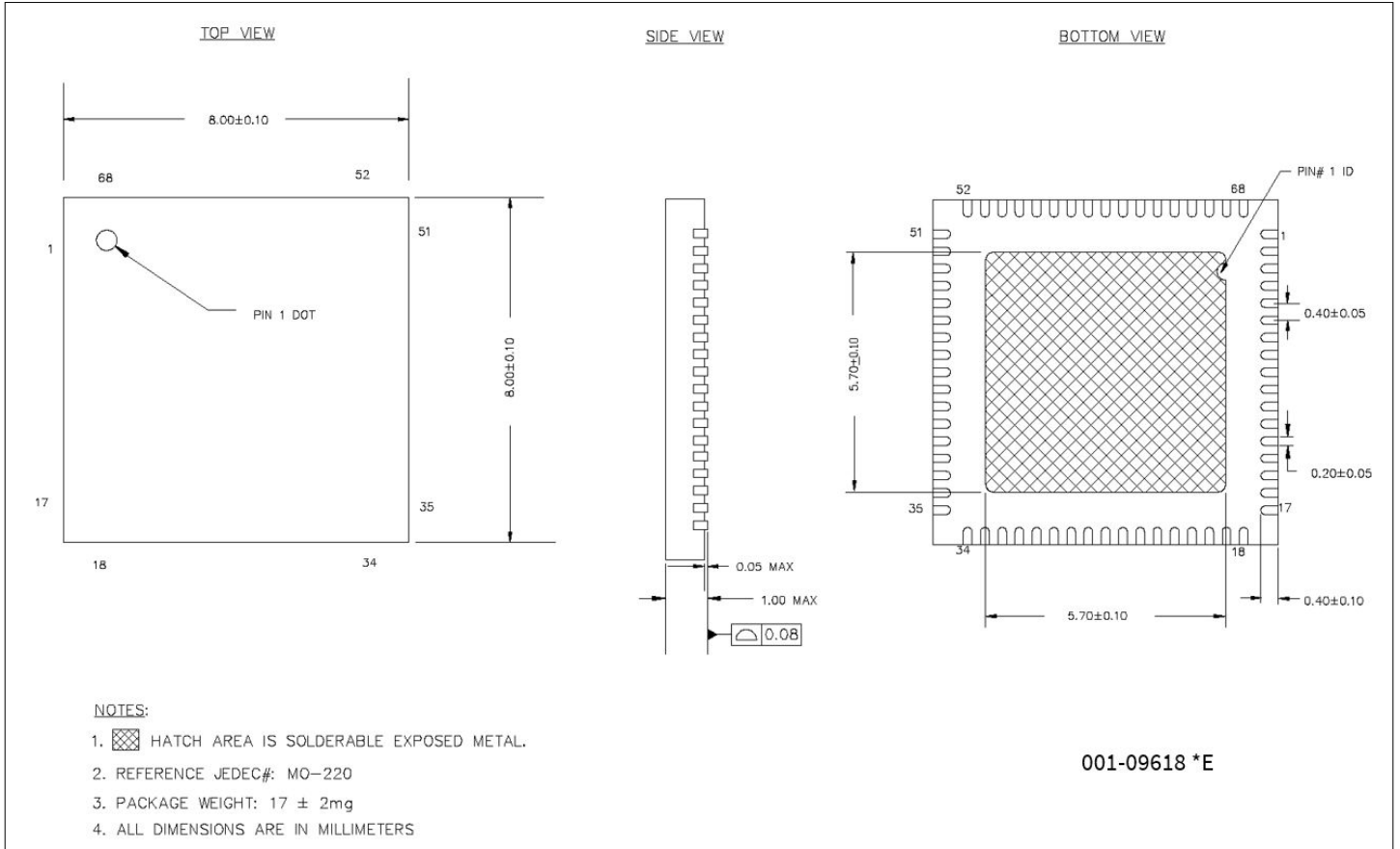


Figure 9 68-Pin QFN 8 × 8 × 1.0 mm package outline (PG-VQFN-68)

Note: The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

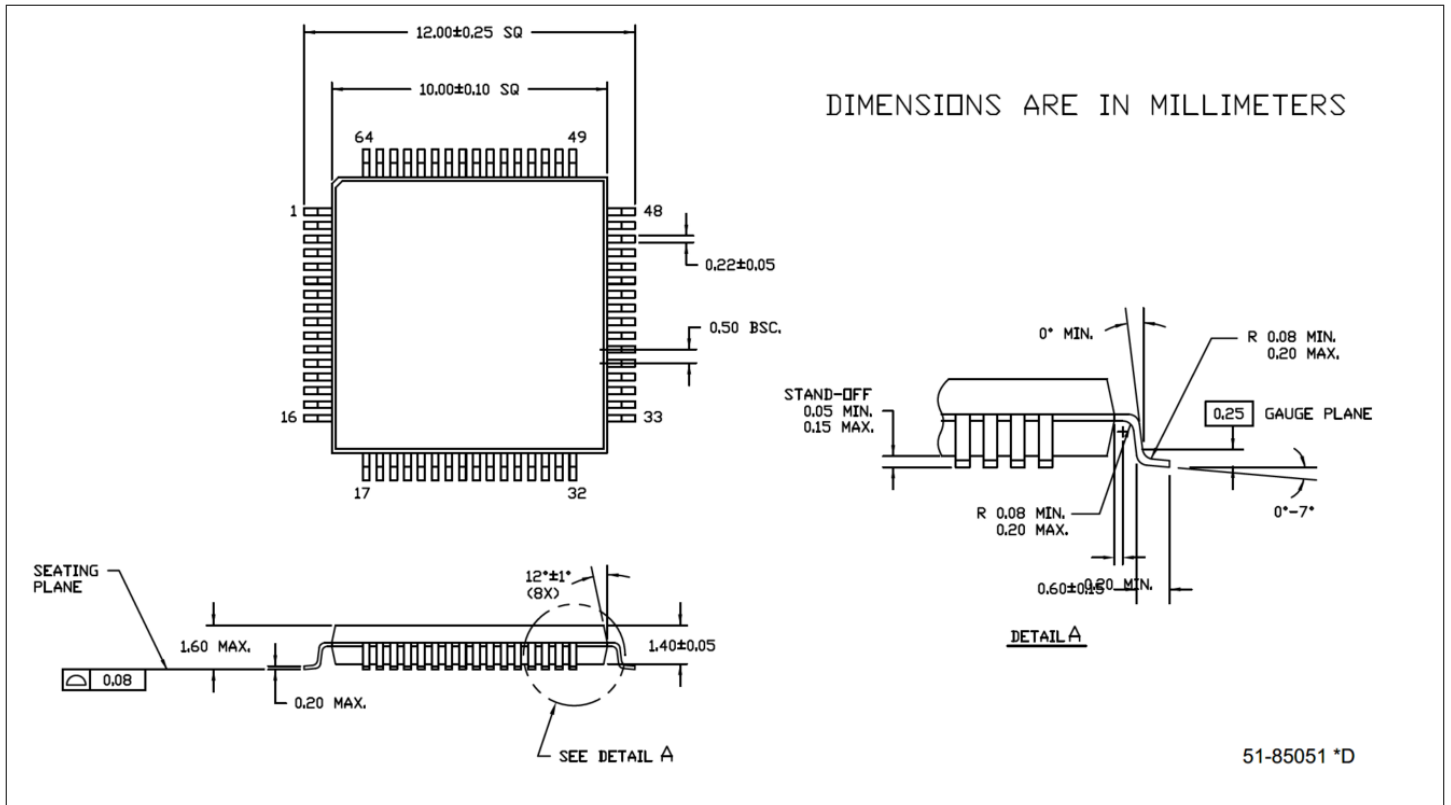


Figure 10 64-Pin TQFP 10 × 10 × 1.4 mm package outline (PG-TQFP-64)

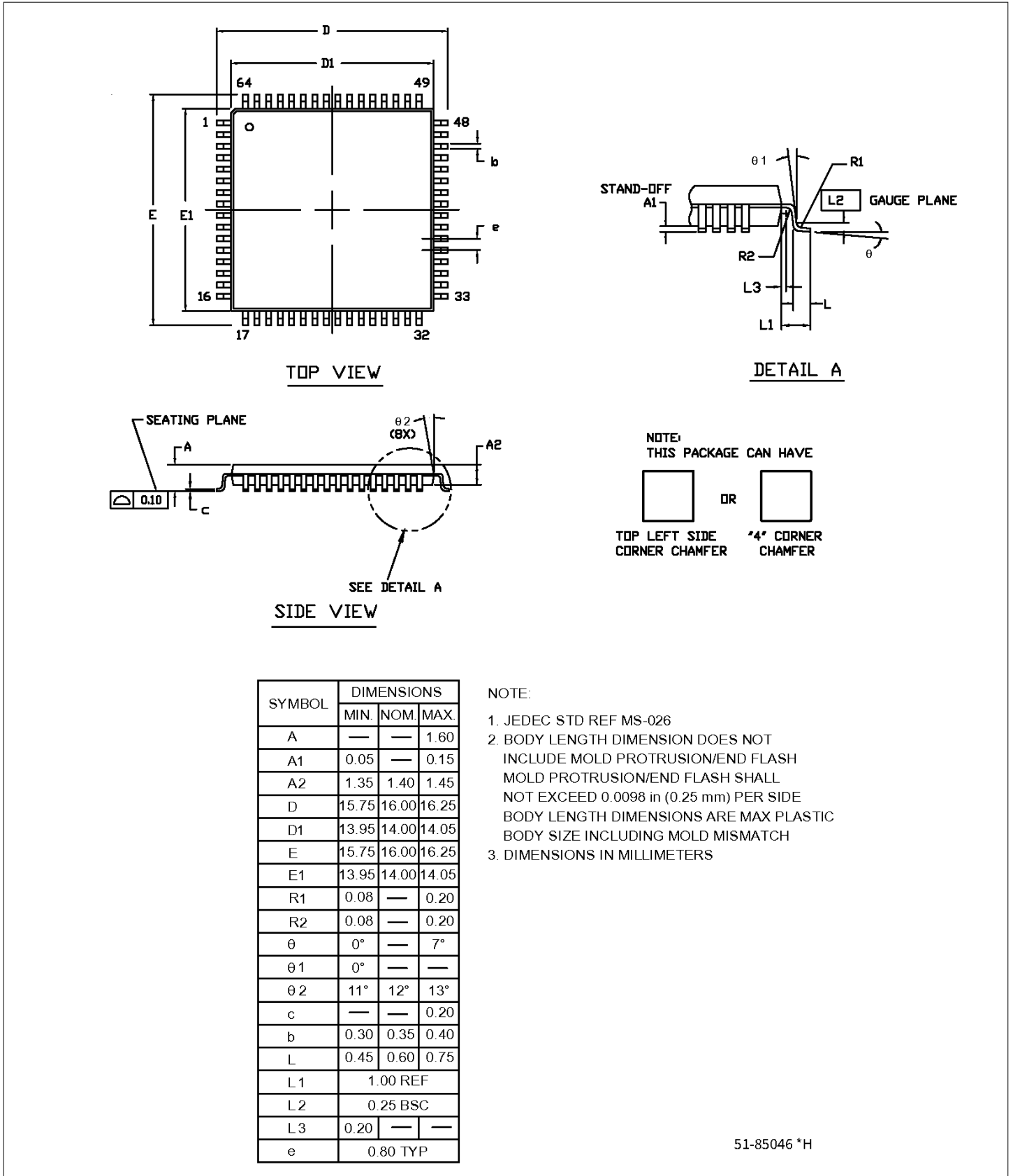


Figure 11 64-Pin 14 × 14 × 1.4 mm TQFP package outline (PG-TQFP-64)

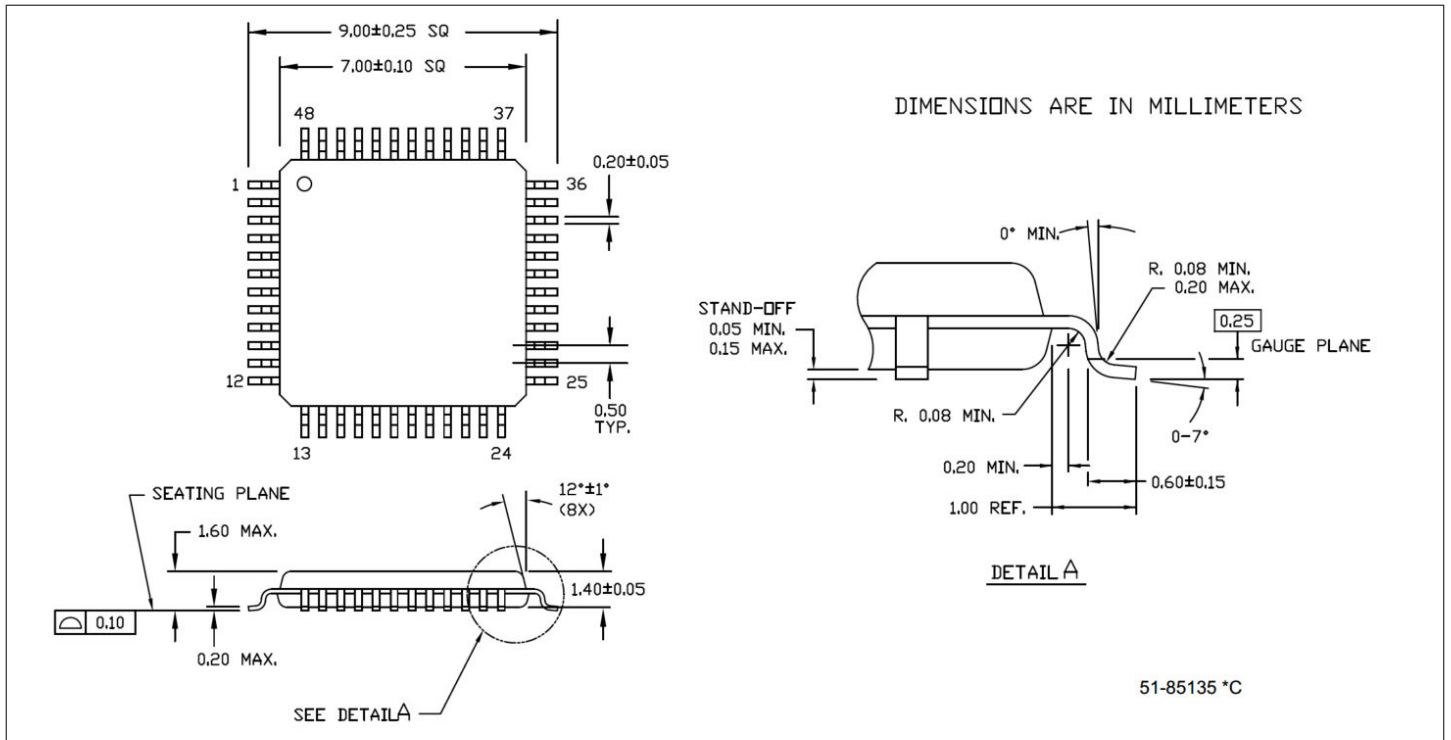


Figure 12 48-Pin 7 × 7 × 1.4 mm TQFP package outline (PG-TQFP-48)

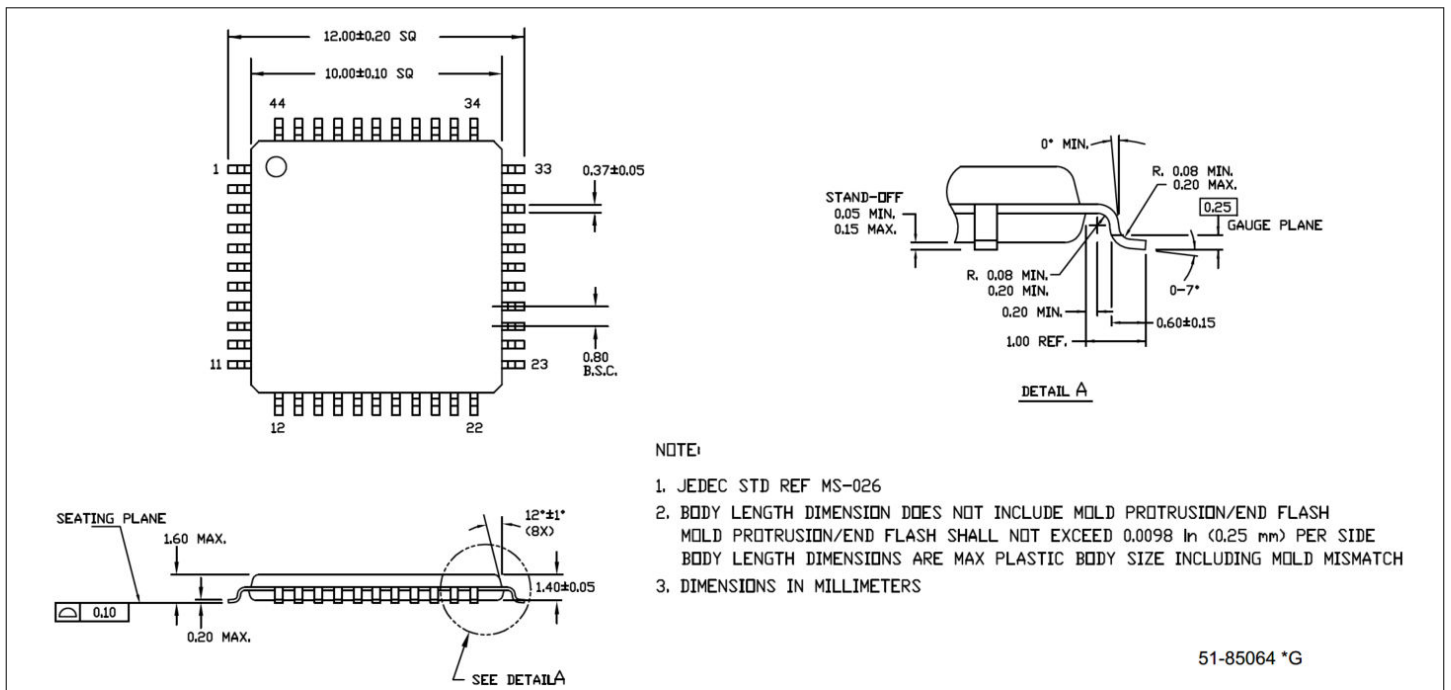


Figure 13 44-Pin 10 × 10 × 1.4 mm TQFP package outline (PG-TQFP-44)

9 Acronyms

Table 49 Acronyms used in this document

| Acronym | Description |
|---------|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |

(table continues...)

Table 49 (continued) Acronyms used in this document

| Acronym | Description |
|--------------------------|--|
| EPSR | execution program status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC™ pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |

(table continues...)

Table 49 (continued) Acronyms used in this document

| Acronym | Description |
|----------------|---|
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC™ | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I2C serial clock |
| SDA | I2C serial data |

(table continues...)

Table 49 (continued) Acronyms used in this document

| Acronym | Description |
|----------------|--|
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC™ pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

10 Document conventions

10.1 Units of measure

Table 50 Unit of measure

| Symbol | Unit of measure |
|---------------|------------------------|
| °C | degrees celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |

(table continues...)

Table 50 (continued) **Unit of measure**

| Symbol | Unit of measure |
|---------------|------------------------|
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

11 Revision history

| Document revision | Date | Description of changes |
|-------------------|------------|---|
| *B | 2015-06-03 | Release to web. |
| *C | 2015-06-29 | Removed note regarding hardware handshaking in the UART Mode section. Changed max value of SID51A to 2 ms. Added “Guaranteed by characterization” note for SID65 and SID65A Updated Ordering Information. Removed the Errata section. |
| *D | 2015-07-08 | Corrected Block Diagram |
| *E | 2015-09-30 | Updated CAPSENSE™ section. Updated the note at the end of the Pinout table. Removed Conditions for spec SID237. Updated Ordering Information. |
| *F | 2015-11-25 | Added Comparator ULP mode range restrictions and corrected typos. |
| *G | 2016-08-19 | Added extended industrial temperature range. Added specs SID290Q, SID182A, and SID299A. Updated conditions for SID290, SID223, and SID237. Added 44-pin TQFP package details. Updated Ordering Information. |
| *H | 2016-10-21 | Added back CY8C4245LTI-DM405 and CY8C4246LTI-DM405 parts. |
| *I | 2017-10-23 | Updated the Cypress logo and copyright information. Added CY8C4246AXI-M443 in Ordering Information. Updated 64-pin TQFP package diagram (spec 51-85046) to current revision. |
| *J | 2018-03-28 | Corrected MPN Table to show three SCBs for 48 TQFP packages and two SCBs for 44 TQFP package. |
| *K | 2018-04-24 | Corrected MPN Table to show three SCBs for 48 TQFP packages and two SCBs for 44 TQFP package. |
| *L | 2019-06-28 | Added CY8C4246AZQ-M443, CY8C4247AZQ-M485, and CY8C4247AXQ-M485 in Ordering Information. |
| *M | 2024-02-16 | Migrated to IFX template. Deleted DN VSSD pins from Pinout. Added Note in Packaging. Updated Development ecosystem Deleted Reference section |

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