



**THE DATASHEET OF
SN74LVU04AD**

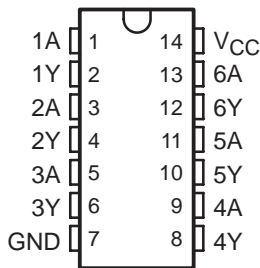


SN54LVU04A, SN74LVU04A HEX INVERTERS

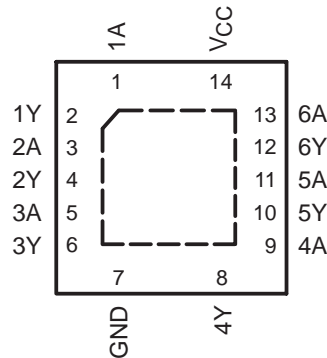
SCES130L – MARCH 1998 – REVISED DECEMBER 2004

- 2-V to 5.5-V V_{CC} Operation
- Unbuffered Outputs
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

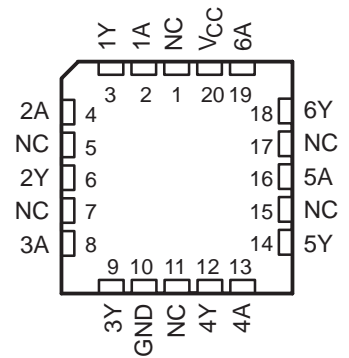
SN54LVU04A ... J OR W PACKAGE
SN74LVU04A ... D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVU04A ... RGY PACKAGE
(TOP VIEW)



SN54LVU04A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These hex inverters are designed for 2-V to 5.5-V V_{CC} operation.

The 'LVU04A devices contain six independent inverters with unbuffered outputs. These devices perform the Boolean function $Y = \bar{A}$.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVU04ARGYR	LVU04A
	SOIC – D	Tube of 50	SN74LVU04AD	LVU04A
		Reel of 2500	SN74LVU04ADR	
	SOP – NS	Reel of 2000	SN74LVU04ANSR	LVU04A
	SSOP – DB	Reel of 2000	SN74LVU04ADBR	LU04A
	TSSOP – PW	Tube of 90	SN74LVU04APW	LU04A
Reel of 2000		SN74LVU04APWR		
Reel of 250		SN74LVU04APWT		
TVSOP – DGV	Reel of 2000	SN74LVU04ADGVR	LU04A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVU04AJ	SNJ54LVU04AJ
	CFP – W	Tube of 150	SNJ54LVU04AW	SNJ54LVU04AW
	LCCC – FK	Tube of 85	SNJ54LVU04AFK	SNJ54LVU04AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

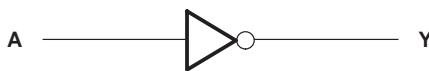
SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130L – MARCH 1998 – REVISED DECEMBER 2004

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130L – MARCH 1998 – REVISED DECEMBER 2004

recommended operating conditions (see Note 5)

		SN54LVU04A		SN74LVU04A		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	2	5.5	2	5.5	V	
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.7	1.7		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.8	V _{CC} × 0.8			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.8	V _{CC} × 0.8			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.8	V _{CC} × 0.8			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.3	0.3		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.2	V _{CC} × 0.2			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.2	V _{CC} × 0.2			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.2	V _{CC} × 0.2			
V _I	Input voltage	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 2 V		-50		-50	μA
		V _{CC} = 2.3 V to 2.7 V		-2		-2	mA
		V _{CC} = 3 V to 3.6 V		-6		-6	
		V _{CC} = 4.5 V to 5.5 V		-12		-12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	mA
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
T _A	Operating free-air temperature	-55	125	-40	85	°C	

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVU04A			SN74LVU04A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1			V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V						0.1	V
	I _{OL} = 2 mA	2.3 V						0.4	
	I _{OL} = 6 mA	3 V						0.44	
	I _{OL} = 12 mA	4.5 V						0.55	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
C _i	V _I = V _{CC} or GND	3.3 V		4			4		pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LVU04A, SN74LVU04A HEX INVERTERS

SCES130L – MARCH 1998 – REVISED DECEMBER 2004

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	3.2*	10.9*	1*	14*	1	14	ns	
			$C_L = 50\text{ pF}$	6.6	13.4	1	16	1	16		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	2.5*	8.9*	1*	10.5*	1	10.5	ns	
			$C_L = 50\text{ pF}$	4.7	11.4	1	13	1	13		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LVU04A		SN74LVU04A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	2.2*	5.5*	1*	6.5*	1	6.5	ns	
			$C_L = 50\text{ pF}$	3.9	7	1	8	1	8		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER		SN74LVU04A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

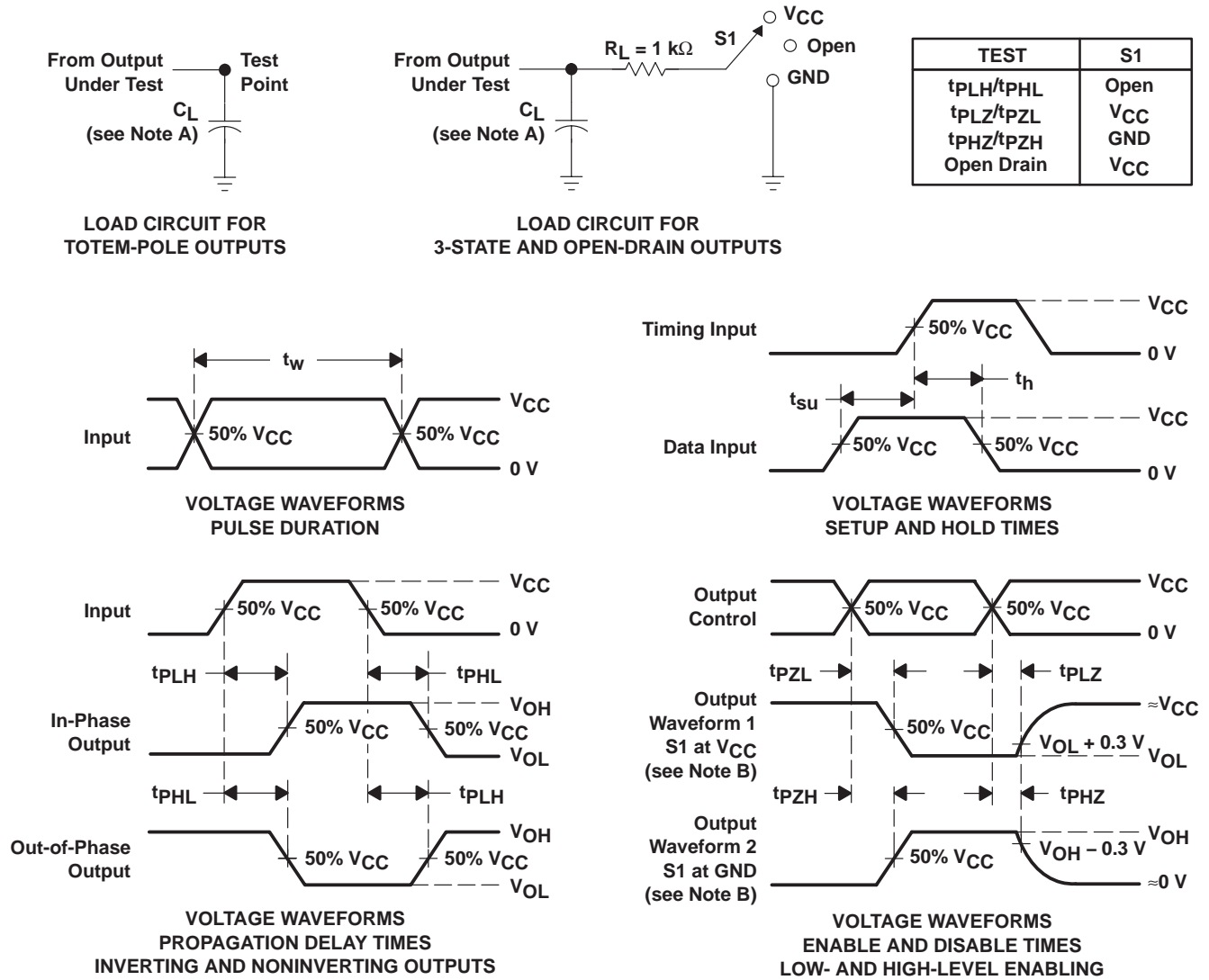
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	5.6	pF
			5 V	6.7	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVU04ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples
SN74LVU04ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVU04A	Samples
SN74LVU04ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVU04A	Samples
SN74LVU04APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples
SN74LVU04APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LU04A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

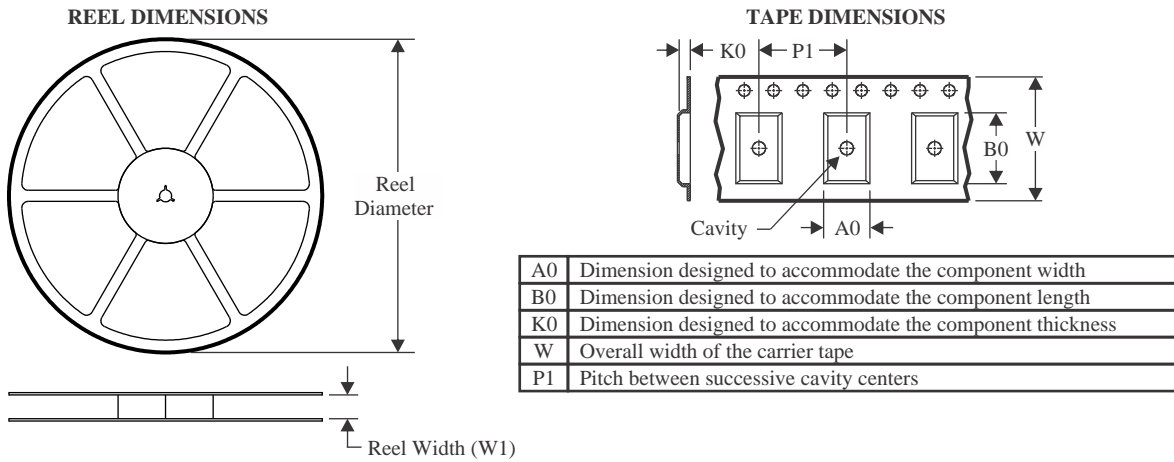
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVU04A :

- Automotive : [SN74LVU04A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVU04ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVU04ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVU04ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVU04APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVU04ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVU04ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVU04ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVU04APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

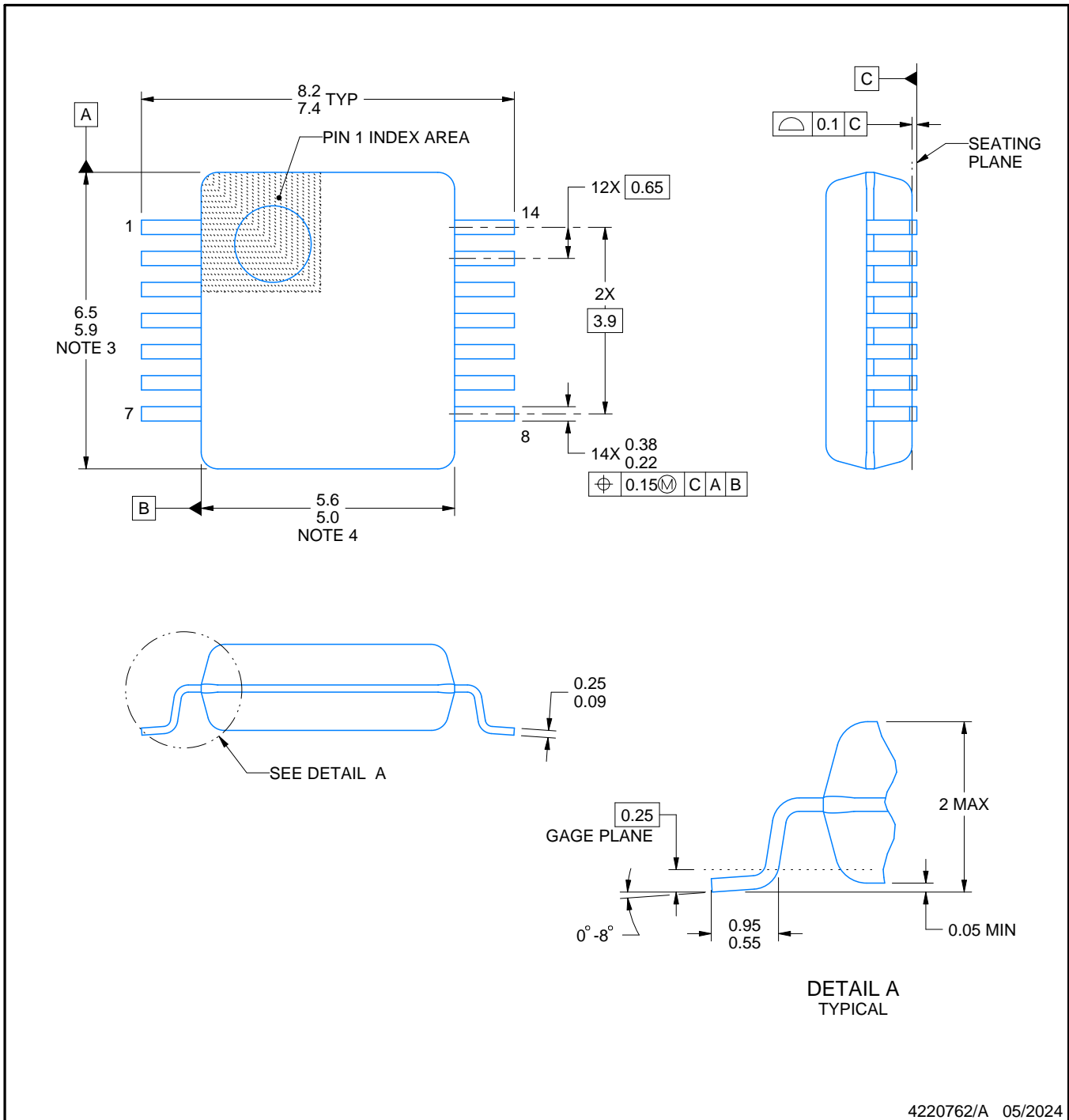
DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

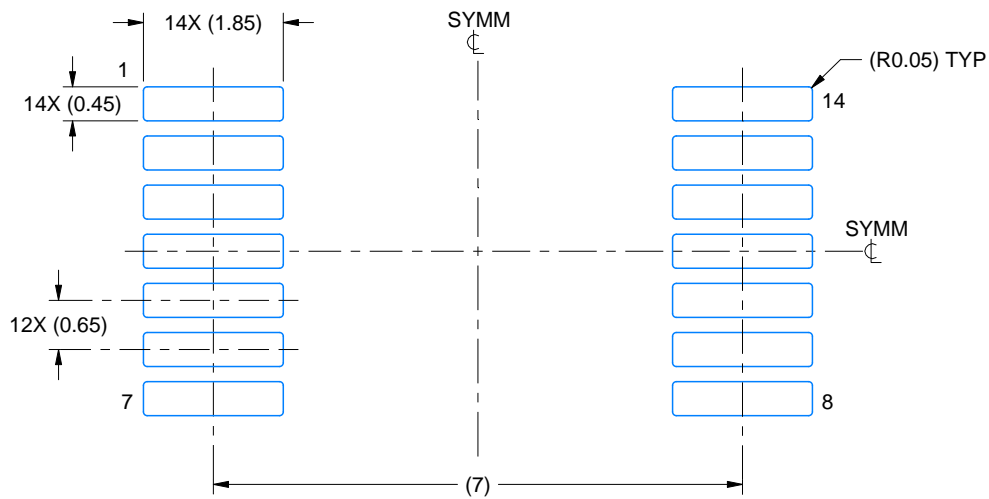
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

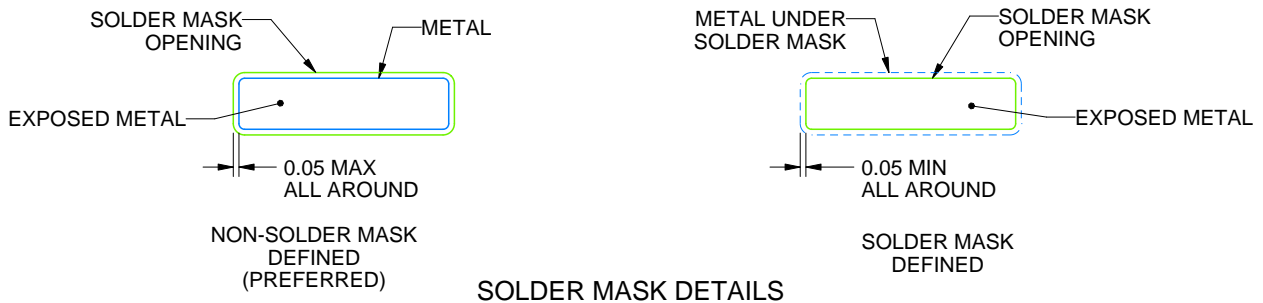
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

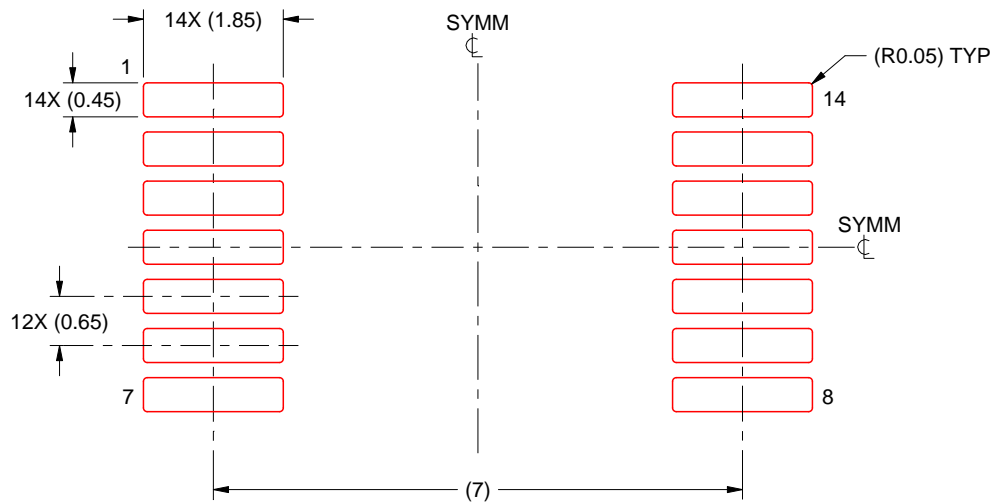
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

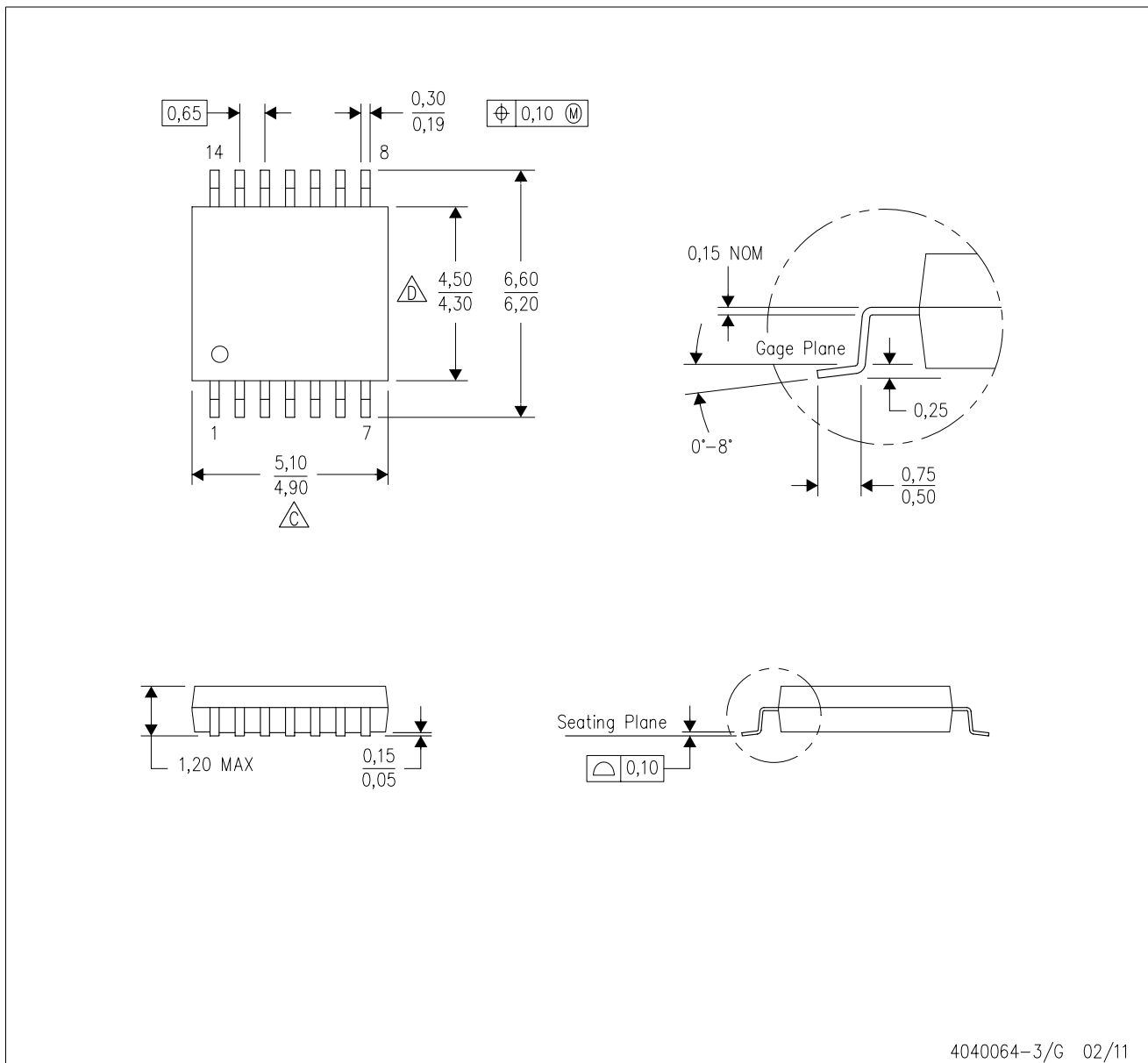
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LVU04AD](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management