THE DATASHEET OF

EVAL1ED44176N01FTOBO1

Low-side driver with over-current protection and fault/enable

1ED44176N01F Technical description

About this document

Scope and purpose

This application note describes the features and key advantages of using Infineon's 1ED44176N01F gate driver. This document will help the designer use the device within the recommended operating range by explaining how to select the current-sensing shunt resistor (RCS), resistor and capacitor (RC) filter for over-current protection (OCP) and short-circuit protection (SCP), fault clear time capacitor, and how to design the interfacing circuitry with the controller. In this application note we will explain the benefits of using 1ED44176N01F by showing the potential cost savings and increased power density capability.

Intended audience

This document is intended for people who would like an introduction to 1ED44176N01 and for designers who are looking to reduce their system cost and space while increasing the power density of their design.

Table of Contents

1 Product overview

1.1 Internal block diagram and features

Figure 1 illustrates the internal block diagram of the 1ED44176N01F.

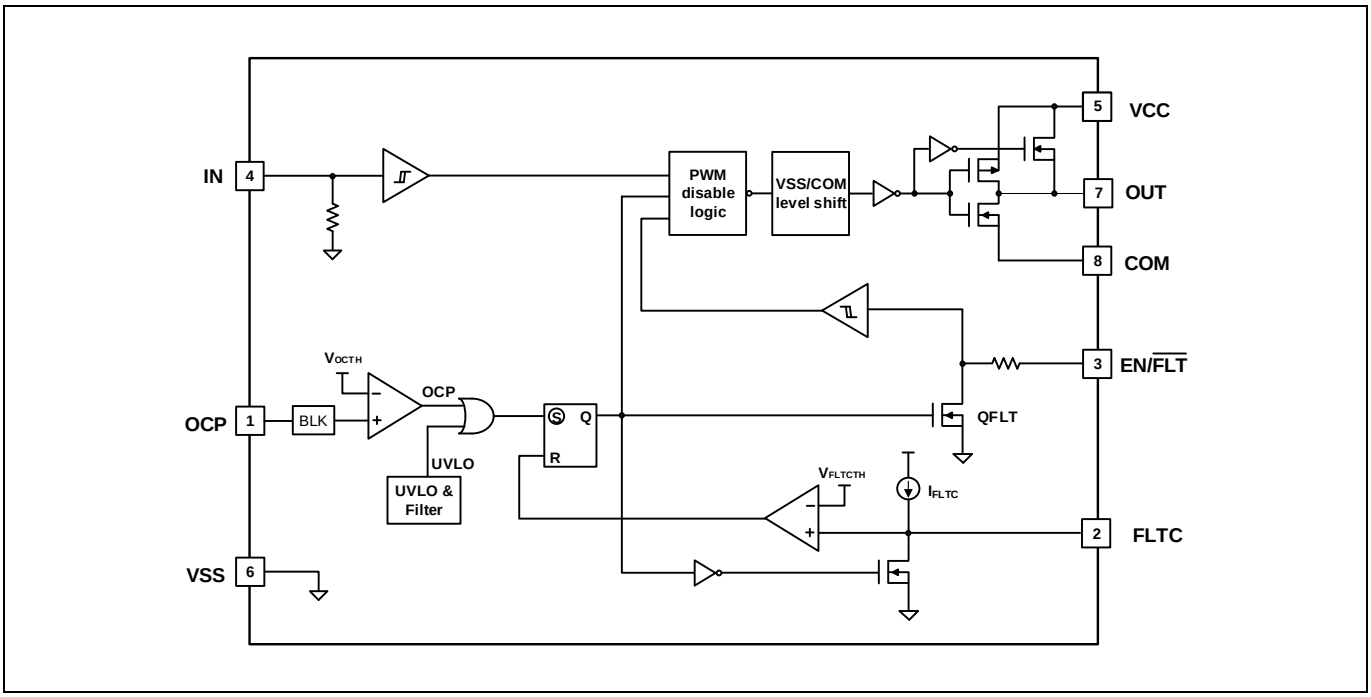


Figure 1 Internal block diagram

1.2 The detailed features and integrated functions of 1ED44176N01F

1.2.1 Features

- Over-current detection with positive voltage input
- 0.5 V over-current threshold with accurate ±5% tolerance at 25 °C
- Dedicated pin for fault output and enable
- Programmable fault clear time
- Under voltage lockout
- CMOS Schmitt-triggered inputs
- 3.3 V, 5 V and 15 V input logic compatible
- Output in phase with input
- Separate logic and power ground
- 2kV ESD HBM

1.2.2 Functions

- OC shutdown
- UVLO
- Fault output and enable
- The switch turns off during protection

- Active-high input signal logic

1.3 Maximum electrical ratings

Table 1 Detailed description of absolute maximum ratings

Symbol	Definition		Min.	Max.	Units
V_{CC}	Fixed supply voltage		– 0.5	25	V
V_O	Output voltage (OUT)		COM - 0.5	VCC + 0.5	
V_{OCP}	Voltage at current sense pin (OCP)		– 0.5	VCC +0.5	
$V_{EN/\overline{FLT}}$	Voltage at enable and fault reporting pin ($EN/\overline{FLT}$)		– 0.5	VCC + 0.5	
V_{FLTC}	Voltage at fault clear time program pin (FLTC)		– 0.5	VCC + 0.5	
V_{IN}	Logic input voltage (IN)		– 0.5	VCC + 0.5	
COM	Driver return voltage		– 5	VCC + 0.5	
P_D	Package power dissipation @ $T_A \leq 25°C$	PG-DSO 8-910	—	0.625	W
R_{thJA}	Thermal resistance, junction to ambient		—	200	°C/W
T_J	Junction temperature		– 40	150	°C
T_S	Storage temperature		– 55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Table 1: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS. The thermal resistance and power dissipation ratings are measured under board-mounted and still-air conditions.

1.4 Description of the input and output pins

Table 2 defines the 1ED44176N01F input and output pins. The detailed functional descriptions are as follows:

Table 2 Pin descriptions of 1ED44176N01F

Pin number	Pin name	Pin description
1	OCP	Current sense input
2	FLTC	Fault clear time program input
3	$EN/\overline{FLT}$	Enable and fault reporting pin, two functions: 1. Logic input to enable I/O functionality. I/O logic functions when ENABLE is high and enable function is not latched. 2. Fault reporting function like over-current or undervoltage lockout, this pin has negative logic and an open-drain output.
4	IN	Logic input for gate driver output (OUT), in phase
5	VCC	Supply voltage
6	VSS	Logic ground
7	OUT	Gate drive output
8	COM	Gate drive return

Over-current detection pin

Pin 1: OCP

- The R_{CS} should be connected between the pin (emitter of low-side IGBT or source of low-side MOSFET) and the power ground to detect short-circuit current (refer to Figure 5). An RC filter needs to be connected between the shunt resistor and the OCP pin if the internal blanking time is not enough to eliminate the noise.
- The integrated comparator is triggered if the voltage of the OCP pin (V_{OCP}) is higher than 0.5 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin $\mathrm{EN}/\overline{\mathrm{FLT}}$ is pulled down to low.
- The connection length between the R_{CS} and OCP pin should be minimized.

Fault clear timer

Pin 2: FLTC

- This is a programmable fault clear time pin. There is an internal current source to charge up the external capacitor (which is connected between FLTC and VSS pins) to program the fault clear time once the fault condition (UVLO or OCP) occurs.
- Once the fault condition occurs, the $\mathrm{EN}/\overline{\mathrm{FLT}}$ pin is internally pulled down to Vss. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ output stays in the low state until the fault condition has been removed and the fault clear timer expires.

Fault output and enable pin

Pin 3: $\mathrm{EN}/\overline{\mathrm{FLT}}$

- This is the fault output pin. An active low output is given on this pin for a fault state condition in the 1ED44176N01F. The fault conditions are OC detection and VCC under voltage operation.
- The $\mathrm{EN}/\overline{\mathrm{FLT}}$ output is open-drain configured. The $\mathrm{EN}/\overline{\mathrm{FLT}}$ signal line should be pulled up to the logic power supply (5 V or 3.3 V) with proper resistance.
- Externally pulling down the pin can disable the output. For normal operation, the pin needs to be pulled up.

Signal input pin

Pin 4: IN

- This is the pin to control the operation of the external device.
- It is activated by voltage input signals. The terminal is internally connected to a Schmitt-trigger circuit composed of 5 V- class CMOS.
- The signal logic of the pin is active-high. The device associated with the pin will be turned "ON" when a sufficient logic voltage is applied to the pin.
- The wiring of the input should be as short as possible to protect the 1ED44176N01F against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 3.

Bias voltage pin

Pin 5: VCC

- This is the control supply pin for the internal IC.

- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good quality filter capacitor with low equivalent series resistance (ESR) and low equivalent series inductance (ESL) should be mounted very close to this pin and VSS pin.

Common supply ground pin

Pin 6: VSS

- This pin connects the control ground for the internal circuit of the driver.

Gate drive output pin

Pin 7: OUT

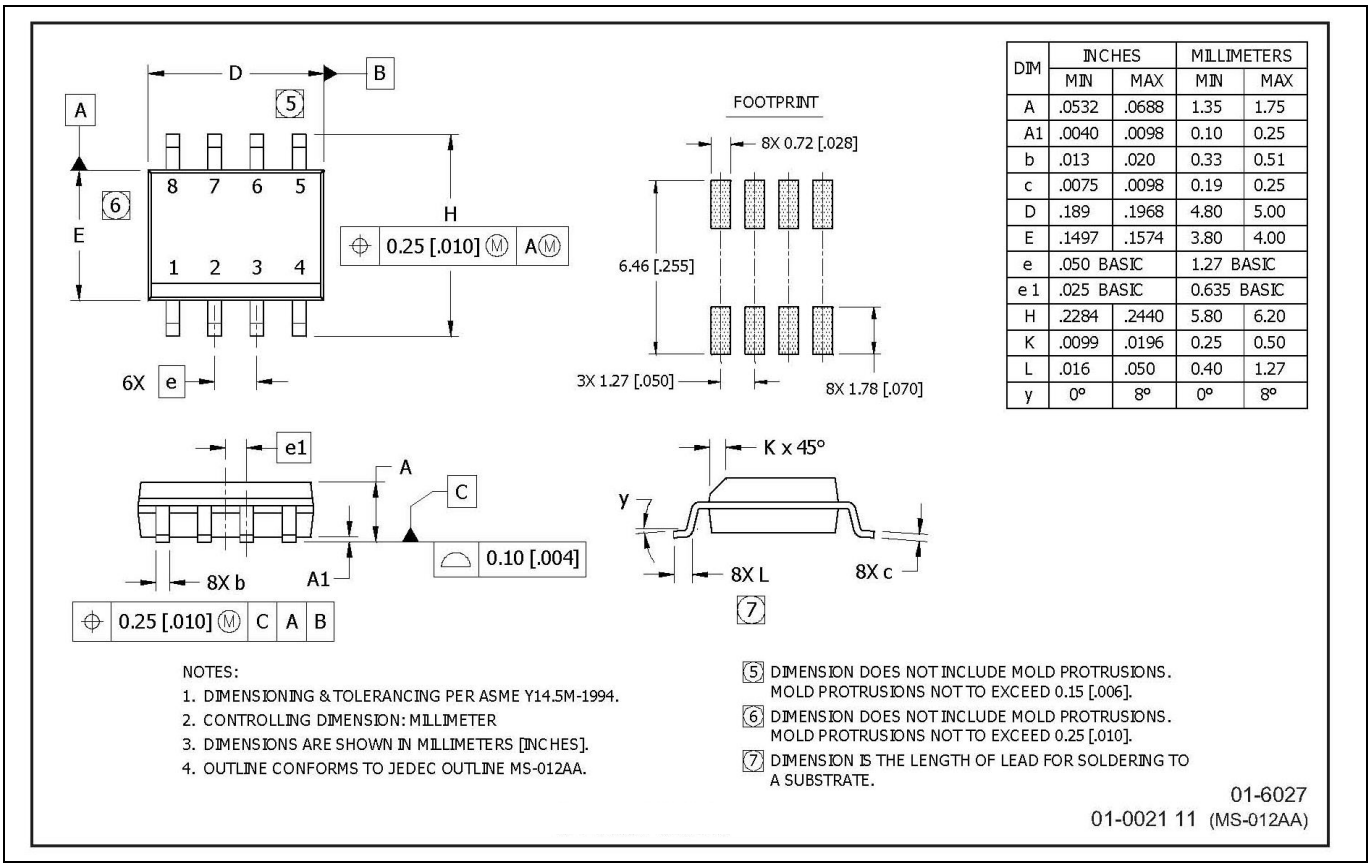
- The pin is connected to the gate of the IGBT or MOSFET by the gate resistor to turn the power device on or off.
- To prevent oscillations, a gate resistor is needed to be in series with the pin and the gate of IGBT or MOSFET.

Gate drive return pin

Pin 8: COM

- This pin connects the driver output return.

1.5 Outline drawings



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Figure 2 Package outline dimensions

2 Interface circuit and layout guide

2.1 Input/Output signal connection

Figure 3 shows the I/O interface circuit between a micro-controller (µC) or digital signal processing (DSP) and the 1ED44176N01F. The 1ED44176N01F input logic is active-high. The EN/$\overline{\text{FLT}}$ output is an open-drain configuration. This signal should be pulled up to high by an external logic power supply with a pull-up resistor. A 3.3k pull-up resistor is recommended if the external logic power supply is 3.3 V.

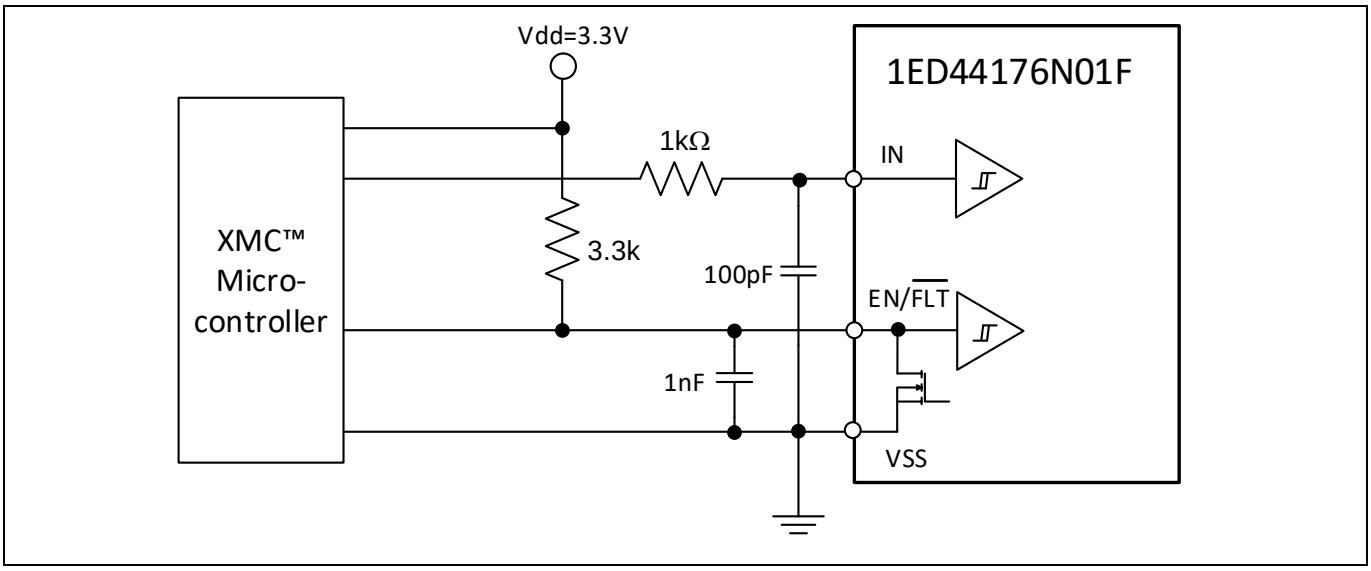


Figure 3 Recommended micro-controller I/O interface circuit

Table 3 Maximum ratings of IN and EN/$\overline{\text{FLT}}$ pins

Item	Symbol	Condition	Rating	Unit
Fixed supply voltage	VCC	Applied between VCC – VSS	25	V
Logic input voltage	IN	Applied between IN – VSS	-0.5 ~ VCC+0.5	V
Voltage at enable and fault reporting pin	EN/$\overline{\text{FLT}}$	Applied between EN/$\overline{\text{FLT}}$ – VSS	-0.5 ~ VCC+0.5	V

The input and fault output maximum rating voltages are listed in Table 3. Since the fault output is open-drain configured and its rating is VCC+0.5 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 3.3 V logic power supply which is similar to the input signals. It is also recommended to place bypass capacitors as close as possible to the EN/$\overline{\text{FLT}}$ and VSS pins.

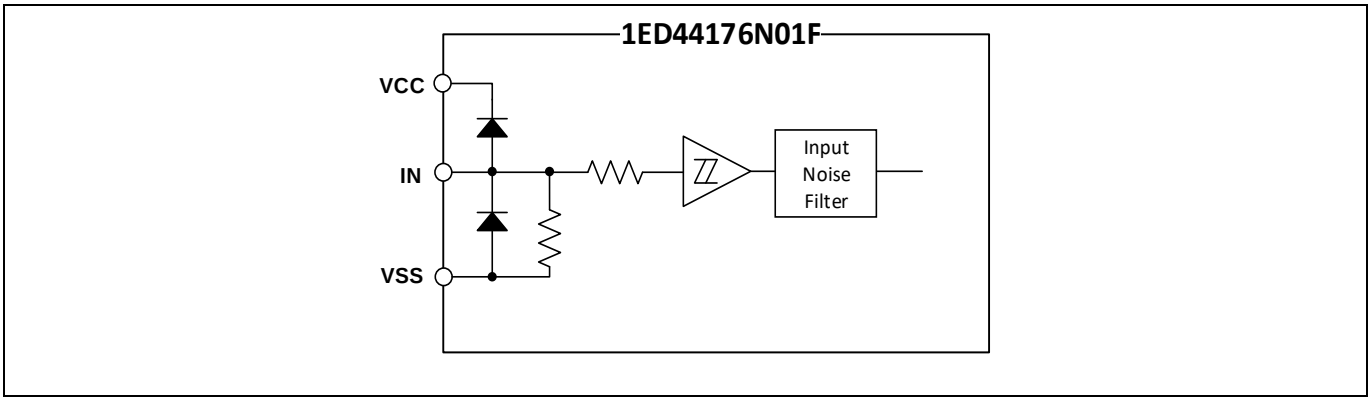


Figure 4 Simplified input structure diagram of 1ED44176N01F

The 1ED44176N01F input pin is internally clamped to VCC and VSS by diodes, it also includes a pull-down resistor, an input Schmitt-trigger and a noise filter for better noise immunity. The input pin has the capability to process input voltage up to supply voltage of the driver and it is also compatible with 3.3 V µC or DSP. Table 4 shows the logic input threshold.

Table 4 Input threshold voltage (at VCC = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (IN)	V_{INH}	IN – VSS	1.7	2.1	2.5	V
Logic "0" input voltage (IN)	V_{INL}		0.8	1	1.2	V

As shown in Figure 4, the 1ED44176N01F input signal section integrates a pull-down resistor. Therefore, when using an external filtering resistor between the micro-controller output and 1ED44176N01F input, pay attention to the signal voltage drop at the 1ED44176N01F input terminal. It should fulfill the logic "1" input voltage requirement. For instance, R = 1 kΩ and C = 100 pF are recommeded for the parts shown in Figure 3.

2.2 General interface circuit example

Figure 5 shows a typical application circuit of 1ED44176N01F for the interface schematic with control signals connected directly to a XMC™ µC.

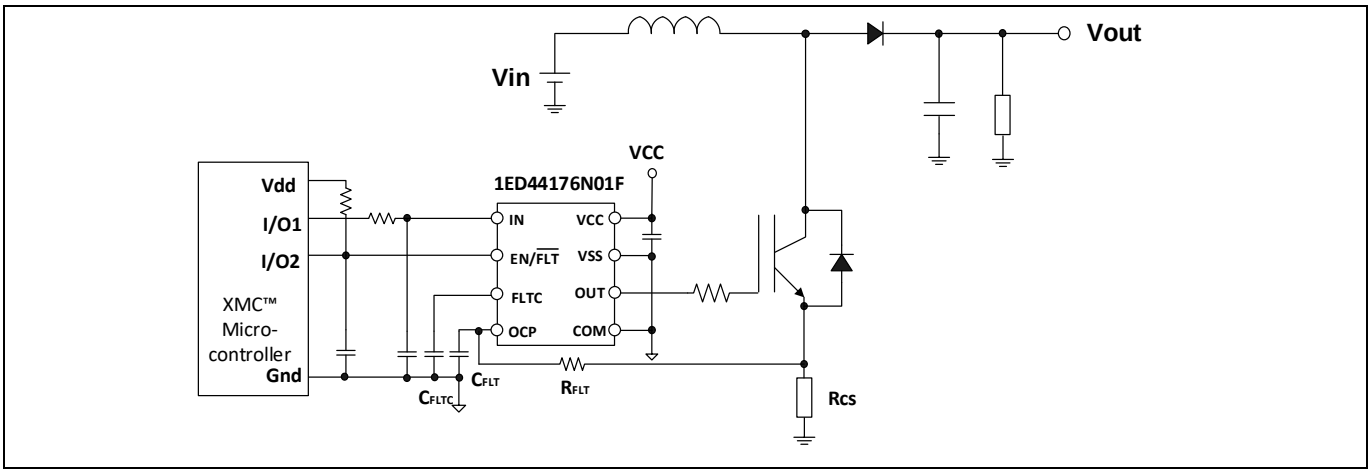


Figure 5 Application circuit example of active power factor correction (APFC) with R_{CS} for OCP

Note:

1. *The input signal is active-high configured. There is an internal pull-down resistor from the input signal line to VSS. When employing an RC coupling circuit between micro-controller and 1ED44176N01F, the RC values should be properly selected so that the input signal is compatible with the 1ED44176N01F logic "1"/logic "0" input voltages.*
2. *To avoid malfunction, the wiring of the input should be as short as possible (less than 2-3 cm).*
3. *The input of 1ED44176N01F can be directly connected to the micro-controller terminal without any opto-coupler or transformer isolation.*
4. *$EN/\overline{FLT}$ output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V or 3.3 V logic power supply with a pull-up resistor. When positioning the RC filter, a close location to 1ED44176N01F is recommended.*

5. *An internal current source in FLTC pin charges C_{FLTC} to program the fault clear time when the fault condtion occurs. C_{FLTC} wiring should be placed as close to FLTC and VSS pins as possible.*
6. *To prevent protection function errors, the R_{FLT} and C_{FLT} wiring between OCP and power ground should be as short as possible. C_{FLT} wiring should be placed as close to OCP and VSS pins as possible.*
7. *Each capacitor should be mounted as close to the pins of the 1ED44176N01F as possible.*
8. *Separate the output return ground from input logic ground to avoid noise coupling of the logic input pins.*
9. *It is recommended to connect the gate output return to COM and connect the ground pin of the micro-controller to the VSS pin.*

2.3 Recommended layout pattern for over-current protection (OCP) & short circuit protection (SCP) functions

As shown in Figure 6, it is recommended that the OCP filter capacitor connections to the 1ED44176N01F pins be as short as possible. The OCP filter capacitor should be connected to the VSS pin directly without overlapping the driver OUT return ground pattern. It is also recommended to keep the current sense loop, which is shown in Figure 6, as small as possible for better noise immunity. External current-sensing resistors are applied to detect over-current. A high ESL R_{CS} or a long wiring pattern between the R_{CS} and low side IGBT will cause excessive surges that might damage the 1ED44176N01F and current detection components. This may also distort the sensing signals. To decrease the parasitic inductance, the wiring between the R_{CS} and emitter of low side IGBT should be as short as possible. **Low ESL film resistors** are strongly recommended for the **R_{CS}**.

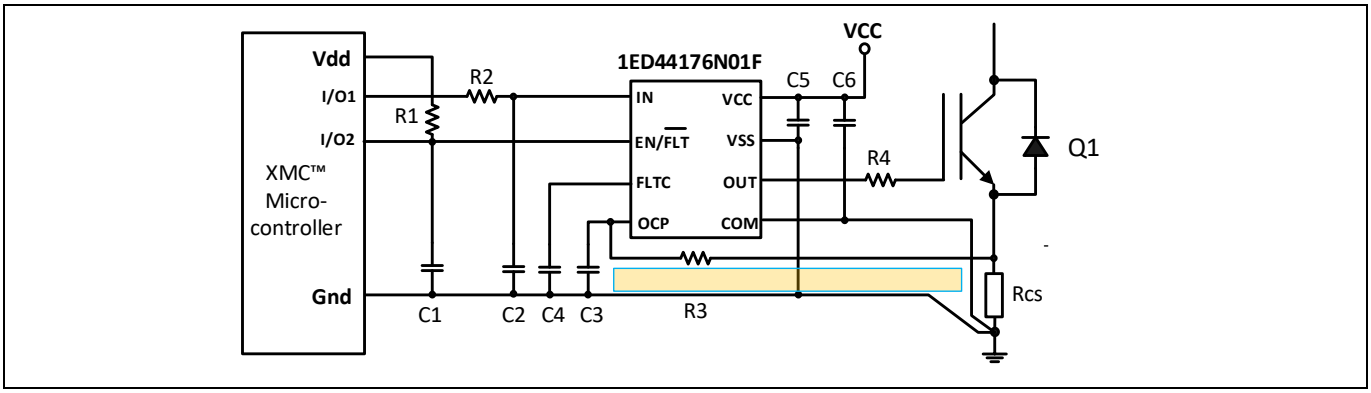


Figure 6 Recommended layout pattern for OCP & SCP function

2.4 Recommended wiring of the bypass capacitors

It is recommended to place two low ESL ceramic bypass capacitors (C5/C6) about 1µF, one (C5) connected between VCC and VSS, the other (C6) connected between VCC and COM directly. Also connect the ground of the capacitor (C1~C4) to VSS. Finally connect VSS, COM and µC signal ground at R_{CS}. The signal ground and power ground at R_{CS} are connected at only one point. It is also recommended to keep the driver output return loop, which is shown in Figure 7, as small as possible.

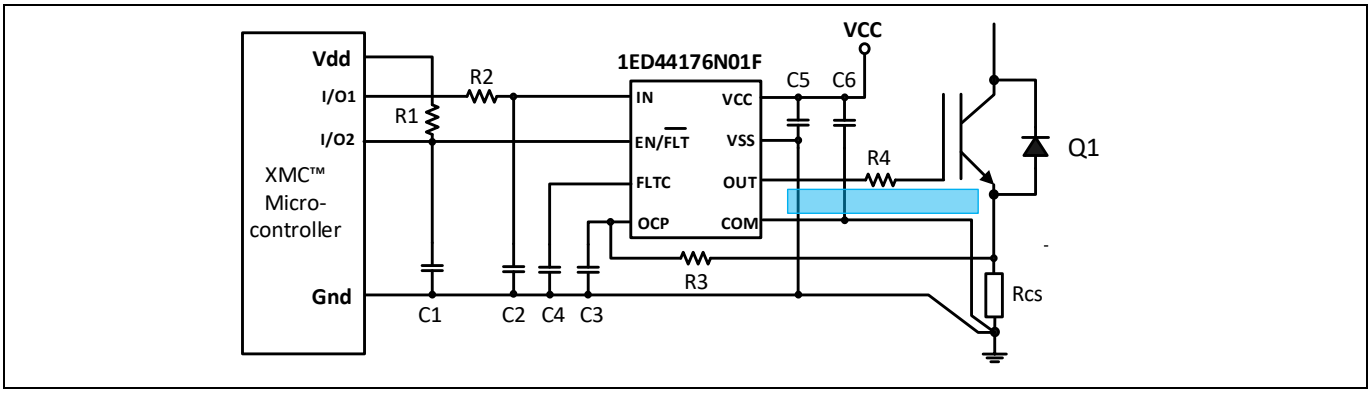


Figure 7 Recommended wiring of bypass capacitors

2.5 Recommended PCB layout

Proper PCB layout is important in high-current, fast-switching circuits to provide proper device operation and robustness of the design. Improper component and placement may cause errant switching, excessive voltage ringing, or circuit latch-up.
Here is the recommended PCB layout:

1. PCB trace loop area and inductance must be minimized.
   - This is accomplished by placing the 1ED44176N01F directly at the power switch (IGBT/MOSFET).
   - Placing the bypass capacitor (C5/C6) directly at the 1ED44176N01F.
   - Locating ground planes or ground return traces directly above or beneath 1ED44176N01F can reduce trace inductance.
2. A ground plane also helps as a radiated noise shield and provides some heat sinking for power dissipated within the device.
3. **Separate the gate output return ground from input logic ground to avoid noise coupling of the logic input pins.**

Figure 8 is the example of the PCB layout for the schematic of Figure 7.

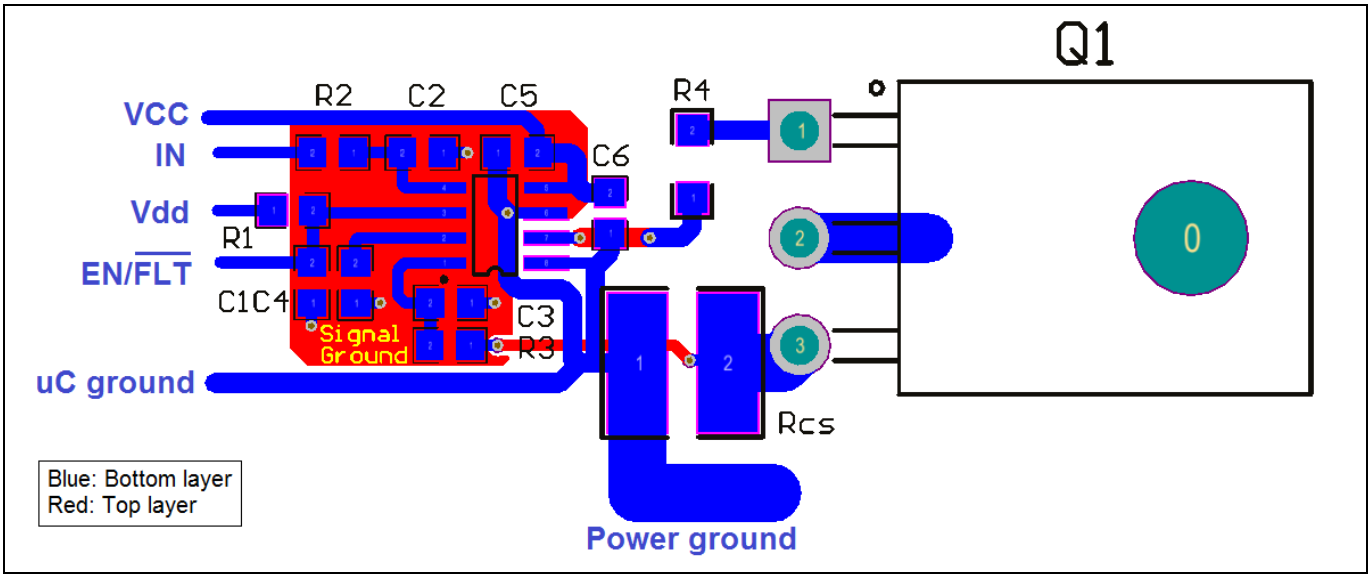


Figure 8 Example of the PCB layout for the schematic of Figure 7

3 Protection features

3.1 Undervoltage lockout protection (UVLO)

The 1ED44176N01F has an internal UVLO protection feature on the VCC pin supply circuit blocks. Table 5 shows the UVLO threshold.

Upon power-up, if the VCC voltage fails to reach the V_{CCUV+} threshold, the driver cannot turn on. Additionally, if the VCC voltage decreases below the V_{CCUV-} threshold and the VCC bias voltage remains lower than the V_{CCUV-} threshold exceeding UVLO filter time (t_{VCCUV}) during operation, the undervoltage lockout circuitry will recognize a fault condition and shut-down the drive output. The EN/$\overline{FLT}$ will then transit to the low state to inform the controller of the fault condition, regardless of the status of the IN input pin. The t_{VCCUV} about 2µs helps to suppress noise from the UVLO circuit, so that negative-going voltage spikes at the supply pin will avoid parasitic UVLO events.

Table 5 VCC UVLO threshold voltage (at VSS = COM, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vcc supply undervoltage positive-going threshold	V_{CCUV+}	Applied between VCC – VSS	11.2	11.9	12.7	V
Vcc supply undervoltage negative-going threshold	V_{CCUV-}		10.7	11.4	12.2	
Vcc supply undervoltage lockout hysteresis	V_{CCUVH}		—	0.5	—	

When VCC is higher than V_{CCUV+} and longer than t_{FLTC}, EN/$\overline{FLT}$ becomes high and the OUT will follow the input signal IN. (Figure 9 shows the UVLO time is shorter than t_{FLTC}.)

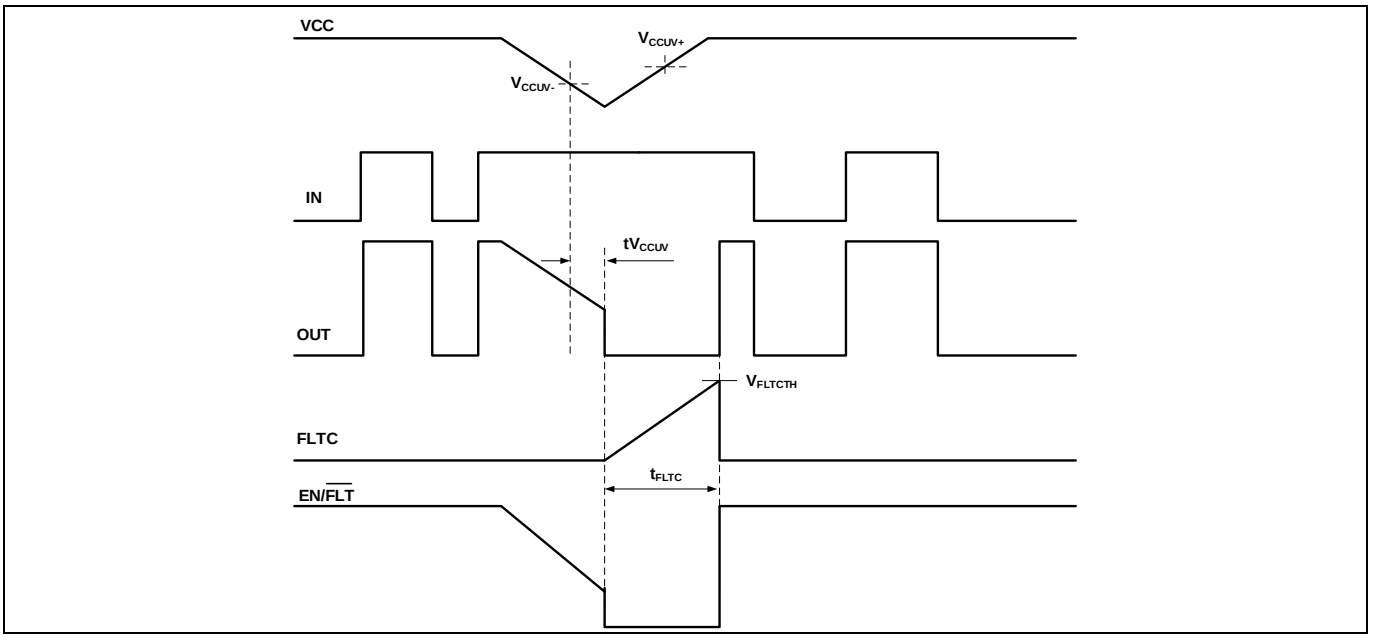


Figure 9 Vcc under voltage protection case one

Once EN/$\overline{\text{FLT}}$ enters UVLO mode, EN/$\overline{\text{FLT}}$ keeps low until t_{FLTC} is over and VCC supply voltage higher than V_{CCUV+}. (Figure 10 shows the UVLO time is longer than t_{FLTC}.)

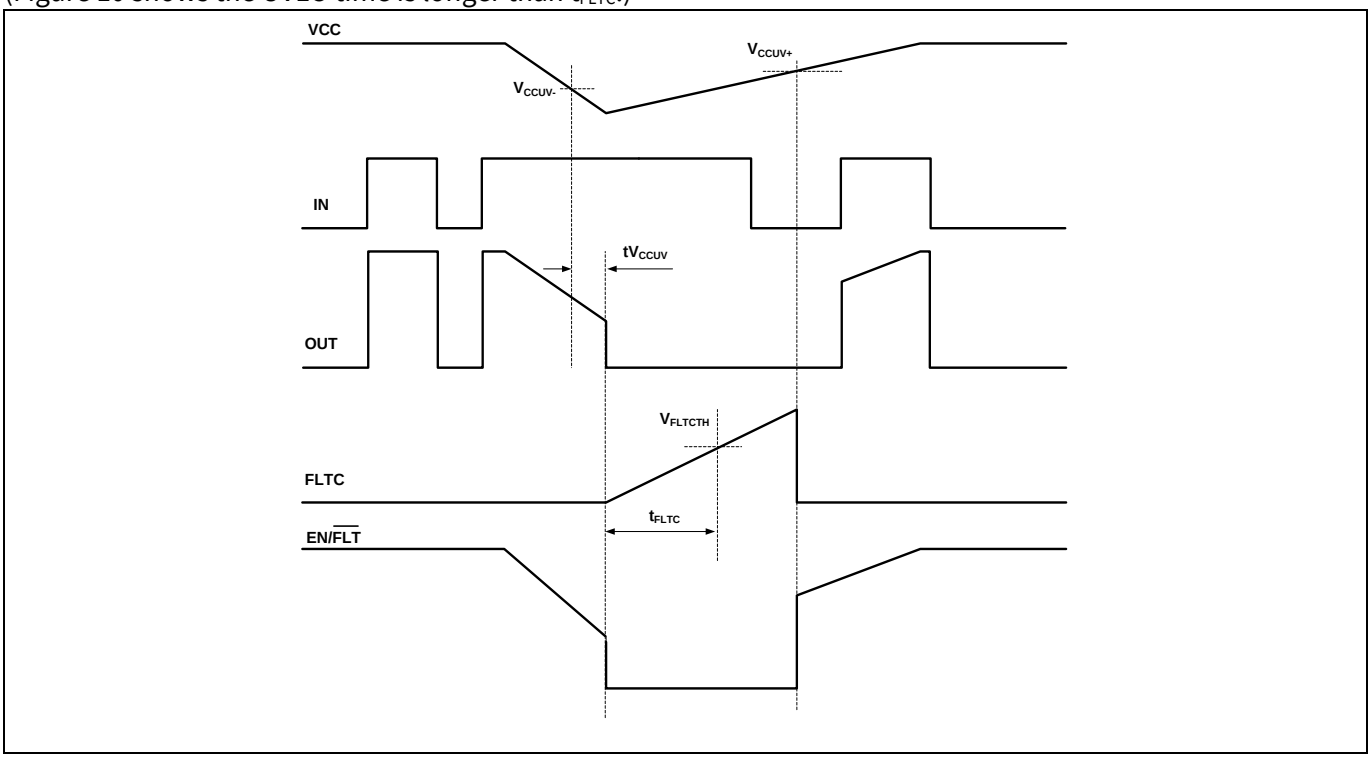


Figure 10 Vcc under voltage protection case two

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power device could be driven with a low voltage, resulting in the power device conducting current while the channel impedance is high. This could result in very high conduction losses within the power device and could lead to power device failure.

The VCC power for the 1ED44176N01F is normally provided by a single 15 V supply that is connected to the VCC and VSS terminals. The VCC power supply should be well filtered with a low impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the 1ED44176N01F's pins.

High-frequency noise on the supply might cause the internal control circuit to malfunction and to generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ±1 V. The potential at the 1ED44176N01F's VSS terminal is different from the emitter of low-side IGBT terminal by the voltage drop across the current-sensing resistor. It is very important that all control circuits and power supplies are referred to this point and not to the low-side IGBT emitter terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (VSS) a ground plane in the PCB layout.

3.2 Overcurrent protection (OCP)

3.2.1 Timing chart of OCP

The 1ED44176N01F has an OC shutdown function. Its internal comparator monitors the voltage of the OCP pin. If this voltage exceeds the OCP threshold (V_{OCTH}), which is specified in Table 6, a fault signal is activated and the OUT is turned off. The tolerance of the OCP threshold is ±5%; it keeps the accurate OCP in the system design.

Table 6 Current limit threshold voltage (at VCC = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current limit threshold voltage	V_{OCTH}	OCP – VSS	475	500	525	mV

Typically the maximum short-circuit current magnitude of the IGBT is gate-voltage dependent. A higher gate voltage results in a larger short-circuit current. Generally the maximum over-current trip level is set to below 2 times the nominal rated collector current. The over-current protection-timing chart is shown in Figure 11.

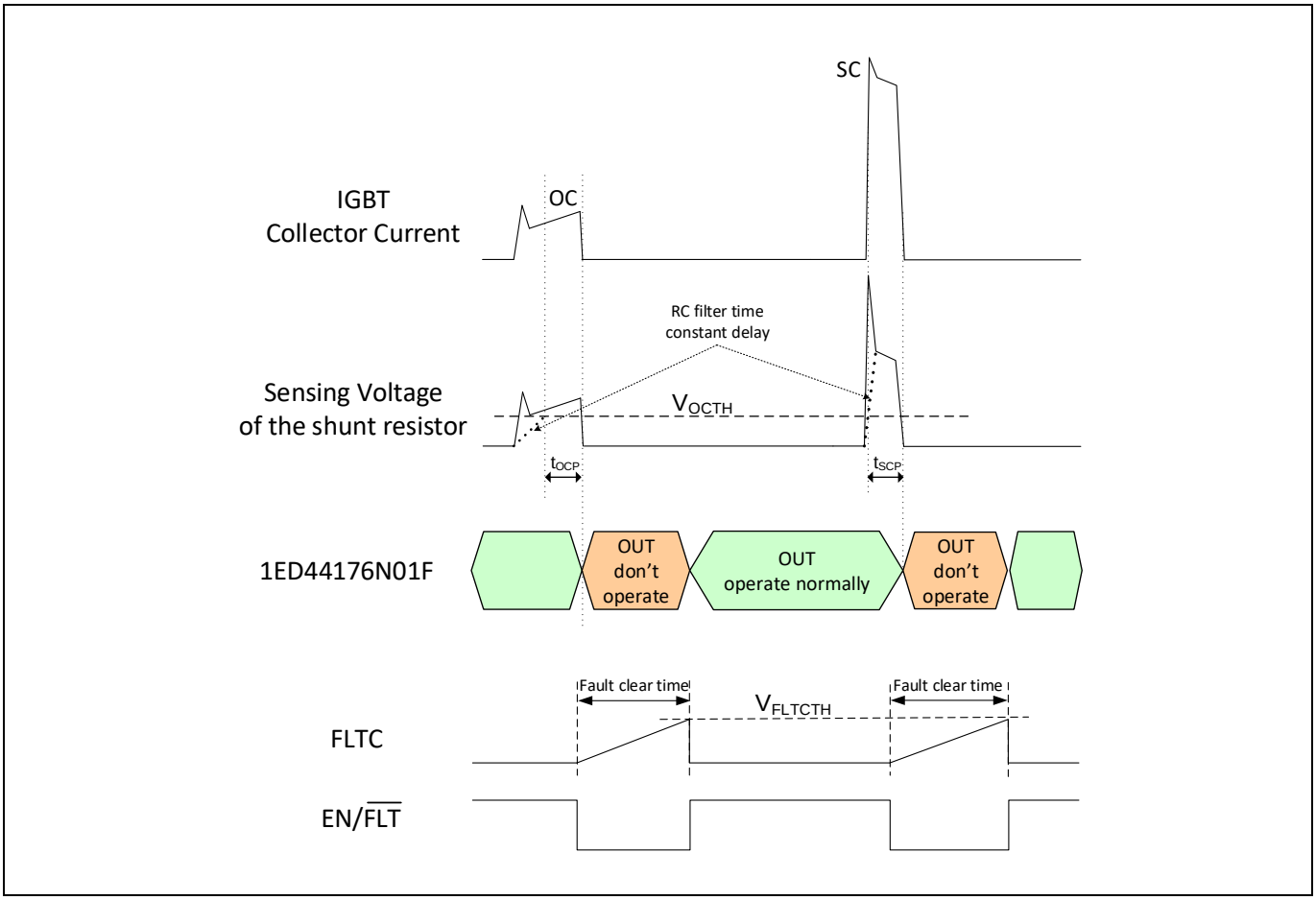


Figure 11 Timing chart of OCP

3.2.2 Selecting R_{CS}

The value of the R_{CS} is calculated by the following equation:

$$R_{SC} = \frac{V_{OCTH}}{I_{OC}} \quad (1)$$

where I_{OC} is the current of the over-current (OC) detection level.

The maximum value of the OC protection level should be set lower than the repetitive peak collector current in the datasheet considering the tolerance of R_{CS}.

For example, if the OCP is 25 A, thus, the recommended value of the R_{CS} is calculated as

$$R_{SC(min)} = \frac{0.5}{25} = 20\,m\Omega$$

For the power rating of the R_{CS}, the following list should be considered:

- Maximum load current (Irms)
- R_{CS} value at Tc=25 °C
- Power derating ratio of R_{CS} at T_C=100 °C according to the manufacturer's datasheet
- Safety margin

The R_{CS} power rating is calculated by the following equation:

$$P_{SC} = \frac{I_{rms}^2 \times R_{SC} \times margin}{derating\,ratio} \quad (2)$$

For example, If R_{SC}=20 mΩ:

- Max. load current: 4 A (rms)
- Power derating ratio of R_{CS} at T_C=100 °C : 80%
- Safety margin : 50%

$$P_{SC} = \frac{4^2 \times 0.02 \times 1.5}{0.8} = 0.6W$$

A proper power rating of R_{CS} is over 0.6 W, e.g. 1 W.

A proper resistance and power rating higher than the minimum value should be chosen considering the OCP level required in the application.

3.2.3 OCP delay time

The internal OCP blanking time ($t_{BLk,}$ Table 7 shows the specification) is necessary in the OC sensing circuit to prevent malfunction of the OCP caused by noise. If the blanking time is not sufficient to suppress the noise, an additional RC filter is necessary. The RC time constant is determined by considering the noise duration and the short circuit withstand time capability of the IGBT.

The sensing voltage on R_{CS} is applied to the OCP pin of 1ED44176N01F via the RC filter. The filter delay time (t_{FILTER}) that the input voltage of OCP pin rises to the OCP positive threshold voltage is caused by RC filter time constant.

In addition there is a shutdown propagation delay of OCP (t_{OCPDEL}, the time from OCP happening to output shutdown). Please refer to Table 8.

Table 7 Specification of OCP blanking time

Item	Min.	Typ.	Max.	Unit
Over current protection blanking time t_{BLK}	100	180	250	ns

Table 8 Specification of OCP to output shutdown propagation delay

Item	Min.	Typ.	Max.	Unit
OCP to output shutdown propagation delay t_{OCPDEL}	—	380	470	ns

Therefore the total delay time from OCP threshold (V_{OCTH}) to the shut down of the IGBT becomes:

$$t_{TOTAL} = t_{FILTER} + t_{OCPDEL} \quad (3)$$

Shut-down propagation delay is inversely proportional to the current rating, therefore the t_{TOTAL} is reduced at higher current conditions. The total delay must be less than the short-circuit withstanding time (t_{SC}) of the IGBT in the datasheet. If the t_{SC} =3 µs, the RC time constant should be set in the range of 1 µs. Recommended values for the filter components are R=680 Ω and C=1 nF.

3.3 Fault output circuit and fault clear time setup

The 1ED44176N01F provides a dedicated fault reporting output pin (EN/$\overline{FLT}$) and a programmable fault clear time pin (FLTC); see Figure 12. Once the fault condition occurs, the EN/$\overline{FLT}$ pin is internally pulled down to VSS. The EN/$\overline{FLT}$ output stays in the low state until the fault condition has been removed and the fault clear timer expires. Once the fault clear timer expires, the voltage on the EN/$\overline{FLT}$ pin will return to its external pull-up voltage.
The t_{FLTC} (see Figure 9) is programmed by external capacitor (C_{FLTC}) which is connected between FLTC and VSS. The t_{FLTC} is calculated by using the formula below:

$$t_{FLTC} = \frac{C_{FLTC} \times V_{FLTCTH}}{I_{FLTC}} \quad (4)$$

where V_{FLTCTH} is fault clear threshold voltage (Typ. 2.7 V), I_{FLTC} is fault clear sourcing current (Typ. 25 µA).

The sample of t_{FLTCLR} setup:

If C_{FLTC} =1 nF, then

$$t_{FLTC} = \frac{1nF \times 2.7V}{25uA} = 108us$$

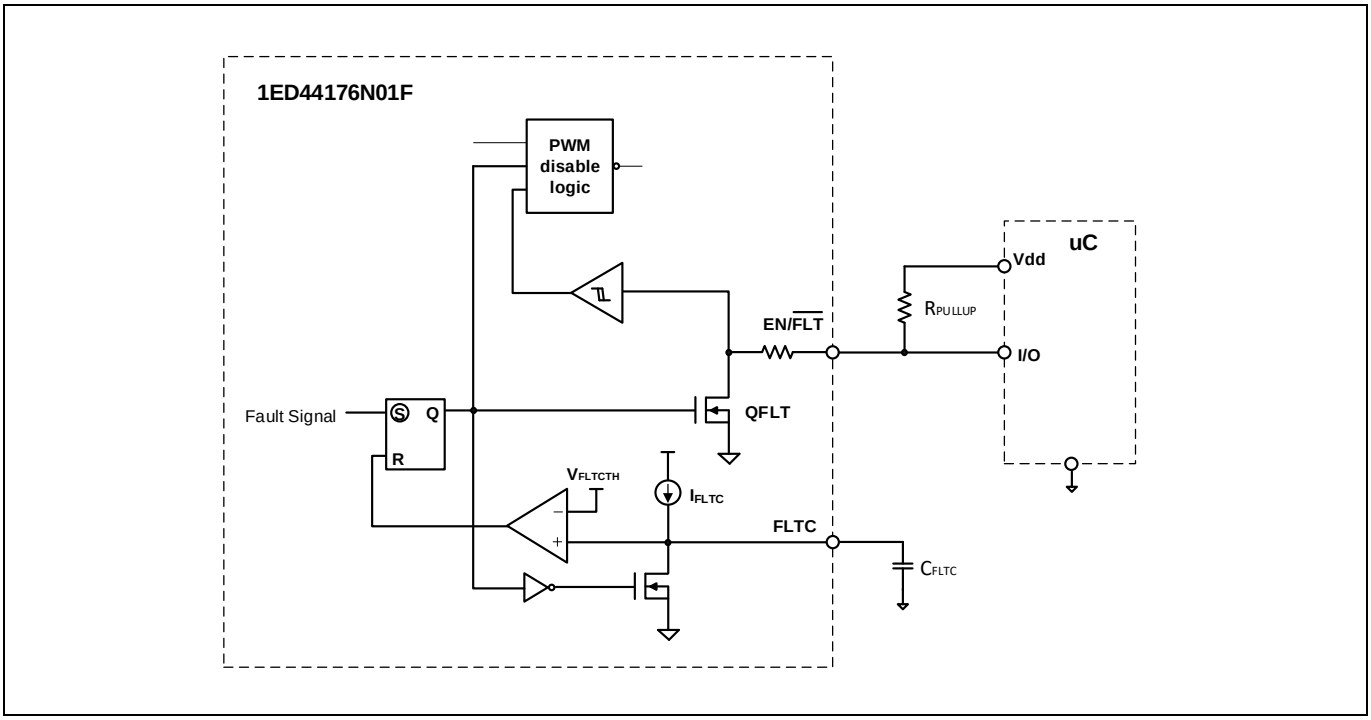


Figure 12 Diagram of the fault output circuit and fault clear time setup

3.4 Enable input circuit

1ED44176N01F provides an enable functionality that allows to shutdown or to enable the output. When EN/$\overline{\text{FLT}}$ is pulled up (the enable voltage is higher than V_{ENH}) the output is able to operate normally, pulling EN/$\overline{\text{FLT}}$ low (the enable voltage is lower than V_{ENL}) the output is disable. The enable function is not latched. See the threshold voltage of V_{ENH} and V_{ENL} in Table 9 and Figure 13.

Table 9 EN/$\overline{\text{FLT}}$ input threshold voltage (at VCC = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (EN/$\overline{\text{FLT}}$)	V_{ENH}	EN/$\overline{\text{FLT}}$ – VSS	1.7	2.1	2.5	V
Logic "0" input voltage (EN/$\overline{\text{FLT}}$)	V_{ENL}		0.8	1	1.2	V

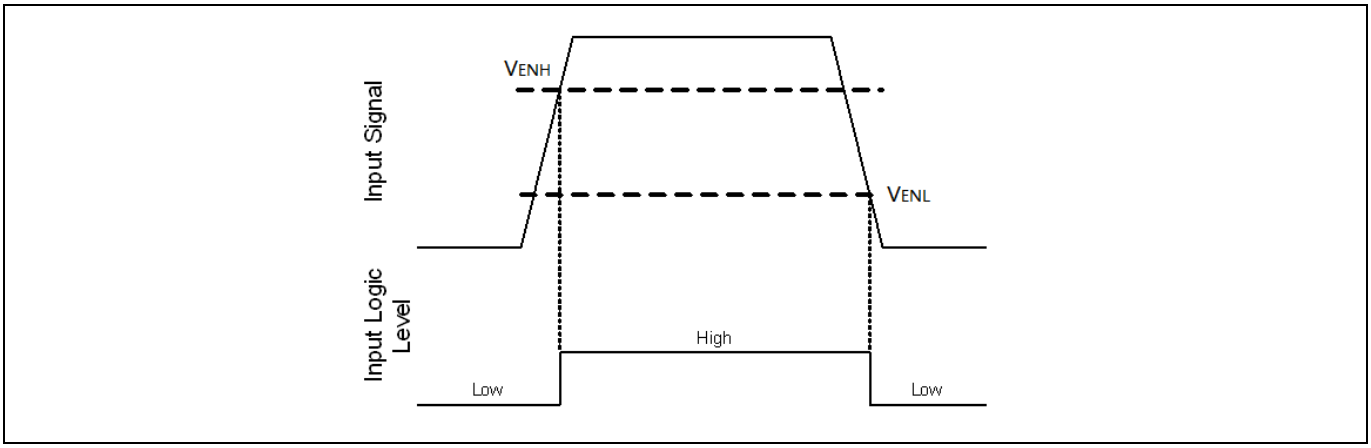


Figure 13 Enable input thresholds

The relationships between the input (IN), output (OUT) and enable (EN/ $\overline{\text{FLT}}$) signals of the 1ED44176N01F are illustrated below in Figure 14.

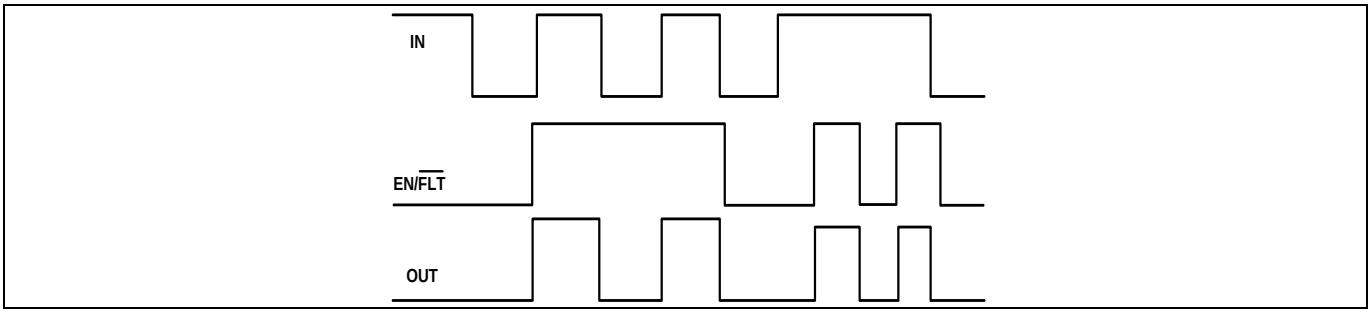


Figure 14 Input/output/enable pins timing diagram

From Figure 15, we can see the definitions of two timing parameters (t_{DISA} and t_{EN}) associated with this device. t_{DISA} is the delay time from enable signal pulling down to output shuting down. t_{EN} is the delay time from enable signal pulling up to output going high (when input is high). Please refer to Table 10. Because of the short propagation delay, EN/ $\overline{\text{FLT}}$ can be used as another input.

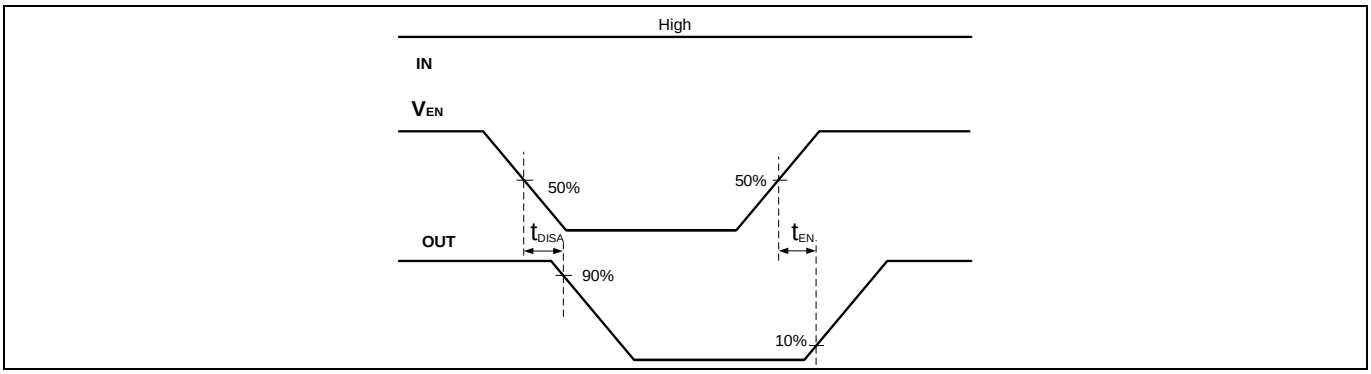


Figure 15 EN pin switching time waveform

Table 10 Specification of enable and disable delay time

Item	Min.	Typ.	Max.	Unit
Enable propagation delay t_{DISA}	—	50	95	ns
Disable propagation delay t_{EN}	—	50	95	

4 Driving capability

4.1 Io+ and Io-

When the 1ED44176N01F is used to drive the PFC switch, e.g. the IGBT, the sourcing current of 1ED44176N01F is designed smaller than the sinking current to optimize the trade off between the switching loss and the switching speed for EMI (see Table 11).This means the turn-on speed of the switch is lower than the turn-off speed if the same gate resistor is used.

Table 11 Io+ and Io-(at VCC = 15 V, T_J = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output sourcing short circuit pulsed current	Io+	V_O = 0 V PW ≤ 10 µs	0.56	0.8	—	A
Output sinking short circuit pulsed current	Io-	V_O = 15 V PW ≤ 10 µs	1.23	1.75	—	

5 Recommended related products

The 1ED44176N01F is able to drive up to 50 A/650 V IGBTs from Infineon at frequency up to 50 kHz for PFC applications. The power rating is up to 2 kW. If the higher frequency is required for the application,Infineon's CoolMOS™ C7 superjunction MOSFET is a good choice. Some parts of the IGBT, CoolMOS™ and rapid switching emitter-controlled diode from Infineon in PFC applications are recommended in Table 12,Table 13 and Table 14.Table 15 shows Infineon's CIPOS™Mini IPM with integrated PFC Stage.

Table 12 Infineon's TRENCHSTOP™ 3 IGBT and TRENCHSTOP™ 5 IGBT

Part Number	Voltage level	Type	Package	IC @ 100°C max	IC @ 25°C max
IKFW40N60DH3E	600 V	IGBT + Diode	PG-TO247-3-AI	NA	34 A
IKFW50N60DH3E	600 V	IGBT + Diode	PG-TO247-3-AI	NA	40 A
IKFW60N60DH3E	600 V	IGBT + Diode	PG-TO247-3-AI	NA	53 A
IKW30N65H5	650 V	IGBT+ Diode	PG-TO247-3	35 A	55 A
IKW40N65H5	650 V	IGBT+ Diode	PG-TO247-3	46 A	74 A
IKW50N65H5	650 V	IGBT+ Diode	PG-TO247-3	56 A	80 A

For more options visit www.infineon.com/IGBT

Table 13 Infineon's CoolMOS™ C7 superjunction MOSFET

Part Number	Voltage level	Package	RDS (on)	ID @ 25°C max	ID,pulse @ 25°C max
IPW(Z)65R019C7	650 V	PG-TO 247-3(4)	19 mΩ	75 A	496 A
IPW(Z)65R045C7	650 V	PG-TO 247-3(4)	45 mΩ	46 A	212 A
IPW(Z)65R065C7	650 V	PG-TO 247-3(4)	65 mΩ	33 A	145 A
IPW(Z)65R095C7	650 V	PG-TO 247-3(4)	95 mΩ	24 A	100 A
IPW65R125C7	650 V	PG-TO 247	125 mΩ	18 A	75 A
IPW65R190C7	650 V	PG-TO 247	190 mΩ	13 A	49 A

For more options visit www.infineon.com/MOSFET

Table 14 Infineons RAPID 1 diode

Part Number	Voltage level	Package	VF @ 25°C max	IF @ 100°C max	IF @ 25°C max
IDW30E65D1	650 V	PG-TO247-3	1.7 V (IF=30 A)	30 A	60 A
IDW40E65D1(E)	650 V	PG-TO247-3(-AI)	1.7 V (IF=40 A)	40 A	80 A
IDW60C65D1	650 V	PG-TO247-3	1.7 V (IF=30 A)	30 A	60 A
IDW80C65D1	650 V	PG-TO247-3	1.7 V (IF=40 A)	40 A	80 A

For more options visit www.infineon.com/rapiddiodes

Recommended related products

Table 15 Infineon's CIPOS™Mini IPM with integrated PFC Stage

Part Number	Voltage level	Type	Package	IC @ 25°C max (inverter IGBT)	PFC Working frequency
IFCM15S60GD	600 V	PFC and 3-phase inverter	Mini DCB	15 A	20 kHz
IFCM15P60GD	600 V	PFC and 3-phase inverter	Mini DCB	15 A	40 kHz
IFCM10S60GD	600 V	PFC and 3-phase inverter	Mini DCB	10 A	20 kHz
IFCM10P60GD	600 V	PFC and 3-phase inverter	Mini DCB	10 A	40 kHz

For more options visit www.infineon.com/IPM

6 References

1. [1] Datasheet of 1ED44176N01F, Rev 1.0

7 Revision history

Major changes since the last revision

Version number	Revision Date	Revision description
1.0	2018-05-15	Initial version

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Published by

Infineon Technologies AG

81726 Munich, Germany

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